Context Switching Simulator V.0

1. Given Verilog design files, a Verilog testbench, and the name of the module to be swapped.
2. Search for this module in the design.
3. Traverse down the design starting from this module.
4. Create a list containing all the state elements (registers and memories) in this module and all underlaying submodules recursively.
5. Once a SAVE signal is asserted, the current state elements' values will be saved in the list.
6. Then, these elements are corrupted (by writing X or zeros), and simulation continues until a RESTORE signal is asserted.
7. Once a RESTORE signal is asserted, the saved values are restored to the state elements.