CSE260 Lab Report

Experiment Name: Design and Implementation of 4-bit Parallel Binary Adder

Submitted by

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Name of the experiment:

Design and Implementation of 4-bit Parallel Binary Adder.

Objective:

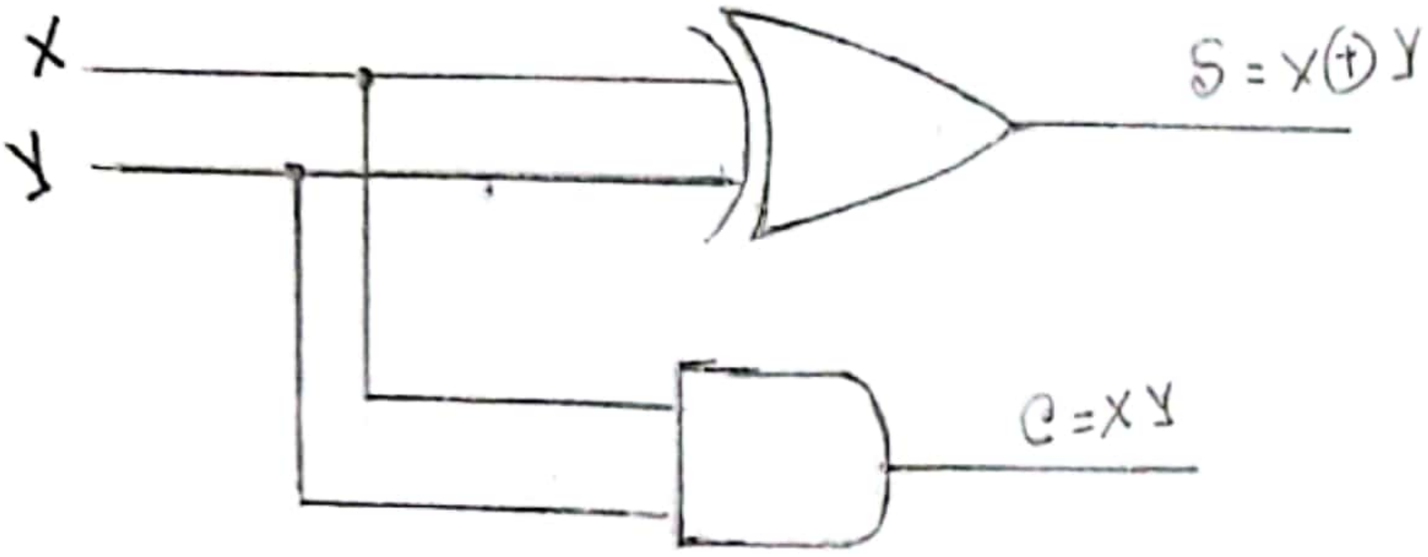
i) To observe the practical application of 4-bit parallel adder and a 4-bit full adder.

ii) In order to implement a half adder circuit and full adder circuit using X-OR gate, AND gate and OR gate.

Required Components and Equipment:

i) X-OR gate.
ii) AND gate.
iii) OR- gate.
iv) Logic state.
v) Led - Red.
vi) Ground.

Experimental Setup:



$S = X \oplus Y$

$C = XY$

Figure 1: Half Adder Circuit

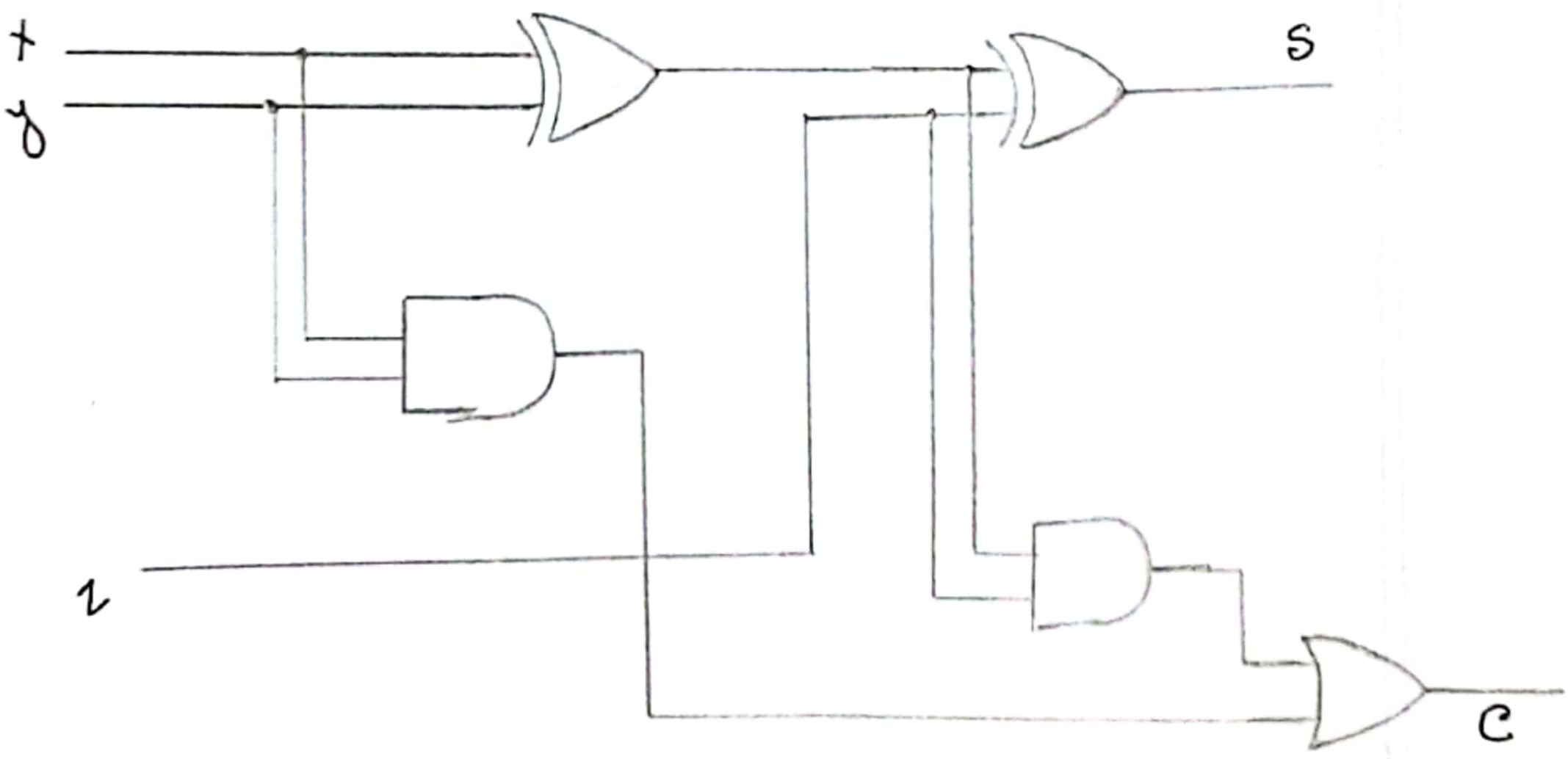
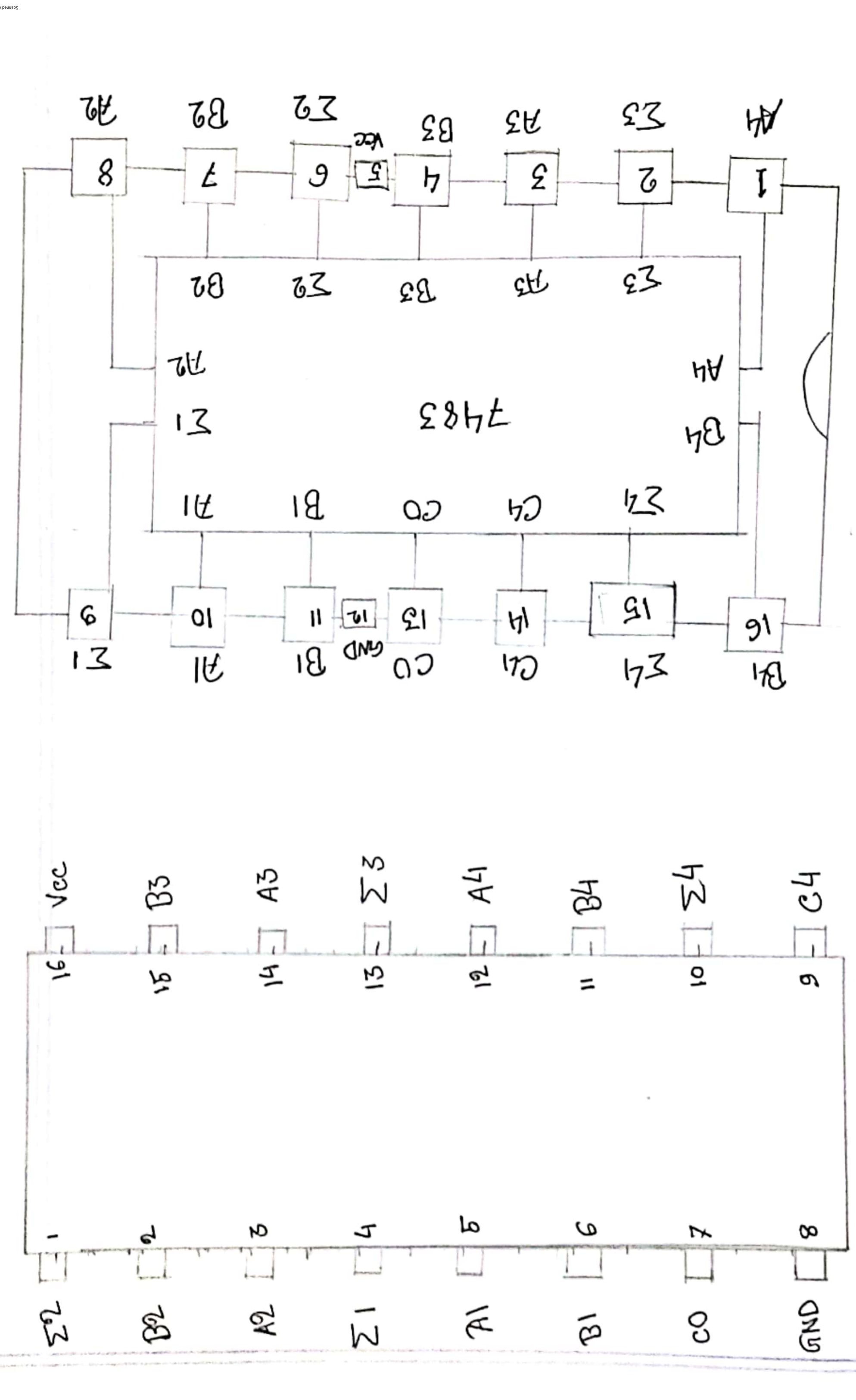
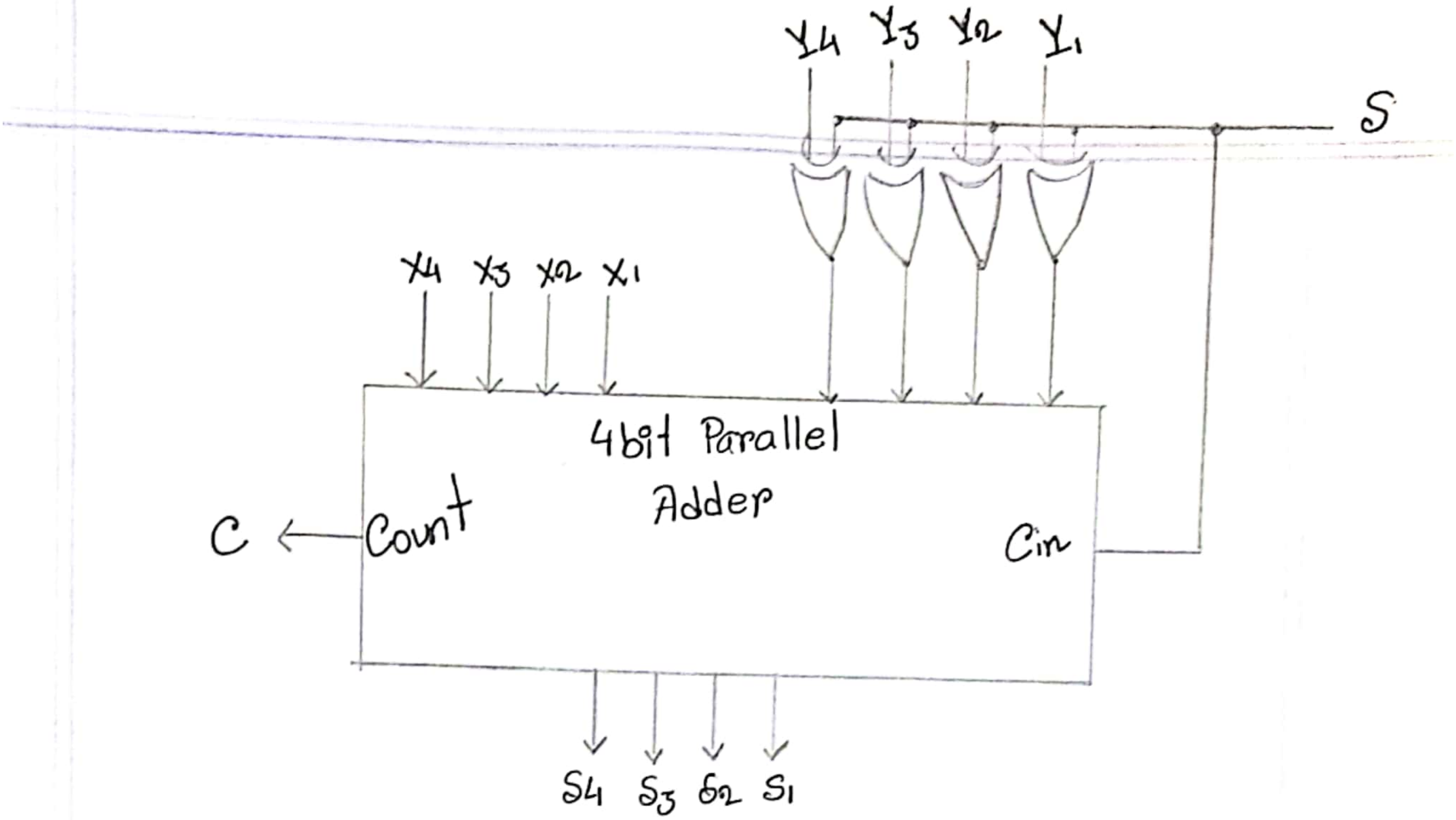


Figure 2: Full Adder Circuit





Truth Table:

Half Adder:

X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full-Adder :

X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Zebra :

$$S = X'Y'Z + X'YZ' + XY'Z' + XYZ$$

$$= X'(Y'Z + YZ') + X(YZ' + YZ)$$

$$= X'(Y \oplus Z) + X(Y \oplus Z)'$$

$$= X'(Y \oplus Z) + X(X \oplus Y \oplus Z)$$

$$= XY + Z(X \oplus Y)$$

$$= XY + Z(X \oplus Y)'$$

$$C = XY + XZ + YZ$$

Lab - Discussion:

This lab-work has taught me about half-adder and full--adder. In addition, I learnt how to use half adder and full-adder.