CSE260 Lab Report

Experiment Name: Parity Generator and Checker

Submitted by

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Section: 09

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Name of the Experiment:

Parity Generator and Checker.

Objective:

To design an implement an Even parity Generator and parity checker using X-OR gates. (IC- 7486)

Required Components and Equipments:

(i) AT-700 Portable Analog/Digital Laboratory.

(ii) 7400 x3

(iii) X-OR gate.

(iv) LOGIC STATE

(v) LOGIC PROBE (BIG)

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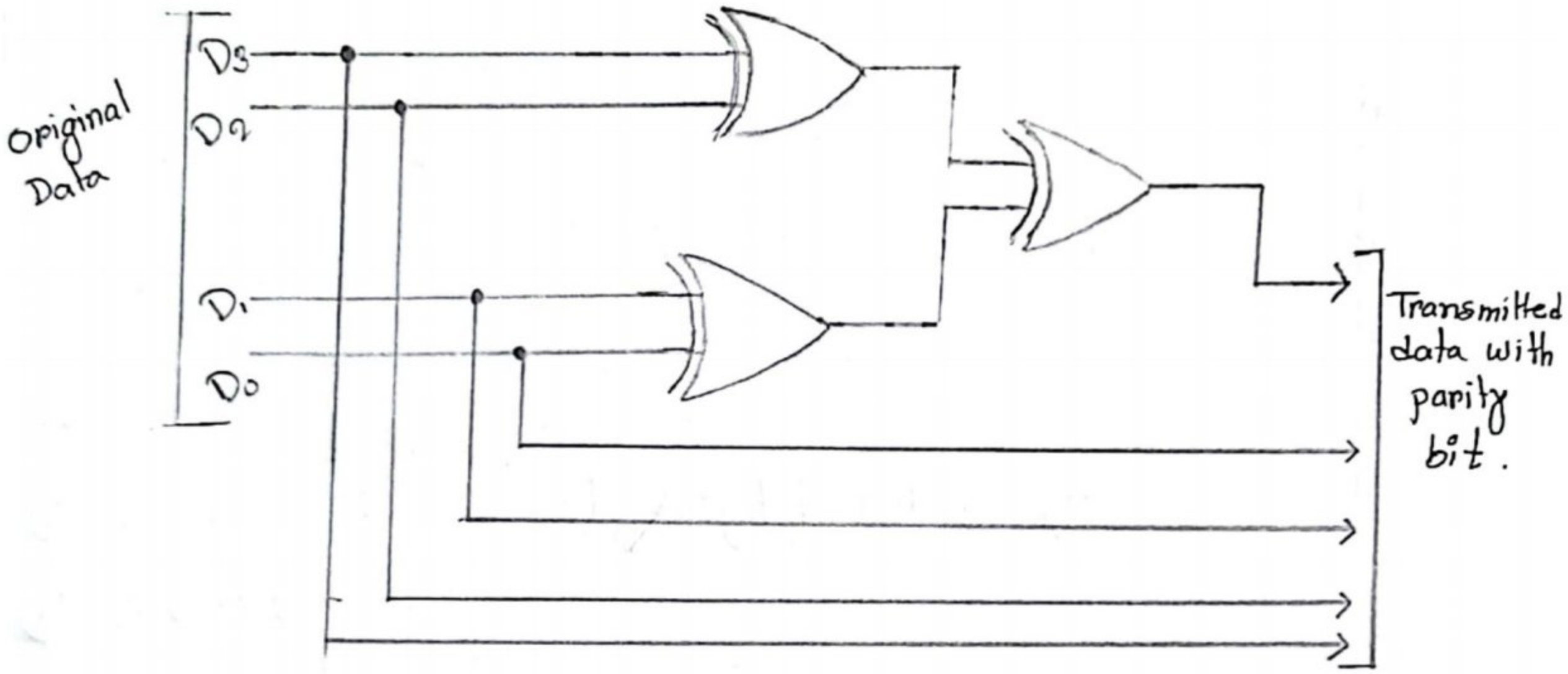
Diagram of Circuit :

Even Parity generator:



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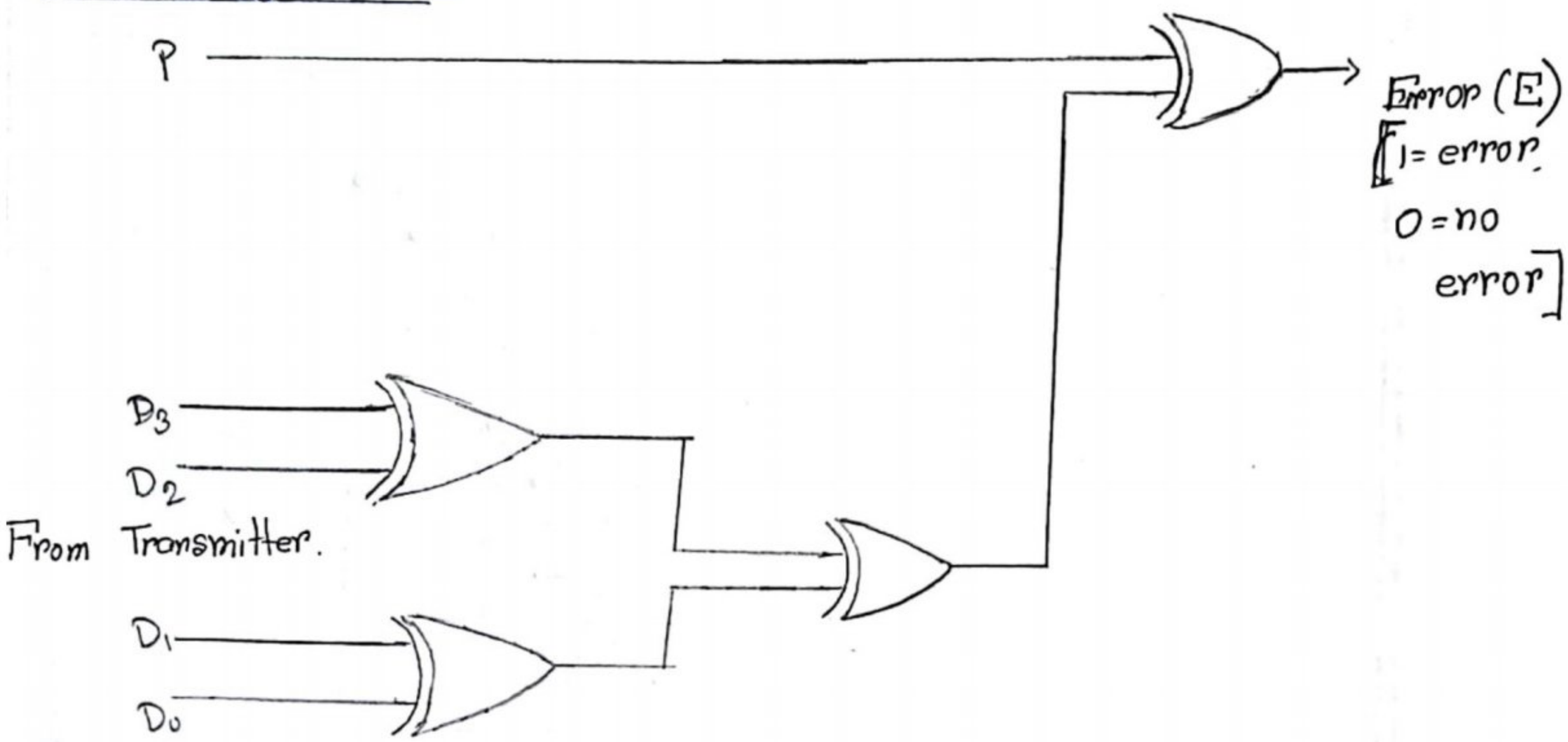
Even Parity Checker:



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Result of Truth Table :

Parity Generator :

D_3	D_2	D_1	D_0	$D_2\bar{D}_3 + \bar{D}_2 D_3$	$D_0\bar{D}_1 + \bar{D}_0 D_1$	A
0	1	1	1	1	0	1
1	0	0	1	1	1	0
0	0	0	0	0	0	0
0	1	0	0	1	0	1

Parity Checker :

P	D_3	D_2	D_1	D_0	$D_2\bar{D}_3 + \bar{D}_2 D_3$	$D_0\bar{D}_1 + \bar{D}_0 D_1$	A	$PA' + P'A$ (XOR
0	1	0	1	0	1	1	0	0
1	1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	0	0	1

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Sender's Parity	Reciever's Parity	X-OR
0	0	0
1	1	0
1	0	1
1	0	1

Discussion:

We already know that the output of an XOR gate is zero if the inputs are both zero. If this is not the case, the result will be 1. According to the truth table, the first two ~~output~~ outcomes are 0 and the last outcome is 1. Essentially, this means that there was no mistake in the first and the second set inputs and the XOR of the sender's parity and receiver's parity is equal to zero. After that, the output of the third and fourth input is 1. As a result, there were mistakes. If there is more than one bit change, the parity checking technique will not function properly.

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