

# Dual N-Channel 20 V (D-S) MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
20	0.198 at $V_{GS} = 4.5$ V	1.3 <sup>a</sup>	0.9 nC
	0.225 at $V_{GS} = 2.5$ V	1.3 <sup>a</sup>	
	0.263 at $V_{GS} = 1.8$ V	1.3 <sup>a</sup>	

## FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 %  $R_g$  Tested
- Typical ESD Protection 2100 V HBM
- Compliant to RoHS Directive 2002/95/EC

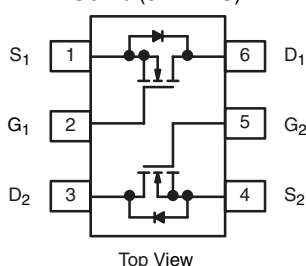


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

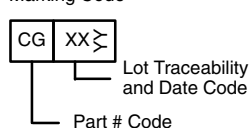
- Load Switch for Portable Applications

**SOT-363**  
SC-70 (6-LEADS)



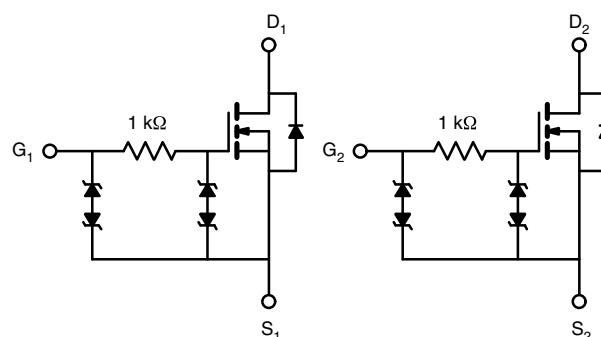
Top View

Marking Code



### Ordering Information:

Si1922EDH-T1-GE3 (Lead (Pb)-free and Halogen-free)



## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	$I_{DM}$	4	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	0.61 <sup>b, c</sup>
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	130	170	°C/W
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	80	100	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- Maximum under steady state conditions is 220 °C/W.

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		20		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 2.3		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.4		1	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 25	μA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 4.5 V			1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = 4.5 V	4			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1 A		0.165	0.198	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1 A		0.187	0.225	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 0.2 A		0.210	0.263	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 4 V, I <sub>D</sub> = 1.5 A		4		S
Dynamic <sup>b</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 8 V, I <sub>D</sub> = 1.5 A		1.6	2.5	nC
		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.5 A		0.9	1.8	
Gate-Source Charge	Q <sub>gs</sub>			0.1		
Gate-Drain Charge	Q <sub>gd</sub>			0.2		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.4	1.9	3.8	kΩ
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 8.3 Ω I <sub>D</sub> ≅ 1.2 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		43	65	ns
Rise Time	t <sub>r</sub>			80	120	
Turn-Off Delay Time	t <sub>d(off)</sub>			480	720	
Fall Time	t <sub>f</sub>			220	330	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 8.3 Ω I <sub>D</sub> ≅ 1.2 A, V <sub>GEN</sub> = 8 V, R <sub>g</sub> = 1 Ω		22	33	
Rise Time	t <sub>r</sub>			46	70	
Turn-Off Delay Time	t <sub>d(off)</sub>			645	968	
Fall Time	t <sub>r</sub>			215	323	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			1	A
Pulse Diode Forward Current	I <sub>SM</sub>				4	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.2 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.2 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		9	18	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			2	4	nC
Reverse Recovery Fall Time	t <sub>a</sub>			5		ns
Reverse Recovery Rise Time	t <sub>b</sub>			4		

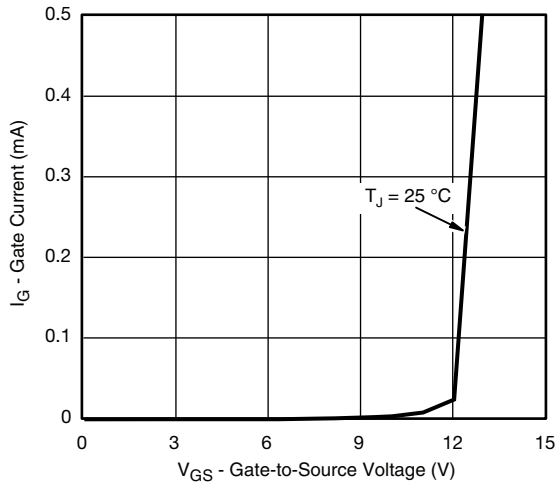
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

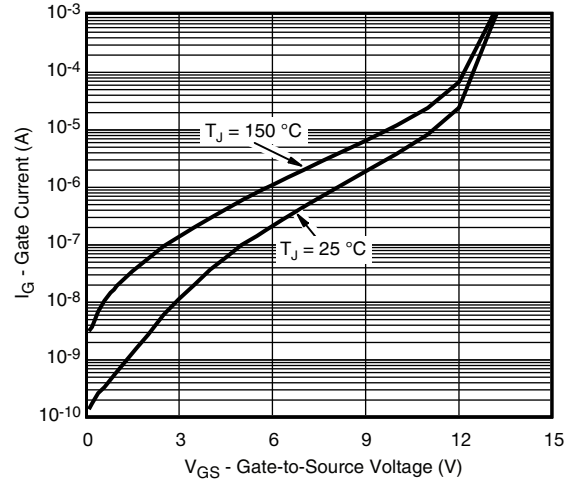
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

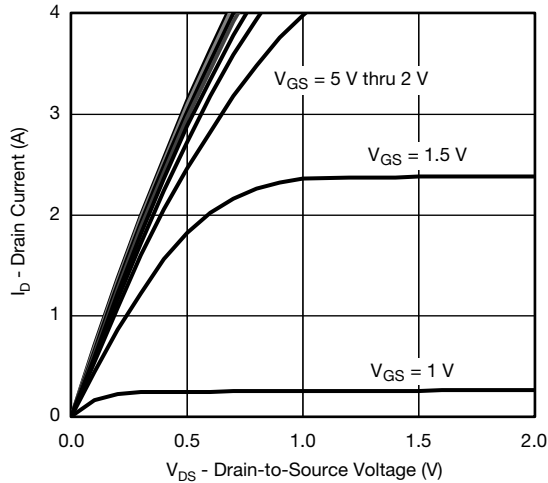
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



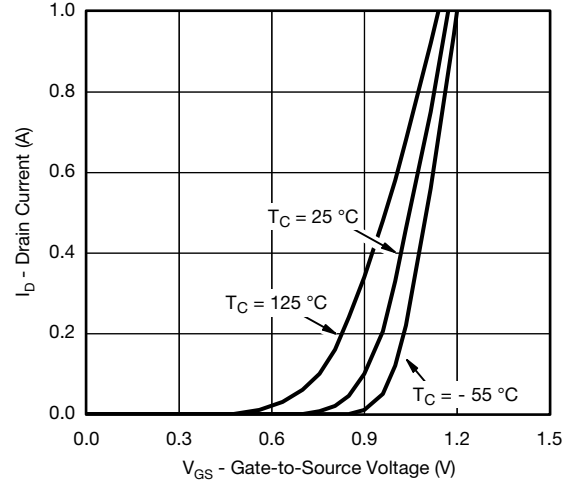
Gate Current vs. Gate-to-Source Voltage



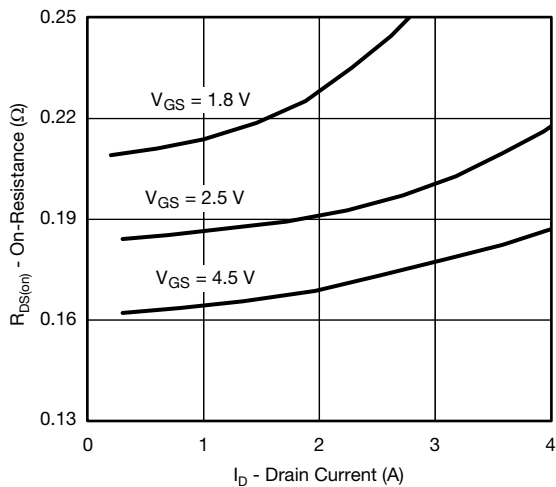
Gate Current vs. Gate-to-Source Voltage



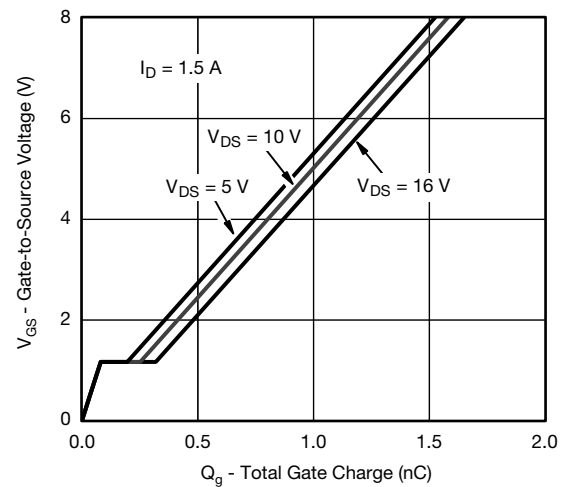
Output Characteristics



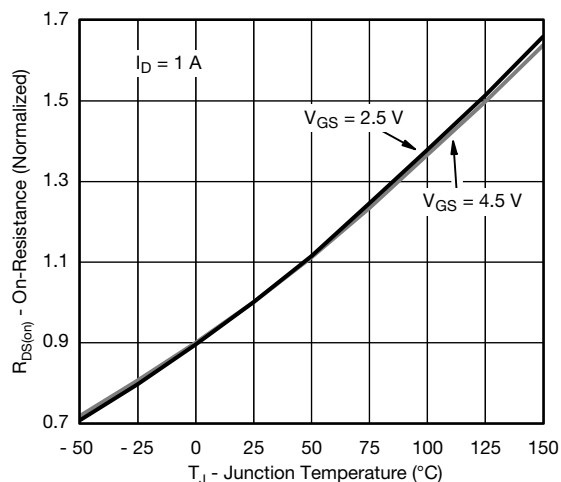
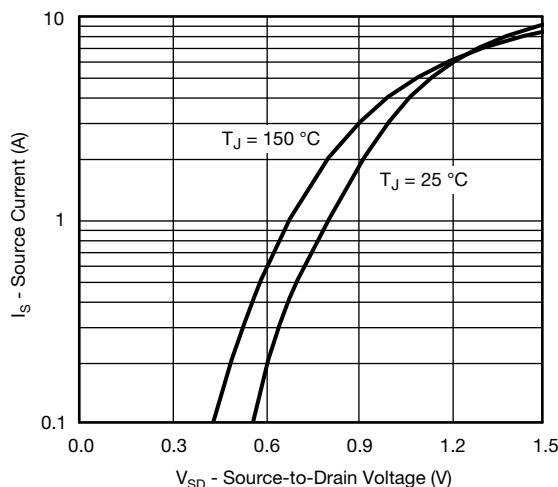
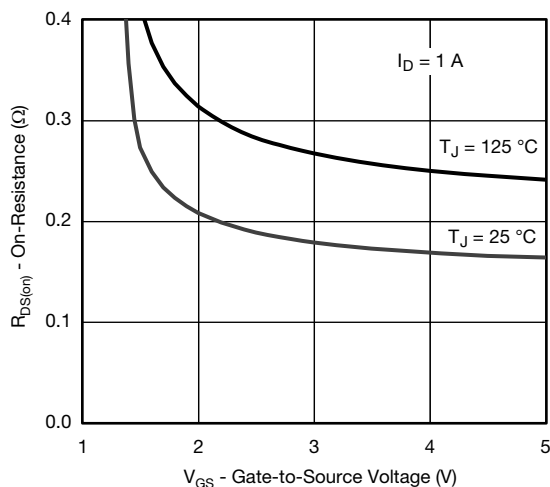
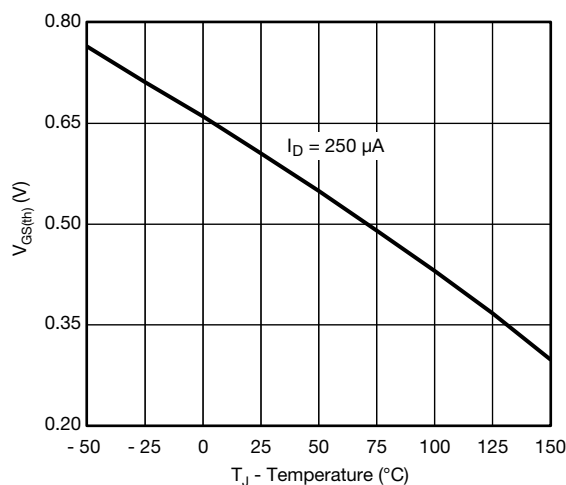
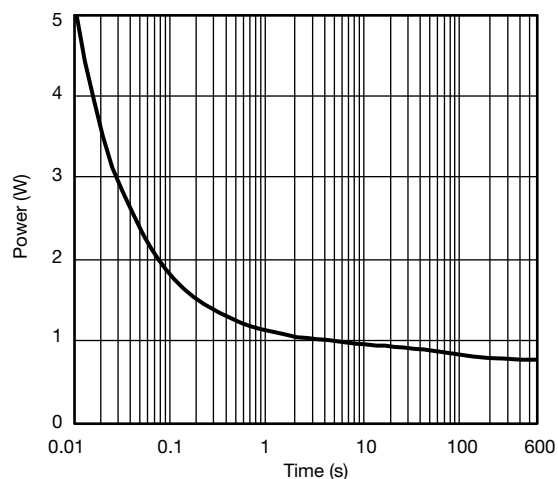
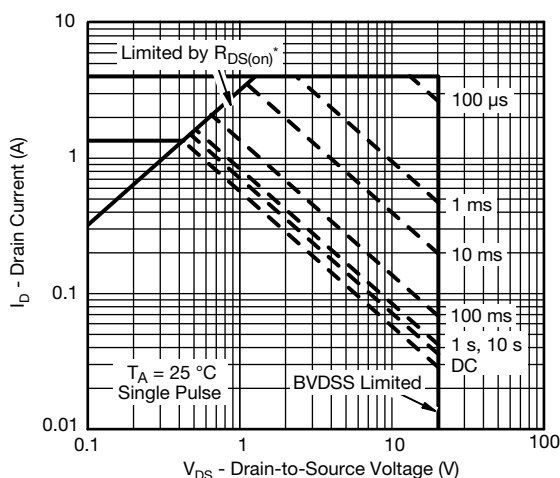
Transfer Characteristics



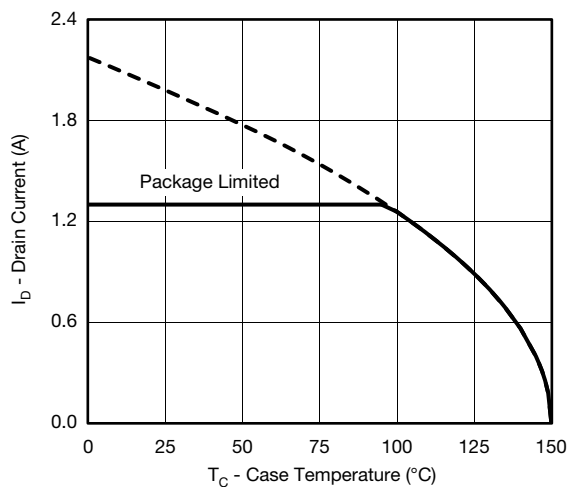
On-Resistance vs. Drain Current



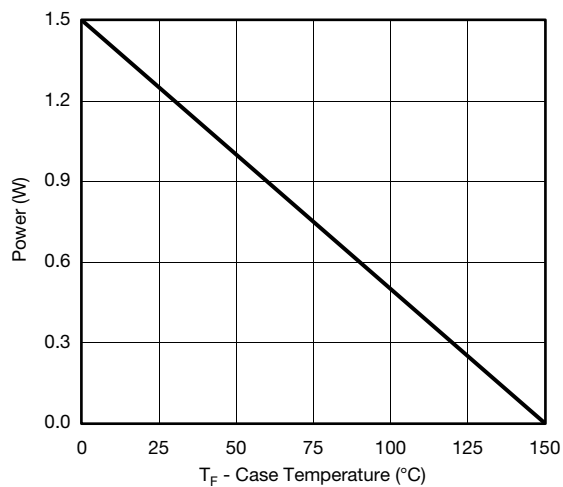
Gate Charge

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient**\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified**Safe Operating Area, Junction-to-Ambient**

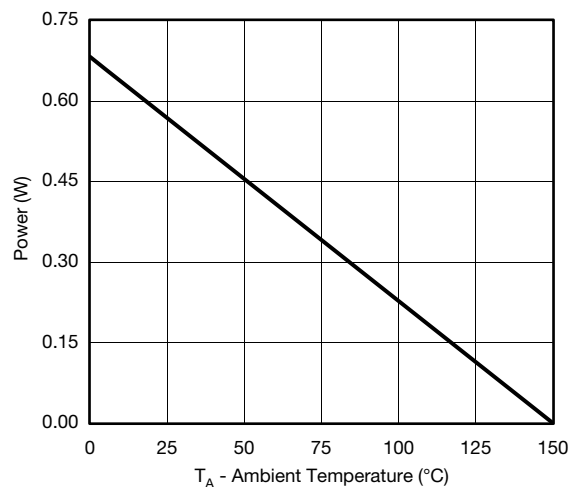
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating\*

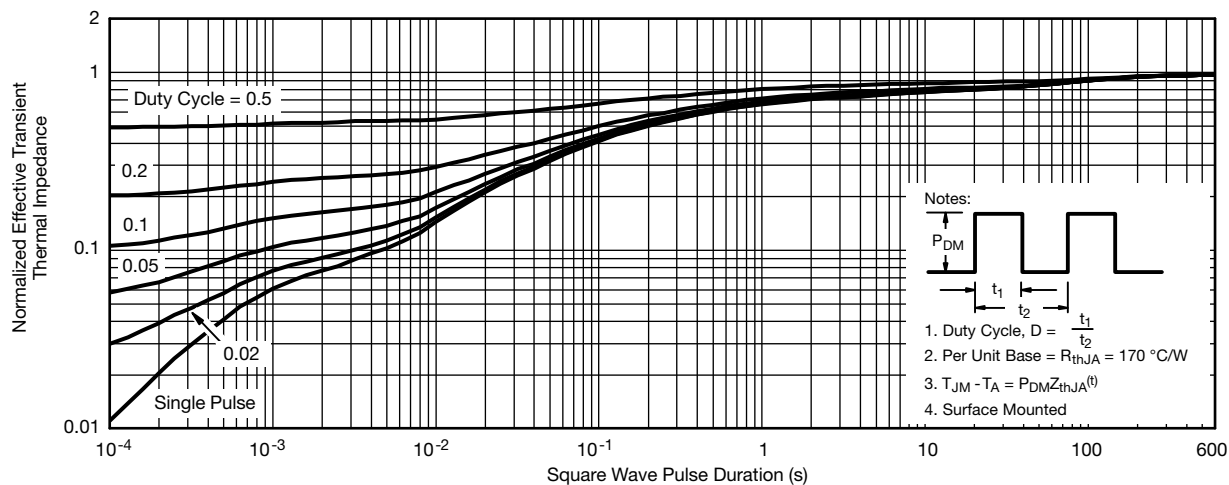
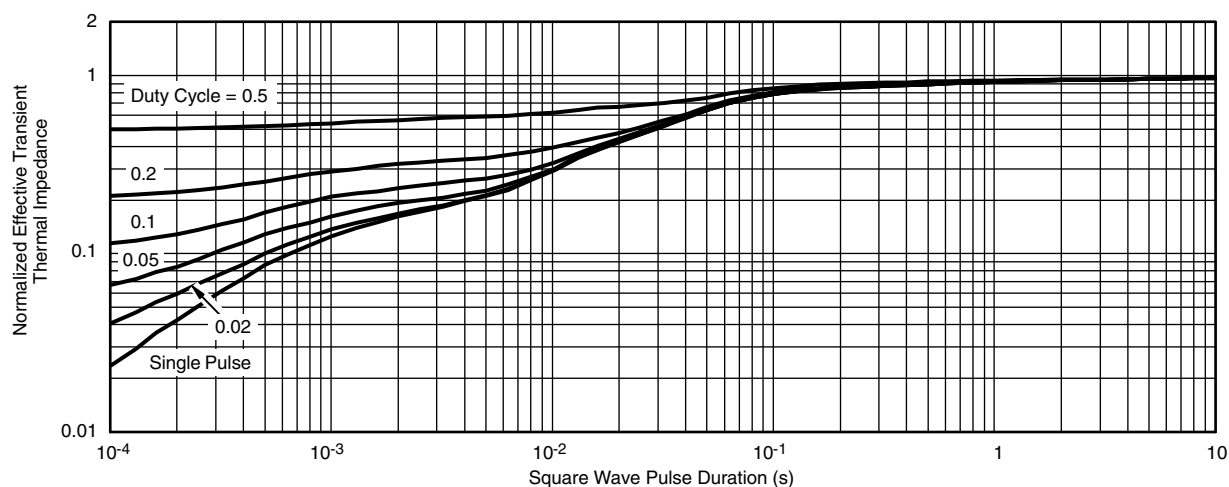


Power, Junction-to-Foot



Power, Junction-to-Ambient

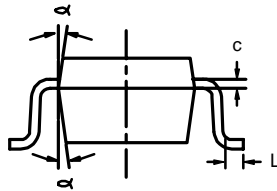
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

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**SC-70: 6-LEADS**



	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	0.90	—	1.10	0.035	—	0.043
A <sub>1</sub>	—	—	0.10	—	—	0.004
A <sub>2</sub>	0.80	—	1.00	0.031	—	0.039
b	0.15	—	0.30	0.006	—	0.012
c	0.10	—	0.25	0.004	—	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5550						

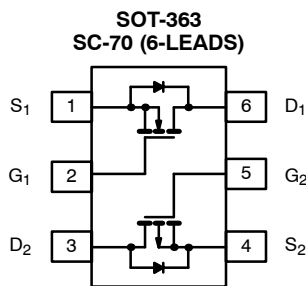
# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

## INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

## PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.



Top View  
FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

## BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

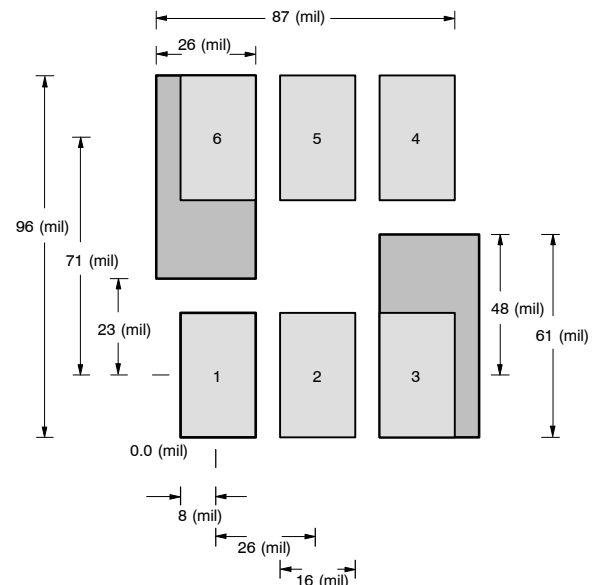


FIGURE 2. SC-70 (6 leads) Dual

## EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch<sup>2</sup> PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.



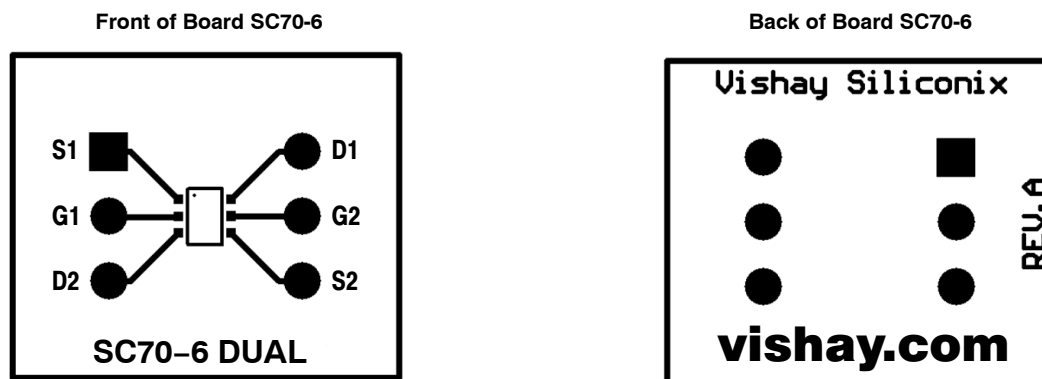


FIGURE 3.

## THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the “foot” is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

### Power Dissipation

The typical  $R\theta_{JA}$  for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch<sup>2</sup> FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

### Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{413^{\circ}\text{C/W}}$	$P_D = \frac{150^{\circ}\text{C} - 60^{\circ}\text{C}}{413^{\circ}\text{C/W}}$
$P_D = 303 \text{ mW}$	$P_D = 218 \text{ mW}$

### COOPER LEADFRAME

Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{224^{\circ}\text{C/W}}$	$P_D = \frac{150^{\circ}\text{C} - 60^{\circ}\text{C}}{224^{\circ}\text{C/W}}$
$P_D = 558 \text{ mW}$	$P_D = 402 \text{ mW}$

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

## TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of  $R\theta_{JA}$  for the dual 6-pin SC-70 with varying leadframes are as follows:

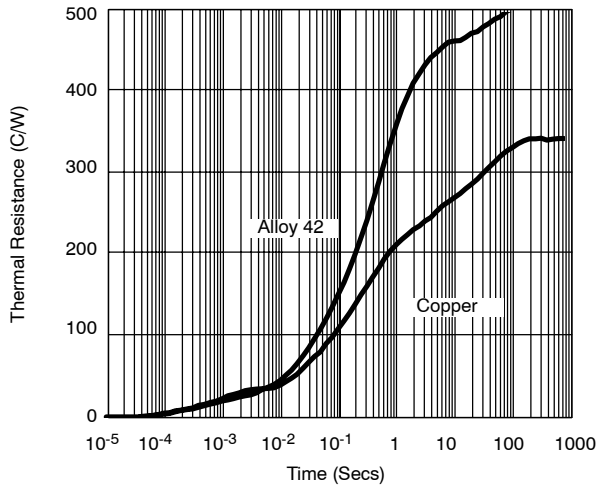
### LITTLE FOOT 6-PIN SC-70

	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch <sup>2</sup> PCB with maximum copper both sides.	413°C/W	224°C/W

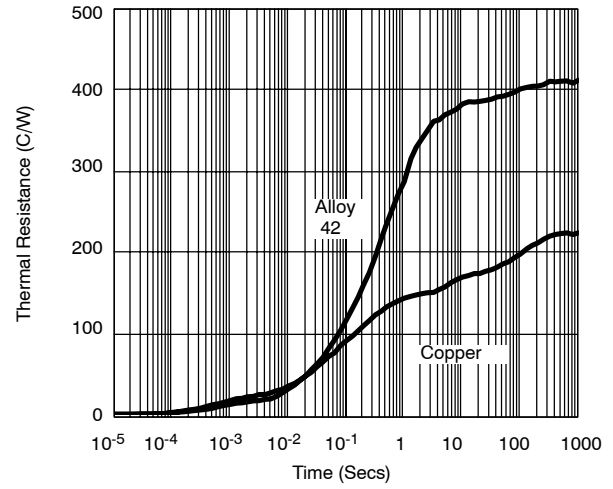
The results indicate that designers can reduce thermal resistance ( $\theta_{JA}$ ) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch<sup>2</sup> PCB area.

The Dual copper leadframe versions have the following suffix:

Dual: Si19xxEDH  
 Compl.: Si15xxEDH

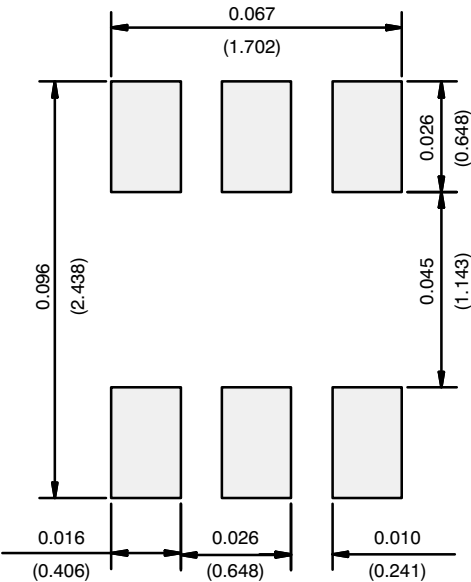


**FIGURE 4.** Dual SC70-6 Thermal Performance on EVB



**FIGURE 5.** Dual SC70-6 Comparison on 1-inch<sup>2</sup> PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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