

QTP: what's the advantage of the second version?

```
if ( i < j )
    i++;
else
    j++;

bge $s3, $s4, doelse
    addi $s3, $s3, 1 # if-body
    b endelse # skip else

doelse:
    addi $s4, $s4, 1 # else-body
endelse:</pre>
```

```
int N = 100;
int i = 0;
while ( N > 0 ) {
   N = N / 2;
   i++;
}
```

```
# $s0 == N, $t0 == i
    li $s0, 100  # N = 100
    li $t0, 0  # i = 0
    ble $s0, $zero, done # see if loop is necessary
loop:
    sra $s0, $s0, 1  # calculate N / 2
    addi $t0, $t0, 1  # i++
    bgt $s0, $zero, loop # check whether to restart
done:
```

Converted while loop to a do-while

QTP: what's the advantage?

for Loop Example

```
int Sum = 0, Limit = 100;
for (int i = 1; i <= Limit; ++i) {
   Sum = Sum + i*i;
}</pre>
```

QTP: convert this to the do-while pattern

Program Termination

Unlike the high-level languages you are accustomed to, MIPS assembly does not include an instruction, or block syntax, to terminate the program execution.

MIPS programs can be terminated by making a system call:

```
## Exit
li $v0, 10 # load code for exit system call in $v0
syscall # make the system call to exit
```

Without such code, the system could attempt to continue execution into the memory words that followed the final instructions of the program. That rarely produces graceful results.

Pseudo-Instructions

You may have noticed something is odd about a number of the MIPS instructions that have been covered so far. For example:

li \$t0, 0xFFFFFFF

Now, logically there's nothing wrong with wanting to place a 32-bit value into one of the registers.

But there's certainly no way the instruction above could be translated into a 32-bit machine instruction, since the immediate value alone would require 32 bits.

This is an example of a *pseudo-instruction*. A MIPS assembler, or MARS, may be designed to support such extensions that make it easier to write complex programs.

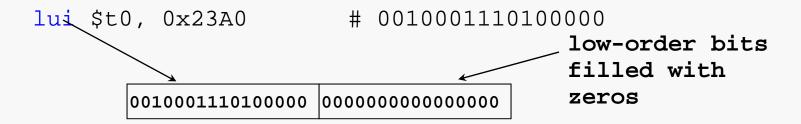
In effect, the assembler supports an *extended MIPS architecture* that is more sophisticated than the actual MIPS architecture of the underlying hardware.

Of course, the assembler must be able to translate every pseudo-instruction into a sequence of valid MIPS assembly instructions.

```
move $t1, $t2 # $t1 <-- $t2
                 $t1, $t2, $zero # recall: x OR 0 == x
             or
li
    $t1, < imm> # $t1 = 32-bit imm value
  # e.g., suppose <imm> is 0x23A0FB18
  # The assembler sometimes needs a register in which it can
  # store temporary values. The register $at is reserved for
  # such use.
  and 0s in the lower byte
        $t1, $at, 0xFB18 # put lower byte into req
  ori
```

lui and ori Details

We'd like to be able to load a 32-bit constant into a register Must use two instructions, new "load upper immediate" instruction



Then must get the lower order bits right, i.e.,

ori \$t0, \$t0, FB18 # 1111101100011000

00	010001110100000	0000000000000000
00	000000000000000000000000000000000000000	1111101100011000

ori

0010001110100000	1111101100011000