MIPS32® Instruction Set
Quick Reference

R_D — Destination register
R_S, R_T — Source operand registers
R_A — Return address register (R31)
PC — Program counter
Acc — 64-bit accumulator
Lo, Hi — Accumulator low ($Acc_{31:0}$) and high ($Acc_{63:32}$) parts
± — Signed operand or sign extension
∅ — Unsigned operand or zero extension
:: — Concatenation of bit fields
R2 — MIPS32 Release 2 instruction
DOTTED — Assembler pseudo-instruction

Please refer to *"MIPS32 Architecture For Programmers Volume II: The MIPS32 Instruction Set"* for complete instruction set information.

Arithmetic Operations

X	ADD	R_D, R_S, R_T	$R_D = R_S + R_T$	(overflow trap)
X	ADDI	R_D, R_S, const16	$R_D = R_S + \text{const16}^{\pm}$	(overflow trap)
X	ADDIU	R_D, R_S, const16	$R_D = R_S + \text{const16}^{\pm}$	
X	ADDU	R_D, R_S, R_T	$R_D = R_S + R_T$	
	CLO	R_D, R_S	$R_D = \text{CountLeadingOnes}(R_S)$	
	CLZ	R_D, R_S	$R_D = \text{CountLeadingZeros}(R_S)$	
	LA	R_D, label	$R_D = \text{Address(label)}$	
	LI	R_D, imm32	$R_D = \text{imm32}$	
X	LUI	R_D, const16	$R_D = \text{const16} << 16$ Rt=	
	MOVE	R_D, R_S	$R_D = R_S$	
	NEGU	R_D, R_S	$R_D = -R_S$	
	SEB[R2]	R_D, R_S	$R_D = R_{S7:0}{}^{\pm}$	
	SEH[R2]	R_D, R_S	$R_D = R_{S15:0}{}^{\pm}$	
X	SUB	R_D, R_S, R_T	$R_D = R_S - R_T$	(overflow trap)
X	SUBU	R_D, R_S, R_T	$R_D = R_S - R_T$	

Shift and Rotate Operations

	ROTR[R2]	R_D, R_S, bits5	$R_D = R_{S\text{bits5}-1:0} :: R_{S31:\text{bits5}}$
	ROTRV[R2]	R_D, R_S, R_T	$R_D = R_{S\text{RT4:0}-1:0} :: R_{S31:\text{RT4:0}}$
X	SLL	R_D, R_S, shift5	$R_D = R_S << \text{shift5}$ Rt << shift5
X	SLLV	R_D, R_S, R_T	$R_D = R_S << R_{T4:0}$ Rt << Rs[4:0]
X	SRA	R_D, R_S, shift5	$R_D = R_S{}^{\pm} >> \text{shift5}$
X	SRAV	R_D, R_S, R_T	$R_D = R_S{}^{\pm} >> R_{T4:0}$
X	SRL	R_D, R_S, shift5	$R_D = R_S{}^{\varnothing} >> \text{shift5}$
X	SRLV	R_D, R_S, R_T	$R_D = R_S{}^{\varnothing} >> R_{T4:0}$

Logical and Bit-Field Operations

X	AND	R_D, R_S, R_T	$R_D = R_S \& R_T$
X	ANDI	R_D, R_S, const16	$R_D = R_S \& \text{const16}^{\varnothing}$
	EXT[R2]	R_D, R_S, P, S	$R_S = R_{S\,P+S-1:P}{}^{\varnothing}$
	INS[R2]	R_D, R_S, P, S	$R_{D\,P+S-1:P} = R_{S\,S-1:0}$
	NOP		No-op
X	NOR	R_D, R_S, R_T	$R_D = \sim(R_S \mid R_T)$
	NOT	R_D, R_S	$R_D = \sim R_S$
X	OR	R_D, R_S, R_T	$R_D = R_S \mid R_T$
X	ORI	R_D, R_S, const16	$R_D = R_S \mid \text{const16}^{\varnothing}$
	WSBH[R2]	R_D, R_S	$R_D = R_{S23:16} :: R_{S31:24} :: R_{S7:0} :: R_{S15:8}$
X	XOR	R_D, R_S, R_T	$R_D = R_S \oplus R_T$
X	XORI	R_D, R_S, const16	$R_D = R_S \oplus \text{const16}^{\varnothing}$

Condition Testing and Conditional Move Operations

	MOVN	R_D, R_S, R_T	if $R_T \neq 0$, $R_D = R_S$
	MOVZ	R_D, R_S, R_T	if $R_T = 0$, $R_D = R_S$
X	SLT	R_D, R_S, R_T	$R_D = (R_S{}^{\pm} < R_T{}^{\pm})$? 1 : 0
X	SLTI	R_D, R_S, const16	$R_D = (R_S{}^{\pm} < \text{const16}^{\pm})$? 1 : 0
X	SLTIU	R_D, R_S, const16	$R_D = (R_S{}^{\varnothing} < \text{const16}^{\varnothing})$? 1 : 0
X	SLTU	R_D, R_S, R_T	$R_D = (R_S{}^{\varnothing} < R_T{}^{\varnothing})$? 1 : 0

Multiply and Divide Operations

DIV	R_S, R_T	$Lo = R_S{}^{\pm} / R_T{}^{\pm}$; $Hi = R_S{}^{\pm} \bmod R_T{}^{\pm}$
DIVU	R_S, R_T	$Lo = R_S{}^{\varnothing} / R_T{}^{\varnothing}$; $Hi = R_S{}^{\varnothing} \bmod R_T{}^{\varnothing}$
MADD	R_S, R_T	$Acc += R_S{}^{\pm} \times R_T{}^{\pm}$
MADDU	R_S, R_T	$Acc += R_S{}^{\varnothing} \times R_T{}^{\varnothing}$
MSUB	R_S, R_T	$Acc -= R_S{}^{\pm} \times R_T{}^{\pm}$
MSUBU	R_S, R_T	$Acc -= R_S{}^{\varnothing} \times R_T{}^{\varnothing}$
MUL	R_D, R_S, R_T	$R_D = R_S{}^{\pm} \times R_T{}^{\pm}$
MULT	R_S, R_T	$Acc = R_S{}^{\pm} \times R_T{}^{\pm}$
MULTU	R_S, R_T	$Acc = R_S{}^{\varnothing} \times R_T{}^{\varnothing}$

Accumulator Access Operations

MFHI	R_D	$R_D = Hi$
MFLO	R_D	$R_D = Lo$
MTHI	R_S	$Hi = R_S$
MTLO	R_S	$Lo = R_S$

Jumps And Branches (Note: One Delay Slot)

	B	off18	$PC += \text{off18}^{\pm}$
	BAL	off18	$R_A = PC + 8$, $PC += \text{off18}^{\pm}$
X	BEQ	R_S, R_T, off18	if $R_S = R_T$, $PC += \text{off18}^{\pm}$
	BEQZ	R_S, off18	if $R_S = 0$, $PC += \text{off18}^{\pm}$
	BGEZ	R_S, off18	if $R_S \geq 0$, $PC += \text{off18}^{\pm}$
	BGEZAL	R_S, off18	$R_A = PC + 8$; if $R_S \geq 0$, $PC += \text{off18}^{\pm}$
	BGTZ	R_S, off18	if $R_S > 0$, $PC += \text{off18}^{\pm}$
	BLEZ	R_S, off18	if $R_S \leq 0$, $PC += \text{off18}^{\pm}$
	BLTZ	R_S, off18	if $R_S < 0$, $PC += \text{off18}^{\pm}$
	BLTZAL	R_S, off18	$R_A = PC + 8$; if $R_S < 0$, $PC += \text{off18}^{\pm}$
X	BNE	R_S, R_T, off18	if $R_S \neq R_T$, $PC += \text{off18}^{\pm}$
	BNEZ	R_S, off18	if $R_S \neq 0$, $PC += \text{off18}^{\pm}$
X	J	addr28	$PC = PC_{31:28} :: \text{addr28}^{\varnothing}$
	JAL	addr28	$R_A = PC + 8$; $PC = PC_{31:28} :: \text{addr28}^{\varnothing}$
	JALR	R_D, R_S	$R_D = PC + 8$; $PC = R_S$
	JR	R_S	$PC = R_S$

Load and Store Operations

	LB	R_D, off16(R_S)	$R_D = \text{mem8}(R_S + \text{off16}^{\pm})^{\pm}$
	LBU	R_D, off16(R_S)	$R_D = \text{mem8}(R_S + \text{off16}^{\pm})^{\varnothing}$
	LH	R_D, off16(R_S)	$R_D = \text{mem16}(R_S + \text{off16}^{\pm})^{\pm}$
	LHU	R_D, off16(R_S)	$R_D = \text{mem16}(R_S + \text{off16}^{\pm})^{\varnothing}$
X	LW	R_D, off16(R_S)	$R_D = \text{mem32}(R_S + \text{off16}^{\pm})$
	LWL	R_D, off16(R_S)	$R_D = \text{LoadWordLeft}(R_S + \text{off16}^{\pm})$
	LWR	R_D, off16(R_S)	$R_D = \text{LoadWordRight}(R_S + \text{off16}^{\pm})$
	SB	R_S, off16(R_T)	$\text{mem8}(R_T + \text{off16}^{\pm}) = R_{S7:0}$
	SH	R_S, off16(R_T)	$\text{mem16}(R_T + \text{off16}^{\pm}) = R_{S15:0}$
X	SW	R_S, off16(R_T)	$\text{mem32}(R_T + \text{off16}^{\pm}) = R_S$
	SWL	R_S, off16(R_T)	$\text{StoreWordLeft}(R_T + \text{off16}^{\pm}, R_S)$
	SWR	R_S, off16(R_T)	$\text{StoreWordRight}(R_T + \text{off16}^{\pm}, R_S)$
	ULW	R_D, off16(R_S)	$R_D = \text{unaligned\_mem32}(R_S + \text{off16}^{\pm})$
	USW	R_S, off16(R_T)	$\text{unaligned\_mem32}(R_T + \text{off16}^{\pm}) = R_S$

Atomic Read-Modify-Write Operations

LL	R_D, off16(R_S)	$R_D = \text{mem32}(R_S + \text{off16}^{\pm})$; link
SC	R_D, off16(R_S)	if Atomic, $\text{mem32}(R_S + \text{off16}^{\pm}) = R_D$; $R_D = \text{Atomic}$? 1 : 0

MIPS

Registers

0	zero	Always equal to zero
1	at	Assembler temporary; used by the assembler
2-3	v0-v1	Return value from a function call
4-7	a0-a3	First four parameters for a function call
8-15	t0-t7	Temporary variables; need not be preserved
16-23	s0-s7	Function variables; must be preserved
24-25	t8-t9	Two more temporary variables
26-27	k0-k1	Kernel use registers; may change unexpectedly
28	gp	Global pointer
29	sp	Stack pointer
30	fp/s8	Stack frame pointer or subroutine variable
31	ra	Return address of the last subroutine call

Default C Calling Convention (O32)

Stack Management
- The stack grows down.
  - Subtract from $sp to allocate local storage space.
  - Restore $sp by adding the same amount at function exit.
- The stack must be 8-byte aligned.
  - Modify $sp only in multiples of eight.

Function Parameters
- Every parameter smaller than 32 bits is promoted to 32 bits.
- First four parameters are passed in registers $a0−$a3.
  - 64-bit parameters are passed in register pairs:
    - Little-endian mode: $a1:$a0 or $a3:$a2.
    - Big-endian mode: $a0:$a1 or $a2:$a3.
- Every subsequent parameter is passed through the stack.
  - First 16 bytes on the stack are not used.
  - Assuming $sp was not modified at function entry:
    - The 1st stack parameter is located at 16($sp).
    - The 2nd stack parameter is located at 20($sp), etc.
  - 64-bit parameters are 8-byte aligned.

Return Values
- 32-bit and smaller values are returned in register $v0.
- 64-bit values are returned in registers $v0 and $v1:
  - Little-endian mode: $v1:$v0.
  - Big-endian mode: $v0:$v1.

MIPS32 Virtual Address Space

kseg3	0xE000.0000	0xFFFF.FFFF	Mapped	Cached
ksseg	0xC000.0000	0xDFFF.FFFF	Mapped	Cached
kseg1	0xA000.0000	0xBFFF.FFFF	Unmapped	Uncached
kseg0	0x8000.0000	0x9FFF.FFFF	Unmapped	Cached
useg	0x0000.0000	0x7FFF.FFFF	Mapped	Cached

Reading The Cycle Count Register From C

```c
unsigned mips_cycle_counter_read()
{
    unsigned cc;
    asm volatile("mfc0 %0, $9" : "=r" (cc));
    return (cc << 1);
}
```

Assembly-Language Function Example

```
# int asm_max(int a, int b)
# {
#   int r = (a < b) ? b : a;
#   return r;
# }

    .text
    .set    nomacro
    .set    noreorder

    .global asm_max
    .ent    asm_max

asm_max:
    move    $v0, $a0        # r = a
    slt     $t0, $a0, $a1   # a < b ?
    jr      $ra             # return
    movn    $v0, $a1, $t0   # if yes, r = b

    .end    asm_max
```

C / Assembly-Language Function Interface

```c
#include <stdio.h>

int asm_max(int a, int b);

int main()
{
    int x = asm_max(10, 100);
    int y = asm_max(200, 20);
    printf("%d %d\n", x, y);
}
```

Invoking MULT And MADD Instructions From C

```c
int dp(int a[], int b[], int n)
{
    int i;
    long long acc = (long long) a[0] * b[0];
    for (i = 1; i < n; i++)
        acc += (long long) a[i] * b[i];
    return (acc >> 31);
}
```

Atomic Read-Modify-Write Example

```
atomic_inc:
    ll      $t0, 0($a0)     # load linked
    addiu   $t1, $t0, 1     # increment
    sc      $t1, 0($a0)     # store cond'l
    beqz    $t1, atomic_inc # loop if failed
    nop
```

Accessing Unaligned Data
note: **ULW** and **USW** automatically generate appropriate code

Little-Endian Mode		Big-Endian Mode	
LWR	R$_D$, off16(R$_S$)	LWL	R$_D$, off16(R$_S$)
LWL	R$_D$, off16+3(R$_S$)	LWR	R$_D$, off16+3(R$_S$)
SWR	R$_D$, off16(R$_S$)	SWL	R$_D$, off16(R$_S$)
SWL	R$_D$, off16+3(R$_S$)	SWR	R$_D$, off16+3(R$_S$)

Accessing Unaligned Data From C

```c
typedef struct
{
    int u;
} __attribute__ ((packed)) unaligned;


int unaligned_load(void *ptr)
{
    unaligned *uptr = (unaligned *)ptr;
    return uptr->u;
}
```

MIPS SDE-GCC Compiler Defines

__mips	MIPS ISA (= 32 for MIPS32)
__mips_isa_rev	MIPS ISA Revision (= 2 for MIPS32 R2)
__mips_dsp	DSP ASE extensions enabled
_MIPSEB	Big-endian target CPU
_MIPSEL	Little-endian target CPU
_MIPS_ARCH_CPU	Target CPU specified by −march=CPU
_MIPS_TUNE_CPU	Pipeline tuning selected by −mtune=CPU

Notes

- Many assembler pseudo-instructions and some rarely used machine instructions are omitted.
- The C calling convention is simplified. Additional rules apply when passing complex data structures as function parameters.
- The examples illustrate syntax used by GCC compilers.
- Most MIPS processors increment the cycle counter every other cycle. Please check your processor documentation.