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A practical, low-overhead, one-cycle correction design method for variation-tolerant digital circuits

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Abstract: This paper presents a practical, low-overhead, one-cycle correction better-than-worst-case design method for ultra-low voltage digital circuits. Excessive design margin for PVT variation brought by traditional worst-case design method is eliminated. Proposed method is completely compatible with EDA tools. Considerable design efforts are relaxed compared with other variation-tolerant techniques. We have implemented our proposed technique on a 16 bits × 16 bits pipelined multiplier in SIMC 55 nm CMOS process. The experimental results show that our proposed technique can get about 59% energy efficiency improvements compared with operating in worst-case timing margin.

Keywords: AVS, DVFS, adaptive circuits, EDAC, time borrowing, variation tolerance

Classification: Integrated circuits

References

[1] S. Nassif, *et al.*: "High performance CMOS variability in the 65 nm regime and beyond," IEEE International Electron Devices Meeting (2007) (DOI: 10.1109/IEDM.2007.4419002).

[2] K. Bowman, *et al.*: "Circuit techniques for dynamic variation tolerance," Proc. 46th Annual Design Automation Conference. ACM (2009) (DOI: 10.1145/1629911.1629915).

[3] T. Fischer, *et al.*: "A 90-nm variable frequency clock system for a power-managed itanium architecture processor," IEEE J. Solid-State Circuits **41** (2006) 218 (DOI: 10.1109/JSSC.2005.859879).

[4] P. Macken, *et al.*: "A voltage reduction technique for digital systems," 37th IEEE International Conference on Solid-State Circuits (1990) (DOI: 10.1109/ISSCC.1990.110213).

[5] A. Drake, *et al.*: "A distributed critical-path timing monitor for a 65 nm high-performance microprocessor," IEEE International Solid-State Circuits Confer-

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Publicized December 22, 2017
Copyedited January 25, 2018

ence. Digest of Technical Papers (2007) 398 (DOI: 10.1109/ISSCC.2007.373462).
[6] D. Ernst, *et al.*: "Razor: A low-power pipeline based on circuit-level timing speculation," 36th Annual IEEE/ACM International Symposium on Microarchitecture (2003) 7 (DOI: 10.1109/MICRO.2003.1253179).
[7] S. Das, *et al.*: "RazorII: In situ error detection and correction for PVT and SER tolerance," IEEE J. Solid-State Circuits **44** (2009) 32 (DOI: 10.1109/JSSC.2008.2007145).
[8] I. Kwon, *et al.*: "Razor-lite: A light-weight register for error detection by observing virtual supply rails," IEEE J. Solid-State Circuits **49** (2014) 2054 (DOI: 10.1109/JSSC.2014.2328658).
[9] M. Fojtik, *et al.*: "Bubble razor: Eliminating timing margins in an ARM cortex-M3 processor in 45 nm CMOS using architecturally independent error detection and correction," IEEE J. Solid-State Circuits **48** (2013) 66 (DOI: 10.1109/JSSC.2012.2220912).
[10] M. R. Choudhury, *et al.*: "Time-borrowing circuit designs and hardware prototyping for timing error resilience," IEEE Trans. Comput. **63** (2014) 497 (DOI: 10.1109/TC.2012.190).
[11] K. A. Bowman, *et al.*: "Energy-efficient and metastability-immune resilient circuits for dynamic variation tolerance.," IEEE J. Solid-State Circuits **44** (2009) 49 (DOI: 10.1109/JSSC.2008.2007148).
[12] J. Tschanz, *et al.*: "A 45 nm resilient and adaptive microprocessor core for dynamic variation tolerance," IEEE International Solid-State Circuits Conference - (ISSCC) (2010) (DOI: 10.1109/ISSCC.2010.5433922).
[13] J. Zhou, *et al.*: "HEPP: A new in-situ timing-error prediction and prevention technique for variation-tolerant ultra-low-voltage designs," IEEE Asian Solid-State Circuits Conference (A-SSCC) (2013) (DOI: 10.1109/ASSCC.2013.6690999).
[14] Y. Zhang, *et al.*: "8.8 iRazor: 3-transistor current-based error detection and correction in an ARM Cortex-R4 processor," IEEE International Solid-State Circuits Conference (ISSCC) (2016) (DOI: 10.1109/ISSCC.2016.7417956).
[15] S. Kim and M. Seok: "Variation-tolerant, ultra-low-voltage microprocessor with a low-overhead, within-a-cycle in-situ timing-error detection and correction technique," IEEE J. Solid-State Circuits **50** (2015) 1478 (DOI: 10.1109/JSSC.2015.2418713).

1 Introduction

With the popularity of portable device, low power IC design becomes an important requirement to save the battery life of movable devices. Due to quadratic dependence of energy and supply voltage, significant energy can be saved by reducing supply voltage. But with the scaling of supply voltage, IC becomes more sensitive to PVT (Process, Voltage, and Temperature) variations which brings a large design margin [1]. Especially in near-threshold and sub-threshold regions, the path delay increases exponentially with the drop of supply voltage. This means that the traditional worst-case design method is not suitable for ultra-low voltage design [2]. Large design margin for PVT variations has become a roadblock to ultra-low voltage integrated circuit. To overcome this problem, several design techniques aimed at reducing the safety margin have been proposed. The basic idea of these approaches is to adjust the supply voltage (and/or operating fre-

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quency) to the optimal value depending on the current operating conditions of the circuit.

In order to reduce design margin for PVT variations in low voltage design, several techniques have been proposed. Replica Path technique and canary circuit [3, 4, 5] mimics critical path delays to predict timing error appearance, instead of measuring the speed of the real circuit. When PVT variations cause the increase of path delay, replica path gives error signal before actual error occurrence. Razor system [6, 7, 8] uses in-situ delay error detector to detect timing error. When unexpected transition induced by PVT variation appears during the detecting window, error signal is activated. Pipeline flushing or architectural replay will be followed for error correction. Razor system gives the opportunity for circuits operating below the critical voltage. The optimal energy efficient point appears at where the overhead for error correction equals the benefits from voltage reduction. Regretfully, Razor system is architectural-invasive, which make it only suitable for CPU-like circuits. Bubble-razor [9] has the ability of recovering within one-cycle when error appears. However, it only can be applied to latch-based circuits and must pay large design effort for complex control logic. TIMBER [10] detects and uses the benefits of time borrowing from adjacent logic stages, some small timing violations can be recovered by time borrowing. DSTB [11, 12] and TDTB [11] remove meta-stability from date path to error path. HEPP [13] places timing violation predictor at the Half-Path-Delay point of critical path, timing violation can be predicted before real timing violation happens. Due to the number of Half-Path-Delay point of critical paths is very large, HEPP will have a considerable design effort and area overhead in large scale circuits.

We propose a new digital circuit design method for ultra-low voltage variation-tolerant design. A novel error detection circuit was proposed, which is simple and fully supported by standard cells. The proposed technique is totally supported by EDA tools and can be easily applied to general digital circuits. Time to market can be greatly saved when the proposed technique is used.

The remainder of this paper is structured as follows. Section 2 presents our proposed technique. Section 3 presents the work flow with *SYNOPSYS* EDA tools. Section 4 presents silicon results of implemented multiplier circuits and comparison with other works. In section 5, a brief conclusion and remarks are presented.

2 Proposed technique

The main idea of our proposed method is that the endpoint Flip-Flops of critical paths is replaced with designed error detection latch (EDL). The error detection latch is consisting of a positive latch and a transition detector. It is shown as Fig. 1.

The logic stage L1 end with error detection latches (EDL) contains critical paths. Delay timing error will appear if an unexpected transition of data path occurs during the positive phase of the clock affected by PVT variations. Error pulse generated by transition detector are sent to the error control unit.

The structure of error control unit is shown as Fig. 2. Error control unit mainly has three functions. Firstly, it ORed the error pulses from EDLs together to generate a single p_ERR signal. Secondly, it ensures that the p_ERR only can be propagated

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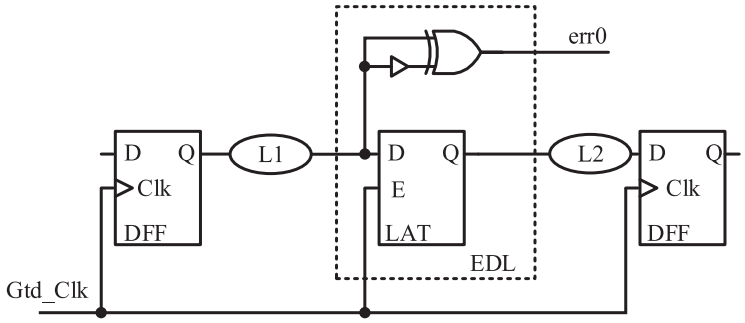

Fig. 1. Proposed error detection latch (EDL)

to clock control unit during the positive phase of clock. Thirdly, in order to prevent the error pulse from being too short to propagate to the clock control unit, it extends the width of error pulse as much as possible. The timing diagram simulated by *Hspice* is also shown in Fig. 2.

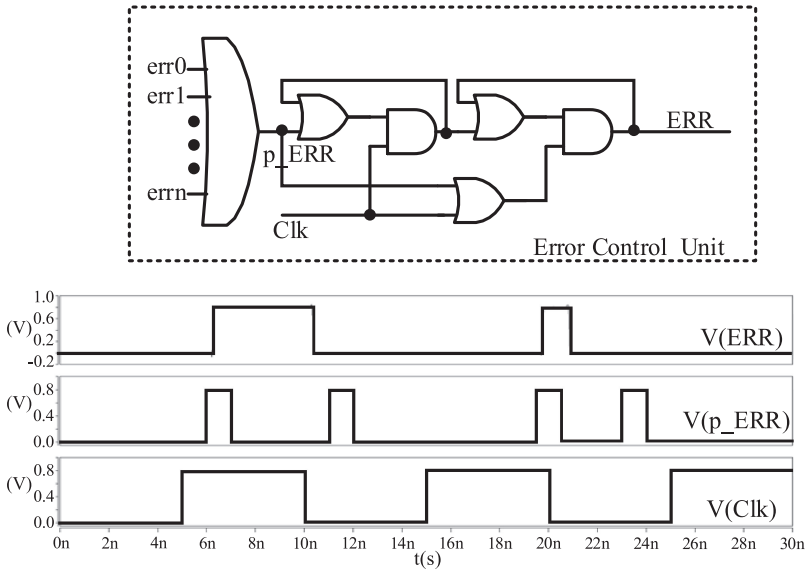

Fig. 2. Structure of error control unit and its timing diagram simulated by *Hspice*

When timing violation occurs, timing error will not corrupt the system immediately due to the time borrowing ability of latch. To give enough time to the stage next to EDL, just as shown L2 in Fig. 1, to resolve correct logic value. When ERR signal is propagated to clock control unit, the clock control unit generates a clock stall. The structure and timing diagram of clock control unit is shown as Fig. 3. Error pulse (ERR) arrived during the positive phase of clock, then the positive edge of next clock is gated. The line V(Clk) represents the main clock signal, the line V(ERR) represents the error signal from error control unit, and the line V(Gtd_Clk) represents the gated-clock of the clock control unit. Even though there is a continuous timing error between adjacent pipeline stages, the clock control unit can also recover the error by continuous clock stalls. (Note: The timing diagrams simulated by *Hspice* have been redrawn for better visibility.)

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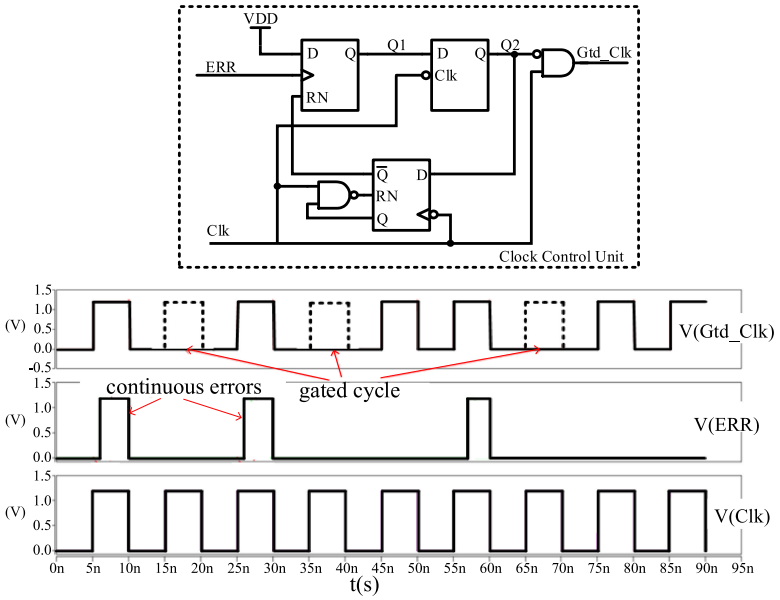


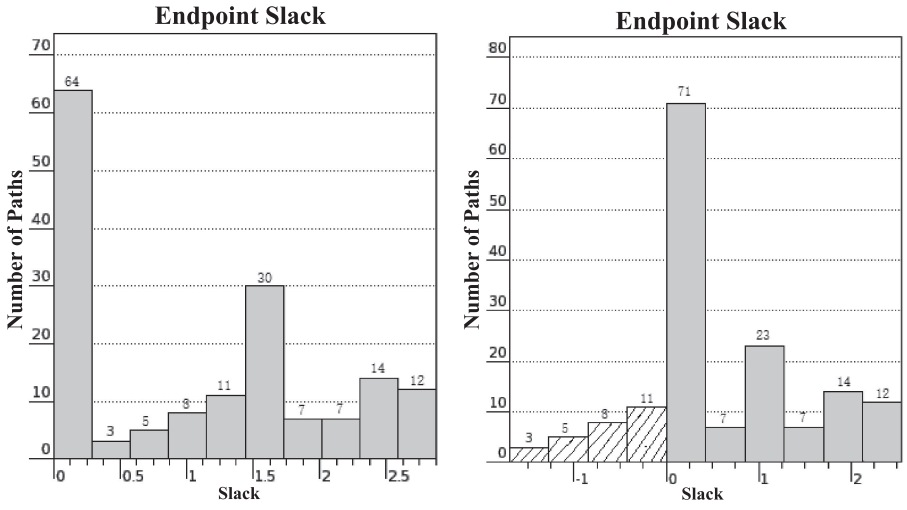
Fig. 3. Structure of clock control unit and its timing diagram simulated by *Hspice*

3 Work flow with EDA tools

3.1 Method of choosing DFFs to be replaced

Different from traditional best-worst case design method, we check timing constraints at worst PVT conditions by STA (Static Timing Analysis), but synthesis the RTL code at typical PVT conditions. On the assumption that circuits has been synthesised and implemented with nearly zero slack remained in typical PVT condition. Negative slack will be obtained when do STA in worst PVT conditions. The endpoints with negative slack will be marked for replacing with EDLs. Paths slacks distribution at typical PVT conditions is shown in Fig. 4(a).

When the gate-level circuits are analyzed at worst PVT conditions, negative timing slack will appear. The endpoints of paths with negative slacks are replaced



(a) (b)

Fig. 4. Distribution of paths slack in typical PVT conditions (a) and worst PVT conditions (b)

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with EDLs. The timing slack distribution at worst PVT condition is shown in Fig. 4(b). The area with slash in Fig. 4(b) reflects the paths with negative slacks. The endpoint DFFs in this area will be replaced with EDLs. As described in section III, the EDL can detect timing error induced by PVT variations maximum to about 1.5 clock cycles. This means negative slack at worst PVT conditions cannot exceed half of clock cycle.

According to the structure of EDL, it can be easily concluded that the maximum detecting window of timing error is that,

$$T_w = \frac{1}{2} T_c - T_{su} \tag{1}$$

Where the T_W represents the max detecting window of EDL, the T_C represents the period of main clock, and the T_{su} represents the setup time of positive latch of EDL. Therefore, when PVT variation affects the delay of critical paths increase, time borrowing will be detected by transition detector of EDLs, the max variation can be tolerated is that the delay of critical path increases to $T_C + T_W$.

Another constraint must be applied to short path end with EDLs. That is the delay of the short paths end with EDLs cannot be less than the positive phase of the clock. In the *SYNOPSYS* EDA tools, the short path constraint can be described as follows,

*Set_min_delay -to xxx/xxx/xxx/EDL/D [expr 0.5 * $clock_period]*

Where *xxx* presents the hierarchy of design. The area overhead for padding short path is about 3% in experiment circuits.

3.2 Work flow with EDA tools

The method we proposed with EDA tools is shown in the following flow chart as Fig. 5. RTL code is translated into gate level netlist using *Design Compiler* (DC). DC can report critical paths of synthesized design, but due to lacking of physical information of wire delay and actual RC parasitic parameters, critical paths reported

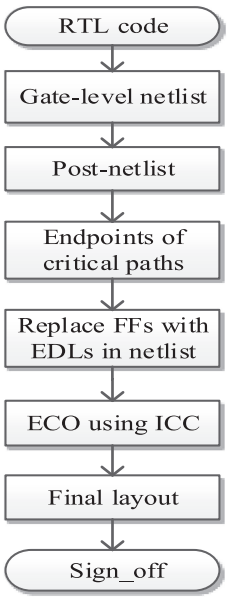

Fig. 5. Flow chart of proposed method

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by DC are not very accurate. In order to obtain the most actual delay information of circuits, we implement our experiments circuits using *IC Compiler*. When post-netlist has been got after physical implementation completed, critical paths are extracted by Prime Timing sign-off timing tool, which has a very accurate timing extraction ability. ECO flow is utilized for replacing the DFFs need to be changed with EDLs. ECO brings little effects on the whole circuits. The routed wire will get the least affects. Timing of the modified circuit has a no big difference with the circuit before ECO.

3.3 Design of OR gate in error control unit

As described in section 2, a large number of error signals from EDLs are ORed together by a OR gate in error control unit to generate a single error signal, just as p_ERR in Fig. 2. The delay of OR gate in error control unit is an important point to be carefully considered. Too large delay of OR gate can result timing error in error control unit itself, which will cause that the clock control unit cannot generate clock stall in time. Therefore, the OR gate in error control unit must be fast enough, especially for large scale circuits.

There are two methods to solve this problem. Method one, for small scale circuit, just as experimented circuit and [10], the ability of timing optimization of EDA tools can be fully exploited for optimizing the OR gate under proper constraint.

The constraint for OR gate is shown as follows,

$$T_{OR} \leq \frac{1}{2} T_c$$

Where the T_{OR} represents the maximum delay of OR gate in error control unit, T_c represents the period of clock. This constraint can be applied during synthesize process by *Design Compiler*.

Method two, for large scale circuit, dynamic OR gate can be used for better timing closure, which has been proved an effective way by [7, 8, 14, 11]. The schematic of dynamic OR gate is shown in Fig. 6.

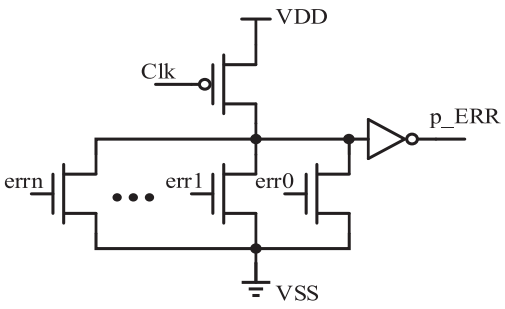

Fig. 6. Schematic of dynamic OR gate

4 Silicon result of experiment circuit

Proposed method was applied to a 16 bits × 16 bits pipelined multiplier at SMIC 55 nm HVT. Some stats of the implemented circuits are shown as follows:

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1) Tech node: SMIC 55 nm HVT
2) Operating frequency: 500 MHz
3) Cell count: 2270 cells
4) Total DFFs: 489
5) EDL count: 42

Fabricated die with proposed technique has been tested under following test environment as shown in Fig. 7.

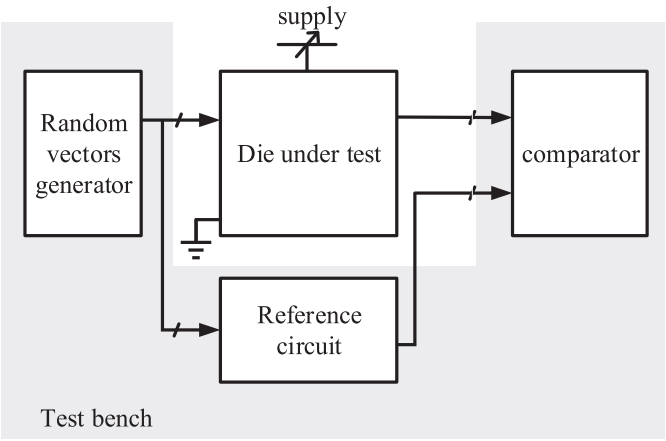

Fig. 7. Test structure of experiment die

The test environment is built by *NI PXIe-1085* instrument. The random vector generator generates 32 bits random binary codes, which are entered into implemented die. The reference circuits modeled by *NI PXIe-1085* instrument. Comparator indicates the correctness of outputs of die under test by comparing the outputs of reference circuits and test die. With the supply voltage decreasing, the minimum voltage of the test die can be measured.

The experiment results show that the die can operate correctly under 0.72 V, which is 40% lower than nominal voltage 1.2 V. The profit of lower operating voltage is about 59% energy benefits.

The comparison with other works is shown as Table I. As can be seen that our proposed technique has an acceptable area overhead 3.9% and a considerable energy improvement 59%. Proposed technique also has an advantage of low design effort and only one cycle penalty for a timing error.

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Table I. Comparison with other works

	[7]	[12]	[15]	[14]	This work
Type	Latch	Flip-Flop	Latch	Latch	Flip-Flop
Technology	130 nm	45 nm	65 nm	40 nm	55 nm
Design effort	Medium	Medium	High	High	Low
EDA supportable	No	Yes	No	No	Yes
Total area overhead	N/A	3.8%	8.3%	11.9%	3.9%
Energy improvement	33.1%~37.5%	22%	38%	30%~46%	59%
Penalty for an error	More than 1 cycle	More than 1 cycles	1 cycle	1 cycle	1 cycle

5 Conclusion

We propose a practical, low-overhead, one-cycle correction variation tolerant digital circuit design method. Large design margin for PVT variations in traditional worst-case design method has been eliminated by the proposed method. The proposed technique is totally supported by EDA tools. The proposed technique has less design effort and the ability of one-cycle error correction, which make it a practical method for ultra-low voltage variation-tolerant digital circuits. The silicon results of 16×16 bits pipelined multiplier used proposed technique shows that nearly 59% energy was saved at supply voltage of 0.72 V compared with nominal supply voltage 1.2 V.

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