Min Han

Atlanta, GA | (423) 356-7763 | U.S. Citizen | 20min05han@gmail.com | linkedin.com/in/minhan05 | minhan.fyi

EDUCATION

Georgia Institute of Technology

Atlanta, GA

Bachelor of Science in Computer Engineering (Minor in Mathematics)

Aug. 2024 - Dec. 2026

HKN Initiation Officer, SiliconJackets Web Dev, TA, VIP Researcher, Future RA

University of Georgia

Athens, GA

Bachelor of Science in **Electrical Engineering**

Presidential Scholar (Fall 2023)

Aug. 2023 - May 2024

Classes

Circuit Analysis: Thevenin-Norton Equiv, Low/High Pass Filter, Laplace Analysis, Frequency Response

Data Structures: AVLs, HashMaps, KMP, Boyer-Moore, BST Trees, Kruskal's Algorithm, Dijkstra's Algorithm Hardware Programming: RISC-V, Assembly, Memory Management, Firmware Development, C, DE-10, FPGA

SKILLS

Programming: TypeScript, Python, Java, C/C++, Perl, Assembly (RISC-V)

Digital Design: VHDL, Verilog, SystemVerilog

Hardware: RISC-V, CAD, Circuit Analysis, Computer Architecture, Firmware, KiCAD, Systems Architecture

PROJECTS

MyGPT2 - Recreating OpenAI's GPT-2 Model

Sep. 2023 – Jun. 2024

- Developed a GPT-2 model from scratch using PyTorch, emulating the capabilities of OpenAI's ChatGPT.
- Achieved 92% perplexity reduction compared to the baseline model.
- Successfully debugged and evaluated models, reducing latency by 30% to optimize real-time performance on GPU.

Plender – Mobile App for Better Time Management

Jun. 2024 – Sep. 2024

- \bullet Developed a cross-platform mobile app using React Native, with 95% shared codebase for Android and iOS.
- Optimized React state management, eliminating 98% of full-page re-renders and improving UI speed by 40%.
- Integrated SQLite for offline data storage, enabling seamless functionality and ensuring 100% sync integrity.

RISC-V ALU

Sep. 2024 – Dec. 2024

- Used SystemVerilog to create an ALU module for a custom single core RISC-V CPU for SiliconJackets@GT.
- Collaborated with other module divisions to ensure interoperability of the Hardware Architecture and ALU.
- Improved efficiency using rigorous logic design and testing for Hardware Validation and Debugging (Test Engineering).

EXPERIENCE

AI Foundations Teaching Assistance

Jan. 2025 – Present

Undergraduate TA

Atlanta, GA

- Lead a studio lab session to help students apply what they've learned about machine learning with PyTorch.
- Manage 20 students to teach them concepts and verify results they get from their training, such as Neural Nets.
- Successfully balance working with 6 other teaching assistance to ensure fairness and balance.

SiliconJackets@GT

Sep 2024 – Present

 $Digital\ Design\ Engineer\ \ \ Web\ Designer$

Atlanta, GA

- Designed and implemented the ALU module for a custom RISC-V CPU using SystemVerilog.
- Analyzed the RISC-V architecture documentation to enhance processor design and functionality.
- Simulated and verified processor functionality with Verilog, improving digital circuit reliability and performance.
- Additionally contributed as a Web Designer, enhancing the team's online presence through WordPress.

Sharc Lab@GT

Aug. 2022 – May. 2023

Student Research Intern

Atlanta, GA

- Contributed to the development of Implicit Neural Representation using PyTorch for software-hardware co-design.
- Analyzed and synthesized research papers to identify and implement potential algorithmic enhancements.
- Utilized communication skills to effectively work and convey ideas with lab members and professors.
- Collaborated with graduates, undergraduates, and professors to leverage expertise in EDA and GNN research.