CSE 436/536 Assignment 2:

2-Bit Carry Ripple Adder Design Using

Pre-designed Logic Cells

Deadline: 22/11/2024 23:59

Objective:

In this project, students will design a 2-bit Carry Ripple Adder using previously designed logic cells (NAND, NOR, and Inverter) from the last assignment. The primary goal is to implement this design in **Magic VLSI** and verify its functionality using **SPICE simulation**. Students are encouraged to focus on optimizing the design for minimal area usage while ensuring correct operation.

Requirements:

1. **Design Structure:**
    - Implement a 2-bit Carry Ripple Adder using the NAND, NOR, and Inverter cells designed in the previous assignment.
    - Ensure proper connections between the stages to achieve the desired carry ripple structure.
2. **Implementation in Magic:**
    - Layout the design using **Magic VLSI**.
    - Focus on minimizing the layout area while maintaining clear and functional connections.
3. **SPICE Simulation:**
    - Use **SPICE** to verify the correct addition functionality of your design.
    - Test cases should include all possible 2-bit input combinations to demonstrate accurate addition and carry propagation.
4. **Optimization:**
    - Aim to minimize the layout area of your design.
    - Clearly document any strategies used to optimize the design for area efficiency, such as compact cell placement or optimized interconnections.

Deliverables:

- **Magic Layout:** Submit the complete layout file from Magic.
- **SPICE Simulation Results:** Provide the SPICE netlist and simulation output showing the correctness of addition for all input combinations.
- **Report:** Include a brief report documenting your design approach, layout optimization strategies, and SPICE verification results.

Evaluation Criteria:

- **Functionality:** Correctness of the 2-bit addition operation.
- **Optimization:** Efficiency of layout in terms of area.
- **Documentation:** Clarity and completeness of the report, including design steps, challenges, and results.

Good luck, and focus on compact and efficient design principles while leveraging your previous logic cell work!