TUNKU ABDUL RAHMAN UNIVERSITY OF MANAGEMENT AND TECHNOLOGY

FACULTY OF COMPUTING AND INFORMATION TECHNOLOGY

ACADEMIC YEAR 2024/2025

OCTOBER EXAMINATION

BACS1024 INTRODUCTION TO COMPUTER SYSTEMS

WEDNESDAY, 23 OCTOBER 2024 TIME: 9.00 AM – 11.00 AM (2 HOURS)

BACHELOR OF COMPUTER SCIENCE (HONOURS) IN DATA SCIENCE

BACHELOR OF INFORMATION TECHNOLOGY (HONOURS) IN INFORMATION SECURITY
BACHELOR OF INFORMATION TECHNOLOGY (HONOURS) IN INTERNET TECHNOLOGY
BACHELOR OF INFORMATION TECHNOLOGY (HONOURS) IN SOFTWARE SYSTEMS DEVELOPMENT

BACHELOR OF SOFTWARE ENGINEERING (HONOURS)

Instructions to Candidates:

Answer **ALL** questions. All questions carry equal marks.

BACS1024 INTRODUCTION TO COMPUTER SYSTEMS

Question 1

a) Perform the following operations.
(If the expression is valid, show your working steps clearly. If the expression is invalid, state the reason.)

(i) Convert 255_{10} to an octal number. (2 marks)

(ii) Convert OCT_{16} to a binary number. (2 marks)

(iii) Add 33.625_8 and 25.625_8. Then, convert your answer to a hexadecimal number. (3 marks)

(iv) Multiply FEB_{16} and $C1_{16}$. Then, convert your answer to a decimal number. (3 marks)

b) Assuming that an 8-bit system is applied. Answer the following questions. *(You are required to show your working steps clearly.)*

$$(-64_{10}) + (-44_{10})$$

(i) Solve this operation using the Two's Complement method. (5 marks)

(ii) Verify your answer using a signed decimal value. Then, comment on the validity of your answer. (2, 3 marks)

c) A binary IEEE754 single precision notation is shown below:

$$11000001011001000000000000000000_2$$

Given that:
- The excess-127 notation is applied.
- The implied binary point is to the right of the first bit of the mantissa.
- The "1" in the sign position represents a negative number while the "0" in the sign position represents a positive number.

Convert the binary IEEE754 single precision notation given above to a decimal floating-point number. *(You are required to show your working steps clearly.)* (5 marks)

[Total: 25 marks]

Question 2

a) Assume that the following instructions are found at the given locations in computer memory.

Program Counter: 55
Value in memory location 55: 580 (LOAD)
Value in memory location 56: 181 (ADD)
Value in memory location 57: 382 (STORE)

. . .

Value in memory location 80: 17
Value in memory location 81: 49
Value in memory location 82: 00

During the computer instruction execution, the contents of the *Instruction Registers (IR), Program Counter (PC), Memory Address Register (MAR), Memory Data Register (MDR) and Accumulator (A)* change accordingly. Examine and show the changes in the contents of the IR, PC, MAR, MDR and A respectively during the execution of the following instructions respectively. *(You are required to show your working steps clearly.)*

(i) Instruction 55 (5 marks)

(ii) Instruction 57 (5 marks)

b) Given that a program is coded to perform sorting on a large group of numbers. The entire group of numbers is transferred from an external hard disk drive to computer memory. Then sorting is performed in memory. Upon completion, the sorted numbers are stored back on the external hard disk drive for future reference.

(i) Suggest the most appropriate type of computer Input/Output (I/O) handling technique to facilitate the operation above. Then, justify your answer. (5 marks)

(ii) Explain the working of the Input/Output (I/O) handling technique that you have suggested in Question 2 b) (i). Support your answer with a diagram. (5 marks)

c) The following list of memory addresses was found in the respective registers.

Code segment register	:	2537_{16}
Data segment register	:	3526_{16}
Stack segment register	:	7585_{16}
Stack pointer register	:	$AABB_{16}$
Destination index register	:	$CCDD_{16}$
Instruction pointer register	:	$EEFF_{16}$

Identify the segment address register and offset address register used to hold the address of the next instruction to be executed in the memory segment. Then, calculate the absolute address accordingly. *(Show your final answer in a 20-bit hexadecimal number format.)* (2, 3 marks)

[Total: 25 marks]

Question 3

a) Given the following scenarios, suggest the most appropriate type of computer network topology implementation for each of them. Justify your answer.

(i) A small sized enterprise is connecting all its 50 desktop computers directly to a central hub and a print server. (5 marks)

(ii) Alex is connecting his laptop computer to his own printer to facilitate the assignment report printing for a less expensive implementation. (5 marks)

b) Given that the computer memory is partitioned as P1 through P5 with the partition size of 300KB, 200KB, 100KB, 500KB and 400KB and the job labelled as J1 through J4 with process size of 140KB, 240KB, 440KB and 40KB respectively.

Show how the jobs could be allocated in the memory and calculate the total internal fragmentation generated when the following memory allocation algorithms are applied respectively. *(You are required to write your answer in the table format shown below.)*

(i) First fit memory allocation algorithm. (5 marks)

(ii) Best fit memory allocation algorithm. (5 marks)

Table format:

Memory Partition	Memory Partition Size (KB)	Job	Job Size (KB)	Internal Fragmentation (KB)

c) In the context of computer system software, give **ONE (1)** characteristic of an embedded operating system. Give and explain **TWO (2)** examples of embedded operating system. (1, 4 marks)

[Total: 25 marks]

Question 4

a) Consider a list of processes named A, B, C and D arriving in order and having the CPU cycle time as shown in Table 1 below.

Process	Arrival Time (ns)	CPU Cycle Time (ns)
A	0	3
B	1	1
C	2	4
D	4	2

Table 1: List of processes

(i) Draw the Gantt Chart using the Shortest Job First (SJF) and Shortest Remaining Time (SRT) process scheduling algorithms respectively. Then, calculate the *Average Turnaround Time* and *Average Waiting Time* accordingly. *(You are required to write your answer in the following table format.)* (4, 4 marks)

Table format:

Process	Arrival Time (ns)	CPU Cycle Time (ns)	Finish time (ns)	Turnaround time (ns)	Waiting time (ns)

(ii) Which process scheduling algorithm offers better CPU utilisation? Justify your answer. (2 marks)

b) Assuming that a memory consists of **THREE (3)** empty page frames. Given the page fault trace analysis has been conducted as below. Answer the following questions.

Page no.	**1**	**3**	**5**	**5**	**7**	**2**	**2**	**7**	**5**	**3**	**8**	**5**
Frame 1	(1)	1	1	1	(7)	7	7	7	7	7	(8)	8
Frame 2		(3)	3	3	3	(2)	2	2	2	(3)	3	3
Frame 3			(5)	5	5	5	5	5	5	5	5	5

(i) Identify the name of the page replacement algorithm implemented. (2 marks)

(ii) Based on your answer to Question 4 b) (i), elaborate on how the mentioned page replacement algorithm decide which page to replace. (2 marks)

(iii) Based on your answer to Question 4 b) (i), explain **ONE (1)** advantage and **ONE (1)** disadvantage of the mentioned page replacement algorithm. (4 marks)

(iv) Calculate the percentage of page faults. (2 marks)

c) It is often stated that computer networks play a crucial role in facilitating business operations. Do you agree with this statement? Provide **TWO (2)** reasons for your answer. (1, 4 marks)

[Total: 25 marks]