Noted by Hanlin CAI

No. 2023/01/07

Date

EE302FZ 2021 Paper.

(18)

Q1. (a) I/O device : 0x8000 – 0x81FF

(i) range $= (0x1FF)_{16} = (511)_{10}$ $\rightarrow 512$

I/O range : 511 + 1 = 512.

(ii) 8 Bit CPU : (8×1024 – 1 = 01FF)

ROM	0x0 – 0x3FF	(1024B)	1K	
EEPROM	0x1000 – 0x17FF	(2KB)	4K	2/4
EEPROM*	0x1800 – 0x1FFF	(2KB)		
RAM ①	0x4000 – 0x47FF	(2KB)	8K	2/8
RAM ②*	0x4800 – 0x5FFF	(6KB)		
I/O	0x8000 – 0x81FF	($\frac{1}{2}$KB)	0.5K	
UART	0x8000 – 0x8003			

没有即 unused

有,但没有用 unused-RAM

ROM

unused

EEPROM ①

u–EEPROM ②

unused

RAM

unused – RAM ← UART在最上面.

IO

(iii) Active-low chip

boot loader ROM
0x0 → 0 0 0 00 0000 0000
0x3FF → 0 0 0 11 1111 1111

EEPROM
0x1000 → 1 0 000 0000 0000
0x17FF → 1 0 111 1111 1111

UART
0x8000 → 1 000 0000 0000 0000
0x8003 → 1 000 0000 0000 0011

(If Active low chip) :

$\sim ROM\_CS = \sim(\sim A_{15} \sim A_{14} \sim A_{13} \sim A_{12} \sim A_{11} \sim A_{10})$

$\sim EEPROM\_CS = \sim(\sim A_{15} \sim A_{14} \sim A_{13}\ A_{12} \sim A_{11})$

$\sim UART\_CS = \sim(A_{15} \sim A_{14} \sim A_{13} \sim A_{12} \sim A_{11} \sim A_{10} \sim A_{9} \sim A_{8} \sim A_{7} \sim A_{6} \sim A_{5} \sim A_{4} \sim A_{3} \sim A_{2})$.

注:题目中要高位, Active High 因此这里不用取反 (原先自行设低)

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No. 3.3V → 4.7 kohm.

$\begin{cases} V_{cc} \text{ 接} \rightarrow \text{Pulled-up} \\ \text{GND 接} \rightarrow \text{pulled-down} \end{cases}$

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Q1. (b) RC3 → high → 1 (no key)

(i) RC0 → 0 RC1 → 0 RC2 → 0

(按扭 press → 通电)

(ii) RC3 → high → 1. key 3

RC0 → 0 RC1 → 0 RC2 → 1

(iii) Resistor R1 R2 R3 provide the default state to scan lines. So if the resistor are pulled to GND, they will have default state of 0V, while if resistors are pulled high, they will have state of supply. (i.e. 3.3V or 5V).

The resistor values should be suitable, the pull-up should not create loading effect along with the parasitic capacitance of traces, and, also should not act as weak pull-up.

{ even 隅 → bit = 0
{ odd 奇 → bit = 1

Q2. 9600, 8, E, 2.

(10)

(a) 9600 symbol/sec 8 data bit/per word even parity 2 stop bit.

```
init()
    // configue a pin of I/O part for output and call it pin Tx.
    set Tx = MARK // initially at the idle or stop level.

transmitChar(val)  // start bit, 8 data bits, Even parity 2 stop bit.
    set Tx = SPACE, evenBit = 0
    delay(SYMBOL_PERIOD).
    for i=0 to 7                                          (set not)
        if bit i of val is 1, set Tx = MARK, evenBit = ~evenBit
        else, set Tx = SPACE
        delay(SYMBOL_PERIOD - LOOP_PERIOD)
    Tx = evenBit
    Tx = MARK  // Stopbit x 2.
    delay(SymBOL_PERIOD) * 2
```

对 → Asyn & Syn 同.

(8)

(c) ① In Syn, a common clock is shared by the transmitter and receiver, while in Asyn, each charcter contains its own start/stop bits.
② In Syn, data is sent in frames/blocks. In Asyn, is bytes/characters.
③ In Syn, there is no gap between the data. But in Asyn there is a gaps due to the start/stop bit feature.

→ SPI & I2C.

① SPI is full duplex, I2C is half duplex
② SPI is multi master/slave, I2C is ~~sig~~ single master.
③ SPI is 3 (4) wire protocol, I2C is 2 wire.
④ SPI is faster than I2C.
⑤ I2C has extra overhead start and stop bit, while SPI does not.

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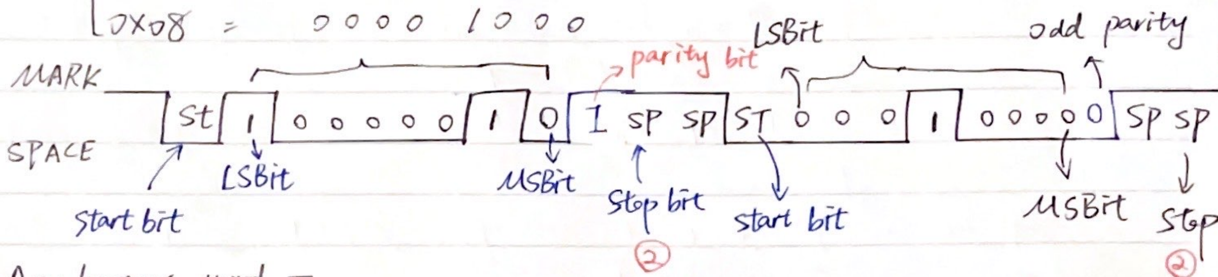
Q2. (b) 15

(i) 9600 8 O 2.

baudRate = 9600 symbol/sec
numDataBitsPerWord = 8 data bits/word
O → parity = odd parity bit
numStopBits = 2 stop bit/per asychronous word

(ii) 0X41 = 0100 0001
0X08 = 0000 1000



Asychronous word =

(iii) 1 start bit + 8 word bit + 1 parity bit + 2 stop bit = 12 bit

$12 \times \frac{1}{9600} = 0.00125\ s$

2 word need 0.0025 s $N = \frac{1}{t} = 400$ sample/second

Q3 (a) $V_{out} = V_{DD}\left(\frac{R_1}{R_1 + R_{FSR}}\right)$. 8bit ADC

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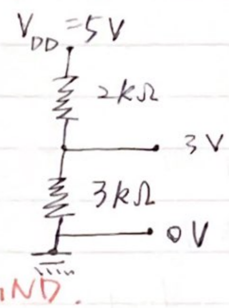
(i) sol.

bit per sample give us the resolution or step size of ADC
Voltage reference value determine the voltage range which is
divided into 2^8 step.

2^8.

(ii) We choose 0~3V



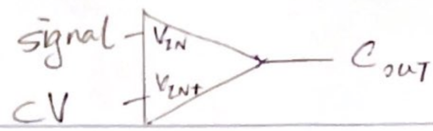
(iii) min voltage step size $= \frac{3}{2^8} = 0.0117\ V$ (ADC signal resolution)

(iv) $5 \times \frac{10K}{(10+20)K} = 1.66V \rightarrow N = \frac{1.66}{0.0117} = 142$ (ADC value)

(v) $N = 208$ (Let the resistance be X.)

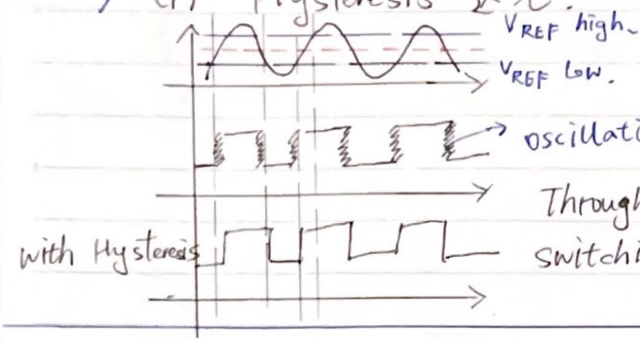
$208 \times 0.0117 = 5 \times \frac{10}{10+X}$

$X = 10.5457 \longrightarrow R = 10.55\ k\Omega$



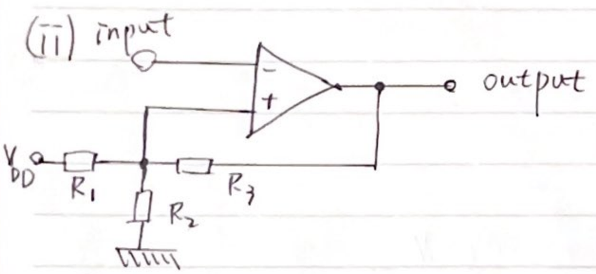
Q3 (b) 2 → 4 (2.5) (18)

(i) Hysteresis 迟滞.



Through Hysteresis, we can prevent excessive switching when exposed to noisy signals.

(ii)



$$\begin{cases} \dfrac{R_3}{R_1} = \dfrac{V_{low}}{V_{high} - V_{low}} \\[2ex] \dfrac{R_2}{R_1} = \dfrac{V_{low}}{V_{DD} - V_{high}} \end{cases}$$

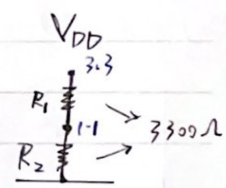
To prevent oscillation near reference level, basic solution to implement 2 thersholds : low & high.

如果是5V，换个数据代入计算即可（过程不变！）

(iii) $V_{DD} = 3.3$ $V_{SS} = 0V$ threshold Voltage → 1.1 V

Noise $\leq \pm 0.2V$ → $\begin{cases} V_{low} = 1.1 - 0.2 = 0.9\ V \\ V_{High} = 1.1 + 0.2 = 1.3\ V \end{cases}$

$\pm 0.3V$



Ref circuit should not ~~end~~ exceed 1 mA.

Hence, we choose $R_1 + R_2 \approx \frac{3.3V}{1mA} = 3300\ \Omega$

$\therefore R_1 = (2R_2) = 2200\ \Omega$ $(R_2 = 1100\ \Omega)$

$$\begin{cases} \dfrac{R_2}{R_1} = \dfrac{0.9}{3.3 - 1.3} = \dfrac{9}{20} \longrightarrow R_2 = \dfrac{9}{20} R_1 = 990\ \Omega. \checkmark \\[2ex] \dfrac{R_3}{R_1} = \dfrac{0.9}{0.4} = \dfrac{9}{4} \longrightarrow R_3 = \dfrac{9}{4} R_1 = 4950\ \Omega \end{cases}$$

Therefore $R_1 = 2200\ \Omega$ $R_2 = 990\ \Omega$ $R_3 = 4950\ \Omega$

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2019 MU Paper ← 注意本题数据.

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Q4. (a) $V_{out} = \text{scale} \times V_{DD}/24$ $\qquad V_{DD} = 3.3\text{ V}$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad$ VCON → 0xEB

sol.

(i) $0xEB \rightarrow 1110\ \underbrace{1011}_{1\text{-}4}$

bitmask → 0001 1110 → 0x1E

(ii) oldScale = (VCON & bitmask) >> 1

```
  0b 1110 1011
     0001 1110
  -------------
     0000 1010 >> 1 ——→ 0b(0000 0101) = 0x05
```

(iii) $1.375\text{ V} = \text{scale} \times \frac{3.3}{24} \rightarrow \text{Scale} = 10$

newScale $= (10)_{10}$ = 0xA = 0b(0000 1010)

VCON = (VCON & ~mask) | (newScale << 1)

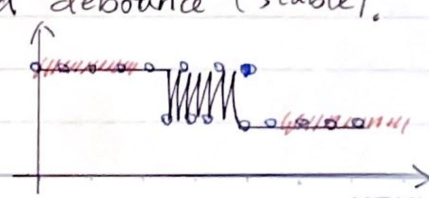
```
  0b 1110 1011
   ~(0001 1110) = 1110 0001   &
  ---------------------------
               (1110 0001)

  0b 0000 1010 << 1 = (0001 0100)   |
                    ↓
       0b(1111 0101) = 0xF5
```

VCON final = 0b(1111 0101).

(iv) Software debounce.

① Count based Measure switch value repeatedly, value must be same for N polls to be considered debounce (stable).



② Digital filter based

Digital simulation of low pass filter (with schmitt trigger).

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Q4(b) max timeout duration

(i) $f_{osc} = 10\,MHz$

$f_{src} = \frac{f_{osc}}{4} = \frac{10}{4}\,MHz \rightarrow T_{scr} = \frac{1}{f} = 0.4\,(\mu s)$

① Largest timeout $= 0.4 \times 8 \times 2^{16}\,\mu s = 209715.5\,\mu s$ timeout duration

② 分辨率 Resolution $= 0.4 \times 8 = 3.2\,\mu s$ timer resolution.

(ii) $\begin{cases} f_A = 10\,Hz \\ t_A = 100\,ms \end{cases}$ $\begin{cases} f_B = 8\,Hz \\ t_B = 125\,ms \end{cases}$

greatest common divisor (gcd) = 25 ms = tick time

$\begin{cases} t_A = 4 \text{ tick} \\ t_B = 5 \text{ tick} \end{cases}$

(iii) tick period = 25 ms $\quad \frac{2.5 \times 10^4}{0.4 \times 2^{16}} = 0.9537 < 1$

不需要预分频 $\longrightarrow \frac{2.5 \times 10^4}{0.4} = 62500$

$2^{16} - 62500 = 3036$

(iv)

```
taskA() =
    static count = TASK_TICKS    // 4 ticks
    decrement count
    if count is 0 :
        set count = TASK_TICKS
        mainBody Of TASKA().
```

Best Wishes for you!

—Hanlin CAI

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