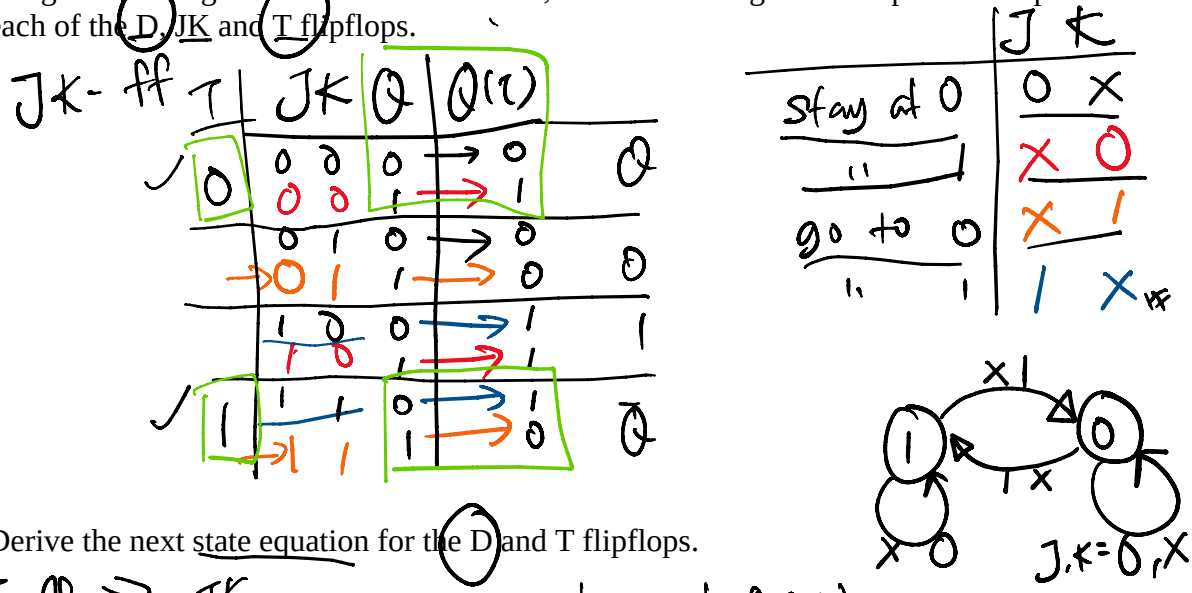
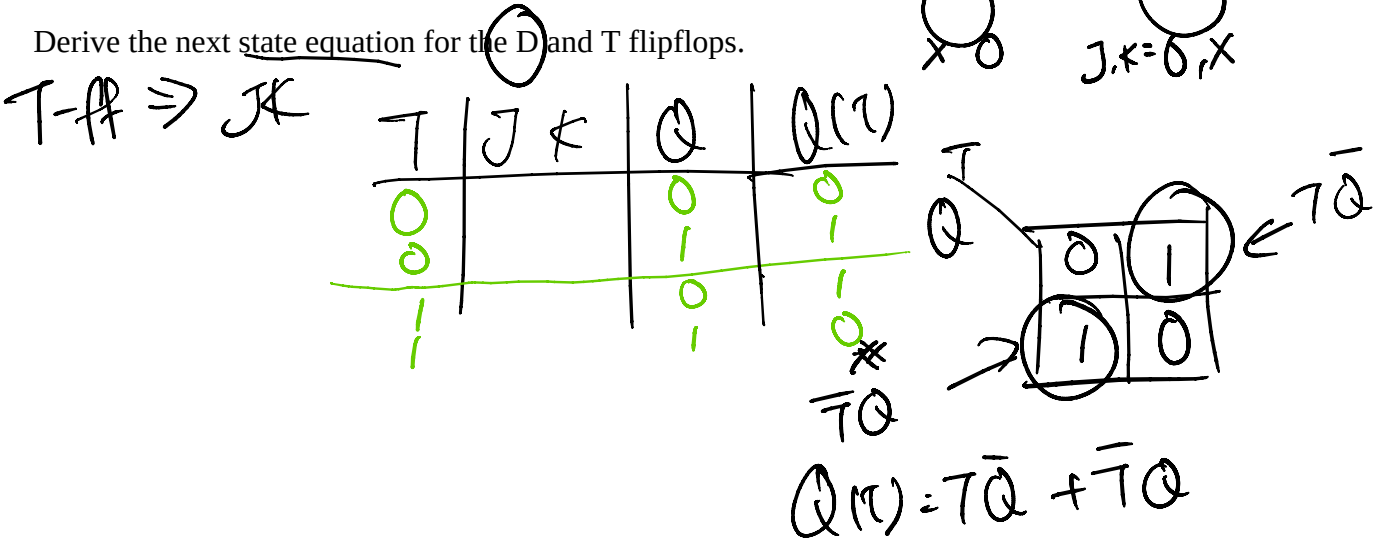
Tutorial Sheet 5 – *Sequential Logic & Flipflops*

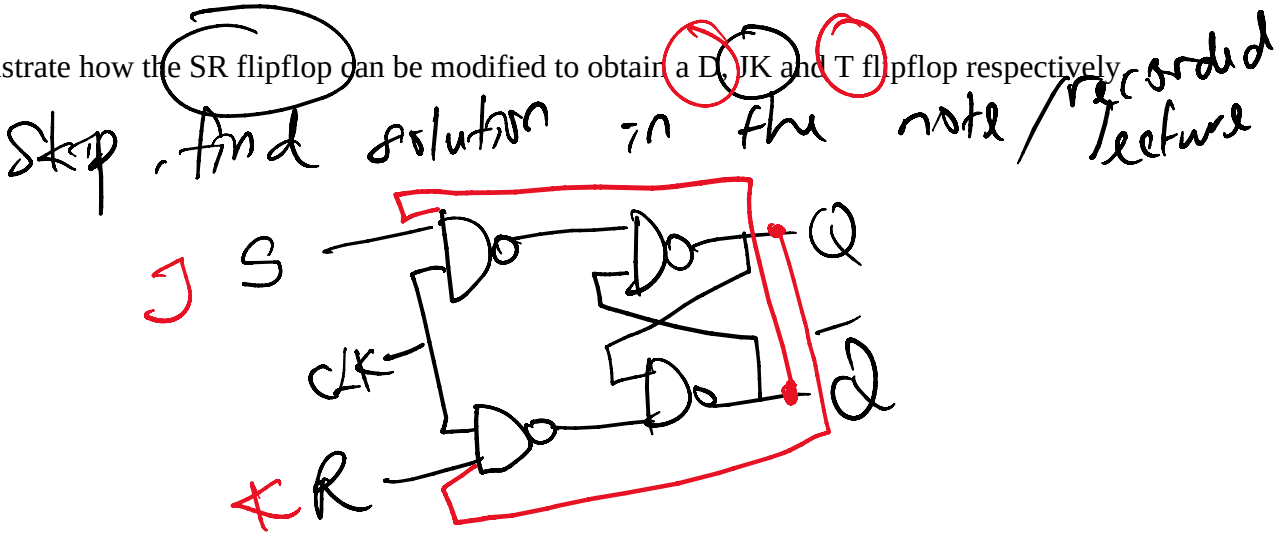
1. It is shown in the notes how the operation of a synchronous SR flipflop can be expressed using a state diagram. In a similar manner, use a state diagram to express the operation of each of the D, JK and T flipflops.



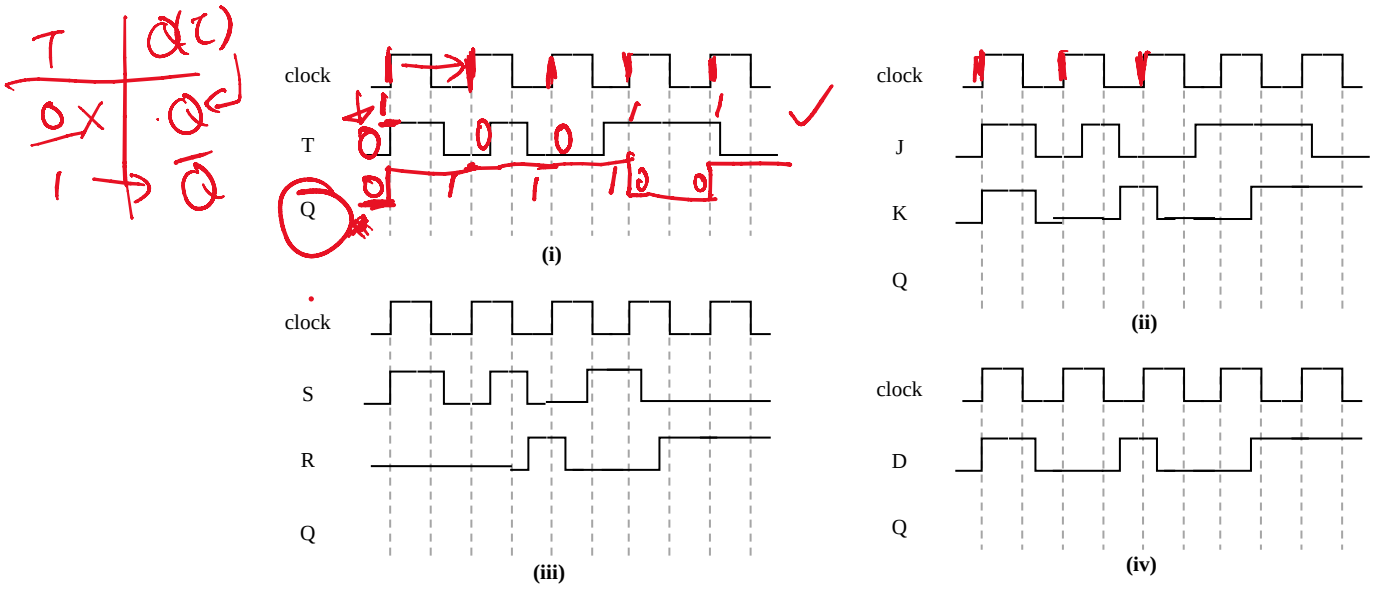
2. Derive the next state equation for the D and T flipflops.



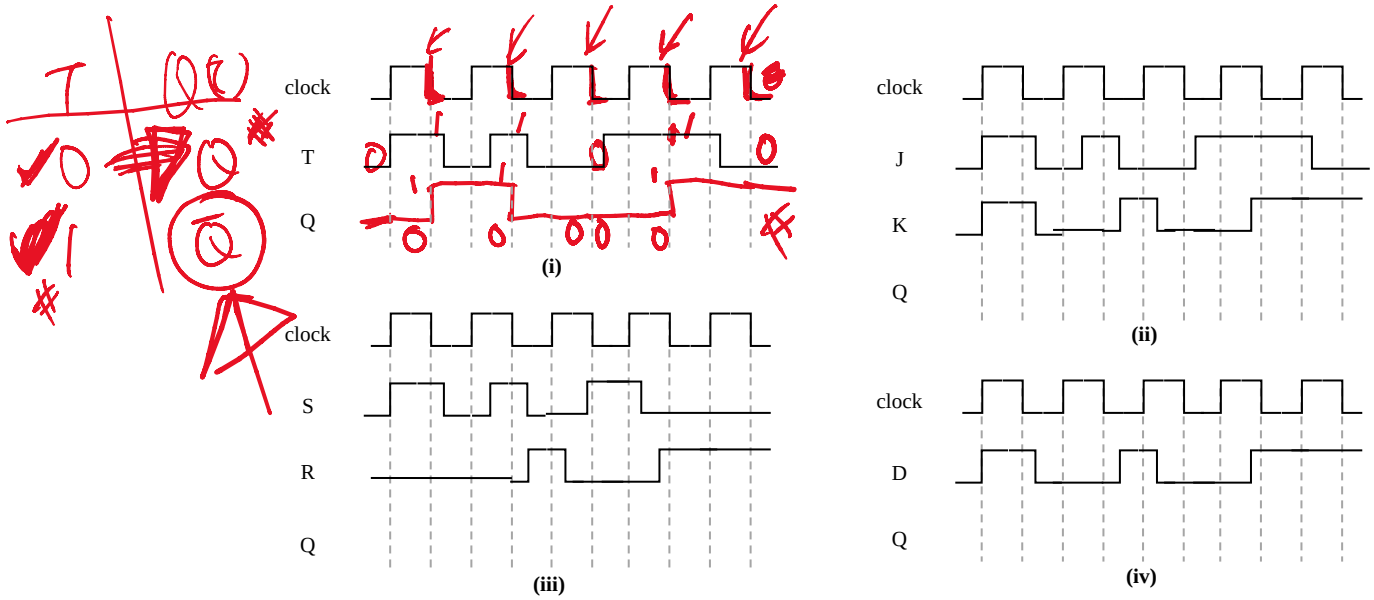
3. Illustrate how the SR flipflop can be modified to obtain a D, JK and T flipflop respectively.



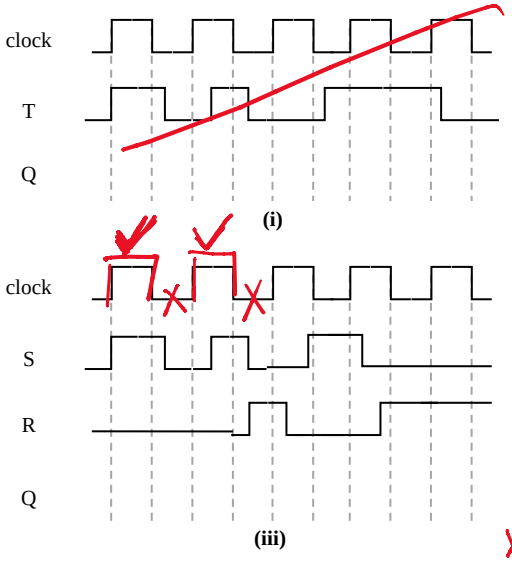
4. Complete the following timing diagrams given that the devices in question are positive edge-triggered flipflops. Assume that the output starts in a LOW state.

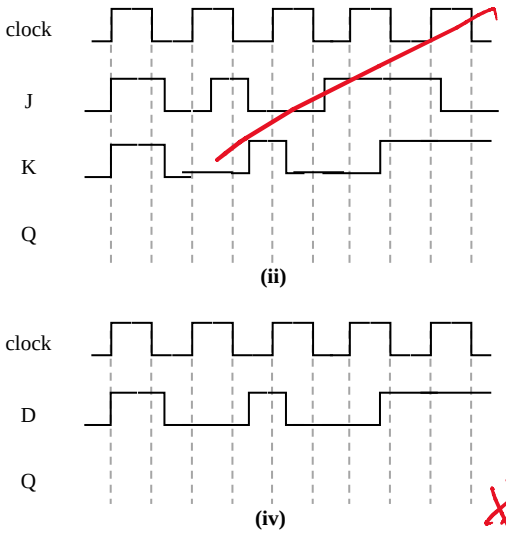


5. Repeat Q4, given that the devices in question are negative edge-triggered flipflops.



6. Repeat Q4 for parts (iii) and (iv), given that the devices are latches and that the clock signal is now an enable signal in each case.





7. It is shown in the notes how a single D flipflop can be used to obtain the *divide-by-2* function. Draw out a circuit diagram, using D flipflops, to obtain a *divide-by-8* function. Provide a timing diagram (i.e. input and output waveforms) to illustrate the actual operation of your circuit.