EE302FZ Hanlin CAI 20122161 83200211 No. NO.32 Date

I choose Q1 Q2 Q3 ! Thank you! Q1(a)

Q1. (a) sol As the question given, we know :

RAM 0x0 (4/6 kiB) 0x0 – 0xFFF – 0x17FF
boot loader ROM (highest 512B) 0x1E00 – 0x1FFF
EEPROM 0x1800 (1 kiB) 0x1800 – 0x1BFF
I/O 0x1C00 – 0x1CFF (UART 4, Inerial Senser 10).

(i) range of I/O is 0x1C00 – 0x1CFF ⟶ range = 0xFF
Hence, range = (255)
So number = 255^{10} + 1 = 256 (in Dec.)

(ii) UART = 0x1C00 – 0x1C03 (0x1C04–0x1C05 can not use)
Sensor = 0x1C06 – 0x1C0F (suitable address)

Therefore, the address map is :

RAM	0x00 – 0xFFF	①
unused RAM	0x1000 – 0x17FF	②
EEPROM	0x1800 – 0x1BFF	③
UART	0x1C00 – 0x1C03	④
can not use////////	0x1C04 – 0x1C05	⑤
Inerial Sensor	0x1C06 – 0x1C0F	⑥
unused I/O	0x1C10 – 0x1CFF	⑦
////Unused////////	0x1D00 – 0x1DFF	⑧
boot loader ROM	0x1E00 – 0x1FFF	⑨

(iii) algebraic expression: Active Low !

① boot loader ROM { 0x1E00 = (0 0 0) 1 1110 0000 0000
0x1FFF = (0 0 0) 1 1111 1111 1111

$\sim CS\_ROM = \sim(A_{12} A_{11} A_{10} A_9)$

② EEPROM { 0x1800 1 1000 0000 0000
0x1BFF 1 1011 1111 1111 (Active Low)

$\sim CS\_EEPROM = \sim(A_{12} A_{11} \sim A_{10})$

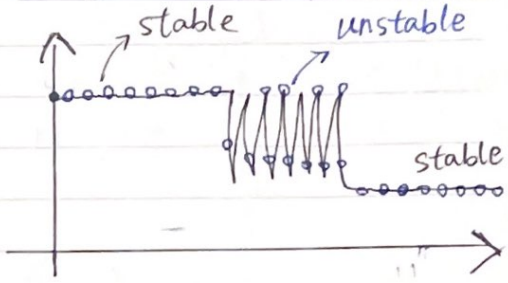
③ Inerial Sensor { 0x1C06 [1 11 00 0000 011] 0 — 0x1C08
0x1C0F [1 11 00 0000 111] 1

$\sim CS\_Sensor = \sim(A_{12} A_{11} A_{10} \sim A_9 \sim A_8 \sim A_7 \sim A_6 \sim A_5 \sim A_4 A_3)$

Q1. (b) sol (i) switch debounce :

① Count based Method : Measure switch value repeatedly value must be same for N polls to be considered stable.

② Digital filter based method : which is using digital simulation of low pass filter (with schmitt trigger) to realize switch debounce



(b) (ii) requirement :

① the bus-aware devices must have tri-state ouputs
② the bus-aware devices must connect with the address bus (or data bus) directly
③ the bus-aware devices have suitable address.

(b) (iii) ADCON0 is ob(1011 0001)
△

We would like to select channel 4.

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Q2(a)

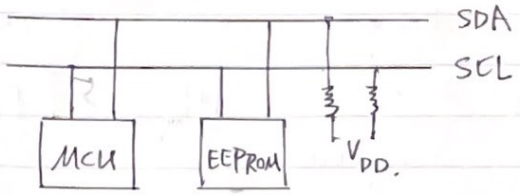
Date Q2(a):

Q2 (a) Two difference between Syn and Asyn is shown as :

(i)

Synchronous	Asynchronous
① A common clock is share by transmitter and receiver.	① While in Asyn, each character contain its own start / stop bits.
② Data is sent in frames / blocks	② Data is sent in bytes / characters.
③ There is no gap between the data	③ There is a gap due to the stop bit.

(ii)

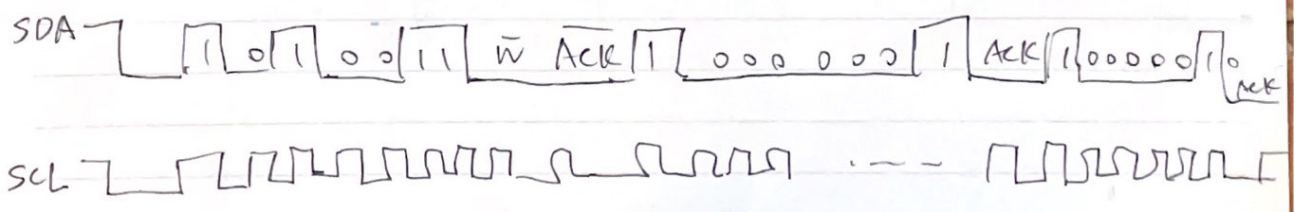


(I^2C).

I_2C protocol :

(iii) ① start
② set EEPROM (address) register 0x53 (slave)
③ write.
④ ACK
⑤ data '0x81' → (0x470) slave
⑥ data '0x82' → (0x481) slave
⑦ Stop

(iv) 0x53 = 0101 0011
0x81 = 1000 0001
0x82 = 1000 0010

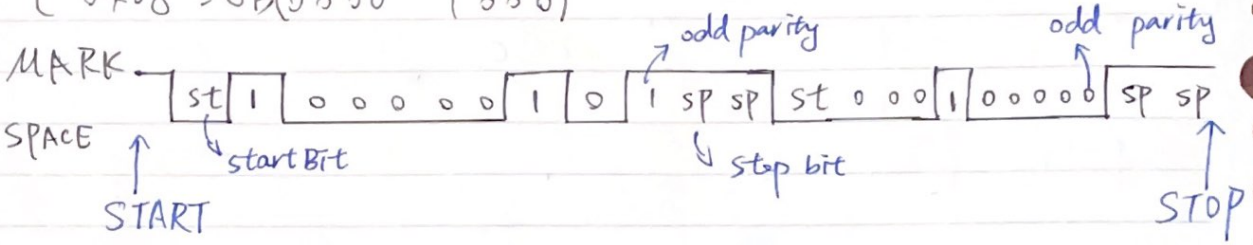


sol. Q2.

Q2 (b) (i) 9600 8 O 2

baudRate = 9600 symbol / sec
numDataBitPerWord = 8 data bit per asychronous word
parity = odd parity bit
numStopBits = 2 stop bit per asychronous word

(ii) 0x41 = 0b(0100 0001)
0x08 = 0b(0000 1000)



(iii) As the diagram given above, one asychronous word
= 1 startBit + 8 word bit + 1 parity bit + 2 stopBit
= 12 bit

Hence $T_1 = 12 \times \frac{1}{9600} = 0.00125\ s$

2 Word need $2T_1 = 0.00250\ s$

Therefore $N = \frac{1}{T} = \frac{1}{0.0025} = 400$ sample / sec

The max rate is 400 (sample / rate.)

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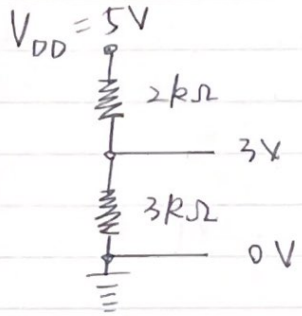
Date Q3.(a)

Q3 (a) sol $V_{out} = V_{DD}\left(\frac{R_1}{R_1+R_{FSR}}\right)$. (8 bits ADC) 2^8

(i) ① The number of bit per sample give us the resolution or step size of ADC. ② Voltage reference value determine the voltage range which is divided into 2^8 step.

(ii) We choose the voltage of 0 ~ 3 V, and the circuit is given as:



(iii) the min voltage step size $= \frac{3}{2^8} = 0.01172$ (V/step)

(iv) $U = 5 \times \frac{10k\Omega}{(10+20)k\Omega} = 1.667$ V

$N_1 = \frac{U}{\text{step}} = \frac{1.667}{0.01172} = 142.2 \approx 142$

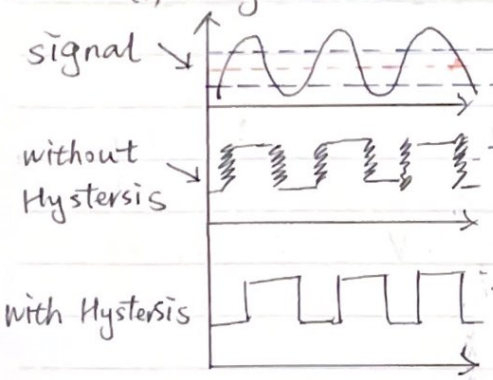
(v) $N_2 = 208$

Hence $208 \times 0.01172 = 5 \times \frac{10}{10+X}$

$\therefore X = 10.545$ Hence $R_{FSR} = 10.55\ (k\Omega)$

Q3 (b) sol.

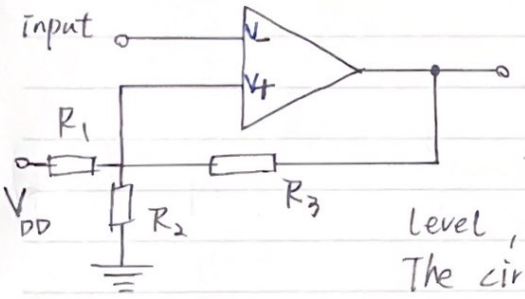
(i) Hystersis



The oscillation due to noise.

Through the comparator hysteresis, we can prevent excessive switching when the signal is exposed to noise.

b(ii) circult is given as:



Among:

$$\begin{cases} \frac{R_3}{R_1} = \frac{V_{low}}{V_{high} - V_{low}} & ① \\ \frac{R_2}{R_1} = \frac{V_{low}}{V_{DD} - V_{high}} & ② \end{cases}$$

To prevent the oscillation near reference level, basic solution is implement 2 thershold. The circult utilizes the three resistance to reduce the oscillation caused by noise, which improve the stability of the whole circult.

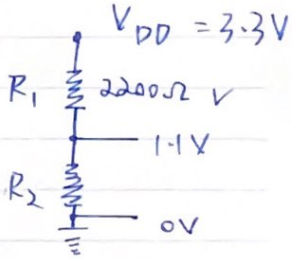
b(iii) $V_{DD} = 3.3V$ $V_{SS} = 0V$ threshold Voltage is 1.1 V

Due to noise is less than $\pm 0.2V$

$$\begin{cases} V_{low} = 0.9V \\ V_{high} = 1.3V \end{cases}$$

And the REF circuit should not exceed 1 mA

Hence $R_1 + R_2 \geq \frac{3.3V}{1mA} = 3300$



According to the diagram, we know $R_1 = 2200\,\Omega$

Hence $\begin{cases} R_2/R_1 = \frac{9}{20} \\ R_3/R_1 = \frac{9}{4} \end{cases} \Rightarrow \begin{cases} R_2 = \frac{9}{20} R_1 = 990\,\Omega \\ R_3 = \frac{9}{4} R_1 = 4950\,\Omega \end{cases}$

Therefore $\begin{cases} R_1 = 2200\,\Omega \\ R_2 = 990\,\Omega \\ R_3 = 4950\,\Omega \end{cases}$

(OVER).