EE204FZ
Lecture 5
Applications of MOSFETs

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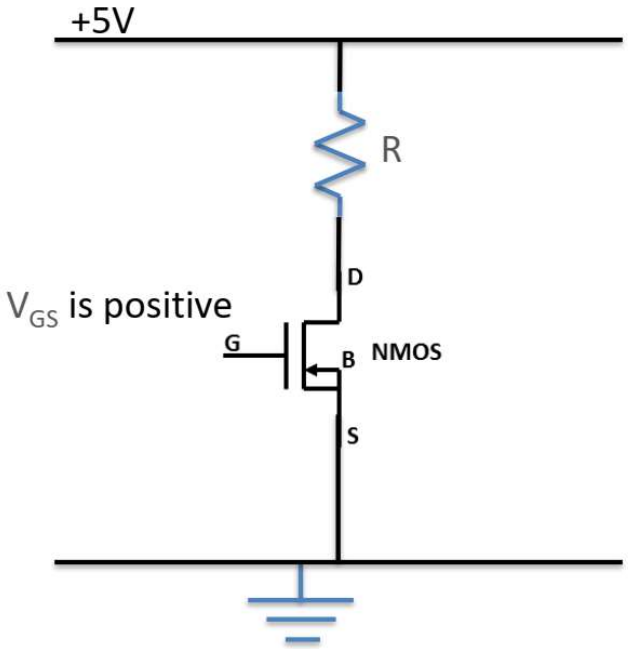
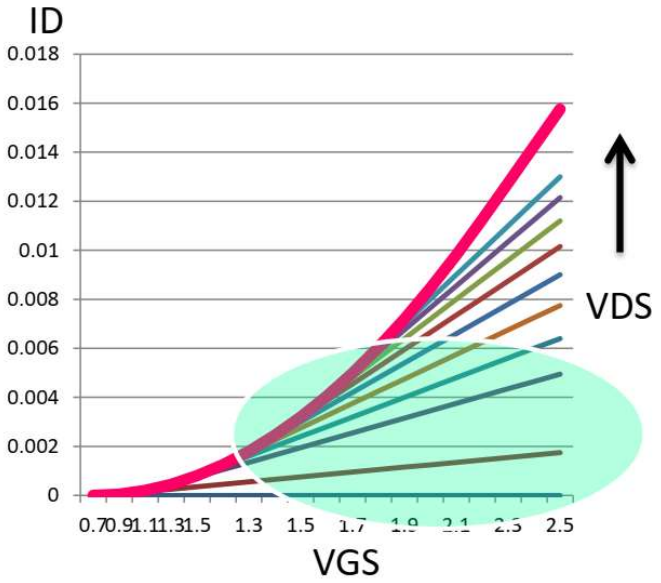
How Can We Use MOSFETs?

- We can use transistors in many ways, but the most common ones are
  - as a resistor;
  - as a switch;
  - as an amplifier (will be discussed in the next section of this course module).
- We will go through each of these briefly and talk about them and show some examples.

As a Resistor

- Consider a device where we want a small DC resistance. Assuming reasonable currents, the voltage dropped across a small resistance will be a small voltage. So V_{DS} is small.
- Normally you would see this in a structure like the following circuit.





Look at the Key Equation

- The first thing is to check what region of the transistor we are in. We said V_{DS} was to be small, so what does this mean?
- If $V_{DS} > V_{GS} - V_T$, then we are in saturation. For a small V_{DS}, we are not likely to be in saturation, but just to be sure, let us pick a voltage for V_{GS} where this is not true:

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

but $R_{DS} = V_{DS}/I_D$,

$$R_{DS} = \frac{V_{DS}}{\mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]}$$

Look at the Key Equation

- Let's make an assumption. The square of a small number is a very small number. Let's remove the $(V_{DS})^2$. It adds a small error, but we can live with that.

$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}$$

in which

- $\mu_n C_{ox} \approx 30 \times 10^{-6}$ A/V^2 (depending on doping, etc);
- W/L is a manufacturing feature, but ratios of 5:1 to 100:1 are common. If you are doing IC design, you can control this;
- V_T is a constant and can range from 0.3 to 2 V.

What Resistances Are Possible?

Let's use the following values:

- $\mu_n C_{ox} \approx 30 \times 10^{-6}$ A/V^2 (depending on doping, etc);
- $W/L = 50$;
- $V_T = 0.5$ V.

$$R_{DS} = \frac{1}{(30 \times 10^{-6})(50)\,(V_{GS} - 0.5)}$$

So therefore for

$V_{GS} = 1$ V	$R_{DS} = 1333\ \Omega$
$V_{GS} = 2$ V	$R_{DS} = 444\ \Omega$
$V_{GS} = 5$ V	$R_{DS} = 148\ \Omega$

If we double W/L, we halve the resistance. Hence, we can make pretty accurate low-value resistors.

What About High-Value Resistances?

- Here we are talking about the saturation region (since if we are in the triode region, $V_{GS} \uparrow$, $R_{DS} \downarrow$);
- We have a large value of V_{DS}, so we need to use the saturation region equation. Ideally, the maximum current is given by

$$I_{D(sat)} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

and the resistance is

$$R_{DS} = \frac{V_{DS}}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2}$$

- This is not working out very nicely for us, but let us plug in some numbers as from before.

What About High-Value Resistances?

- Let's use the following values:
  - $\mu_n C_{ox} \approx 30 \times 10^{-6}$ A/V^2 (depending on doping, etc);
  - $W/L = 50$;
  - $V_T = 0.5$ V.

Remember, $V_{DS} > V_{GS} - V_T$ for saturation region.

	V_{DS} = 1 V	V_{DS} = 2 V	V_{DS} = 3 V	V_{DS} = 5 V
V_{GS} = 1 V	5333	10666	15999	26666
V_{GS} = 2 V	592	1185	1777	2692
V_{GS} = 3 V	213	426	619	1065
V_{GS} = 5 V	65	130	195	325

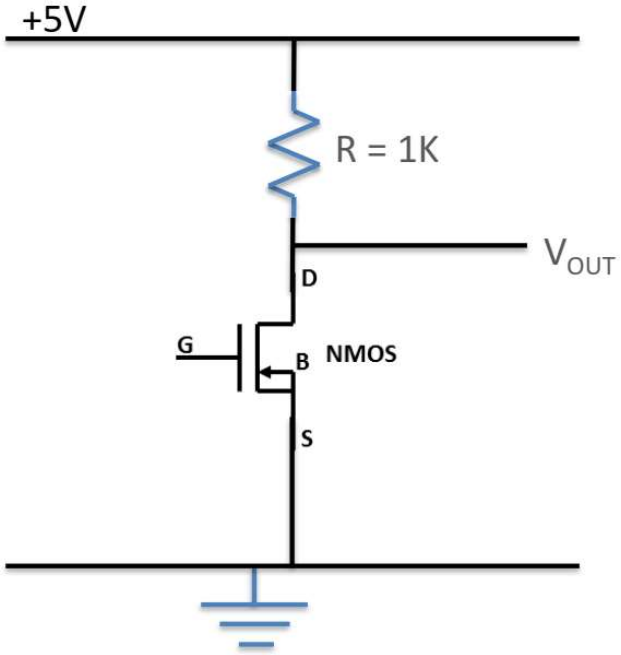
- We can't get good high valued DC resistance from a MOSFET, except under one condition.....

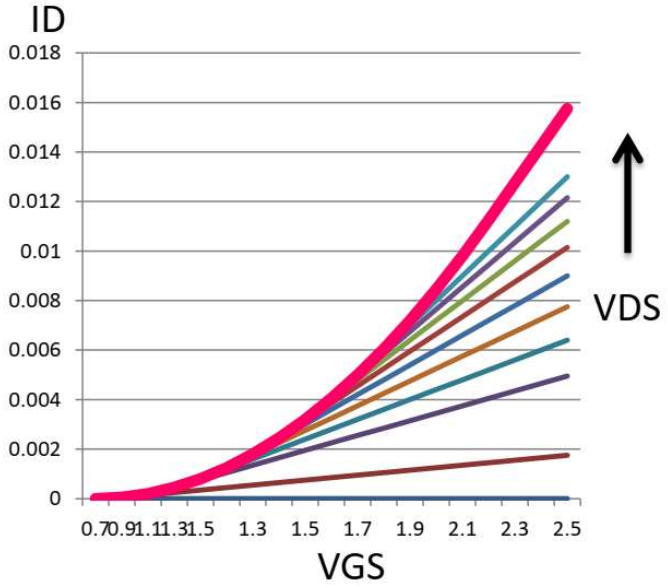
Summary: The Transistor as a Resistor

- If V_{GS} is less than the threshold voltage:
  No current flows, a very high resistance (MΩ);
- If $V_{GS} > V_T$, but V_{DS} is small and we are not in saturation:
  A small, controllable resistance (50 - 500 Ω). This can be made smaller by making V_{GS} bigger or by making the device wider (W/L bigger);
- If $V_{GS} > V_T$, but V_{DS} is large and we are in saturation:
  A very changeable resistor – depending on V_{GS} and V_{DS} and not very large (50 - 50000 Ω).
- So why bother,
  - It is voltage controlled, so we can change it;
  - It can be precise, we can get a resistance exactly TWICE of another, etc;
  - It is smaller than the area we would need to make a resistor in silicon.

The Transistor as a Switch

- In this scenario, we turn the transistor ON as far as possible and then turn it OFF as far as possible. Consider the following circuit:

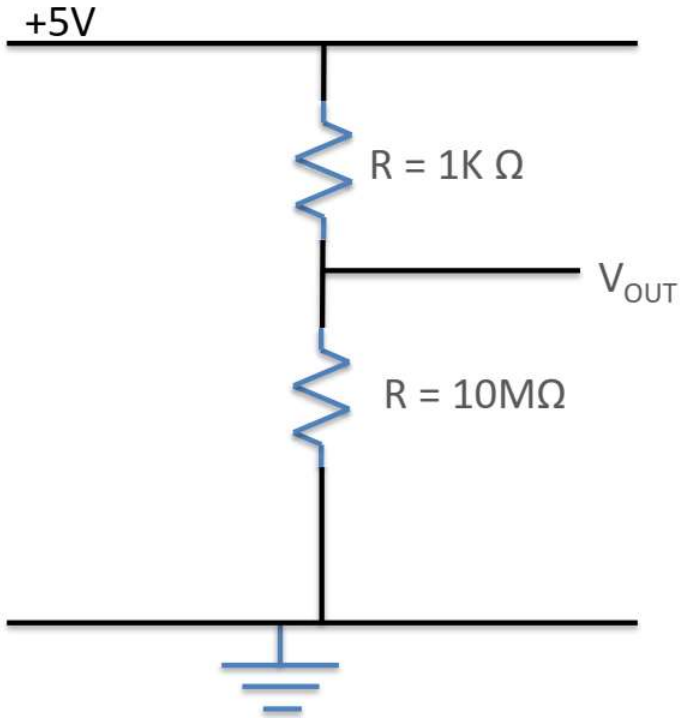




- What happens if I connect G to ground?
- What happens if I connect G to +5 V?

The Transistor as a Switch (OFF)

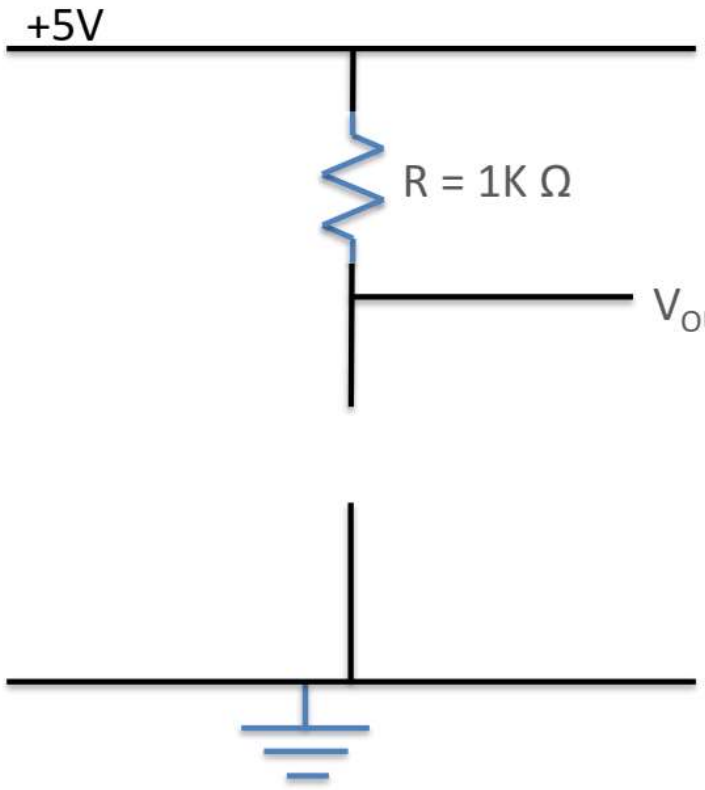
- When the gate is connected to ground, there is no inversion region. There are two back-to-back diodes. No current flows. A very high resistance.



What voltage will I see on V_{OUT}?

The Transistor as a Switch (OFF)

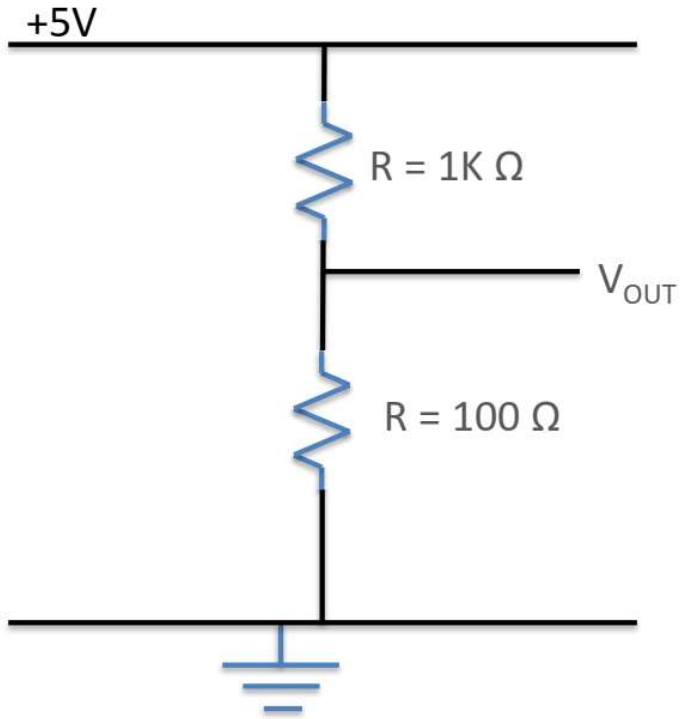
- An easier way to view this is to assume that a turned-off MOSFET is an open circuit.



What voltage will I see on V_{OUT}?

The Transistor as a Switch (ON)

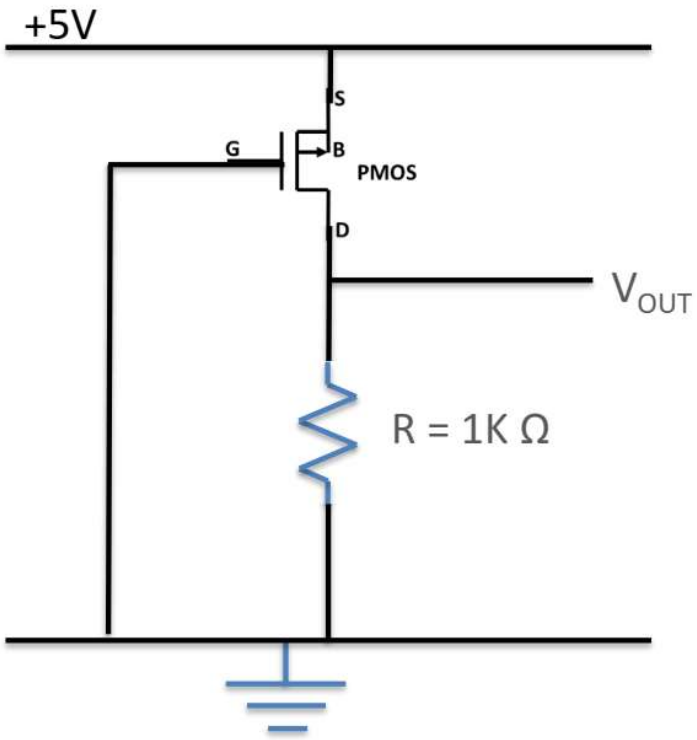
- Now when the GATE voltage is made positive with respect to the source/bulk ($V_{GS} > V_T$), we get an inversion region and we get a resistor defined by the characteristic equation (say 100 ohms). It could be lower depending on the transistor.

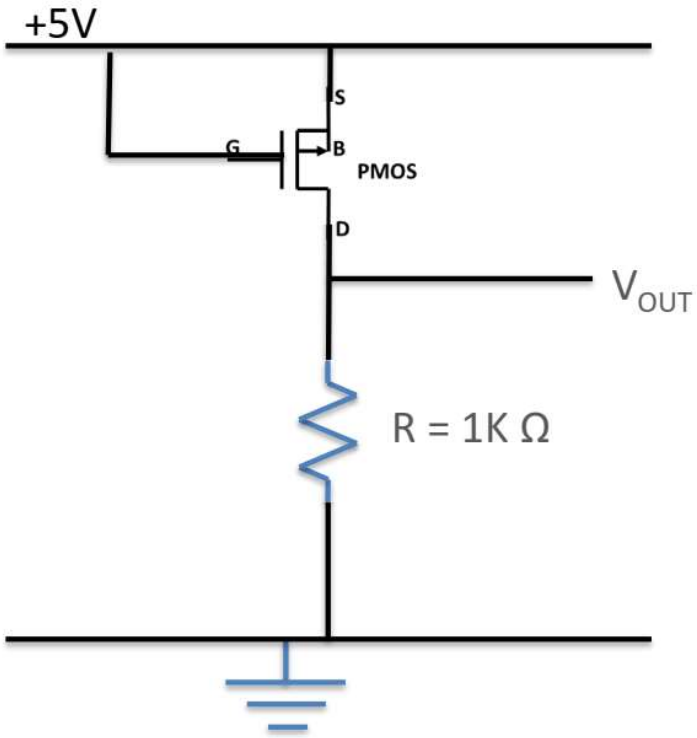


What voltage will I see on V_{OUT}?

Looking at the PMOS

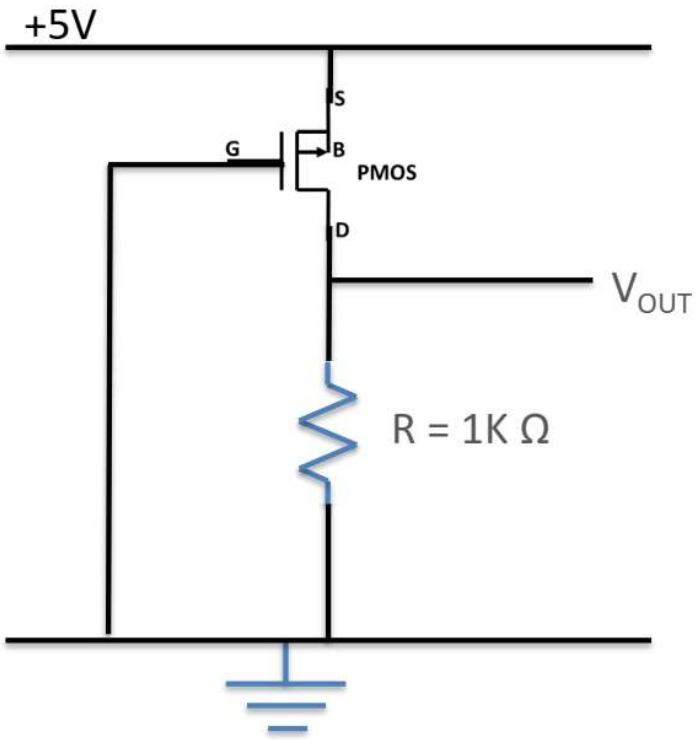
- What resistance will the transistor display for the following circuits?



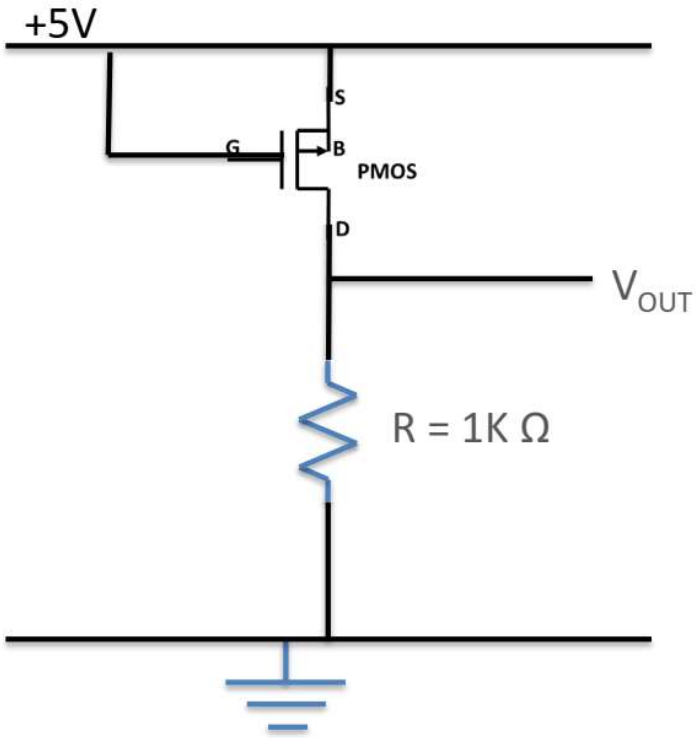


Looking at the PMOS

- What resistance will the transistor display for the following circuits?

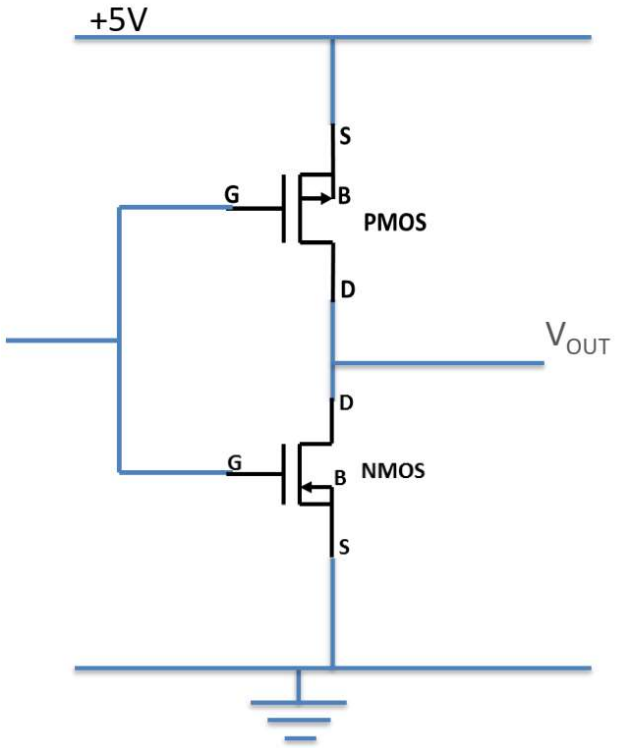


ON



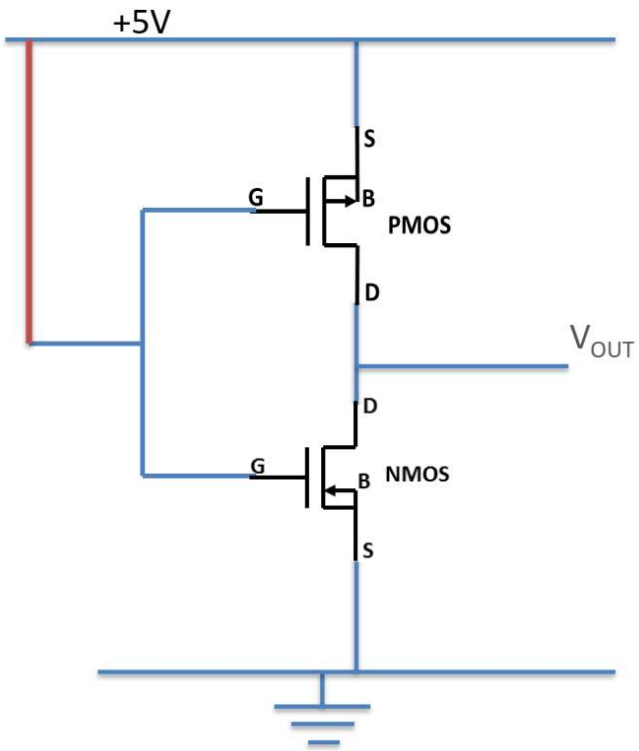
OFF

Consider the Following Circuit

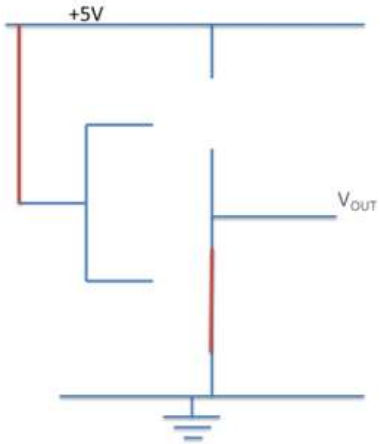


- What happens if I connect G to ground?
- What happens if I connect G to +5 V?

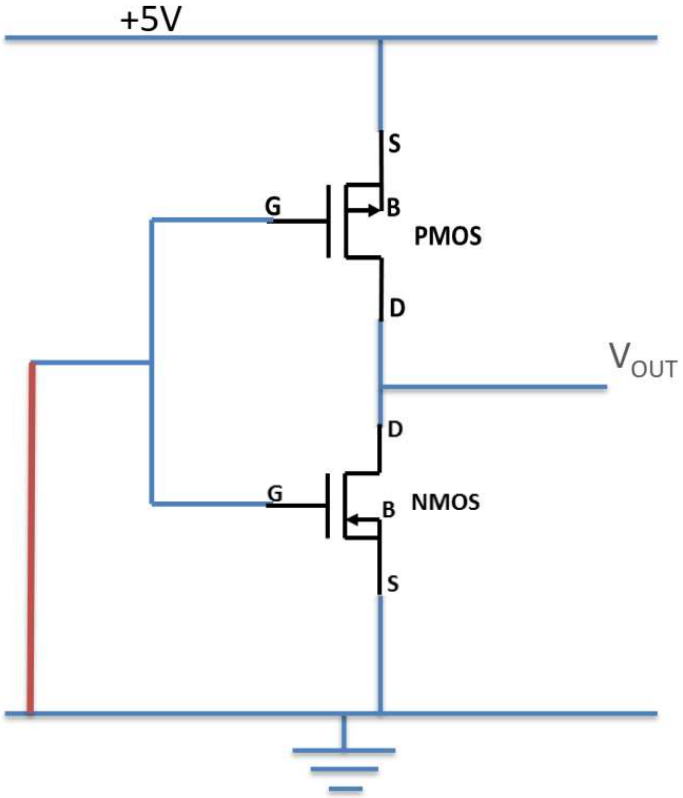
Gate is Connected High



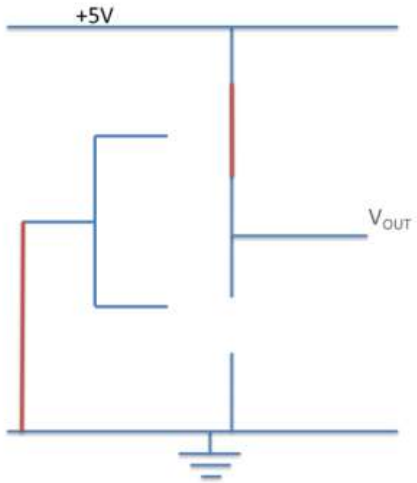
- When the gate is connected to 5 V, the NMOS has V_{GS} = 5 V, greater than V_T, turns on fully (saturated);
- The PMOS has V_{GS} = 0 V, less than $|V_T|$, turns off fully (no inversion region);
- The output V_{OUT} goes to ZERO.



Gate is Connected Low



- When the gate is connected to 0 V, the NMOS has V_{GS} = 0 V, less than V_T, turns off fully (no inversion region);
- The PMOS has V_{GS} = -5 V, $|V_{GS}|$ greater than $|V_T|$, turns on fully (saturated);
- The output V_{OUT} goes to 5 V.



A Table of the Results

	V_{OUT}
$V_G = 0$ V	5 V
$V_G = 5$ V	0 V

- If we considered a binary system to have voltages of 0 and 5 V to represent binary 0 and 1. What would this table correspond to in terms of a logic gate?

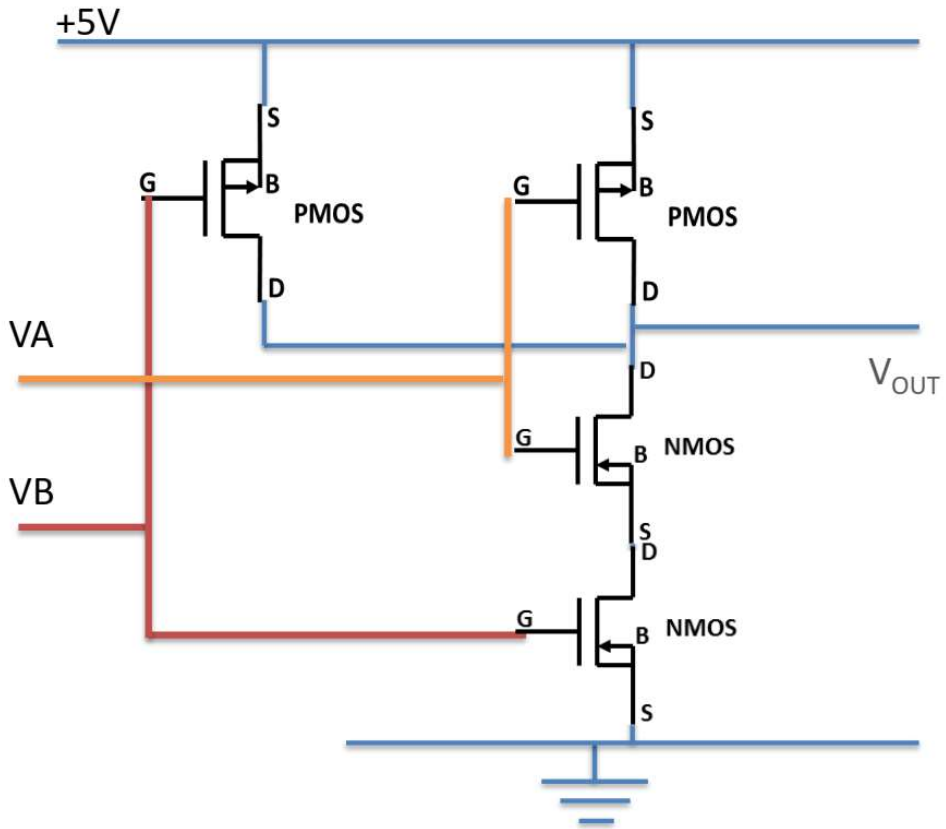
A Table of the Results

	V_{OUT}
$V_G = 0$ V	5 V
$V_G = 5$ V	0 V

- If we considered a binary system to have voltages of 0 and 5 V to represent binary 0 and 1. What would this table correspond to in terms of a logic gate?

This is an inverter (NOT gate)!

Consider the Following Circuit



- What happens to V_{OUT} as V_A and V_B take either 0 or 5 V and in different combinations?

A Table of the Results

V_A (V)	V_B (V)	V_{OUT} (V)
0	0	
0	5	
5	0	
5	5	

- If we considered a binary system to have voltages of 0 and 5 V to represent binary 0 and 1. What would this table correspond to in terms of a logic gate?

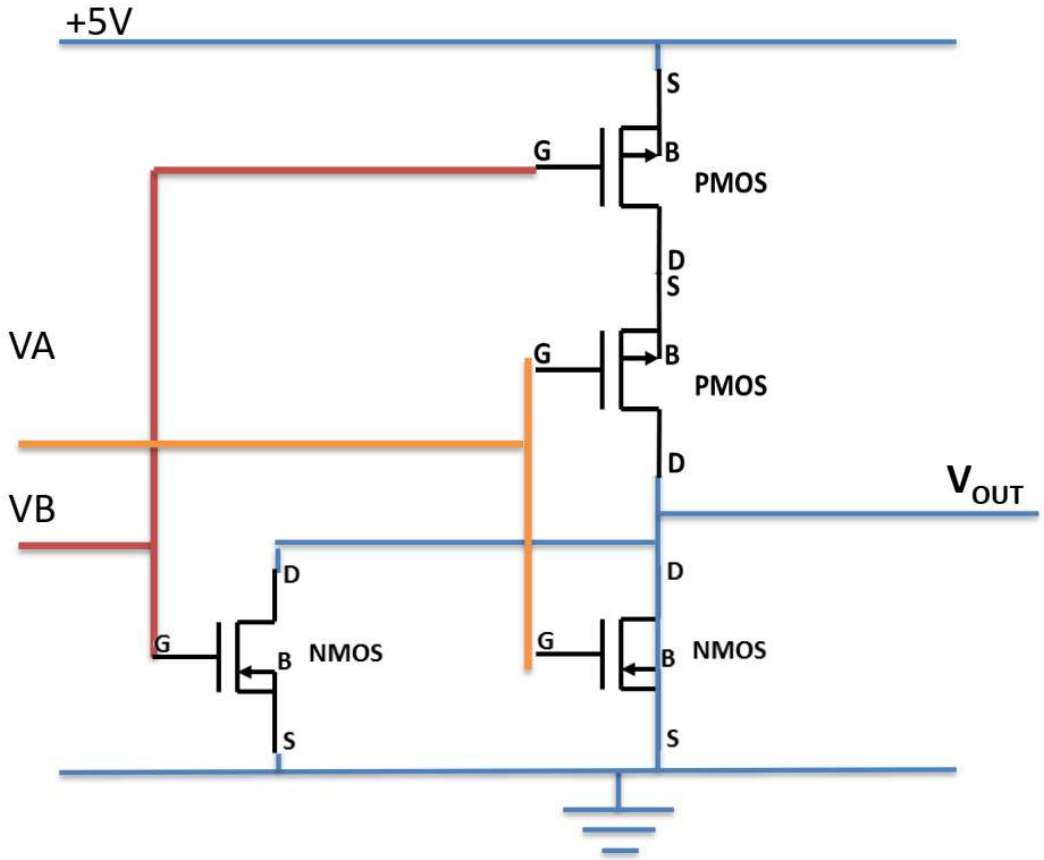
A Table of the Results

V_A (V)	V_B (V)	V_{OUT} (V)
0	0	
0	5	
5	0	
5	5	

- If we considered a binary system to have voltages of 0 and 5 V to represent binary 0 and 1. What would this table correspond to in terms of a logic gate?

This is a NAND gate.

Consider the Following Circuit



- What happens to V_{OUT} as V_A and V_B take either 0 or 5 V and in different combinations?

A Table of the Results

V_A (V)	V_B (V)	V_{OUT} (V)
0	0	
0	5	
5	0	
5	5	

- If we considered a binary system to have voltages of 0 and 5 V to represent binary 0 and 1. What would this table correspond to in terms of a logic gate?

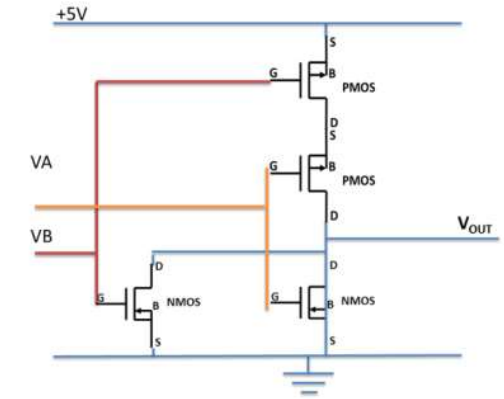
A Table of the Results

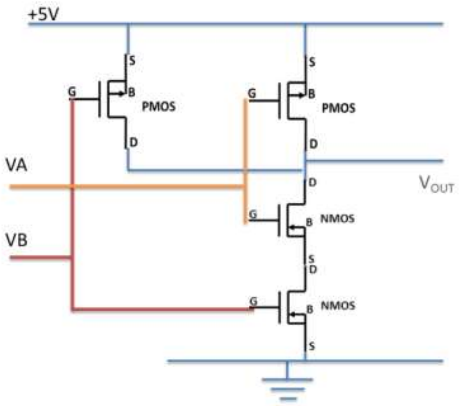
V_A (V)	V_B (V)	V_{OUT} (V)
0	0	
0	5	
5	0	
5	5	

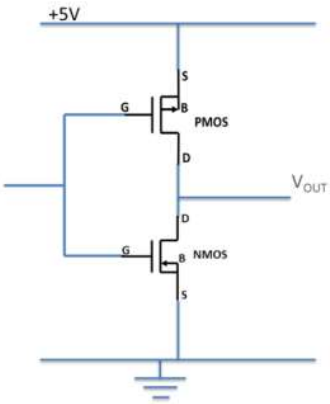
- If we considered a binary system to have voltages of 0 and 5 V to represent binary 0 and 1. What would this table correspond to in terms of a logic gate?

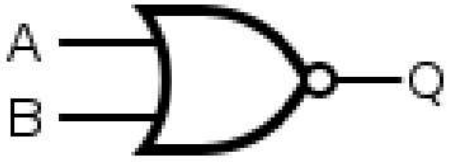
This is a NOR gate.

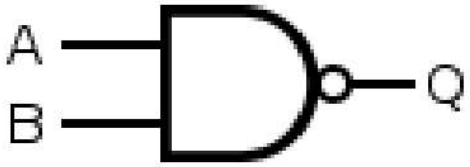
CMOS Logic

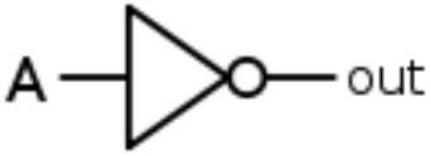












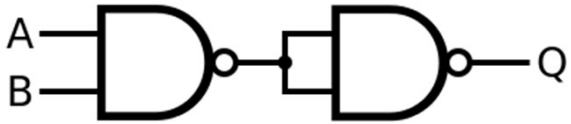
NOR NAND NOT (Inverter)

- These are the three fundamental logic gates built using CMOS transistors. Why the "C" in "CMOS", because we must use a PMOS AND an NMOS to make them work.

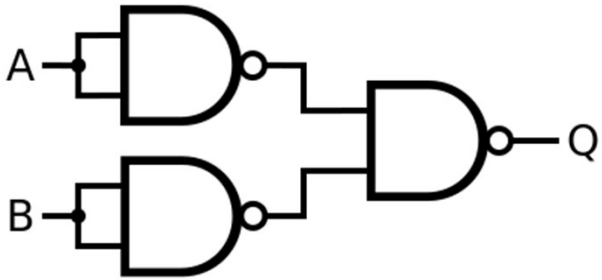
NAND & NOR Logics

- Both NAND and NOR gates have the property of functional completeness. They are both "universal gates";
- Any Boolean expression can be re-expressed by an equivalent expression utilising only NAND or NOR gate;
- Some examples using of NAND logic:

NOT



AND



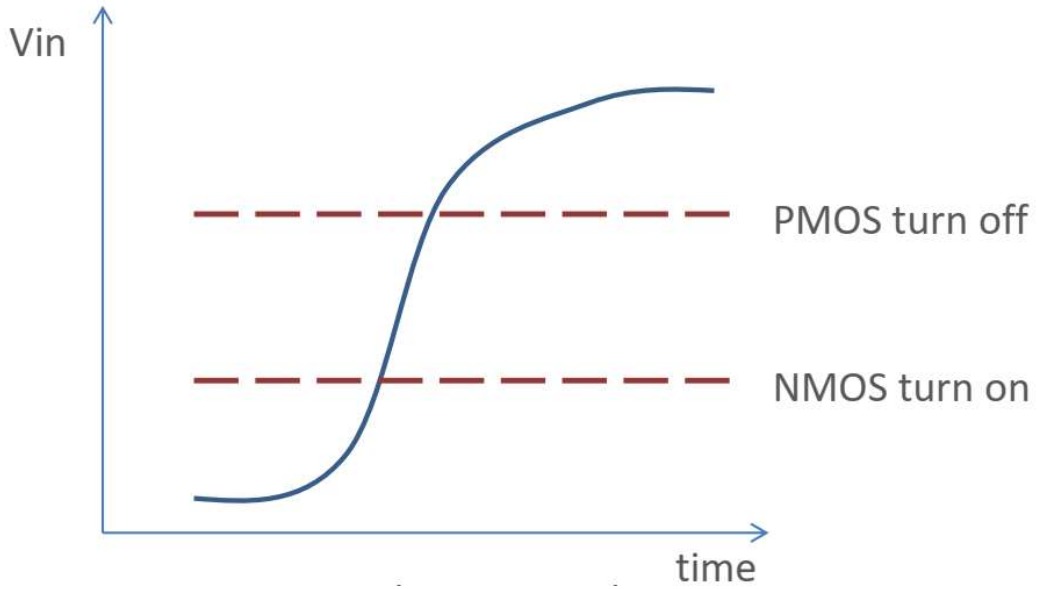
OR

Most solid-state drives (SSDs) use non-volatile NAND flash memory.

Problems & Benefits

- When looking at any logic gate implementation, we need to figure out a couple of things first:
  - How fast can it run?
  - How much power does it use?
- The answers for CMOS are quite good in both cases but not perfect and we need to touch on these.

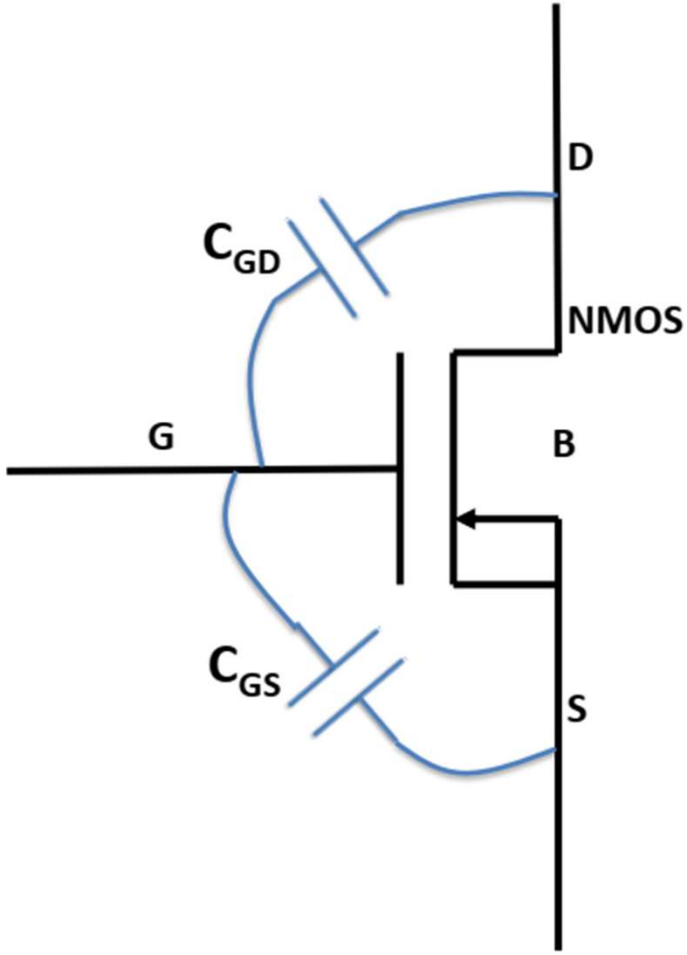
Starting and Falling Time Delays



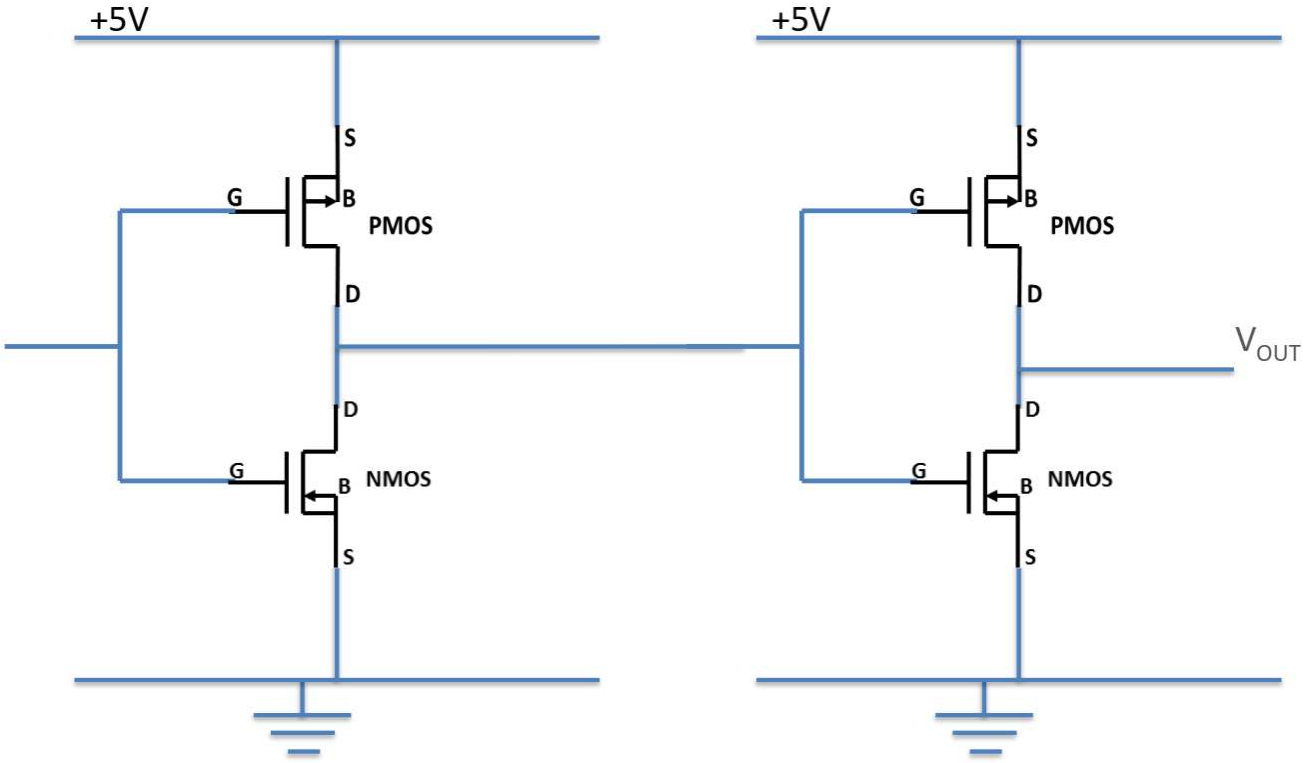
- Imagine we have a square wave (zoomed in) and we see the voltage ramping up from ZERO to 5 V. Clearly the transistors change state when the inversion region appears and disappears;
- It is going to take some time for the input signal to go from ZERO to $V_{T(NMOS)}$ and then some more time for it to get to $V_{T(PMOS)}$;
- When the NMOS turns on, the output voltage starts dropping, but it only gets properly low when the PMOS turns off.

Those Darn Parasitics

- The problem is mostly because of the parasitic capacitances. They take time to charge and discharge;
- To charge/discharge a capacitor you need to add or remove charge (through current). The bigger the capacitance, the more charge you need to add or remove;
- If you want it to change faster, you need to be able to push a lot of current in or out of the GATE during changeover. It is only for a short period of time.

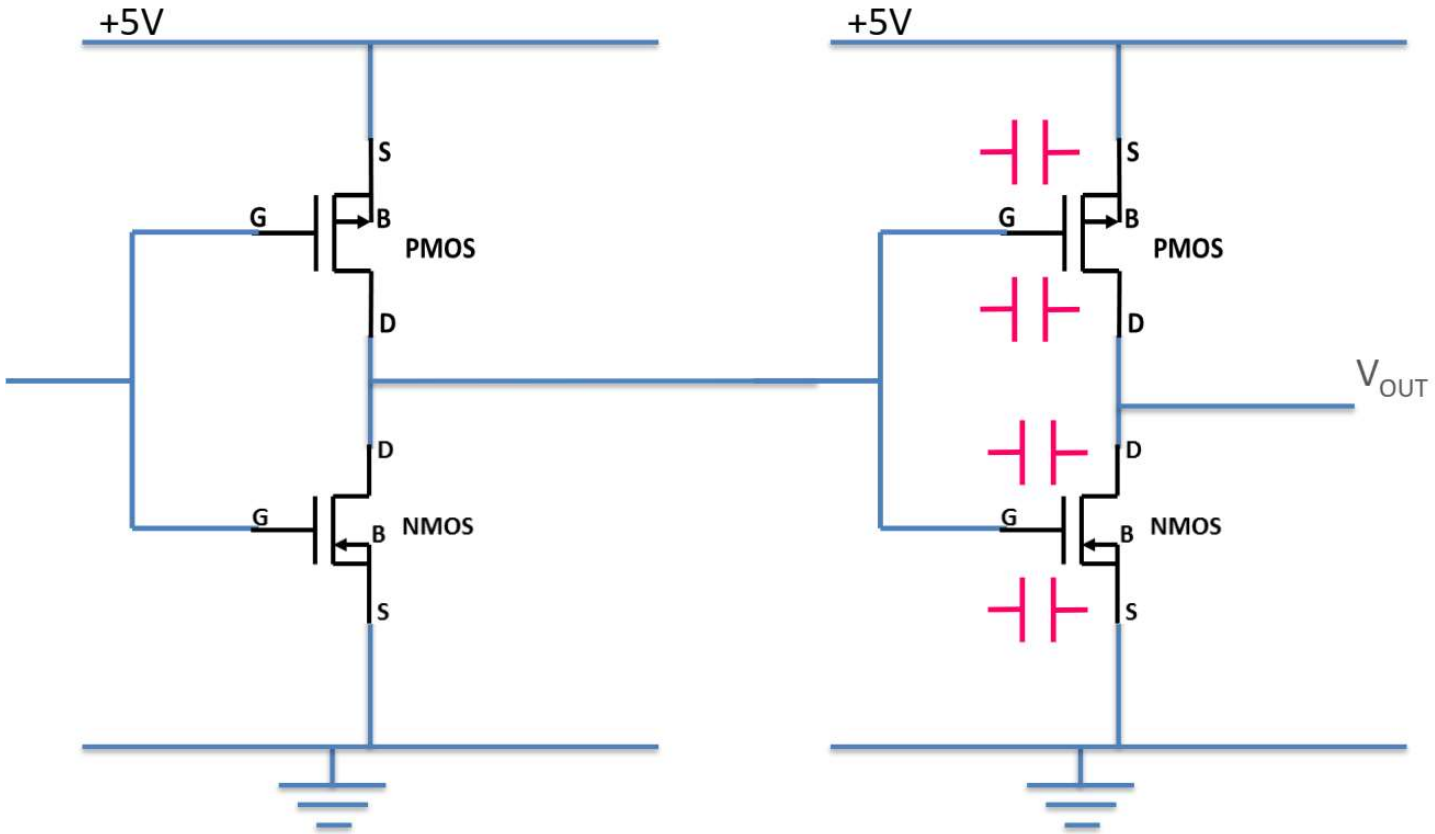


Those Darn Parasitics



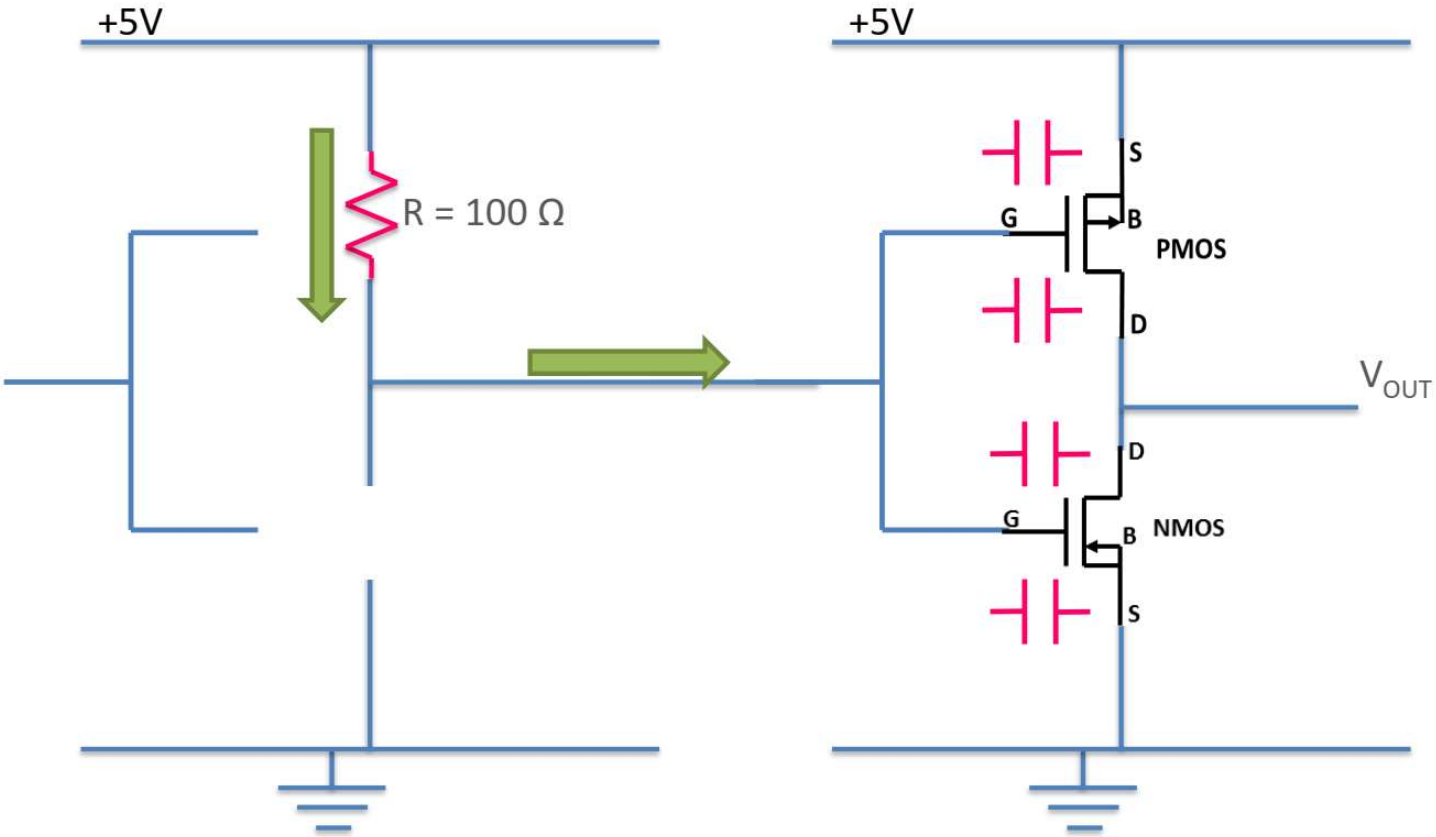
- We have two inverters connected together, but let's just look at the middle.

Those Darn Parasitics



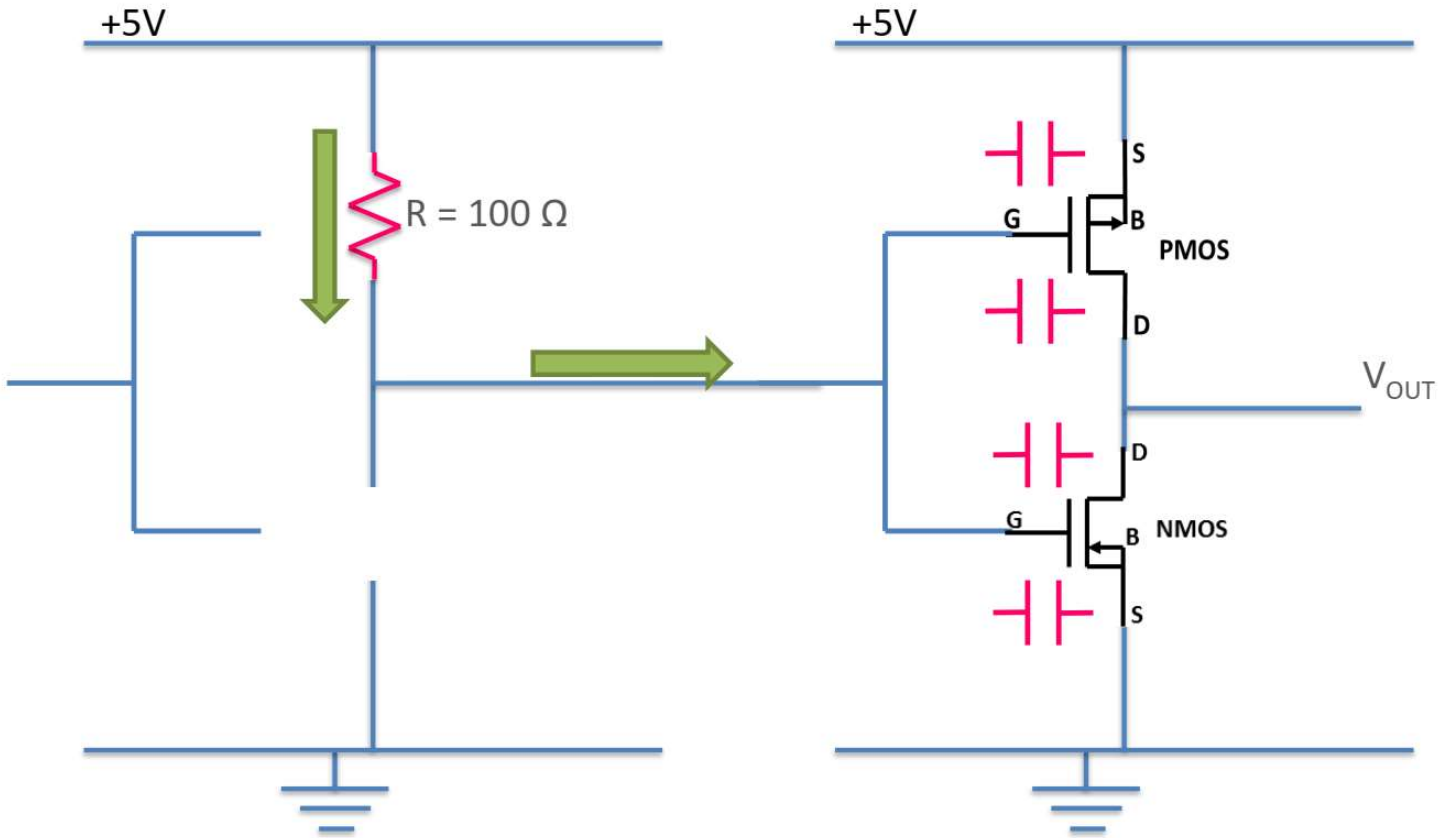
- We have an output from the middle of the other inverter, connecting to a gate which has 4 parasitic capacitors.

Those Darn Parasitics



- Now the first inverter has switched, and we have the NMOS off and the PMOS on. The current through the PMOS low resistance flows into the gate of the next inverter, charging/discharging the capacitors. The speed that we can change the voltage is proportional to *RC* time constants.

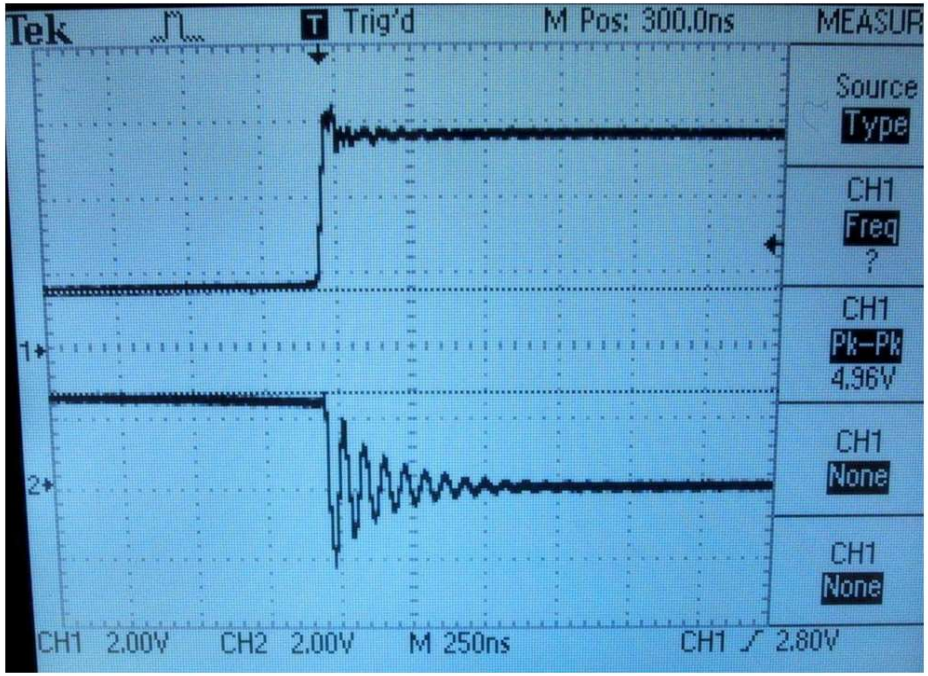
Those Darn Parasitics



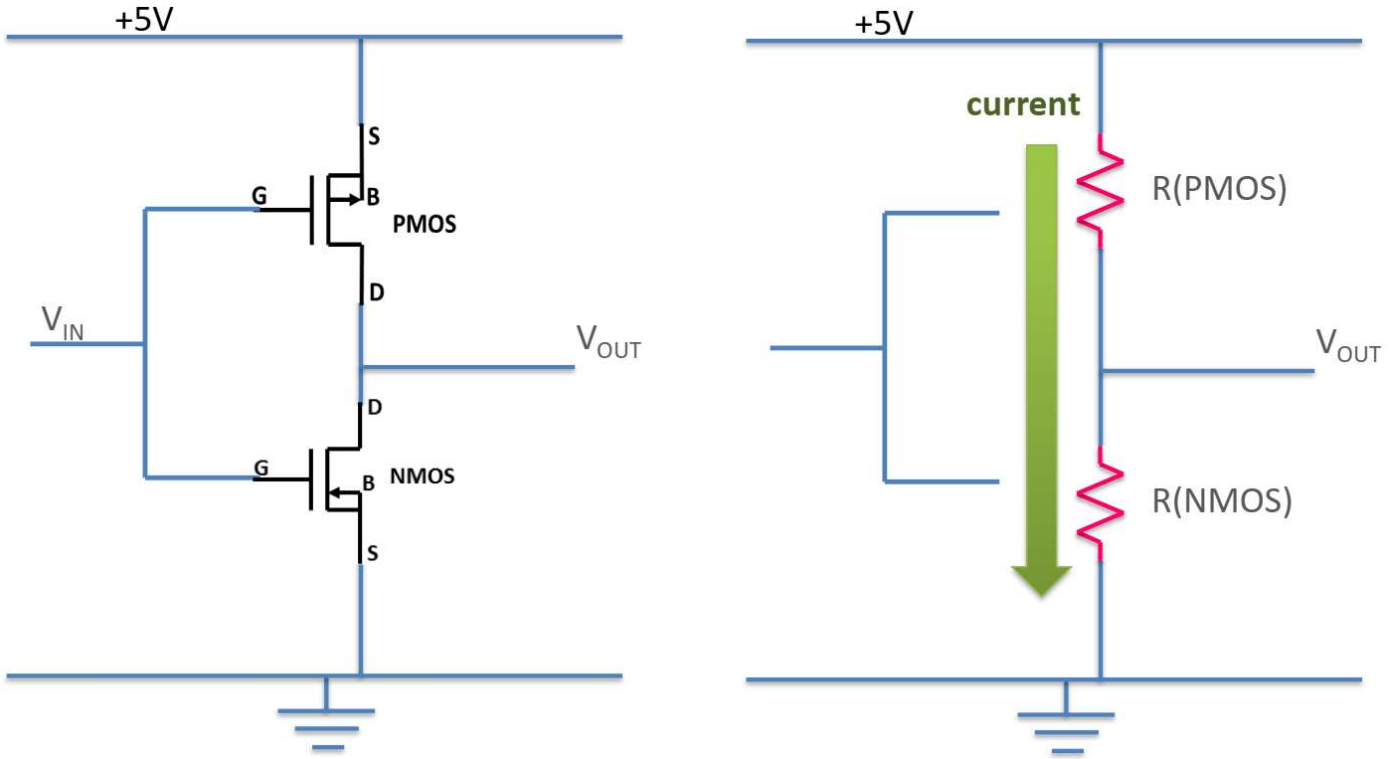
- Consider a transistor with the following values: C_{GS} = 27 pF, C_{GD} = 3 pF (which is very big), and R = 100 ohm (small R, big current);
- $\tau \approx$ 6 ns (or ~200 MHz).

Even More Darn Parasitics

- The other thing that happens is that we meet up with some parasitic inductors (from the wires). *RLC* combinations produce oscillations which we can see on the oscilloscope as **RINGING**. It fades away but can be big. So we can't look at the output until a little time after the switch.

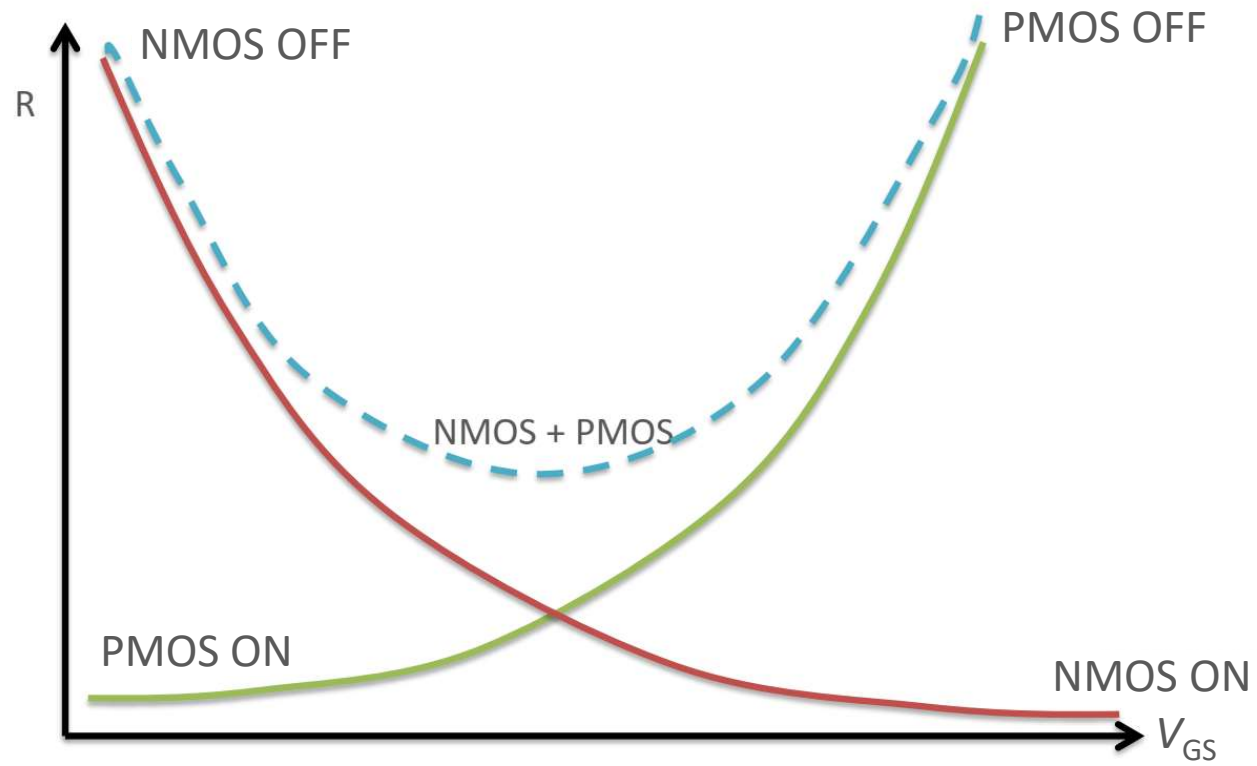


Current Flows



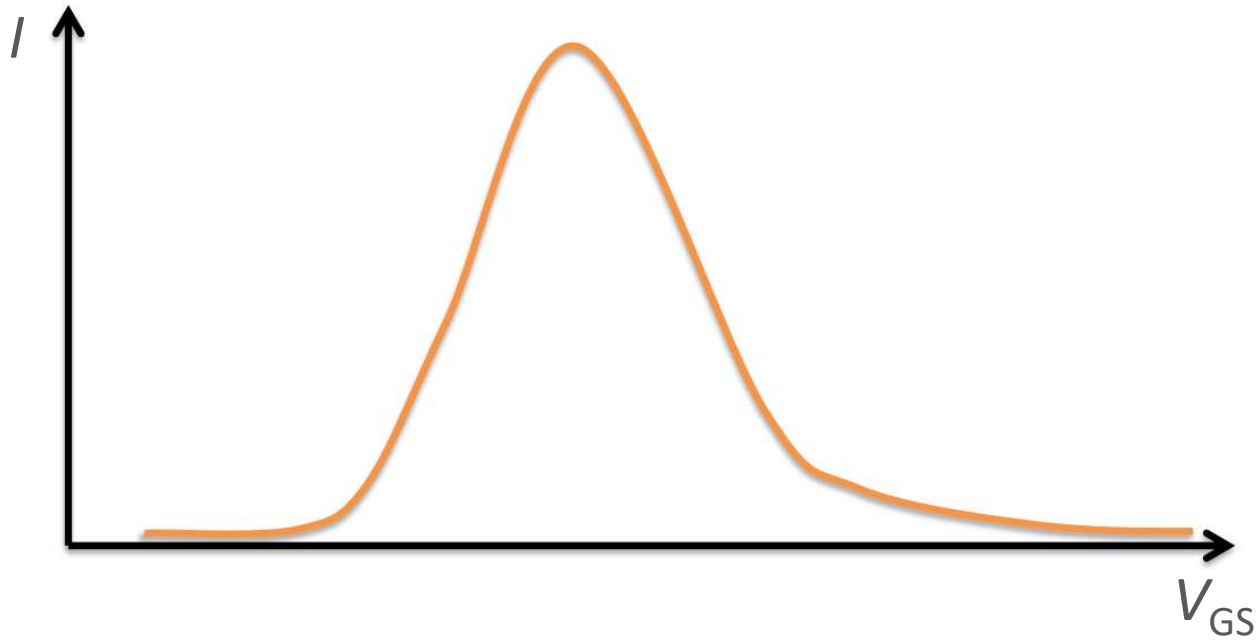
- The basic equation is still ***P = VI***.
  The voltage is fixed but the resistance will change as we turn transistors on and off. The current depends on both resistors.

The Resistance of the Transistors



- When we are at either extremes of V_{GS}, the resistance is very high, however, in the middle the resistance could be "low", say 1 – 10 kΩ.

The Current Therefore



- The current is very small at either extremes, but it is much bigger in the middle. Not big, but still noticeable.
- There is no current at either extreme values of V_{GS}, so with no current, there is no power consumed.

What is Important

- Do NOT set the gate voltage for an inverter to be in the middle, it will consume a lot of power and will eventually burn the transistors;
- Power is only consumed when we have mid-range values for V_{GS}. This means we only spend power in a CMOS logic gate when we are changing values. There is no power consumed when we are at either extremes;
- Move fast from one extreme to the other, the less time we spend in the middle, the less power we will consume.

- Our choices are not straightforward, it will depend, but we can
  - Have less capacitance on our output (reduce *RC*, speeds up switching);
  - Decrease *R* so we can switch faster (bigger spikes of current, more power);
  - Increase *R* so we have lower current spikes when we are changing (slower).