Tutorial Sheet 7 - *Multi-output Minimisation*

1. A seven segment display can represent the letters of the alphabet from A to H as shown in figure 1 below. Each letter is defined by a three digit binary code ABC from 000 to 111.

(a) Draw out a truth table for the logic needed to drive the display segments.
(b) Using Karnaugh Maps find the simplest Boolean expressions for each segment driver.
(c) Show how the drivers can be realised using ***only 2-input NAND gates***.

The seven segment display is connected in common cathode mode.

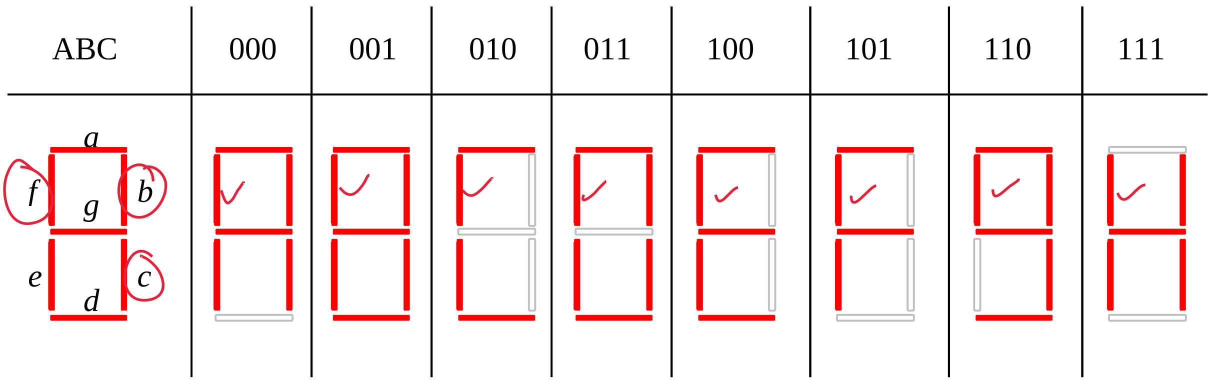
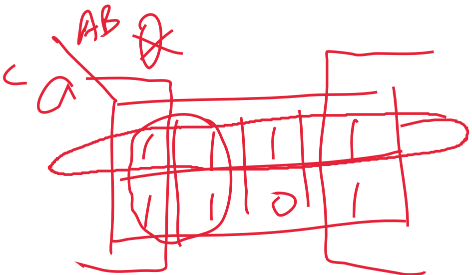
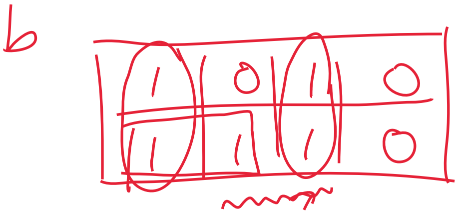


Figure 1

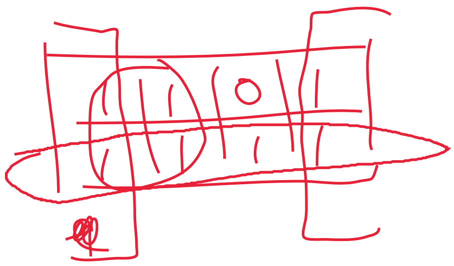


$a = \bar{A} + \bar{B} + \bar{C}$

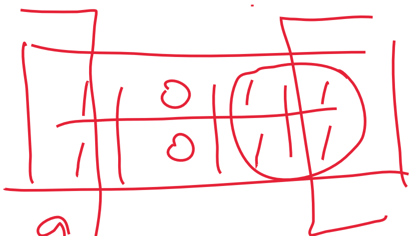


$b = C = AB + \bar{A}C + \bar{A}\bar{B}$

$d = A\bar{C} + \bar{A}C + \bar{A}\bar{B}$



$e = \bar{A} + \bar{B} + C$



$g = A + \bar{B}$

$f = 1$

De Morgan

14 - 2 input NAND.

2. A seven segment display similar to that described in question 1 is to be used to display the letters A to E. Combinations 101, 110 and 111 cannot occur and are to be treated as don't care conditions. Determine the minimal realisation of the display driver logic ***using only 2-input NAND gates***. What would the display show if the don't care terms were applied as inputs?

1	1	X	1
1	1	X	X

1	0	X	0
1	1	X	X

$b = c = C + \overline{A}\overline{B}$

0	1	X	1
1	1	X	X

$d = A + B + C$

$a = e = f = 1$

1	0	X	1
1	0	X	X

$g = \overline{B}$

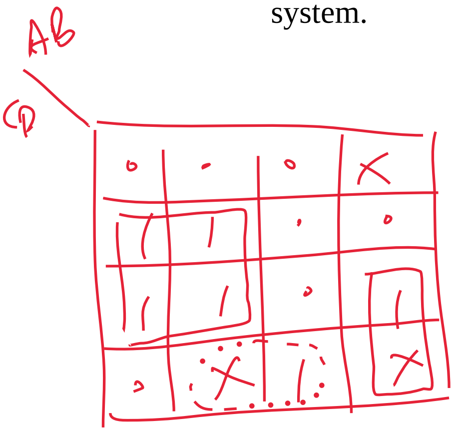
De Morgan

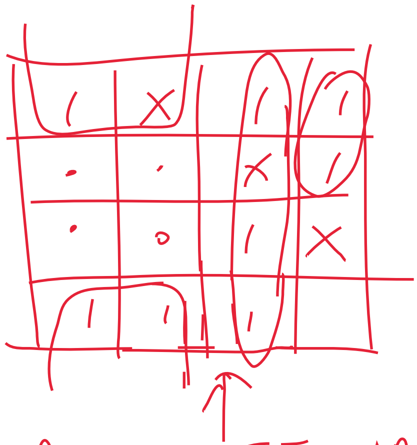
4, 2-input NAND

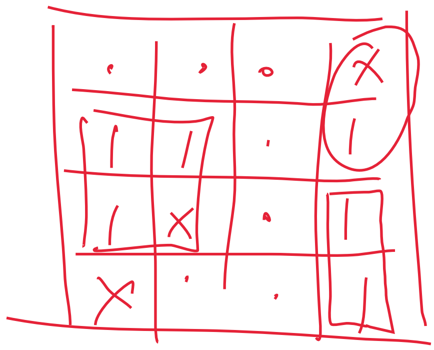
3. A logic system is characterised by the following functions:

$$f_{1(A,B,C,D)} = \sum(1, 3, 5, 7, 11, 14) + d(6, 8, 10)$$
$$f_{2(A,B,C,D)} = \sum(0, 2, 6, 8, 9, 12, 14, 15) + d(4, 11, 13)$$
$$f_{3(A,B,C,D)} = \sum(1, 3, 5, 9, 10, 11) + d(2, 7, 8)$$

Using multi-output minimisaton, obtain a minimal SOP implementation for this system.







$f_1 = \bar{A}D + A\bar{B}C + BC\bar{D}$

$f_2 = A\bar{B}\bar{C} + \bar{A}\bar{D} + AB$

$f_3 = A\bar{B}C + \bar{A}D + A\bar{B}\bar{C}$

6 product terms