Tutorial Sheet 4 - *NAND and NOR Implementation*

1. Implement the following function using no more than three NAND gates. Assume that inputs and their complements are available:

$$f = (A + D)(\overline{A} + B)(\overline{A} + \overline{C})$$

2. Implement the following function using the don't care conditions where appropriate. Use no more than four NAND gates. Assume that inputs and their complements are available:

$$f = \overline{B}D + \overline{B}C + ABCD$$
$$d = \overline{A}BD + A\overline{B}\overline{C}\overline{D}$$

3. Implement the following function using no more than two NOR gates, using the don't care conditions where appropriate. Assume that both the normal and complemented inputs are available:

$$f = \overline{A}\overline{B}\overline{C} + A\overline{B}D + \overline{A}\overline{B}C\overline{D}$$
$$d = ABC + A\overline{B}\overline{D}$$

4. Determine the inputs required for the gates in figure 1(b) below, such that figure 1(b) implements the same function as figure 1(a).

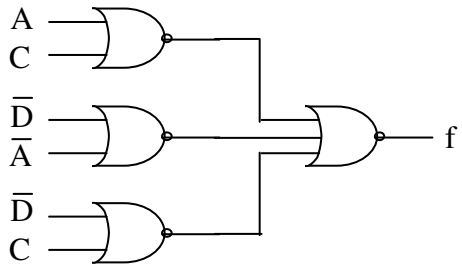

Figure 1(a)

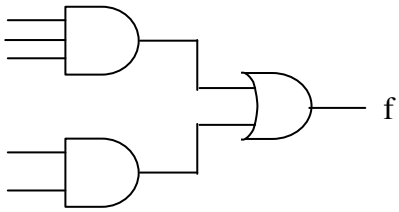

Figure 1(b)

5. Implement a minimal solution using only NOR gates for the following function. Complements of the inputs are *not* available.

$$f_{(A,B,C,D)} = \sum(0, 1, 5, 8, 9, 10, 11, 13, 14, 15)$$

6. **(i)** A logic circuit contains four inputs A, B, C and D and one output f. Combinations of the inputs that are divisible by 4 cannot occur and therefore can be treated as don't care conditions (note that 0 is divisible by 4). Furthermore, the output of the circuit is only high when any of the possible combination of inputs is divisible by either 2 or 3 or both. Derive a minimal sum-of products expression for this circuit.

(ii) Determine a minimal NAND and a minimal NOR implementation for the circuit in part (i). Each implementation is to be minimal only in respect of the number of gates required (i.e. the number of inputs for each gate does not need to be taken into consideration). Note that complemented input variables are available.

(iii) Had complemented input variables not been available, would this have affected your solution to part (ii) above? Justify your answer.

ANSWERS

1 $\overline{(\bar{A}\bar{D})(A\bar{B}\bar{C})}$

2 $\overline{(\bar{B}\bar{D})}\,\overline{(\bar{B}\bar{C})}\,\overline{(\bar{C}\bar{D})}$

3 $\overline{B + \overline{(A + \bar{C} + \bar{D})}}$

4 $\bar{A}\bar{A}\bar{C} + A\bar{D}$ or $\bar{A}\bar{C}\bar{C} + A\bar{D}$ or $\bar{A}\bar{C} + A\bar{A}\bar{D}$ or $\bar{A}\bar{C} + A\bar{D}\bar{D}$

5 $\overline{(\bar{B} + C + D)} + \overline{(A + \bar{C})}$

6 (i) $\bar{D} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C$

(ii) $\overline{D \cdot A\bar{B}\bar{C} \cdot \overline{ABC} \cdot \bar{A}\bar{B}\bar{C}},$

$\overline{\bar{D} + \overline{(\bar{A}+B+C)} + \overline{(\bar{A}+\bar{B}+\bar{C})} + \overline{(A+B+\bar{C})}}$ or $\overline{\overline{(A+C)} + \overline{(\bar{B}+C)} + \overline{(A+\bar{B}+\bar{D})} + \overline{(\bar{A}+B+\bar{C}+\bar{D})}}$

(iii) Same solutions as (ii), but more gates required to implement them!