Analogue Electronics 1 (EE204FZ)

Tutorial 3 (Solutions)

Q1.

1. (B)
2. (C)
3. (A)
4. (B)
5. (A)

Q2.

1.

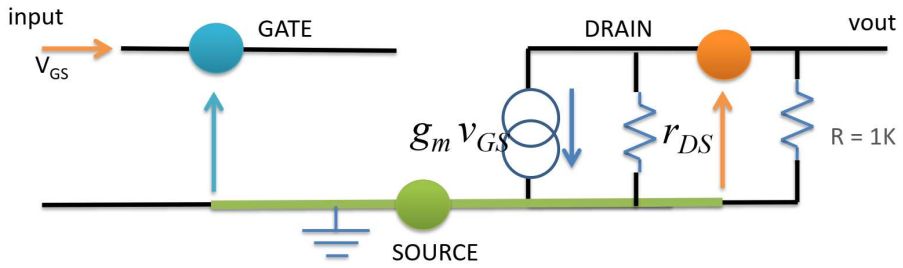
A small signal is defined as a signal which remains in an area and is so small that it can be approximated by a straight line (linearization) without introducing large errors.

2.

Clipping is a small-signal failure. It occurs when the signal you are amplifying hits either the maximum or minimum voltage and thus it becomes flatlines as it cannot go past either of these limits.

To avoid it, set the bias point such that the signal is away from the edges. However, if the signal is too large, clipping becomes inevitable.

3.



Q3.

We apply the MOSFET equation in the saturation region (with the channel length modulation parameter accounted for):

$$I_{\mathrm{D}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2(1 + \lambda V_{\mathrm{DS}})$$

Hence, $I_{\mathrm{D1}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2(1 + \lambda V_{\mathrm{DS}}\ )$ and $I_{\mathrm{D2}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2(1 + \lambda V_{\mathrm{DS2}})$

$$\frac{I_{\mathrm{D1}}}{I_{\mathrm{D2}}} = \frac{1 + \lambda V_{\mathrm{DS1}}}{1 + \lambda V_{\mathrm{DS2}}}$$

Insert the values provided in the question:

$$\frac{3}{3.4} = \frac{1 + 5\lambda}{1 + 10\lambda}$$

Solving the above equation gives $\lambda = 0.4/13 = 0.0308\ \mathrm{V}^{-1}$ (pay attention to the fact that the channel length modulation parameter has units).

In order to calculate the small-signal output resistance, we first calculate $I_{\mathrm{D(Sat)}}$:

$$I_{\mathrm{D(Sat)}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2 = \frac{I_{\mathrm{D2}}}{1 + \lambda V_{\mathrm{DS2}}} = \frac{3.4\ \mathrm{mA}}{1 + 0.0308 \times 10} = 2.6\ \mathrm{mA}$$

$$r_{\mathrm{O}} = \frac{1}{\lambda I_{\mathrm{D(Sat)}}} = \frac{1}{0.0308 \times 2.6 \times 10^{-3}} = 12.5\ \mathrm{k\Omega}$$

Q4.

The calculation given here tries to provide an exact solution to the problem. However, in the first-order approximation, one can ignore the channel length modulation parameter while calculating I_{DQ} and V_{DSQ}. This will simplify at least part (a) of the question quite a bit.

(a) We start by assuming that the MOSFET is in the saturation region and we will prove with the V_{DSQ} we obtain that it is indeed the case:

$$I_{\mathrm{DQ}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2 (1 + \lambda V_{\mathrm{DSQ}})$$

The MOSFET is under voltage-divider bias, we can calculate its V_{GS}:

$$V_{\mathrm{GS}} = V_{\mathrm{G}} = \frac{R_2}{R_1 + R_2} V_{\mathrm{DD}} = \frac{60}{240 + 60}(3.3\ \mathrm{V}) = 0.66\ \mathrm{V}$$

All the terms in the first equation are known except for I_{DQ} and V_{DSQ}. Applying Kirchhoff's voltage law to the drain-source side of the MOSFET:

$$V_{\mathrm{DD}} - I_{\mathrm{DQ}} R_{\mathrm{D}} - V_{\mathrm{DSQ}} = 0$$

We have two equations with two unknowns (I_{DQ} and V_{DSQ}). Solving the set of two simultaneous equations, we have:

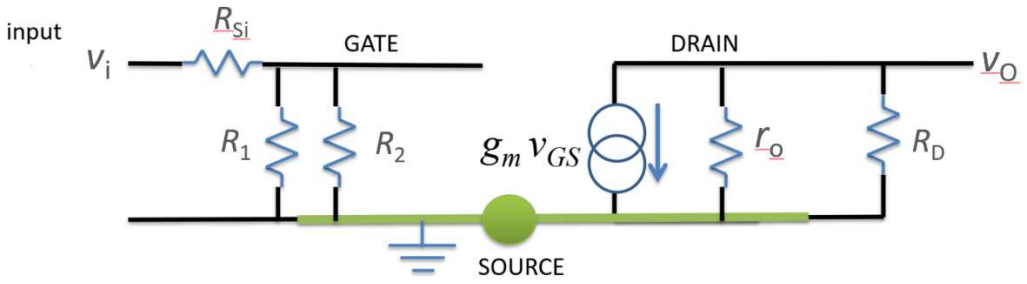
$I_{\mathrm{DQ}} = 2.76 \times 10^{-4}$ A = 0.276 mA and $V_{\mathrm{DSQ}} = 1.09\ \mathrm{V} > V_{\mathrm{GS}} - V_{\mathrm{T}} = 0.26\ \mathrm{V}$

The MOSFET is indeed in the saturation region.

(b) $g_m = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}}) = 2.08 \times 10^{-3}\ \mathrm{A/V}$

$$r_{\mathrm{O}} = \frac{1}{\lambda I_{\mathrm{D(Sat)}}} = \frac{1}{\frac{\lambda}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2} = 1.85 \times 10^5\ \Omega = 185\ \mathrm{k\Omega}$$

(c) Assuming that the frequency is sufficiently high, the input (de)-coupling capacitor C_{C1} can be ignored. The small-signal equivalent circuit is (students are encouraged to discuss why this is the case):



$R_1||R_2 = 48\ \text{k}\Omega$

$$v_{\text{GS}} = \frac{R_1||R_2}{R_{\text{Si}} + R_1||R_2} v_{\text{i}} = \frac{48}{2+48} v_{\text{i}} = 0.96 v_{\text{i}}$$

$r_{\text{O}}||R_{\text{D}} = (185\ \text{k}\Omega)||(8\ \text{k}\Omega) = 7.67\ \text{k}\Omega$

$$A = \frac{v_{\text{O}}}{v_{\text{i}}} = 0.96 \frac{v_{\text{O}}}{v_{\text{GS}}} = 0.96[-g_m(r_{\text{O}}||R_{\text{D}})] = -(0.96)(2.08 \times 10^{-3})(7.67 \times 10^{3}) = -15.3$$

If one ignores all the complications and apply the gain equation directly,

$$A = -g_m R_{\text{D}} = -(2.08 \times 10^{-3})(8 \times 10^{3}) = -16.6$$

The difference is only ~8% which means that the later often is a good enough approximation for many applications.

Q5.

The NMOS is under voltage-divider bias. Let's calculate its gate electric potential first:

$$V_{\text{G}} = \frac{R_2}{R_1 + R_2} V_{\text{DD}} = \frac{175}{225 + 175} (5\ \text{V}) = 2.19\ \text{V}$$

The electric potential difference between the gate and the source is:

$$V_{\text{GS}} = V_{\text{G}} - V_{\text{S}} = V_{\text{G}} - I_{\text{DQ}} R_{\text{S}} = 2.19 - I_{\text{DQ}} R_{\text{S}}$$

Let's assume that the NMOS is in the saturation region (we have to double check it after we obtain the value of V_{DSQ}). Since we also know that $\lambda = 0$, we have

$$I_{\text{DQ}} = \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{T}})^2$$

Insert this equation into the expression for V_{GS}:

$$V_{\text{GS}} = 2.19 - \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{T}})^2 R_{\text{S}} = 2.19 - 0.5(V_{\text{GS}} - 0.8)^2$$

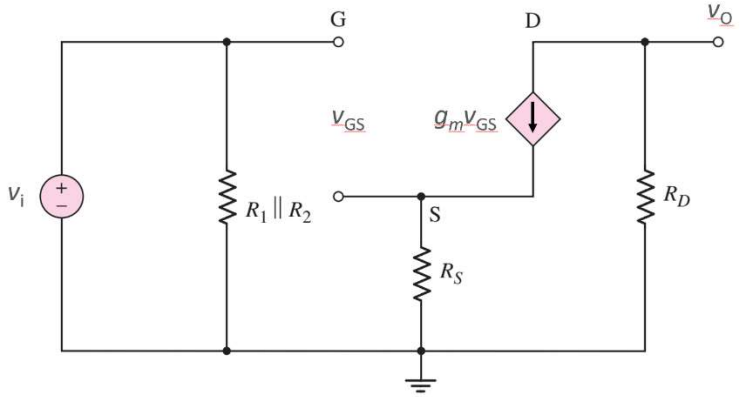
since $\frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} R_{\text{S}} = 0.5\ \text{V}^{-1}$. This is a parabolic equation with respect to V_{GS}. Solving the equation we have V_{GS} = 1.74 V.

$$I_{\text{DQ}} = \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{T}})^2 = 0.5(1.74 - 0.8)^2 = 0.442\ \text{mA}$$

$$V_{\mathrm{DSQ}} = V_{\mathrm{DD}} - I_{\mathrm{DQ}}(R_{\mathrm{D}} + R_{\mathrm{S}}) = 5 - (0.442 \times 10^{-3})[(1+4) \times 10^{3}] = 2.79\ \mathrm{V}$$

We should double check that V_{DSQ} = 2.79 V > $V_{\mathrm{GS}} - V_{\mathrm{T}}$ = 1.74 – 0.8 = 0.94 V. Hence, the NMOS is indeed in the saturation region.

(b) Assume that the frequency of the input signal is sufficiently high, so the input (de)-coupling capacitor C_{C1} can be ignored. We also ignore the small-signal output resistance r_{O} of the NMOS since it is usually a very large value. When R_{L} is infinitely large, the small-signal equivalent circuit is provided below (students are encouraged to discuss why the various resistors are positioned in such a way in the equivalent circuit):



We can calculate g_m using the large-signal parameters:

$$g_m = \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}}) = 0.94\ \mathrm{mA/V}$$

Apply Kirchhoff's voltage law:

$$v_{\mathrm{O}} = 0 - g_m v_{\mathrm{GS}} R_{\mathrm{D}}$$

$$v_{\mathrm{GS}} = v_{\mathrm{i}} - g_m v_{\mathrm{GS}} R_{\mathrm{S}} \text{ or } v_{\mathrm{i}} = v_{\mathrm{GS}} + g_m v_{\mathrm{GS}} R_{\mathrm{S}}$$

The gain of the circuit is

$$A = \frac{v_{\mathrm{O}}}{v_{\mathrm{i}}} = \frac{-g_m v_{\mathrm{GS}} R_{\mathrm{D}}}{v_{\mathrm{GS}} + g_m v_{\mathrm{GS}} R_{\mathrm{S}}} = \frac{-g_m R_{\mathrm{D}}}{1 + g_m R_{\mathrm{S}}} = \frac{-(0.94)(4)}{1 + (0.94)(1)} = -1.94$$

(c) If R_{L} is not infinitely large, it is connected in parallel with R_{D}. We only need ($R_{\mathrm{D}}||R_{\mathrm{L}}$) to be 75% of R_{D} for the gain to drop to its 75% point. Since R_{D} = 4 kΩ, ($R_{\mathrm{D}}||R_{\mathrm{L}}$) = 3 kΩ. Solving for R_{L}, we have R_{L} = 12 kΩ. Incidentally, as long as one understands that R_{L} and R_{D} are connected in parallel in the small-signal equivalent circuit, one will be able to answer this part of the question correctly, even if one cannot answer parts (a) and (b).