EE204FZ
Lecture 3
Junction Field Effect Transistors (JFETs)

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What is a Transistor?

- There are two basic types of transistors and lots of different ways to build them.
  - A current controlled variable “resistor” -> BJT
  - A voltage controlled variable “resistor” -> FET
- Using “resistor” here is a bit dodgy but basically by applying a given voltage across the device, one can change something in the device that varies the current.

What is a Transistor?

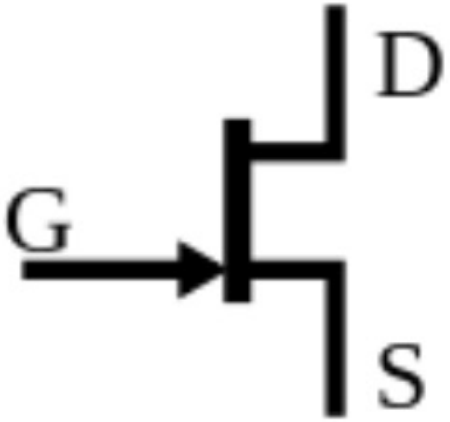
- FETs come in several forms, the most common are
  - Bipolar Junction Transistors (BJTs)
  - Field Effect Transistors (JFETs and MOSFETs)
- Now we also have
  - FinFETs
  - Multi-Gate FETs (MuGFETs)
  - Metal-Semiconductor FETs (MESFETs)
  - And lots of different other types.

Which Type of Transistors is the Best?

BJTs	FETs
First type of transistors, used widely in old designs.	Used widely in modern designs.
Best for low-noise performance.	A bit noisy.
Run the fastest (> 50 GHz) & materials dependent.	Usually slower, but modern FETs can operate at ~ 10 GHz.
Not easy to integrate.	Scales very well with modern fab technology, a very large number of FETs can be packed on the same chip.
Not power efficient.	FETs circuits can be extremely power efficient.
Current controlled.	Voltage controlled.

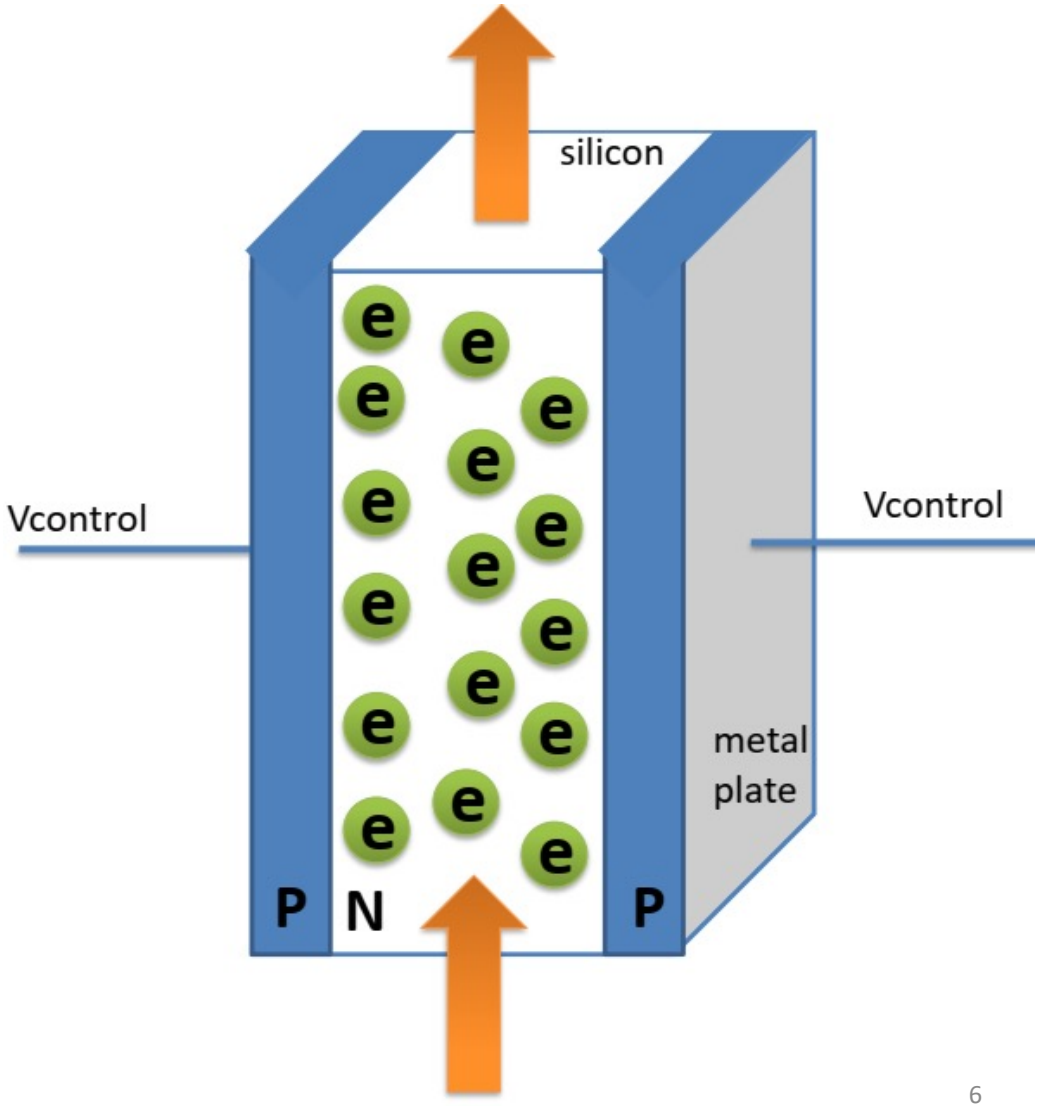
- We use mostly FETs in this course (including the lab sessions).
- When you are doing analogue electronics designs, select the transistor that best suits your applications.

What is a Field-Effect Transistor?



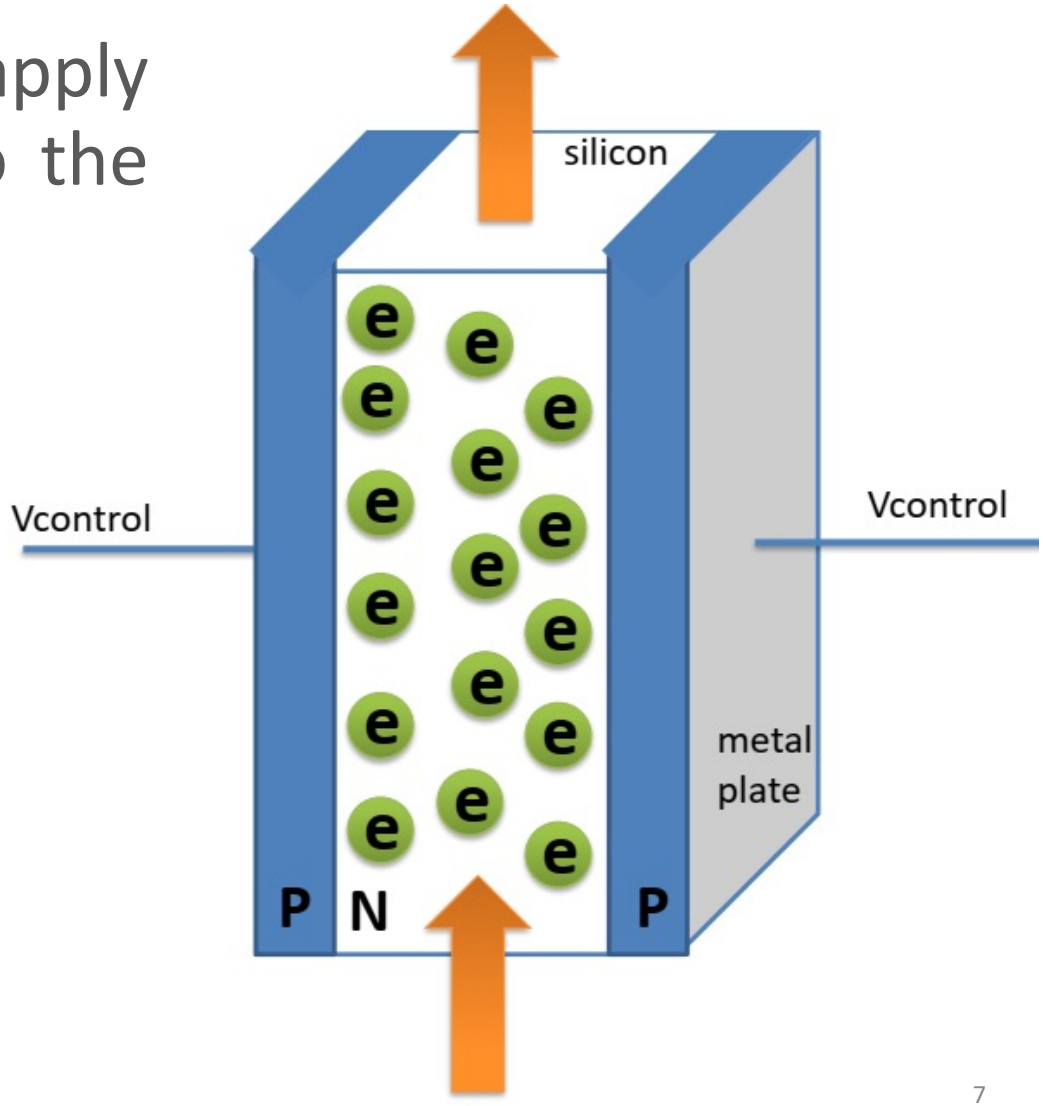
- More seriously, FET is a transistor whose behaviour can be controlled by electric fields. Electric fields are generated by electric potential differences (voltages), so FETs are voltage-controlled devices.

Junction Field Effect Transistors (JFETs)



Junction Field Effect Transistors (JFETs)

- What happens if we apply a negative voltage to the blue plates?

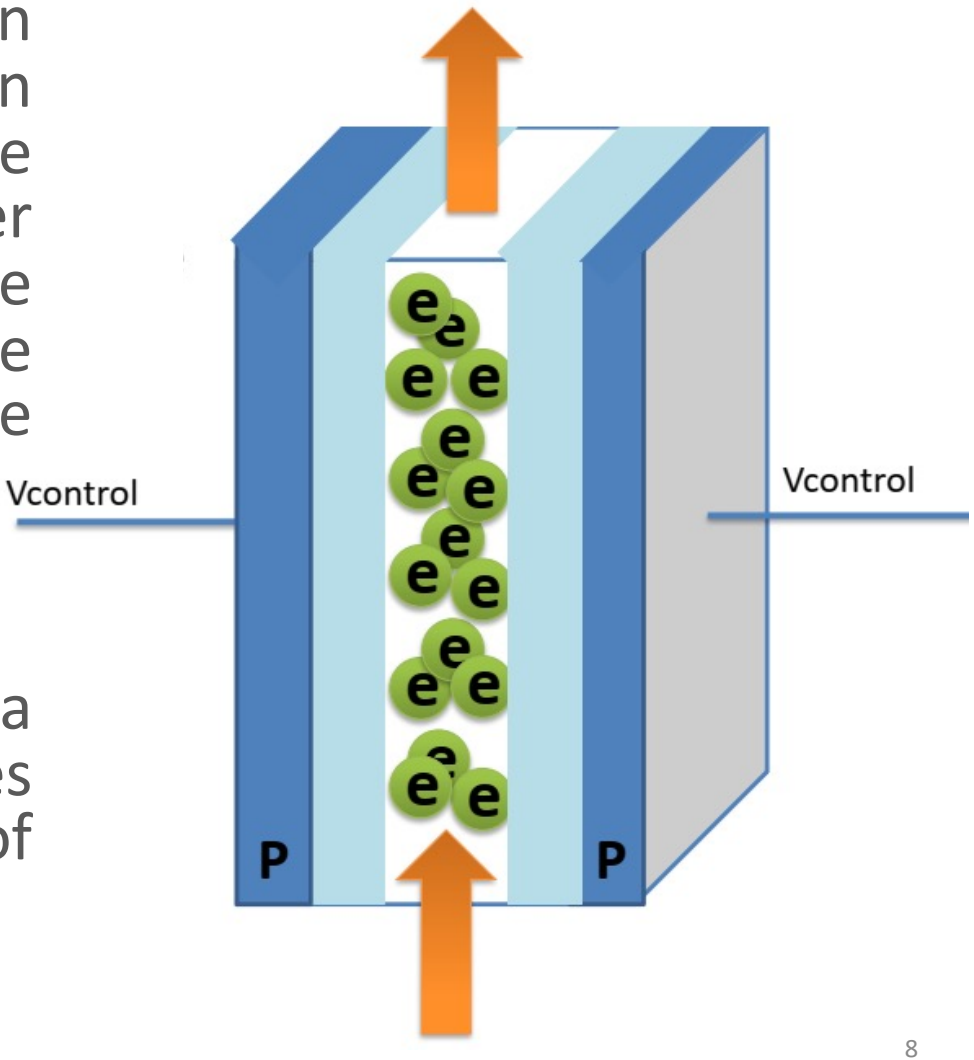


Junction Field Effect Transistors (JFETs)

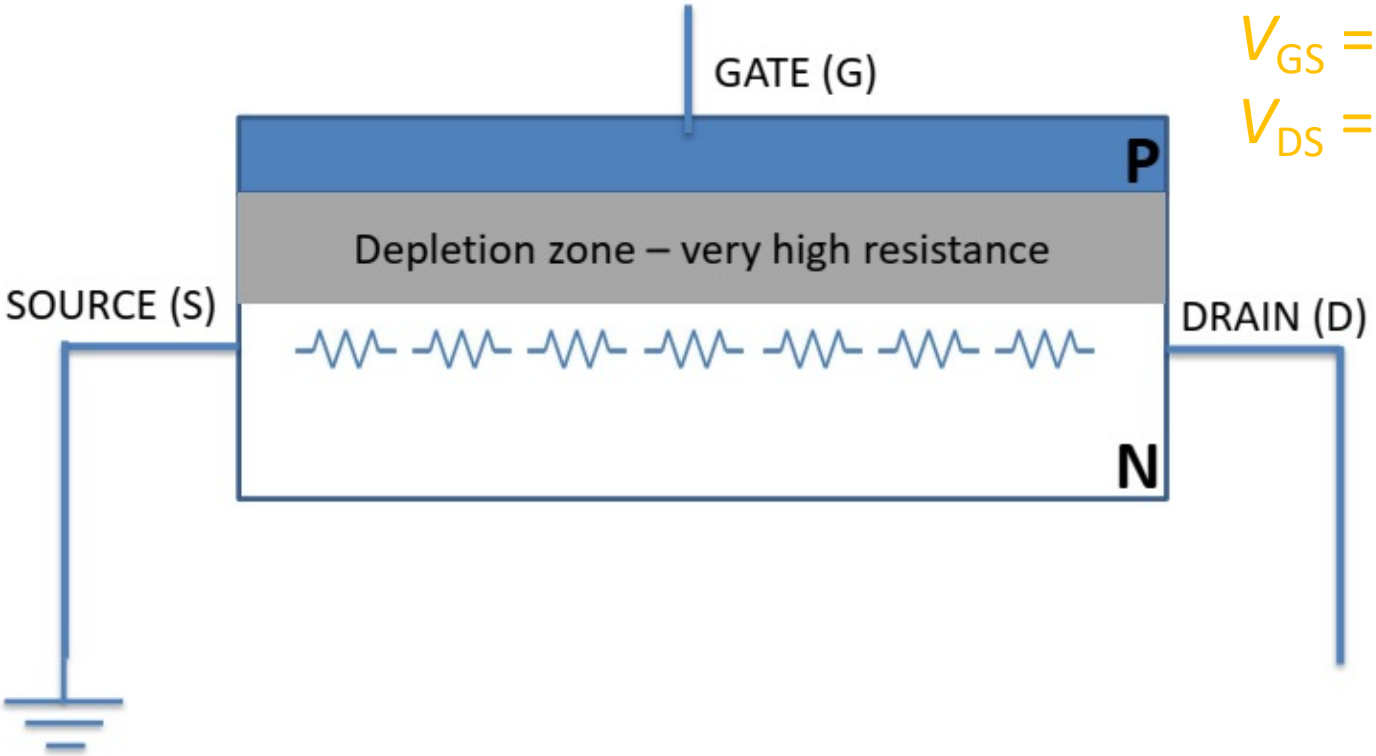
- We've squeezed the area in which the electrons can move by enhancing the depletion region. Higher voltage differences produce bigger fields and expel more and more negative charge carriers.

$$R = \rho \frac{L}{A}$$

- As the cross-sectional area reduces, the resistance goes up, limiting the amount of current that can flow.



$V_{DS} = 0$

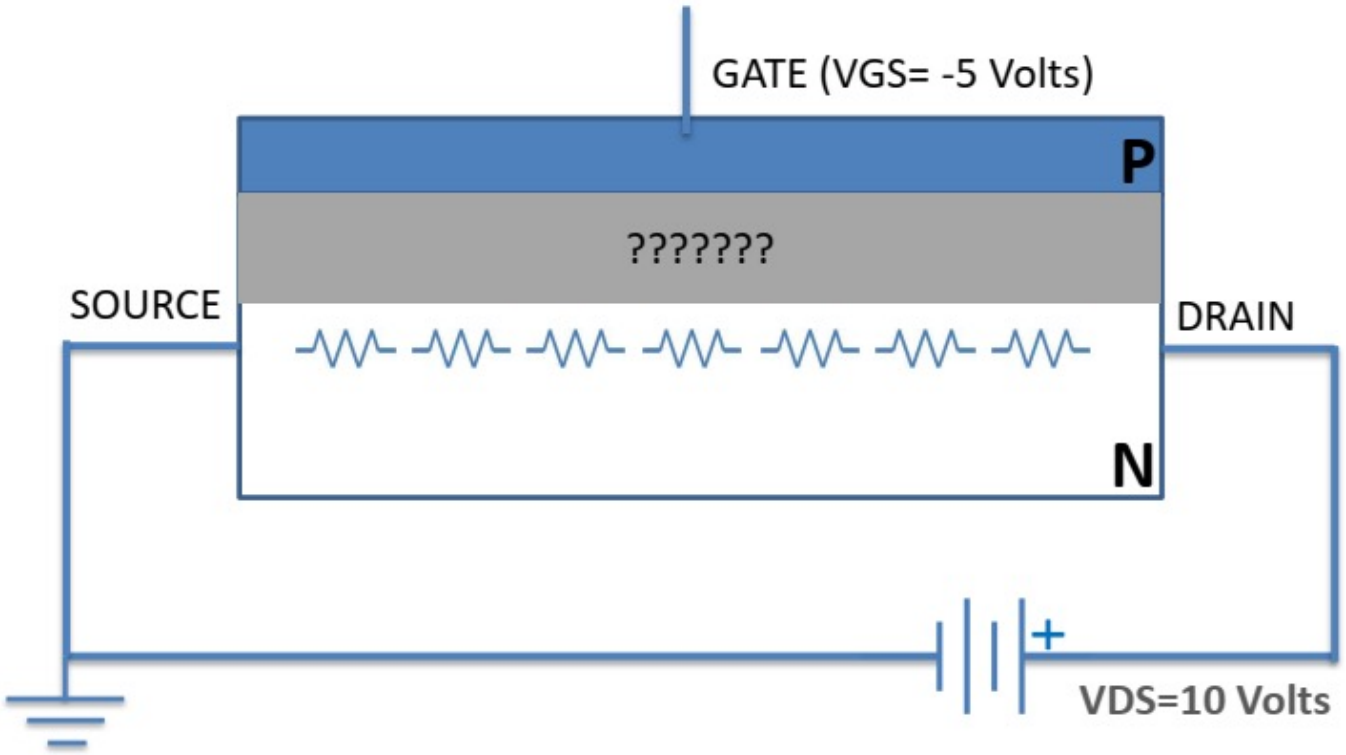


$V_{GS} = V_G - V_S$

$V_{DS} = V_D - V_S$

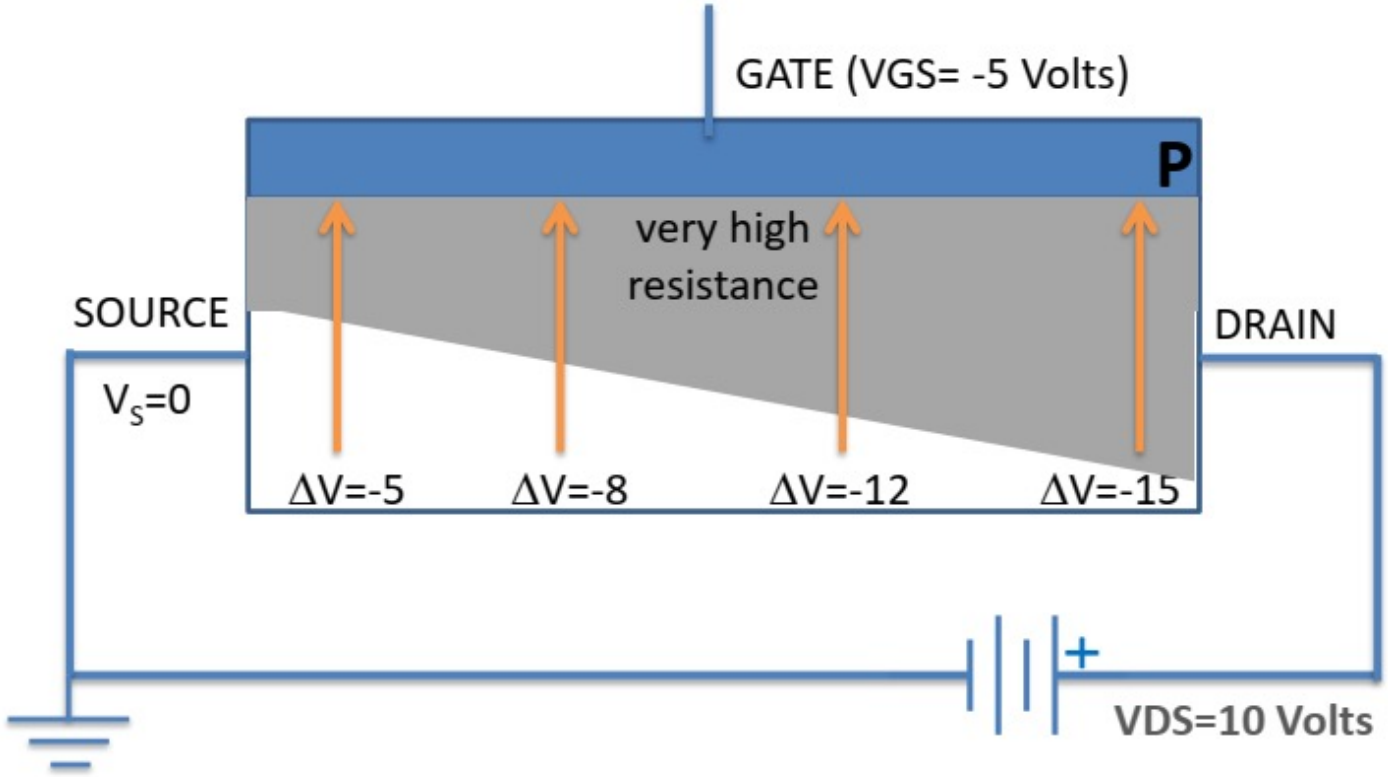
- The p-n junction must be reversed biased (say V_{GS} = -5 V).
- If no current flows, what is the electric potential difference across the p-n junction at different points INSIDE the device?

$V_{DS} > 0$



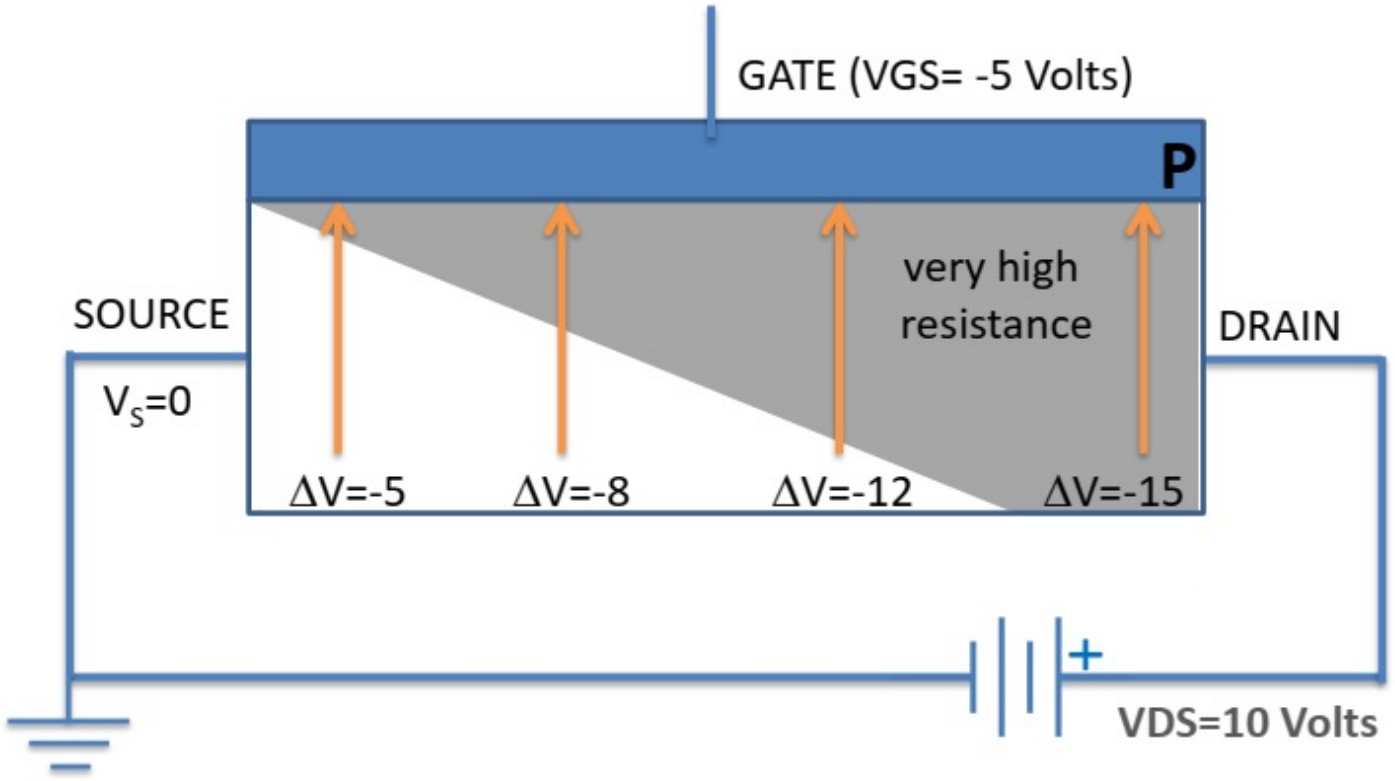
- Now consider if we apply a voltage between drain (D) and source (S), V_{DS} = +10 V, what will be the voltage difference across the p-n junction at different points in the device? What happens to the depletion region?

$V_{DS} > 0$



- Current flows in the channel, so the source terminal is at the ground potential (0 V), and the drain terminal is at $+V_{DS}$ = 10 V. There is a linear fall off in between. If we have too high a V_{DS}, what do you think will happen?

$V_{DS} >> 0$

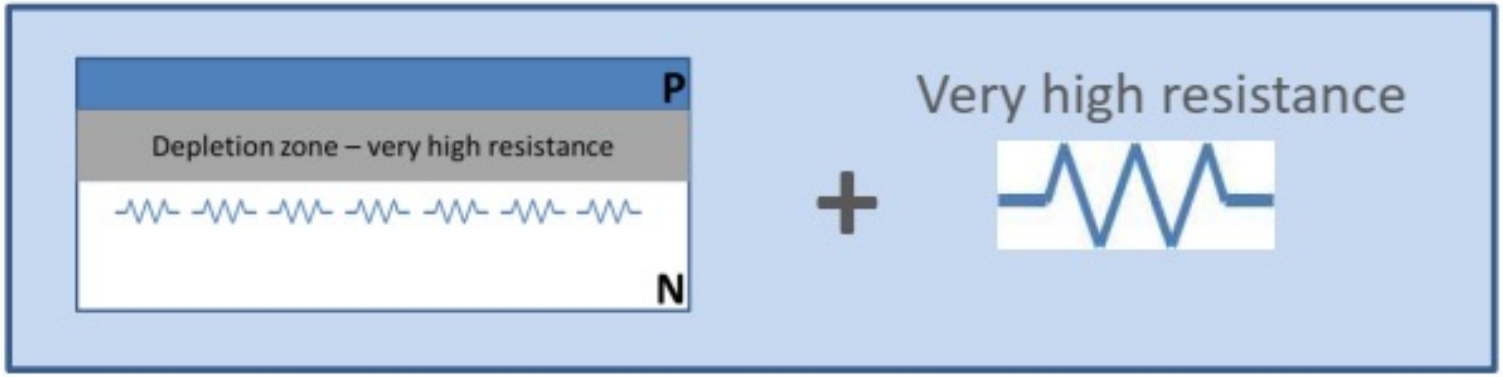


- This is called pinch-off. In theory no current can flow or at least a very high resistance is present. We can say that we've closed off the channel (in practice, the channel is never fully closed). So what do you think happens when no current can flow? ($V = IR$)

Pinch-Off Voltage

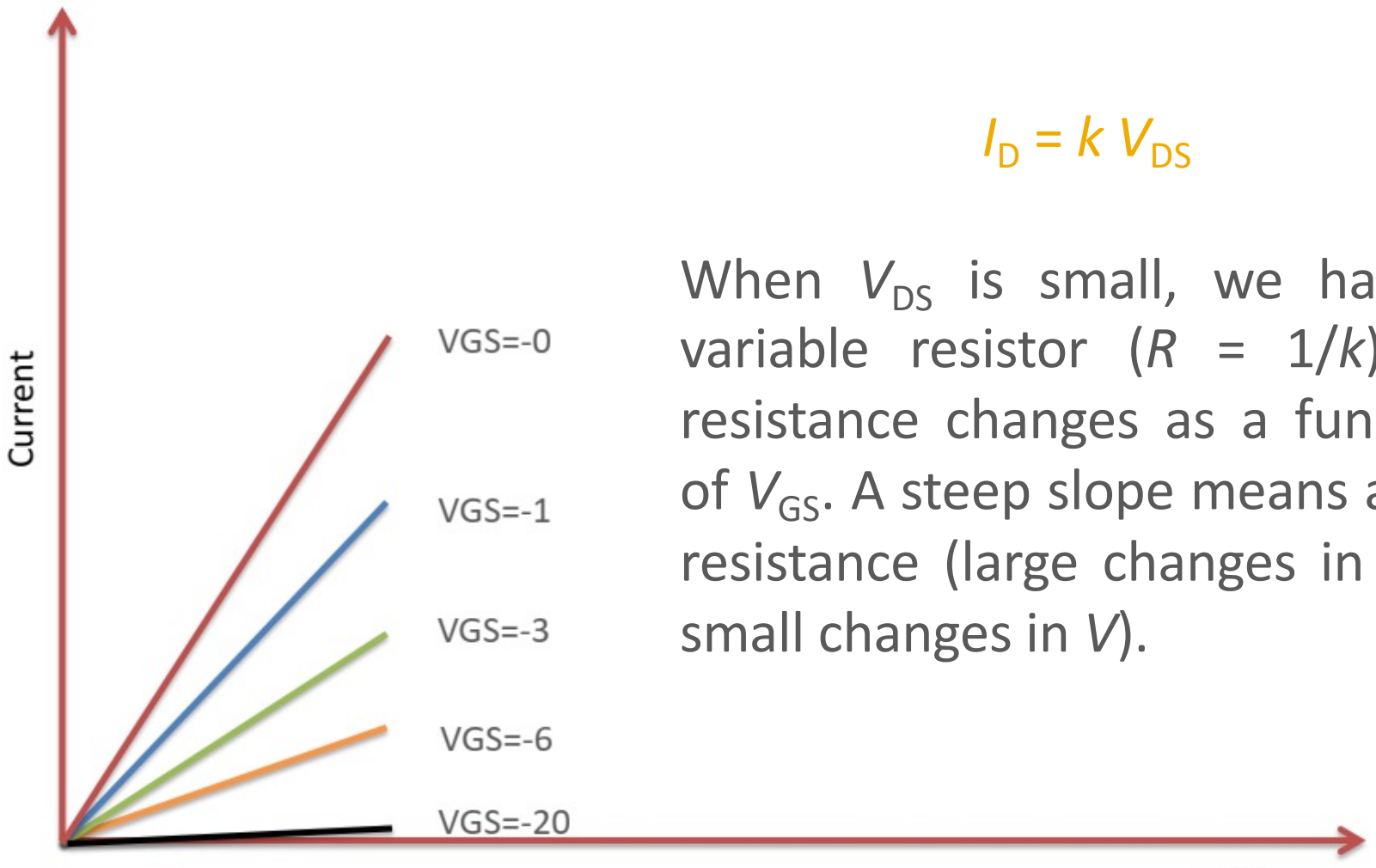
- In a JFET, when V_{GS} = 0, increasing V_{DS} leads to a narrowing of the conduction channel;
- Pinch-off refers to the condition when V_{DS} is increased to a level that the depletion region completely ”blocks” the conduction channel. The level of V_{DS} that establishes this condition is called the pinch-off voltage;
- The pinch-off voltage is also the level of V_{GS} required to completely shut down a JFET (I_D = 0 mA);
- V_P is defined as a negative voltage for n-channel JFETs and a positive voltage for p-channel JFETs.

What Happens at Pinch-Off?



- In reality, pinch-off does not fully shut down the conduction channel;
- So if we took the high resistance bit outside, we'd have a FET that COULD conduct and a high external resistance. In that sense some current will always flow, no matter what the applied voltage is;
- As the applied voltage gets bigger, the "external" resistance gets bigger, but not as fast as the voltage climbs, so we get some increase in current in saturation.

Drain Characteristics (I_D *vs.* V_{DS})



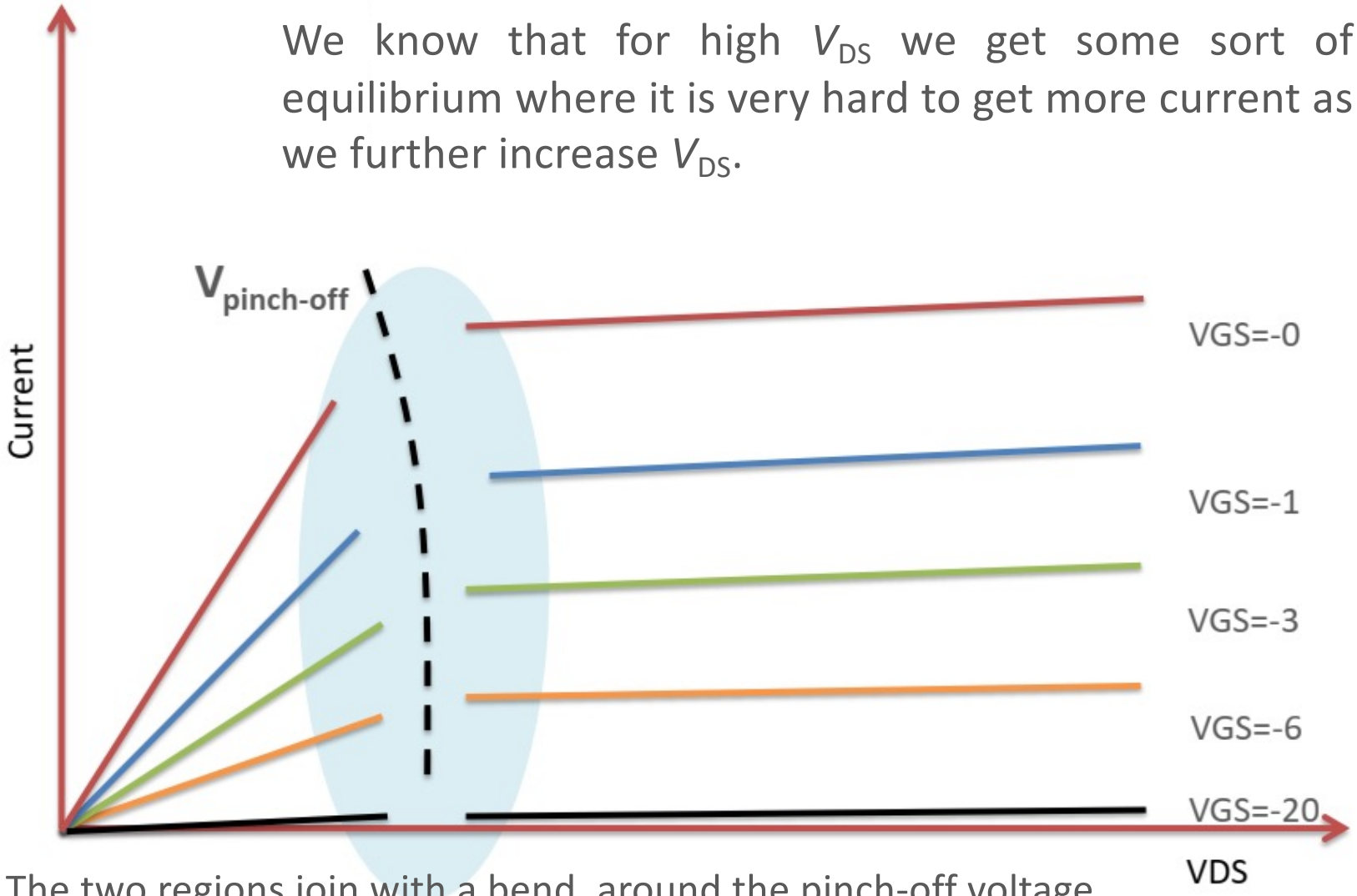
$$I_D = k\, V_{DS}$$

When V_{DS} is small, we have a variable resistor ($R = 1/k$). Its resistance changes as a function of V_{GS}. A steep slope means a low resistance (large changes in I for small changes in V).

PS: if $|V_{GS}|$ is too high, no current can flow.

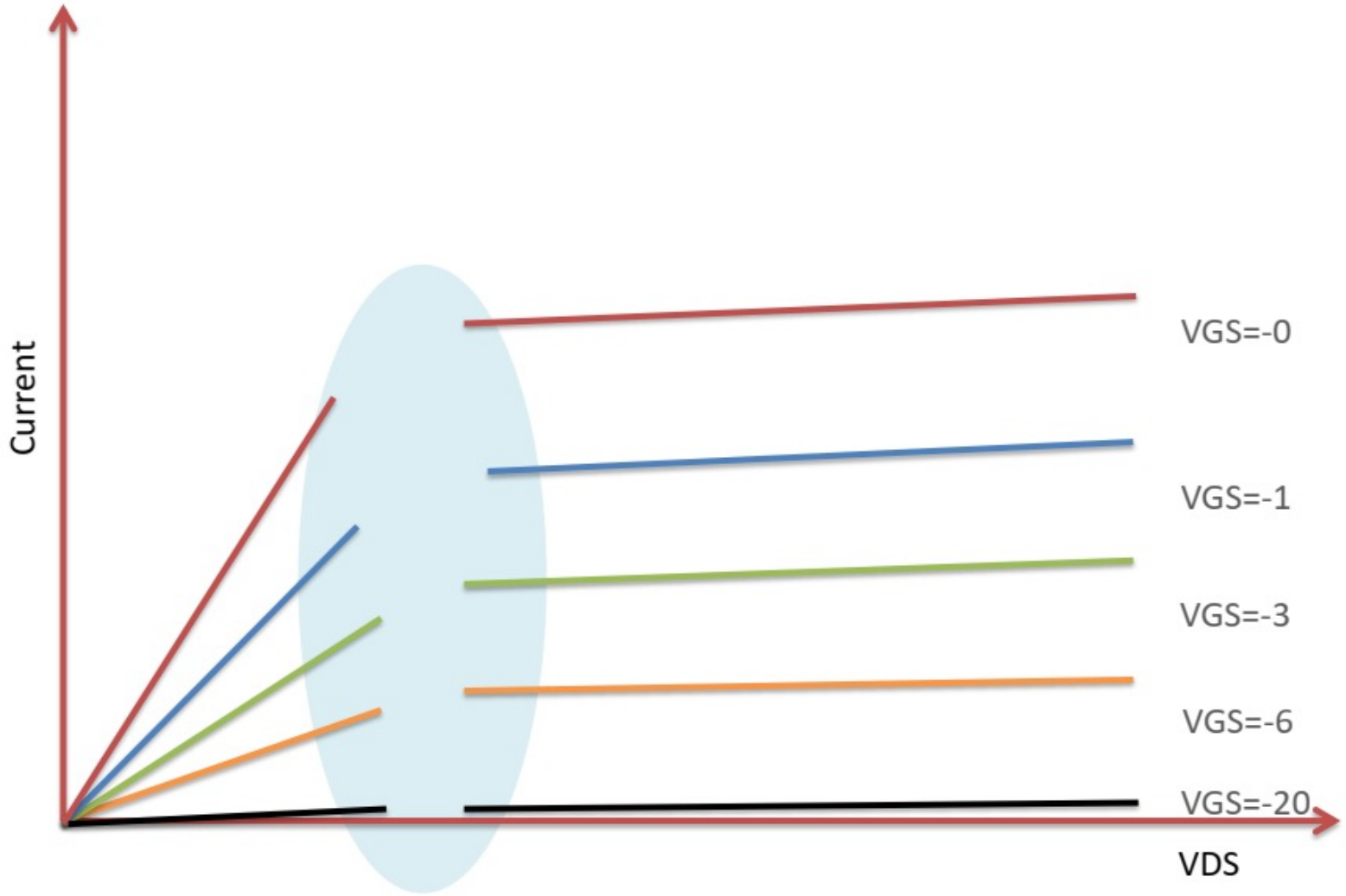
Drain Characteristics (I_D *vs.* V_{DS})

We know that for high V_{DS} we get some sort of equilibrium where it is very hard to get more current as we further increase V_{DS}.



The two regions join with a bend, around the pinch-off voltage.

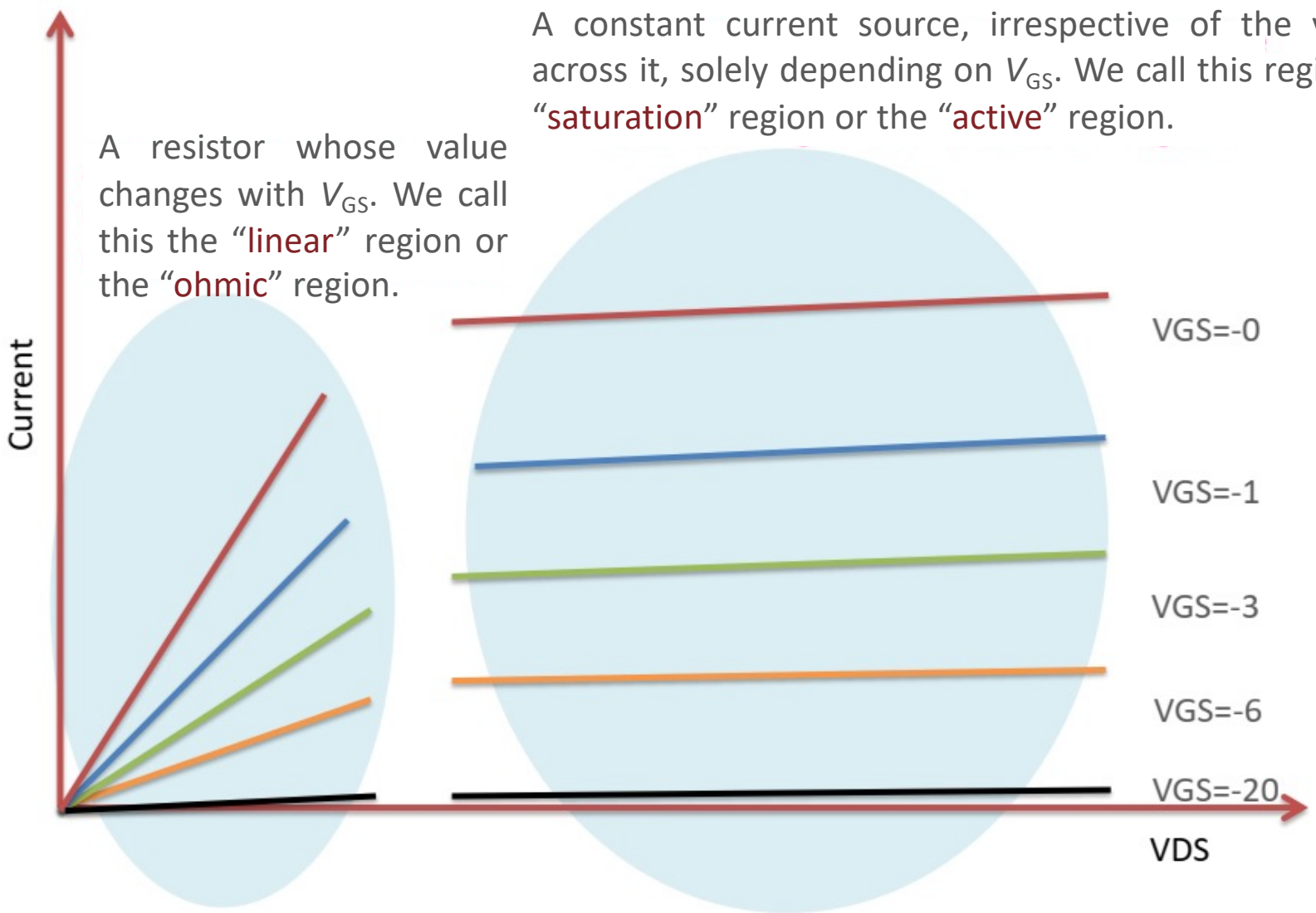
What Do You See in the Drain Characteristics?



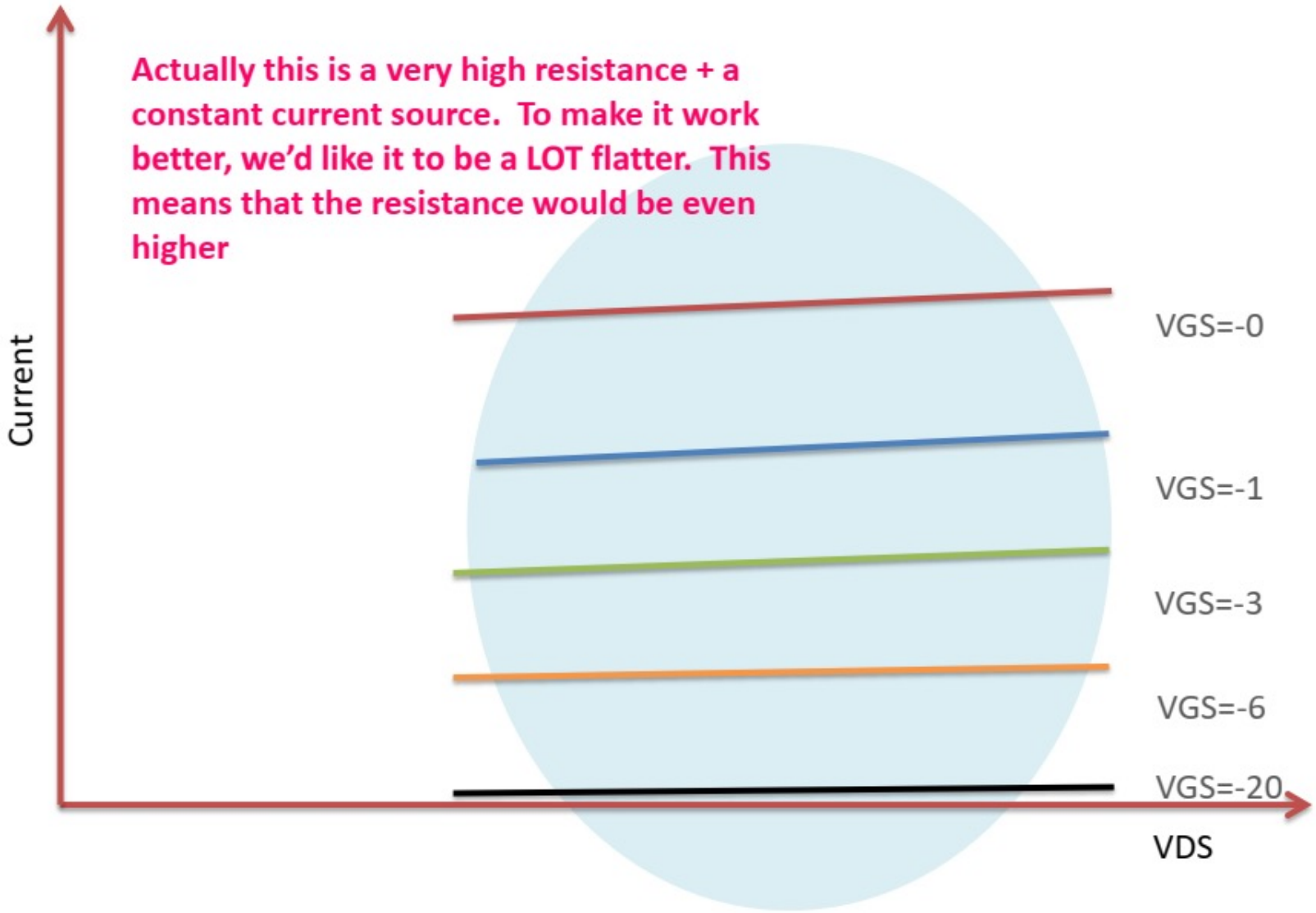
Two Regions in the Drain Characteristics

A constant current source, irrespective of the voltage across it, solely depending on V_{GS}. We call this region the "saturation" region or the "active" region.

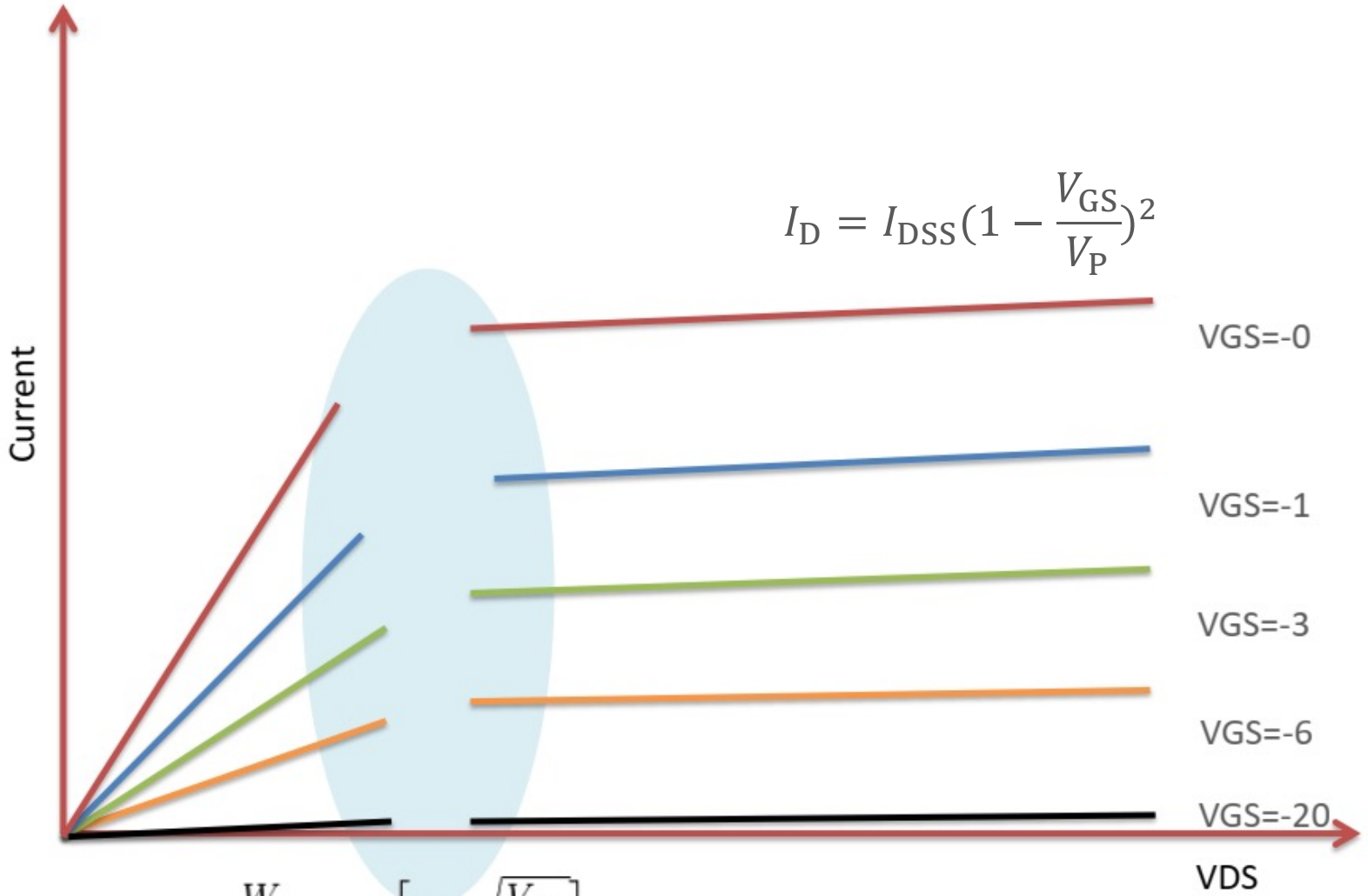
A resistor whose value changes with V_{GS}. We call this the "linear" region or the "ohmic" region.



Saturation Region



Drain Characteristics Equations



$$I_D = (2a)\frac{W}{L}qN_d\mu_n\left[1 - \sqrt{\frac{V_{GS}}{V_P}}\right]V_{DS}$$

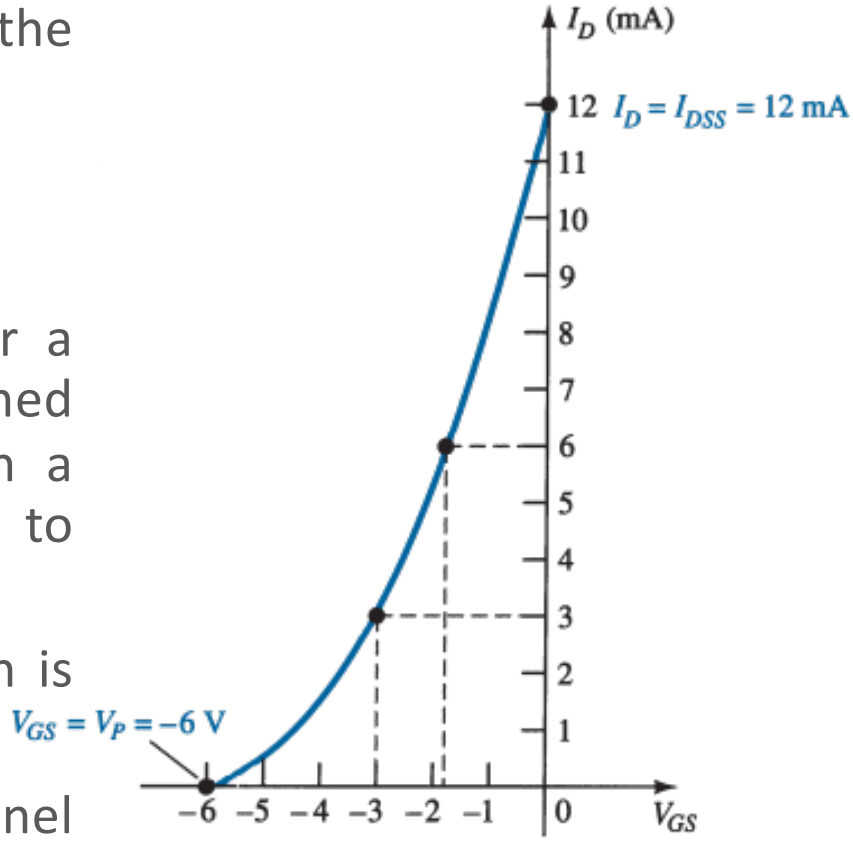
Note: If V_{GS} = const., $I_D = G \times V_{DS}$.

Shockley's (Transistor) Equation

- In the saturation region, the relation between the output current I_D and the input control parameter, V_{GS} is nonlinear.

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

- I_{DSS} is the maximum drain current for a JFET that occurs at V_{GS} = 0. I_{DSS} is named after the "drain-to-source current with a short-circuit connection from gate to source";
- V_{GS} is the gate-to-source voltage, which is the control parameter;
- V_P is the pinch-off voltage. For an n-channel JFET, both V_{GS} and V_P < 0.

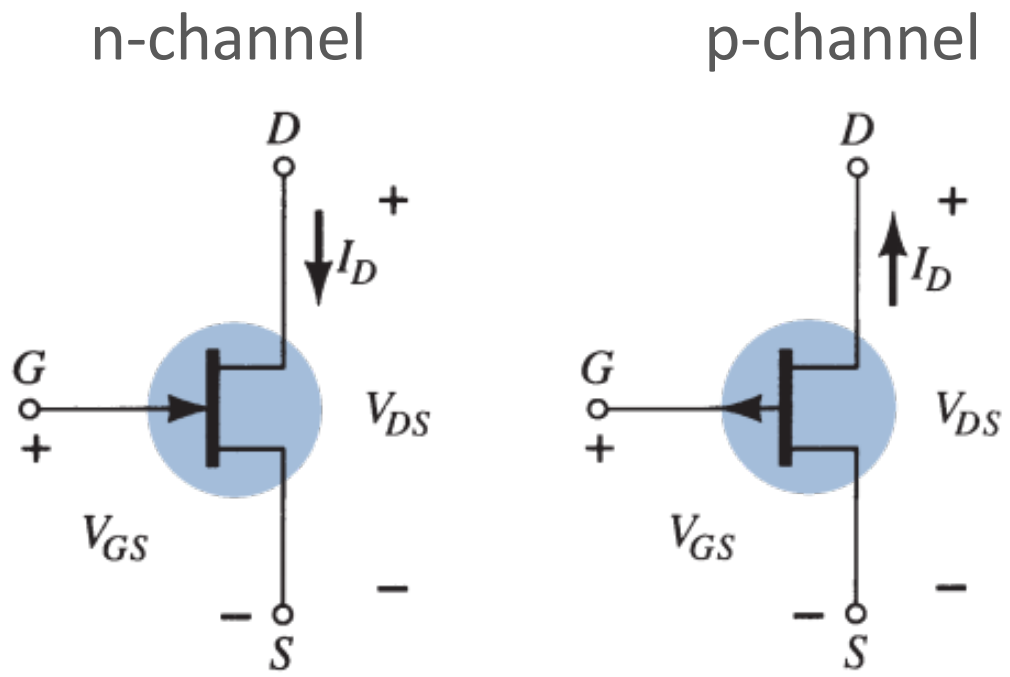


Additional Remarks: JFETs

- JFETs come in n type as well as p type.
- In an n-type JFET, the source is connected to the ground or the low voltage side. In a p-type JFET, the source is connected to the high voltage side.
- The source is named because that is where the electrons come from in an n-type material or where the holes come from in a p-type material. The source is where the majority charge carriers come out and the drain is where they go after leaving the device.
- A good visual explanation of a JFET can be found here (Flash required).

  http://www-g.eng.cam.ac.uk/mmg/teaching/linearcircuits/jfet.html

Circuit Symbols for JFETs



- Pay attention to the directions of the arrows in the symbols. The direction of the arrow represents the forward bias direction of a p-n junction in the FET.

Do We Use JFETs a Lot?

- Well no, it depends a little bit on whom you ask. But in general, we don't, at least not as much as some would think.

- Ideally we'd like the flat part in the saturation region to be very flat. JFETs can be good but they don't get it flat enough… increasing V_{DS} pushes more current through even when a JFET is in saturation. They also never turn off (block all current flows) properly.

- JFETs are mainly used in some niche applications today where high gain has to be combined with low noise, e.g., preamplifiers for interfacing low-level signals.

- However, the most important reason is that MOSFETs are a LOT better, they are especially flat in the saturation region, and they can stop current flowing very well (fully off).