

EE203 LAB3 Biasing a FET Transistor

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☐ EQUIPMENT :

A voltage source, voltmeters, a laboratory lead kit A signal generator and an oscilloscope.

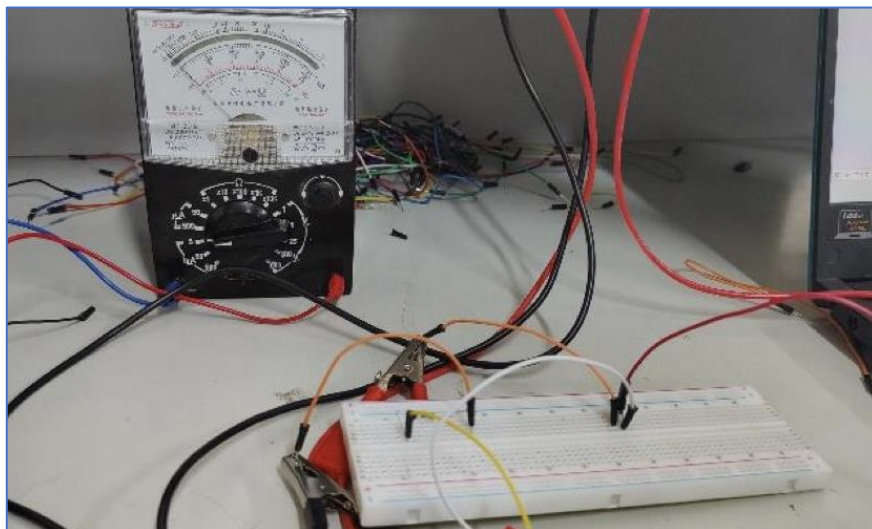
☐ OBJECTIVE :

The purpose of this experiment is to demonstrate various biasing techniques for FET transistors

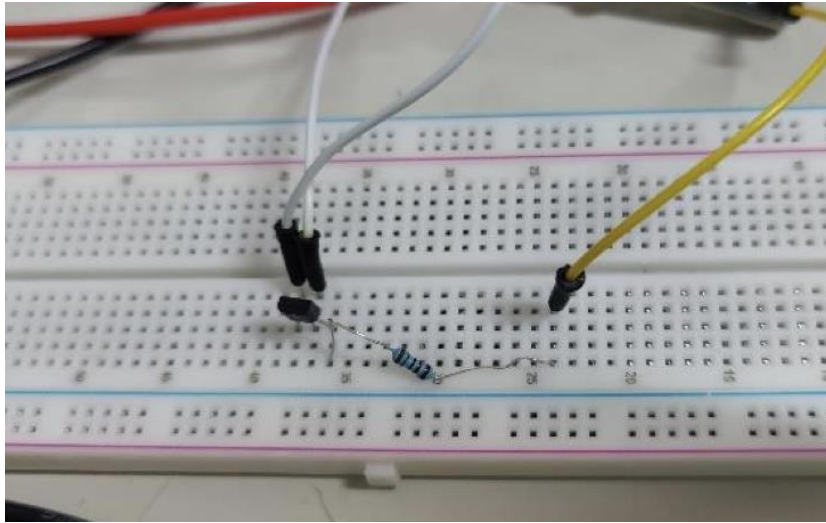
Part1

For PMOS, I measure that the V_{in} is 1.99V,

So that, $V_t = V_{gs} = -V_{sg} = V_{in} - 5 = -3.01V$



For NMOS, I measure that the V_{in} is 1.96V,
so $V_t = V_g = V_{in} = 1.96V$



So PMOS $V_t = -3.01V$,
And NMOS $V_t = 1.96V$

Part2

PMOS,



I measure that when the V_{in} is 1.59, the V_{out} is 2.5V

$$V_{gs} = -V_{sg} = V_{in} - 5 = -3.41V$$

$$V_{gs} - V_t = -0.4V$$

So $V_{ds} = V_{out-0} = 2.5V$

$V_{ds} > V_{gs} - V_t$,

This equation is true So it meets the formula, I verify it is in saturation.

NMOS



I measure that when the V_{in} is 3.01, the V_{out} is 2.5V

$V_{gs} = V_{in} = 3.01V$

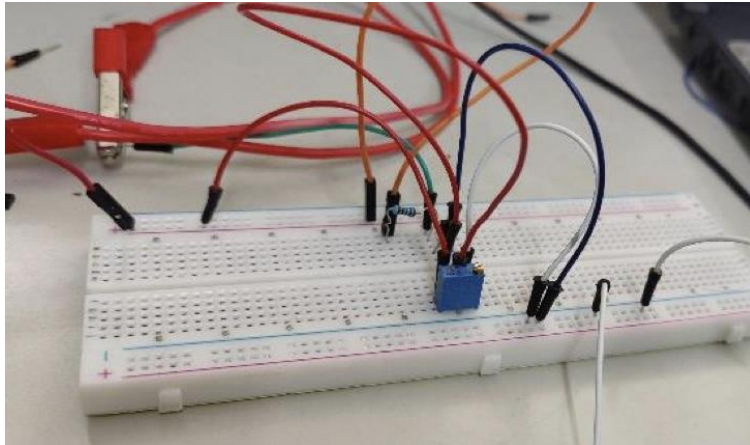
$V_{gs} - V_t = 1.05V$

So $V_{ds} = V_{out-0} = 2.5V$

$V_{ds} > V_{gs} - V_t$,

This equation is true So it meets the formula, I verify it is in saturation.

PART3



I measure that when

$$R_{bias1}=831\Omega$$

$$R_{bias2}=1212\Omega,$$

I could make $V_{out}=2.5V$.

So the ratio of two resistances is

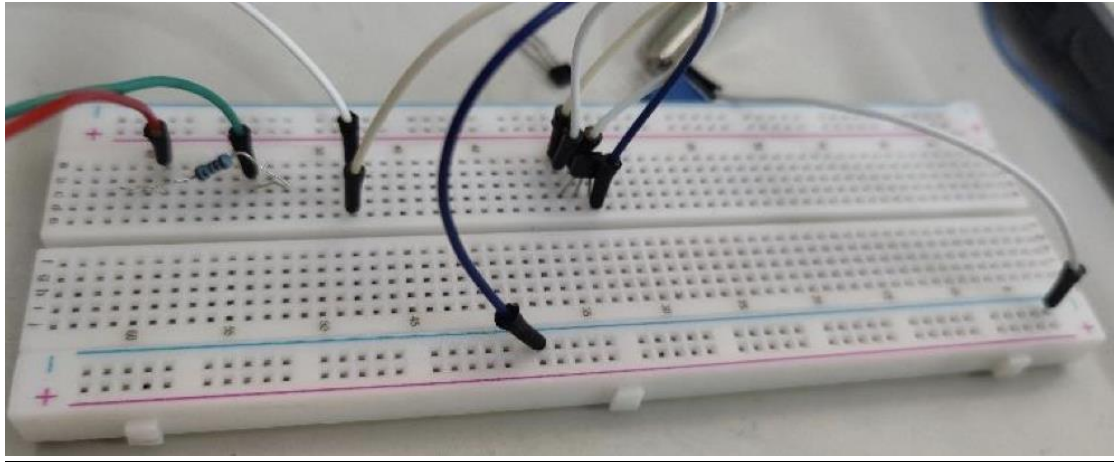
$$R_{bias1}/R_{bias2}=1212\Omega/831\Omega=1.46$$

the ratio of divider resistance is 1.46

Would there be any benefit to going for very small resistors as compared to very big resistors?

Because the resistance between GS is not infinite actually, so I could use a small resistor. It would minimize error. Gate resistance is small, switching device on and off fast, small switching loss; Otherwise, it is slow and the switching loss is large.

PART4



I measure that

$$I_{ds} = 2.7\text{mA}$$

$$V_{out} = 5\text{V} - I_{ds}$$

$$R = 2.3\text{V}$$

$$\text{And, } V_{ds} = V_{out} - 0 = 2.3\text{V}$$

So the equivalent resistance of MOS is $V_{ds}/I_{ds} = 851.85\Omega$

For this Drain-feedback biasing model. The voltage of THE VDD will be partially applied to the G terminal to achieve the effect of controlling the V_{gs} .

□ Summary

1. Firstly, I successfully construct the circuit, and measure values that I want.
2. Then I calculate the V_t of NMOS and PMOS.
3. Next, I also set two biasing approaches to finish the required tasks and use resistor divider correctly and get the ratio of two resistance.
4. Ultimately, I set Drain-feedback biasing model, I successfully get the equivalent resistance.

That's all, thank you!

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