EE204FZ
Lecture 4
Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)

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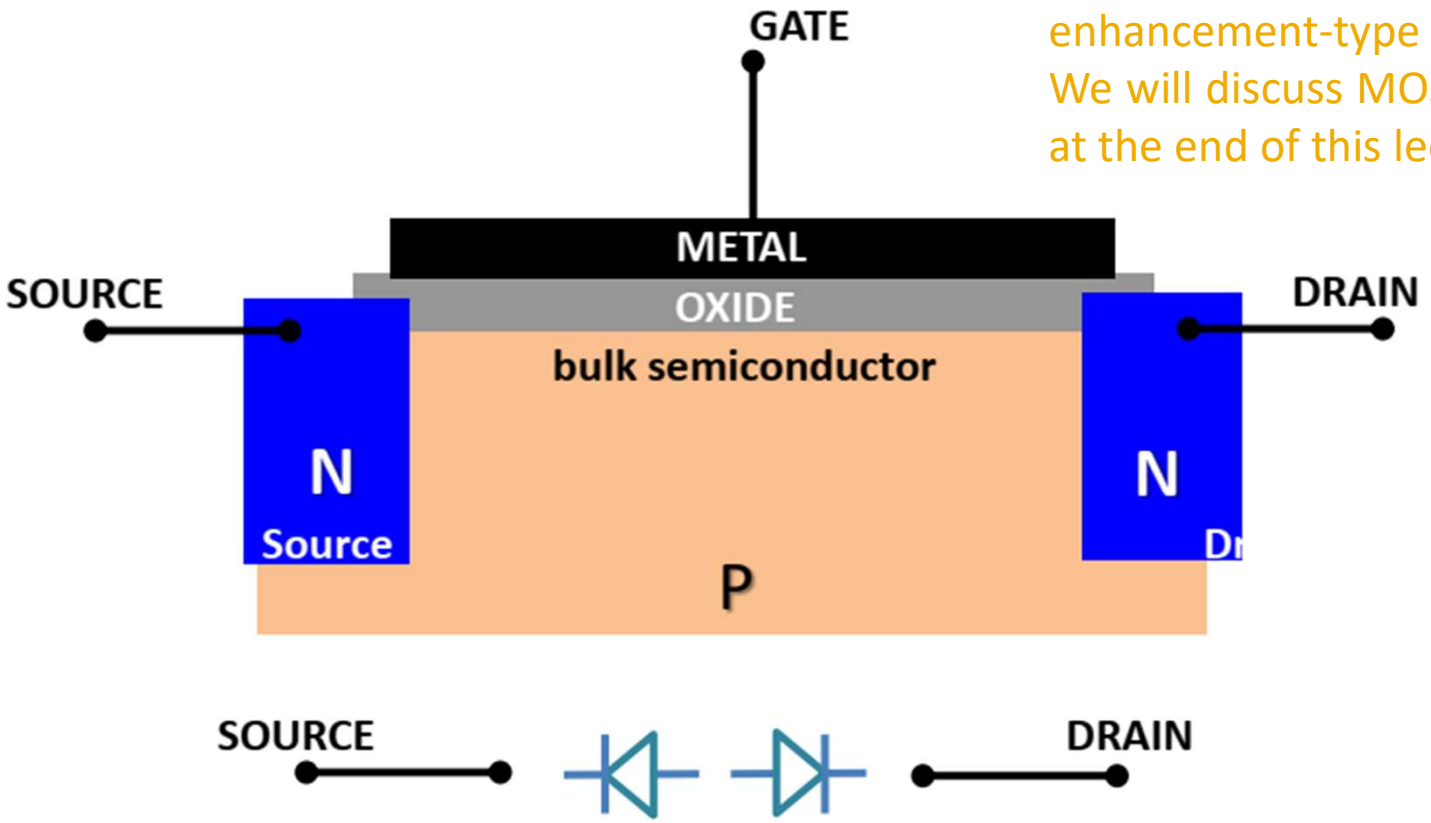
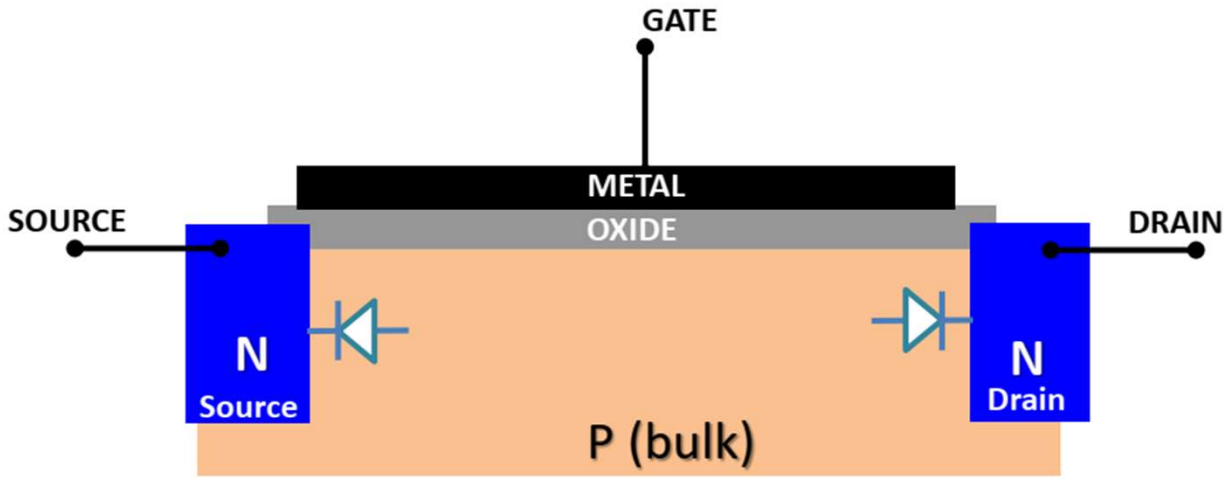
Metal-Oxide-Semiconductor FETs

This is in fact an n-channel enhancement-type MOSFET. We will discuss MOSFET types at the end of this lecture.



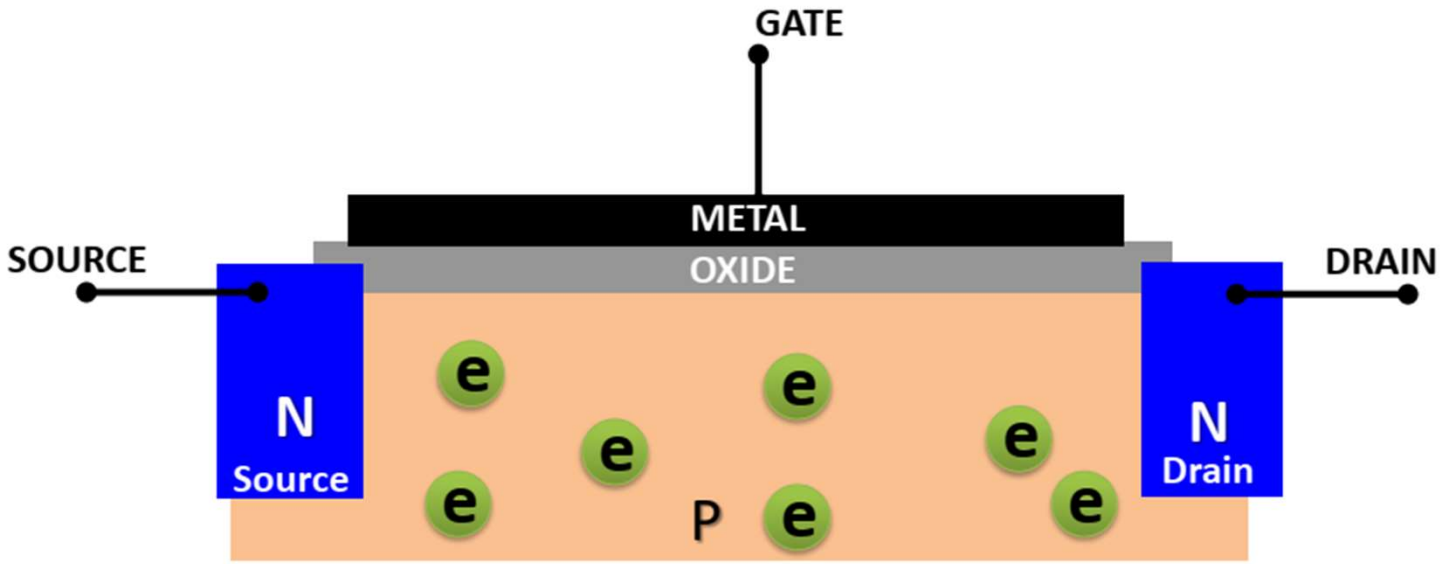
http://www-g.eng.cam.ac.uk/mmg/teaching/linearcircuits/mosfet.html

Metal-Oxide-Semiconductor FETs



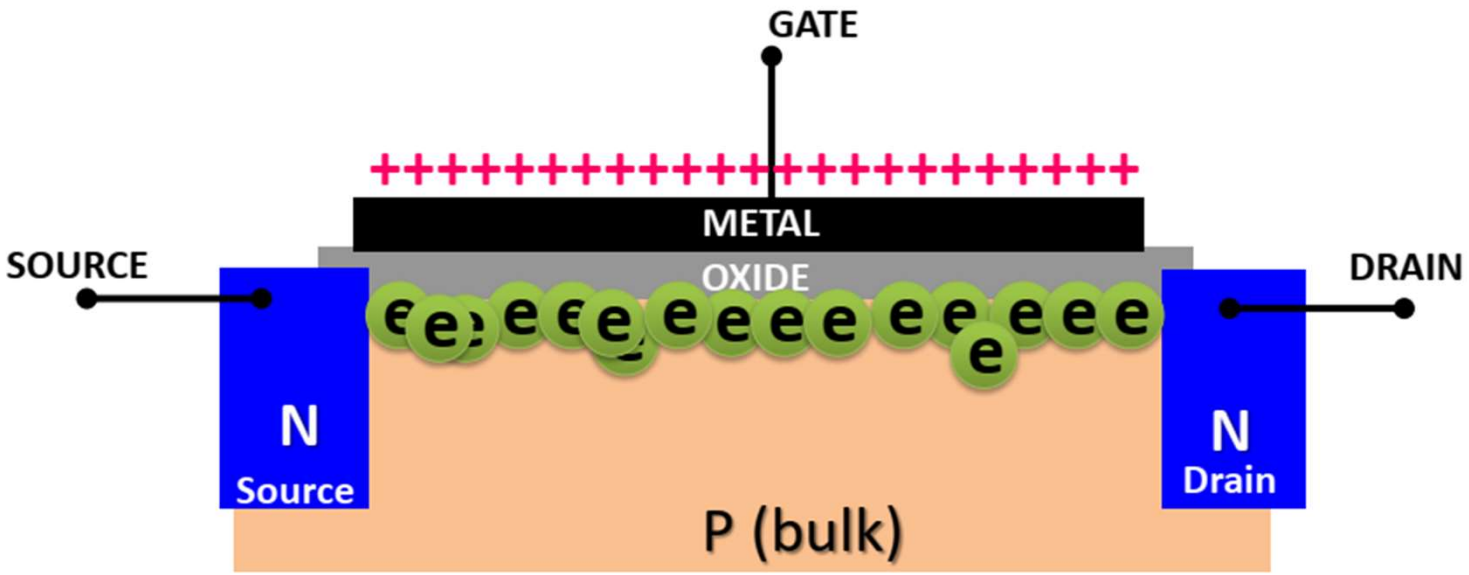
- Now in vague memory of solid-state electronics, a p-n junction is made when p-type and n-type semiconductors come together, and current can't flow through a reverse biased p-n junction (It is a diode). In this scenario, current cannot NORMALLY flow from source to drain.
- Also note, the device is symmetric, so source and drain are swappable until you apply a voltage.

Metal-Oxide-Semiconductor FETs



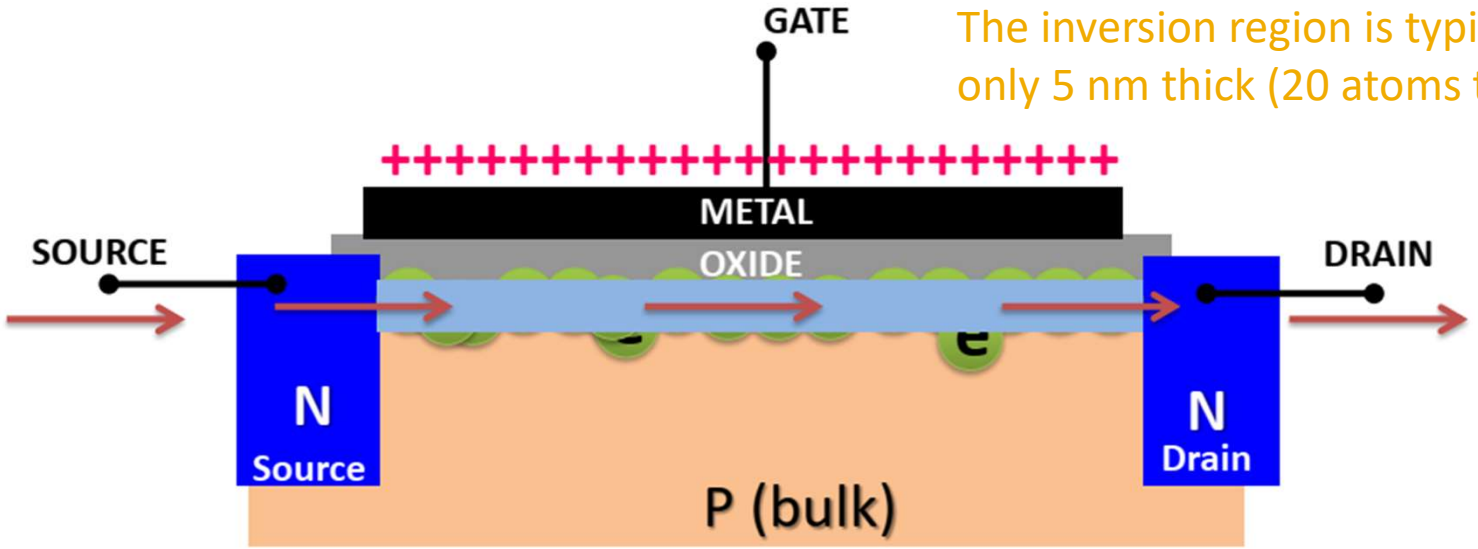
- An n-type material is made when dopants make an excess of electrons. A p-type material is made when dopants make a shortage of electrons. But there are, however, always some electrons in the material.
- Here's a question, how can we make a p-type material n-type?

Metal-Oxide-Semiconductor FETs



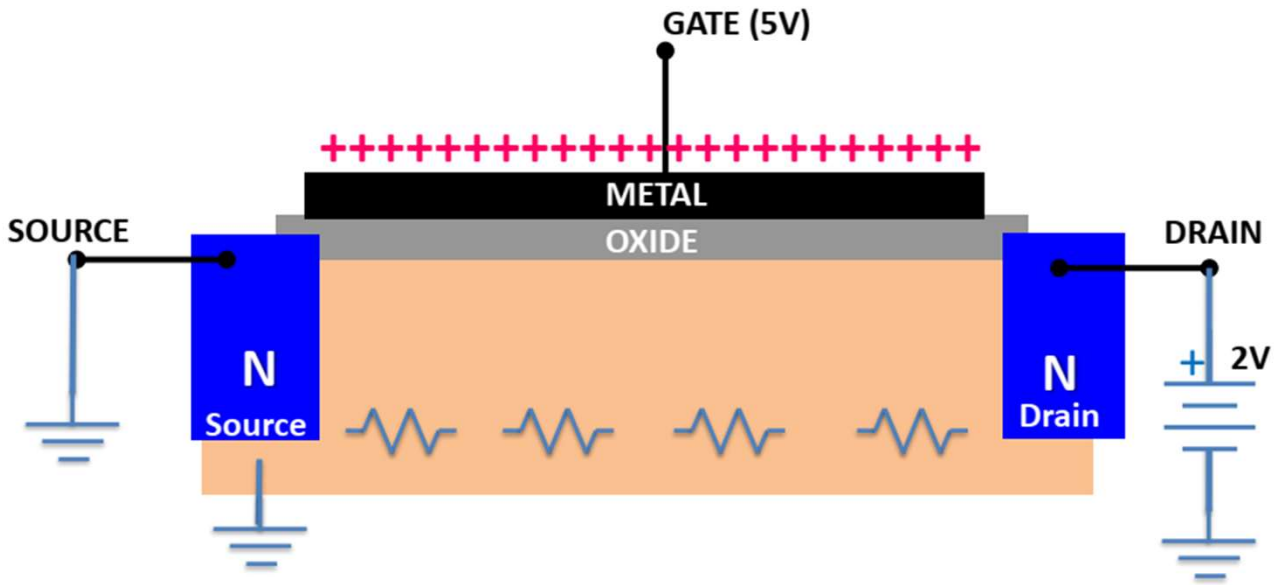
- So all the electrons in the p-type material get attracted to the POSITIVE gate, but the oxide is a good insulator and stops them from getting over to the gate.
- This makes the rest of the material more p-type.
- If enough electrons get attracted, what happens to the p-n junction???

Metal-Oxide-Semiconductor FETs



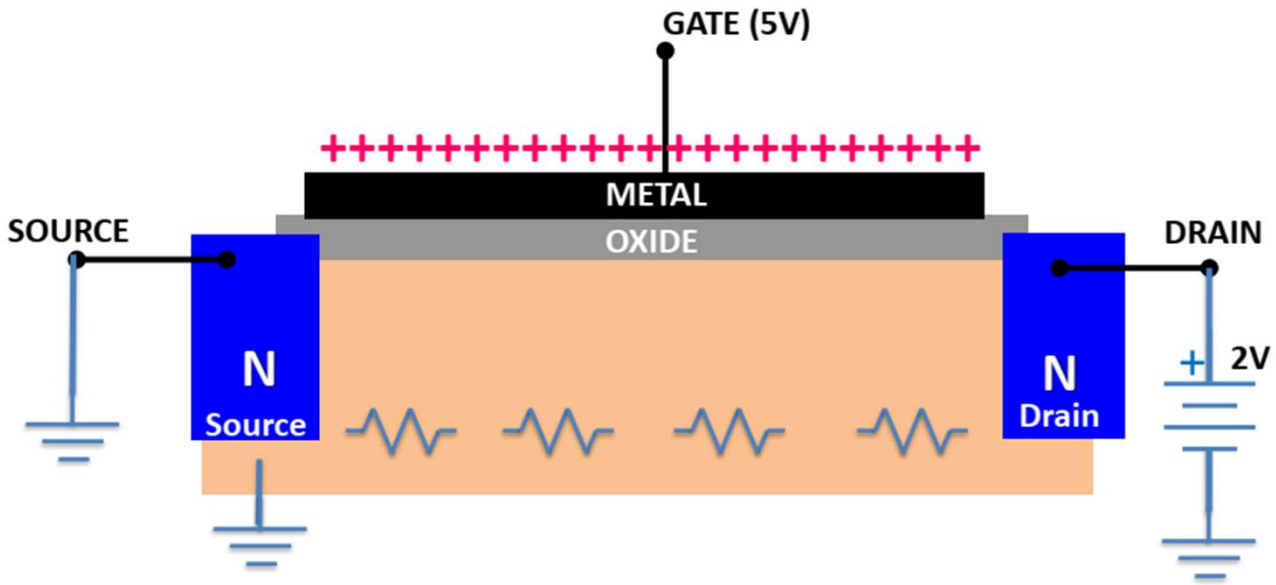
- We call the newly "generated" n-type region the inversion region as we swapped region types. It only lasts as long as the gate is charged.
- There is a minimum gate-bulk voltage difference that needs to be achieved for an inversion region to form. We call this V_T (the threshold voltage).
- So now we have n → n → n, there is no p-n junction, current can now flow.

Metal-Oxide-Semiconductor FETs



- So we've connected the bulk to GROUND.
- We've connected the source to GROUND.
- We've connected the gate to +5 V.
- We've connected the drain to +2 V.
- What happens?

Metal-Oxide-Semiconductor FETs



- So we've connected the bulk to GROUND.
- We've connected the source to GROUND.
- We've connected the gate to +5 V.

} An inversion region will form as the electrons are attracted to the gate.

- We've connected the drain to +2 V.

} Current will flow.

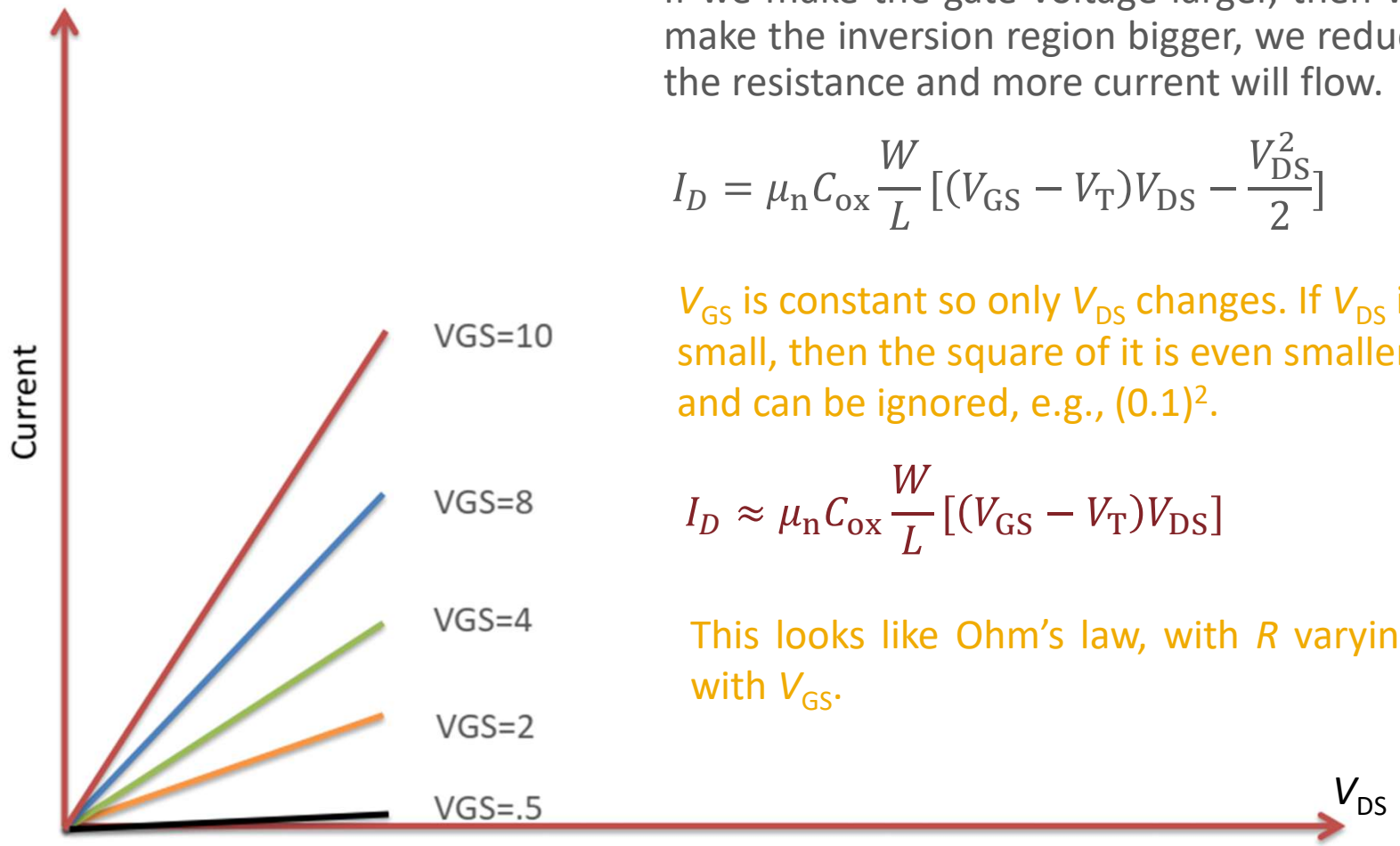
The MOSFET Equation

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

- μ_n: Mobility (of electrons) at the channel surface;
- C_{ox}: Gate oxide capacitance in F/m^2;
- L and W: Channel length and width, respectively;
- V_T: Threshold voltage;
- V_{GS} and V_{DS}: $V_{GS} = V_G - V_S$ and $V_{DS} = V_D - V_S$.

When you see a complex equation, try to spot the constants that depend on the construction and physical make up of the device. Even these 'complex' equations are simplifications. Full models of transistors can be 100-page long!

Plotting the MOSFET Equation



If we make the gate voltage larger, then we make the inversion region bigger, we reduce the resistance and more current will flow.

$$I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

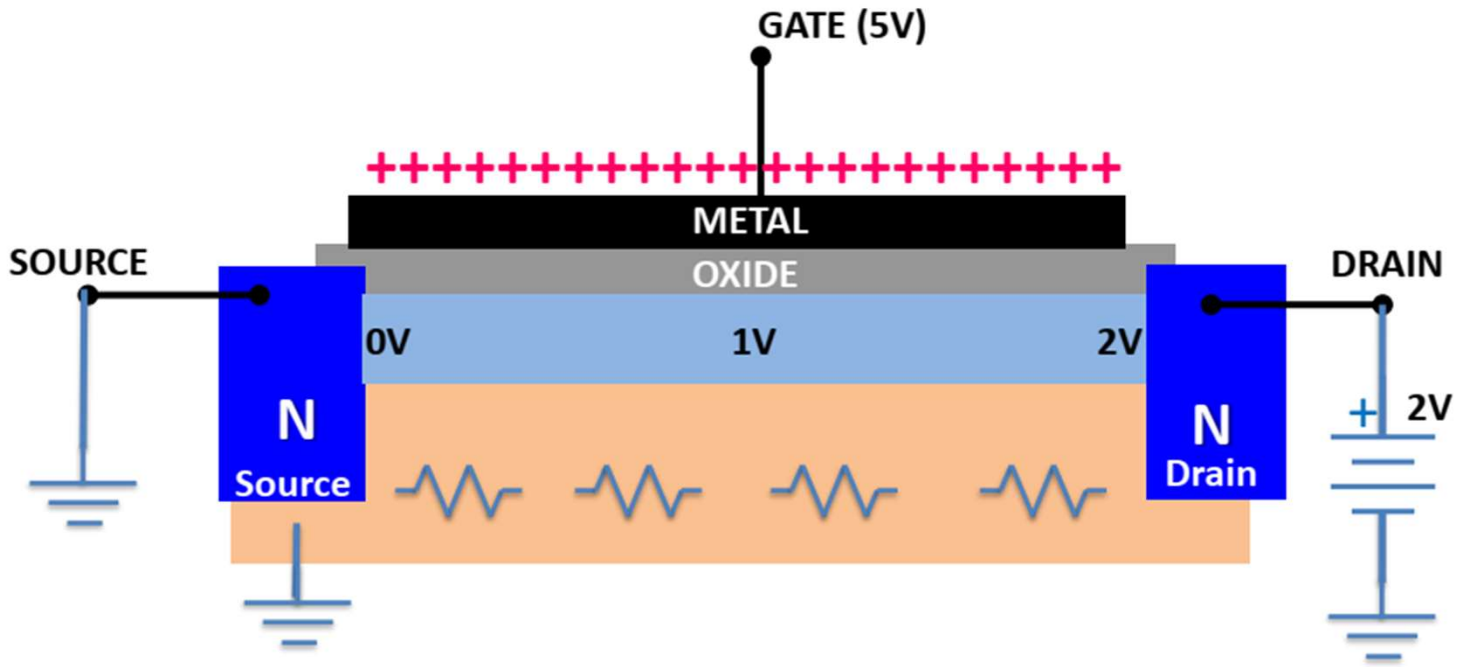
V_{GS} is constant so only V_{DS} changes. If V_{DS} is small, then the square of it is even smaller and can be ignored, e.g., $(0.1)^2$.

$$I_D \approx \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS}]$$

This looks like Ohm's law, with R varying with V_{GS}.

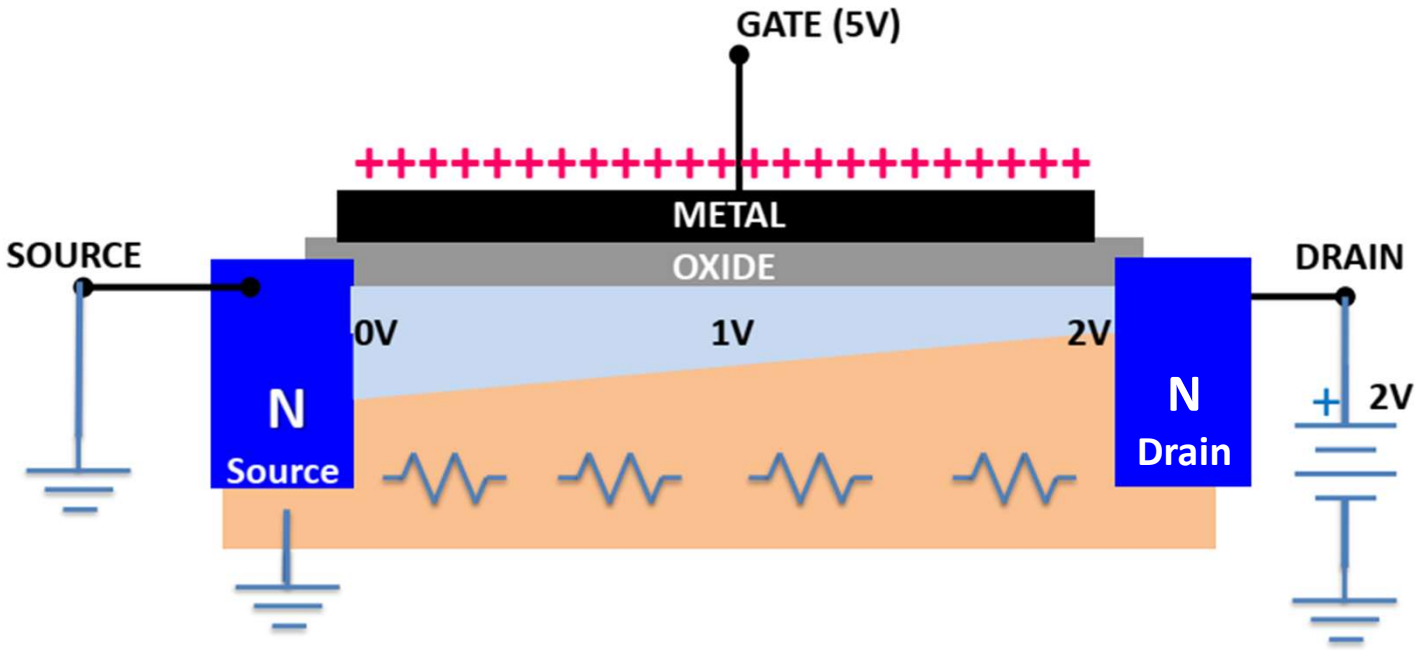
PS: V_{GS} needs to be bigger than V_T to work (typically 0.3 Volts).

The Effect of V_{DS}



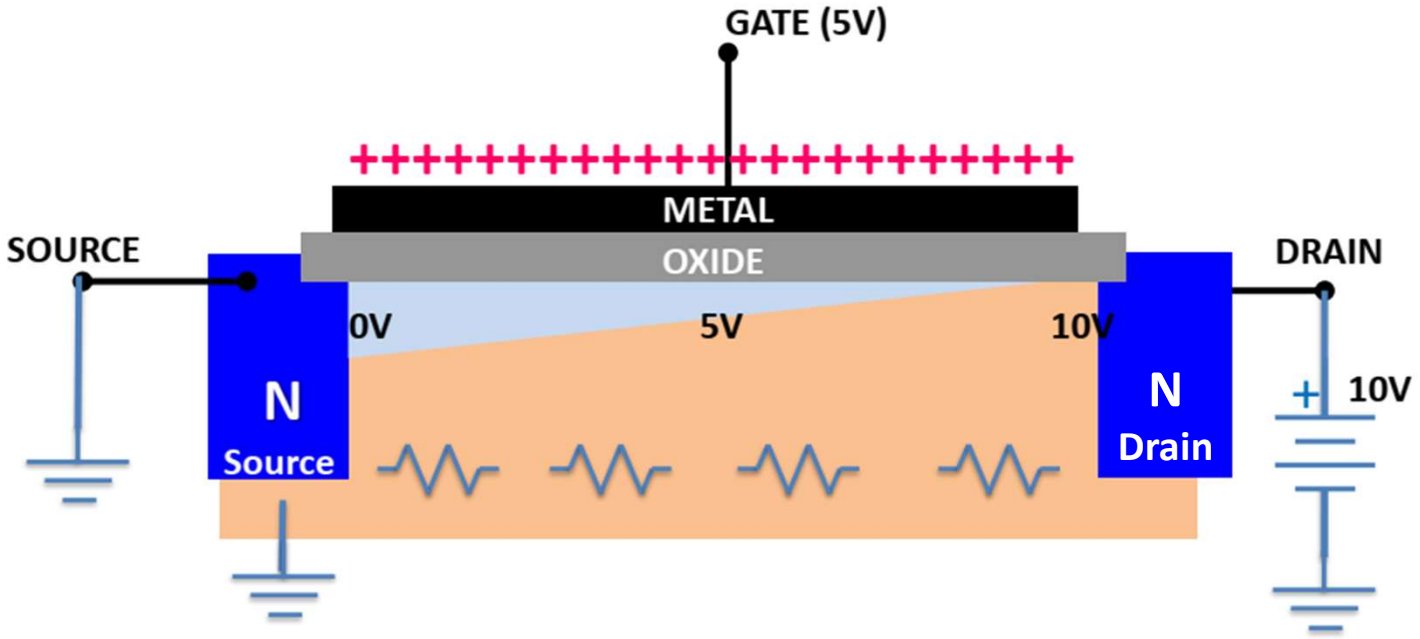
- Internally it's just a resistor, so the voltage at the drain starts at 2 V and drops to zero at the source side. If the resistance is the same everywhere, it will be a linear drop off.
- What does this do to the inversion region?

The Effect of V_{DS}



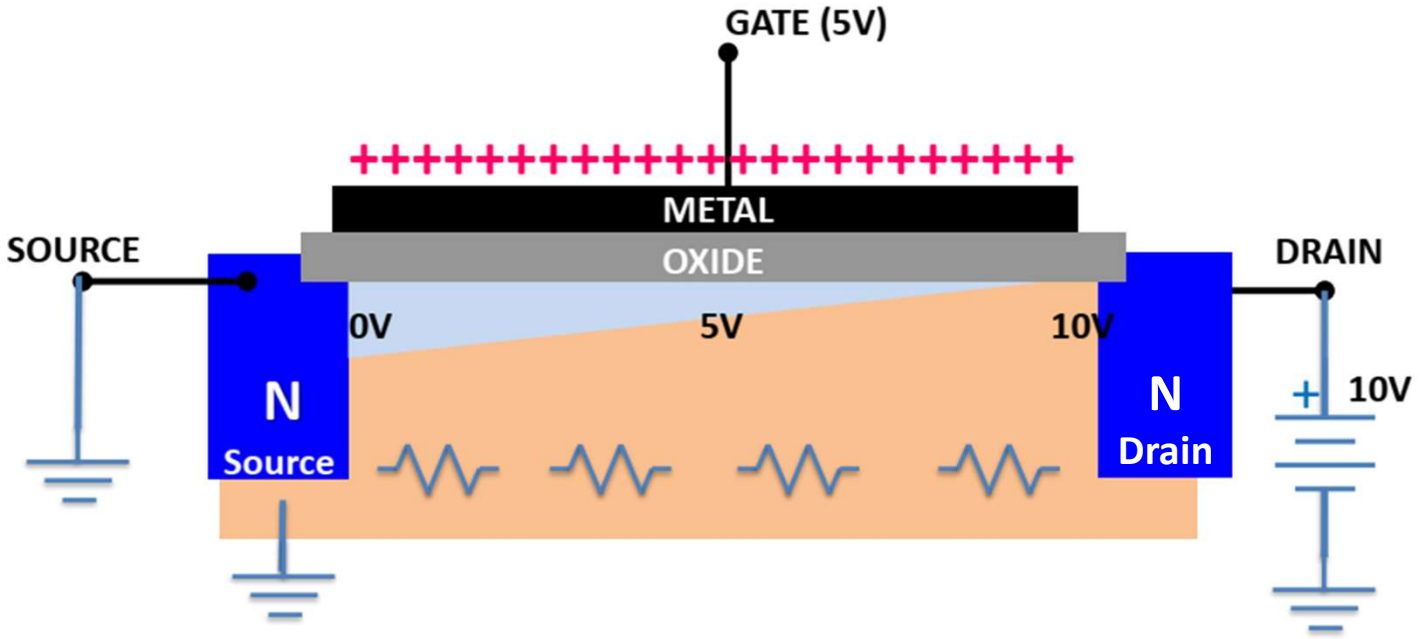
- Inversion regions are bigger if the voltage difference is bigger, so we get a triangular-shaped region.
- The bigger the region, the less resistive it is.

Now Increase V_{DS}



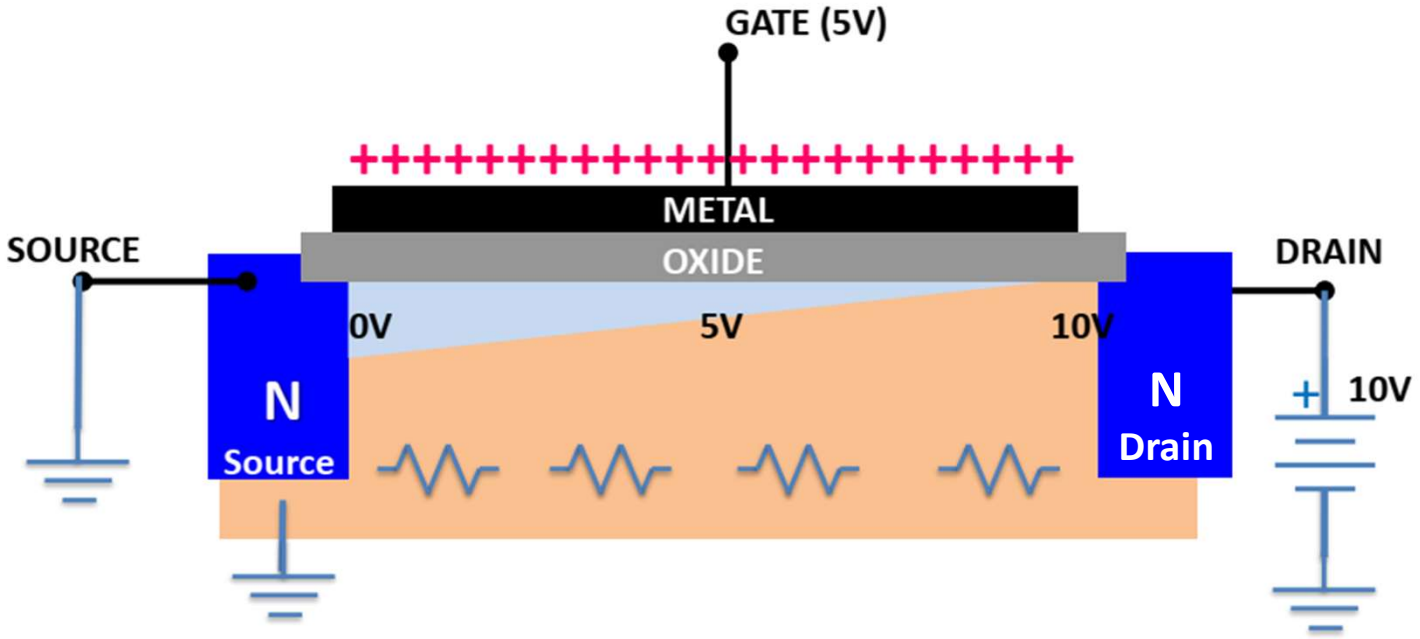
- We have a gap. If the voltage of the bulk material is higher than the gate, then electrons won't want to come to the top. No inversion region.

Channel Pinch-Off



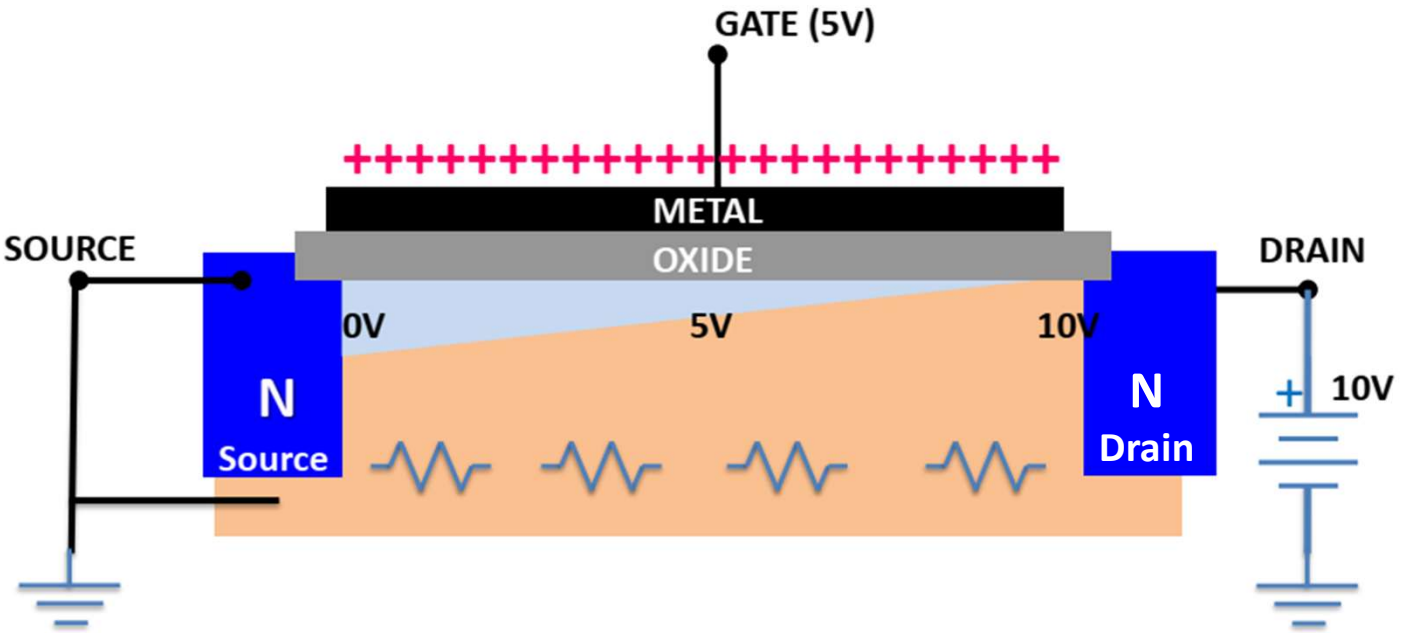
- If the inversion region disappears, the p-n junction returns. The bulk goes back to zero volts (the drain is detached). The inversion region then re-appears and current flows again. When we get these sort of on/off behaviours, in practice we hit an equilibrium between the on/off stages and we get a stable current value. This is the saturation region. The current is ideally stuck at the maximum value that allows an inversion region everywhere.

Channel Pinch-Off



- The equilibrium state is reached when current × (resistance of the inversion region) > (gate voltage - bulk voltage - V_T).
- Current × (resistance of the inversion region) is the source-drain voltage, V_{DS}.

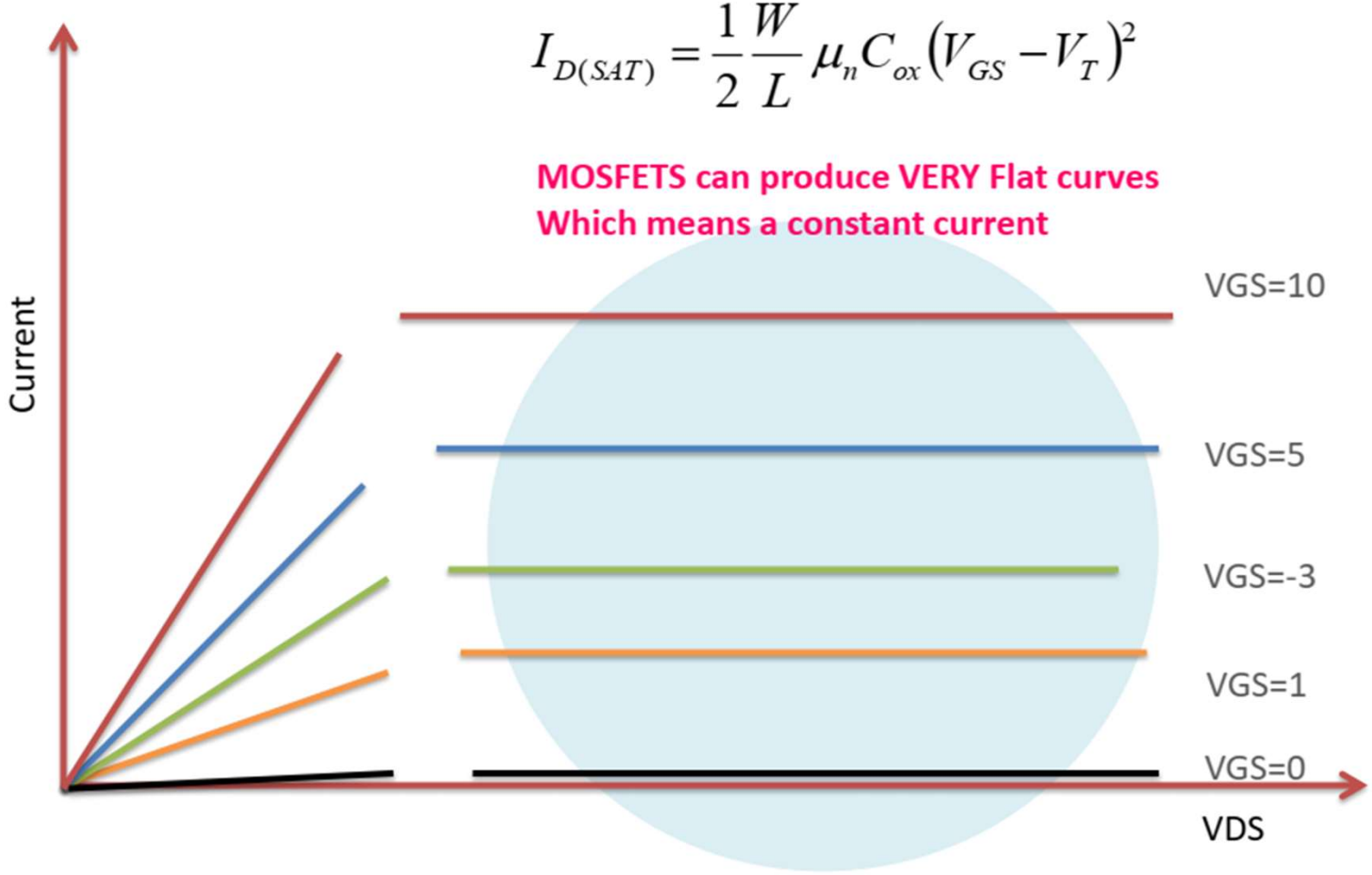
Operation Voltages of MOSFETs



- For simplicity, the bulk is nearly always connected to the source, so now we can say that when
  - $V_{GS} > V_T$: an inversion region forms;
  - $0 < V_{DS} < V_{GS} - V_T$: a current flows in the inversion region;
  - $V_{DS} = V_{GS} - V_T$: we hit the maximum current that can flow;
  - $V_{DS} > V_{GS} – V_T$: no more current should ideally flow.

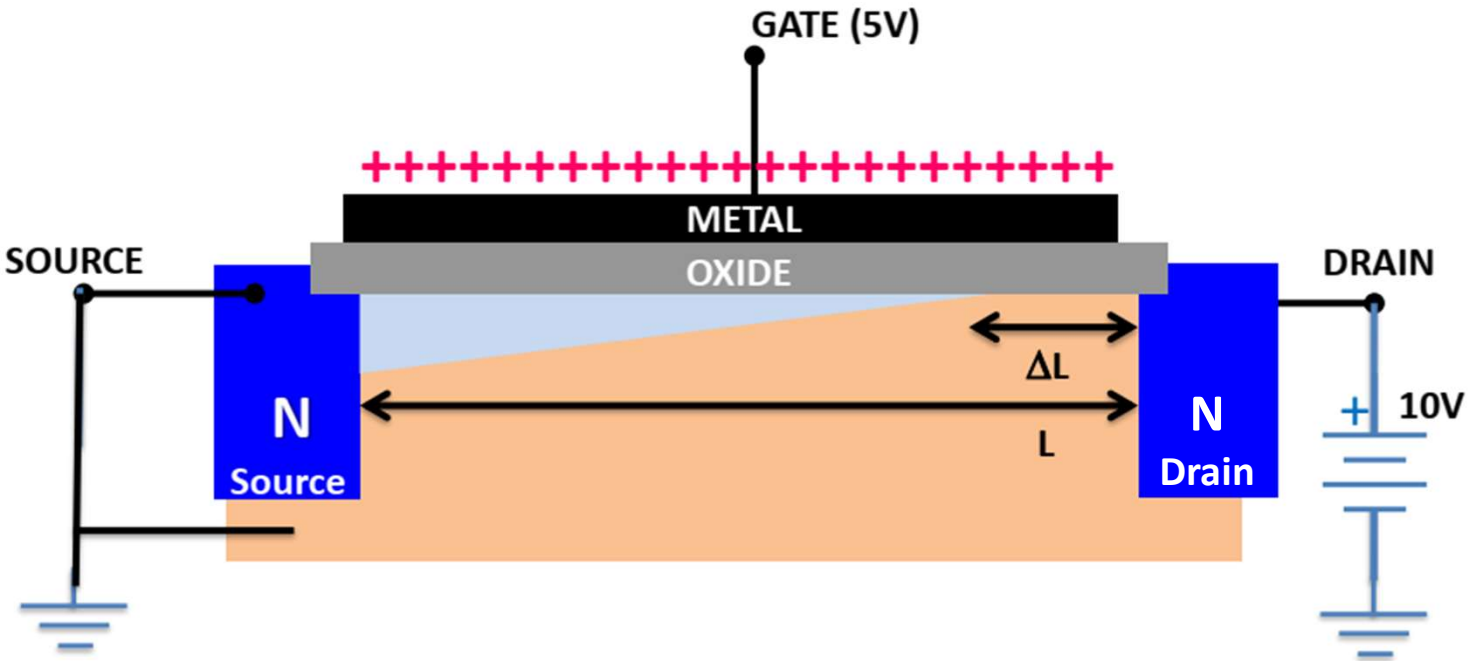
Saturation Region

$$I_{D(SAT)} = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2$$



You can get the $I_{D(SAT)}$ equation by letting $V_{DS} = (V_{GS} - V_T)$.

Channel Length Modulation

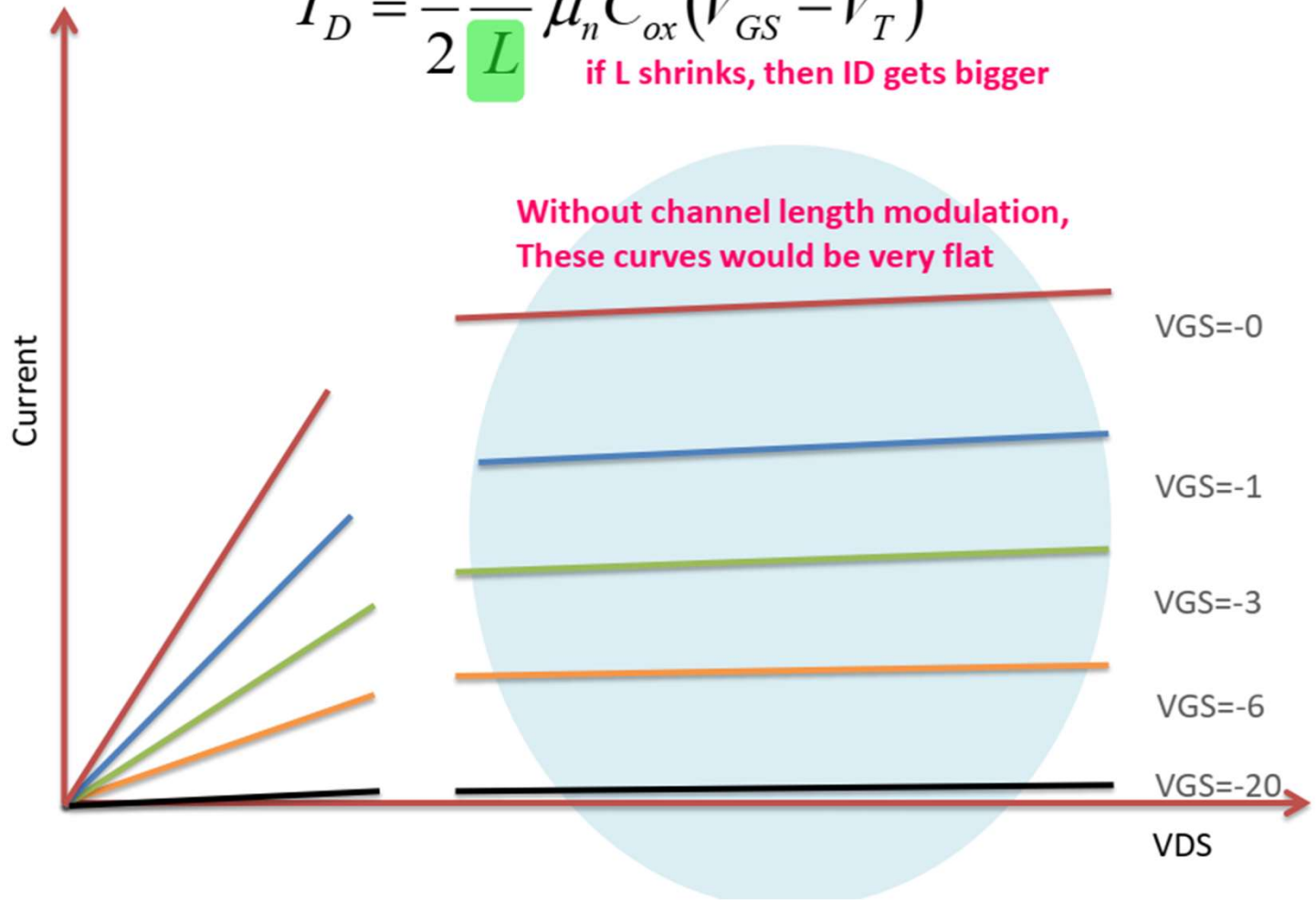


- Effectively as we increase V_{DS} in the saturation region, the channel gets smaller and the gap in between is filled with a depletion region.
- The effective length of the channel becomes (original length - the gap).
- A shorter channel is less resistive ($R = \rho L/A$) so that means more current can flow.

Channel Length Modulation

$$I_D = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2$$

if L shrinks, then ID gets bigger



How do We Avoid it?

- Bigger devices, that make a change in L less of an issue. For example,

- For ΔL = 1 nm,
- L_1 = 50 nm (device 1)
- L_2 = 500 nm (device 2)

- $(L_1 - \Delta L)/L_1$ = 49/50 = 98 % of original value.
- $(L_2 - \Delta L)/L_2$ = 499/500 = 99.8 % of original value.

- There are also other ways being developed in the industry to make this effect less of an issue.

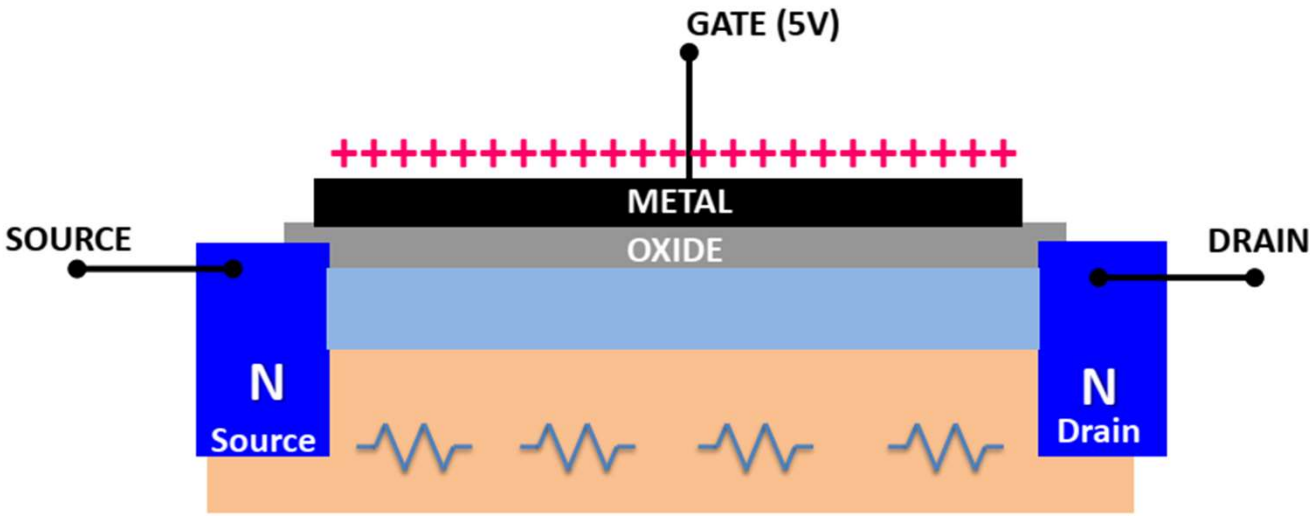
Key Equations for MOSFETs

- $I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$
- $I_{D(sat)} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$
- $I_D = I_S$
- $I_G = 0$

- So this comes from the device physics, and different transistors will have different values, but the "shape" of the equation will remain the same for MOSFETs.

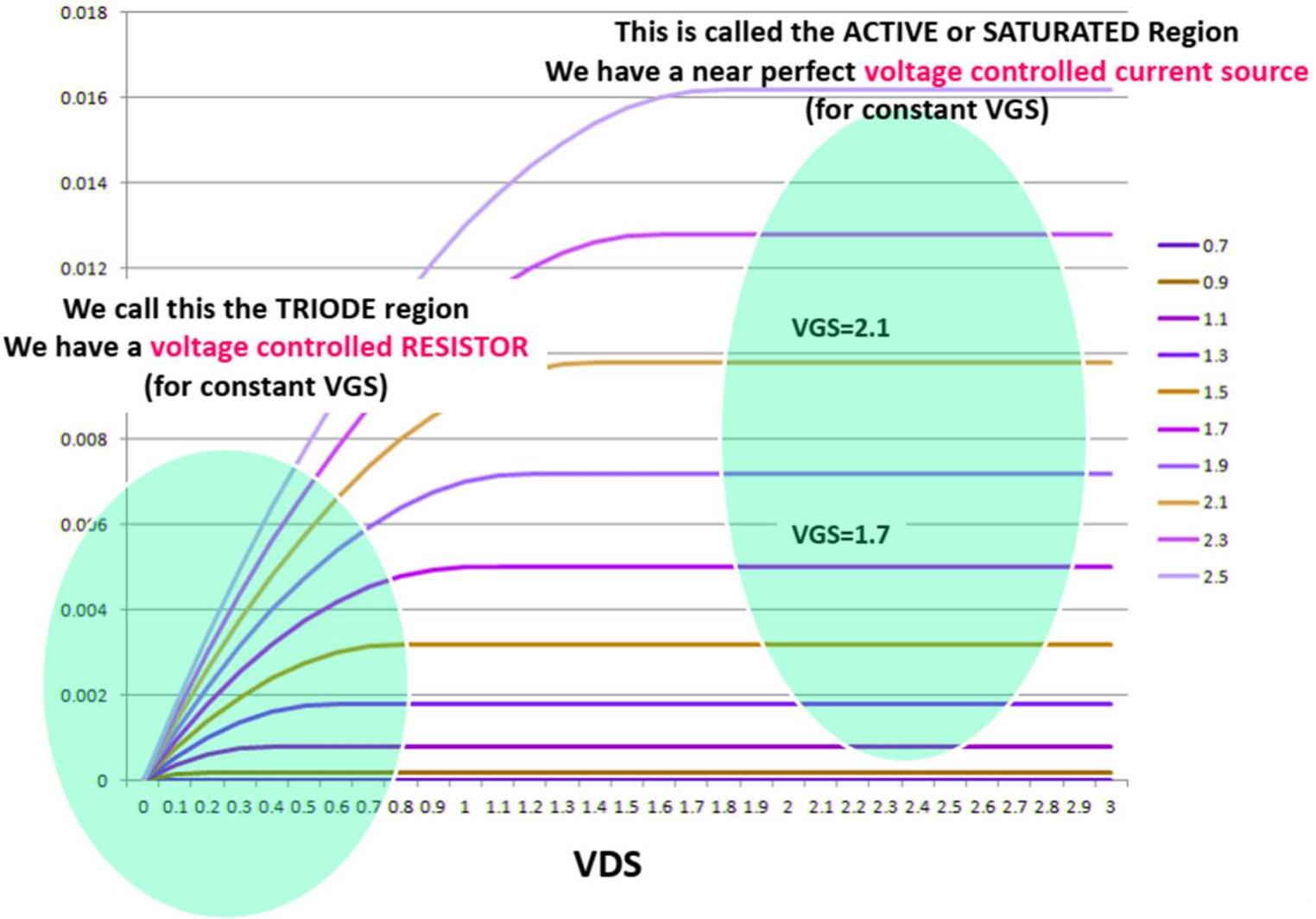
Key Equations for MOSFETs

$$I_G = 0 \qquad I_D = I_S$$

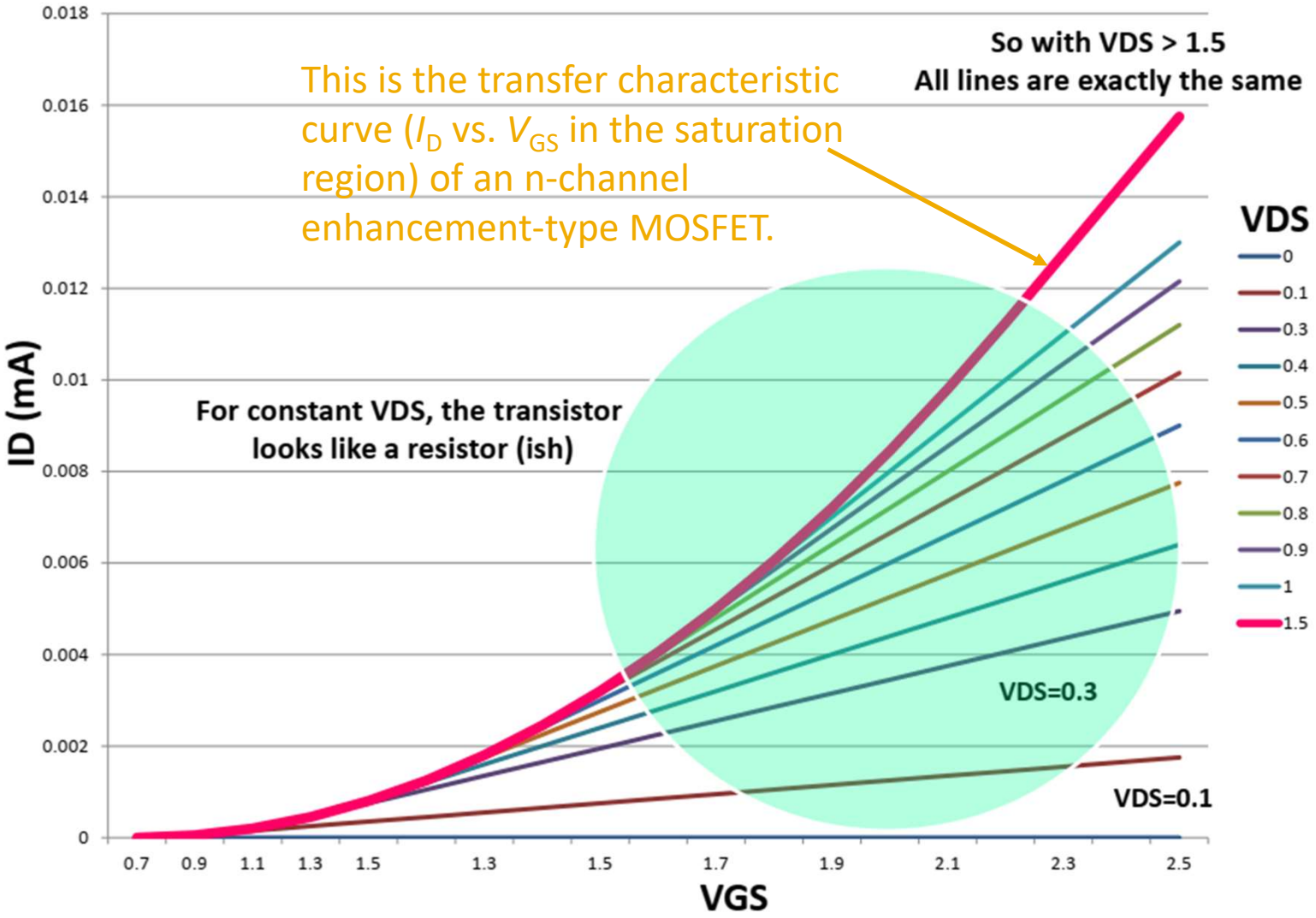


- The gate oxide is a good insulator. It blocks any current flowing from the gate to either SOURCE or DRAIN.
- It also means that any current entering from the SOURCE must go to the DRAIN.

Plotting Key MOSFET Equations

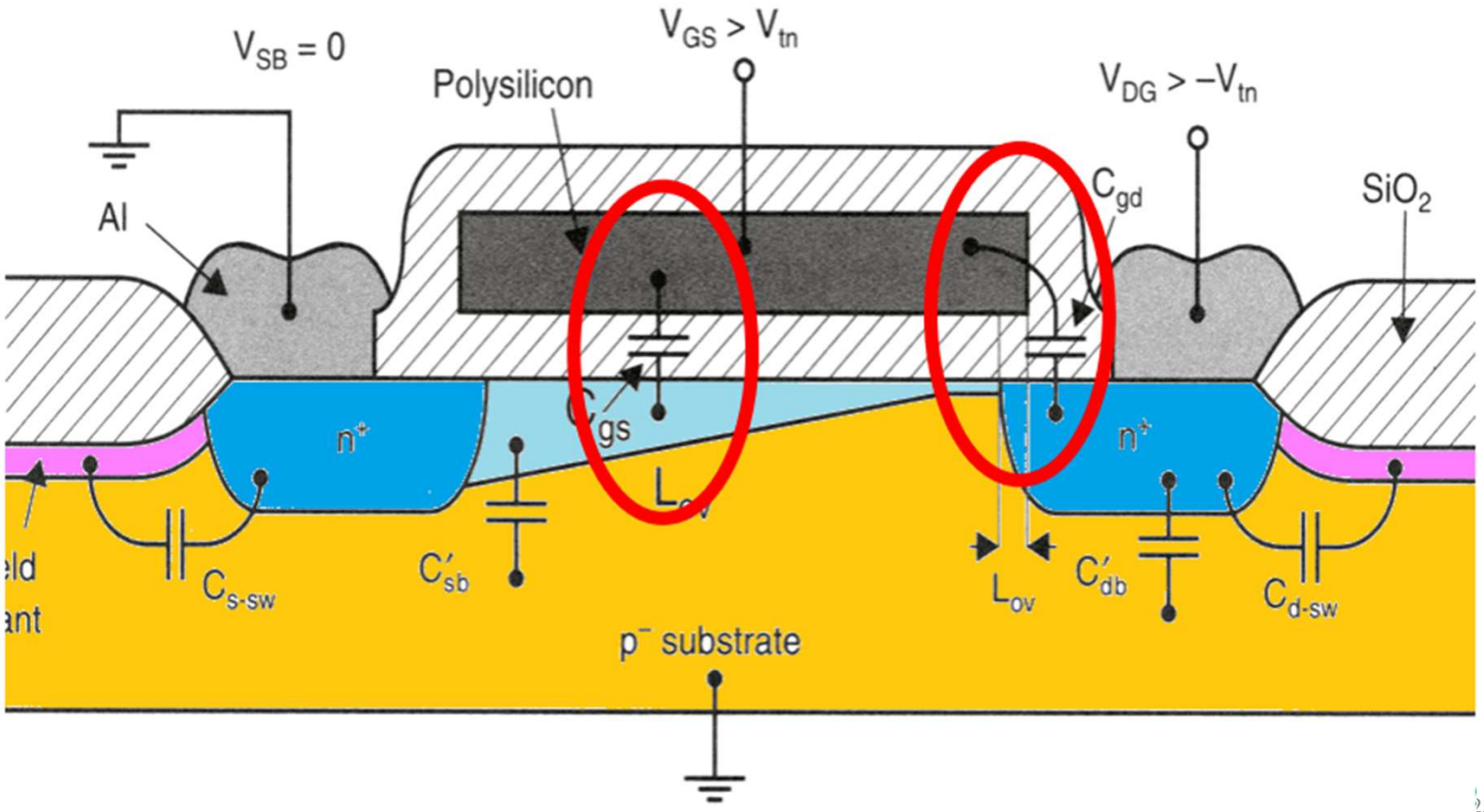


Plotting Key MOSFET Equations (I_D vs. V_{GS})

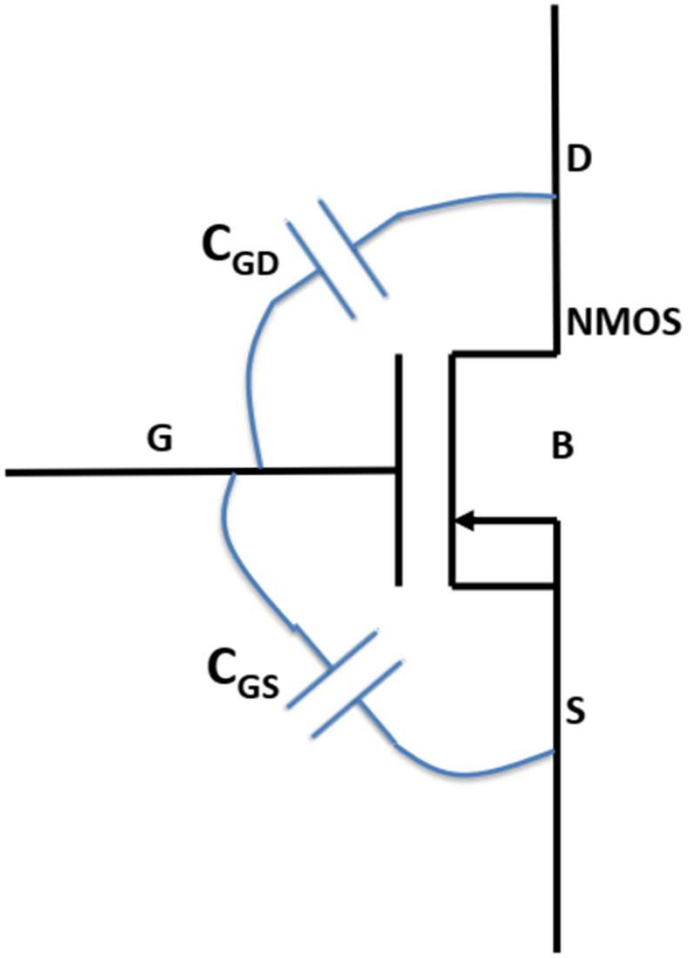


Parasitic Components in MOSFETs

Capacitors form when charged areas are separated by an insulator. Any conducting region overlapping with another is potentially a capacitor.



Parasitic Components in MOSFETs



- There are other parasitic capacitors, but these are the two most important ones. We won't initially worry about them, but we will have to come back to them.
- They do not cause a problem when we are changing things slowly as they charge/discharge rapidly (compared to how fast things change).
- But when we are doing things 100's and 1000 of million times / sec, it is these parasitic capacitances that limit the performance.
- C_{GS} is the biggest in size but C_{GD} has the biggest impact.

Key Points to Remember

- In practice, we can assume NO CURRENT flows into the gate terminal.
- In the saturation region, the curves are VERY FLAT.
- When the device is turned off, they let VERY LITTLE current through.
- The key equation for everything is (when $V_{GS} > V_T$):

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

- And in the saturation region, i.e., when $V_{DS} > (V_{GS} - V_T)$:

$$I_{D(sat)} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

In Practice

- If you are using transistors in a lab, the equations usually are given in the form of curves and you just read the values from the datasheet.
- The equations are scary but if you use them in the most common ways, then they are really easy to understand. All the equations do will help you explain why things are changing.
- If you design computer chips for Intel or Analog Devices, you can choose the key parameters *W*/*L* to change their behaviour to what you need.
- NOTE: The transistor equation here is a very simple equation and the real equations can fill many A4 pages with thousands of parameters. That's simply too complex for humans to get any meaningful info from. Excellent for computers though. 😁

NMOS & PMOS

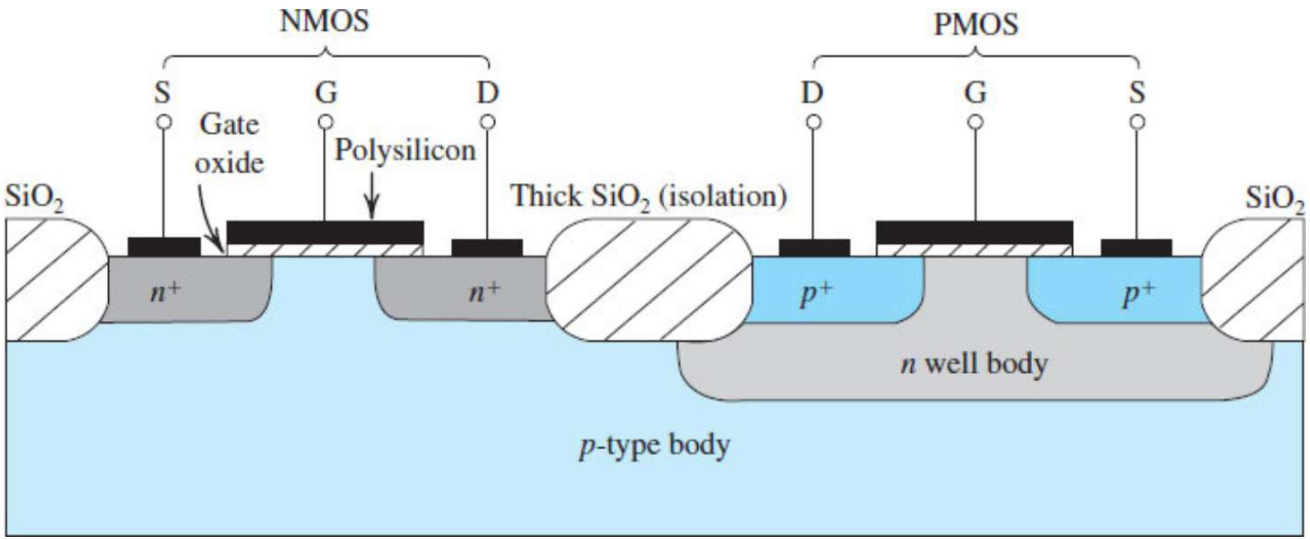
- Based on the majority charge carriers in the channel region, MOSFETs come in two versions:
  - NMOS (n-channel);
  - PMOS (p-channel).

- NMOS and PMOS are complementary devices.

- For enhancement-type MOSFETs:
  - NMOS need the gate voltage to be HIGHER than source to work.
  - PMOS need the gate voltage to be LOWER than source to work.

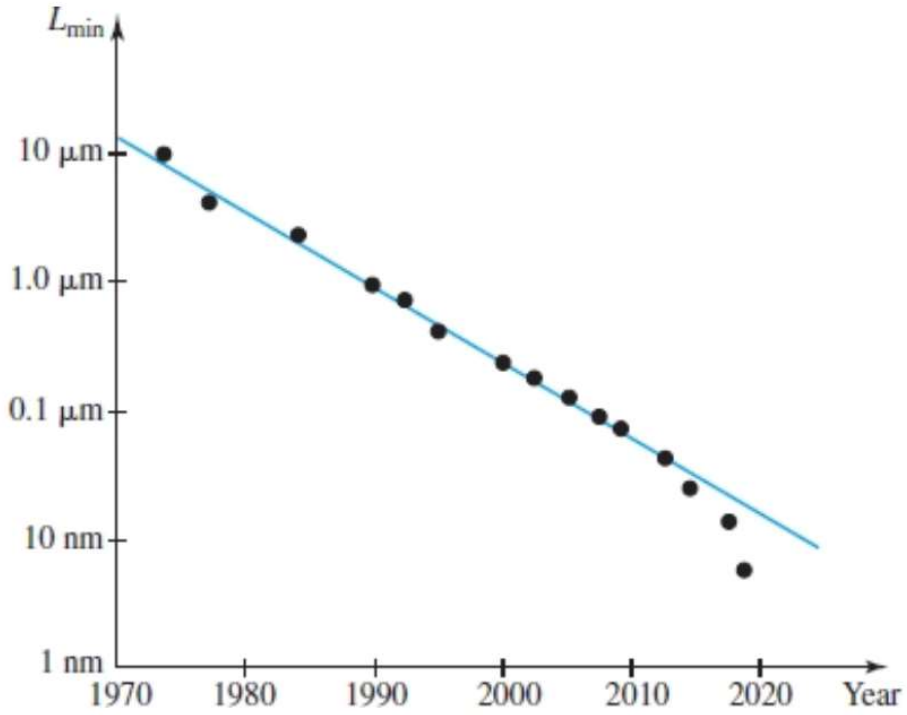
CMOS

- Effective logic circuits can be fabricated by putting n-channel and p-channel MOSFETs onto the same substrate;
- This configuration is called complementary MOSFET arrangement (CMOS) which has significant applications in modern digital electronics.



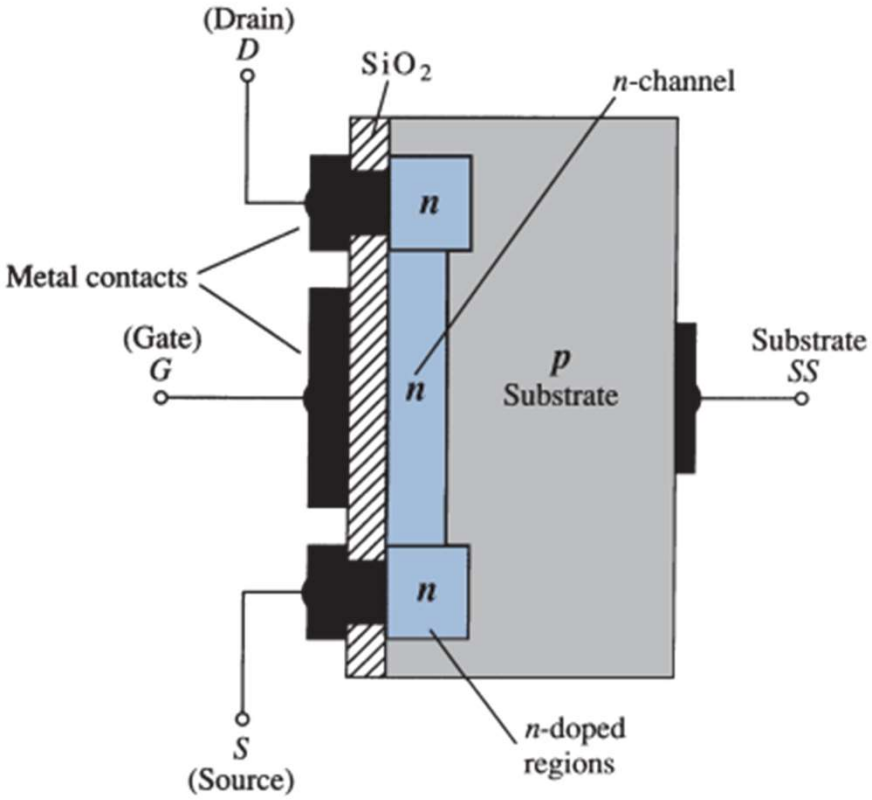
Moore's Law

- Advances in CMOS fabrication technology have led to the reduction in minimum channel length in MOSFETs by 30% every 2 – 3 years;
- This means that one can assemble twice as many transistors on a silicon chip of the same area. This is the famous Moore's law.



Enhancement- & Depletion-Type MOSFETs

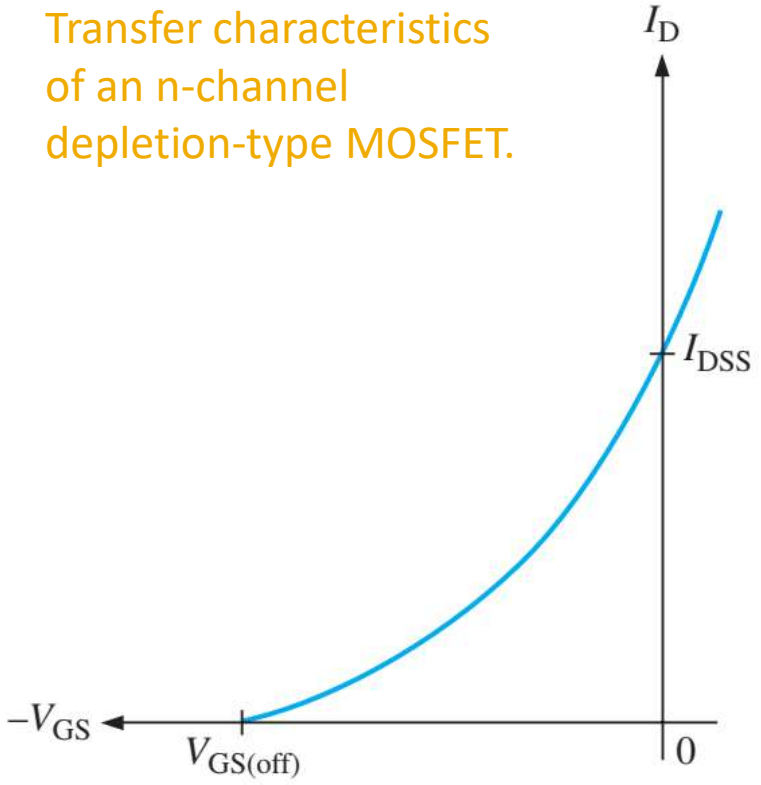
- In all the MOSFETs we discussed so far, the conduction channel is induced by the gate voltage (no channel when V_{GS} = 0). We call these devices enhancement-type MOSFETs.
- There is another type of MOSFET devices where a channel exists under V_{GS} = 0 (it is realised through doping the substrate). These devices are called depletion-type MOSFETs.



Depletion-Type MOSFETs

- Depletion-type MOSFETs are 'normally on' devices (they are conducting when $V_{GS} = 0$);
- Depletion-type MOSFETs can operate in either the depletion-mode or the enhancement-mode (gate voltage may be either positive or negative).

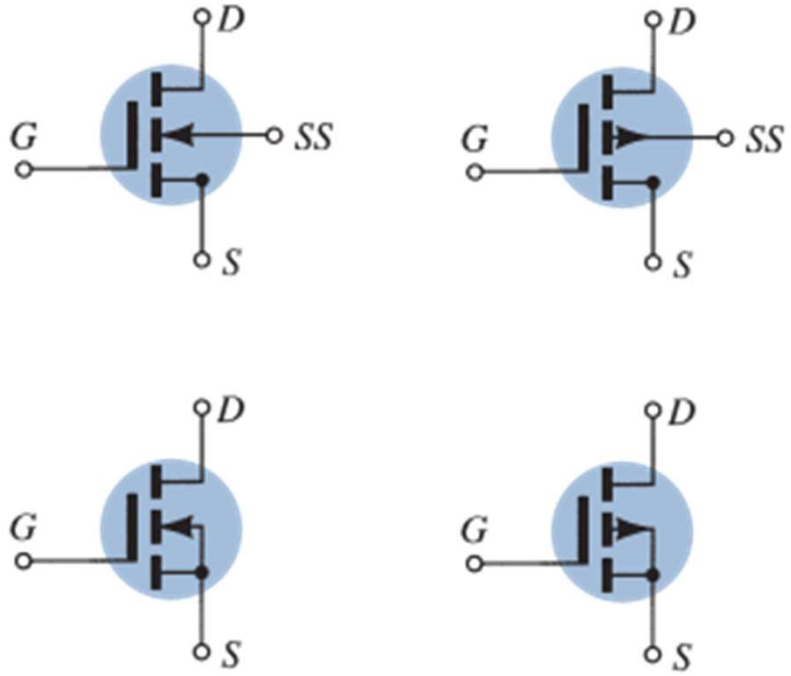
Transfer characteristics of an n-channel depletion-type MOSFET.



Watch Out! It may have already occurred to you. MOSFET equations discussed previously do NOT work for depletion-type MOSFETs.

Circuit Symbols for Enhancement-Type MOSFETs

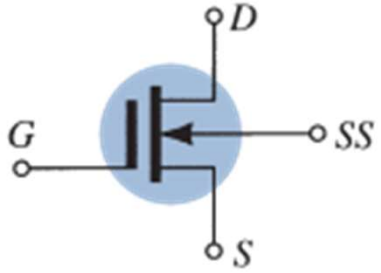
n-channel p-channel

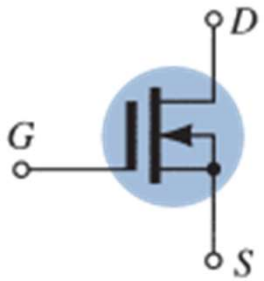


- Pay attention to the directions of the arrows in the symbols. The direction of the arrow represents the forward bias direction of a p-n junction in the FET.

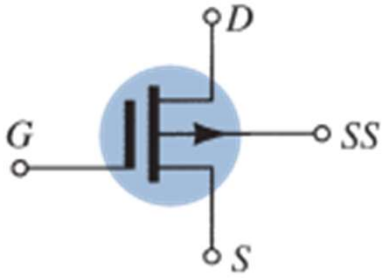
Circuit Symbols for Depletion-Type MOSFETs

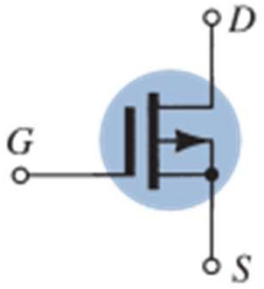
n-channel





p-channel



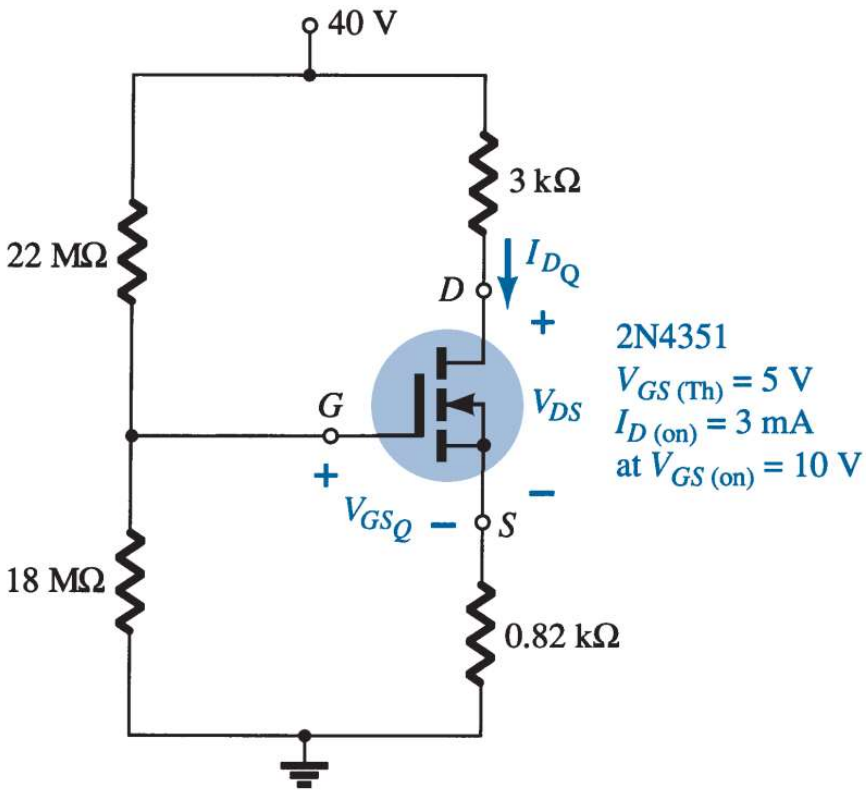


- Pay attention to the difference between enhancement-type and depletion-type MOSFETs. The channels are represented by dashed lines in enhancement-type devices but by solid lines in depletion-type devices.

Example: MOSFET Equations

- Find I_{DQ}, V_{DS} and V_{GSQ}.

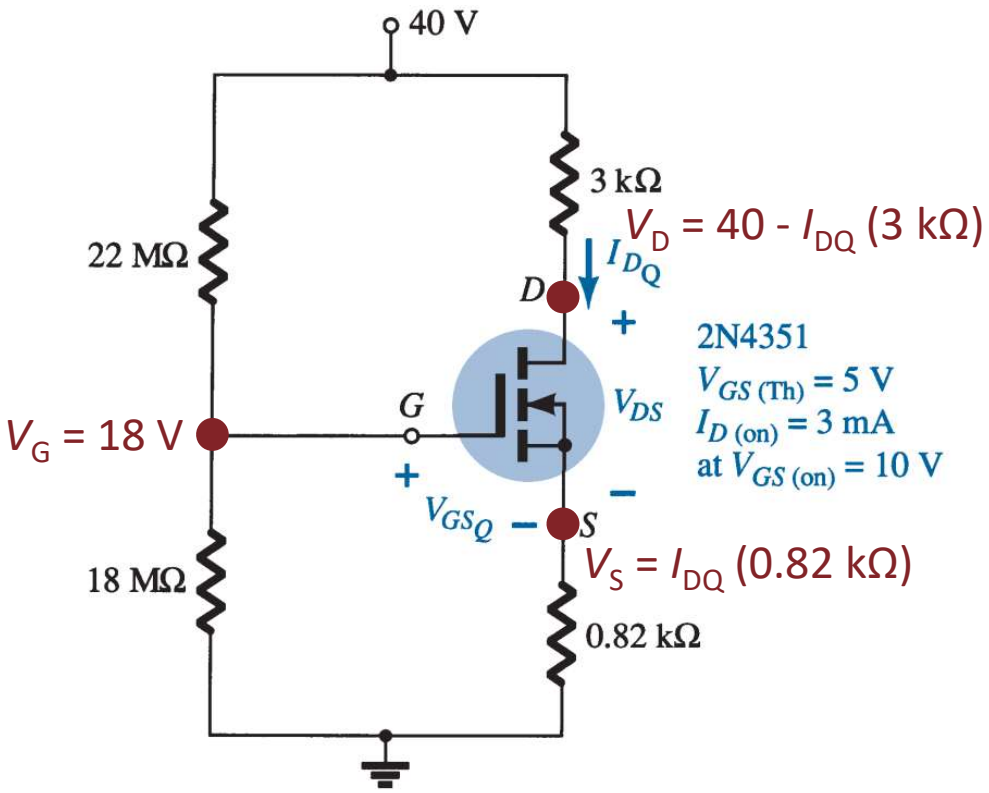
- The symbol "Q" refers to the quiescent (operating) point or simply the Q point. This is the DC operating point of the transistor (to be discussed more in the coming weeks).



Example: MOSFET Equations

- $I_{\mathrm{D}} = K(V_{\mathrm{GS}} - V_{\mathrm{T}})^2$ in which $K = \frac{1}{2}\left(\frac{W}{L}\right)\mu_{\mathrm{n}}C_{\mathrm{ox}}$;
- Insert the information from the data sheet,

$$K = \frac{I_{\mathrm{D}}}{(V_{\mathrm{GS}} - V_{\mathrm{T}})^2} = 1.2 \times 10^{-4}\ \mathrm{A/V^2}$$



Example: MOSFET Equations

- We can build an equation on

$$I_{\mathrm{DQ}} = K\left(18 - 820I_{\mathrm{DQ}} - 5\right)^2$$

- Solving the equation gives:

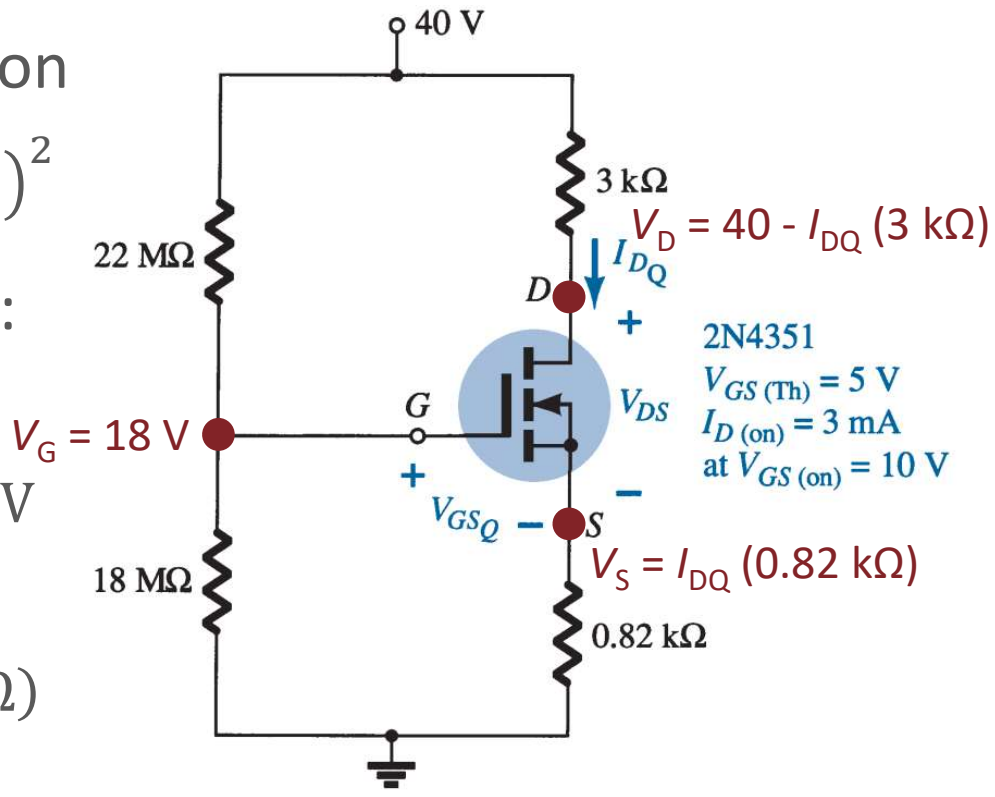
$$I_{\mathrm{DQ}} = 6.73\ \mathrm{mV}$$

$$V_{\mathrm{S}} = I_{\mathrm{DQ}}(0.82\ \mathrm{k\Omega}) = 5.5\ \mathrm{V}$$

$$V_{\mathrm{GS}} = V_{\mathrm{G}} - V_{\mathrm{S}} = 12.5\ \mathrm{V}$$

$$V_{\mathrm{DS}} = 40 - V_{\mathrm{S}} - I_{\mathrm{DQ}}(3\ \mathrm{k\Omega})$$

$$= 14.3\ \mathrm{V}$$



One should double check and make sure that the MOSFET is in the saturation region. How can one do it?