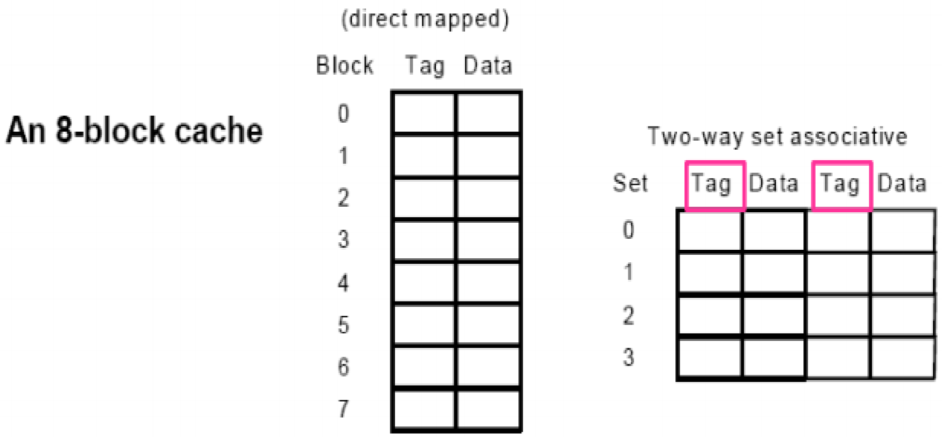
DSD HW3

Speaker: Alex

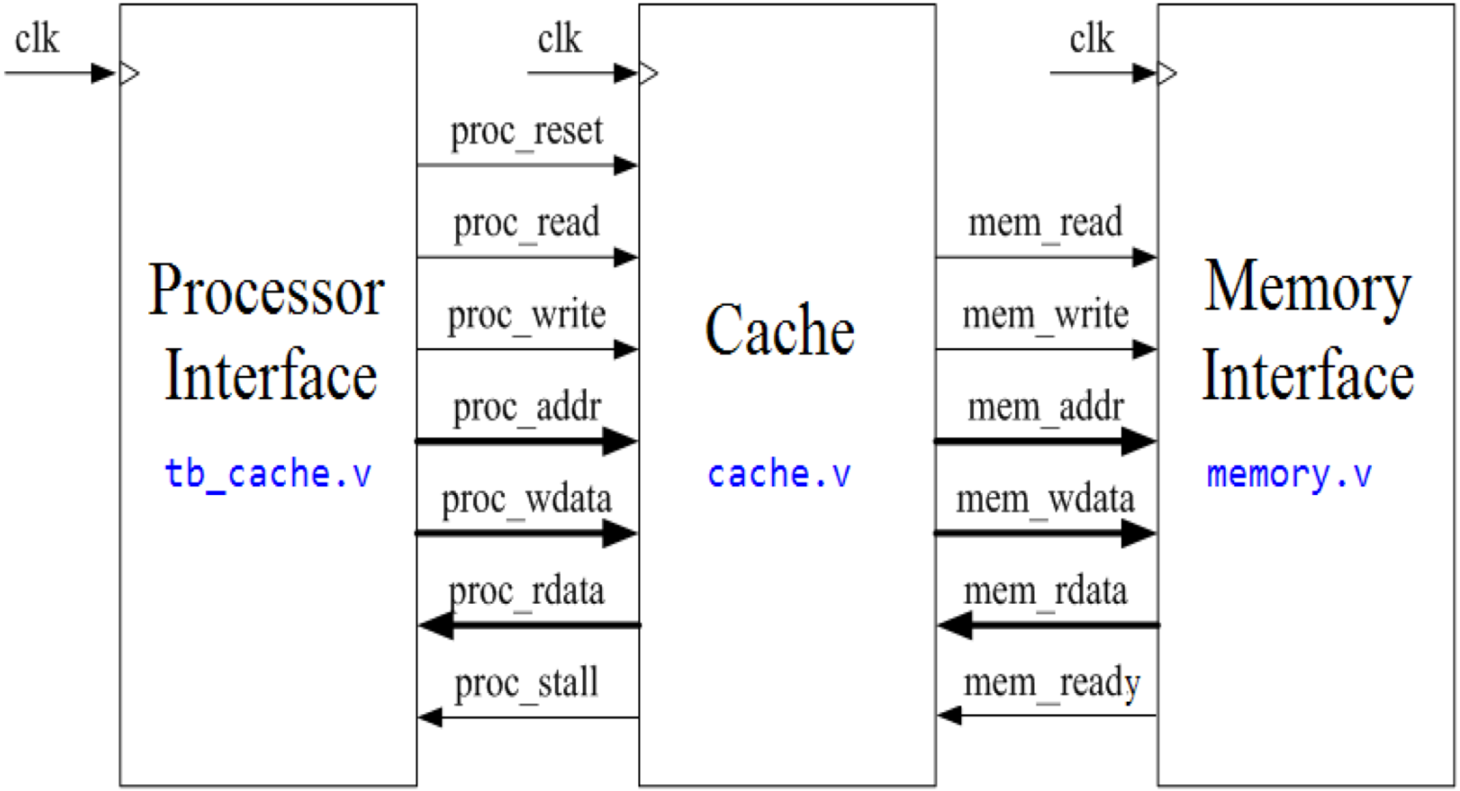
Date: 2025/05/01

Cache Specification

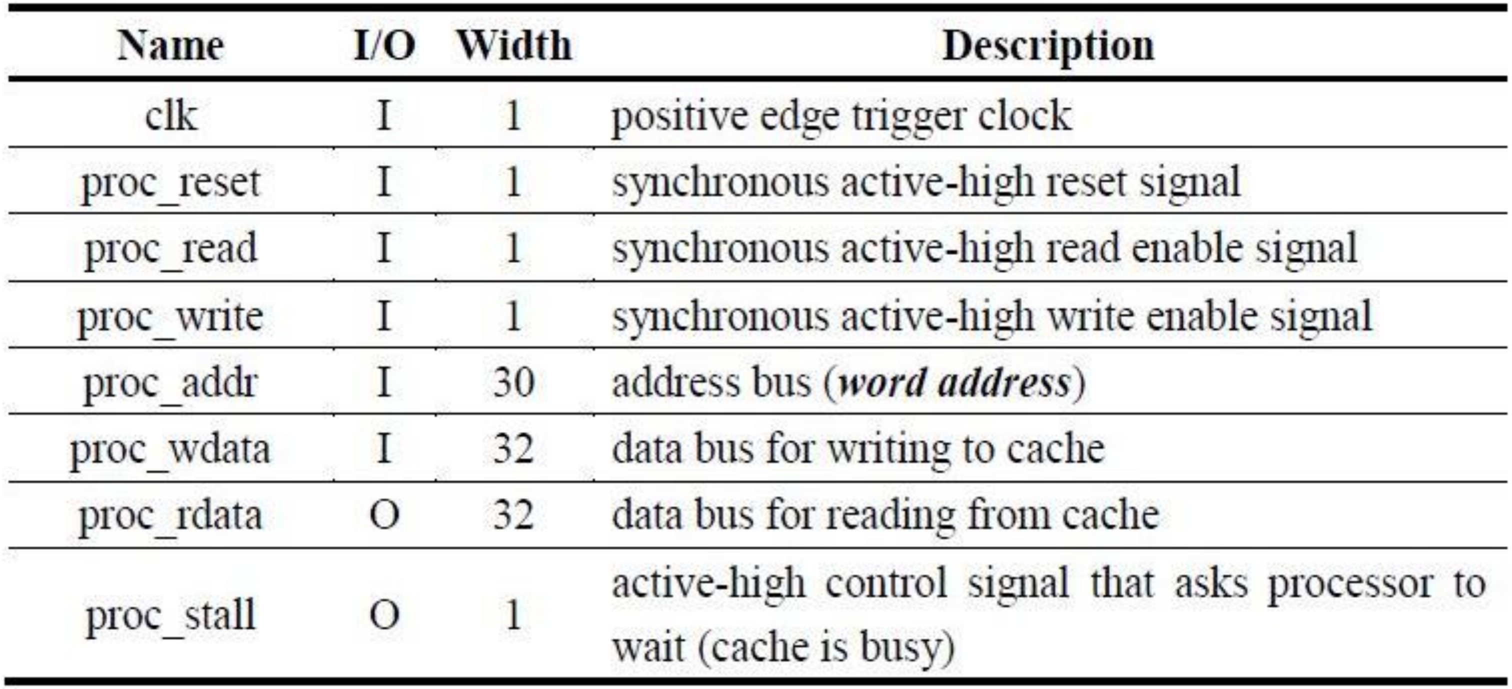
- Implement two architectures
  - **Direct-mapped**
  - **Two-way associative**
- **8 blocks with 4 words in each block**
- Write-through & write back are both available write policies
- Least Recently Used (LRU) & Least Frequently Used (LFU) are both available placement policies



I/O Interface of The Cache Unit

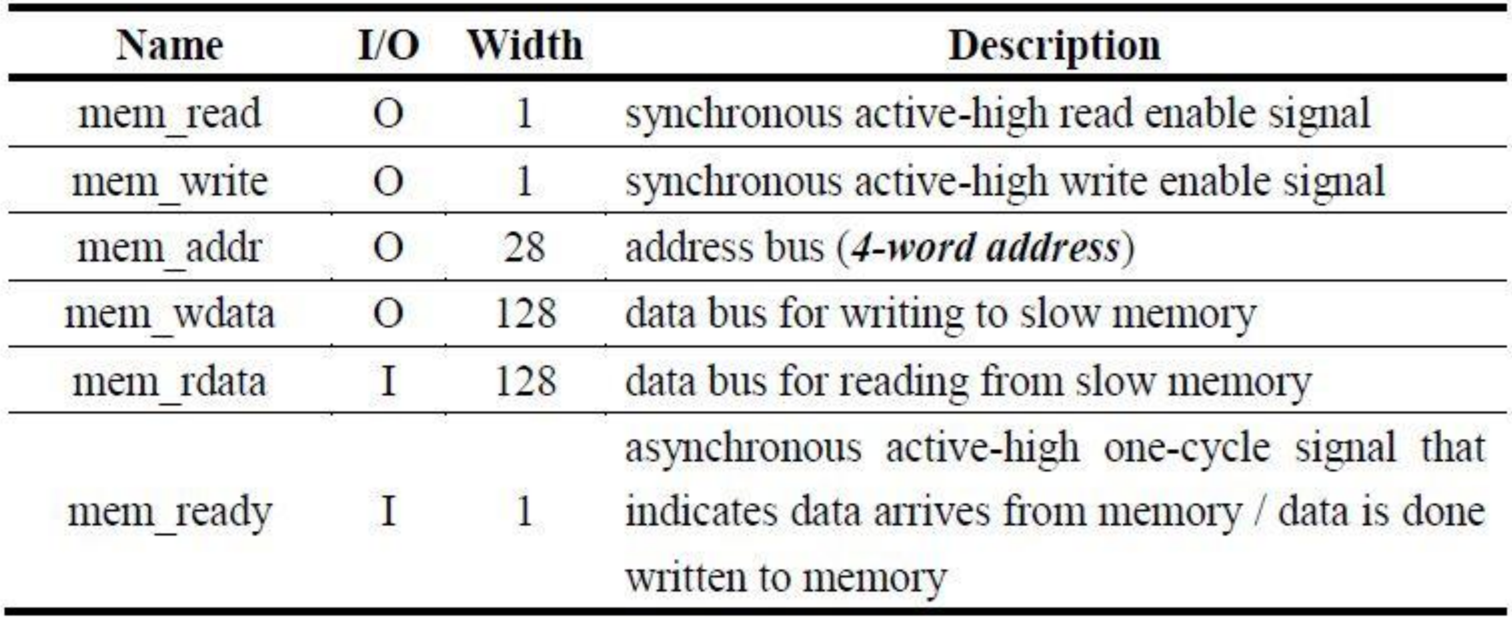


I/O Specification of The Processor Interface



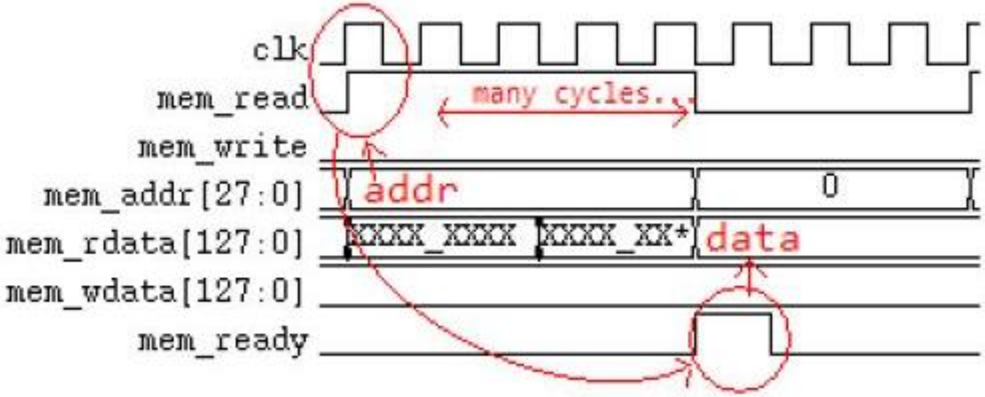
Name	I/O	Width	Description
clk	I	1	positive edge trigger clock
proc_reset	I	1	synchronous active-high reset signal
proc_read	I	1	synchronous active-high read enable signal
proc_write	I	1	synchronous active-high write enable signal
proc_addr	I	30	address bus (***word address***)
proc_wdata	I	32	data bus for writing to cache
proc_rdata	O	32	data bus for reading from cache
proc_stall	O	1	active-high control signal that asks processor to wait (cache is busy)

I/O Specification of The Memory Interface

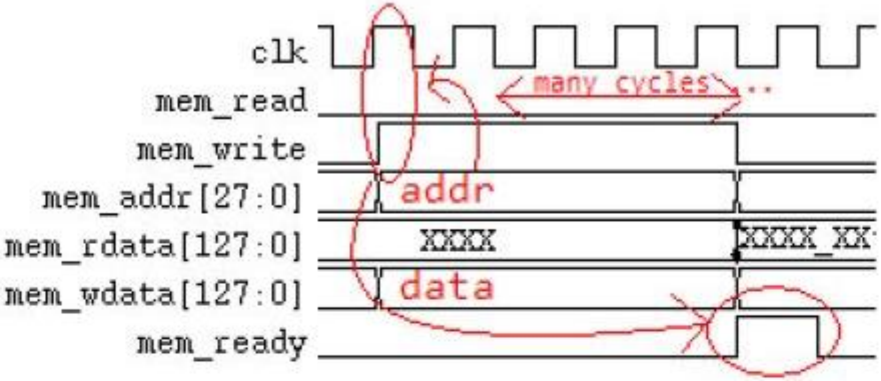


Name	I/O	Width	Description
mem_read	O	1	synchronous active-high read enable signal
mem_write	O	1	synchronous active-high write enable signal
mem_addr	O	28	address bus (***4-word address***)
mem_wdata	O	128	data bus for writing to slow memory
mem_rdata	I	128	data bus for reading from slow memory
mem_ready	I	1	asynchronous active-high one-cycle signal that indicates data arrives from memory / data is done written to memory

Timing Diagram of The Memory Interface



(a) Read operation.



(b) Write operation.

Stall

- When the cache needs to access data from the memory and then wait for several cycles, the *proc_stall* signal should be set high to stall the processor.
- Two possible cases where a stall is necessary
  - **Read miss** in both write-through and write-back caches
  - **Write hit** in only write through caches

Cache Design (35% Each)

- **Evaluation is only based on the given testbench “tb_cache.v”**
- **RTL Simulation (20%)**
- **Synthesis**
  - No latches
  - No negative endpoint slack
  - No timing violations
- **Gate-level Simulation (15%)**
  - Get the points if you pass the gate-level simulation without timing violations or negative endpoint slacks
  - Still need to pass the RTL simulation and no inferred latches
- **Performance is not part of the grading criteria**
  - Specify your cycle time in the report and cycle.txt
  - Still encouraged to optimize it for your final project

Report (30%)

- **Cycle time to pass the post-synthesis simulation**
  - cache_syn.sdc
  - tb_cache.v
  - Cycle time should be reported in “**cycle.txt**” too
- **General Specification**
  - Write policy
  - Placement Policy
- **Finite State Machine**
- **Performance**
  - Read/Write miss rate
  - Execution cycles
  - Stalled cycles
- **Comparison of the two architectures and their results**

Bonus (Up to 5%)

- **If your cache units are implemented with other skills that enhance the performance significantly**
- **Describe your methods or architectures in detail in the report**
- **Regulations**
  - direct-mapped & two-way associative
  - 8 blocks with 4 words each

Submission

- *DSD_HW3_學號/*
    - *report.pdf*
    - *cycle.txt*
    - *rtl/*
        - *cache_dm.v*
        - *cache_2way.v*
    - *syn/*
        - *cache_dm_syn.v*
        - *cache_dm_syn.sdf*
        - *cache_dm_syn.ddc*
        - *cache_2way_syn.v*
        - *cache_2way_syn.sdf*
        - *cache_2way_syn.ddc*

- Compress all the files into one **ZIP** file
    - File name: DSD_ HW3 _學號.zip
- Deadline: 2025/05/14 23:59
- Late submission penalty: 20% off per day