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Lab 1: Logic Gates and Multiplexer_4_1

Today we will get introduced to Vivado and the general flow of designing digital circuits with VHDL. We will see how to create a Vivado project, how to create VHDL entities, and how to test the entities in simulation.

14:15-14:35: Demonstration 1 – AND-gate

1. Introduction to Vivado
2. Creation of a project
3. Creation of our first VHDL entity: The AND-gate
4. Testing of the entity in behavioral simulation

a	b	o
0	0	0
0	1	0
1	0	0
1	1	1

Table 1: AND-gate truth table

14:35-15:00: Task 1 – OR-gate and NOT-gate

1. In the same project, create a new file ‘or_gate.vhd’
   a. Two *STD_LOGIC* inputs *a* and *b*, one *STD_LOGIC* output *o*
2. Write VHDL such that the relationship between inputs *a* and *b* and output *o* follows the truth table in table 2
3. Test your design in behavioral simulation
4. Repeat for ‘not_gate.vhd’, truth table in table 3

a	b	o
0	0	0
0	1	1
1	0	1
1	1	1

Table 2: OR-gate truth table

a	o
0	1
1	0

Table 3: NOT-gate truth table

15:00-15:05: Break

15:05-15:15: Demonstration 2 – Vivado Block Design

1. Creation of new block design
2. Block design of truth table in table 4
3. Behavioral simulation of block design

a	b	c	o
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 4

15:15-15:45: Task 2 – Multiplexer_4_1

1. Create a new block design ‘multiplexer_4_1’
2. Using only AND-gates, OR-gates, and NOT-gates, implement a 4x1 multiplexer, figure 1 and table 5, in block design
3. Verify the behavior in simulation
4. Hint will be given if required

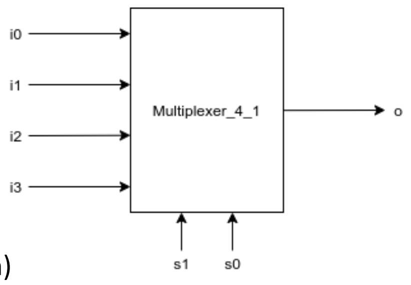

Figure 1: 4x1 multiplexer

s1	s0	o
0	0	i0
0	1	i1
1	0	i2
1	1	i3

Table 5: 4x1 multiplexer truth table

Bonus Task

- Implement a 2x1 multiplexer in a new VHDL file (that is, write the multiplexer fully as a new VHDL entity and not in block design)
- Can you make it as *generic* as possible, so the size of the multiplexer is easily changeable? 2x1, 4x1, 4x2, etc.
  Think about which parameters you would need in order to make the multiplexer generic in size.

Credit to original Author Frederik Falk Nyboe ffn@mmmi.sdu.dk