Emad Samuel Malki Ebeid
esme@sdu.dk
DIG 2026

SDU
Digital and High-Frequency Electronics Section

Assignment 1: Design a digital clock

Aim

To develop skill in VHDL programming and functional simulation by designing, implementing, and testing both sequential and concurrent digital circuits.

Task: VHDL Design and Simulation

1. Digital Clock Design

Create a VHDL-based digital clock capable of displaying **seconds** and **minutes**.

The design should include appropriate sequential logic (counters, clock dividers, etc.) and any required concurrent processes.

2. Simulation

Perform a functional simulation of the entire clock circuit.

The simulation must clearly demonstrate that the clock is **counting time correctly for** 2 minutes (120 clocks).

3. Documentation Requirements

Prepare a brief report summarizing your work. The report must include:

- **Descriptions of the components** used in the design (e.g., counters, dividers, logic gates, etc.).
- **An explanation of how the digital clock operates**, including functional timing behavior.
- **Evidence of testing and validation**, supported by simulation waveforms.

To support your explanations:

- Include **relevant code pieces**.
- Include **screenshots** of simulation results.
- Ensure that **all circuit outputs** (seconds and minutes) are visible in the simulation waveforms.

Bonus Task (Optional)

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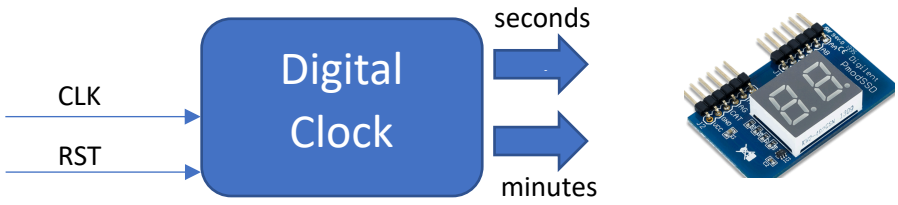
For additional credit, format the seconds and minutes outputs so they correspond to the representation used by a **7-segment display** (e.g., BCD encoding or segment-level output) that is provided with the FPGA kit.



Submission Details

- **Submission platform:** Itslearning → Assignments
- **File format:** PDF
- **Deadline: 16/03/2025, before 23:59**
- **Page limit:** Maximum **3 pages**
- **Minimum font size: 10 pt**