ABSTRACT

The main purpose of this project is to design high performance gate drive circuits for high speed switching applications. It is an informative collection of “one-stop-solution” for most common design challenges. Thus it should be of interest to power electronics engineers at all levels of experience. The most popular circuit solutions and their performance are analyzed, including the effect of parasitic components, transient and extreme operating conditions. Design procedure for ground referenced and high side gate drive circuits should also be area of interest for design.

The discussion starting with an overview of MOSFET technology and switching operation and different types power MOSFET. After that we will discuss on gate driver circuit . Finally last low-loss and high speed digital gate driver circuit design and challenges has been discussed in detail.

HISIM_HV PDK is used for designing the gate driver circuit and this circuit is designed for LDMOS power MOSFET which has high switching frequency.

Contents

LIST OF FIGURES

MOTIVATION

As the fundamental building elements, power semiconductor switching devices are the most important components in a power electronic system. Like valves in a vein, they control the direction of electrical power flow within the system. Through the intense technology evolution, power semiconductor devices like power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), IGBTs (Insulated Gate Bipolar Transistors) have been developed.
In order to trigger power MOSFET a large gate voltage (20V for this work) is required.

Subsequently, we need some circuit to generate this high voltage (20V) on-chip. The charge pump circuit, which is basically found in RF circuit design, could be the on-chip solution to this problem. In this thesis, a compact charge pump circuit has been designed in order to serve this purpose. The transition across voltage domains from low to high voltages is performed by a DC-DC converter such as a charge pump. A charge pump is a switched capacitor circuit that relies on the charge redistribution principle to create voltage levels different from the input voltage. A charge pump output can be higher, lower, or of opposite polarity to the input voltage. In our context, we are mainly interested in charge pump architectures that step up the input voltage. The charge pump module is designed through switches and capacitors only; it would be efficiently integrable with the gate driver module.

Power MOSFET will have some rated current it can offer to flow through it without any loss in load as well as in channel of power MOSFET. and also, there will be some rated current for the load, it means the maximum current that load can withstand. So, we need to track the current that flows in the channel and the load and we do to put some circuit that can sense the current and it will take action if the current crosses the maximum value.

LITERATURE SURVEY

The use of electricity for everyday operations, such as charging laptops and smartphones, is often taken for granted; on the other hand, the principle of converting electricity for such mundane uses is not fully understood by consumers [1]. This act of transforming electrical energy into a different form is commonly known as electronic power conversion. By definition, electronic power conversion refers to transform one or more characteristics of an electric power system, essentially with minimal power losses. Conversion can be used to change the parameters of electric power, such as voltage, number of phases, or frequency.

Power electronics is a field of electrical engineering concerned with the processing of electrical power between several forms using converters. Power electronic converters are used in nearly all electrical devices that we use in our daily lives. Applications include computers, consumer electronics, transportation electronics, telecommunications equipment, medical equipment, industrial electronics, and many more.

The application requirements, efficiency, reliability, size, and cost are the most important requirements an engineer must consider when designing a converter. A common choice for the switching component used in the converter is a Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). Its advantages include voltage control, stable state preservation, and short switching times, justifying it as a prime candidate for power converters.

Switching power devices play an important role in power electronic applications. Silicon devices have been the most widely used semiconductor in power converter applications for decades. However, with the new requirements for the design of power converters, silicon devices (Si) have been upcoming to their physical limits.

The new material is not without its limitations. In the power converters, the switching components need to be turned completely on or off. Compared to their Si-counterparts, SiC MOSFETs require a higher control voltage for turning on to minimize conduction losses. They also require lower control voltage for turning them off to prevent them from accidentally entering a conductive state. This is caused by SiC MOSFETs possessing a lower threshold voltage than Si-devices, meaning that they start to conduct at rather low gate voltages.

1. INTRODUCTION

The focus of this topic is the gate drive requirements of the power MOSFET in various switch mode power conversion applications. It has the potential to revolutionize power electronics in much the same way silicon integrated circuits revolutionized computer systems; reducing power consumption, size, and cost of power electronic systems and enhancing their speed, portability, versatility, and efficiency, especially in high-voltage and high-temperature applications.

The practical usage of high-voltage MOSFETs has significantly increased in recent years due to their successful application in e.g. cellular wireless networks, consumer appliances, mobile computers or automotive electronics. This development became possible by advances in process technologies allowed the production of complex high-voltage circuits. For an efficient design such integrated high-voltage circuits, accurate compact models of high-voltage MOSFET are in strong demand.

Two major high-voltage MOSFET types, commonly used by the semiconductor industry, can be distinguished. The first type is a laterally-diffused asymmetric structure called LDMOS, and the second type is a symmetric structure with drift regions for high-voltage capability at both source and drain. Here the compact high-voltage MOSFET model HiSIM-HV is reported, which is valid for modeling both structure types, and was recently selected by the Compact Model Council (CMC) as the industry-standard high-voltage MOSFET model.

In order to drive a power MOSFET into and out of conduction (i.e. turn it ‘on’ or ‘off’) fast enough so that it can be used in high frequency applications and provide good signal fidelity, an efficient, reliable, and robust gate driver circuit is required. This circuit should be able to take a low voltage and low current input control signal, amplify its voltage, and produce a high-current drive output to control the gate of high-power transistors power MOSFET. The gate driver circuit might utilize a voltage level shifter and delay circuits to achieve the required voltage translation and to reduce any shoot-through current at the final stage to improve the rise/fall time of the output signal and reduce dynamic power dissipation, in addition to current buffer stages that increase the current drive at the output stage.

The gate driver presented in this thesis is built on SiC material to drive a SiC power MOSFET. Gate drivers are very important part of any switching power electronics that utilizes power MOSFET switching to achieve various tasks. A multitude of systems use a switching power MOSFET with applications including, but not limited to, power supplies, voltage converters, motor controllers, industrial automation applications, x-ray tubes, communications equipment, aviation applications, manufacturing plants, data centers, automobiles, spacecraft, etc. This particular project is focused on integration of this gate driver into a Toyota Pries plug-in hybrid electric vehicle (PHEV) charger module. The application of this high frequency charger will result in a charger system with 5 times more output power, 10 times size reduction causing reduction in weight of the system as well, and substantial cost reduction on the long run.

Power MOSFET drive circuits often have to work at high temperature environments like server farms, automobiles, extreme industrial environments, space vehicles, etc. These applications demand a gate driver circuit that is functional, efficient, and reliable at high temperatures. With its high thermal conductivity and wide bandgap energy, SiC circuits can operate efficiently at high temperatures which are extremely suitable for applications in these scenarios.

A SiC power MOSFET can be switched at higher switching frequencies with smaller power dissipation when compared to their silicon counterparts. Hence, good driver circuitry able to drive the SiC power MOSFET switch at high frequencies enables usage of these power MOSFETs in high frequency applications that leads to significant reduction in size of inductors and capacitors for a given power rating thereby increasing the converter power density. This property will be enormously useful for portability and transportation applications like aircraft, automobiles, spacecraft, space stations, etc.

2. Introduction of HiSIM_HV

Integrated circuits combine a huge number of transistors to create various functions. At this time, using a transistor model that describes the transistor characteristics, the transistor response to a given voltage is calculated to predict the integrated circuit characteristics while proceeding with the design. Transistor characteristics include current to voltage and charge response stored in the transistor.

Since the accuracy of the transistor model determines the accuracy of circuit characteristic prediction, a high-precision model has been desired. Further, since the number of transistors in the integrated circuit is large, it is also required that the calculation time is short (several microseconds). If a short calculation time cannot be realized, it will not be possible to actually predict the circuit characteristics within a limited time. It was a very difficult task to realize the above two requirements at the same time. HiSIM (Hiroshima-university STARC IGFET Model) cannot develop a model with high accuracy and short calculation time by the approximation used in model development so far . Development was carried out and the above difficult tasks were achieved. The HiSIM created in this way has become the world's first potential model and continues to provide guidance for new model development. By the way, most of the newly developed models are potential models. The features of the model are that the higher-order differentiation of transistor characteristics is smooth, and it has been demonstrated that complex circuit characteristic predictions are accurate. It is also a great merit that the non-linear characteristics of Transis can be described reasonably.

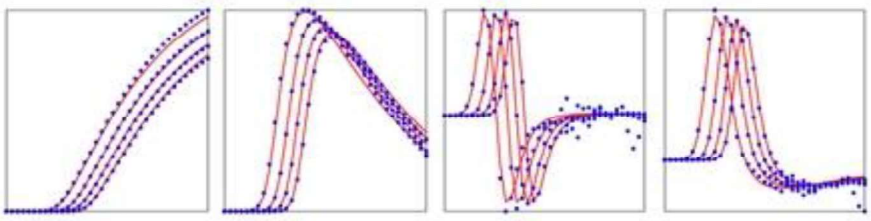

Figure 1 Results of higher-order differentiation of current-voltage characteristics (far left). Blue dot: measured value, red line: HiSIM result.

So far, four of the HiSIM Family models have been certified as global standards and are used all over the world. Since we have been developing models based on the transistor principle, we have demonstrated from the development of a wide variety of models so far that we can respond quickly even if transistors of various materials and structures are developed.

3. INTRODUCTION OF SWITCH

The switch is an electrical device that is used to break or make an electrical circuit manually or automatically. The working principle of switch depends on ON/OFF mechanism. Various electrical or electronic circuits use switches to control or trigger the owl circuit. The types of switches depend on the connections of the circuit they make.

The following power electronic devices which act as solid-state switches in the circuits. They act as a switch without any mechanical movement.

- Power Diodes
- Power MOSFET
- Bipolar -Junction Transistor (BJT)
- Insulated-Gate Bipolar Transistor (IGBT)
- Thyristors (SCR, GTO, MCT)

When using the Power MOSFET as a switch we can drive the Power MOSFET to turn "ON" faster or slower, or pass high or low currents. This ability to turn the power MOSFET "ON" and "OFF" allows the device to be used as a very efficient switch with switching speeds much faster than standard bipolar junction transistors.
Power MOSFET is a type of Power MOSFET which is specially meant to handle high levels of power. These exhibit high switching speed and can work much better in comparison with other normal Power MOSFETs in the case of low voltage levels. However its operating principle is similar to that of any other general MOSFET.

3.1 OVERVIEW OF IDEAL SWITCH :-

For an ideal switch, we would like that when the switch is ON the current to be able to flow both in the positive and also in the negative direction meaning T to P and P to T, and during the time on the switch is OFF we would like the voltage across the switch that is to be supported by the switch. It should be capable of supporting both the forward voltage and also reverse voltage, with zero conduction loss. Zero conduction loss meaning when the switch is ON there is a current flow there should not be any I square or loss within the switch or there should not be any drop across the switch only under such conditions will zero conduction loss happen. So, let us say one of the characters of an ideal switch is that when the switch is ON there is no power loss in it. As a corollary feature, you have zero conduction resistance.

In the OFF state when the switch is OFF again looking at the characteristic, it has to Support voltage. So, it should be capable of supporting both positive and negative voltage Across the switch, this is one character of the ideal switch, and also like during ON state, During OFF state also there should be zero of state loss no leakage current should be flowing through the switch. And the resistance when the switch is OFF should be infinite meaning zero leakage currents flowing through the switch and also meaning zero losses in the switch.

Another important characteristic of an ideal switch is that the switch from ON state to OFF state, OFF state to ON state should be instantaneous it should be in zero time which is not possible in a practical switch, but this is a desirable feature in an ideal switch. This also implies that if it is instantaneous if this switching ON and switching OFF happens in zero time also means that there is no power loss during switching.

So, these are some of the classic features of an ideal switch; however, we know that none of these features are fully met in a practical switch, as we have seen even in the static characteristic of BJT diodes and MOSFETs they do not reflect the static characteristic of the ideal switch. So, we have to consider the shortcomings in each of the switches and try to design a drive circuit that will try to make up for the shortcomings and take it to as good a semiconductor switch electronics switch as possible.

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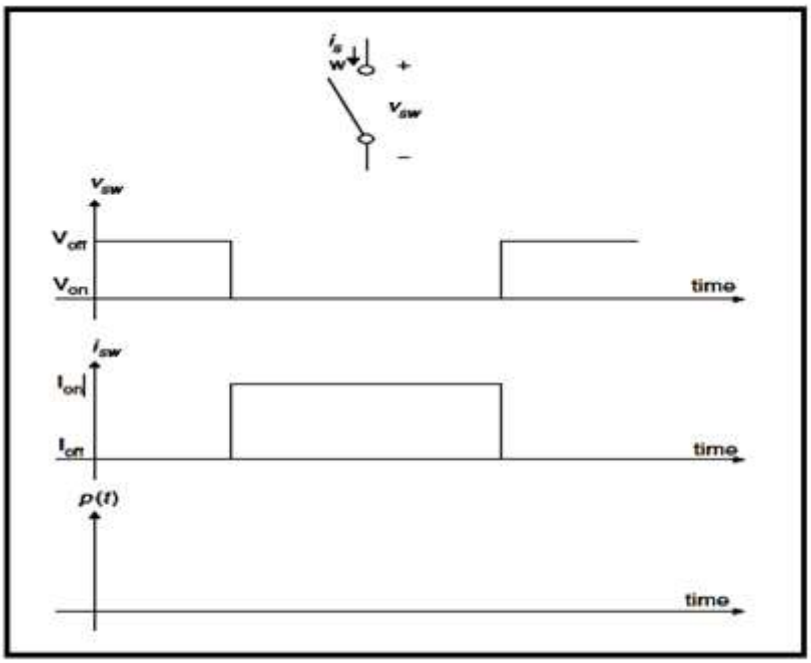

Figure 2 : Ideal switch

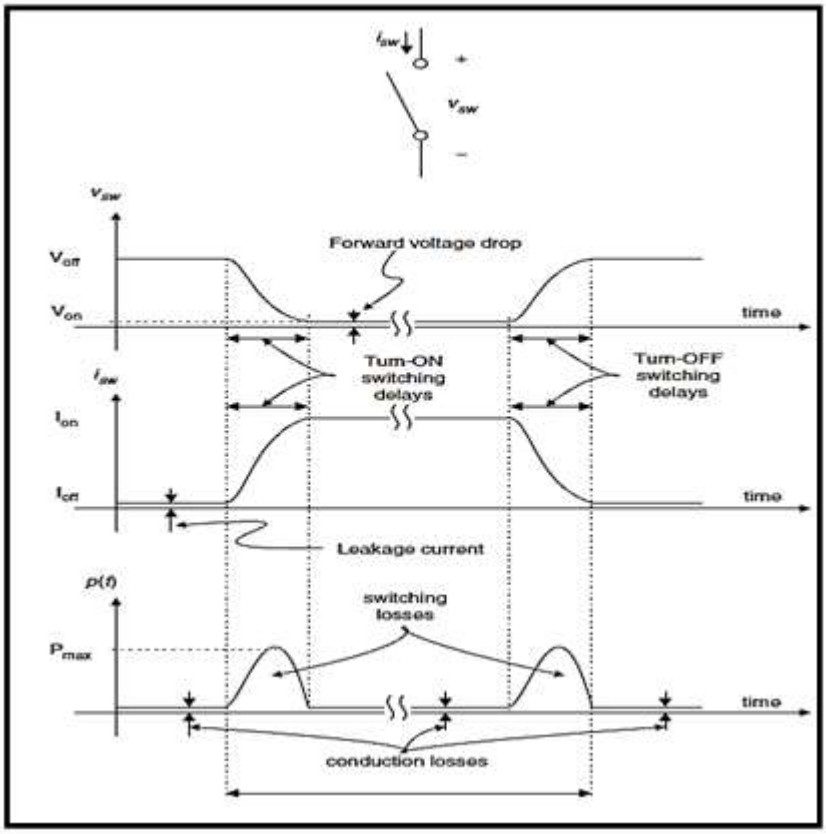

Figure 3 : Practical Switch

4. POWER MOSFET

it is a voltage-controlled majority carrier (or unipolar) three-terminal device.Its symbols are shown in below figure As compared to the simple lateral channel MOSFET for low-power signals, power MOSFET has different structure. It has a vertical channel structure where the source and the drain are on the opposite side of the silicon wafer. This opposite placement of the source and the drain increases the capability of the power MOSFET to handle larger power.

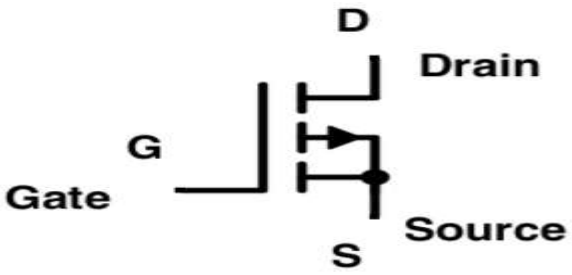

Figure 4 : MOSFET

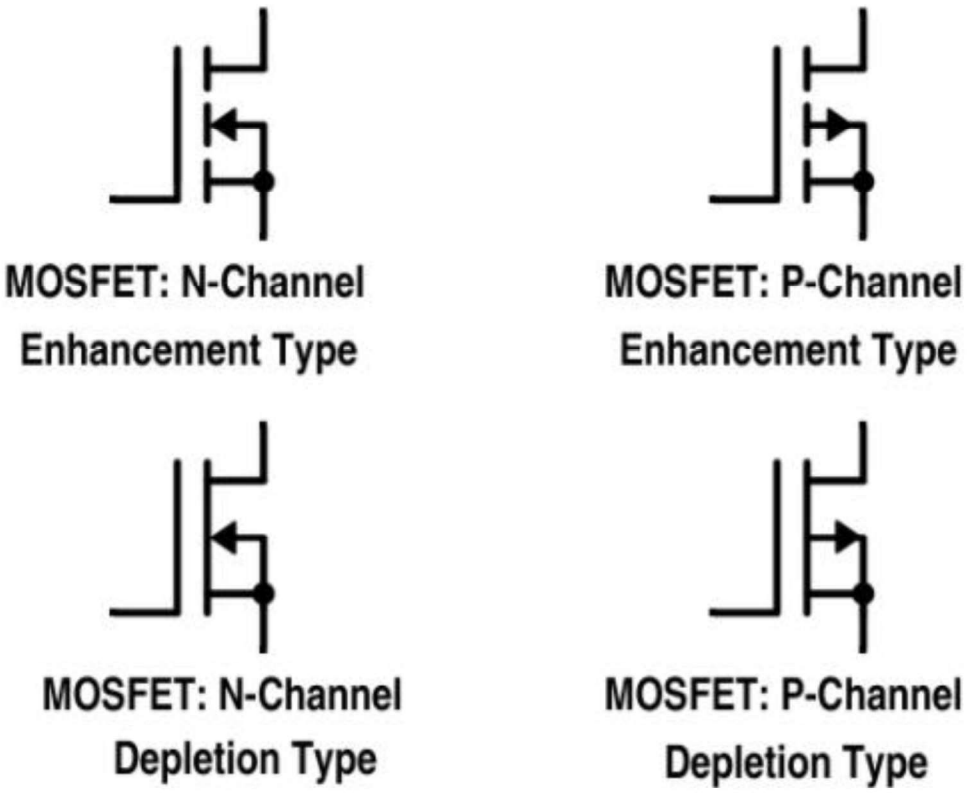

Figure 5 : power MOSFET Symbols for Different Modes

In all of these connections, substrates are internally connected. But in cases where it is connected externally, the symbol will change as shown in the n-channel enhancement type Power MOSFET in Fig. 9. N-channel enhancement type Power MOSFET is more common due to high mobility of electrons.

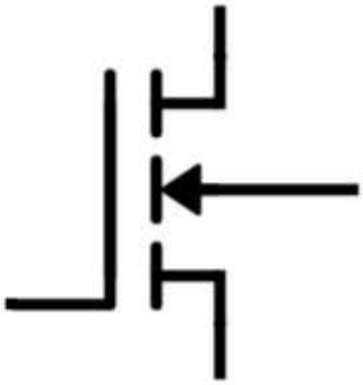

Figure 6 N-channel Enhancement-Type MOSFET with Substrate Connected Externally

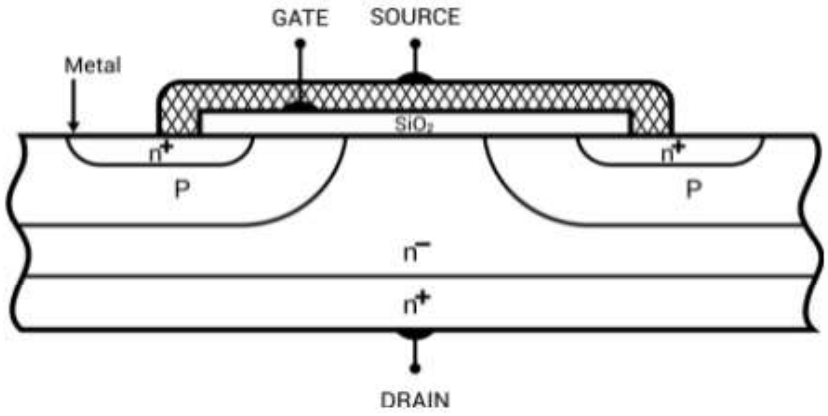

Figure 7 Cross-Sectional View of the Power MOSFET

Basic circuit diagram and output characteristics of an n-channel enhancement power MOSFET with load connected are in below Figure.

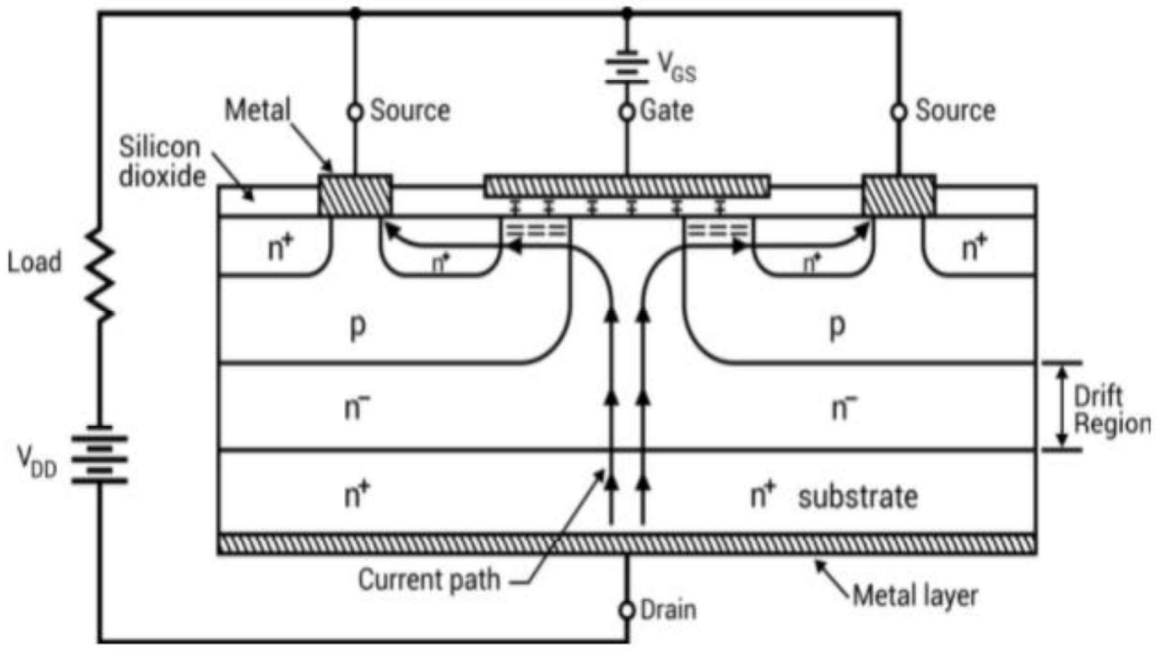

Figure 8 Power MOSFET Structural View with Connections

Drift region shown in above figure determines the voltage-blocking capability of the MOSFET.

When $V_{GS} = 0$,

⇒ V_{DD} makes it reverse biased and no current flows from drain to source.

When $V_{GS} > 0$,

⇒ Electrons form the current path as shown in above figure. Thus, current from the drain to the source flows. Now, if we will increase the gate-to-source voltage, drain current will also increase.

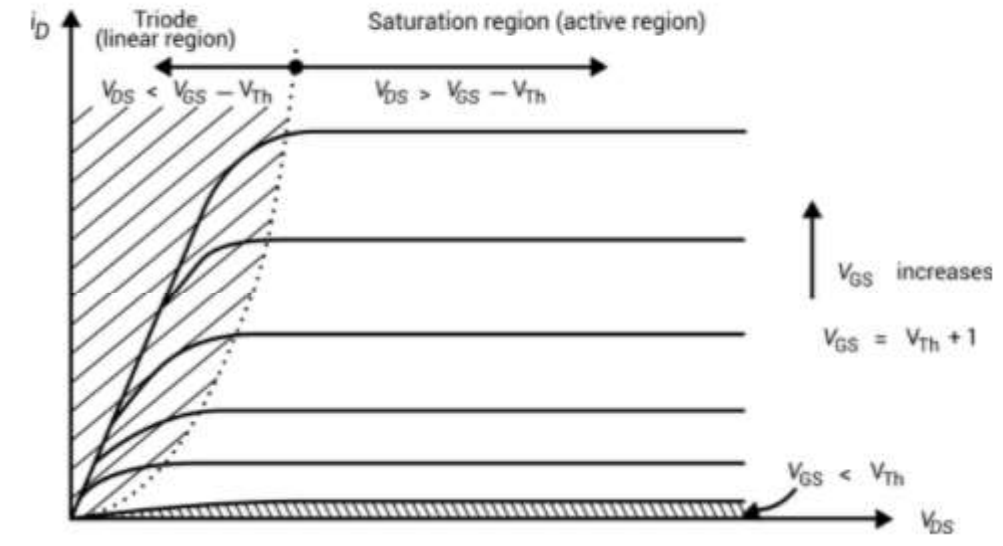

Figure 9 Drain Current (ID) vs Drain-to-Source Voltage (VDS) Characteristics Curves

For lower value of V_{DS}, MOSFET works in a linear region where it has a constant resistance equal to V_{DS} / I_D. For a fixed value of V_{GS} and greater than threshold voltage V_{TH}, MOSFET enters a saturation region where the value of the drain current has a fixed value.

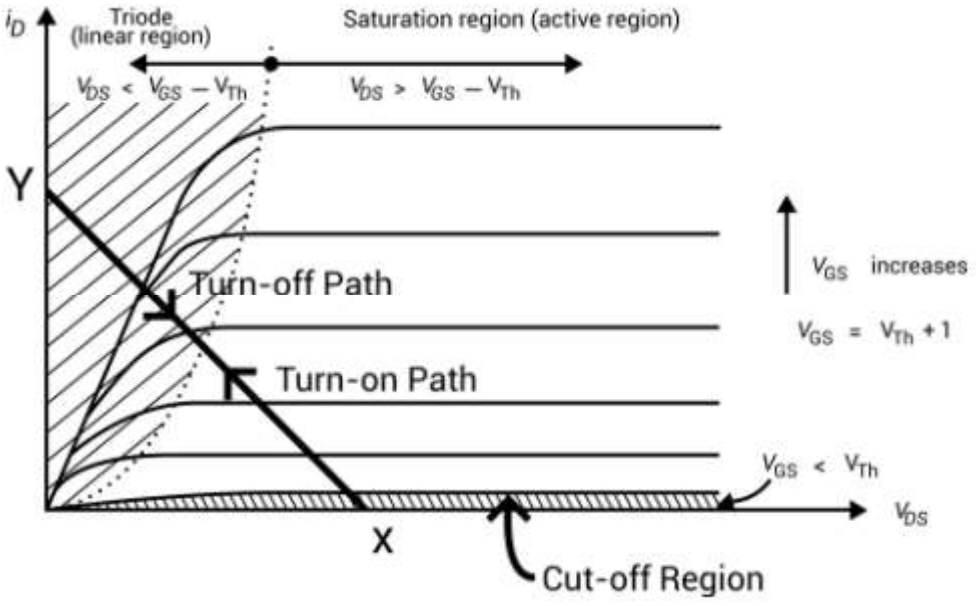

Figure 10 Output Characteristics with Load Line

The load line is drawn by joining the saturation and cut off points. The region that lies between these two is the linear region. A transistor acts as a good amplifier in this linear region.
If this load line is drawn only when DC biasing is given to the transistor, but no input signal is applied, then such a load line is called as DC load line. Whereas the load line drawn under the condition, when an input signal along with the DC voltages is applied, such a line is called as an AC load line.

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the Saturation point. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the Cutoff point.
When a line is drawn joining these two points, such a line can be called as Load line. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point or quiescent point or simply Q-point.
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If XY represents the load line, then the X-point represents the turn-off point and Y-point is the turn-on point where $V_{DS} = 0$. The direction of turning on and turning off process is also shown in Figure Besides the output characteristics curves, transfer characteristics of power MOSFET is also shown in Figure.

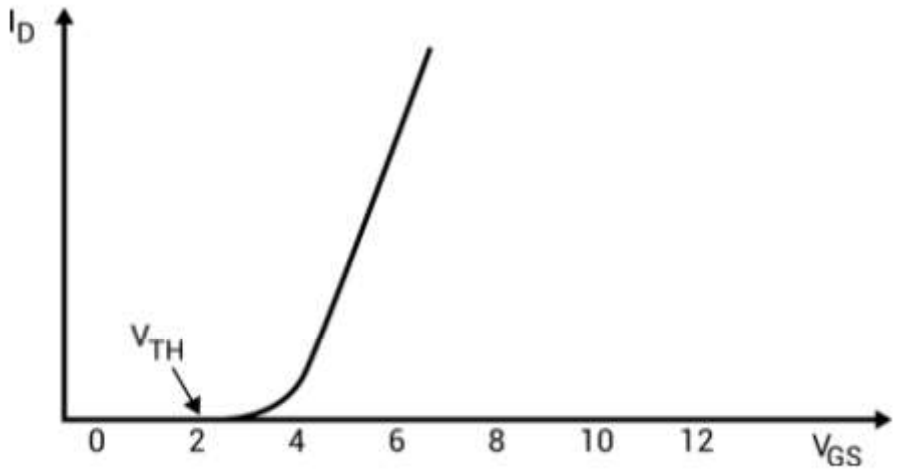

Figure 11 Gate-to-Source Voltage vs. Drain Current Characteristics for Power MOSFET

Here, V_{TH} is the minimum positive voltage between gate and the source above which MOSFET comes in on-state from the off-state. This is called threshold voltage. It is also shown in the output characteristics curve.
Close view of the structural diagram given in Fig. 11 reveals that there exists a fictitious BJT and a fictitious diode structure embedded in the power MOSFET as shown in Fig. 15.
As source is connected to both base and emitter of this parasitic BJT, emitter and base of the BJT are short circuited. That means this BJT acts in cut-off state.

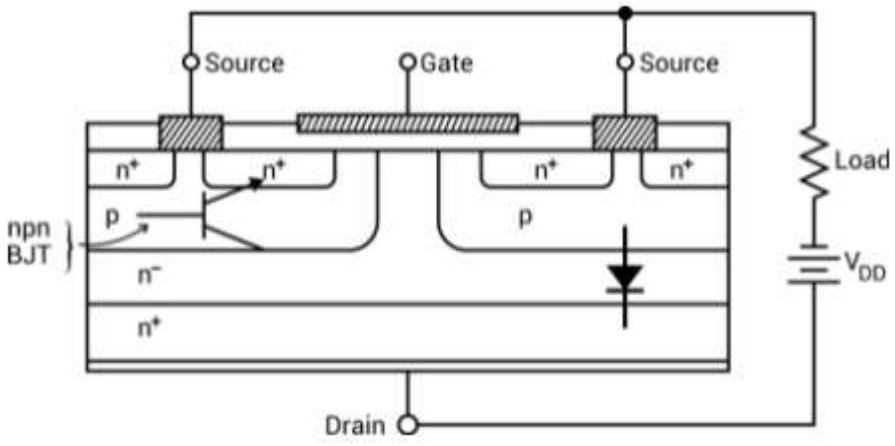

Figure 12 Fictitious BJT and Fictitious Diode in the Power MOSFE

The negative voltage VDD across the drain and source, it will be forward biased. That means, the reverse-blocking capability of the MOSFET breaks. Thus, this can be used in inverter circuit for reactive loads without the need of excessive diode across a switch.

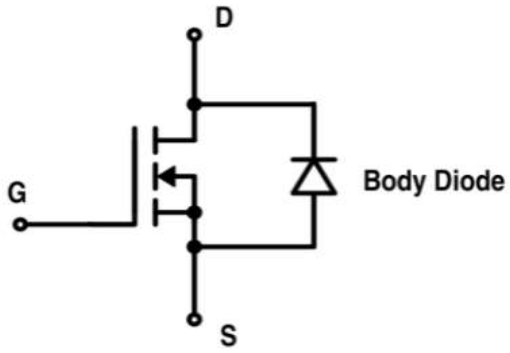

Figure 13 MOSFET Representation with Internal Body Diode

Although MOSFET internal body diode has sufficient current and switching speed for most of the applications, there may be some applications where the use of ultra-fast diodes is required. In such cases, an external fast-recovery diode is connected in an antiparallel manner. But a slow-recovery diode is also required to block the body diode action as given in below figure 11.

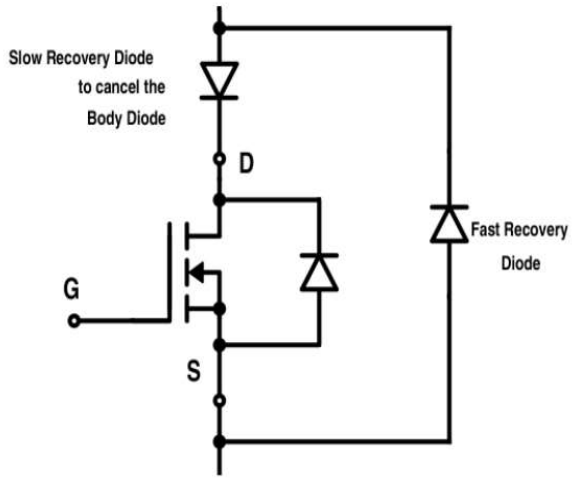

Figure 14 Implementation of Fast-Recovery Diode for Power MOSFET

One of the important parameters that affects the switching characteristics is the body capacitances existing between its three terminals i.e. drain, source and gate. Its representation is shown in below figure.

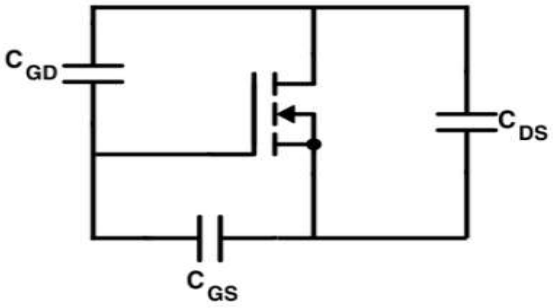

Figure 15 MOSFET Representation Showing Junction Capacitances

Parameters CGS, CGD and CDS are all non-linear in nature and given in the device's data sheet of a particular MOSFET. They also depend on the DC bias voltage and the device's structure or geometry. They must be charged through gate during turn-on process to actually turn on the MOSFET. The drive must be capable of charging and discharging these capacitances to switch on or switch off the MOSFET.Thus, the switching characteristics of a power MOSFET depend on these internal capacitances and the internal impedance of the gate drive circuits. Also, it depends on the delay due to the carrier .

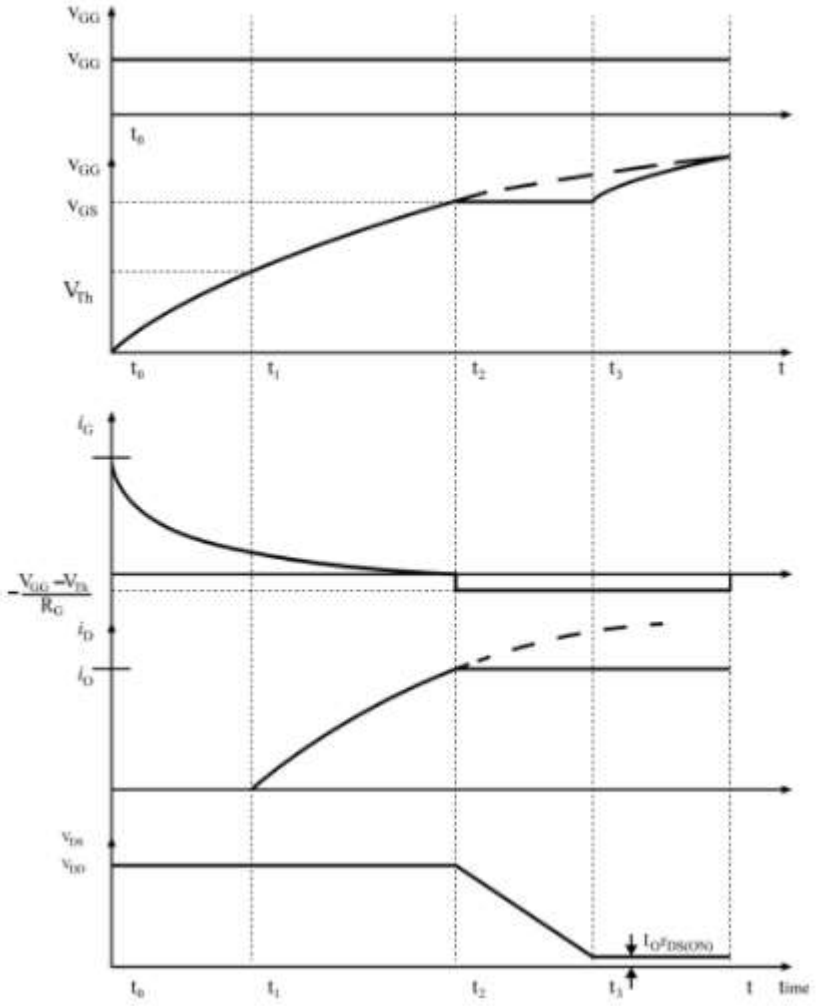

Figure 16 Turn-on Characteristics of Power MOSFET

There is a delay from t0 to t1 due to charging of input capacitance up to its threshold voltage VTH. Drain current in this duration remains at zero value. This is called a delay time. There is a further delay from t1 to t2 during which the gate voltage rises to VGS, a voltage required to drive the MOSFET into on-state. This is called the rise time. This total delay can be reduced by using a low-impedance drive circuit. The gate current during this duration decreases exponentially as shown. For the time greater than t2, the drain current ID has reached its maximum constant value I.

For turn-off characteristics, assume that the MOSFET is already in the switched-on situation with steady state. As t = t0, gate voltage is reduced to zero value; CGS and CGD start to discharge through gate resistance RG. This causes a turn-off delay time up to t1 from t0. Assuming the drain-to-source voltage remains fixed. During this duration, both VGS and IG decreases in magnitude, drain current remains at a fixed value drawing current from CGD and CGS.

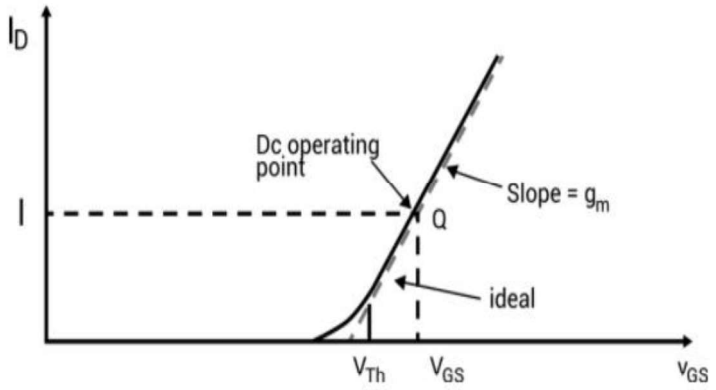

Figure 17 Transfer Characteristics of Power MOSFET with Operating Point

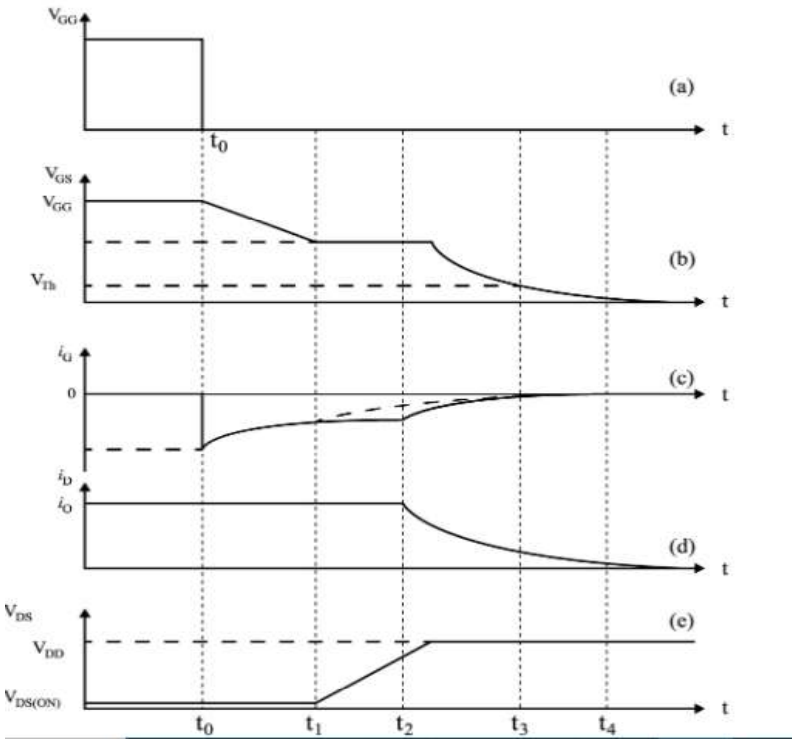

Figure 18 Turn-Off Characteristics of Power MOSFET

For the time where t2 > t > t1, gate-to-source voltage is constant. Thus, the entire current is now being drawn from CGD. Up to time t3, the drain current will almost reach zero value; which turns off the MOSFET. This time is known as the fall time, this is when the input capacitance discharges up to the threshold value. Beyond t3, gate voltage decreases exponentially to zero until the gate current becomes zero.

4.1 Silicon Carbide LDMOS:

Power MOSFET is a popular component to be utilized as a switch in power converters due to its high switching frequency capabilities. Conventionally, the main manufacturing material is silicon (Si), but new materials have been constantly under investigation. As Si-based power devices are approaching their physical performance limitations, fresh alternatives such as silicon carbide (SiC) have been introduced to power device markets. The essential benefits of SiC-based power devices include a wide bandgap and low on-resistance, and their development makes faster device operation in higher temperatures and voltages a reality

LDMOS technology has continued to evolve to meet the ever more demanding requirements of the cellular infra structure market, achieving higher levels of efficiency, gain, power and operational frequency. The LDMOS device structure is highly flexible. While the cellular infrastructure market has standardized on 28–32V operation, several years ago Freescale developed 50V processes for applications outside of cellular infrastructure. These 50V devices are targeted for use in a wide variety of applications where high power density is a key differentiator and include industrial, scientific, medical (ISM), broadcast and commercial aerospace applications.

Lower on-resistance per unit area leads to smaller chip size, which decreases parasitic capacitances while increasing switching speed capabilities. These attributes correspond to lower switching and conduction losses for the device and enable the evolution of power electronic converters towards higher power density and improved efficiency. In addition, SiC- technology makes it possible to develop components with significantly higher voltage ratings compared to the conventional Si-material, thus having a clear focus on 1200V and 1700V rated components [10]. Therefore, SiC MOSFETs mainly compete against Si Insulated-Gate Bipolar Transistors (IGBTs) in applications requiring high voltage ratings, rather than competing against Si MOSFET equivalents. However, since MOSFETs enable the use of higher switching frequency, they widen the application range for this power device.

4.2 Structure of Power MOSFET LDMOS:

Figure 18 depicts a cross section of a single finger of a typical LDMOS transistor. It includes a source metal region to electrically connect the N+ source to the P+ sinker, which in turn is connected to the back side source metal through the P+ substrate. This patented feature significantly lowers the source inductance to improve performance, but also allows the die to be directly attached onto an electrically and thermally conductive package flange to accommodate low-cost packaging platforms.

The boron p-type “PHV” diffusion establishes the threshold voltage and turn-on characteristics of the device. The polysilicon gate provides a low gate access resistance, important for the large dimensions typical of RF power devices. A low doping concentration arsenic n-type “NHV” drift region between the gate and the highly doped N+ drain region is designed to support high breakdown voltages, low on-state resistance (RDSon) and good hot carrier injection (HCI) reliability. The stacked aluminum drain metal is designed to meet electro migration specifications for high reliability. A metal-2 gate bus running parallel to the gate makes periodic connections to the gate polysilicon stack to reduce its resistance. Grounded shield structures (the ground strap is not shown in this figure) are also employed to reduce feedback capacitance between the drain and gate, and to control surface electric fields to allow for improved device performance without sacrificing breakdown voltage or HCI margin. Another Free scale innovation pioneered in the

Cellular infrastructure market that is incorporated into the 50V LDMOS RF power product portfolio is an enhanced ESD protection structure that can tolerate moderate reverse bias conditions being applied to the gate lead (see Figure 2). An example of when this enhanced device is very beneficial is Class C operation at high input RF power levels. The RF swing could easily turn on a standard ESD structure during a small negative voltage swing, while the enhanced ESD device would remain off. The enhanced structure employed in the RF power products is much more robust against a broad range of operating conditions that may be encountered during operation.

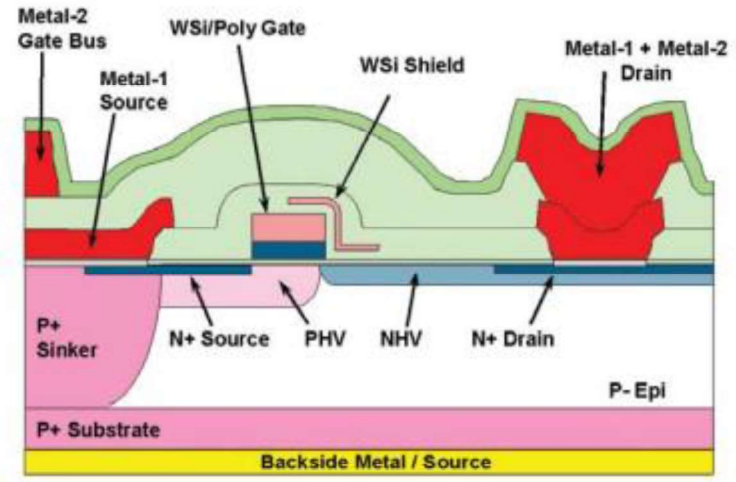

Figure 19 Cross section of an LDMOS device

4.3 Advantage of SiC mosfet over the Si mosfet

Silicon Carbide has quite a list of advantages over Si when used in semiconductor technology, including:

- A higher critical breakdown field, which means a voltage rating can be maintained while still reducing the thickness of the device
- A wider bandgap, leading to lower leakage current at relatively high temperatures
- A higher thermal conductivity, which supports a higher current density
- An overall reduction in energy losses Using Silicon Carbide in place of Si in MOSFETs also results in Reduced switching losses, which impact losses that occur when the MOSFET is transitioning from blocking to conducting (and vice versa)

- Higher switching frequencies, which means smaller peripheral components (e.g., filters, inductors, capacitors, transformers) can be used
- Increased critical breakdown strength, about 10x what is achievable with Si
- Higher temperature operation, which means simplified cooling mechanisms (e.g., heat sinks)

5. OVERVIEW OF GATE DRIVER CIRCUIT

Traditional gate driver components designed for controlling power MOSFETs are PWM controllers with different embedded functions. Circuits generally control switches, by connecting them between a supply voltage and circuit ground reference potentials. This action enables the controlling of power, frequency, and voltage of a power converter. Controllers are also used to monitor different quantities, such as current and overvoltage, and react to undesirable situations. Monitoring makes it possible for the converter to remain within specified operation mode and area. To achieve the full benefits of a SiC device, a proper gate driver circuit has to be designed to fit the application in question. As these switches are especially convenient for high-speed and high-voltage applications.

5.1 Fast charging & Discharging path:

In today's power IC (Integrated Circuit) market, there are kinds of power MOSFET gate drive chips available. Usually, all these commercial gate drivers have the same circuit configuration: a "Totem-Pole" structure, in which the drain terminal of a P- channel MOSFET is connected to the drain of an N-channel MOSFET. In this thesis, all gate drivers with t h e above simple "Totem-Pole" structure are referred to as "conventional gate drivers [16].
MOSFET is a charge control device voltage or a voltage control device it is this charge that is important. We must give an amount of charge for the MOSFET as required by the datasheet of the MOSFET and if you give that amount of charge to the gate-source then that will turn ON the device.

In the OFF state when the switch is OFF again looking at the characteristic, it has to Support voltage. So, it should be capable of supporting both positive and negative voltage Across the switch, this is one character of the ideal switch, and also like during ON state, During OFF state also there should be zero of state loss no leakage current should be flowing through the switch. And the resistance when the switch is OFF should be infinite meaning zero leakage currents flowing through the switch and also meaning zero losses in the switch.

Another important characteristic of an ideal switch is that the switch from ON state to OFF state, OFF state to ON state should be instantaneous it should be in zero time which is not possible in a practical switch, but this is a desirable feature in an ideal switch. This also implies that if it is instantaneous if this switching ON and switching OFF happens in zero time also means that there is no power loss during switching.

The circuit is a "Totem-Pole" structure. The upper MOSFET is p-type and the lower one is N-type. The resistor RON & ROFF between "Gate Driver" and power MOSFET stands for the gate resistance of the power MOSFET. it includes the MOSFET semiconductor bulk resistance, power packaging resistance, and the ON-resistance "Totem- Pole" structure. In some applications, an external resistor can be used in series with the gate of the power MOSFET to prevent high-frequency rings, in those applications, it also includes the external resistor.

On the right side, we have Sic power MOSFET Cinstands for the equivalent gate input capacitance of the power MOSFET .it is not external to the MOSFET, although it is drawn so for convenience . because of the "Miller Effect" , the gate capacitance of power MOSFET varies at different voltage levels. In other words, Cin is nonlinear in reality above Cin can thus be regarded as the average capacitance over the complete charging and discharging transitions. Figure 4.2 shows the relationship between the gate voltage and the gate charge of a typical power MOSFET. the flat portion of the curve comes from the "Miller Effect".

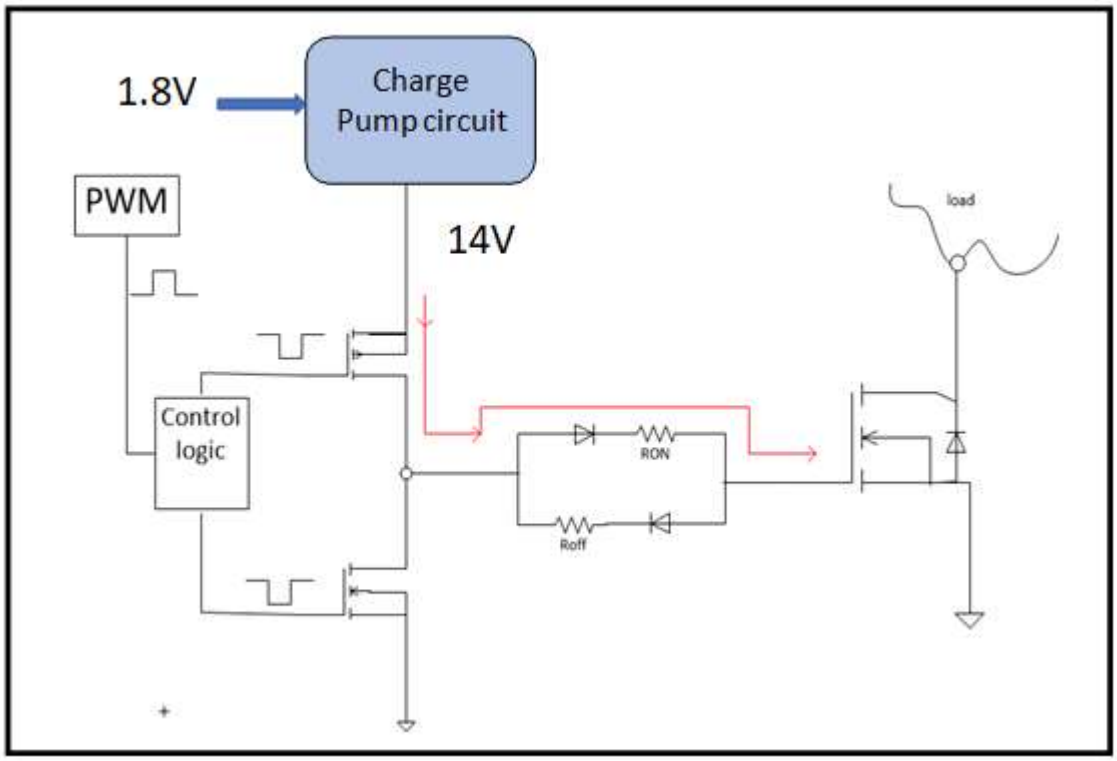

Figure 20 Fast Charging Path

5.2 FAST DISCHARGING PATH :

Discharging time of the gate driver circuit is decided by the discharging path, in our design we provided a separate path for charging and discharging to eliminate the crosstalk between the charging and discharging path. Discharging time depends upon how fast we can remove the charge from the power switch, Roff is very low and it is connected to the totem pole circuit when the switch is off the total charge will be grounded by using this fast discharge path.

To slow down the large transients we need to connect some other path that can take care of the switch. We have Ron which is very low for providing the fast-switching speed we cannot increase the value for Ron it will decrease the switching speed.
Usually, this transient will take place when the short circuit occurs in the load, so whenever this short circuit happens, we need to provide a separate path to the current. We will use a control logic circuit to decide the operation of the discharge path.
The soft turn-off is achieved by a soft-off resistor (Rsoft) after overcurrent. Rsoft is large and series connected with a soft turn-off circuit. MOSFET which is connected to R turns on and the gate current will go through it after overcurrent occurs.

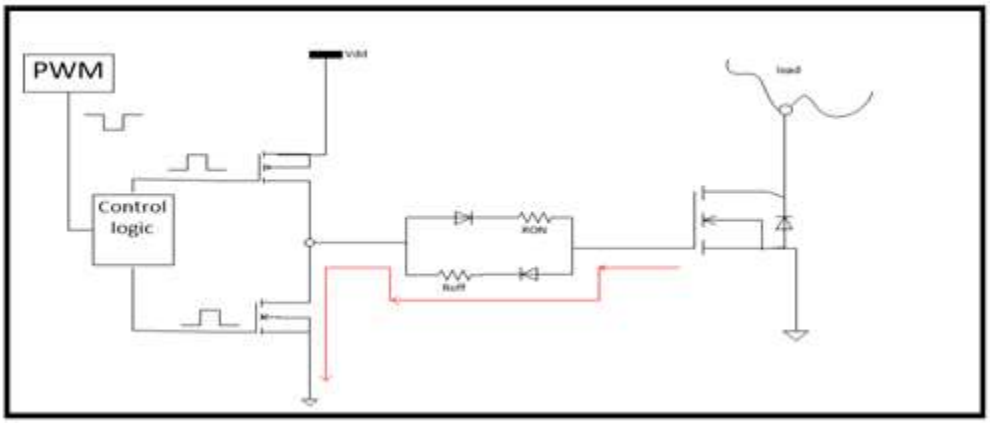

Figure 21 Fast Discharging Path

5.3 OVERCURRENT PROTECTION CIRCUIT :

Need for Over-Current protection:

POWER MOSFET will have some rated current it can offer to flow through it without any loss in load as well as in channel of POWER MOSFET. and also, there will be some rated current for the load, it means the maximum current that load can withstand. So, we need to track the current that flows in the channel and the load and we do to put some circuit that can sense the current and it will take action if the current crosses the maximum value.

Design details:

The main objective in this over-current protection circuit is to sense the current that flows in the load for that we used one diode. the diode will sense the current in the MOSFET. Here we replaced the power MOSFET switch with its equivalent ON resistance [32]. The ON resistance of the power MOSFET switch is 100milli ohm. and the diode is reverse biased for the MOSFET current that means it will not allow the switch current to flow into it. another end of the diode is connected to a low voltage Vdd that is 1.8V with the resistor.Then to compare the voltage drop across the diode and POWER MOSFET. we used one Op-Amp comparator .it will generate the fault signal when it crosses the reference value.

Circuit Operation:

The circuit operation as Fellowes, let us start with the MOSFET is OFF this means the diode will be reverse biased there will be no current flowing through the diode and the voltage at the V+ terminal of the Op-Amp is zero that means the fault signal is zero.

Then the MOSFET is ON and there will finite voltage drop across the switch because if finite Ron, through the Vdd the diode is in forward bias there will be current flow from Vdd to POWER MOSFET through the diode to the ground. When the current which is greater than the 10A flows through the switch, it will increase the voltage drop across the V+ that will cause the fault signal generated at the output of the comparator.

Here the power MOSFET that we have can handle the current of 10A, so for this 10A of current we designed the circuit, which means we decided the Vref that will assure the 10A as the maximum current so here my MOSFET is giving 1V across it and my diode is giving 0.2v volts as the forward voltage drop. The reference voltage nothing but the voltage across the switch plus the forward voltage drop of the diode according to this we decided the reference voltage of the op-amp inverting terminal.

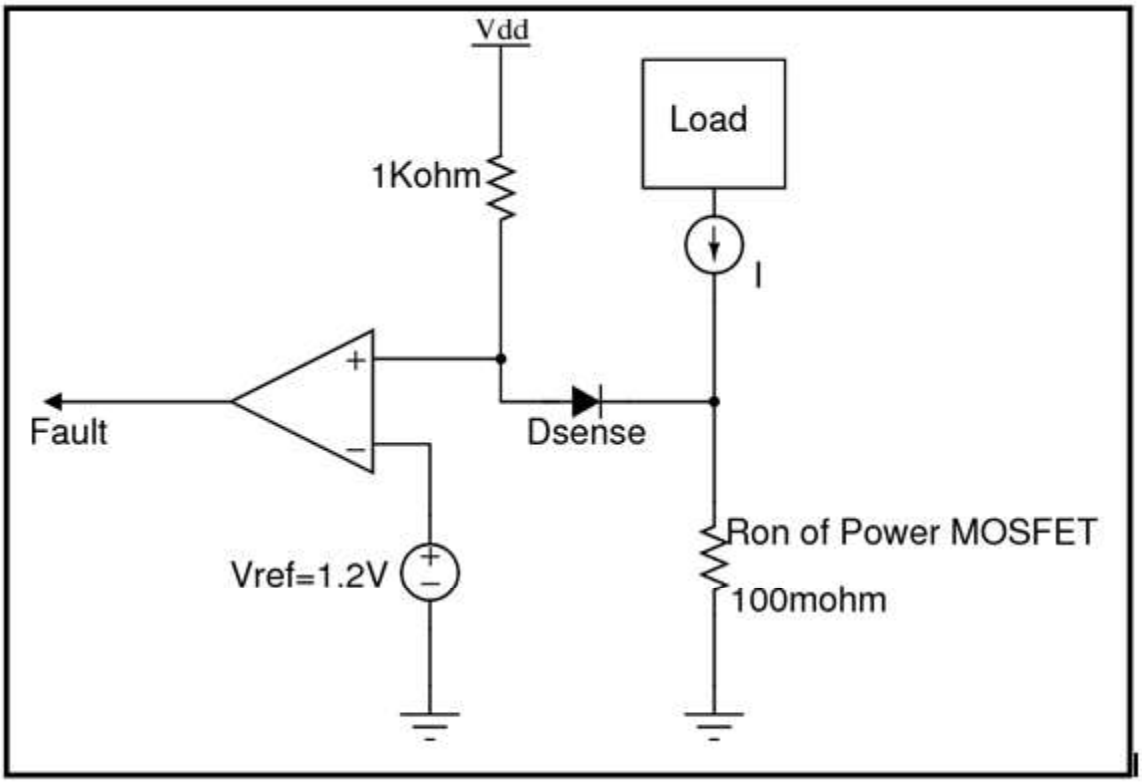

Figure 22 Over-Current protection circuit

Output waveforms:

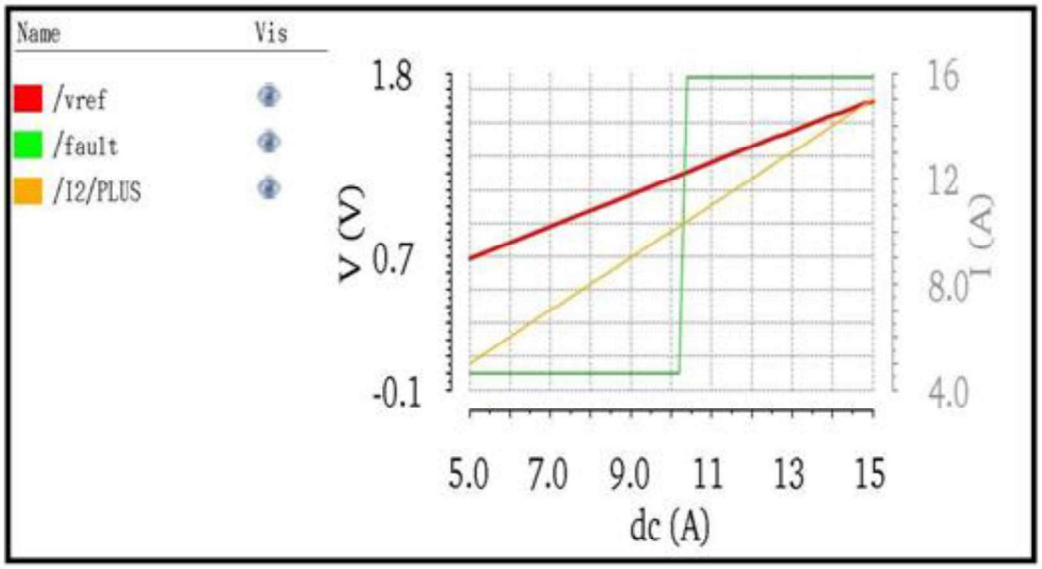

Figure 23 Output waveforms of Over-Current protection circuit

5.4 Transient protection:

SiC MOSFET operates in high frequency and high di/dt and dv/dt will be existed during the switching time due to parasitic inductance [6]. Higher operation frequency will require a higher switching speed, which will inevitably generate high dv/dt and di/dt, which will in turn cause voltage and current overshoots and oscillations because of the existence of parasitic inductance in the gate and drain loop. The large overshoot across Vds has the potential to destroy the device and also cause degradation.
Gate resistance plays an important role in gate driver. It influences the turn-on and turn-off time of the SiC MOSFET and also can affect the dv/dt and dv/dt during the switching time. A big gate resistance may increase turn-on and turn-off time and slow down the switching frequency, but it will reduce the dv/dt and di/dt during switching transient. The EMI is also reduced. A small gate resistance may increase the switching speed, but it brings large dv/dt, di/dt and EMI.

To slow down the large transients we need to connect some other path that can take care of the switch. We have Ron which is very low for providing the fast-switching speed we cannot increase the value for Ron it will decrease the switching speed.

Usually, this transient will take place when the short circuit occurs in the load, so whenever this short circuit happens, we need to provide a separate path to the current. We will use a control logic circuit to decide the operation of the discharge path.

The soft turn-off is achieved by a soft-off resistor (Rsoft) after over current. Rsoft is large and series connected with a soft turn-off circuit. MOSFET which is connected to R turns on and the gate current will go through it after over current occurs.

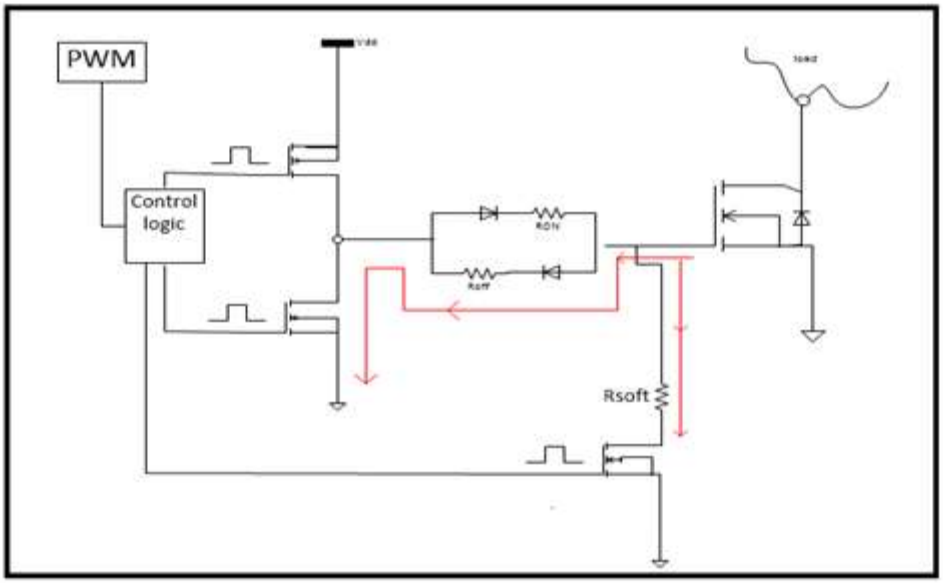

Figure 24 Transient protection circuit

5.5 Short circuit current protection along with transient protection:

Now, how do we go about doing current protection, we have here the drain current and we need some action if the drain current exceeds the rating as a particular set limit. So, if there is a current then this drive must be switched off the MOSFET must be switched off even if the drive current the gate drive is present.

The principle that we are going to use is that as the current increases the voltage Vds across the MOSFET is going to increase. The voltage across the device is going to increase. Now we have to detect this increase set a point and once the increase goes beyond a particular value, then we say that overcurrent has happened and we will switch off the MOSFET. So, that is the principle that we are going to take. So, now this is a series pass switch we will operate. Next, we use an Op-amp comparator Op-amp is a high slew rate comparator, Op-amp non-inverting terminal has connected to the positive power supply, and the op-amp inverting terminal, we will give a reference voltage. So, now this is a series pass switch we will operate. Next, we use an Op-amp comparator Op-amp is a high slew rate comparator, Op-amp non-inverting terminal has connected to the positive power supply, and the op-amp inverting terminal, we will give a reference voltage.

When the MOSFET is on there is a drop across that is Vds ON. Vds ON is coming across that this diode is conducting in this fashion to the ground from the power supply there is a current flowing through this diode through the on-device and to the ground. So, therefore, this potential will be a diode drop plus Vds ON.

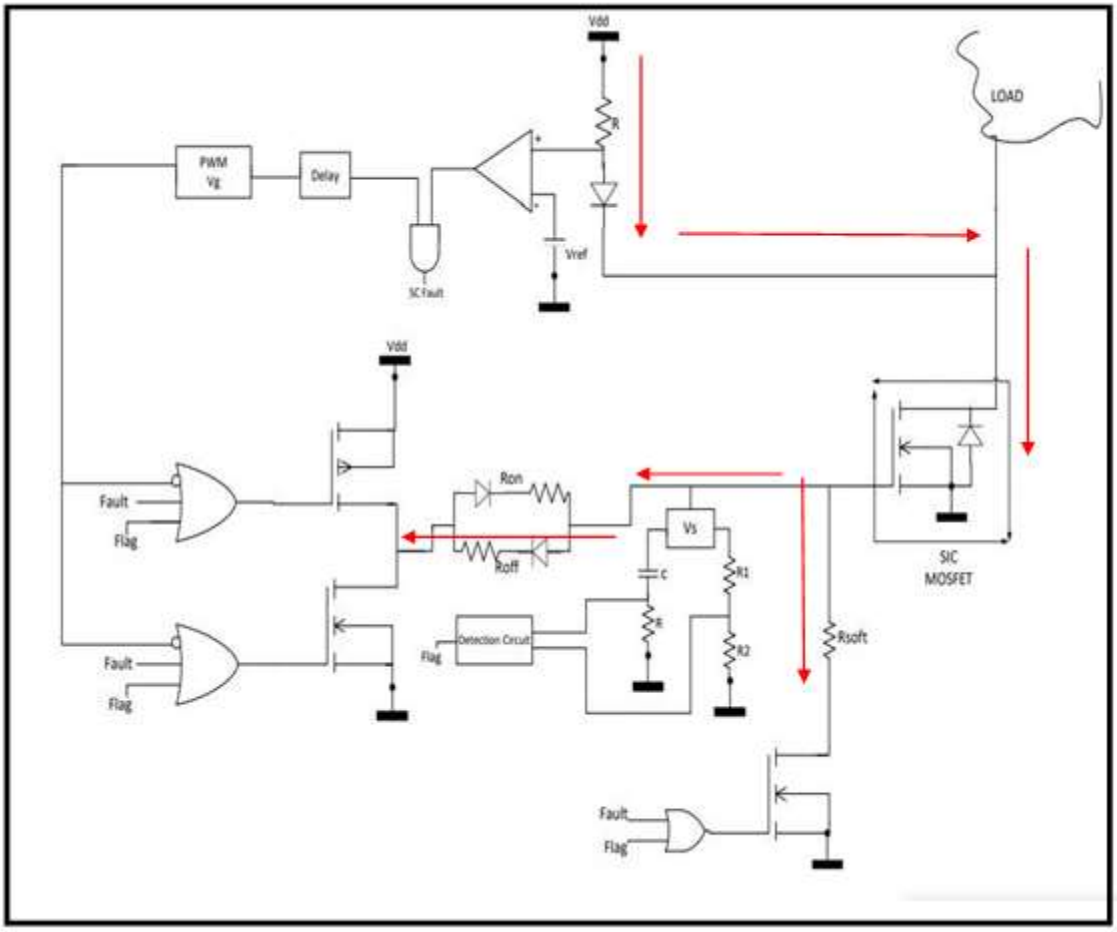

Figure 25 Over-current protection circuit

6. OVERVIEW OF LOSS ANALYSIS

For a unipolar device such as SiC MOSFET or GaN HFET, the switching process of MOSFET is substantially the process of charging and discharging its parasitic capacitances. Almost all commercial datasheet has Ciss, Coss, and Crss provided. But it is hard to use these to analyze the switching process. This is especially true for the Coss, which combines Cgd and Cds and Cds play different roles in the switching process.

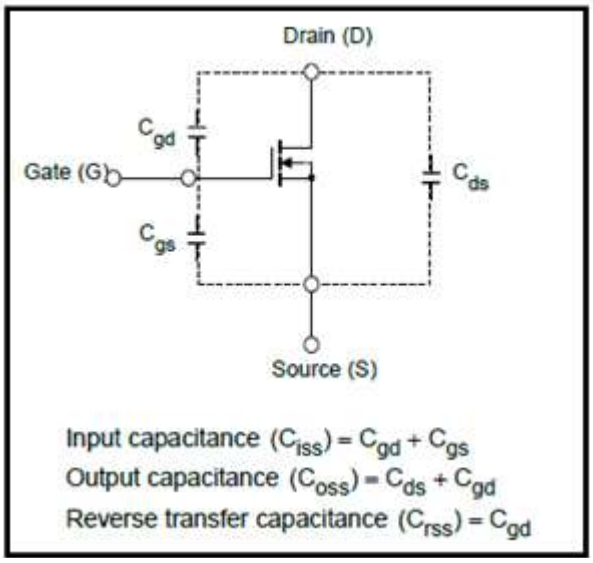

Figure 26 Capacitances of POWER MOSFET

6.1 Turn-On Energy Loss:

During the turn-on process, two phases of the turn-on process can be identified:

1. Rapid current rise phase (Tr)

2. Fast voltage fall phase (Tf)

Significantly the MOSFET channel current able to be measured in the TCAD mixed-mode simulation but is not measurable in actual device testing. The channel current is very important, which is the real current going through the MOSFET resistively [37]. During the current rise phase, the channel current is the same as the measured drain-source current. During the voltage fall phase, it is significantly larger than the drain-source current as shown in figure.2. The origin of the original large channel current is the discharge of the Cds and Cgd. Therefore, during the turn-on voltage phase,

Channel current = load current + discharge current of Cds + discharge current of Cgd

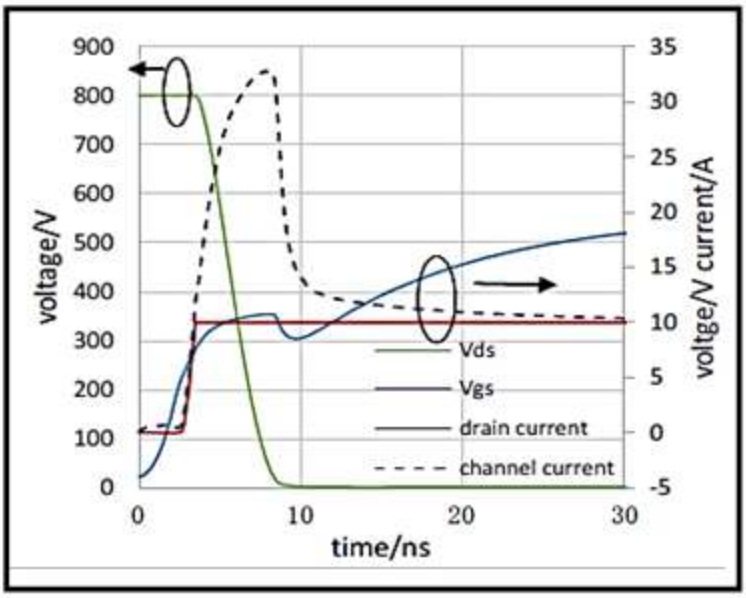

Figure 27 Turn on waveform

From an energy loss point of view, the additional loss due to the discharge of Cgd and Cds is equivalent to the amount of energy stored before the turn-on, which is the Eoss energy stored in Coss= Cgd+Cds[37]. This is very important since this energy loss is not measurable using current and voltage probes. Therefore, conventional Eon loss estimation is significantly incorrect and underestimates the Eon loss. The actual turn-on loss should be expressed as

$$Eon=Eon\ (measures) + Eoss$$

Where Eon measured is typically obtained by integrating measured V and I.

6.2 Turn-On Speed:

On the other hand, the turn-on speed, T=Tr+Tf, is both influenced by the gate driver condition. especially the voltage fall-time Tf, hence the dV/dt, is determined by the Cgd discharging speed or Cds discharging speed, whichever is slower! The available discharging current for Cgd is determined by the gate current value during this phase. In commonly used voltage- source type gate driver, gate current depends on the maximum gate drive and gate resistance. the maximum available discharging current for Cds is the short circuit current of the MOSFET minus be load current.

In most power, electronic circuit implementation, large Rg (external + internal) is typically used. Therefore, the Cgd discharge speed is slower hence determining the dV/dt rate. However, with lower drive resistance, the dV/dt could be ultimately determined by the Cds discharge speed.

Parameters	Turn-on process	
	Turn-on loss	*Turn-on time*
Cgd	Dominance	Dominance
Cds	Dominance (potential)	Dominance (potential)
Load current	Influence	Almost no influence
Gate current	Dominance	Dominance

Figure 28 Turn on the process of main parameters of MOSFET

6.3 Turn-Off Energy Loss:

The turn-off process is very different from the turn-on process. During the turn-on, available currents to discharge Cgd and Cds are provided by the MOSFET (not the load current) and the turn-on speed is determined by the gate drive circuit and device capacitance. On the other hand, for the turn-off, the charging of Cgd and Cds will be determined by the available load current [37]. A typical simulation waveform is shown in figure.3. Again, the measured channel current Ids are included to highlight the difference between the drain to source current and the current that flows through the resistive loss generating channel. Due to the inductive load turn-off behaviour, the load current hence the conventionally measured drain-source current does not drop until the device voltage rises above the DC link voltage and turns on the freewheeling diode. However, the channel current decreases quickly as soon as the gate voltage starts to decrease. The initiate decreases of the Cgs which has an opposite direction to the channel current.

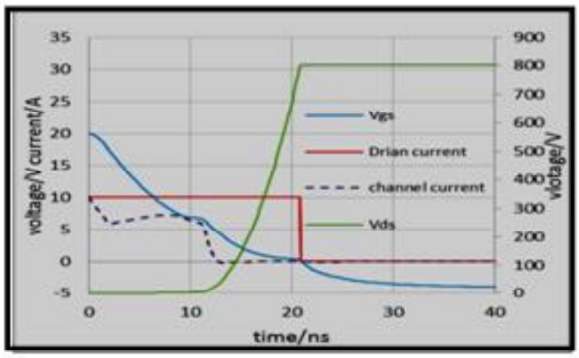

Figure 29 Turn-off waveform of SiC MOSFET

Therefore, the turn off loss should only be calculated using channel current instead of the drain-source current and

Channel current = load current – charging current of Cds – charging current of Cgd

Since the channel current is controlled and determined by the gate drive circuit as shown in the figure.3, it is possible to have the channel current reduced to zero, zero turn-off loss is possible in the SiC MOSFET, turn off if the gate drive circuit is fast enough.
Regardless of the speed of the gate drive circuit, the above discussion verifies that the conventional way of calculation turn-off loss Eoff is incorrect. The measured loss includes the amount of energy used to charge Cgd and Cgs. Therefore, the correct way of calculating Eoff is

$$E_{off}(actual) = E_{off}(measured) - E_{oss}$$

Adding the above equations together will result in a total switching loss

$$E_{total} = E_{on}(measured) + E_{off}(measured)$$

Although the effect of Eoss is cancelled out on the total loss calculation, it is important to remember the physical meaning of Eon and Eoff and use the correct equations to calculate Eon and Eoff breakdown. It is extremely important to use the above equations if soft-switching such as ZVS is used to recover the energy during turn-on.

6.4 Turn off speed:

It is therefore clear that the gate drive circuit determines the channel current reduction speed hence the turn-off loss. The load current will determine the charging rate of the Cgd and Cds hence the turn off dV / dt. Unless gate resistance is large, the dV / dt will then not be determined by the gate drive circuit. If SBD or MOSFET body diode is used as the freewheeling diode, a portion of the load current will be diverted to discharge the Coss of the SBDMOSFET, and there will be a decreased load current to charge the turning off MOSFET's Cgd/Cds. Lower dV/dt is therefore expected due to the increased total capacitance that needs to be charged/discharged by the same load current.

Parameters	**Turn-on process**	
	Turn-off loss	***Turn-off time***
Cgd	Influence	Influence
Cds	Influence	Almost no Influence
Load current	Dominance	Dominance
Gate current	Dominance	Dominance

Figure 30 The influence of the main parameters of the turn-off process is summarised

7. Positive-Negative Charge pump circuit

Below Figure shows the complete circuit diagram of multi-stage high voltage charge-pump that can generate both positive and negative voltages. Core of the circuit is designed using series connected stages of basic voltage-multiplier unit cell. Here five stages are cascaded to generate high voltages (but this is not the limitation of circuit and one can use different number of stages according to specification).

In the process of generation of positive voltage, we need positive input in the unit cell and to generate negative voltage we need ground connection to the input side of the unit cell 2 for this we can use inverter .when we applied positive input then inverter gives zero voltage to the unit cell2.and when input applied is zero inverter gives output to the unit cell.NMOS is synchronize with inverter so that this configuration provides alternative output to the both cascade connection.

This following design provides 20V output in positive way and -8V provides in negative.

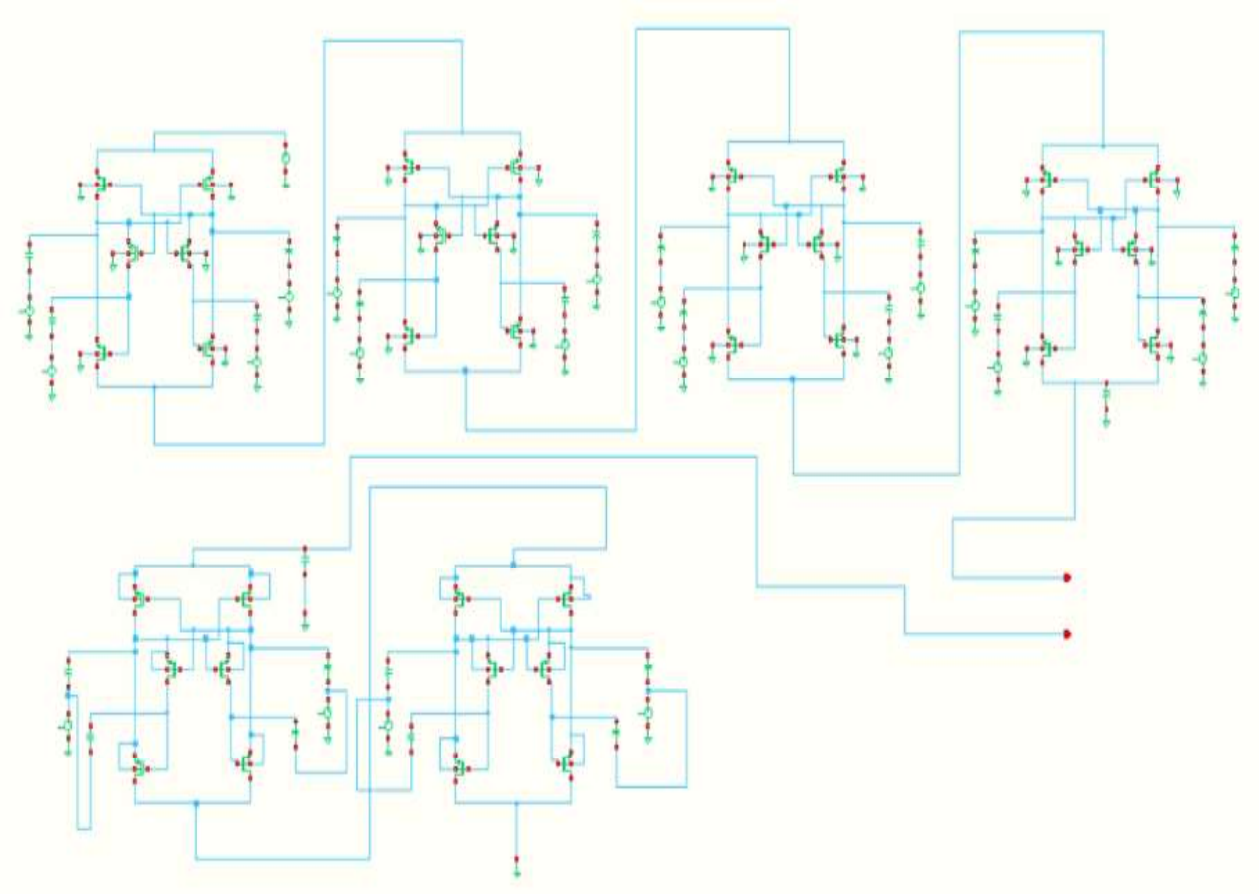

Figure 31 Positive-Negative Charge pump circuit

8. Operating principle of Positive Voltage Multiplier unit cell

This circuit shown in below Figure has capability to generate both positive and negative voltages. When circuit is used for positive voltage generation, then supply voltage VDD is applied to “VIN” node and with no clock condition, nodes NA1 and NA2 will charge to “VDD – Vtn” voltage levels. As soon as clock is enabled, assuming CK is “VDD”, CKN is “0”, CKH is “2*VDD” and CKHN is “0”. Due to coupling effect across capacitors C1 and C2, node NA1 will charge to “2VDD-Vtn” and NA2 will charge to “VDD”. Due to cross-coupled configuration of MN3 and MN4, NB1 and NB2 will charge to “3*VDD” and “VDD” respectively. As NB1 is at “3*VDD” and NA1 is at “2*VDD” so NMOS MN5 has sufficient Vgs to pass “2*VDD” voltage from node NA1 to VOUT. In this way, a positive voltage (higher than input supply voltage) is generated and passes on to output node to drive capacitive and current load. During different clock cycles, node NA1 and NA2 Switches between “VDD” and “2*VDD”. Similarly, NB1 and NB2 toggles between “VDD” and “3*VDD” voltage levels.

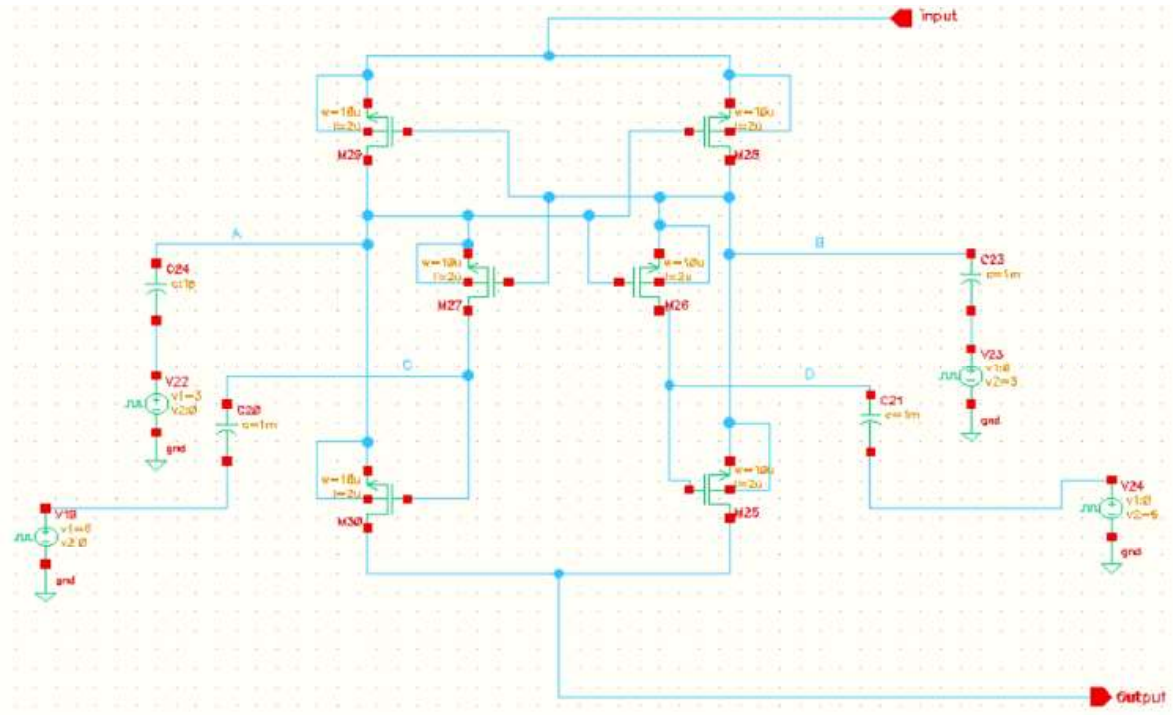

Figure 32 Operating principle of Positive Voltage Multiplier unit cell

9. Operating principle of Negative Voltage Multiplier unit cell

When the same circuit operates as negative voltage generator, then clock configuration remains same, but input is applied at node “VOUT” and output is taken from terminal “VIN”. During negative voltage configuration, “VOUT” node is connected to “GND” and in no clock condition, NA1 and NA2 will discharge to “Vtn” voltage level. When CKH goes to “2*VDD” (at this time CK is “VDD”) it switch ON the NMOS MN5 and charges node NA1 to “0”. During next clock cycle, when CKH switch from “2*VDD” to “0” and CK changes state from “VDD” to “0” then node NA1 move from “0” to “–VDD”. In addition, node NB1 discharge to “–VDD” via transistor MN3 and switch-OFF the transistor MN5. In this way, node NA1 reaches to “–VDD” voltage level. Due to effect of CKN and CKHN, node NA2 gets charge to “0” via MN6. As NA2 is at “0” and NA1 is at “–VDD”, this configuration switch-ON the transistor “MN1” and pass “–VDD” voltage to “VIN” node. In this way, a negative voltage (opposite in polarity to supply voltage) is generated and passes on to “VIN” node. During negative voltage configuration, node NA1 and NA2 toggle between “0/–VDD” and vice versa. Similarly, nodes NB1 and NB2 toggle between “VDD/–VDD” and vice versa. As explained, a single multiplier circuit can be configuring to generate both positive and negative voltages. In order to generate high positive or negative voltages, more number of stages can be cascaded in series that is explained in subsequent sections.

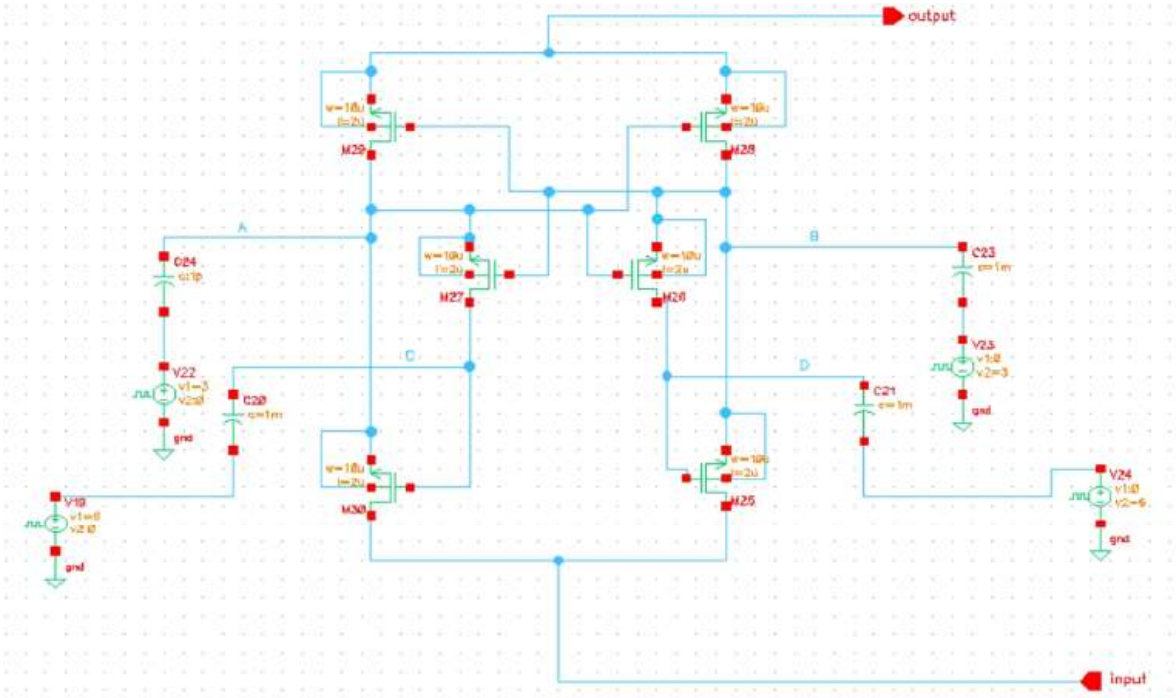

Figure 33 Operating principle of Negative Voltage Multiplier unit cell

10. Simulation result

This charge-pump circuit is design in 180nm-BCD technology using standard NMOS and PMOS transistors (not using DMOS). MOM capacitors are used in each stage for clock boost and bootstrapped configurations. the transient result for proposed circuit for four-stage charge-pump operated in positive and negative configuration. In this simulation, supply voltage is 4V, capacitive load is 10pF and operating clock frequency is 50MHz. In positive charge-pump case, we got 20V; hence, 900mV of voltage drop (VPAR) occurs due to parasitic element and Diode (DPOS) thus showing 93% of voltage multiplication efficiency. the variation in output voltage with increase in output load current. Output current is varied from 5mA to 100mA and accordingly output voltage is observed. There is a drop in output voltage due to finite output impedance shown by charge-pump.Dc voltage which is applied across the source of PMOS of the inverter is shown below in figure.

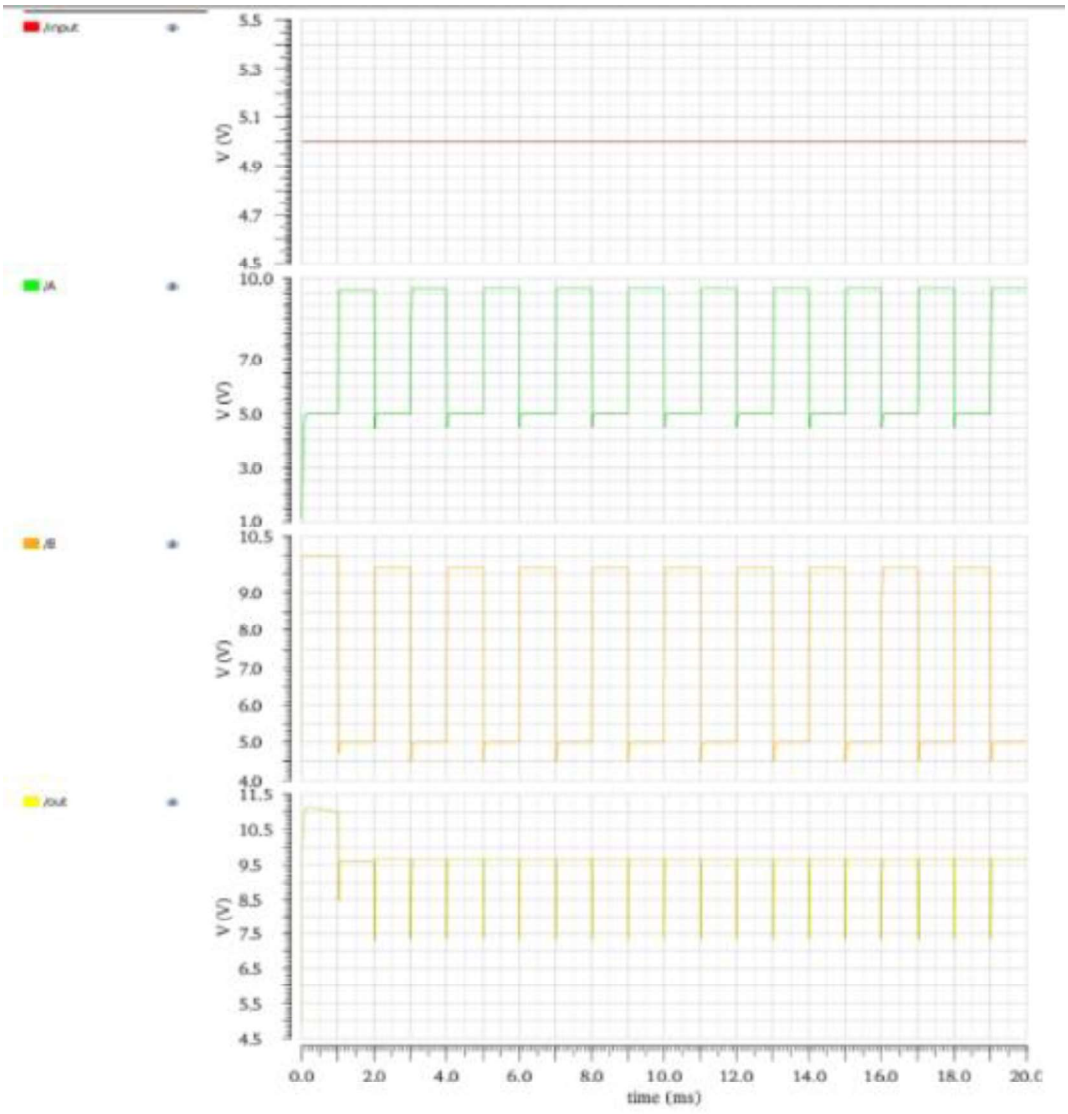

Figure 34 Unit cell Output for Positive Output Voltage

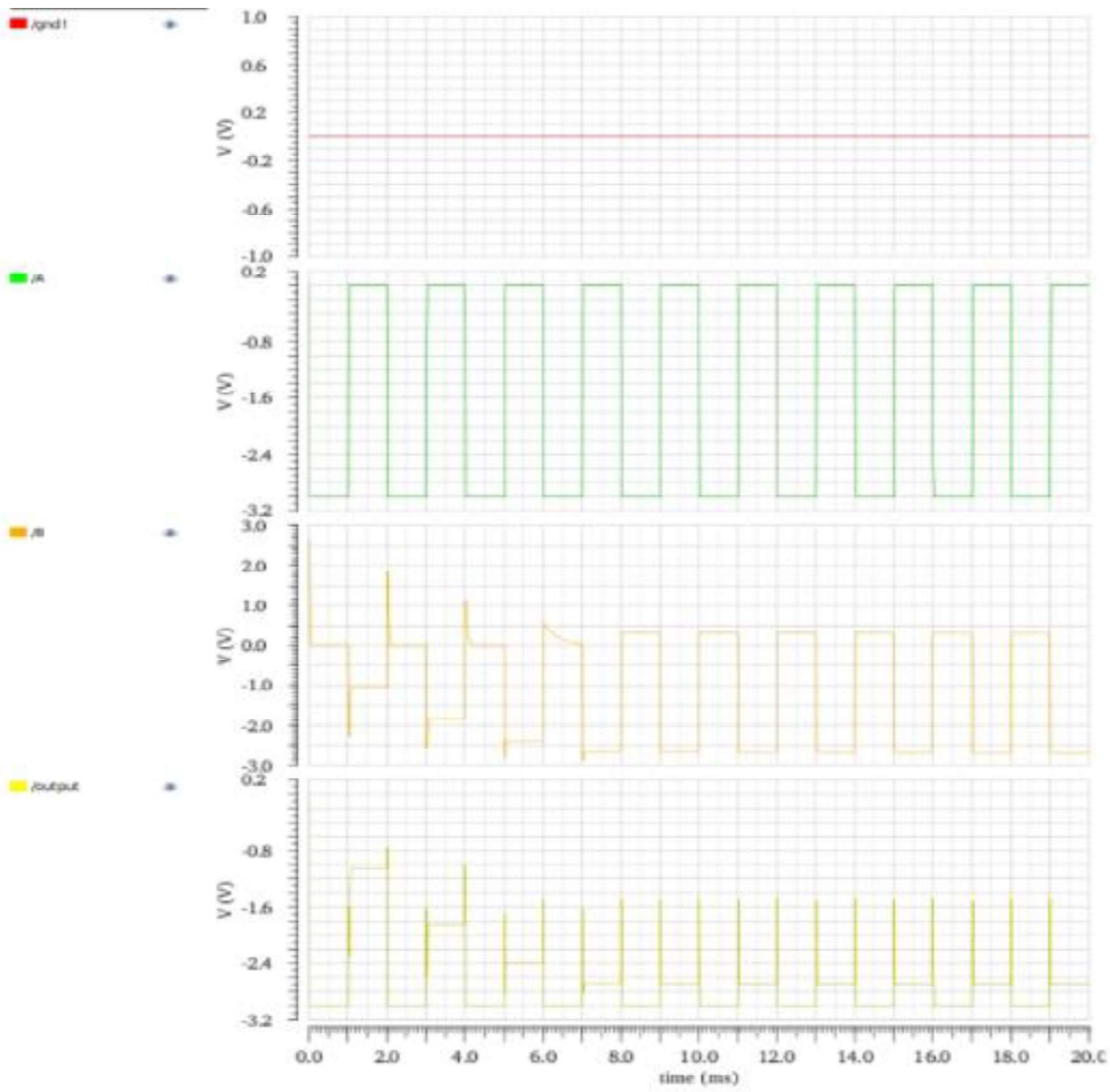

Figure 35 Unit cell Output for Negative Output Voltage

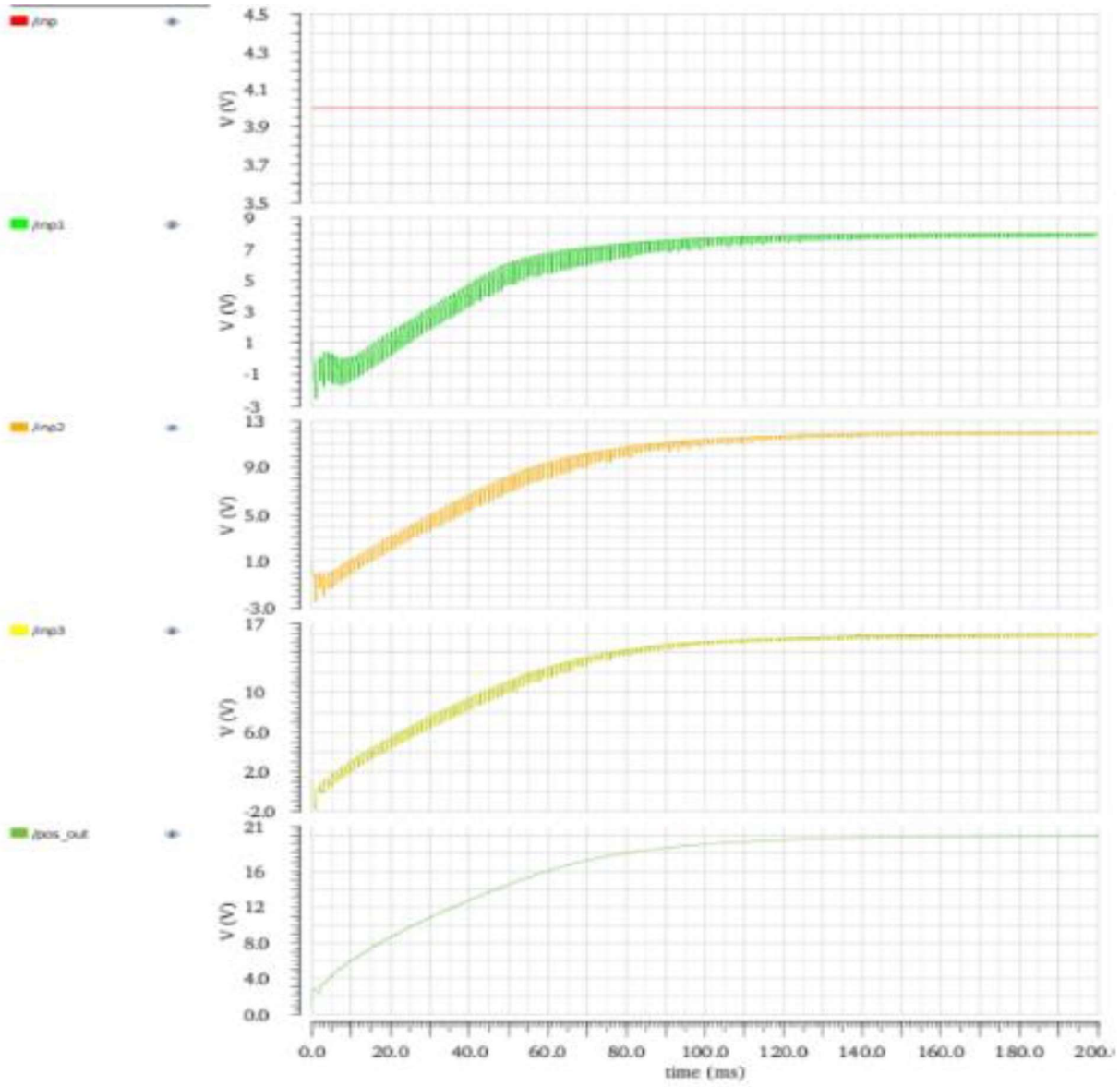

Figure 36 Charge pump circuit output Positive 20V

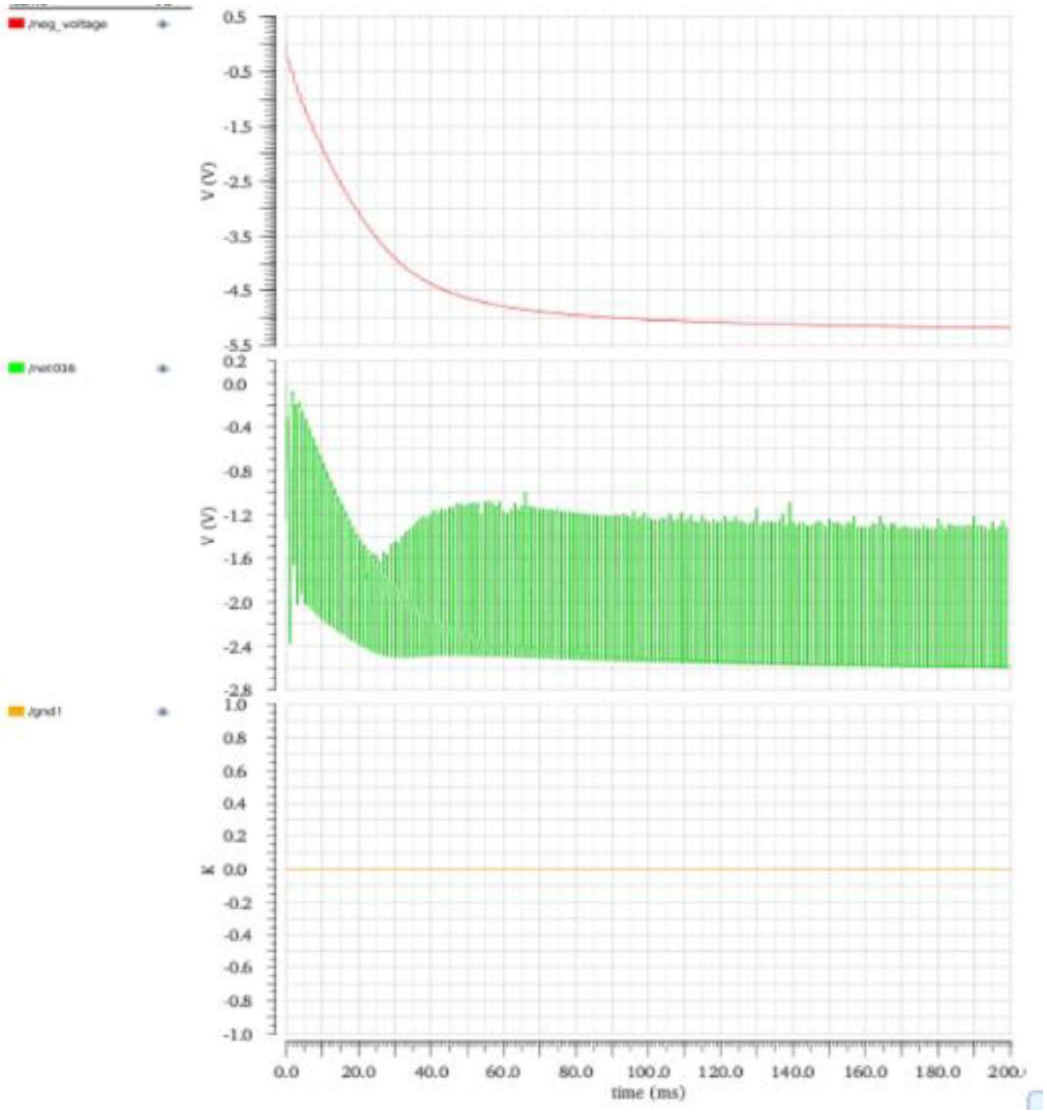

Figure 37 Charge pump circuit output Positive 20V

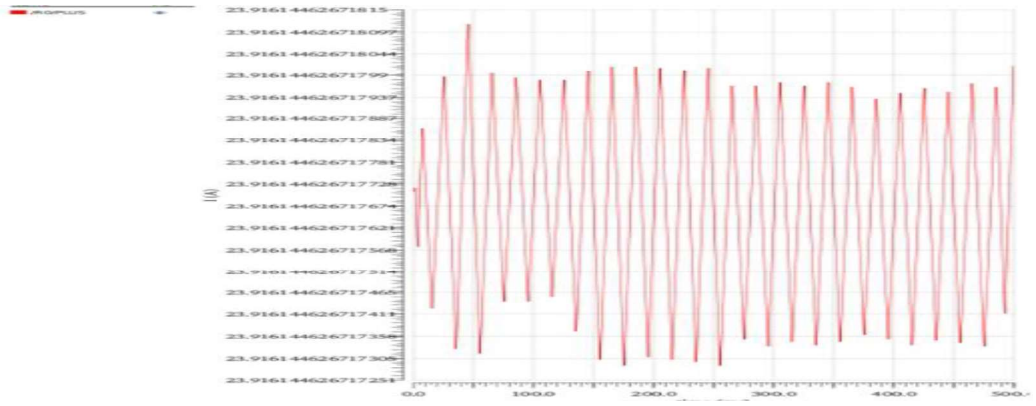

Figure 38 Charge Pump circuit current

11. Result

This thesis discuss about a voltage multiplier stage, which can be used to generate either positive voltage or negative voltage. A NMOS based voltage multiplier scheme is designed and implemented that can be used to generate positive and negative voltages. Due to use of only NMOS transistors, bulk management is very easy in negative voltage case. For positive voltage case, voltage efficiency achieved is 89% and for negative voltage case, voltage efficiency achieved is 83%. This feature of generating both positive and negative voltages from a single circuit makes this idea very attractive and can be used to reduce chip area in many applications specifically in Non-Volatile Memories.

12. Conclusion

As the fundamental building elements, power semiconductor switching devices are the most important components in a power electronic system. in this report we have designed a gate driver circuit for SiC Power MOSET. The main purpose of this work is to demonstrate the preliminary design of high-performance gate drive module for high-speed switching applications. With the help of wide bandgap power devices such as SiC MOSFET, we can achieve low loss and fast switching capabilities. But the problem with the SiC MOSFET is that it requires a high gate voltage (14v in this work) to operate and there are some special problems in the application of SiC MOSFETs including lower short circuit withstand time, higher voltage, and current transient rate at switching. But providing this voltage and interfacing the same with the high-power module on-chip is a challenging task. In order to address this issue we proposed a compact charge-pump architecture. This charge-pump circuit utilizes the cross-coupled connection of MOSFETs and capacitors, with the help of this we generated 14V preliminarily, which could be enhance 20V with minor design modification. The key objective was to introduce the compact integrable charge pump architecture which has been served in this work. However, the present PDK is unsupportive for this higher breakdown voltage, the BCD (Bipolar-CMOS-DMOS) is the most suitable for this purpose and could be used in further development. For overcurrent protection, the 'Dsense method' of detecting overcurrent has been proposed in this work. Finally for high switching speed and to reduce switching loss we proposed a driver architecture that has 6 NMOS driver transistors on a chip whose activation patterns are controlled by 3-bit digital signals and a 20 MHz clock (PWM). also, we designed one control logic circuit to take for proper driving operation.

SiC circuits will have massive impact on future power electronics systems on a vast gamut of applications decreasing their size and cost, and increasing their efficiency, robustness and reliability. The gate driver circuit is a very important part of such systems directly affecting the systems prominent performance parameters like overall size, efficiency, and cost. Due to material properties of Silicon, Silicon and Silicon on Insulator technologies are unlikely to offer advantageous circuits beyond the 300 °C operating temperatures and for high-power switching applications. SiC, however, with its superior properties is a very promising technology for these applications.

The presented work in this thesis comprises a gate driver in SiC technology which can operate beyond 400 °C temperature range and switch at high frequencies beyond 500 kHz. The only other SiC gate driver developed to date has rise and fall times that are more than three times greater than the presented gate driver in this thesis and clipped final output voltage [27]. Several new circuit topology and new design and layout approaches were employed to develop this gate driver to overcome several constraints imposed by the fledgling SiC process. The novel circuit topologie and approaches presented in this thesis can be used in any other present or future NMOS only process to overcome process limitations and strictures.

The fabricated gate driver was tested and found to be operable at temperatures ranging from 25 °C to beyond 400 °C with only slight variation in performance parameters. The rise and fall times with a SiC Power MOSFET load, which is a larger load than a 4 pF capacitor, was measured to be as low as 45 ns and 41 ns respectively with power dissipations of only about 6 W at a 500 kHz switching frequency. The propagation delay is less than 200 ns which is the targeted specification.

13. References

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