Introduction to simulation model PROFET™ +2 12 V

PROFET™ +2 12 V BTS7xxxx-nEmy

About this document

Scope and purpose

This document outlines the main features of **PROFET™ +2 12 V BTS7xxxx-nEmy** by means of its digital twin, referred to as simulation model, in typical application setups aiming to be an easy, time-efficient and cost-effective solution for exploring device capabilities and integration in complex applications.

Information covered in this document does not substitute datasheet content and shall be regarded as complementary to it. For a more precise description of the device and its features, refer to the datasheet.

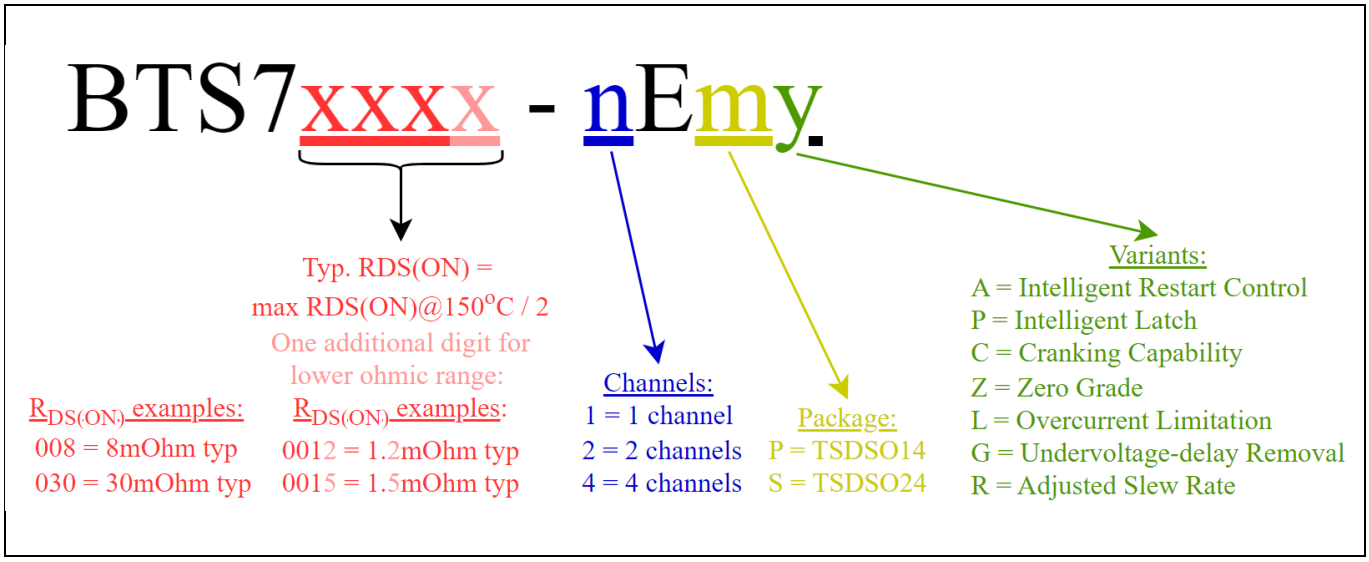

Figure 1 PROFET™ +2 12 V Naming conventions

Intended audience

This application note, along with the simulation model itself, offers an interactive solution targeted at anybody who aims to explore the functionality and “what if” scenarios for the **BTS7xxxx-nEmy** device.

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1 Details of the delivery package

The package contains the setup using the transient Spice/MAST model for the Infineon **BTS7xxxx-nEmy**:

- **BTS7xxxx-nEmy_encrypted**: code source file:
  - ".lib" for OrCAD PSpice and LTspice
  - ".sin" for SaberRD
- Schematic symbol view for the graphical user interface:
  - ".olb" for OrCAD PSpice
  - ".asy" for LTspice
  - ".ai_sym" for SaberRD
- Project/schematic file(s) containing the test setups:
  - ".opj" and ".dsn" for OrCAD PSpice
  - ".asc" for LTspice
  - ".ai_sym", ".ai_dsn" and ".ai_settings" for SaberRD

The model library is encrypted to protect Infineon IP.

Note: The package also includes additional model libraries and schematic symbol views that are useful for the test bench, such as MOSFETs, diodes, and LEDs.

Application test benches:

- **Switching resistive loads**: normal operation

Note: all model libraries are already configured, and the project is ready for use.

2 Simulation model features

The simulator enables you to:

- Perform transient simulations: observe and analyze transient device response to different stimuli. The number of stimuli and probes is unlimited
- Measure the device's electrical parameters in typical conditions with increased precision (compared to the default values of the simulator) at small resolution (for example, 100 ns / 1 µV / 1 µA)
- Integrate the simulation model into complex applications and explore new possibilities
- Explore the main features of the real device (for more information, refer to the datasheet):
    - Typical static and dynamic behavior
    - Reverse ON for low power dissipation in reverse polarity
      (not applicable for BTS7120-2EPx, BTS7200-2EPx and EPL devices)
    - Switch ON capability while inverse current condition (Inverse ON)
    - Absolute and dynamic temperature limitation with controlled restart/reactivation
    - Overcurrent protection (tripping) with intelligent restart control/intelligent latch (not applicable for EPL devices)
    - Undervoltage shutdown
    - Overvoltage protection for output pin
    - Overvoltage protection for sense output
    - Proportional load current sense
    - Open load in ON and OFF states
    - Temperature dependency for ON-state resistance
    - Device self-heating model (four types of thermal networks)
    - Capacitive Load Switching mode (for ESP and EPL devices only)
    - Overcurrent limitation (fixed threshold for EPL devices only)
- Obtain results in the shortest time possible at zero error cost, without harm to physical components. The simulation can also be run by anyone such as engineers and students without risk of damage

To keep the usability and simulation speed in a reasonable range, the simulation model does not cover all features of the real device:

- Possible thermal dependencies are not included in thermal behavior
- No ESD, EMC, AC, DC, and Monte Carlo analysis simulation capability
- Possible convergence issues for using DC sources, steep ramps or high frequency sources within the setup

The simulation of the thermal behavior of the real device provides an accurate measurement of junction temperature and influences between power transistors for multichannel devices. For more information, refer to Thermal behavior

2.1 Thermal behavior

The simulation model contains 4 junction-to-ambient thermal networks associated to different types of JEDEC standards (**Figure 2**).

Optional on request: 1 junction-to-package thermal network that allows an external heat sink connection (**Figures 3 and 4**), to be used for custom printed circuit board (PCB) cooling.

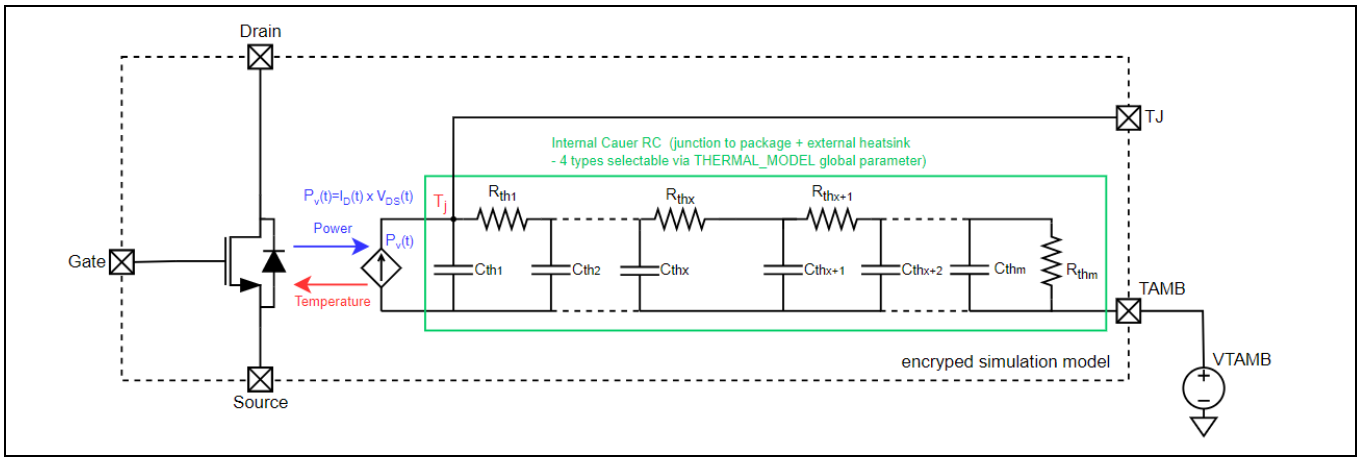

Figure 2 Schematic showing the junction-to-ambient thermal network concept

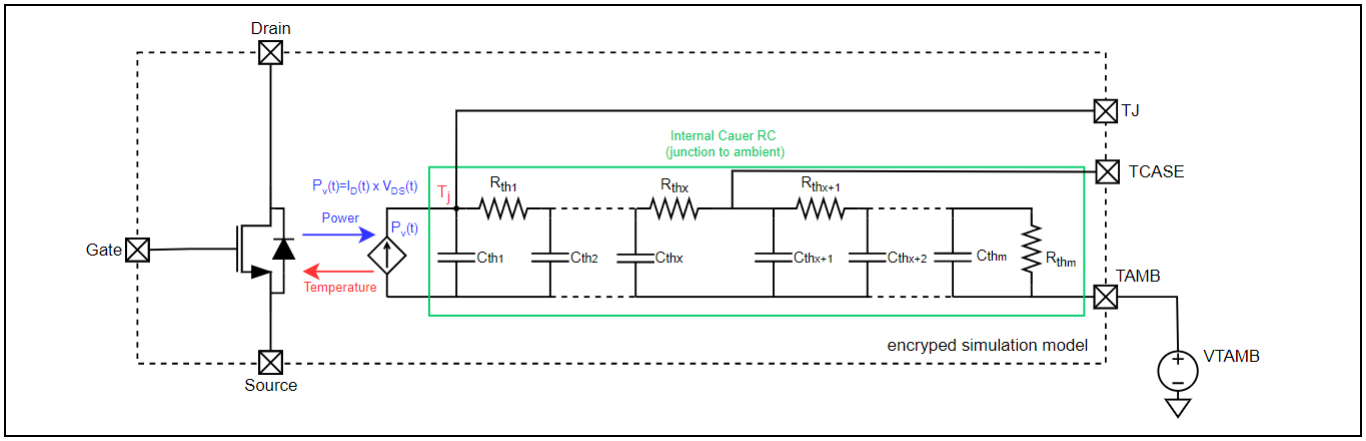

Figure 3 Schematic showing junction-to-ambient thermal network with TCASE concept *

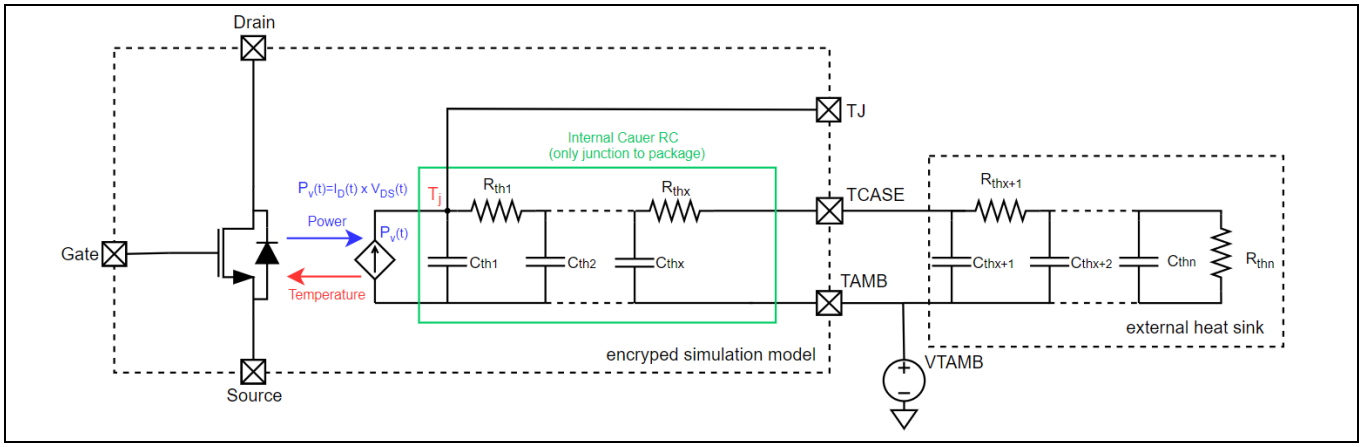

Figure 4 Schematic showing the junction-to-package thermal network concept*

To choose one of them, change the value of the THERMAL_MODEL parameter (for more information on global/local parameters, refer to the **GettingStarted** file for the specific simulator) on the test bench:

- THERMAL_MODEL=0: no thermal network TJ=TAMB
- THERMAL_MODEL=1: P = 1 W; T = 85°C; PCB type: 1s0p 300mm2
- THERMAL_MODEL=2: P = 1 W; T = 85°C; PCB type: 1s0p 600mm2
- THERMAL_MODEL=3: P = 1 W; T = 85°C; PCB type: 1s0p footprint
- THERMAL_MODEL=4: P = 1 W; T = 85°C; PCB type: 2s2p with thermal via
- Optional*: THERMAL_MODEL=5: P = 1 W; T = 85°C; Junction to case thermal model - connect external heat sink between TCASE and TAMB

P = dissipated power on power transistor; T = ambient temperature

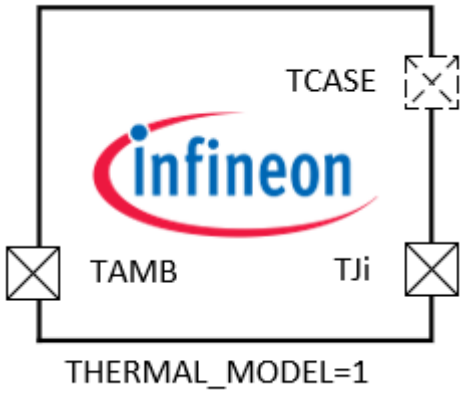

Figure 5 Thermal model parameter

The ambient temperature of the entire chip can be set by connecting a voltage source to the TAMB input pin. Be aware that modifying the simulation temperature via the **TNOM** parameter does not influence in any way the provided simulation model.

Absolute temperature junction ($\mathbf{T_{Ji}}$) is always the sum of:

- The ambient temperature ($\mathbf{T_{AMB}}$)
- The temperature due to self-heating of the power stage ($\mathbf{T_{PS}}$)
- The influences of all the other channels (in case of multichannel devices, $\mathbf{T_{CH}}$), n represents the number of channels and the index i goes from 0 up to n-1 :

$$T_{Ji} = T_{AMB} + T_{PSi} + \sum_{x=0,x\neq i}^{n-1} T_{CHx}$$

It is recommended to leave the TJ pin open (no external connection).

The thermal electrical convention is: 1 V = 1°C.

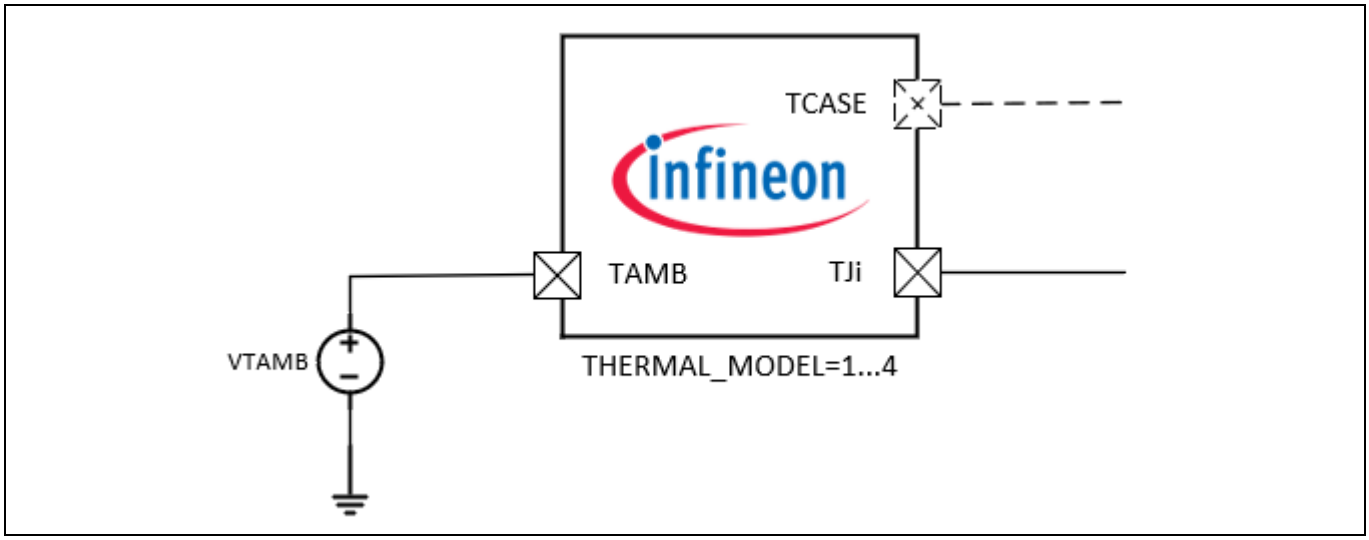

Figure 6 Configuration of TAMB, TCASE* and TJ pins for THERMAL_MODEL=1...4;

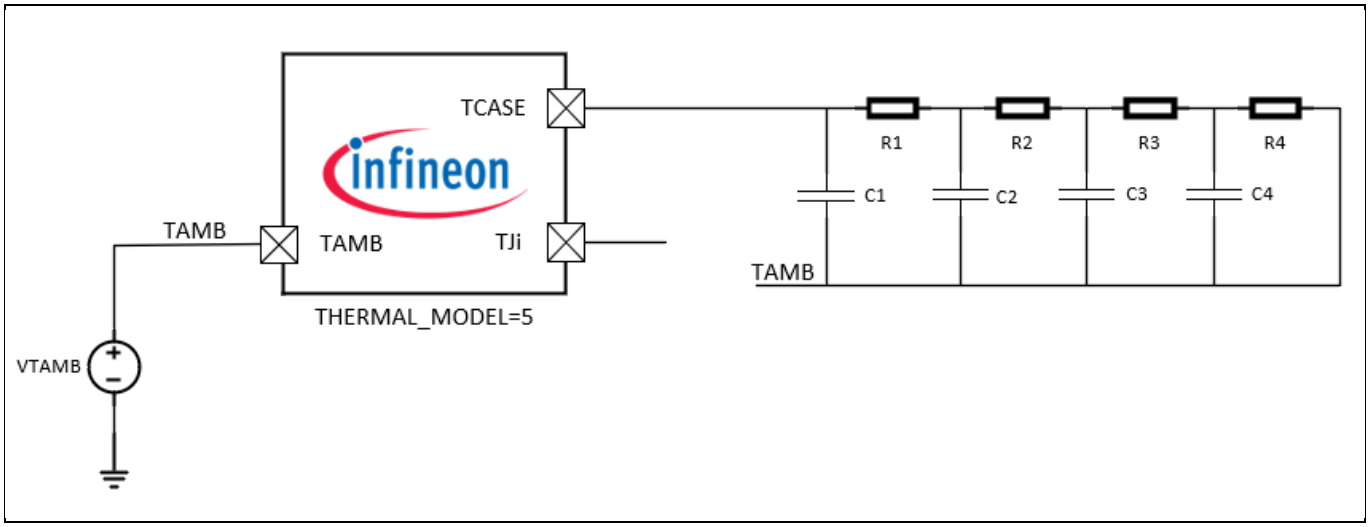

Figure 7 Configuration of TAMB, TCASE and TJ pins for THERMAL_MODEL=5 *

***Not applicable to all product simulation models**

3 Model performance

3.1 Switching resistive loads

The generic test bench switches resistive load(s). This load switching can be used as a starting point for different configurations. Note that depending on the number of channels (n), the application test bench changes, the index i goes from 0 up to n-1. For multichannel devices, an additional input pin, DSEL is present (for more information, refer to the product datasheet).

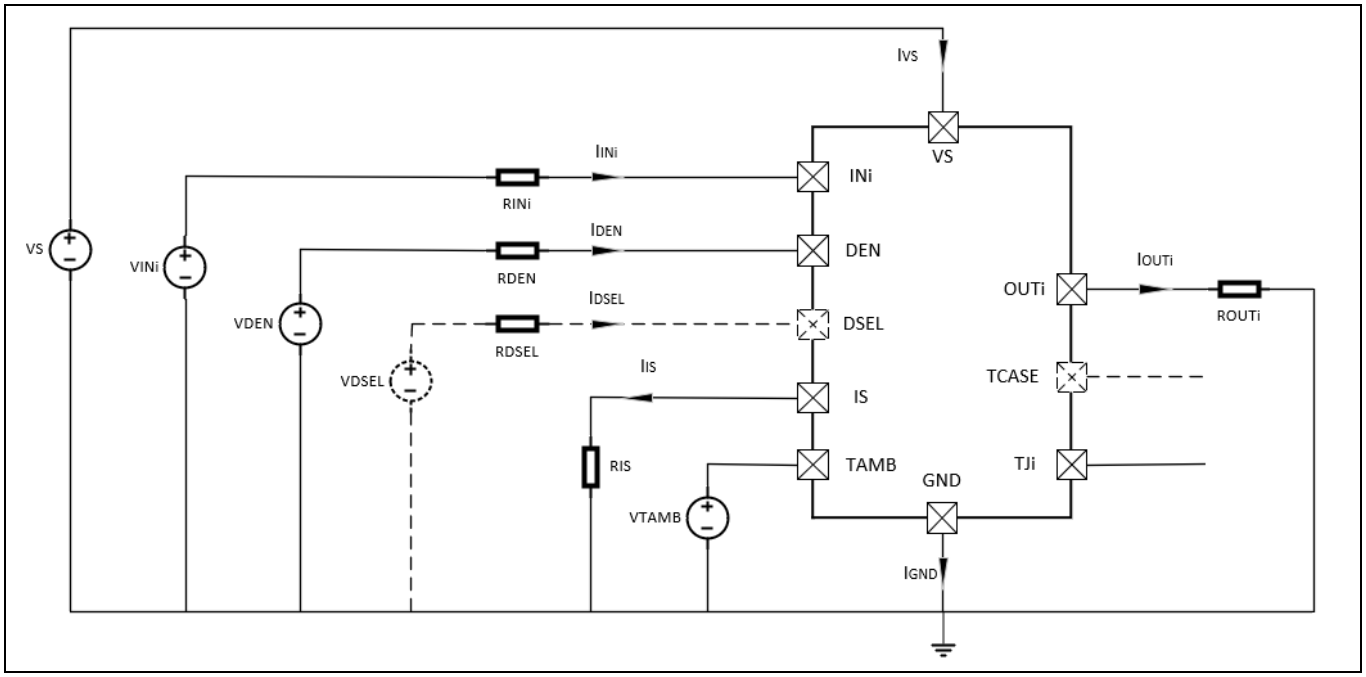

Figure 8 Application test bench

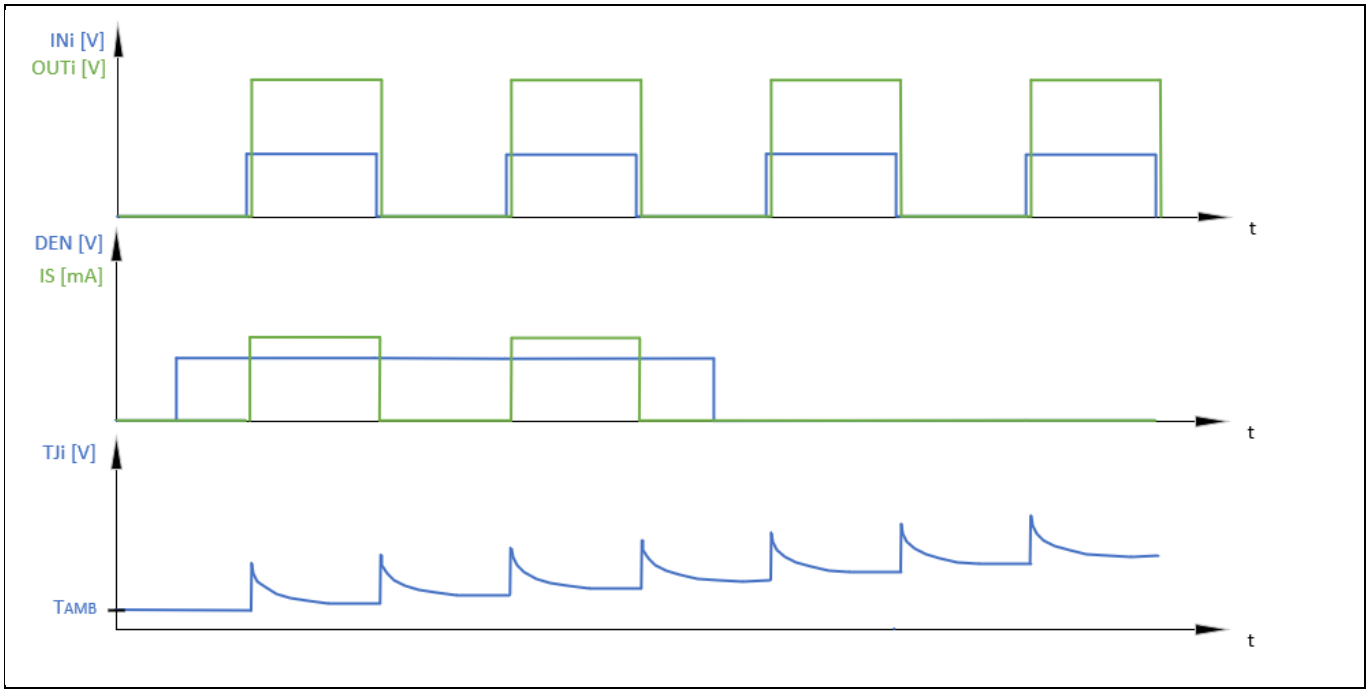

Figure 9 Simulation results

Revision history

Document version	Date of release	Description of changes
Rev.1.30	2024-03-12	Minor text changes
Rev.1.20	2024-01-24	Figure 1 updated Minor text changes
Rev.1.10	2022-12-07	Figures 1 to 9 updated Minor text changes Disclaimer added to the table of contents Updated formula for junction temperature Updated title
Rev.1.00	2022-03-09	Initial version created

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