

MOSFET – Power, Single N-Channel

40 V, 0.48 mΩ, 533 A

NVMTS0D6N04C

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Wettable Flank Plated for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25 °C	I _D	533	A
		T _C = 100 °C		377	
Power Dissipation R _{θJC} (Note 2)	Steady State	T _C = 25 °C	P _D	245	W
		T _C = 100 °C		122.7	
Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25 °C	I _D	76	A
		T _A = 100 °C		54	
Power Dissipation R _{θJA} (Notes 1, 2)	Steady State	T _A = 25 °C	P _D	5.0	W
		T _A = 100 °C		2.5	
Pulsed Drain Current	T _A = 25 °C, t _p = 10 μs		I _{DM}	900	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	–55 to +175	°C
Source Current (Body Diode)			I _S	204.5	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 53 A)			E _{AS}	2035	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

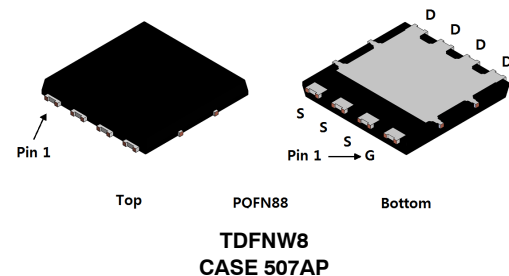
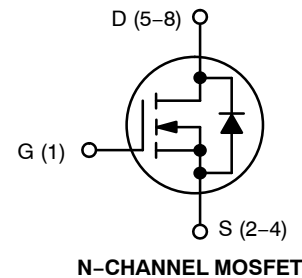
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

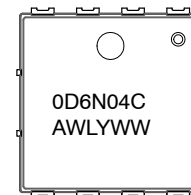
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.61	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	30.2	

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.48 mΩ @ 10 V	533 A



MARKING DIAGRAM



- A = Assembly Location
 WL = 2-digit Wafer Lot Code
 Y = Year Code
 WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMTS0D6N04C

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, ref to 25 °C		13.19		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25 °C		10	μA
			T _J = 125 °C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 250 μA, ref to 25 °C		-8.28		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 50 A		0.39	0.48	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 50 A		233		S
Gate Resistance	R _G	T _A = 25 °C		1.0		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 20 V		11800		pF
Output Capacitance	C _{OSS}			7030		
Reverse Transfer Capacitance	C _{RSS}			199		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A		187		nC
Threshold Gate Charge	Q _{G(TH)}			29.7		
Gate-to-Source Charge	Q _{GS}			46.6		
Gate-to-Drain Charge	Q _{GD}			38.2		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 20 V, I _D = 50 A, R _G = 2.5 Ω		33.6		ns
Rise Time	t _r			27.9		
Turn-Off Delay Time	t _{d(OFF)}			86.0		
Fall Time	t _f			32.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 50 A	T _J = 25 °C		0.76	1.2	V
			T _J = 125 °C		0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A			105		ns
Charge Time	t _a				60		
Discharge Time	t _b				45		
Reverse Recovery Charge	Q _{RR}				274		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

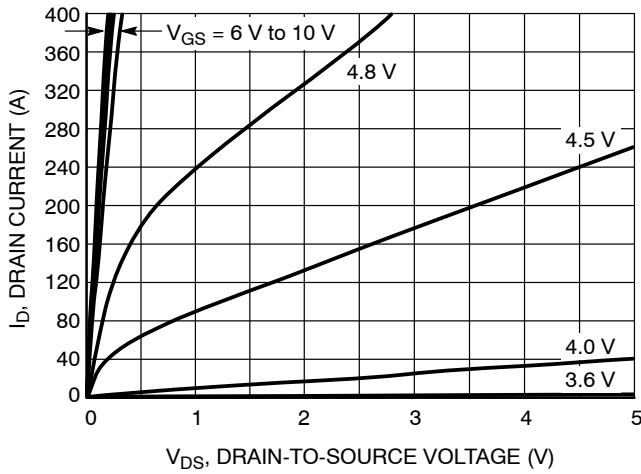


Figure 1. On-Region Characteristics

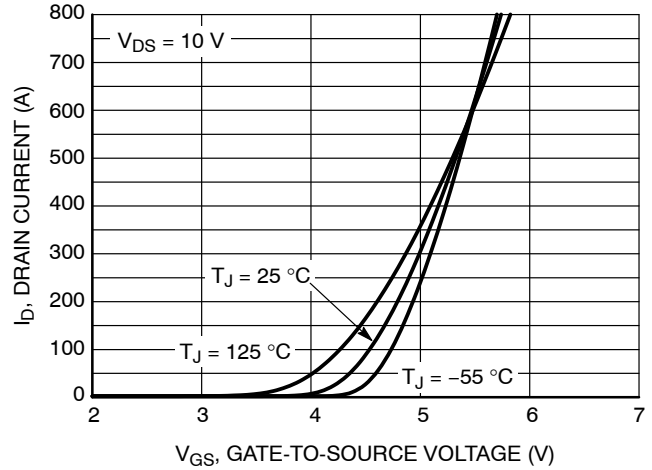


Figure 2. Transfer Characteristics

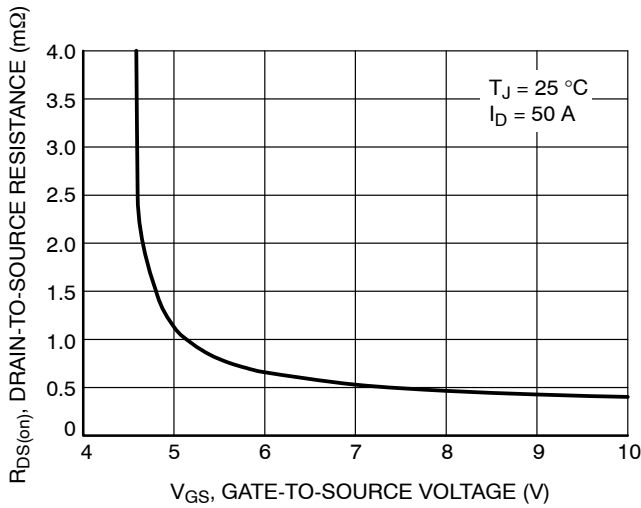


Figure 3. On-Resistance vs. Gate-to-Source Voltage

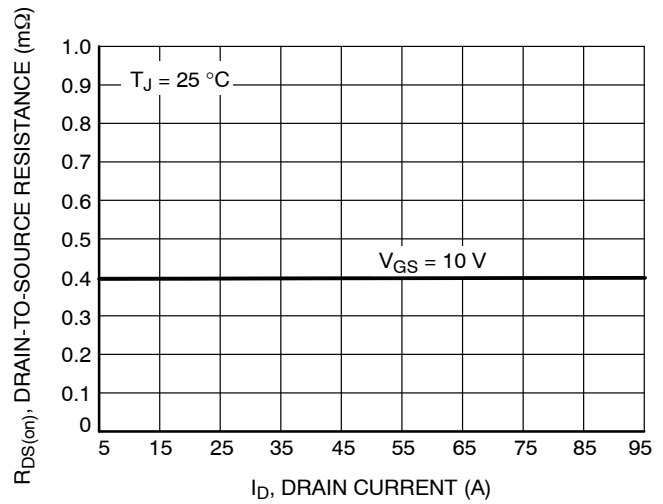


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

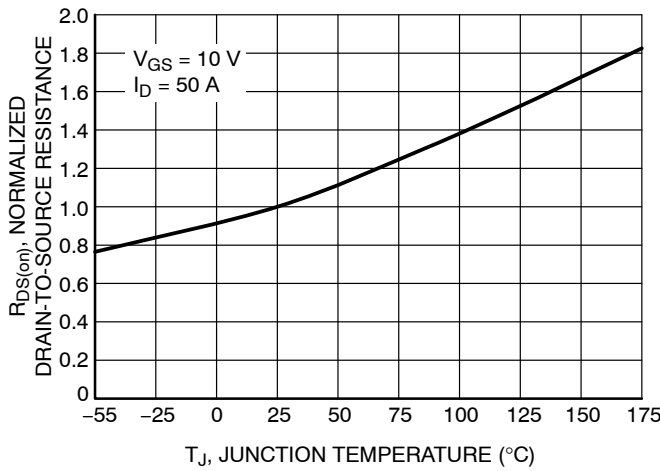


Figure 5. On-Resistance Variation with Temperature

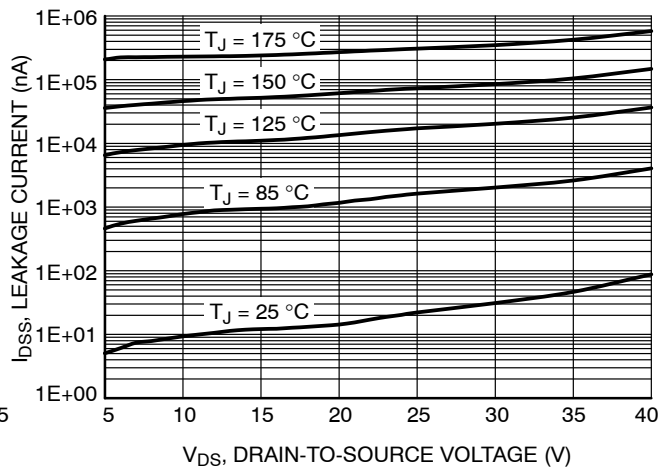


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

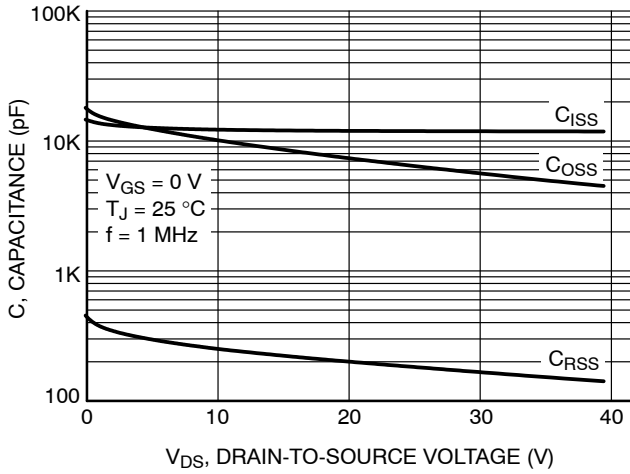


Figure 7. Capacitance Variation

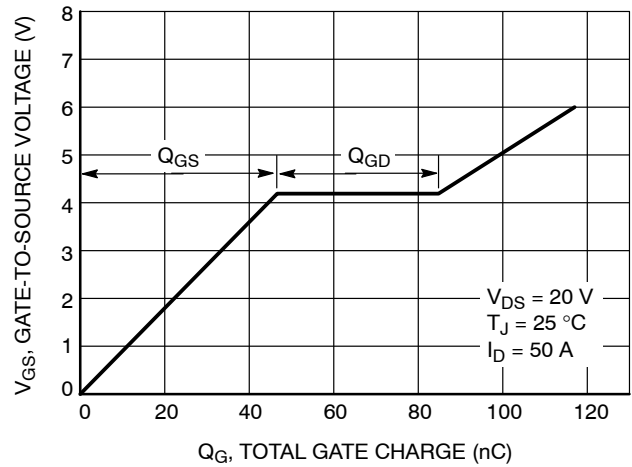


Figure 8. Gate-to-Source Voltage vs. Total Charge

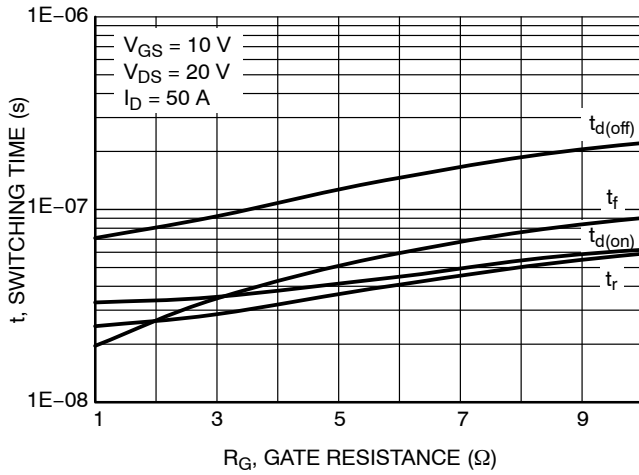


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

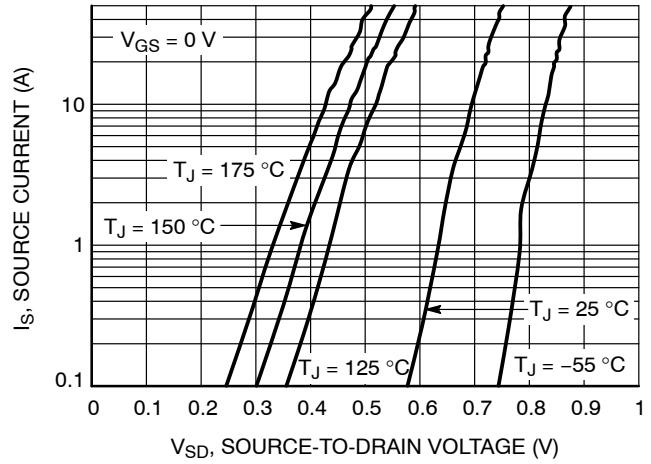


Figure 10. Diode Forward Voltage vs. Current

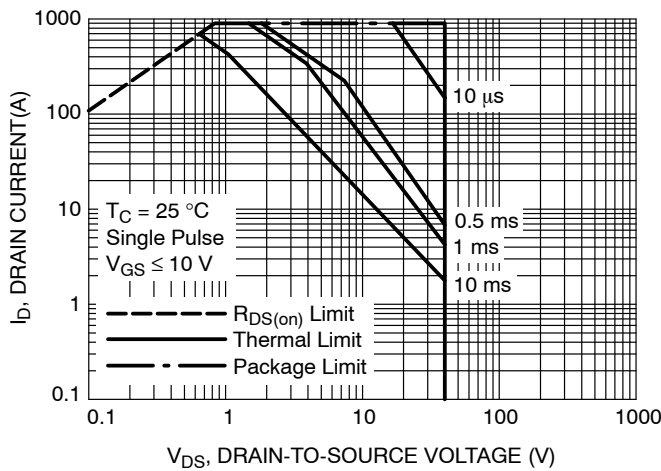


Figure 11. Maximum Rated Forward Biased Safe Operating Area

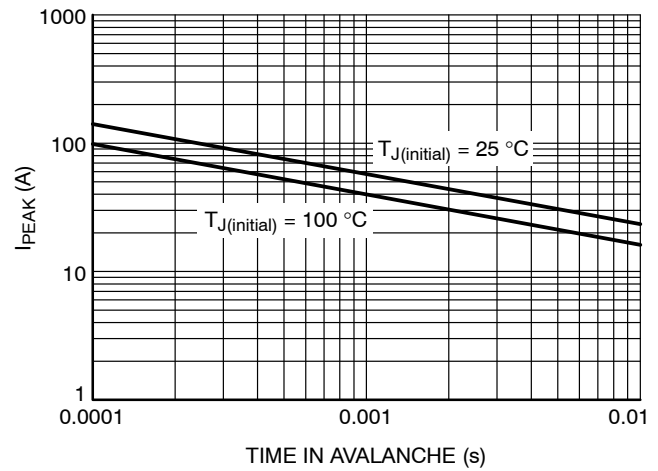


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

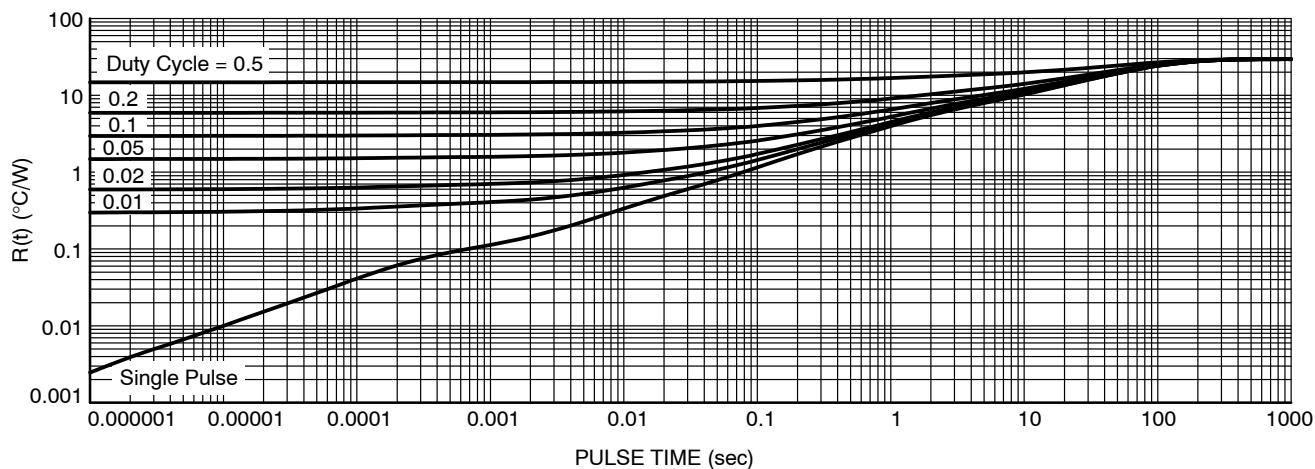


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

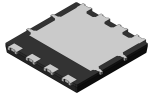
Device	Marking	Package	Shipping [†]
NVMTS0D6N04CTXG	0D6N04C	DFNW8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

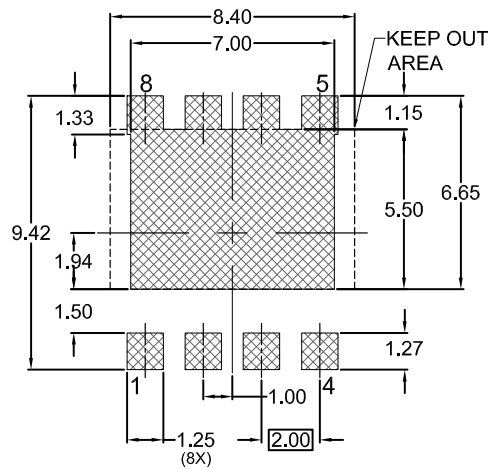
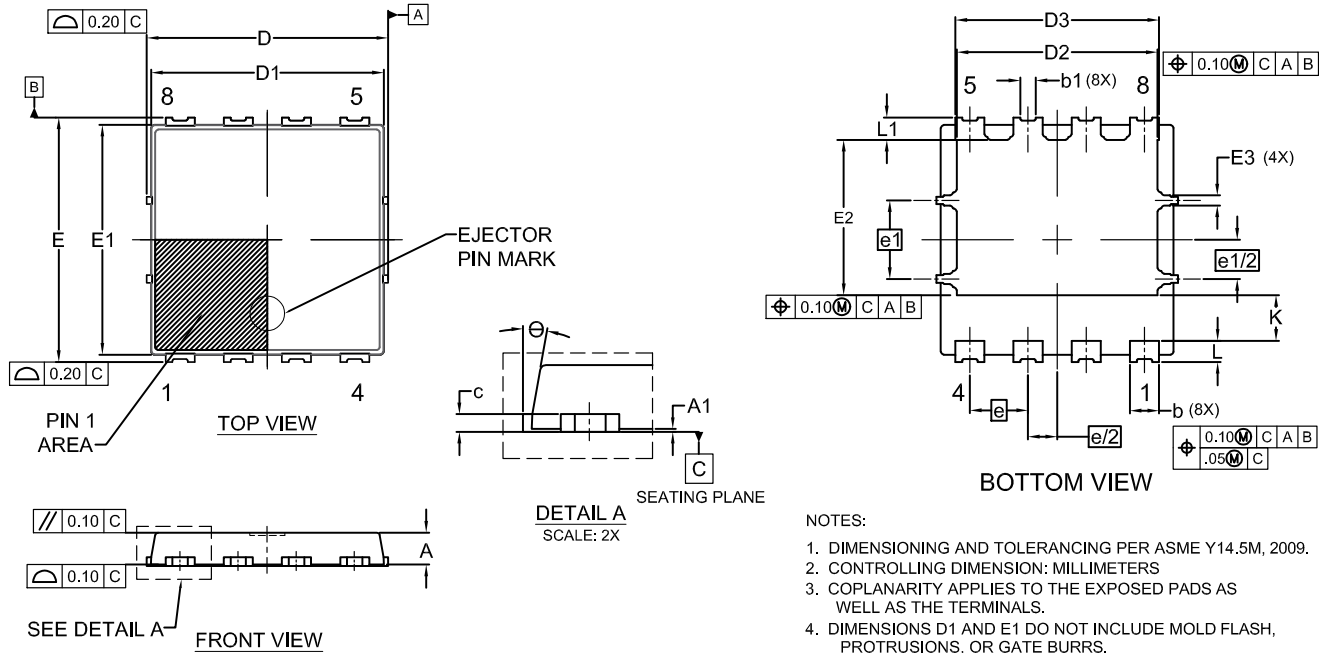
REVISION HISTORY

Revision	Description of Changes	Date
4	Edits to figure 7 labeling	7/3/2025

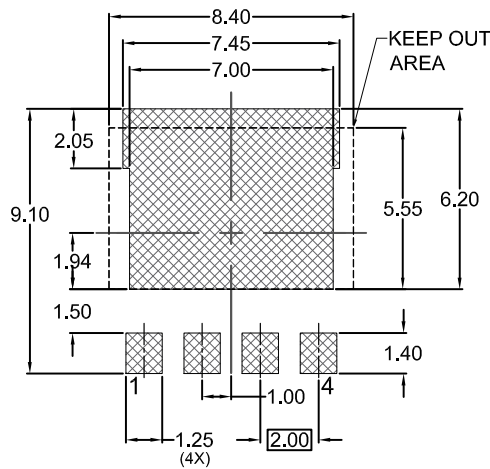
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.


TDFNW8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE E

DATE 08 MAY 2024



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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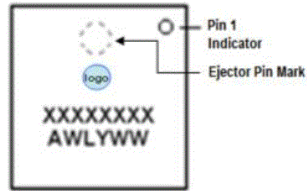
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TDFNW8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE E

DATE 08 MAY 2024

**GENERIC
MARKING DIAGRAM***



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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