The Unified I-V Model of BSIM3v3

For a complete summary of all equations of the BSIM3v3.2.4 model, please refer to the original documentation from University of California at Berkeley (see References to order this paper). The main equations of the BSIM3v3.3.0 model are shown together with a graphical representation for a better understanding of the model.

Please use the models *BSIM3_DC_Tutorial.mdl, BSIM3_CV_Tutorial.mdl, BSIM3_AC_Noise_Tutorial.mdl,* or *BSIM3_Temp_Tutorial.mdl* provided with the BSIM3 Modeling Package to visualize most of the model parameters influences onto the device diagrams. Load the file into IC-CAP to see how certain parameters affect the behavior of a deep submicron MOS transistor.

Threshold Voltage

The threshold voltage is one of the most important parameters of deep submicron MOS transistors and is affected by many different effects when the devices are scaled down into the region of 0.1 microns. The complete equation of the threshold voltage in BSIM3v3.3.0 is given below.

$$V_{th} = V_{Tideal} + \Delta V_{th(1)} + \Delta V_{th(2)} - \Delta V_{th(3)} - \Delta V_{th(4)} + \Delta V_{th(5)} - \Delta V_{th(6)} \quad (45)$$

The different parts of this complex equation are expressed by the following sub-equations in more detail:

$$\begin{aligned} V_{th} = {} & V_{th0} - K_1\sqrt{\Phi_s} \\ & + K_1\frac{T_{ox}}{T_{oxm}}\sqrt{\Phi_s - V_{bseff}} - K_2\left(\frac{T_{ox}}{T_{oxm}}V_{bseff}\right) \\ & + K_1\frac{T_{ox}}{T_{oxm}}\left(\sqrt{\left(1+\frac{Nlx}{L_{eff}}\right)} - 1\right)\sqrt{\Phi_s} \\ & - D_{VT0}\left[e^{\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)} + 2e^{\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)}\right](V_{bi} - \Phi_s) \\ & - D_{VT0w}\left[e^{\left(-D_{VT1w}\frac{W_{eff}L_{eff}}{2l_{tw}}\right)} + 2e^{\left(-D_{VT1w}\frac{W_{eff}L_{eff}}{l_{tw}}\right)}\right](V_{bi} - \\ & + (K_3 + K_{3b}V_{bseff})\frac{T_{ox}}{(W_{eff}+W_0)}\Phi_s \\ & - \left[e^{\left(-D_{sub}\frac{L_{eff}}{2l_{t0}}\right)} + 2e^{\left(-D_{sub}\frac{L_{eff}}{l_{t0}}\right)}\right](E_{ta0} + E_{tab}V_{bseff})V_{ds} \end{aligned} \quad (46)$$

Ideal Threshold Voltage

The basic equation of the threshold voltage is:

$$V_{Tideal} = V_{th0} = V_{FB} + \Phi_s + K_1\sqrt{\Phi_s} \quad (47)$$

$$(48)\quad \Phi_s = 2V_{tm0}\ ln\left(\frac{N_{ch}}{n_{i0}}\right) \text{ at } T = T_{nom}$$

$$(49)\quad V_{tm0} = \frac{k_B T_{nom}}{q}$$

where:

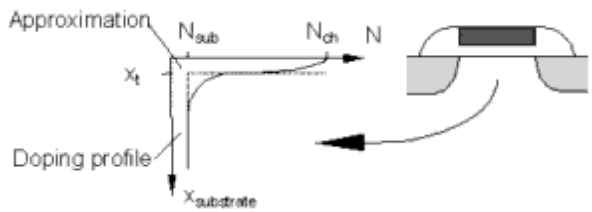
$V_{thideal}$	= ideal threshold voltage
V_{FB}	= flatband voltage
Φs	= surface potential
n_i	= $1.45 \bullet 10^{10}\ (T_{nom}/300.15)^{1.5}\ (21.5566 - E_{g0}/2V_{tmo})$
E_g0	= $1.16 - 7.02 \bullet 10^{-4}\ T_{nom}^2/(T_{nom} + 1108)$

This equation had been implemented into the first MOS simulation models assuming long and wide channels and uniform substrate doping. The following sections describe the effects that overlay this basic equation.

Non-Uniform Vertical Channel Doping

The substrate doping concentration N is not constant in the vertical direction of the channel, as shown in the following figure.

Figure 70 Vertical Doping Profile in the Channel



It is usually higher near the silicon to silicon dioxide interface than deeper in the substrate. This higher doping concentration is used to adjust the threshold voltage of the device. The distribution of impurity atoms inside the substrate is approximately a half Gaussian distribution, which can be approximated by a step function with NCH for the peak concentration in the channel near the Si-SiO_2 interface and Nsub in the deep bulk. XT is the depth where the approximation of the implant profile switches from NCH to NSUB. The non-uniform vertical channel doping affects the threshold voltage when a bulk source voltage is applied to the device and is represented here as the part $\Delta V_{th(1)}$ of the overall threshold voltage.

$$(50)\quad \Delta V_{th(1)} = K_1 \frac{T_{ox}}{T_{oxm}} \sqrt{\Phi_s - V_{bseff}} - K_2 \frac{T_{ox}}{T_{oxm}} V_{bseff}$$

$$(51)\quad K_1 = \gamma_2 - 2K_2\sqrt{\Phi_s - V_{bm}}$$

$$(52)\quad K_2 = \frac{(\gamma_1 - \gamma_2)(\sqrt{\Phi_s - V_{bx}} - \sqrt{\Phi_s})}{2\sqrt{\Phi_s}(\sqrt{\Phi_s - V_{bx}} - \sqrt{\Phi_s}) + V_{bx}}$$

$$(53)\quad \gamma_1 = \frac{\sqrt{2q\varepsilon_{si}N_{ch}}}{C_{ox}}$$

$$(54)\quad \gamma_2 = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}}$$

where:

V_{bx} = substrate bias voltage when the depletion width equals

$$X_t = \Phi_s - \frac{qN_{ch}X_t^2}{2\varepsilon_{si}}$$

V_{bm} = maximum substrate bias voltage

T_{oxm} = gate oxide thickness at which parameters are extracted

T_{ox} = default value of T_{oxm}

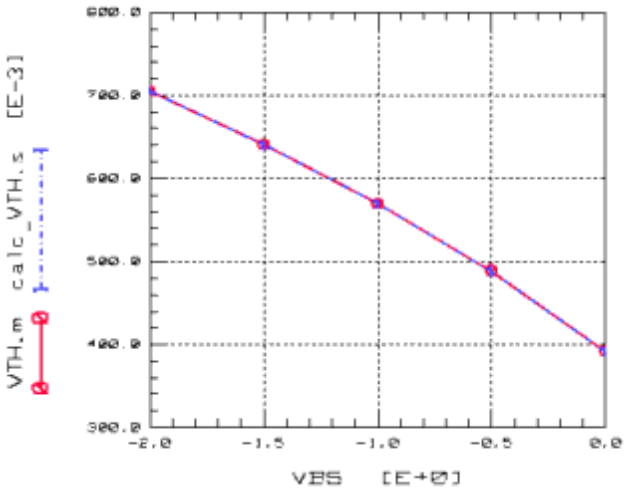
V_{bseff} = $V_{bc} + 0.5\left[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\right]$

$\delta 1$ = 0.001V

V_{bc} = $0.9\left(\Phi_s - \frac{K_1^2}{+K_2^2}\right)$

In BSIM3, either the model parameters K1 and K2 or NCH, NSUB, VBM or XT can be used to model this effect. The following figure shows the threshold voltage V_{th} as a function of the applied bulk voltage for a transistor with a large channel length and a wide channel width (LARGE).

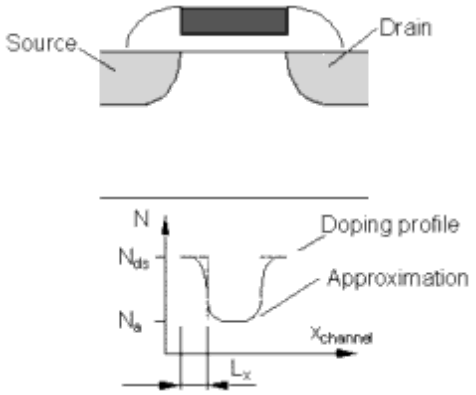
Figure 71 Threshold Voltage V_{th} as a Function of V_{bs}



Non-Uniform Lateral Channel Doping

The doping concentration N_{ds} near the drain and the source is higher than the concentration N_a in the middle of the channel. This is referred to as lateral non-uniform doping concentration and is shown in the following figure.

Figure 72 Lateral Doping Profile in the Channel



As the channel length becomes shorter, the lateral non-uniform doping will cause the threshold voltage to increase strongly because the average doping concentration in the channel becomes higher. This part of the threshold voltage is modeled with the parameter Nl_x and is represented by $\Delta V_{th(2)}$ as a part of the overall threshold voltage.

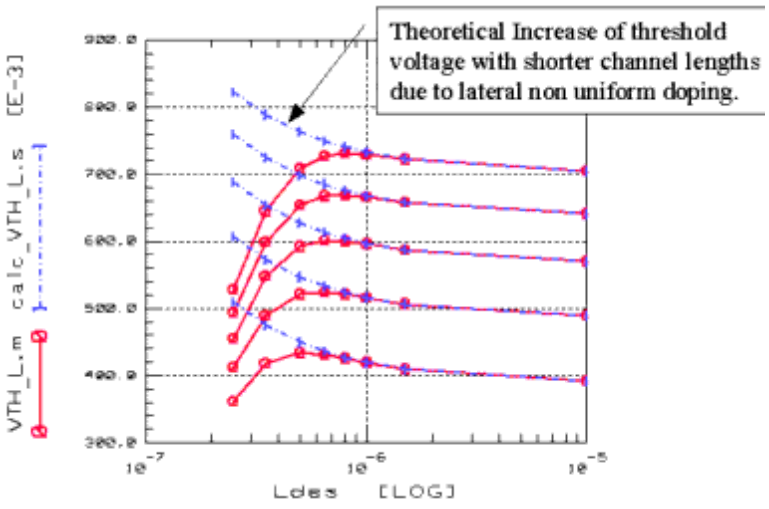
$$\Delta V_{th(2)} = K_1 \frac{T_{ox}}{T_{oxm}} \left(\sqrt{\left(1 + \frac{Nl_x}{L_{eff}}\right)} - 1 \right) \sqrt{\Phi_s} \quad (55)$$

where:

$$Nl_x = 2L_x(N_{ds} - N_a)/N_a$$

The following figure shows the influence of the non-uniform lateral doping on the threshold voltage as a function of gate length.

Figure 73 Threshold Voltage as a Function of Gate Length Due to Lateral Non-Uniform Doping



You can distinguish between the theoretical trace following Equation 55 and the real world ones with the short channel effect described in the next section.

Short Channel Effect

The threshold voltage of a long channel device is independent of the channel length and the drain voltage as it is shown in the equation of the ideal threshold voltage. The decreasing of device dimensions causes the so-called short-channel effects: threshold voltage roll-off and degradation of the subthreshold slope, that in turn increases the off-current level and power dissipation. The threshold voltage then depends on geometrical parameters like the effective channel length and the shape of the source-bulk and drain-bulk junctions. These device dimensions have a strong influence on the surface potential along the channel. A shallow junction with a weak lateral spread is desirable for the control of short-channel effects while the source and drain resistance must be kept as low as possible. However, a trade-off between the search for very shallow junctions and the degradation of the maximum achievable current through the parasitic resistance of low doped drain regions must be found.

Those effects can be shown in device simulators, where drift, diffusion, and additionally the hot electron behavior can be simulated. The following equations are responsible for the modeling of the short channel effect part $\Delta V_{th(3)}$ in the BSIM3 model:

$$\Delta V_{th(3)} = D_{VT0}\left[e^{\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)} + 2e^{\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)}\right](V_{bi} - \Phi_s) \quad (56)$$

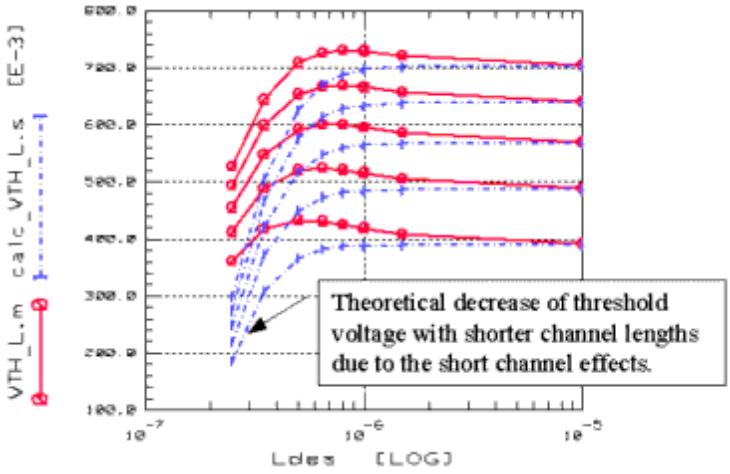
$$l_t = \sqrt{\frac{\varepsilon_{si} T_{ox} X_{dep}}{\varepsilon_{sio2}}}(1 + D_{VT2} V_{bseff}) \quad (57)$$

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}(\Phi_s - V_{bseff})}{qN_{ch}}} \quad (58)$$

where:

V_{bi}	built-in voltage of the PN junction between the source/drain and the substrate
	$= \frac{K_B T}{q} \ln\left(\frac{N_{ch} N_d}{n_i^2}\right)$
N_d	= source/drain doping concentration (or in the LDD regions) if they exist
DVT0, DVT1, DVT2	are parameters used to make the model fit different technologies

Figure 74 Influence of Short Channel Effects on the Threshold Voltage



For short channel lengths together with small channel widths, the following additional expression $\Delta V_{th(4)}$ is needed to formulate the threshold voltage:

$$\Delta V_{th(4)} = D_{VT0w}\left[e^{\left(-D_{VT1w}\frac{W_{eff}L_{eff}}{2l_{tw}}\right)} + 2e^{\left(-D_{VT1w}\frac{W_{eff}L_{eff}}{l_{tw}}\right)}\right](V_{bi}-\Phi_s) \quad (59)$$

where:

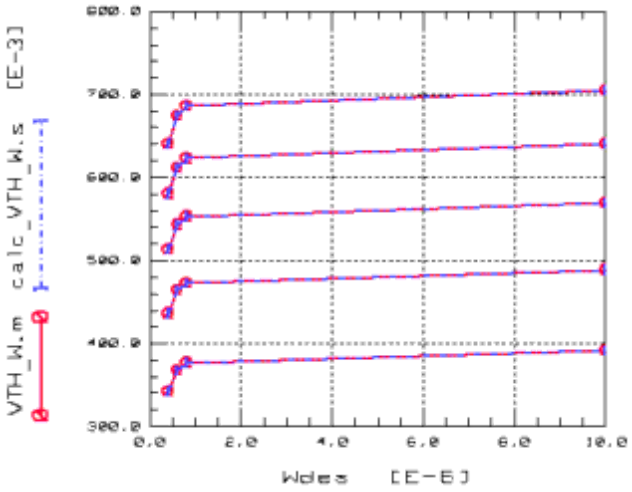
$$l_{tw} = \sqrt{\frac{\varepsilon_{si}T_{ox}X_{dep}}{\varepsilon_{sio2}}}(1+D_{VT2W}V_{bseff})$$

Narrow Channel Effect

All the effects on the threshold voltage are based on the non-uniformity along the channel length. Regarding the channel width, the depletion region is always larger due to the existence of fringing fields at the side of the channel. This effect becomes very substantial as the channel width decreases and the depletion region underneath the fringing field becomes comparable to the depletion layer formed from the vertical field. This additional depletion region results in an increase of the threshold voltage with smaller channel widths, which is expressed by $\Delta V_{th(5)}$.

$$\Delta V_{th(5)} = (K_3 + K_{3b}V_{bseff})\frac{T_{ox}}{(W_{eff}+W_0)}\Phi_s \quad (60)$$

Figure 75 Influence of Narrow Channel Effects on the Threshold Voltage



Threshold Voltage Reduction Through DIBL

The effect of the drain induced barrier lowering (DIBL) will be explained later. BSIM3 uses the following equation to model the DIBL effect in the threshold voltage:

$$\Delta V_{th(6)} = \left[e^{\left(-D_{sub}\frac{L_{eff}}{2l_{t0}}\right)} + 2e^{\left(-D_{sub}\frac{L_{eff}}{l_{t0}}\right)} \right](E_{ta0} + E_{tab}V_{bseff})V_{ds} \quad (61)$$

$$l_{t0} = \sqrt{\frac{\varepsilon_{si}T_{ox}X_{dep}}{\varepsilon_{sio2}}} \quad (62)$$

Carrier Mobility Reduction

BSIM3v3 provides 3 different equations for the modeling of the mobility reduction. They can be selected by the flag MOBMOD.

MOBMOD=1:

$$\mu_{eff} = \frac{\mu_o}{1 + (U_a + U_c V_{bseff})((V_{gsteff} + 2V_{th})/T_{ox}) + U_b((V_{gsteff} + 2V_{th})/T_{ox})^2} \quad (63)$$

MOBMOD=2:

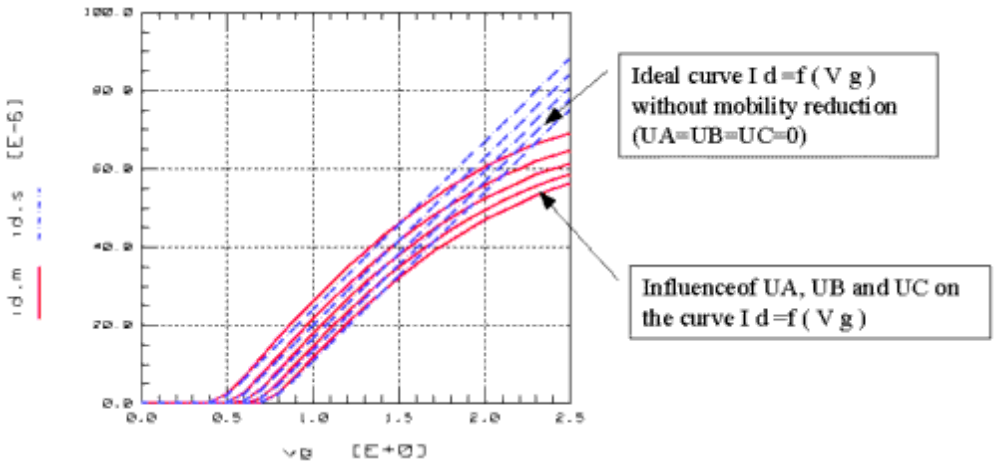
$$\mu_{eff} = \frac{\mu_0}{1 + (U_a + U_c V_{bseff})(V_{gsteff}/T_{ox}) + U_b(V_{gsteff}/T_{ox})^2} \quad (64)$$

MOBMOD=3:

$$\mu_{eff} = \frac{\mu_0}{1 + \left[U_a(V_{gsteff} + 2V_{th})/T_{ox} + U_b((V_{gsteff} + 2V_{th})/T_{ox})^2\right](1 + U_c V_{bseff})} \quad (65)$$

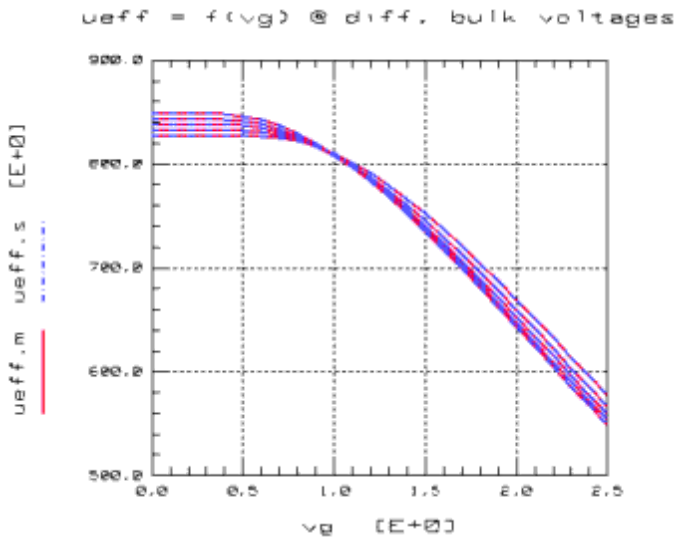
The influence of the mobility reduction parameters is demonstrated in the following figure where the simulated drain current with and without mobility reduction is shown.

Figure 76 Influence of Mobility Reduction



The following figure shows the effective mobility as a function of gate voltage and bulk-source voltage.

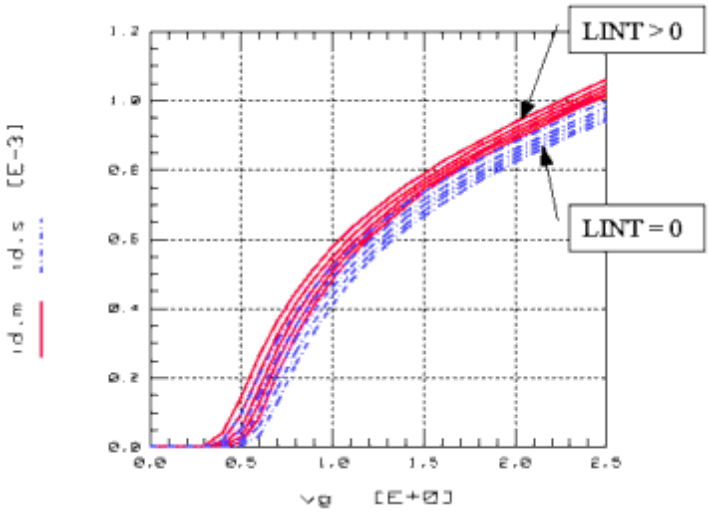
Figure 77 Effective Mobility$_{\mu eff}$ as a Function of Gate- and Bulk-Source-Voltage



Effective Channel Length and Width

Effective Channel Length

Figure 78 Influence of Channel Length Reduction on the Drain Current



The effective channel length is defined in BSIM3 as follows:

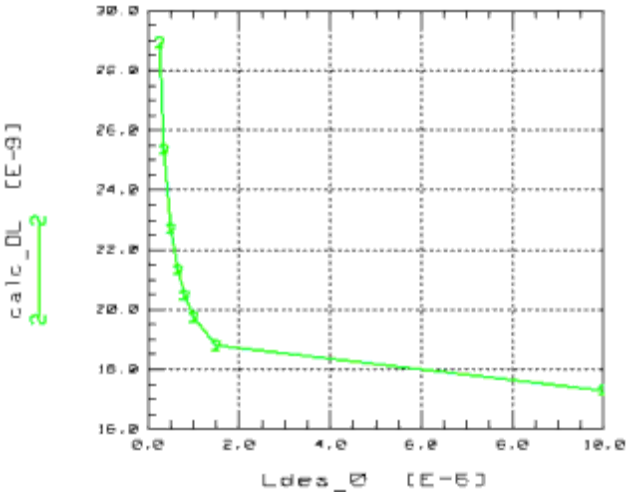
$$L_{eff} = L_{Designed} - 2dL \quad (66)$$

The channel length reduction on one side of the channel consists of several empirical terms as shown below:

$$dL = L_{int} + \frac{L_l}{L^{Lln}} + \frac{L_w}{W^{Lwn}} + \frac{L_{wl}}{L^{Lln} W^{Lwn}} \quad (67)$$

The use of the model parameters LL, LLN, LWN, LW and LWL is very critical because they are only used for fitting purposes. On the other hand, they may be needed to achieve a good fit over a large area of channel lengths especially for processes with a minimum designed gate length of less than 0.25µm. The previous figure shows the influence of the geometrical channel length reduction LINT on the drain current of a short channel transistor while The following figure represents the channel length reduction according to Equation 67.

Figure 79 Channel Length Reduction dL as a Function of Channel Length L



Effective Channel Width

The effective channel width is defined in BSIM3 as follows:

$$W_{eff} = W_{Designed} - 2dW \quad (68)$$

The channel width reduction on one side of the channel consists of several empirical terms as shown below:

$$dW = W_{int} + \frac{W_l}{L^{Wln}} + \frac{W_w}{W^{Wwn}} + \frac{W_{wl}}{L^{Wln} W^{Wwn}} \quad (69)$$

The use of the model parameters WL, WLN, WWN, WW, and WWL is very critical because they are only used for fitting purposes. On the other hand, they may be needed to achieve a good fit over a large area of channel widths especially for processes with a minimum designed gate width of less than 0.25µm. The following figure shows the influence of the geometrical channel width reduction WINT on the drain current of a narrow channel transistor while Figure 81 represents the channel width reduction according to Equation 69.

Figure 80 Influence of Channel Width Reduction on the Drain Current

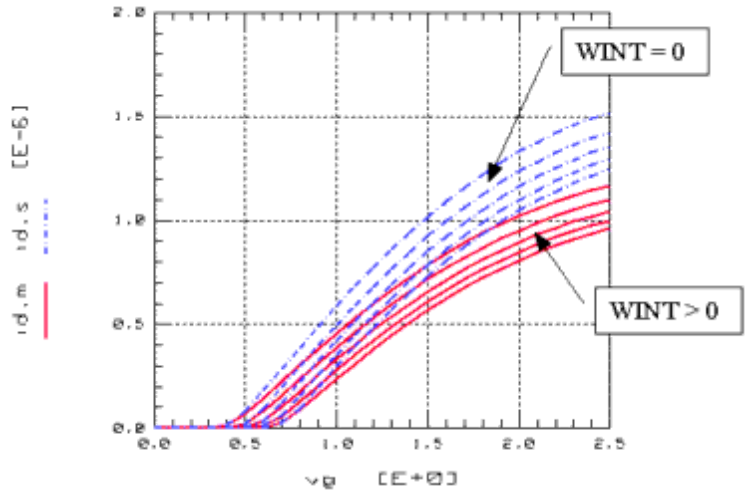
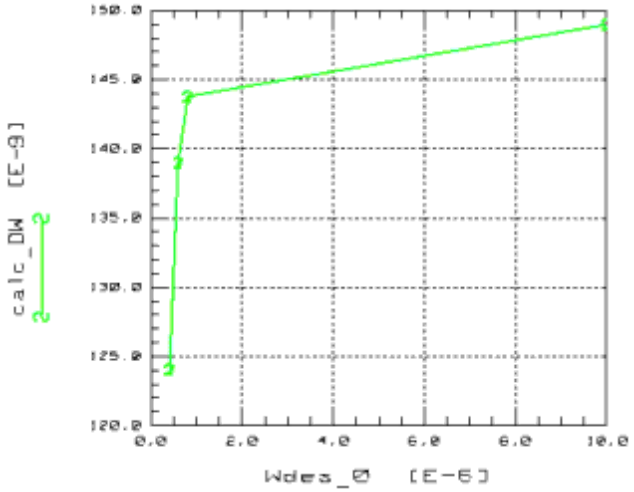


Figure 81 Channel Width Reduction dW as a Function of Channel Width W



Drain Current

Single Equation for Drain Current

In contrast to former implementations of the BSIM3 model, the drain current is represented through a single equation in all three areas of operation (subthreshold region, linear region, and saturation region). Due to this single formula, all first order derivatives of the drain current are continuous, which is an important prerequisite for analog simulations.

In the case that no parasitic drain/source resistance is given, the equation for the drain current is given below:

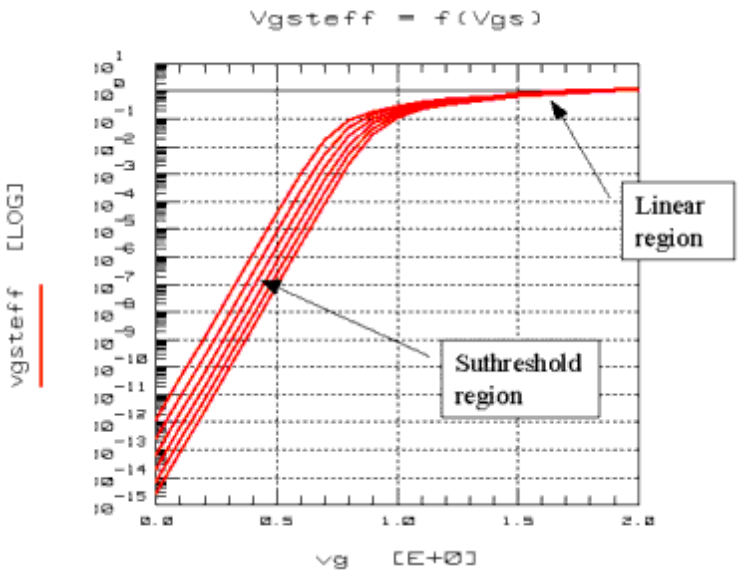
$$(70)\quad I_{ds0} = \mu_{eff} C_{ox} \frac{W}{L} \frac{V_{gsteff}\left(1 - A_{bulk}\frac{V_{dseff}}{2(V_{gsteff}+2V_{tm})}\right)V_{dseff}}{1+\frac{V_{dseff}}{E_{sat}L}}$$

This equation is valid for all three regions of operation of the MOS transistor because the voltages at drain, gate and bulk are replaced by effective drain voltage V_{dseff}, the effective gate voltage V_{gsteff} and the effective bulk voltage V_{bseff}, which are all defined by the continuous equations below:

Equation 71 shows the effective (V_{gs} - V_{th}) voltage, where the factor *n* is defined in Equation 75.

$$(71)\quad V_{gsteff} = \frac{2nv_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}}{2nv_t}\right)\right)}{1+2nC_{ox}\sqrt{\frac{2\Phi_s}{q(\varepsilon_{si}N_{ch})}}\exp\left(\frac{V_{gs}-V_{th}-2V_{off}}{2nv_t}\right)}$$

Figure 82 Effective Voltage V_{gs} - V_{th}



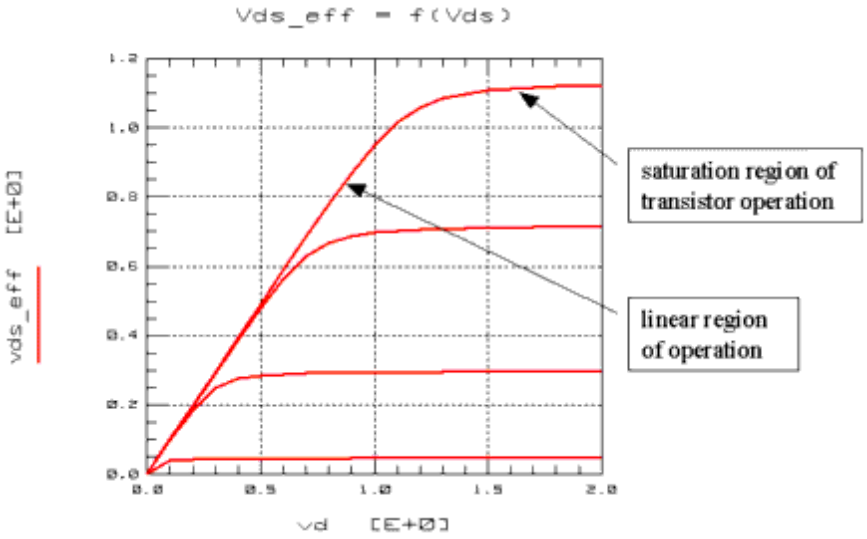
The figure above shows V_{gsteff} in logarithmic scale. V_{gsteff} fits a linear function for values of V_{gs} greater than V_{th} while the subthreshold area is covered by the fit of an exponential function. Through this equation the first derivative is continuous between both operational regions (subthreshold and linear) of the MOS transistor.

Equation 72 shows the effective drain source voltage, V_{dseff}:

$$(72)\quad V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

The following figure shows V_{dseff} in both the linear and the saturation region of operation of the MOS transistor. V_{dseff} models the transition between linear and saturation region without discontinuity in the first derivative of the drain current.

Figure 83 Effective Voltage V_{dseff}



Drain Saturation Voltage Vdsat

The equation for the drain saturation voltage is divided into two cases, the intrinsic case with $R_{ds} = 0$ and the extrinsic case with $R_{ds} > 0$:

$$(73)\quad V_{dsat} = \begin{cases} \dfrac{E_{sat}L_{eff}(V_{gsteff} + 2V_{tm})}{A_{bulk}E_{sat}L_{eff} + (V_{gsteff} + 2V_{tm})}, R_{ds} = 0 \\ \dfrac{-b - \sqrt{b^2 - 4ac}}{2a}, R_{ds} \neq 0 \end{cases}$$

where

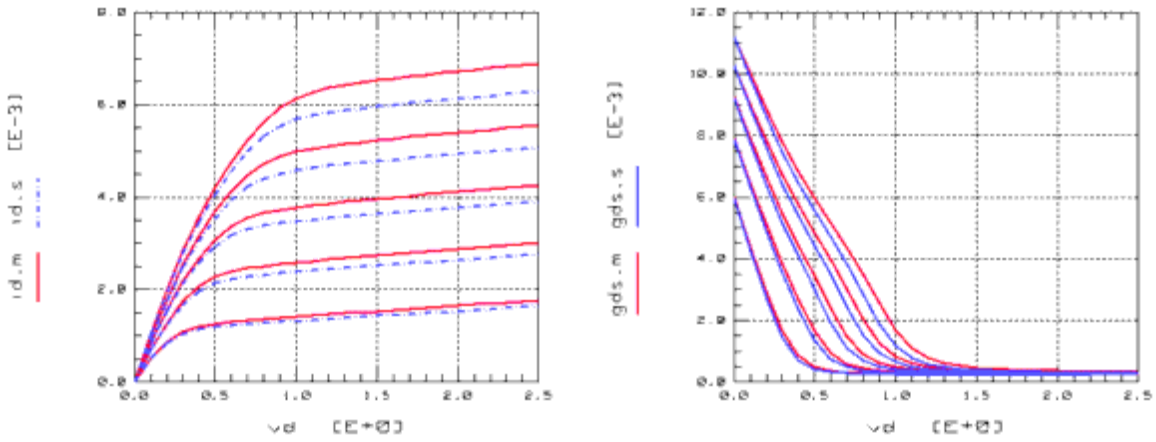
$$a = A_{bulk}^2 R_{ds} C_{ox} W v_{sat} + \left(\frac{1}{\lambda} - 1\right) A_{bulk}$$

$$b = -(V_{gsteff} + 2V_{tm})\left(\frac{2}{\lambda} - 1\right) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}R_{ds}C_{ox}Wv_{sat}(V_{gsteff} + 2V_{tm})$$

$$c = E_{sat}L_{eff}(V_{gsteff} + 2V_{tm}) + 2R_{ds}C_{ox}Wv_{sat}(V_{gsteff} + 2V_{tm})^2$$

The influence of the maximum carrier velocity VSAT on the drain current I_{ds} and the conductance g_{ds} is demonstrated in the following figure.

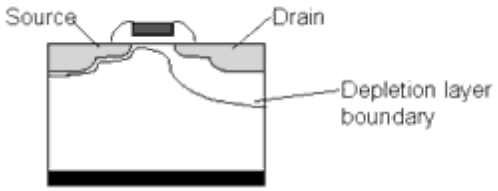
Figure 84 Influence of VSAT on Drain Current I_{ds} and Conductance g_{ds}



Bulk Charge Effect

When the drain voltage is high, combined with a long channel length, the depletion depth of the channel is not uniform along the channel length. This will cause the threshold voltage to vary along the channel length and is called bulk charge effect. The following figure shows the depletion depth as a function of channel length. For long channels, this effect causes a reduction of the drain current.

Figure 85 Depletion Width along the Channel Length

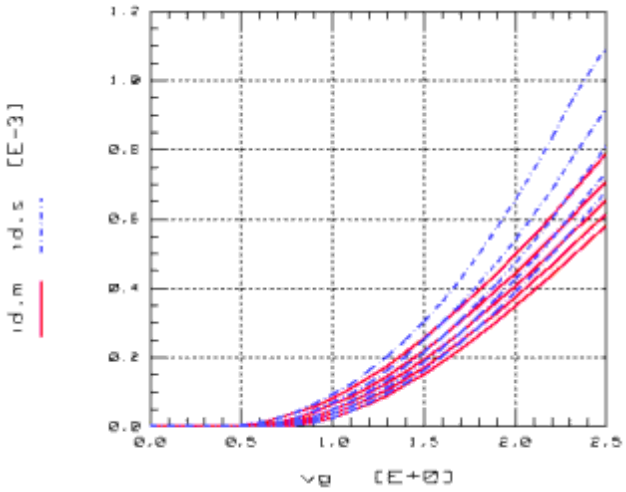


The bulk charge effect A_{bulk} is modeled in BSIM3 with the parameters A0, AGS, B0, B1, and KETA as shown in Equation 74.

$$(74)\quad A_{bulk} = \left(1 + \frac{K_1 \frac{T_{ox}}{T_{oxm}}}{2\sqrt{\Phi_s - V_{bseff}}}\left\{\frac{B_0}{W_{eff} + B_1} + \frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\left[1 - AGS\, V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\right)^2\right]\right\}\right)\frac{1}{1 + K_{eta} V}$$

The influence on the drain current is shown in the following figure.

Figure 86 Influence of A0 and KETA on I_{ds} at High Drain Voltages



Drain Current in the Subthreshold Region

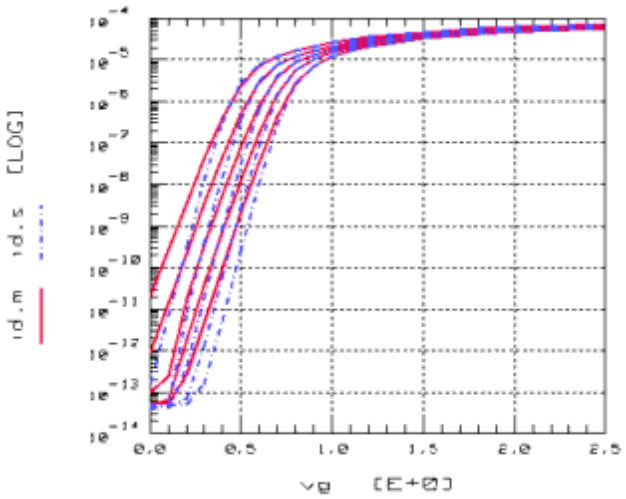
The drain current in the subthreshold region is modeled in BSIM3v3 by the effective voltage V_{gsteff}. The model parameters VOFF and NFACTOR describe the subthreshold current for a large transistor, while the parameters CDSC, CDSCD, and CDSCB are responsible for modeling the subthreshold behavior as a function of channel length. All these parameters contribute to the factor *n* in the formula for V_{gsteff} (see Equation 71).

$$(75)\quad n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})}{C_{ox}}\theta_{th} + \frac{C_{it}}{C_{ox}}$$

$$(76)\quad \theta_{th} = e^{\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)} + 2e^{\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)}$$

The influence of VOFF and NFACTOR on the drain current in the subthreshold region is shown in the following figure.

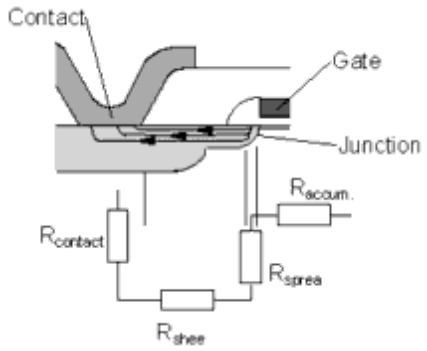
Figure 87 Influence of VOFF and NFACTOR on Drain Current in the Subthreshold Region



Parasitic Resistance

As MOS devices are scaled into the deep submicron region, both the conductance g_m and the current of the device increase. Therefore the voltage drop across the source and drain series resistance becomes a non-negligible fraction of the applied drain source voltage. The resistance components associated with a MOSFET structure are shown in the following figure. These include the contact resistance ($R_{contact}$) between metallization and source/drain area, the diffusion sheet resistance (R_{sheet}) of the drain/source area, the spreading resistance (R_{spread}) that arises from the current spreading from the channel, and the accumulation layer resistance ($R_{accum.}$).

Figure 88 Resistance Components of a MOS Device

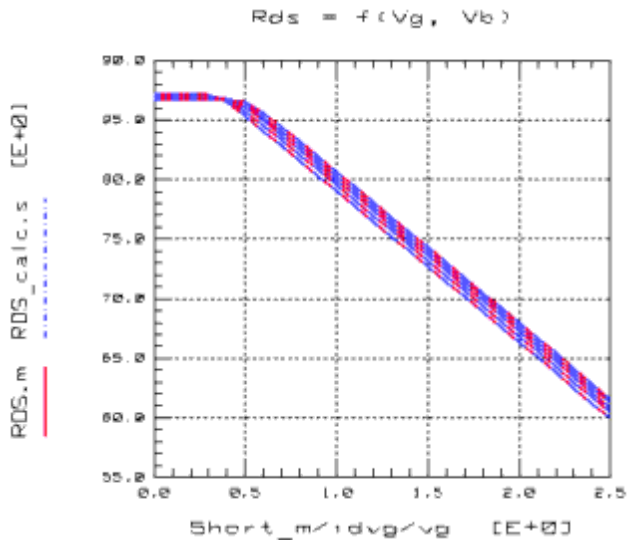


These components are put together to form the following equation in the BSIM3v3:

$$R_{ds} = \frac{R_{dsw}[1 + P_{rwg}V_{gsteff} + P_{rwb}(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s})]}{\left(10^6 W_{eff}\right)^{W_r}} \quad (77)$$

The diagram in the following figure visualizes the equation of R_{ds}. It should be noted that BSIM3 assumes that the drain resistance is equal to the source resistance. This symmetrical approach may cause difficulties if a device with a nonsymmetrical drain source resistance, for example a DMOS power transistor, should be modeled. In this case, a scalable SPICE macro model should add the required behavior to BSIM3.

Figure 89 Drain Source Resistance R_{ds} as a Function of V_g and V_b

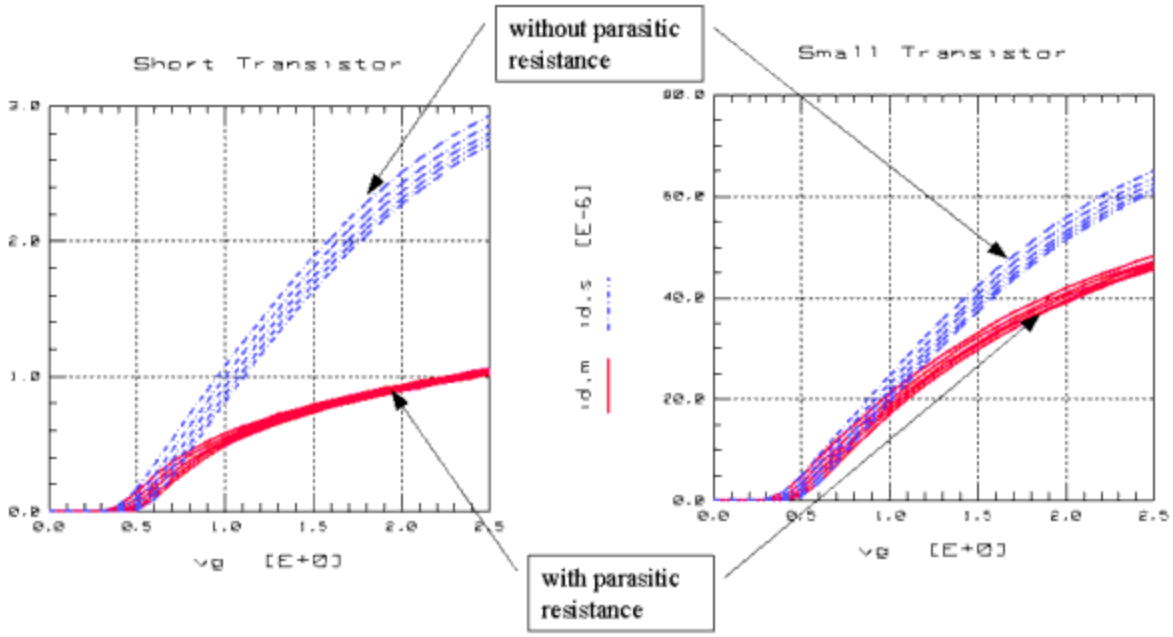


With this enhancement, Equation 70 for the drain current can be rewritten:

$$I_{ds} = \frac{I_{ds0}}{1 + R_{ds} I_{ds0} / V_{dseff}} \quad (78)$$

The influence of the parasitic resistance on the drain current is demonstrated for a SHORT and a SMALL transistor in the following figure.

Figure 90 Influence of Drain Source Resistance on Drain Current



Output Resistance

a) Early Voltage

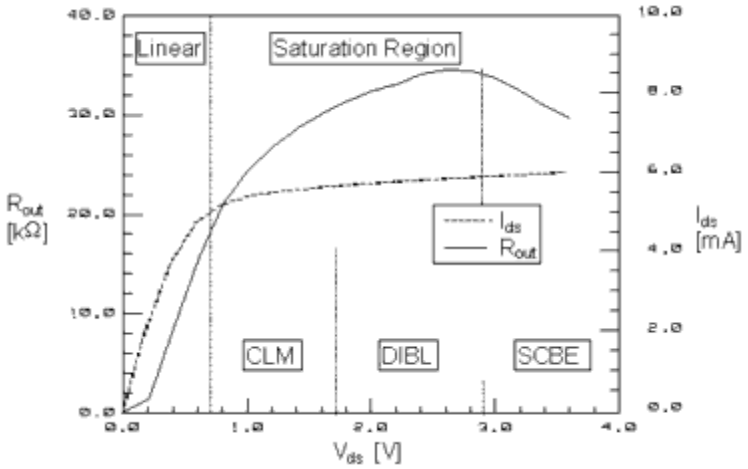
The drain current in the saturation region of submicron MOSFETs is influenced by the effects of channel length modulation (CLM), drain induced barrier lowering (DIBL), and substrate current induced body

effect (SCBE). These effects can be seen clearly looking at the output resistance R_{out} of the device, which is defined as:

$$(79)\quad R_{out} = \frac{\delta V_{ds}}{\delta I_{ds}}$$

In the following figure, the measured drain current and the output resistance of an n-type MOS transistor with a channel length of 0.5 µm are shown.

Figure 91 Drain Current and Output Resistance in Linear and Saturation Region



The left most region in the figure above is the linear region, in which carrier velocity is not saturated. The output resistance is small because the drain current has a strong dependence on the drain voltage. The other three regions belong to the saturation region. The three physical effects CLM, DIBL, and SCBE can be seen in the saturation region and are discussed in the following sections.

With the output resistance, the equation for the drain current (Equation 78) is enhanced by two additional terms and can be rewritten as:

$$(80)\quad I_{ds} = \frac{I_{ds0}}{1 + R_{ds} I_{ds0} / V_{dseff}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

The behavior of the output resistance is modeled in BSIM3 in the same way as the Early voltage of a bipolar transistor is modeled in the Gummel-Poon model. The Early voltage is divided in two parts, V_A due to DIBL and CLM and V_{ASCBE} due to SCBE. V_A is given by:

$$(81)\quad V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}}\right)\left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}}\right)^{-1}$$

where V_{Asat} is the Early voltage at V_{dsat}:

$$(82)\quad V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{ds} v_{sat} C_{ox} W_{eff} V_{gsteff}\left(1 - \frac{A_{bulk} V_{dsat}}{2(V_{gsteff} + 2V_{tm})}\right)}{2/\lambda - 1 + A_{bulk} R_{ds} v_{sat} C_{ox} W_{eff}}$$

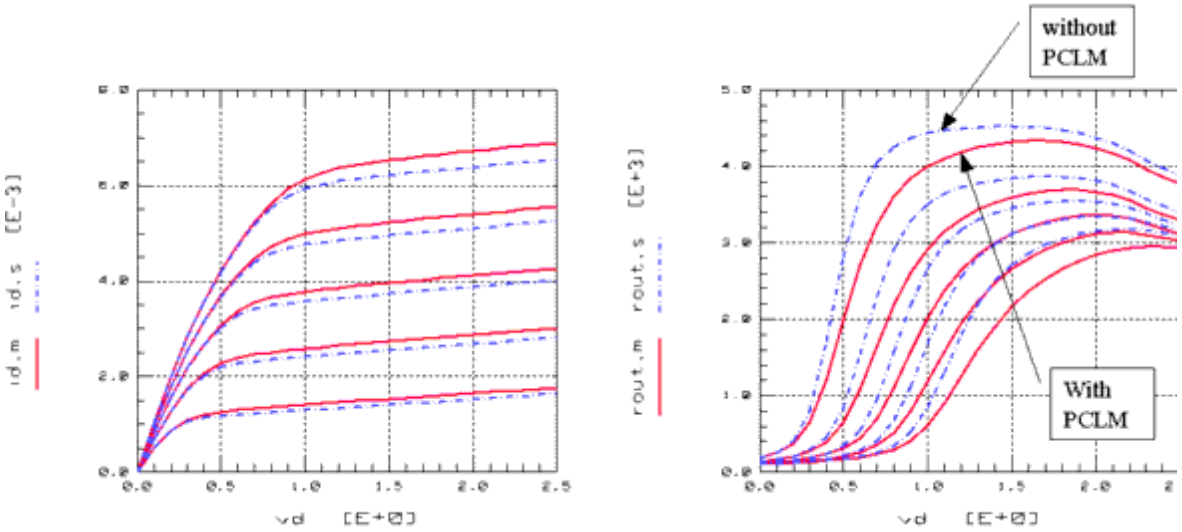
b) Channel length modulation (CLM)

When the drain bias approaches the drain saturation voltage, a region of high electric field forms near the drain and the electron velocity in this region saturates. In saturation, the length ΔL of the high-field region increases by an expansion in the direction of the source with increasing drain-source voltage V_{ds} and the MOSFET behaves as if the effective channel length has been reduced by ΔL. This phenomena is termed channel length modulation (CLM). CLM is not a special short-channel phenomenon, since the effect is present if a MOSFET is short or long. However, its relative importance increases and the effect on the saturated output conductance becomes distinctly more pronounced at shorter gate lengths.

The part of the Early voltage due to CLM is given by:

$$(83)\quad V_{ACLM} = \frac{1}{PCLM}\frac{A_{bulk}E_{sat}L + V_{gsteff}}{A_{bulk}E_{sat}l}(V_{ds} - V_{dseff})$$

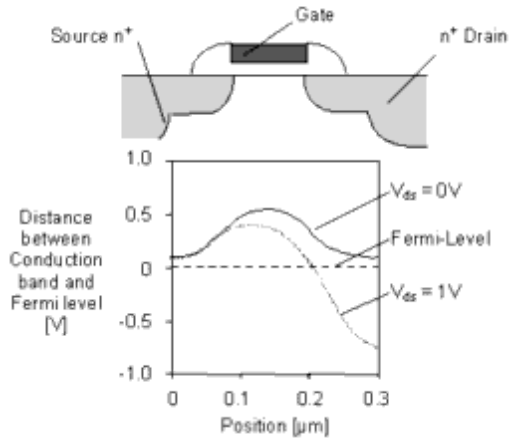
Figure 92 Channel Length Modulation (CLM)



c) Drain Induced Barrier Lowering (DIBL)

The depletion charges near source and drain are under the shared control of these contacts and the gate. In a short-channel device, this shared charge will constitute a relatively large fraction of the total gate depletion charge and can be shown to give rise to an increasingly large shift in the threshold voltage V_{th} with decreasing channel length L. Also, the shared depletion charge near drain expands with increasing drain-source bias, resulting in an additional V_{ds} dependent shift in V_{th}. This effect is related to a drain voltage induced lowering of the injection barrier between the source and the channel and is termed the drain induced barrier lowering (DIBL). The following figure shows the band diagram at the semiconductor-insulator interface of an 0.1 μm n-channel MOSFET simulated by a device simulator. The symmetrical profiles correspond to V_{ds} = 0 and the asymmetrical profiles to V_{ds} > 0. In the figure, the simulated potential barrier near the source is observed to decrease with increasing drain bias, which indicates the origin of the DIBL effect.

Figure 93 Band Diagram at Si-SiO_2 Interface of a 0.1 μm MOSFET



The DIBL effect is modeled in BSIM3v3 with the following equations:

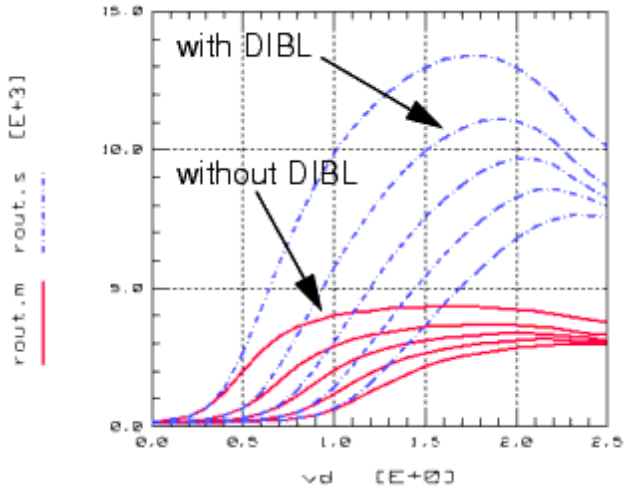
$$(84)\quad V_{ADIBLC} = \frac{(V_{gsteff} + 2V_{tm})}{\Theta_{rout}(1 + P_{DIBLC}V_{bseff})}\left[1 - \left(\frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2V_{tm}}\right)\right]$$

with

$$(85)\quad \Theta_{rout}(L) = P_{DIBLC1}\left[\exp\left(-\frac{D_{rout}L_{eff}}{2l_{t0}}\right) + 2\exp\left(-\frac{D_{rout}L_{eff}}{l_{t0}}\right)\right] + P_{DIBLC2}$$

The following figure shows the influence of the DIBL effect on the output resistance of a short channel transistor.

Figure 94 Influence of Drain Induced Barrier Lowering (DIBL) effect on output resistance



d) Substrate Current Induced Body Effect (SCBE)

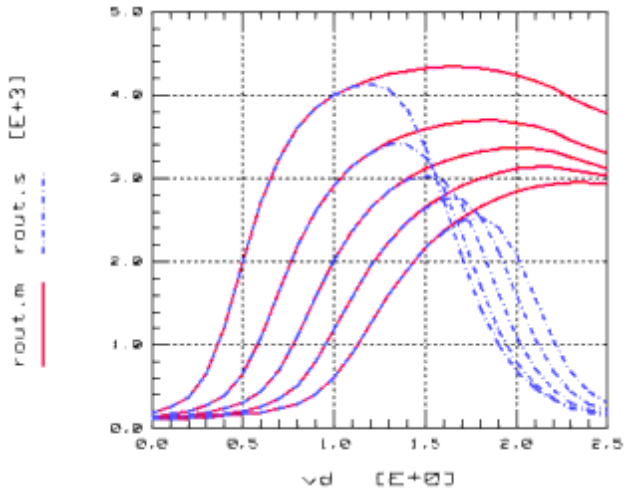
Substrate current is induced through hot electrons at high drain voltages, as described in Substrate Current. It is suggested that the substrate current increases exponentially with the applied drain voltage. The total drain current will change, because it is the sum of the channel current from the source as well as the substrate current. It can be expressed as:

$$(86)\quad I_{ds} = I_{source} + I_{bulk}$$

The increase of the total drain current through hot electrons will be described by the part V_{ASCBE} of the Early voltage which results in a lowering of the output resistance for high drain voltage (following figure).

$$(87)\quad V_{ASCBE} = \left[\frac{P_{SCBE2}}{L}\exp\left(-\frac{P_{SCBE1}{}^{l}}{(V_{ds}-V_{dsat})}\right)\right]^{-1}$$

Figure 95 Substrate Current Body Effect (SCBE)



Substrate Current

In a n-channel MOSFET, electrons in the channel experience a very large field near the drain. In this high field, some electrons coming from the source will be energetic enough to cause impact ionization, and additional electrons and holes are generated by avalanche multiplication. The high energy electrons are referred as *hot* electrons. The generated electrons are attracted to the drain, adding to the channel current, while holes are collected by the substrate contact, resulting in a substrate current, which is shown in the following figure.

Figure 96 Generation of Substrate Current in an n-channel MOSFET

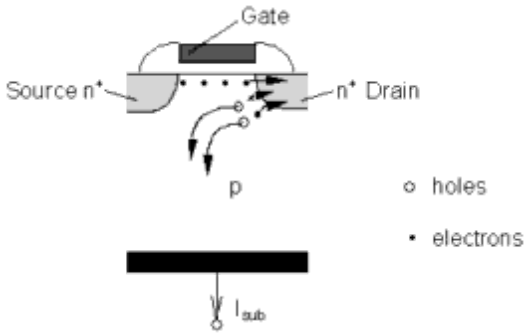
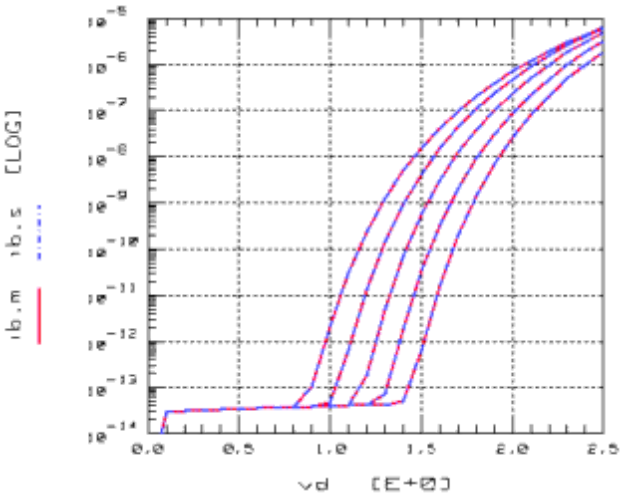


Figure 97 Substrate Current I_{bs} parameterized by V_g



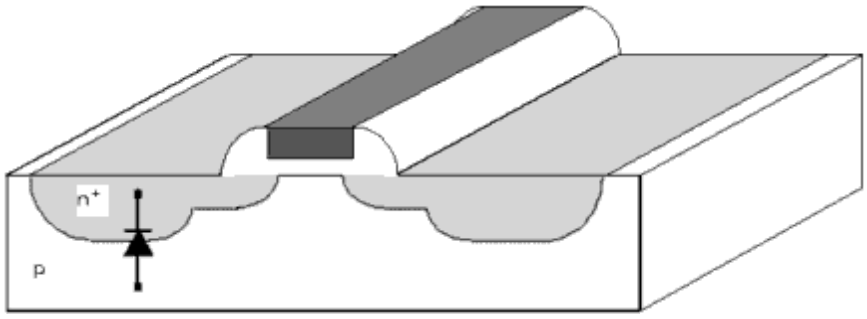
The substrate current is described in BSIM3 by the following equation:

$$(88)\quad I_{sub} = \frac{\alpha_0 + \alpha_1 L_{eff}}{L_{eff}}(V_{ds} - V_{dseff}) \exp\left(-\frac{\beta_0}{V_{ds} - V_{dseff}}\right) I_{ds}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)$$

Drain/Bulk and Source/Bulk Diodes

The following figure shows a pn-junction diode between the bulk and the drain of an n-type MOS Transistor.

Figure 98 pn-junction diode



The drain/bulk and the source/bulk pn-junctions can be used as diodes in CMOS designs. BSIM3v3 offers a simple DC model for the current I_{bs} or Ibd flowing through these diodes.

$$(89)\quad I_{bs} = \begin{cases} I_{sbs}\left(e^{\left(\frac{V_{bs}}{NV_{tm}}\right)} - 1\right) + G_{MIN} V_{bs} \\ IJTH + \frac{IJTH + I_{sbs}}{NV_{tm}}(V_{bs} - V_{jsm}) + G_{MIN} V_{bs} \end{cases}$$

where NJ is the emission coefficient of the source junction and the saturation current I_{sbs} is calculated as:

$$(90)\quad I_{sbs} = A_S J_S + P_S$$

where J_S is the saturation current density of the source/bulk diode, A_S is the area of the source junction, J_{SSW} is the sidewall saturation current density of the source/bulk diode, and P_S is the perimeter of the source junction. J_S and J_{SSW} are functions of the temperature and can be described as:

$$(91)\quad J_S = J_{S0} e^{\left(\frac{\frac{E_{g0}}{V_{tm0}} - \frac{E_g}{V_{tm}} + X_{TI} \ln\left(\frac{T}{T_{nom}}\right)}{NJ} \right)}$$

$$(92)\quad J_{SSW} = J_{S0SW} e^{\left(\frac{\frac{E_{g0}}{V_{tm0}} - \frac{E_g}{V_{tm}} + X_{TI} \ln\left(\frac{T}{T_{nom}}\right)}{NJ} \right)}$$

where:

$$E_{g0} = 1.16 - \frac{7.02 \times 10^{-4} Tnom^2}{Tnom + 1108}$$

$$E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

J_{S0} is the saturation current density (default is 10^{-4} A/m^2)

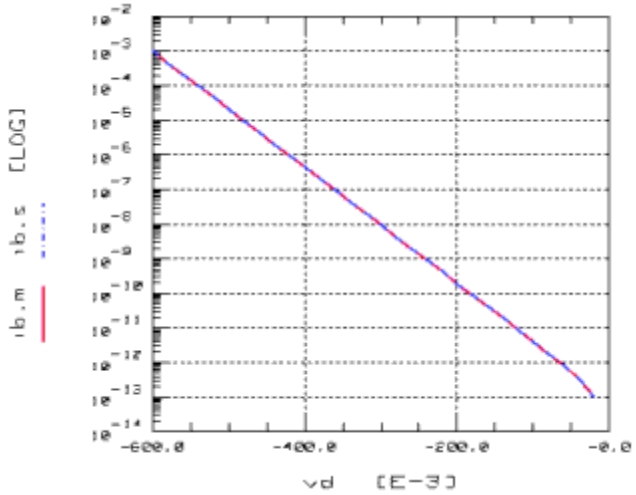
J_{S0SW} is the sidewall saturation current density (default is 0)

$NV_{tm} = NJ \cdot (K_b T/q)$

$V_{jsm} = NV_{tm} \ln (ijth/I_{sbs} + 1)$

The current I_{bs} through the diode is shown in the following figure:

Figure 99 Current I_{bs} Through Diode



Consistency Check of DC measurement data for multiple measured devices

You can perform a quick consistency check of the measured data versus gate length, gate width, and temperature. If there are measurement errors, they can be easily identified using this additional check of DC measurement data.

Drain Saturation Current Idsat

Displaying the absolute values of IDSAT versus the gate length of all measured devices does not easily show measurement errors because the absolute currents spread all over the diagram, as shown in the left part of the following figure.

In this diagram, absolute values of IDSAT versus L and W are displayed. IDSAT is determined at max. Vg, max. Vd, and Vb=0 for one temperature. Each dot represents one transistor and each color a different value of the transistors gate width W. The legend is shown to the right of the plot. If you select one of the dots, at the top of the plot the details of this specific transistor are shown. In our example of Idsat, the red dot in the middle of the plot is a transistor with W=250nm and L=400nm. The actual drain current of this geometry is also shown!

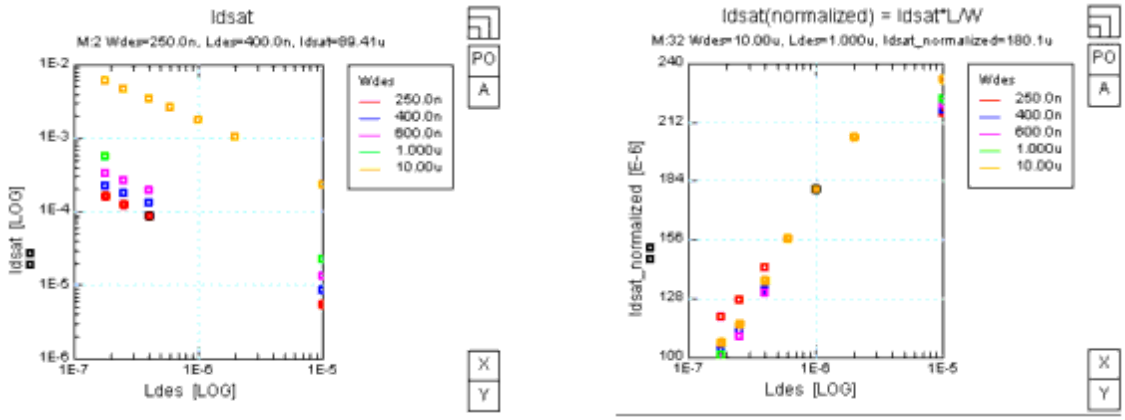
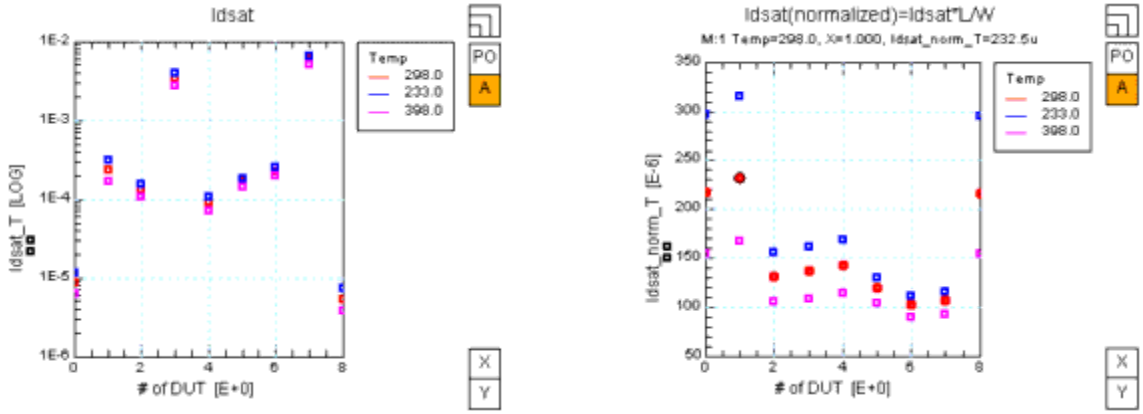


Figure 100 Left part: IDSAT = f(W, L); right part: IDSATnorm = f(W, L)

But if the same values (measured at the same temperature) are displayed in a normalized representation IDSATnorm = Idsat*L/W (see right part of the figure above), the values appear in a sorted way. They are shown from the transistors having the highest gate width values on top of the lower gate width transistors. The transistors having the smallest gate width values are shown at the lowest display position in the diagram.

If the temperature measurements of the transistors are normalized as well, the measured data is again sorted. The following diagram shows IDSAT and IDSATnorm for devices with temperature measurements. Each color represents one temperature and each value of the x-axis represents one device.



Left part: IDSAT = f(temp, device); right part: IDSATnorm = f(temp, device)

Threshold voltage

Similar normalized data representations are available for the threshold voltage Vth of measured devices, see the following figure. Vth is determined for each device at Vb=0 and low Vd. The following diagram shows Vth as a function of L, W (left part), and temperature (right part) for those devices. Vth is determined using the reference current method:

$$V_{th} = V_G(I_{D0})$$

with: $I_{D0} = I_{Dref} \cdot \frac{W}{L}$ using $I_{Dref} = 100nA$

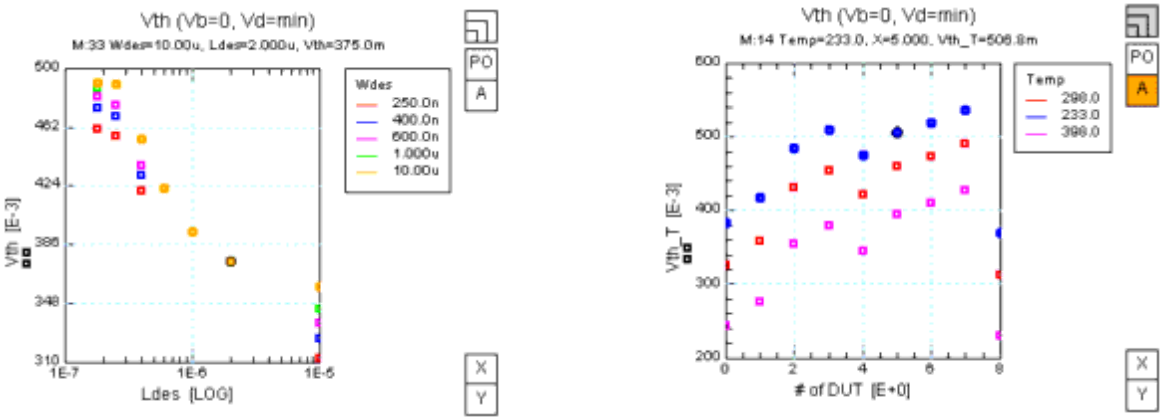


Figure 101 Left part: Vth = f(L, W); Right part: Vth = f(temp, device)