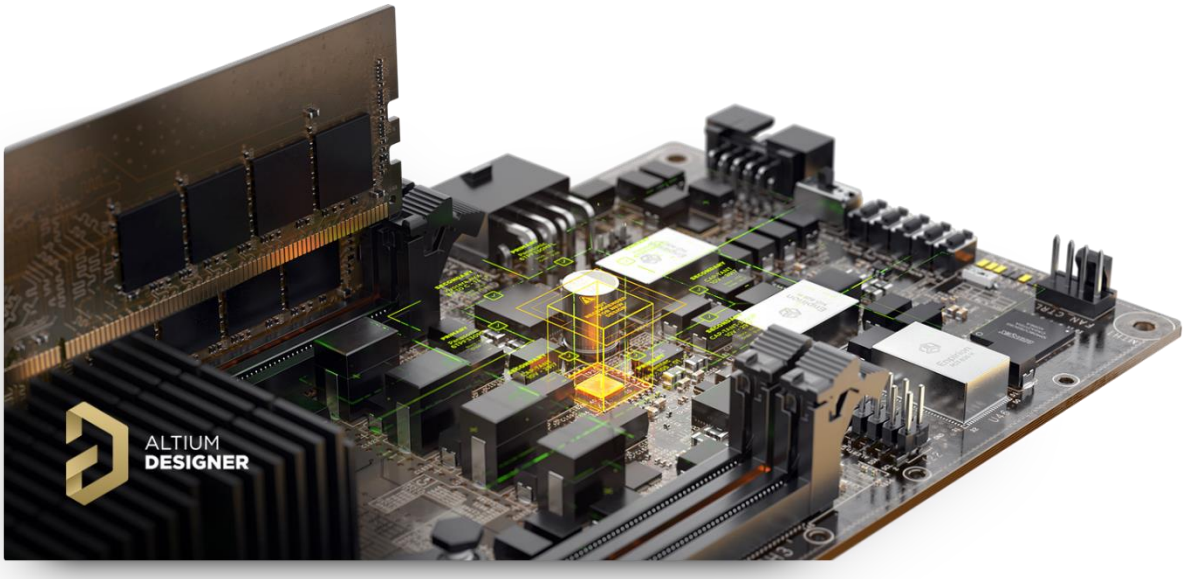

Altium Designer

Advanced Course

Module: Via Stitching and Via Shielding

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Via Stitching and Via Shielding

1.1 Purpose

Via stitching is a technique used to tie together larger copper areas on different layers, in effect creating a strong vertical connection through the board structure, helping maintain a low impedance and short return loops.

Via shielding is used in combination with guard rings to create a via wall, helping create an electromagnetically 'quiet' PCB. Via shielding can also be used to tie areas of copper that might otherwise be isolated from their net, to that net.

1.2 Shortcuts

Shortcuts when working with Via Stitching and Via Shielding

F1:	**Help**
T-H-A:	**Stitching Dialog**
CTRL+S:	**Save Document**

1.3 Preparation

1. **Close all existing projects and documents.**
2. Open the `Via Stitching and Via Shielding.PrjPCB` project found in its respective folder of the Advanced Training.

1.4 Via Stitching

1.4.1 Adding Stitching Vias to a Net

3. Open the `Via Stitching.PcbDoc` document.
4. From the **Tools** menu, select **Via Stitching/Shielding » Add Stitching to Net…**.
5. In the *Add Stitching to Net* dialog, select the *Net* dropdown and then select **GND** as shown in Figure 1 below.

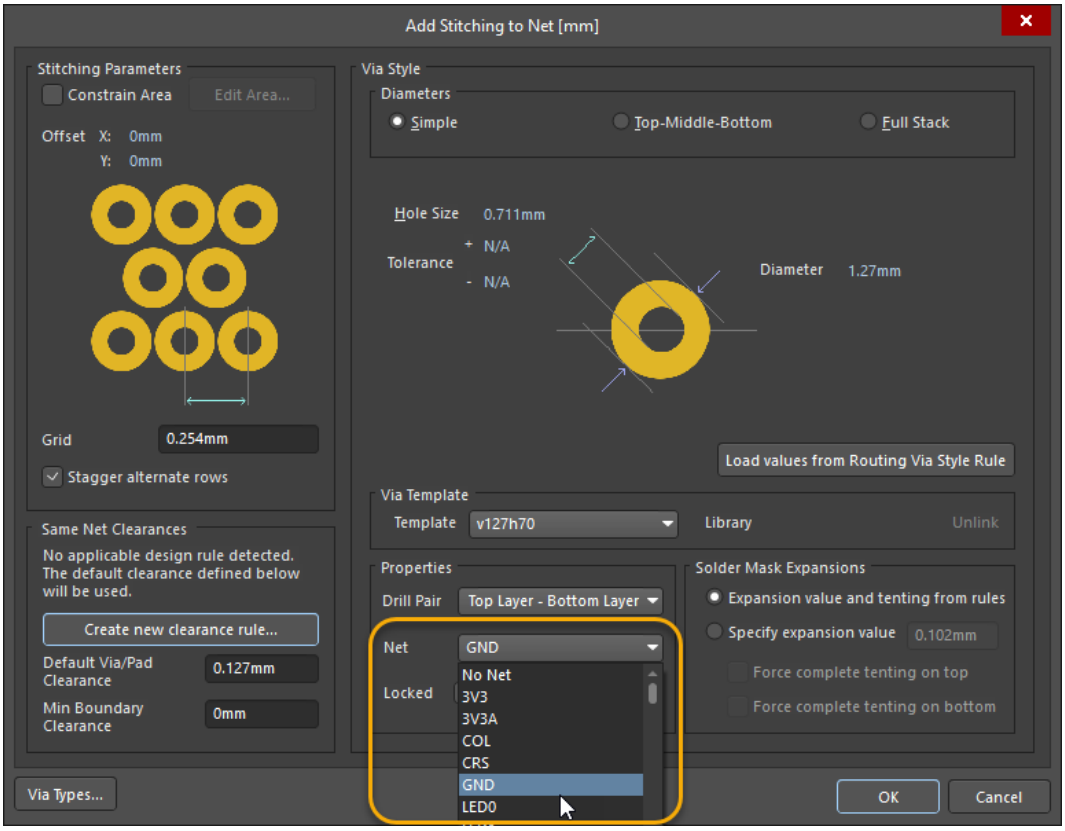

Figure 1. Add Stitching to Net Menu

6. Next, we will use the *Constrain Area* to add stitching to a portion of the polygon. Otherwise, the entire polygon will be used.
   a) Click the **Constrain Area** checkbox in the top left corner of the Stitching window. This will change focus to the PCB with a crosshair on your cursor.
   b) Click on each of the 4 white arrows as shown in Figure 2 below.

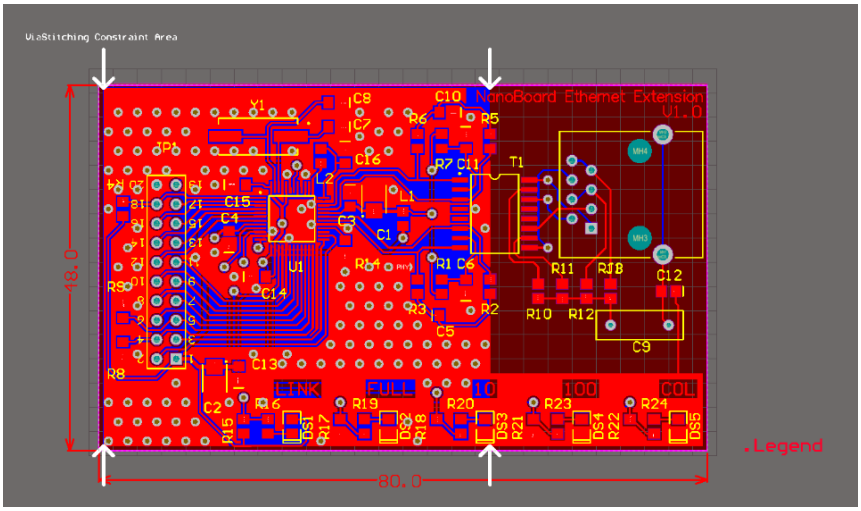

Figure 2. Via Stitching area

   c) Once the area has been defined, hit the **ESC** key to return to the *Add Stitching to Net* dialog.
7. In the *Stitching* dialog window, change the **Grid** size from `0.254mm` to `2.54mm`.

8. Verify the *Hole Size* is `0.711mm` and *Diameter* is `1.27mm` as shown in Figure 3.
9. Enable the **Specify expansion value** radio button so that we can force tenting on the `Top` and `Bottom` of each via.
10. Check the **Force complete tenting on top** and **bottom** checkboxes under the *Solder Mask Expansions* area to have the added stitching vias covered over with Solder Mask as shown in Figure 3.

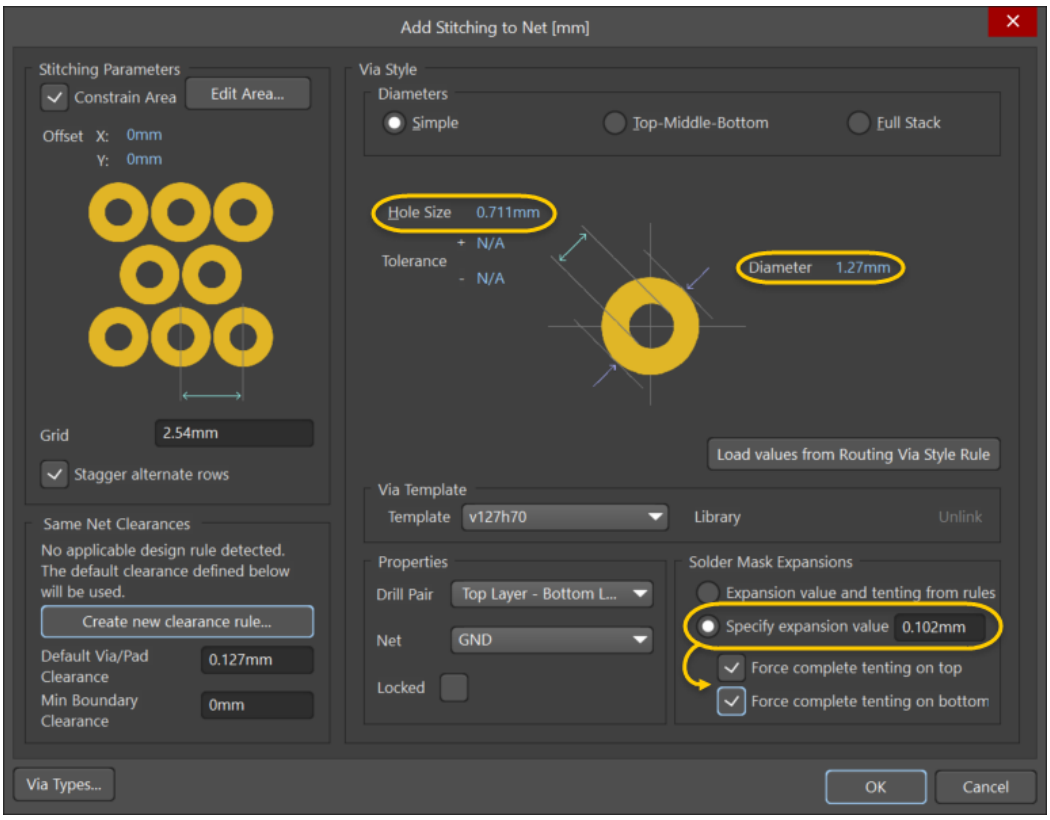

Figure 3. Via hole and tenting values

11. Click **OK** to generate the Via Stitching. An *Information* dialog box will appear, stating that 96 vias have added as shown in Figure 4.

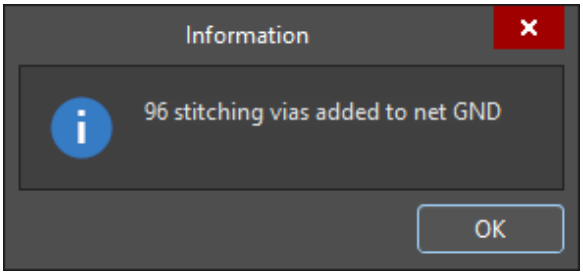

Figure 4. Stitching Vias added

12. Click **OK** on the *Information* dialog box to continue.
13. In the next step, we will modify the via stitching to add an offset to the via location.
    a) Double-click within any part of the constrain area where the via stitching exists. This will populate the *Properties* panel with the *Via Stitching* information.
    b) In the *Offset (X/Y)* area of the *Properties* panel, change the X value to `-0.4mm`.
    c) Once you press **Enter**, you'll be prompted to apply the new changes as shown in Figure 5.

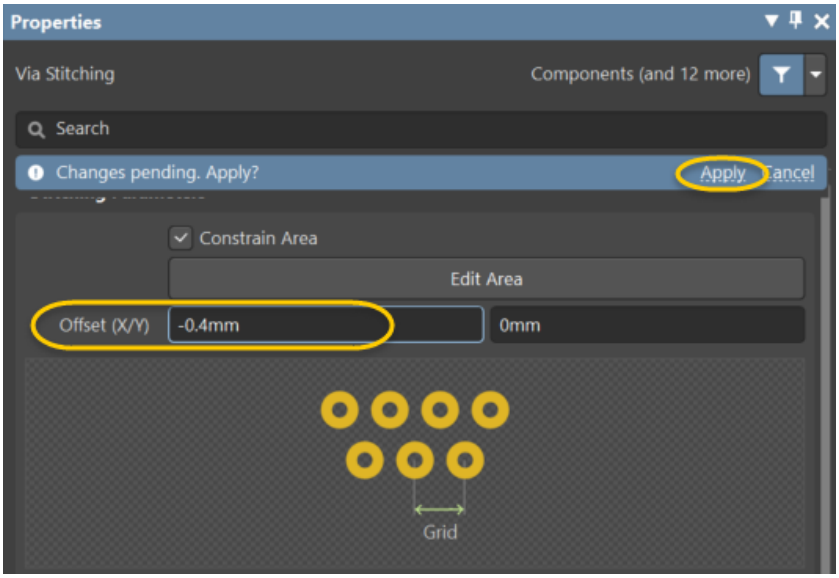

Figure 5. Changing the Via Stitching properties

d) Click the **Apply** button that appears at the top of the *Properties* panel.

e) A new *Information* dialog will appear, displaying the new number of vias added to the stitching area as shown in Figure 6.

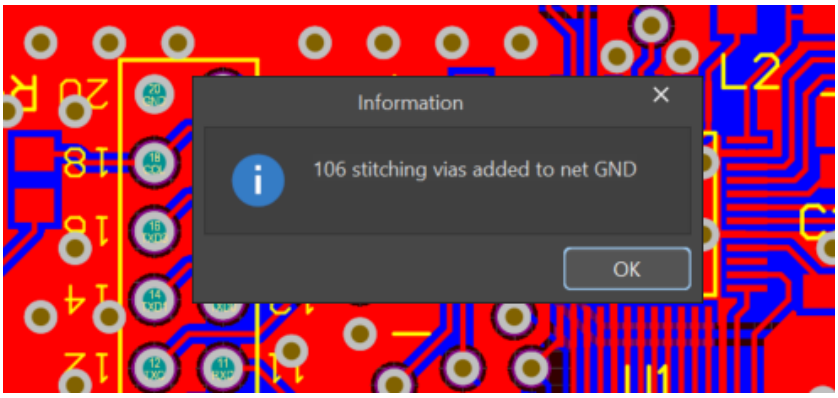

Figure 6. New Information dialog with added vias

14. Click **OK** in the *Information* dialog box to continue.

1.4.2 **Removing Via Stitching**

15. We'll now remove the via stitching by going to the **Tools** menu, select **Via Stitching/Shielding » Remove Via Stitching Group**.
16. Once the cursor turns into a crosshair, select one of the vias in the stitching group to remove the entire group. Vias that are a part of a stitching group will have a `[VS]` identifier on the via itself.
17. After clicking on one of the stitching vias, the stitching group will be removed.
18. Close the `Via Stitching.PcbDoc` document without saving any changes.

1.5 Via Shielding to a Net

1.5.1 **Add Via Shielding**

19. Open the `Via Shielding.PcbDoc` document.
20. From the **Edit** menu, click on **Select,** then select **Connected Copper.**
21. Select the `PWFBOUT` net that connects the component `U1` and `C1` as shown in Figure 7.

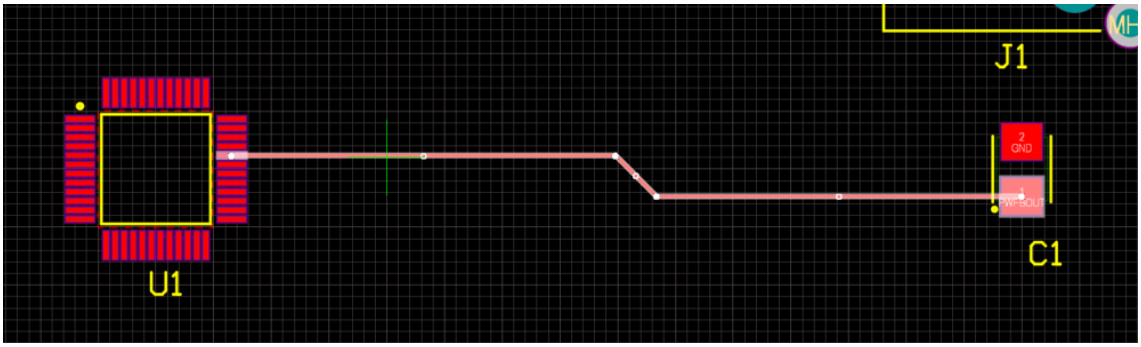

Figure 7. Selecting the Connected Copper for net PWFBOUT

22. Right-click to end the command.
23. From the **Tools** menu, select **Via Stitching/Shielding » Add Shielding to Net…**
24. Using Figure 8 below as a reference to change the values to the following:
    a) Change the *Net* drop down menu to **GND**.
    b) Change the *Hole Size* to `0.3mm` and *Diameter* to `0.8mm`.
    c) Change the *Row spacing* to `0.75mm` and *Distance* to `0.5mm`
    d) Change the *Grid* to `0.254mm`.
    e) Ensure *Rows* is set to `2`, which will add an additional row of via shielding.
    f) Ensure the **Add Shielding Copper** option is enabled. This will create polygon pours where vias exist in the via shielding trail.
    g) Review all of your changes and click **OK** when done.

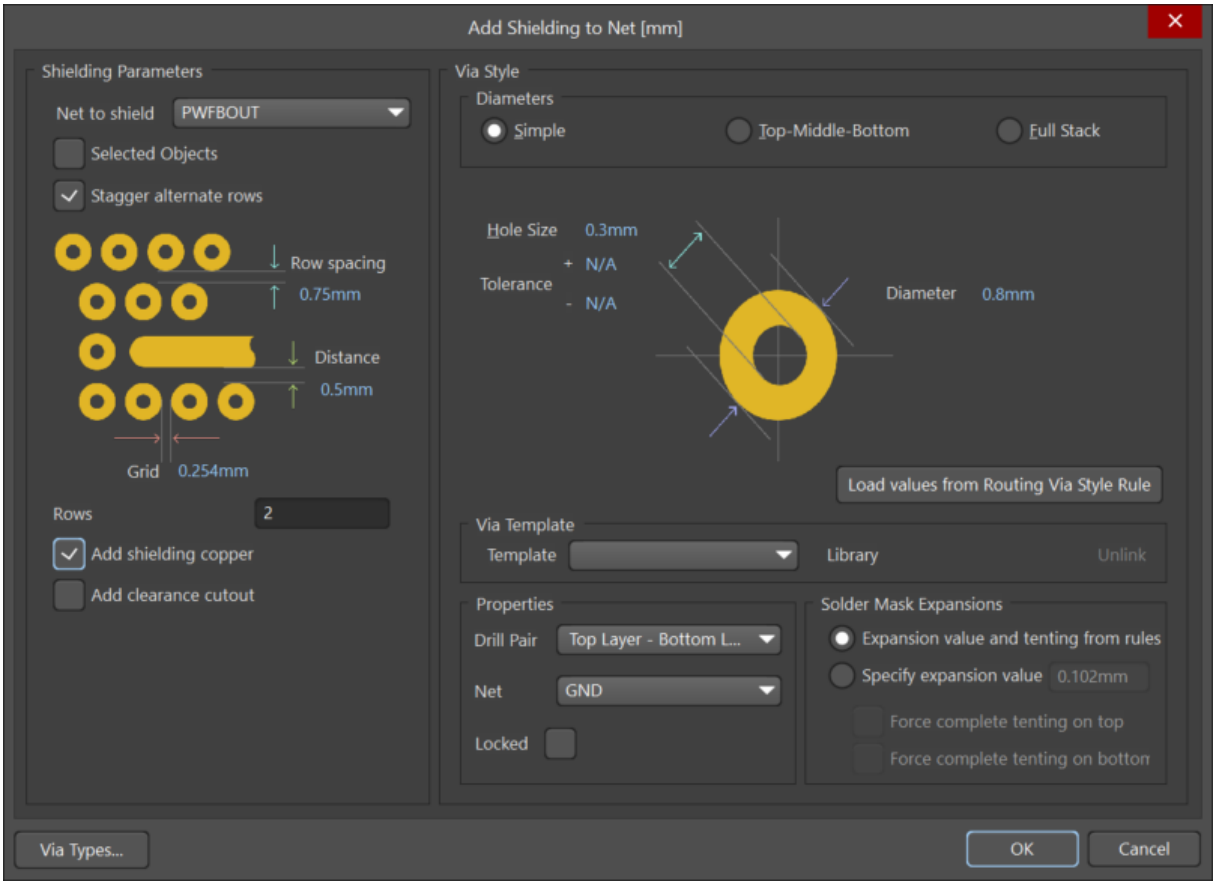

Figure 8. Via Shielding properties

25. The via shielding will be added to that net as shown in Figure 9.

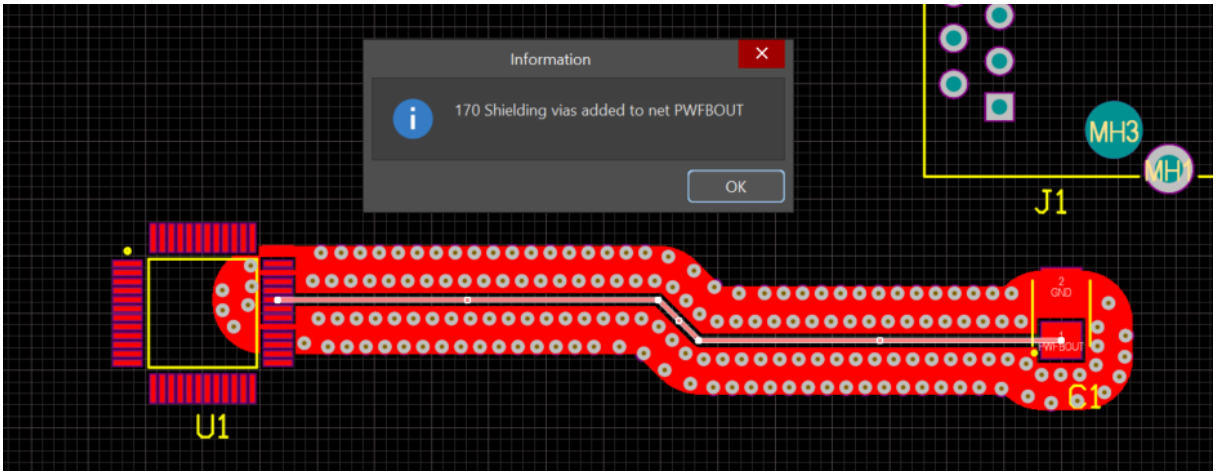

Figure 9. Via Stitching added

26. Click **OK** in the *Information* dialog window to continue.

1.5.2 **Modify the Shielding**

27. To prevent copper pour from filling up the center of `U1`, we will go to the **Place** menu, and select **Polygon Pour Cutout.**
28. Left-click at each corner of the U1 body to complete a square cutout.
29. Right-click twice to exit the cutout command. Your PCB should now look similar to Figure 10. If not, you'll need to repour the polygon from the **Tools** menu.

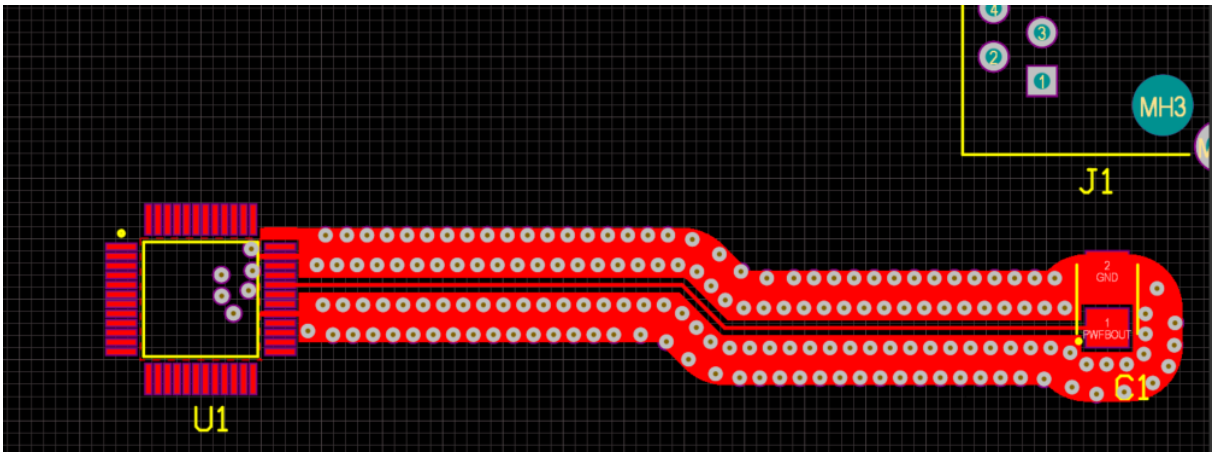

Figure 10. Polygon Pour within component U1

30. To make additional changes to the shielding, double-click on one of the shielding vias to open the *Properties* panel. A shielding via will have the `[VSH]` indicator.
    a) Change the Rows value from `2` to `1` and hit **Enter**.
    b) Click the **Apply** button at the top of the *Properties* panel to apply the changes. You should notice that the vias will be reduced to 1 row.
    c) Click **OK** in the *Information* dialog window to continue.
    d) Changes the Rows value back to `2` and hit **Enter**.
    e) Click the **Apply** button so the shielding returns to its original state.
    f) Click **OK** in the *Information* dialog window to continue.
31. Select the shielding vias under `U1` and manually delete them with the **Delete** key.
32. Confirm that there are no longer polygon pours or vias within component `U1` as shown in Figure 11.

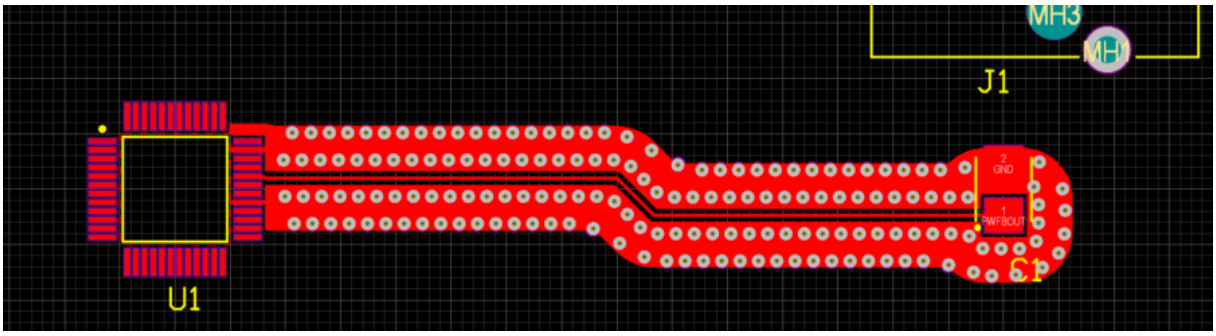

Figure 11. Removed Polygon Pour within component U1

33. Feel free to save your modifications.
34. **Close the project and any open documents.**

Congratulations on completing module

Via Stitching and Via Shielding

from the

Altium Designer Advanced Course

Thank you for choosing Altium Designer