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Isolated Single-Stage Interleave Resonant PFC Rectifier with Active and Novel Passive Output Ripple Cancellation Circuit

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Masterprogram i förnybar elgenerering
Master Programme in Renewable Electricity Production

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Abstract

Isolated Single-Stage Interleave Resonant PFC Rectifier

Abidemi Oluremilekun Eleyele

With the increasing demand for fast, cheaper, and efficient power converters come the need for a single-stage power factor correction (PFC) converter. Various single-stage PFC converter proposed in the literature has the drawback of high DC bus voltage at the input side and together with the shift to wide bandgap switches like GaN drives the converter cost higher. However, an interleaved topology with high-frequency isolation was proposed in this research work due to the drastic reduction in the DC bus voltage and extremely low input current ripple thereby making the need for an EMI filter circuit optional.

Meanwhile, this research work focuses on adapting the proposed topology for a high voltage low current application (EV charger - 400V, 7KW) and low voltage high current application (telecom power supply - 58V, 58A) owing to cost benefits. However, all single-stage PFC are faced with the drawback of second-order(100Hz) output harmonic ripple. Therefore, the design and simulation presented a huge peak to peak ripple of about 50V/3A and 26V/26A for the EV charger and telecom power supply case, respectively. This created the need for the design of a ripple cancellation circuit as the research required a peak to peak ripple of 8V and 200mV for the EV - charger and telecom power supply, respectively.

A novel output passive ripple cancellation technique was developed for the EV charger case due to the ease it offers in terms of control, circuit complexity and extremely low THDi when compared with the active cancellation approach. The ripple circuit reduced the 50V ripple to 431mV with the use of a total of 2.2mF capacitance at the output stage.

Despite designing the passive technique, an active ripple cancellation circuit was designed using a buck converter circuit for the telecom power supply. The active approach was chosen because the passive has a slow response and incurs more loss at a high current level. Adding the active ripple cancellation circuit led to a quasi-single stage LLC PFC converter topology. A novel duty-ratio feedforward control was added to synchronize the PFC control of the input side with the buck topology ripple cancellation circuit. The addition of the ripple circuit with the feedforward control offered a peak to peak ripple of 6.7mV and a reduced resonant inductor current by half.

After analysis, an extremely low THDi of 0.47%, PF of 99.99% and a peak efficiency of 97.1% was obtained for the EV charger case. The telecom power supply offered a THDi of 2.3%, PF of 99.96% with a peak efficiency of 95%.

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POPULAR SCIENTIFIC SUMMARY

Highly efficient frontend converter topologies are in huge demand nowadays, as they are the bridge between the AC mains (grid) and modern power electronic equipment like telecom power supply unit (PSU) and Electric vehicle (EV) charger. LLC enabled converters to fall in this category. Cost is also an essential factor influencing the demand for converters in the industry. To this end, single-stage PFC frontend converters or rectifiers are currently being explored despite the drawbacks of high output peak to peak ripple known as second-order harmonic ripple coming from twice the grid frequency.

Owing to the drawback, the objective of this thesis is to develop isolated single-stage PFC rectifier that eliminates the second-order output harmonics and efficient with reduced cost. Two design cases were implemented in PSIM power electronics design software. The first is a 3.4KW, 58V telecom PSU, employing the use of a buck converter topology at the output stage to act as an active ripple cancellation circuit due to its separate control scheme. The second is an EV charger with a newly developed passive ripple cancellation circuit (PRC) at the output stage to eliminate the second-order harmonic.

The simulation result showed that the active ripple cancellation circuit reduced the output ripple drastically from 26V/26A to 6.7mV/6.7mA, which is way below the maximum of 200mV/200mA specified for the research. The PRC approach also presents an extremely low ripple of 431mV as opposed to a set maximum ripple of 8V.

In conclusion, the PRC approach provided extremely low THDi, better PF, high efficiency and low output capacitance. This behaviour confirms that PRC approach has great potential and benefit than an active ripple cancellation approach if explored further in future works.

I dedicate this research work to God, my Mother, Global Sustainable Electricity Partnership organization (GSEP) and Uppsala University.

Never get discouraged if you fail, learn from it, and keep trying. Learn with both your heads and hands; there is always a way of doing it better - Thomas Edison.

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ABBREVIATIONS

AC	: Alternating current
ACM	: Average current mode
CCM	: Current conduction mode
CRM	: Critical conduction mode
DC	: Direct current
DCM	: Discontinuous conduction mode
DF	: Distortion factor
DPF	: Displacement factor
EMI	: Electromagnetic interference
EV	: Electric Vehicle
K	: Inductance ratio
PF	: Power factor
PFC	: Power factor correction
PRC	: Passive ripple cancellation
PSU	: Power supply unit
PWM	: Pulse width modulation
Q	: Quality factor
SMPS	: Switch mode power supply
SISO	: Single input single output
SRC	: Series resonance converter
THD	: Total harmonic distortion
THDi	: Total harmonic distortion of the input current
ZCS	: Zero current switching
ZVS	: Zero voltage switching

CHAPTER 1

INTRODUCTION

Power Electronics has evolved to be the modern heart of all technologies in Electrical Engineering and other related fields. It is an aspect of Electronics Engineering that deals with the use of solid-state devices for the conversion of electricity from one voltage or current level to another. An example of such is AC to DC converter, commonly known as a rectifier.

Rectifiers are the backbone of any switched-mode power supply units (SMPS) as it acts as the interface between the grid and modern power electronic equipment such as Electric car chargers and power supply unit (PSU) for telecommunication equipment. Conventionally most PSUs consist of line frequency diode bridge performing the rectification of the line AC to DC. This is followed by a large capacitor whose function is to filter out the DC ripple voltage, thus creating the drawback of peak current and high low order harmonics at the input side. This behaviour leads to a low input power factor and making utilities to specify and enforce acceptable harmonic standards and guidelines limiting it.

In a quest to meet these requirements, power factor correction (PFC) technique was developed and have since led to the drastic reduction in harmonics by regulating the electromagnetic interference (EMI). This ensures that the sinusoidal input current from the grid follows the voltage, thereby reducing the output filter requirement and providing a considerable increase in efficiency.

Different rectification topologies like bridge, bridgeless and totem-pole boost converters have been developed with an advanced control scheme which offers a power factor (PF) above 99%, advancement in switches is also a crucial part in reducing the losses and providing high efficiency.

1.1 Scope of work

Recently, a substantial number of single-stage isolated PFC topologies have appeared in the scientific literature. However, most of the authors have focused on high voltage low current application as they mostly boost PFC topologies which perform better for high voltage application. One of the significant

drawbacks of single-stage PFC is the presence of second harmonic ripple at the output and the most common technique used is the active ripple cancellation technique which makes the design complex and more expensive.

For that reason, the main objective of this master's thesis is to fill that missing gap, by developing a single-stage PFC capable of working for low voltage high current application and using an active and passive ripple cancellation technique to remove the second-order harmonics at the output. Both ripple cancellation technique would also be explored and compared as well.

The simulation model will be carried out in PSIM, which is a software package, designed specifically for power electronics and motor drive simulations. The thesis is written in cooperation with HUAWEI research and development centre of Sweden. The research is a high priority project as it fits into the company goal of achieving low cost, small and highly efficient switch-mode power supplies. More emphases are made on the design and implementation in PSIM and less on the real-life implementation due to the present Covid-19 crisis as that would be future work.

Furthermore, the PFC design would focus on 230VRMS AC standard and not for 120VRMS. The control technique is to be made as simple as possible by making use of the average current mode technique with a modified PI controller (second-order) for both the current and voltage loop. The design would be done stage for two case scenarios, which is the telecom network power supply (58V/3.4KW) and an EV charger (400V/7KW). An Active ripple cancellation circuit would be added to the telecom power supply scenario and passive ripple cancellation technique for the EV charger case.

In chapter 2, the basic operation of the interleaved PFC single-stage resonant converter with high-frequency isolation would be described. This would involve component dimensioning, specification and losses in the boost inductor, DC-link capacitor, transistor, and the design of the added active ripple cancellation circuit. The chapter would conclude with control design and simulation results for the circuit.

Chapter 3 would discuss the EV charger design together with a passive ripple cancellation technique added at the output side. The chapter ends with the control design, simulation results and comparison of both ripple cancellation techniques. Chapter 4 concludes the research with a discussion on future work, which would lay emphasis on the limitations and drawbacks of the simulation model.

1.2 Motivation

Most PFC rectifiers topologies are of boost type in nature as boost converters possess an input inductor whose current is continuous. They are mostly two-stage configurations due to the ease in mitigating the second-order output harmonics through the DC bus, but this comes with the limitation of increased cost, complexity, and limit in the efficiency. These drawbacks created a vast interest in single-stage PFC rectifiers as they possess the ability to achieve higher efficiencies, increased power density with small size and cost.

As attractive as single-stage PFC rectifiers are, they come with a drawback of second-order harmonics at the output, which is twice the line frequency ripple appearing at the output. This drawback makes it not suitable for telecommunication and battery charging applications sensitive to voltage variations. Active control strategies are complicated as it uses advanced control techniques to suppress the second-order harmonics.

Therefore, regarding Telecommunication applications which make use of low voltage high current rectifier less job has been done on active ripple suppressing technique for single-stage, single-phase rectifier. More so, the focus has been on active ripple cancellation technique not passive ripple suppressing technique. The passive approach is promising not only to reduce the complexity of the system but also to provide a satisfactory and better result than the active strategies. This research, therefore, plays the role of comparing and showcasing the positive impact both approaches has on second-order ripple reduction or cancellation while maintaining the single-stage PFC configuration.

1.3 Literature

1.3.1 Power factor correction

Before diving into the details of the power factor correction principle, it is essential to affirm some theories. According to [1] the power factor (PF) of any rectifier is the ratio of the real input power to the apparent input power of the rectifier. Let V_i , I_i and α be the input voltage, current and phase angle respectively then the power factor can be evaluated by:

$$PF = \frac{V_i I_i \cos \alpha}{V_{irms} I_{irms}} \quad (1.1)$$

where the displacement factor (DPF) of the rectifier is $\cos \alpha$ in which α is precisely the phase angle between the fundamental components of V_i and I_i . It can be seen from an ideal perspective if $V_{irms} = V_i$ then

$$PF = \frac{I_i \cos \alpha}{I_{irms}} = DF \times DPF \quad (1.2)$$

$$\text{Distortion factor (DF) of the input voltage} = \frac{V_i}{V_{irms}} \quad (1.3)$$

$$\text{Total Harmonic Distortion (THD)} = \frac{\sqrt{1-DF^2}}{DF} \quad (1.4)$$

Evaluating for DF and substituting in (1.2) gives (1.4)

$$PF = \frac{DPF}{\sqrt{1+THD_i^2}} \quad (1.5)$$

It can be seen from (1.5) that the higher the THD, the lower the power factor, thus affirming the need for power factor correction in power converters. The adverse effect of high THD on PF has created attention by authorities on the quality of current absorbed from the grid. Low PF means more power would be absorbed from the grid and this comes with a very high harmonic distortion of the input line current, creating huge EMI and interferences between the equipment being power and the grid. The principle of Power factor correction is based on the input side, emulating a resistor such that the voltage varies sinusoidally in the same manner as input current. This is done by creating a sinusoidal reference with the control techniques in such that the input current follows the reference current as much as possible.[2]

1.3.2. Bridgeless boost PFC AC/DC converter review

1.3.2.1. Basic bridgeless boost PFC AC/DC converter

Bridgeless PFC converters as the name implies does not require an input bridge rectifier while maintaining the behaviour of a boost converter. This absence of bridge rectifier makes it extremely attractive in high power density application where efficiency is very critical. Here the conduction losses have been significantly reduced owing to fewer semiconductor devices that carries current from the AC source to the load. Other benefit includes low heat management requirement because of the absence of the input bridge diodes and less current stress on the high-frequency switches. Despite these benefits, it is also plunged with the drawback of high EMI, which occurs due to high reverse recovery issues coming from the high forward diode current and voltage. At high switching frequency, the huge reverse – recovery current of the diodes creates additional turn-on loses on the switches. Another

drawback is the floating input line with respect to the ground, thus the need for input voltage sensing with a low-frequency transformer or optical coupler and complex input current sensing circuit.[3], [4].

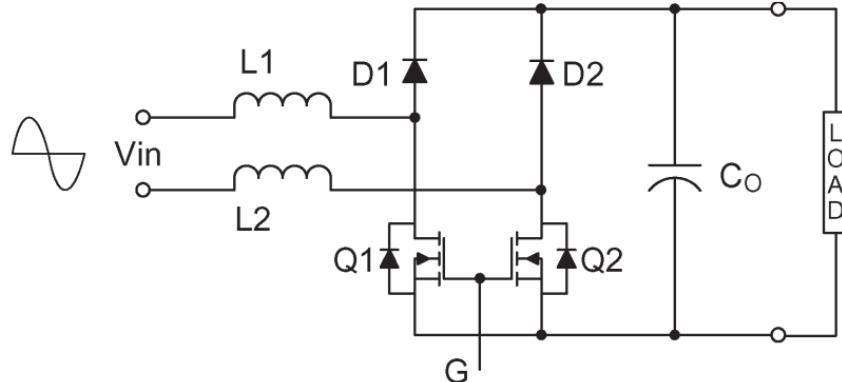


Figure 1.1 Basic bridgeless boost PFC converter[3]

1.3.2.2. Bridgeless interleaved boost (BLIL) PFC converter

This type of converter consists of two boosts connected in parallel and operating in 180 degrees out of phase of each other. This operation allows the input ripple current to be reduced since the two input inductor currents are 180 degrees out of phase, allowing them to cancel out each other, thereby reducing the input EMI noise. The conduction loss and output capacitor high-frequency ripple is also reduced due to the paralleling. The drawback is the high cost and complex control scheme needed for the implementation of the topology.[3]

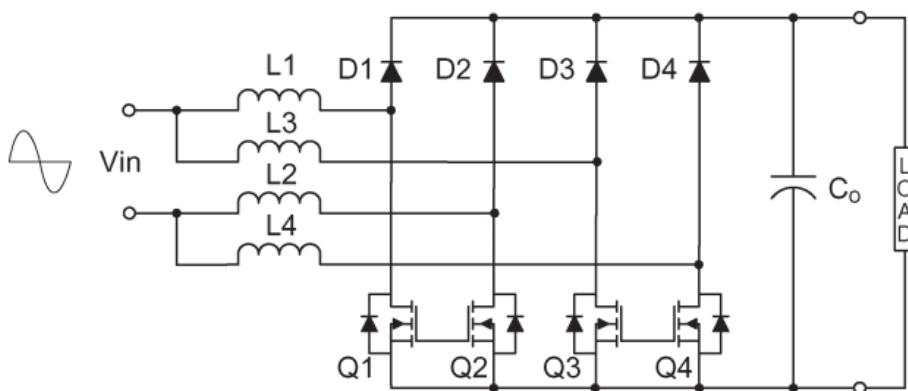


Figure 1.2 BLIL AC/DC converter [3]

1.3.2.3. Bridgeless interleaved totem – pole boost PFC topology

This topology was derived from totem pole dual boost PFC as it solves the issue of operation only in DCM and CRM. Totem pole dual boost PFC cannot operate in CCM owing to the slow reverse recovery time of the body diode of the MOSFET thus more switching losses[5]. This research work is

based on the interleave totem pole PFC integrated with an LLC tank as it overcomes the stated drawback of the totem pole dual boost PFC. Figure 1.3 shows the topology of the circuit, where diode D1 and D2 provide the current return path. Switch S2 and S4 operate as boost switches during the positive cycle and at the same time the body diode of S1, S3 and D2 conduct. S1 and S3 then conduct in the negative cycle when the input voltage Vac becomes negative and follows the opposite case of the positive operation. More details of the operation process would be discussed later in the following chapters.[5]

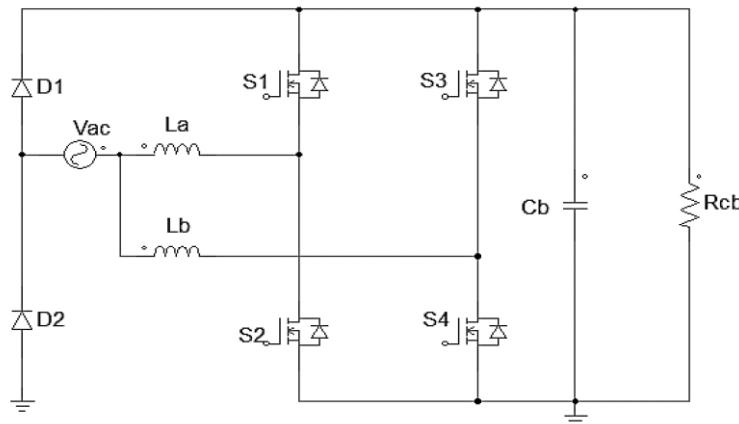


Figure 1.3 Bridgeless interleave totem-pole boost AC/DC converter

1.3.3 Average control mode PFC control techniques review

This control technique allows the inductor current to be sensed and filtered by a current error amplifier which is used to drive the input of a PWM modulator. It consists of an inner current loop which provides the ability to reduce the error between the average input current $i_{g,\text{avg}}$ and its references i_g . As seen in figure 1.4, the outer voltage loop, which is slower, is used to close the loop or generate the inner current loop reference that is compared with the measured input current. [2], [6]

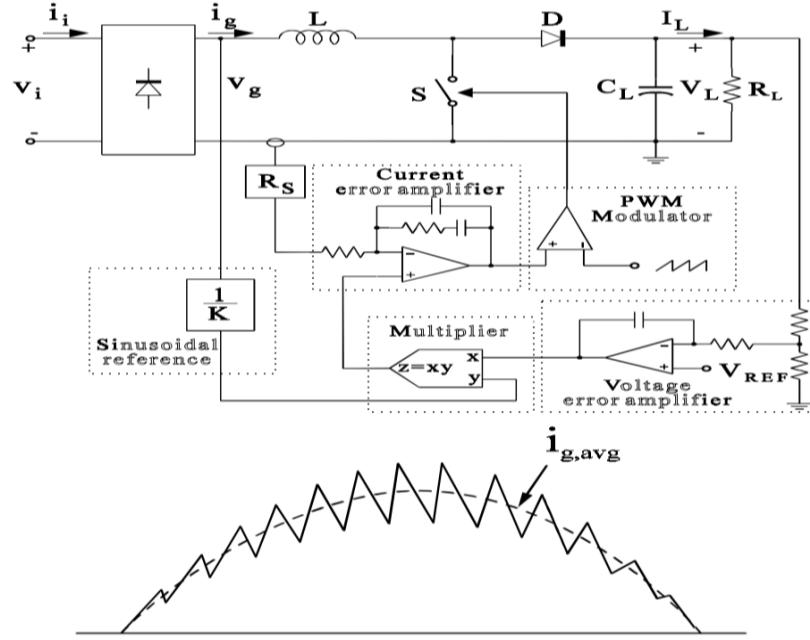


Figure 1.4. ACM for bridge PFC[2]

Figure 1.5 depicts the way the ACM scheme could be used for a bridgeless totem-pole PFC. The average current control technique is commonly used in the industry and was also used for the design carried out in this work. ACM technique solves the issue of commutation noise due to current filtering. In this way, a better input current than the peak current control technique could be achieved. The duty cycle near the zero crossings of the line voltage is almost one, thereby providing the benefit of reduced dead angle in the input current.[2], [6, p. 3].

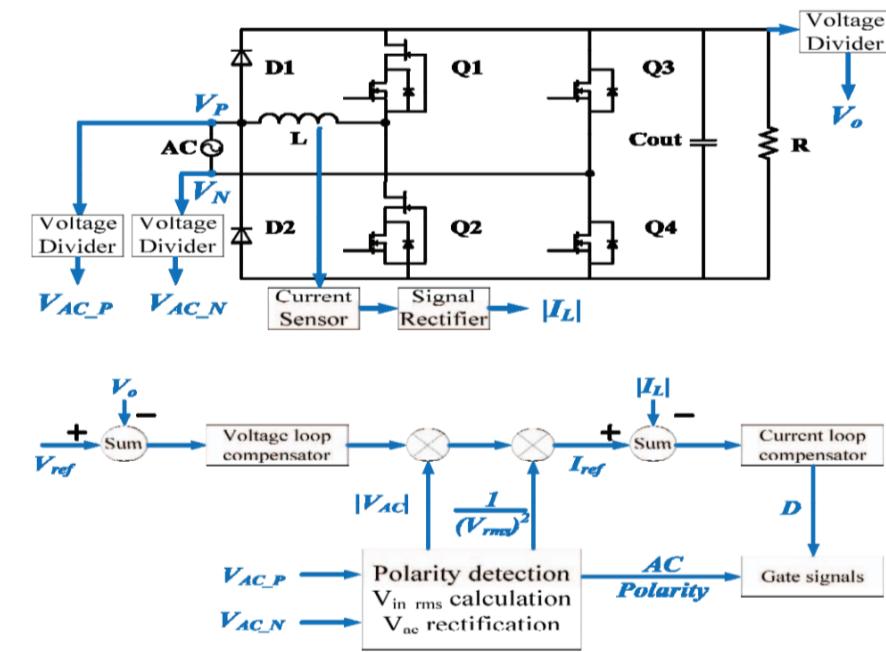


Figure 1.5. ACM for bridgeless PFC[6]

1.4 LLC circuit technology

Power converters with a high-power density and conversion efficiency are desirable in many industrial applications existing today. Conventionally, to realize high power density devices, switching frequency of the converters are usually increased, and the size and weight of the reactive component are reduced. This convectional way described gives rise to hard-switching converters which employ PWM technique to control the dynamic transfer of power from the input to the output. This makes it prone to excessive switching loss as the frequency approaches MHz order and create a tradeoff between efficiency and thermal requirement.[7]

Resonant converter solves this drawback of higher switching loss as frequency increases by providing soft-switching which allows ZVS to turn on and ZCS turn off for the MOSFETs switches and diode, respectively. The smaller size of the reactive components like transformers and inductors is also one of the tremendous benefits of such converter.

They are mainly classified into two types. The first type is the voltage-source series resonant converter, which has its load connected in series with the resonance tank making the output voltage to be derived from the resonant current. Series resonance converter (SRC) provides the benefit of overload protection, but the drawback is its output voltage been sensitive to load variation.

The second type is the current-source parallel resonant converter which has its load connected in parallel with the resonant tank. The designed circuit makes it possible to obtain the output voltage from the voltage across the resonance capacitor. The benefit of this parallel type is the absence of sensitivity to load variation, but overloading circuit protection is needed.[7]

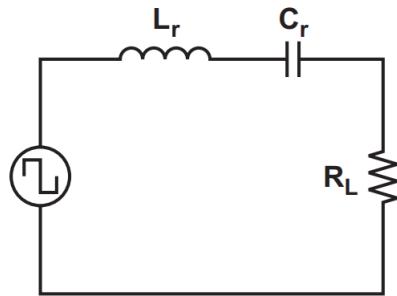


Figure 1.6 Series resonance converter

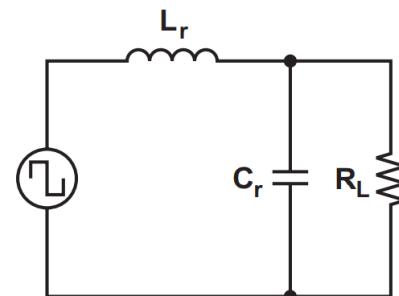


Figure 1.7. Parallel resonance converter

As described above, both resonance converter has limitations and to overcome such, LLC resonance converter was proposed. It offers the advantage of easy coupling of both resonance tank inductor L_r and L_m , wide line and load variation with little variation of switching frequency and high overall efficiency due to ZVS.[8]. This work is based on the LLC resonance converter integrated with a Bridgeless PFC circuit due to the benefit it provides.

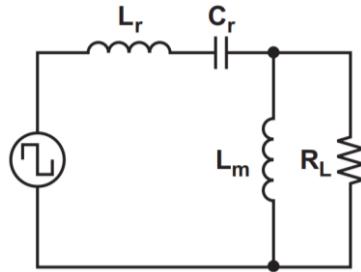


Figure 1.8. LLC circuit.

1.4.1 Operation of LLC resonance converter

LLC resonance converter has three range of operation, as shown in figure 1.9, indicating it has a peak resonance frequency which changes with variation in load. This peak resonance frequency f_r varies from the pole frequency f_p to the series resonance frequency f_o . When the circuit is not loaded $f_r=f_p$ and with an increase in load f_r approaches f_o while a short circuit $f_r=f_o$ providing the conclusion that (1.6) is always true regardless of the variation in the load and (1.7) is only valid at no load.[8]

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (1.6)$$

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \quad (1.7)$$

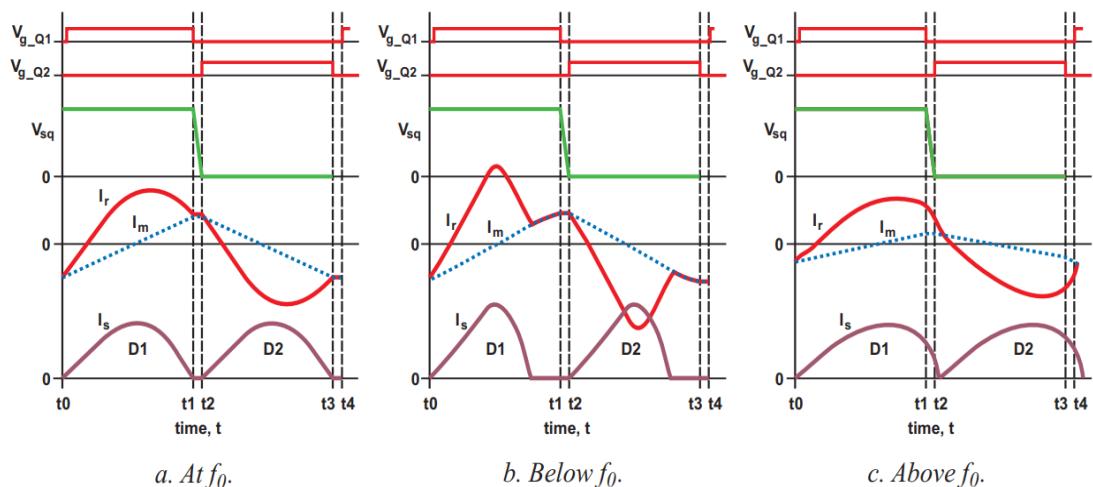


Figure 1.9. Operation of LLC resonant converter at different frequencies.[8]

Figure 1.9a occur when the switching frequency is the same as f_0 and at this stage switch Q1 with a voltage level V_{g_Q1} turns off. The resonance current i_r equals magnetizing current i_m creating a delay for Q2 turn on, thereby achieving ZVS and ZCS turn off on the output side. Figure 1.9b shows the operation below f_0 and it could be observed that i_r drops quickly to i_m , before the turn off time of Q1. At this stage, the circuit still achieves ZVS at the input side and ZCS at the secondary side, however, it creates a discontinuous conduction mode at the output diodes. If huge energy is needed by the load this behaviour will incur more conduction losses in the circuit as the more circulating current would be required by the resonance tank, ZVS would also be lost entirely if the circuit switching frequency becomes very low. Figure 1.9c shows the operation above the series resonance frequency f_0 and in this case, there is a reduction in conduction losses due to the resonant circuit operating in CCM. This offers the benefit of reduced RMS current despite load variation and provides the possibility to achieve ZVS for the switches. The problem with this model is the reverse recovery loss which occurs in the output side due to the absence of ZCS for the output diodes.[8, p. 5]

1.4.2 Modelling of LLC resonance converter

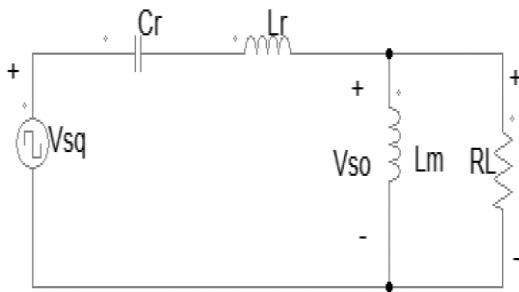


Figure 1.10. nonlinear non-sinusoidal circuit.

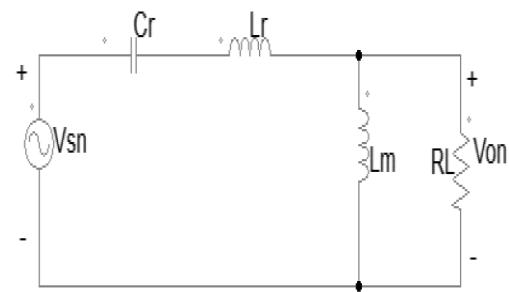


Figure 1.11. Linear sinusoidal circuit

The voltage entering the resonant tank is a sinusoidal voltage V_{sn} and the i_r is the current flowing through C_r and L_r . i_m is the current through L_m , whereas i_n is the current through R_n and V_{Cb} is the voltage across the DC bus, respectively. Then:

$$V_{sn} = \frac{2}{\pi} x V_{Cb} x \sin(2 \pi f_{sw} t) \quad (1.8)$$

From (1.8) the RMS value can be derived and express in:

$$V_{sn} = \frac{\sqrt{2}}{\pi} x V_{Cb} \quad (1.9)$$

V_{on} can be approximated to be a square wave which is extracted at the output side and thus the fundamental voltage is derived in:

$$V_{on} = \frac{4n}{\pi} x V_o x \sin(2 \pi f_{sw} t - \varphi_v) \quad (1.10)$$

φ_v is the phase angle between V_{sn} and V_{on} . The RMS of V_{on} is given by:

$$V_{on} = \frac{2\sqrt{2}}{\pi} \times nV_o \quad (1.11)$$

The fundamental component of the current through R_n is given by:

$$i_n(t) = \frac{\pi}{2} \times \frac{1}{n} \times i_o \times \sin(2\pi f_{sw}t - \varphi_i) \quad (1.12)$$

The rms of i_n is given by:

$$i_n = \frac{\pi}{2\sqrt{2}} \times \frac{1}{n} \times i_o \quad (1.13)$$

dividing (1.10) by (1.12) gives:

$$R_n = \frac{V_{on}}{i_n} = \frac{8n^2}{\pi^2} \times \frac{V_{on}}{i_n} = \frac{8n^2}{\pi^2} \times R_L \quad (1.14)$$

where i_o and V_o are the current flowing and the voltage across the output load R_L respectively, n is the turns ratio of the transformer. R_n is the resistance referring to the output load R_L .

Meanwhile the angular frequency $\omega_{sw}=2\pi f_{sw}$, capacitive reactance $X_{Cr}=\frac{1}{\omega_{Cr}}$ and inductive reactance across L_r and L_m are given by $X_{Lr} = \omega L_r$ and $X_{Lm} = \omega L_m$ respectively. Having affirmed this the RMS current flowing through L_m can be calculated using (1.15)

$$i_m = \frac{V_{on}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \times \frac{nV_o}{\omega L_m} \quad (1.15)$$

The current flowing in the series resonant circuit or the total resonance circulating current can be given by:

$$i_{rc} = \sqrt{i_m^2 + i_n^2} \quad (1.16)$$

The next step is to determine the voltage – gain function which can be compared to the common voltage gain (M_{gDC}) equation (1.17).

$$M_{gDC} = \frac{nV_o}{\frac{V_{Cb}}{2}} \quad (1.17)$$

The bus voltage as in (1.17) is converted into switching mode as shown in figure 1.8 which give rise to the ratio of bipolar square wave voltage (V_{so}) to unipolar square-wave voltage (V_{sq}) making (1.17) to be approximated to (1.18)

$$M_{gDC} \approx M_{gsw} = \frac{V_{so}}{V_{sq}} \quad (1.18)$$

Approximating with the AC voltage ratio from using figure 1.10.

$$M_{gDC} = \frac{nV_o}{\frac{V_{Cb}}{2}} \approx M_{gsw} = \frac{V_{so}}{V_{sq}} \approx M_{gAC} = \frac{V_{on}}{V_{sn}} \quad (1.19)$$

Therefore $M_{gAC} = \frac{V_{on}}{V_{sn}}$ can be regarded as the voltage transfer function, which is needed to design the output voltage controller. From figure 1.10 V_{on} and V_{sn} can be expressed in terms of L_r , L_m , C_r and R_n .

$$M_{gAC} = \frac{V_{on}}{V_{sn}} = \frac{sL_m||R_n}{sL_m||R_n + sL_r + \frac{1}{sC_r}} \quad (1.20)$$

An inductance ratio K is introduced which is needed to combine the two inductances L_m , and L_r .

$$K = \frac{L_m}{L_r} \quad (1.21)$$

The quality factor Q of the LLC circuit is giving by (1.22)

$$Q = \frac{\sqrt{L_r/C_r}}{R_n} \quad (1.22)$$

CHAPTER 2

ANALYSIS AND DESIGN OF PROPOSED CONVERTER

Several isolated PFC rectifier topologies were studied and simulated in this research work. One of the most common drawbacks not usually stated by the authors is the high voltage level of the DC bus capacitor at the input side which is mostly twice the output voltage. This drawback increases the cost of MOSFET switches needed in real-life implementation, making it violate one of the primary purposes of the research, which is the cost. The chosen topology shown in figure 2.1 is based on bridgeless interleaved totem-pole boost PFC topology which offers the benefit of reducing voltage level at the DC bus (C_b) and reduced input current ripple making the need for an EMI filter optional. The switches can achieve ZVS and ZCS on the primary and secondary side of the circuit respectively due to integration with an LLC tank. The LLC tank acts as a high pass filter at a high output voltage level, which helps attenuate the second-order harmonic component present at the output and passes the high-frequency component to the transformer. Owing to this ability, the transformer attain the benefit of reduced size.[9] The opposite is the case for low voltage, high current level, creating the need for a ripple cancellation technique at the output side. The converter operation process, followed by the design and dimensioning of the components, will be explained here.

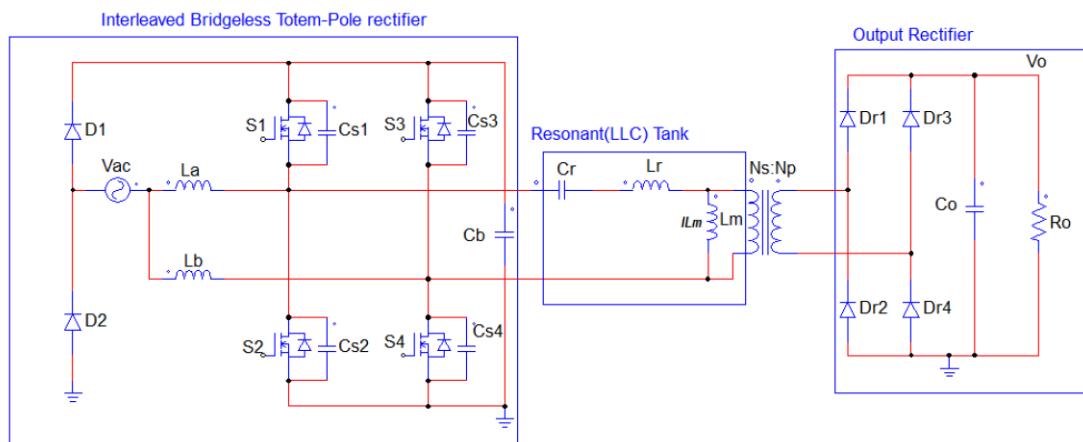


Figure 2.1. Chosen single-stage high-frequency isolated rectifier[9]

2.1 Circuit operation procedure

2.1.1 Positive half-cycle operation

The converter is operated in CCM mode with interleaving, softs switching capability and only the positive half-cycle operation would be discussed. However, the negative half cycle diagram would be shown as it is just the opposite of the positive half-cycle. Let i_{La} and i_{Lb} be the current through La and Lb respectively and V_{ac} , V_{cb} and V_o be the input, DC-bus, and output voltage, respectively.

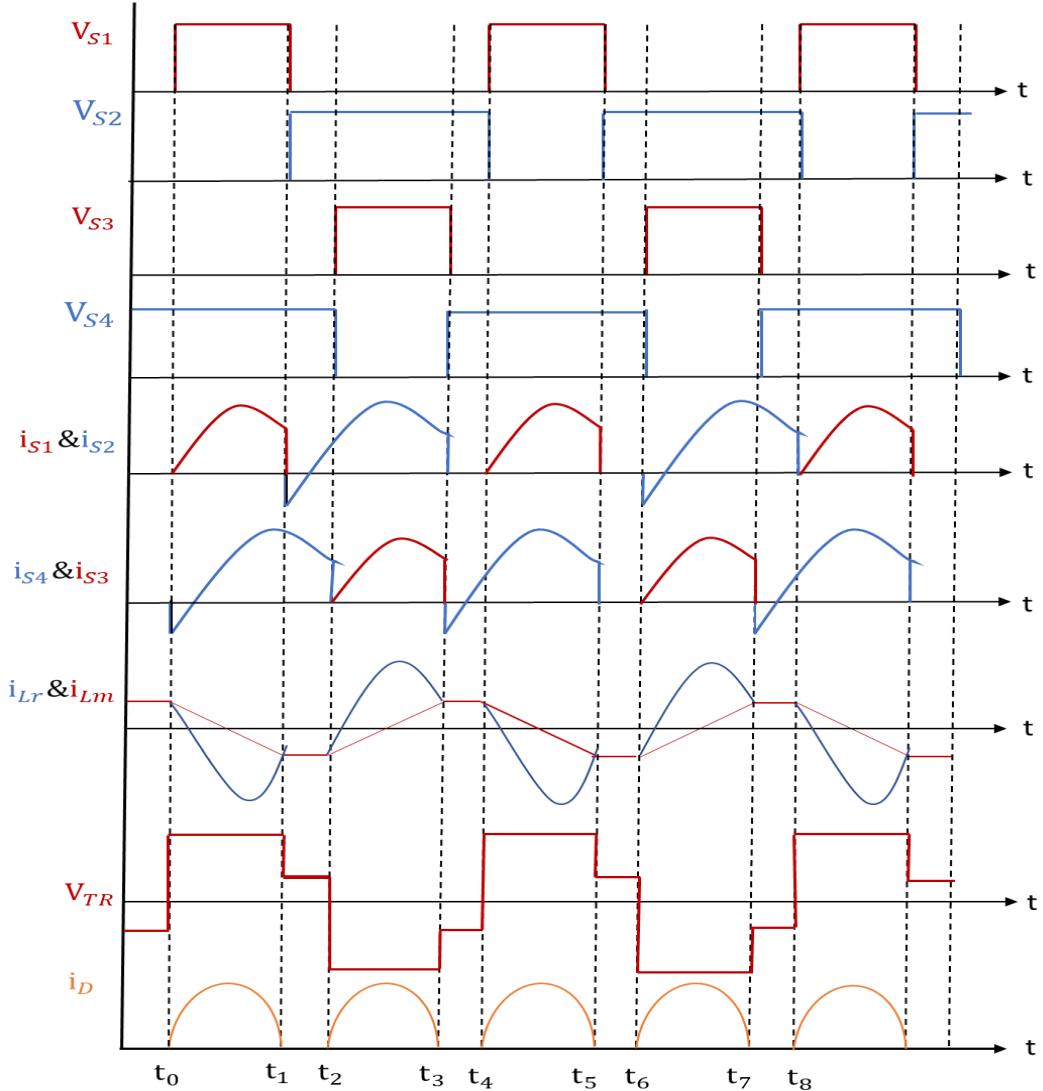


Figure 2.2. Principle waveform of the converter

Mode 1($t_0 \leq t < t_1$): This mode begins with S1 turning on at ZVS, and the input boost inductor L_a discharges linearly by transferring its energy into the dc-link capacitor C_b which stores it as electrical energy. The current through L_a discharges with a slope of $(V_{ac} - V_{dc})/L_a$. The inductor L_b is charged by

the input voltage V_{ac} and therefore, the current i_{Lb} increases. According to [9], the two respective inductor current can be described as follows:

$$i_{La}(t) = i_{La}(t_0) + \frac{V_{ac}(t) - V_{Cb}(t)}{L_a}(t - t_0) \quad (2.1)$$

$$i_{Lb}(t) = i_{Lb}(t_0) + \frac{V_{ac}(t)}{L_b}(t - t_0) \quad (2.2)$$

The bus capacitor C_b is connected to the resonance tank consisting of the resonance capacitor C_r , resonance inductance L_r and magnetizing inductance L_m at the primary side of the transformer. At this stage, the resonance tank current is greater than the magnetizing inductor current i_{Lm} making energy to be transferred to the secondary side, which in turn allow diode Dr1 and Dr4 to conduct. A point to note is that i_{Lm} increases linearly with a value of $\frac{nV_0}{L_m}$ until it reaches resonance at the point t_1 where $i_r(t)$ is equal to zero. Therefore, one can assume the following equations:

$$i_o(t) = i_r(t) - i_{Lm}(t) \quad (2.3)$$

$$i_o(t) = i_r(t) - \frac{nV_0}{L_m}(t) \quad (2.4)$$

where $n = \frac{N_s}{N_p}$ is the transformer turns

From the equation above it could be observed that the difference between the resonance current $i_r(t)$ and magnetizing current $i_{Lm}(t)$ is transferred to the output giving rise to the output current $i_o(t)$. This topology is designed to have its switching frequency to be higher than the series resonance frequency f_r making the resonance tank to be inductive in such a way that i_r lags the input voltage measured across L_a and L_b . The significant is that i_r can flow through the body diode S1 before S1 conducts, affirming the reason why S1 turns on with ZVS.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (2.5)$$

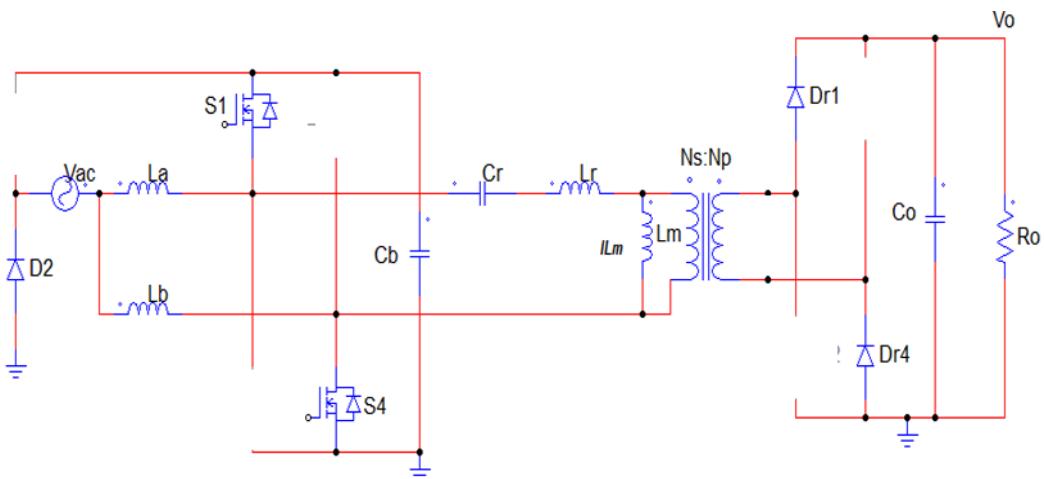


Figure 2.2. mode 1($t_0 \leq t < t_1$)

Mode 2($t_1 \leq t < t_2$): In this mode, the duty cycle is less than 0.5 as it is in the positive half cycle shown in the circuit waveforms in figure 2.2. This is also the point of resonance and the dead time interval. At this stage, the body capacitor of S1 and S3 if included, would be charging and discharging, respectively. Also, the resonance current flows through the body diode of S3 before S3 conducts, making it to turn on with ZVS. Meanwhile, the output capacitor C_o supplies the load and because the duty cycle is almost 0.5 diode Dr1 and Dr4 turns off at ZCS due to $i_r = i_{lm}$. [9], [10] The equation valid for this mode are described below:

$$i_{La}(t) = i_{La}(t_1) + \frac{V_{ac}(t) - V_{Cb}(t)}{L_a}(t - t_1) \quad (2.6)$$

$$i_{Lb}(t) = i_{Lb}(t_1) + \frac{V_{ac}(t) - V_{Cb}(t)}{L_b}(t - t_1) \quad (2.7)$$

The resonance tank at this interval consist of C_r , L_r and L_m making the expression below valid

$$f_r = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \quad (2.8)$$

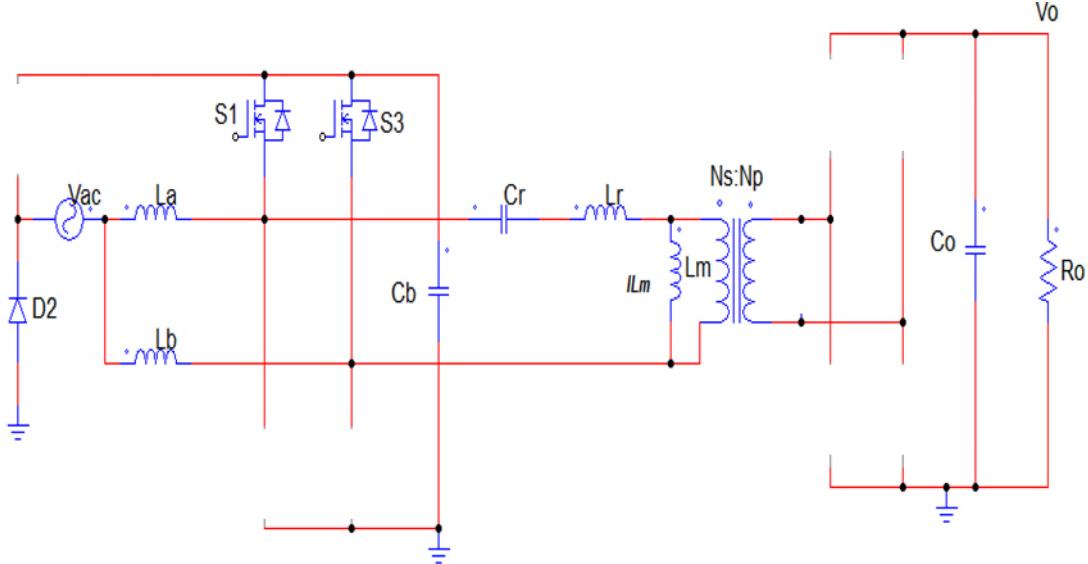


Figure 2.3. mode 2($t_1 \leq t < t_2$)

Mode 3($t_2 \leq t < t_3$): This mode begins at time t_2 as the voltage across the S4 drops to zero. The i_{Lb} decreases linearly with a slope of $(V_{ac} - V_{dc})/ L_b$ as it supplies energy to the DC link C_b making the voltage across the resonant tank to be $-V_{Cb}$. The opposite is the case for L_a , as the current across L_a increases linearly with a slope of V_{ac}/L_a showing that L_a is charged by the input voltage V_{ac} . Owing to the resonance tank being inductive and supplied with $-V_{cb}$, the resonance current i_r lags the supply voltage $-V_{cb}$. Thus i_r flow through the body diode of S2 before S2 turns on at ZVS.[9]. The transformer primary side voltage becomes negative at this stage with a clamping voltage of $-nV_o$ which is the

linearly decreasing factor of i_{Lm} . The difference between i_{Lm} and i_r is transferred to the output making Dr2 and Dr3 charge C_o and supply power to R_o . The following equations are valid for this mode:

$$i_{La}(t) = i_{La}(t_2) + \frac{V_{ac}(t)}{L_a}(t-t_2) \quad (2.9)$$

$$i_{Lb}(t) = i_{Lb}(t_2) + \frac{V_{ac}(t)-V_{Cb}(t)}{L_b}(t-t_2) \quad (2.10)$$

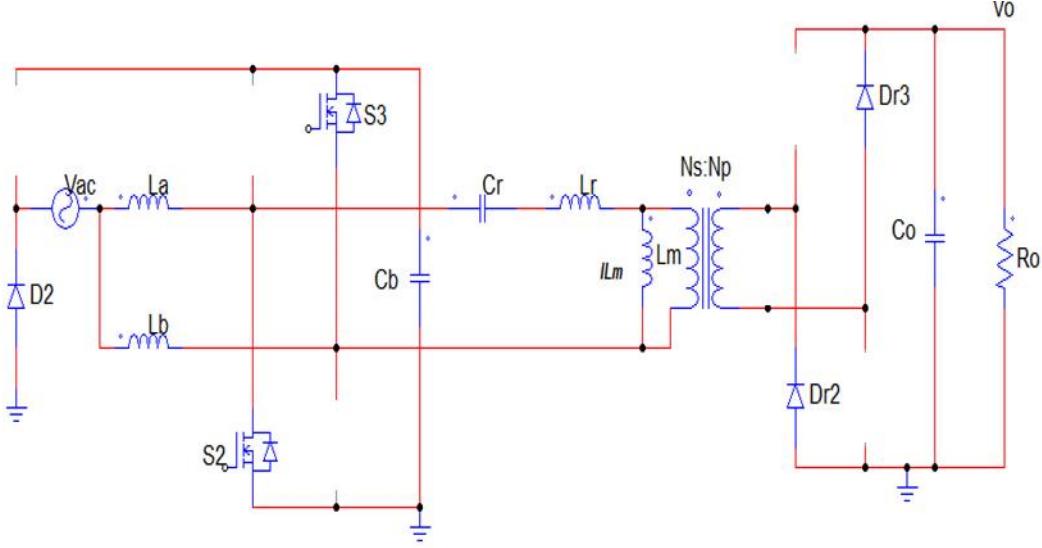


Figure 2.4. mode 3($t_2 \leq t < t_3$)

Mode 4($t_3 \leq t < t_4$): This mode is the same as mode 2, having the same valid equations but with a difference of duty cycle that is higher than 0.5. The analysis of why this is so is not described here but can be found in [9].

$$i_{La}(t) = i_{La}(t_3) + \frac{V_{Cb}(t)-V_{ac}(t)}{L_a}(t-t_3) \quad (2.11)$$

$$i_{Lb}(t) = i_{Lb}(t_3) + \frac{V_{Cb}(t)-V_{ac}(t)}{L_b}(t-t_3) \quad (2.12)$$

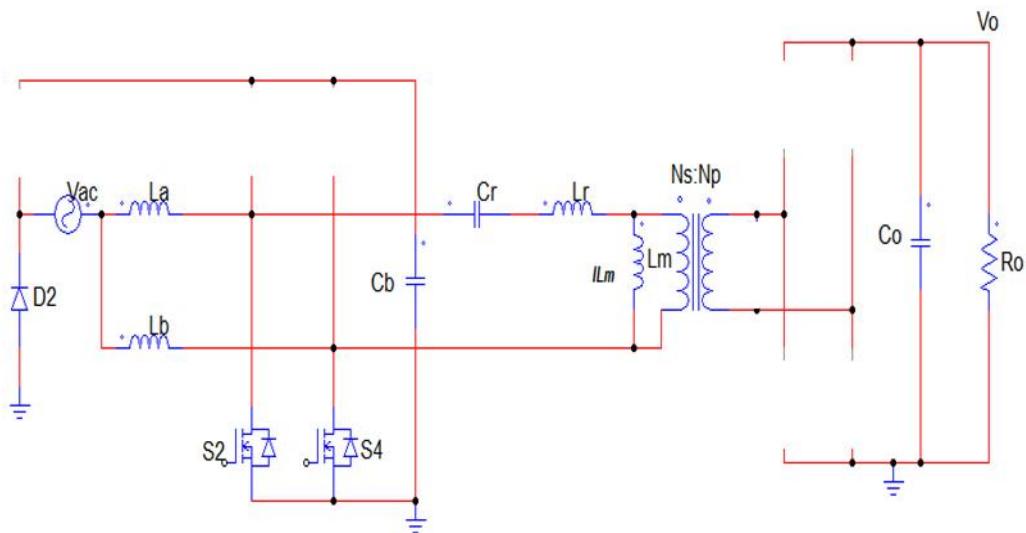


Figure 2.5. mode 4($t_3 \leq t < t_4$)

2.1.2 Negative half-cycle operation

Only the circuit diagram of the negative-cycle operation is shown below. The same positive cycle equation is valid for this cycle operation.

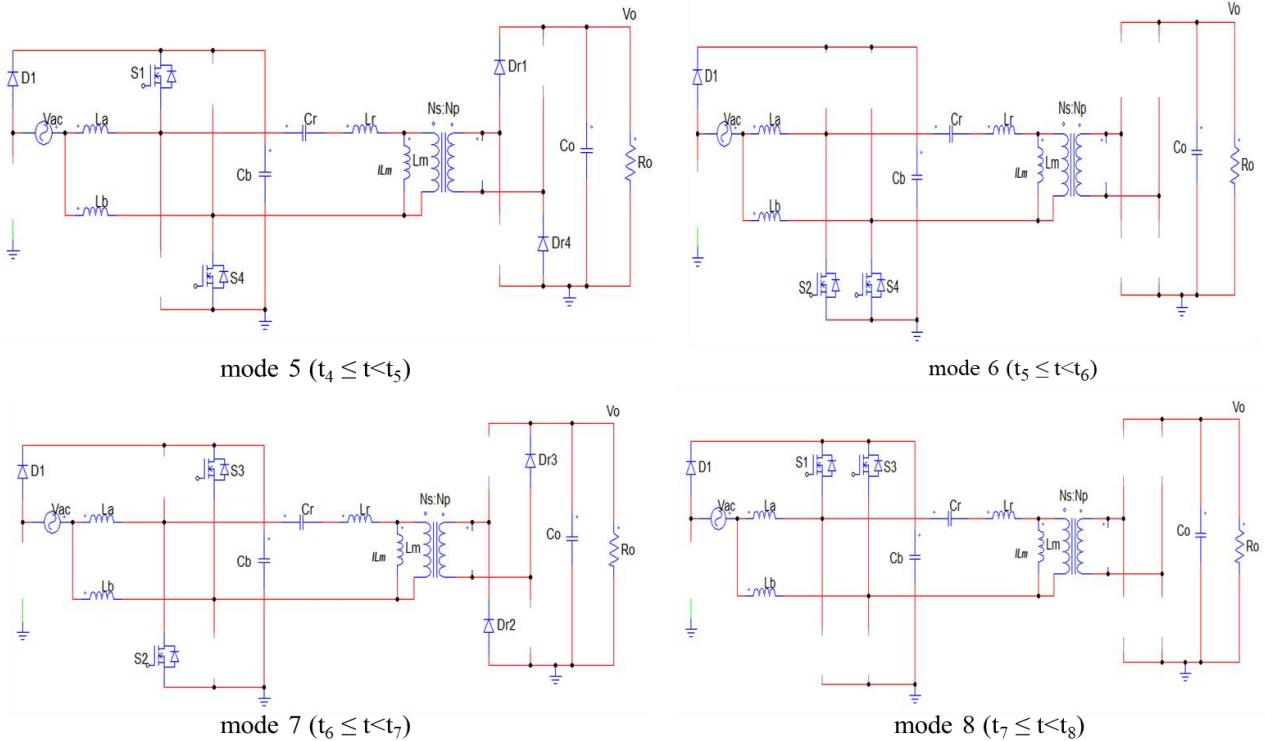


Figure 2.6. Negative cycle operational modes

2.1.3 Converter design requirement

Two design scenarios would be carried out based on the previously described topology. The first is for 3.4KW telecom/network power supply and the second is a 7KW unidirectional EV charger. The required specification by the company is displayed in table 2.1 below.

Table 2.1 Design requirement summary

	Telecom Power supply	EV Charger
Input voltage range	90VRMS~264VRMS	90Vrms~264VRMS
Frequency	45-65Hz	45-65Hz
PF	0.99	0.99
THDi	5%	5%

Output Power	3.4kW	7kW
Output Voltage range	52~58V	380- 420V
Max. Output Current	58A	17A
Holdup time	10ms Full Load	3ms Full Load
Output voltage ripple	200mV	8V
Output current ripple	200mA	1A

2.2. 3.4KW single-stage isolated interleave LLC telecom PSU design

2.2.1. PFC stage design

2.2.1.1 Input boost inductor design

Two non-coupled inductors are used whose value should be high enough to avoid DCM mode and at the same time achieve a high PF, low THDi and EMI. According to [11] the equation below is valid for calculating the value for L_a and L_b :

$$L_a = L_b = \frac{V_{ac\ min}^2}{\Delta_i P_{o\ max} f_{sw}} \left(1 - \frac{\sqrt{2}V_{ac\ min}}{P_{o\ max}}\right) \quad (2.13)$$

Δ_i is the current ripple and f_{sw} is the switching frequency, which is assumed to be 20% and 150KHz respectively. Therefore it was considered that at no-load condition $V_{ac\ min} = 90$ VRMS and at full load $V_{ac\ max} = 230$ VRMS and both cases were calculated in other to determine the best inductor size needed to avoid DCM. At no load, $L_a = L_b = 76.4\mu H$ and full load is $469\mu H$ leading to the chosen inductance value is $500\mu H$. According to [11] the maximum input current flowing through $L_a = L_b$ can be given by

$$i_{max} = i_{La\ max} = i_{Lb\ max} = \frac{\sqrt{2}P_{o\ max}}{2V_{ac\ min}} \left(1 + \frac{\Delta_i}{2}\right) \quad (2.14)$$

where Δ_i is the current ripple which is taken to be 10% and $V_{ac\ min} = 230$ VRMS at full load in this case. The maximum current is 15A.

2.2.1.2 The DC-link capacitor

According to [11] equation (2.15) is valid for the DC link capacitor value calculation, if the hold-up time is not considered. Assuming a dc-link voltage from 450-500V DC. Therefore $V_{Cb\ min} = 450V$, $V_{Cb\ nom} = 480V$ and $V_{Cb\ max} = 500V$ are considered.

$$C_b = \frac{P_{o \max}}{\Delta_v 2\pi V_{cb \min}^2 f_{ac}} = 267 \mu F \quad (2.15)$$

A required hold-up time of 10ms is needed for the design, and this is evaluated below.

$$C_b = \frac{P_{o \max} t_{hold}}{V_{cb \max}^2 - V_{cb \min}^2} = 1734.7 \mu F \quad (2.16)$$

where in this case it was assumed that $V_{cb \min} = V_{cb \text{ nom}} = 480V$, $\Delta_v = 20\% = 0.2$ and $f_{ac} = 50Hz$

Two conditions considered below influence the choice of a capacitance value in the Dc-link. The first is $f_{sw} = f_o$ and second is $f_{sw} > f_o$.

2.2.1.2.1 Condition 1 ($f_{sw} = f_o$)

At this condition, the DC-link capacitor is decoupled by the resonance tank making it no longer directly connected to the DC/DC stage, and as such, there is no ripple constraint imposed on the DC-link voltage V_{cb} as affirmed by [9]. The ripple constraint is instead imposed on the resonance tank which acts as a second-order high pass filter that helps attenuate the 100Hz low-frequency ripple at high voltage level but does not at low voltage, high current level. A low value of $15-50\mu F$ can be chosen as the DC bus capacitor C_b and an amount above this reduces the little ripple cancellation ability the resonance tank provides. The peak current of the resonant inductor also increases, leading to more losses and the need for high current output diodes and switches. However, such a reduction offers the benefit of reduced circuit size and cost.

2.2.1.2.2 Condition 2 ($f_{sw} > f_o$)

This research work for this design follows this condition as it provides better benefit than condition 1. The DC-link capacitance can be higher making (2.15) and (2.16) valid. The resonant tank owing to the higher capacitance, helps to store part of the 100Hz ripple. This condition also helps cut down the resonance inductor current by almost half because the excess energy is absorbed by the ripple cancellation stage (buck stage). This behaviour is beneficial in terms of efficiency due to lower conduction losses. It also provides longer ZVS and ZCS region of operation than condition 1. However, the drawback is a bigger circuit size and a little higher voltage stress of about 10% more than the previous condition on the switches. This is because the bus voltage rises a bit but could be easily mitigated with a good control algorithm.

2.2.2 LLC and rectifier stage design

This stage starts with the design of the transformer turns ratio, followed by choosing the right inductance (K) ratio and quality factor (Q) which allow proper sizing of C_r , L_r and L_m . The resonant tank was the first design to have an output of 80V, 43A. This would be stepped down to the required output voltage and current of 58V and 58A by the ripple cancellation stage that would be added. Let $V_{Cd\ nom} = V_{Cd\ min} = V_{Cd\ max} = 80V$ and $i_{Cd} = 43A$.

2.2.2.1 Transformer turns ratio(n)

The transformer turns ratio can be evaluated from (1.16) as expressed below

$$n = M_{gDC} \times \frac{\frac{V_{Cb\ nom}}{2}}{V_{Cd\ nom}} \mid_{M_{gDC}=1} \quad (2.17)$$

$$n = 3, \text{ where } V_{Cd\ nom} = 80V \text{ and } M_{gDC} = 1$$

2.2.2.2 Minimum and maximum DC gain ($M_{gDC\ min}$, $M_{gDC\ max}$)

$$M_{gDC\ min} = \frac{n(V_{Cd\ min} + 2V_{Fr})}{\frac{V_{Cb\ max}}{2}} \quad (2.18a)$$

$$M_{gDC\ min} = \frac{3(80V \times (1-1\%) + 1.4V)}{\frac{500V}{2}} = 0.97 \quad (2.18b)$$

$$M_{gDC\ max} = \frac{n(V_{Cd\ max} + 2V_{Fr} + V_{loss})}{\frac{V_{Cb\ min}}{2}} \quad (2.19a)$$

$$M_{gDC\ max} = \frac{3(80V \times (1+1\%) + 1.4V + 4.16V)}{\frac{450V}{2}} = 1.15 \quad (2.19b)$$

The operation is needed to be kept at the inductive region and assuming an overload current ability of 110%. Therefore $M_{gDC\ max} = 1.10 \times 1.1 = 1.27$. If the efficiency of 95% is assumed and all the losses are referred to the output side, then there would be a loss of 5% at 43A load. This results in a V_{loss} of 4.16V. $V_{Fr} = 0.7V$ is assumed for the voltage drop across the output diodes, and 1% is used to adjust the output voltage from the line and load regulation.

2.2.2.3 Selecting K and Q

Table 2.3 shows the guide for choosing K and Q and shows the impact on different designs. The table also indicates that there is a tradeoff between K and Q. Low Q and high K provides wide ZVS range and benefits of increased efficiency due to low magnetizing circulating current. However, it comes with a tradeoff of higher magnetics and lower maximum voltage gain limit. This was verified with a

voltage gain sweep C code written in C block of PSIM simulation software. This led to the chosen values of Q=0.3 and K=10, as confirmed in figure 2.7 and 2.8.

Table 2.2. The trade-off between Q and K

	Primary RMS	ZVS angle range	Turn-off current	Voltage gain	Magnetics size	Voltage stress on Cb
Q increase	lower	lower	lower	lower	higher	higher
K increase	lower	lower	lower	lower	higher	higher

To further illustrate, the figure below shows that as K increases the DC gain decreases and moving towards the right of a chosen K value, the quality factor Q decreases. The calculated DC gains shown previously in varies from 0.97 to 1.27, showing Q values can range from 0.2 to 0.45 validating the midpoint choice of a Q value of 0.3.

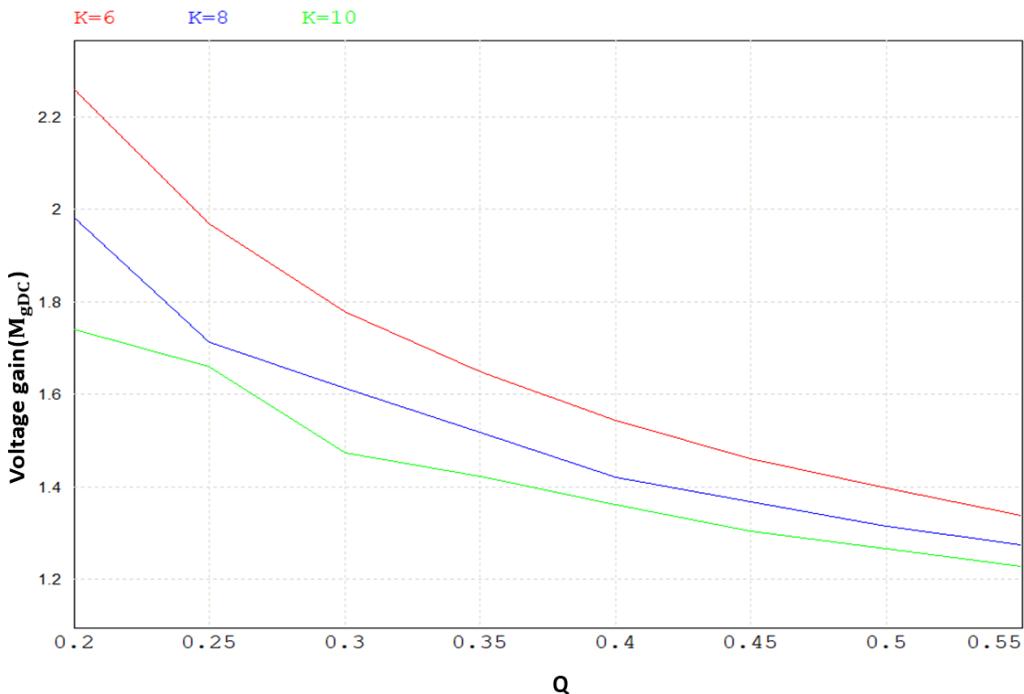


Figure 2.7. Effect of chosen K values on voltage gain and Q

2.2.2.4 Load resistance referred from the output

This was evaluated using (1.13) giving $R_n = 13.57\Omega$ (full load), 12.34Ω (110% overload).

2.2.2.5 Resonance circuit parameters design

The resonance circuit frequency was chosen to be $f_o = \frac{2}{3} f_{sw} = 100\text{KHz}$ as shown in figure 2.8 due to the advantage of having good resonance which allows natural ZVS and soft commutation

(ZCS) of the diode bridge to be achieved at a moderate range and at the same time smaller resonance inductance value.

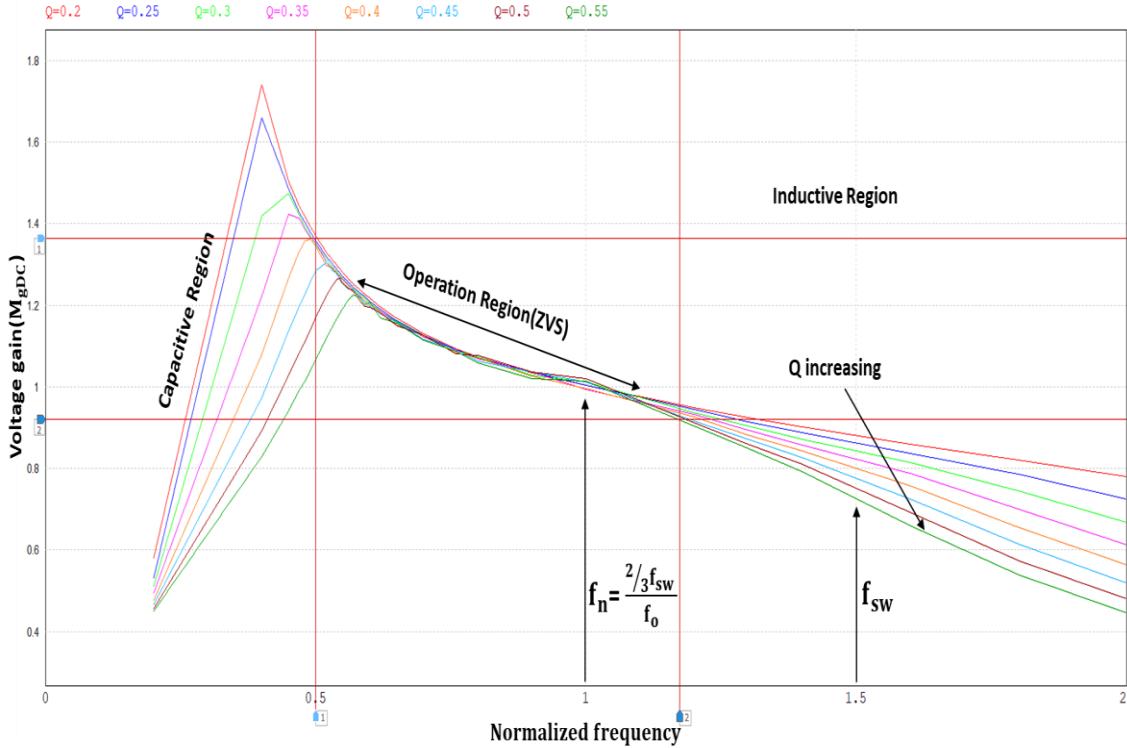


Figure 2.8. The voltage gain of the LLC circuit generated from C – code in PSIM

Moving below the chosen f_0 , gives higher dead time due to the possibility of having the resonant current i_r fallen to the magnetizing current i_{lm} before the end of the driving PWM. This might cause the transfer of power from the primary to the secondary side to stop, despite the continuous flow of the magnetizing current. This characteristic causes the diode bridge to be in the discontinuous mode and thereby requiring more circulating current in the resonant tank to meet the required power of the load. As a result, higher conduction loss is present on both sides of the circuit.

$$Cr = \frac{1}{2\pi Qf_0 Rn} = 390.95 \text{nF} \quad (2.20)$$

$$Lr = \frac{QRn}{2\pi f_0} = \frac{1}{(\pi f_0)^2 Cr} = 6.48 \mu\text{H} \quad (2.21)$$

From (1.20) $L_m = KL_r = 64.8 \mu\text{H}$. It could be observed that the designed met the required specification, and the following frequency specification could be interpolated from the normalized frequency of the plot in Figure 2.9. as shown in (2.22).

$$f_n = \frac{2/3 f_{sw}}{f_0} \quad (2.22)$$

f_{n_max} occurs at $M_{gDC\ min}$ and f_{n_min} occurs at $M_{gDC\ max}$ looking at these gain values extracted from figure 2.8 in figure 2.9 below. Therefore: $f_{o_max} = 1.11 \times 100\text{KHz} = 110\text{KHz}$ and $f_{o_min}=0.55 \times 100\text{KHz} = 55\text{KHz}$. This shows that the converter exhibits a wide natural ZVS range of operation due to the very low Q and high value of K.

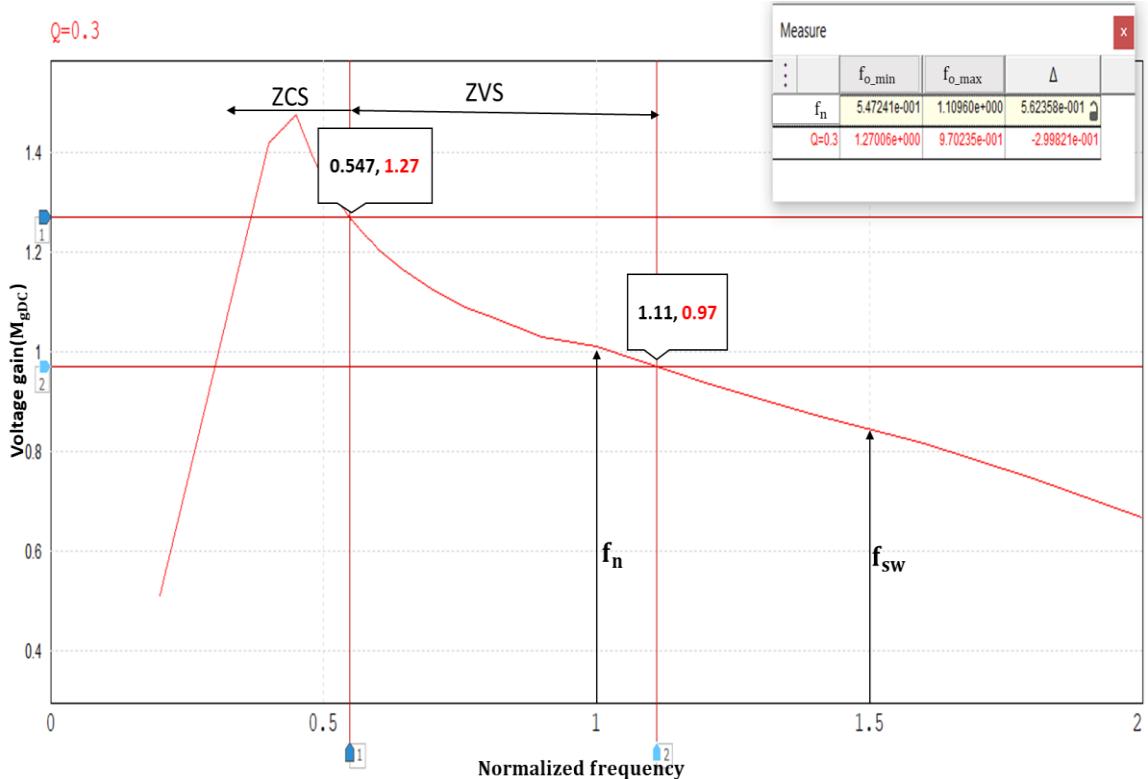


Figure 2.9. Voltage gain vs normalized frequency at chosen $Q = 0.3$

2.2.2.6 Primary side currents

The assumption of 110% overload was used to determine the RMS load current i_n of the primary side at f_{o_min} . This can be evaluated by modifying (1.12) to below.

$$i_n = \frac{\pi}{2\sqrt{2}} \times \frac{i_{cd} \times 1.1}{n} = 17.51\text{A} \quad (2.22)$$

The RMS magnetizing current i_m could also follow the same approach and was evaluated here:

$$i_m = \frac{2\sqrt{2}}{\pi} \times \frac{nV_{cd}}{2\pi f_{o_min} L_m} = 9.65\text{A} \quad (2.23)$$

The total resonance current circulating in the circuit is given by (1.15) which results in:

$$i_{rc} = \sqrt{i_m^2 + i_n^2} = 19.99\text{A.}$$

This is the transformer primary winding current at f_{o_min} . The peak current of the primary winding is given by:

$$i_{p_pk} = \sqrt{2} i_{rc} = 28.28\text{A} \quad (2.24)$$

2.2.2.7 Secondary side currents

This is the RMS current referred from the primary side and is evaluated as

$$i_{n_s} = n i_n = 17.51A \times 3 = 52.54A \quad (2.25)$$

The transformer used is single winding transformer therefore the peak current in the winding is given by:

$$i_{s_pk} = \sqrt{2}i_{n_s} = 74.29A \quad (2.26)$$

2.2.2.8 Resonance inductor specification

The inductor value is $L_r = 6.48\mu H$ and the resonance current flowing through the resonance inductor is given by (2.3) which modifies to:

$$i_r = i_{Lm} + i_{Cd} \quad (2.27)$$

$i_r = 52.65A$ which is the RMS current of the resonance inductor and the peak current is $i_{r_pk} = 74.46A$. The terminal voltage is the bus voltage that is $V_{Lr} = V_{cb \max} = 500V$.

2.2.2.9 Resonance capacitor specification

The capacitor value is $C_r = 390.95nF$ whose voltage ratings must be derated with regards to the f_{o_min} as shown below

$$V_{Cr} = \frac{i_r}{2\pi f_{o_min} C_r} = 389.69V \quad (2.28)$$

$$V_{Cr_pk} = \frac{\sqrt{2}V_{Cr}}{2} + \frac{V_{cb \max}}{4} = 400.56V \quad (2.29)$$

The resonance capacitor rating is chosen to be $390.95nF$, at $450V$.

2.2.2.10 Primary side MOSFETs ratings

The MOSFETs voltage rating is the voltage of the DC – bus which is $V_{Cb \max}(500V)$. The chosen MOSFETs voltage rating is $650V$. The MOSFETs initial startup current could be as high as the resonance inductor current. Using the same assumed overload of 110% gives RMS current in (2.29).

$$i_{mos_1} = i_{mos_2} = i_{mos_3} = i_{mos_4} = 1.1 \times i_r = 57.91A \quad (2.30)$$

Therefore, a MOSFET with an RMS current of $60A$ could be used.

2.2.2.11 ZVS operation design

The requirement for ZVS has already been met due to enough inductive energy present in the circuit. The ZVS dead time is verified below. Typical MOSFETs of $650V$ usually have a $C_{ds} \approx 200pF$ and for this reason the worst-case lowest magnetizing current is calculated as:

$$i_{m_min} = \frac{2\sqrt{2}}{\pi} \times \frac{nV_{cd}}{2\pi f_{sw} L_m} = 3.54A \quad (2.31)$$

$$i_{m_min_pk} = 5.0A$$

For ZVS to be achieved equation 2.31 must be satisfied

$$\frac{1}{2}(L_m + L_r) \times i_{m_min_pk} \geq \frac{1}{2}(2C_{ds} V_{cb_max}^2) \quad (2.32)$$

$178.2\mu J \geq 50\mu J$ was calculated verifying (2.32)

$$t_{dead} \geq 16C_{ds}f_{sw}L_m \quad (2.33)$$

$t_{dead} \geq 31.1ns$ showing t_{dead} of 32ns will meet the design requirement. This low dead-time is also beneficial as it also improves efficiency.

2.2.2.12 Bridge rectifier design

The voltage rating of the diode is evaluated below

$$V_{bridge} = \frac{V_{cb_max}}{n} \times 2 = 166.7V$$

$$i_{Dr1} = i_{Dr2} = i_{Dr3} = i_{Dr4} = \frac{\sqrt{2}i_{n_s}}{\pi} \times 1.1 = 26.02A \quad (2.34)$$

The RMS current rating of the diode bridge can be calculated from (2.34), and a factor of 1.1, which is the assumed overload factor was used to multiply the diode current rating. The diode rating must be able to withstand the peak current that is caused by the resonance inductor current i_r at the primary side. An RMS voltage and current rating of 180V and 30A are specified.

2.2.3 Active ripple cancellation circuit design

This stage employs the use of buck circuit topology seen in figure 2.10. It performs two functions which are to step down the voltage from 80V to 58V and cancels out entirely the 100Hz ripple issue with the single-stage PFC. Therefore, the ripple cancellation circuit design follows a buck converter design process.

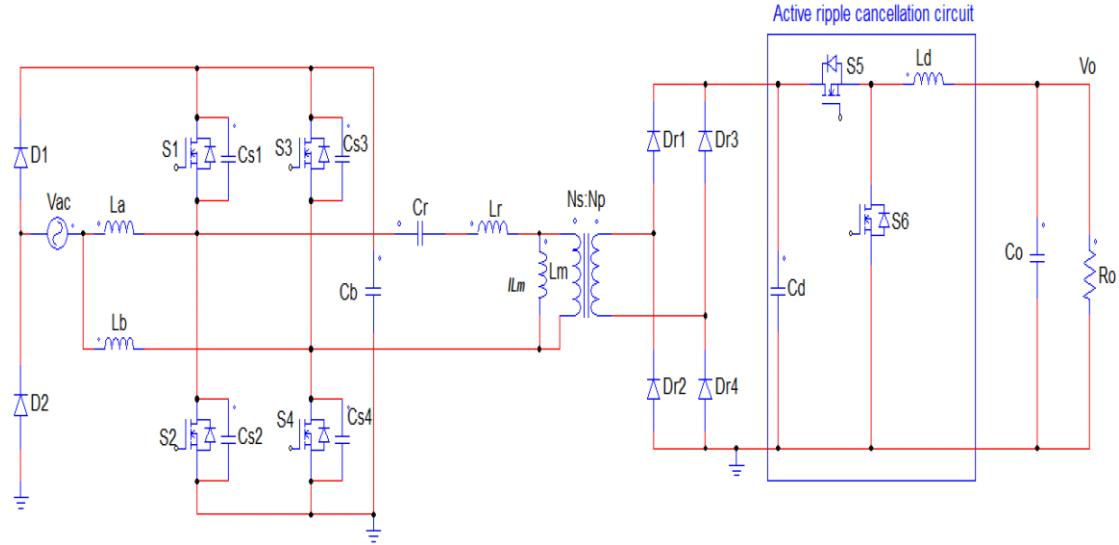


Figure 2.10. Rectifier with proposed active ripple cancellation circuit

2.2.3.1 Decoupling capacitor (C_d)

From figure 2.10, C_d is the decoupling capacitor meant to store the voltage ripple coming from the rectifier, and according to [12], the optimized value for the design is calculated below.

$$C_d = \frac{i_{Ld_pk} D_{max}}{\Delta V_{Cd} f_{sw}} = 2803.33 \mu F \quad (2.35)$$

$$i_{rec_pk} = \frac{\pi}{2\sqrt{2}} \times i_{Cd} = 47.76 A \quad (2.36)$$

where $D_{max} = \frac{V_o}{V_{Cd}}$ with V_{Cd} being 80V and ΔV_{Cd} is the voltage ripple across the rectifier, which is assumed to be 10%. C_d of 3000 μ F, 150V was chosen to reduce the ripple design constraint on the inductor L_d . However, if a capacitance less than the calculated value above is used, then a more significant inductance would be needed to maintain the voltage ripple within the range of 200mV specified for the research work.

2.2.3.2 Output MOSFETs switches

The input voltage to the switches varies between 80-100V, with a load current of 58A and a switching frequency of 150KHz, leading to the specification of 150V, 60A MOSFETs for the design.

2.2.3.3 Output inductor (L_d)

The inductor, in this case, works in CCM and a peak to peak variation of the inductor current is assumed to be 1.5% of 58A, which in this case meet the output ripple requirement. L_d was calculated from (2.37).

$$L_d = \frac{V_o (1 - D_{max})}{\Delta i_{Ld} f_{sw}} = 122.22 \mu H \quad (2.37)$$

The RMS of the inductor current can be determined from (2.36)

$$i_{Ld,RMS} = \sqrt{i_{Ld}^2 + \left(\frac{\Delta i_{Ld}/2}{\sqrt{3}}\right)^2} = 58A \quad (2.38)$$

2.2.3.4 Output capacitor rating (C_o)

A hold-up time (t_{hold}) of 2ms is assumed for the design. The required output voltage/Current (V_o/i_o) is 58V/58A and the maximum allowed voltage/current ripple ($V_{o,pk,pk}/i_{o,pk,pk}$) is 200mV/200mA. In order to meet the above specifications of 200mV, the maximum ESR is first estimated from (2.39).

$$ESR_{max} = \frac{V_{o,pk,pk}}{i_o} = \frac{200mV}{58A} = 3.45m\Omega \quad (2.39)$$

According to [13] the capacitance value is calculated as shown below. A capacitance of 2000 μ F, 60V with an ESR_{max} value of 3.45m Ω is specified.

$$C_o = \frac{i_{o,pk,pk} \times t_{hold}}{V_{o,pk,pk} - (i_{o,pk,pk} \times ESR_{max})} = 2000\mu F \quad (2.40)$$

Table 2.3. Rectifier design specification summary

PFC stage component ratings	
Boost inductor ($L_a=L_b$)	500 μ H
DC-link capacitor (C_b)	2000 μ F, 600V
Transformer RMS ratings	
Turns ratio ($N_p : N_s$)	3:1
Voltage of primary winding:	500VAC
Primary winding rated current	20A
Voltage of secondary winding:	170VAC
secondary winding rated current	60A
No load frequency	110KHz
Full load frequency	55KHz
LLC and Rectifier stage components RMS ratings	
Resonance inductor voltage and current rating	6.48 μ H, 500V, 60A
Magnetizing inductor	64.8 μ H, 500V, 20A
Resonance capacitor voltage rating	390.95nF, 450V
Primary side MOSFETs ratings	650V, 60A
ZVS capacitor ratings ($C_{s1} - C_{s3}$)	650V, 200pF
Output Rectifier diodes ratings (Dr1-Dr4)	180V, 30A
Ripple cancellation stage components RMS ratings	
Decoupling capacitor (C_d)	3000 μ F, 150V
MOSFETs ratings	150V, 60A
Inductor (L_d)	123 μ H, 60V, 58A
Capacitor (C_o)	2000 μ F, 60V, ESR _{max} = 3.45m Ω

2.2.4 Control design

The proposed control system for the circuit is presented in figure 2.11, and it consists of two stages, each having a two-loop cascaded control structure. The first stage is the PFC control which made use of ACM control technique, and the second is the ripple cancellation circuit control stage. The two feedback loops in each control structure are the inner current and the outer voltage control loops, respectively. The purpose of the separate PFC control, in this case, is to make sure that the DC bus voltage is maintained within the specified limit DC reference value of 450-500V by eliminating its non-minimum phase behaviour. The outer loops compare the measured DC – bus voltage (V_{Cb}) with the constant DC reference value (V_{ref}) to generate an error signal.

This signal is fed into the voltage PI controller with an output that is multiplied with the absolute value of the measured input AC voltage ((V_{ac}) to generate the current reference (I_{ref}). The inner loop which is the current loop then takes in the calculations input AC current of the inductor i_{in} , and compare it with the reference current (I_{ref}) to generate an error signal. The signal is then fed into a PI controller to produces an output boost duty cycle supplied to the PWM system. A duty-ratio, feed-ward control as shown in the same figure is also implemented in the PFC control stage to track the behaviour of the decoupling capacitor voltage (V_{Cd}) and the output voltage (V_o). The purpose of this is to synchronize the control systems together and prevent the excessive rise of V_{Cb} and V_{Cd} when there is a sudden load change in the circuit.

The second stage is the ripple cancellation stage which makes use of a type 3 controller to control the inner loop and PI controller to control the output voltage (V_o). The type-3 controller was chosen as it provides robust and better stability for the current control while the purpose of using PI for the outer loop is due to the quick settling time it offers when tested against a type-3 controller.

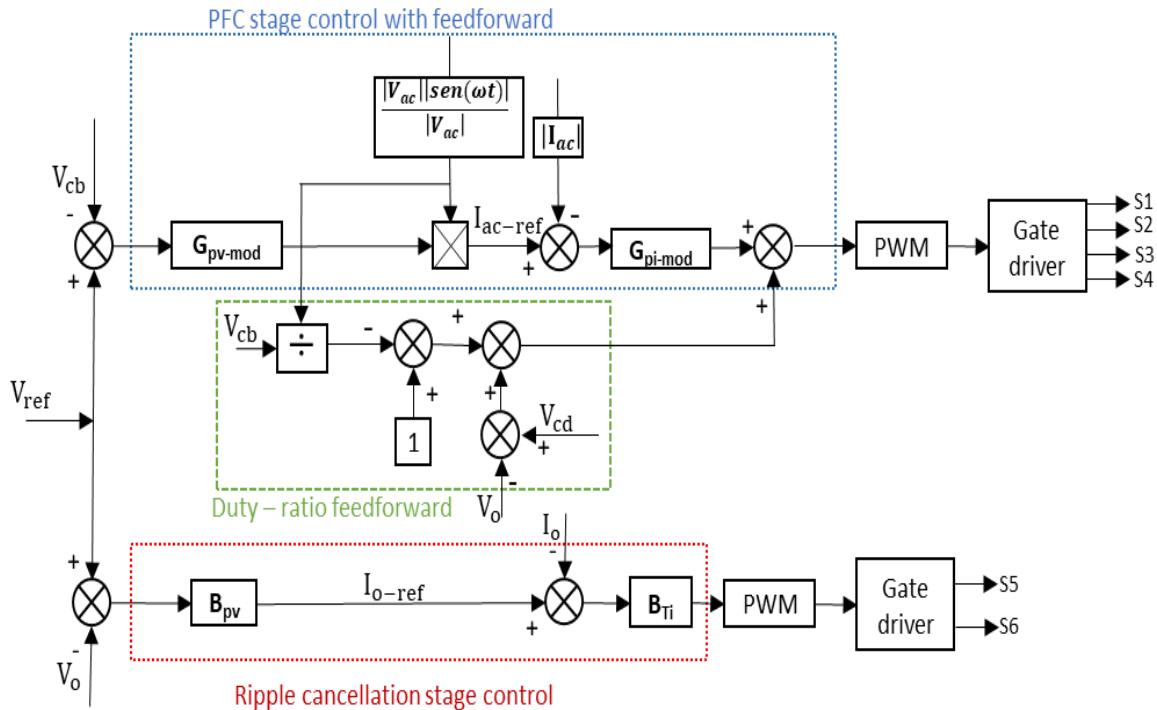


Figure 2.11. Proposed control scheme for the converter

2.2.4.1 PFC stage current loop control design

Figure 2.12 shows the small-signal model of the current loop and in this case $G_{pi-mod}(s)$ is the modified current controller, $T_{PWM_{1,2}}$ is the PWM model, $G_{id}(s)$ is the duty to current transfer function and K_i is the sample ratio of the inductor current. All control input parameters are normalized to have an amplitude of 1.

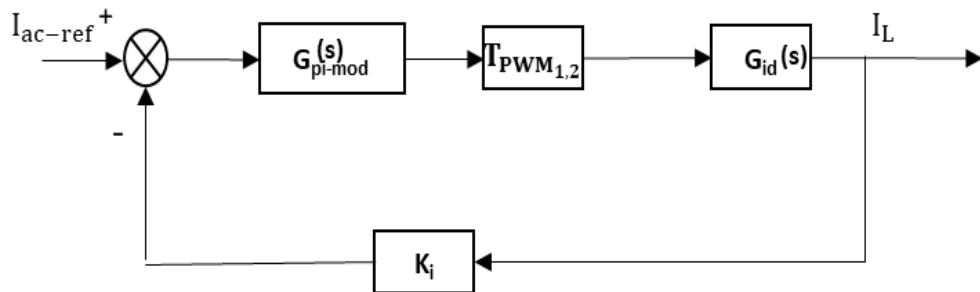


Figure 2.12. current control loop.

2.2.4.1.1 Modulator transfer function

This stage allows the duty cycle d , generated by the controller to be compared with a triangular voltage source. The triangular voltage source is selected to have a unitary amplitude and f_{sw} . The transfer function of the modulator is shown in (2.41).

$$T_{\text{PWM}_1} = \frac{1}{V_{\text{tri}}} = 1 \quad (2.41)$$

$$T_{\text{PWM}_2} = \frac{1}{V_{\text{tri}(\phi=180)}} = 1 \quad (2.42)$$

T_{PWM_2} is applicable to the interleave leg of the circuit where ϕ is the phase delay, which is 180.

2.2.4.1.2 Current transfer function

[14] derived the current transfer function of a totem pole PFC as shown in (2.43)

$$G_{\text{id}}(s) = \frac{V_{\text{cb}}(sC_{\text{b}} + \frac{2}{R_{\text{cb}}})}{LC_{\text{b}}s^2 + \frac{L}{R_{\text{cb}}}s + (1-d)^2} \quad (2.43)$$

where $L_a = L_b = \frac{L}{2}$ gives $L=1\text{mH}$ and $d = 1 - \frac{V_{\text{ac}}}{V_{\text{cb}}} = 0.5$

A bus voltage (V_{cb}) of 480V is needed to be maintained. Therefore the calculated output resistance required to give such voltage is $R_{\text{cb}} = 67.76\Omega$ for the power of 3.4KW. Computing these values gives.

$$G_{\text{id}}(s) = \frac{0.96s + 14.17}{2e^{-6}s^2 + 1.476e^{-5}s + 0.25} \quad (2.44)$$

$$r_{1,2} = -0.0369 \pm 3.5353i \quad (2.45)$$

(2.45) shows the complex conjugate roots of $G_{\text{id}}(s)$ with its real components being negative, depicting that the current system of a bridgeless interleave totem pole PFC boost converter is naturally stable in open loop.

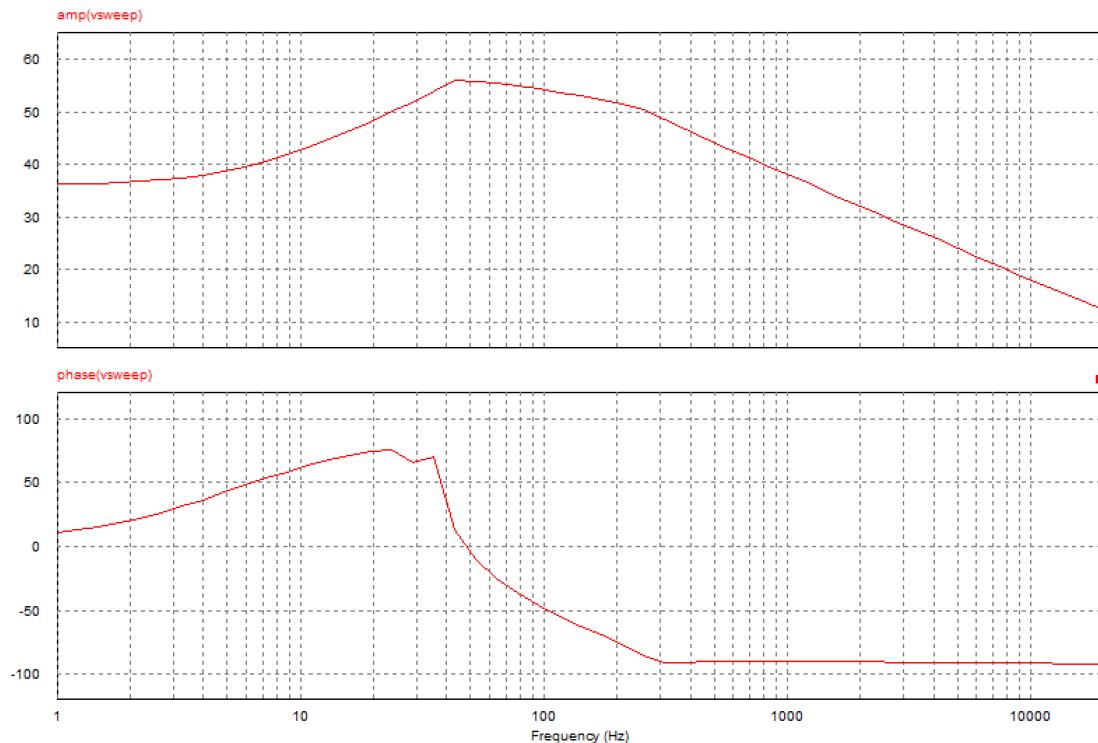


Figure 2.13. Bode plot of the $G_{\text{id}}(s)$ using AC sweep in PSIM

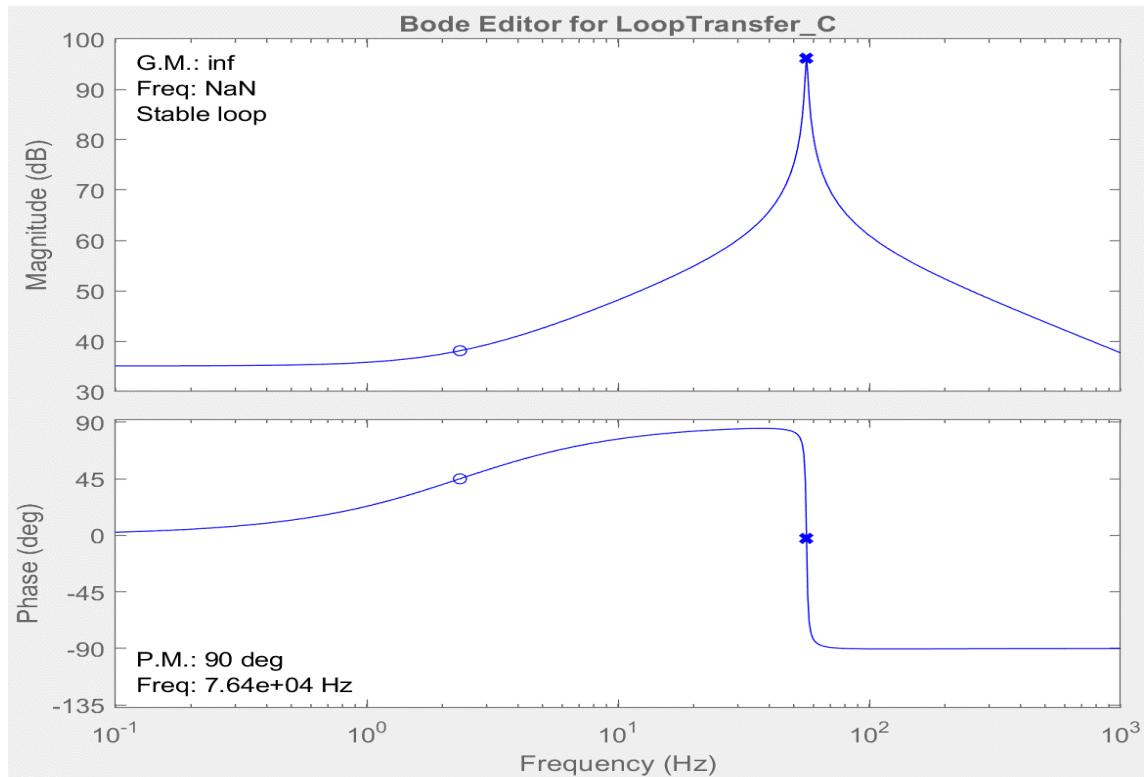


Figure 2.14. Bode plot of the $G_{id}(s)$ using MATLAB SISO tool

Figure 2.13 and 2.14 show the frequency response behaviour of the current transfer function is the same when generated from the designed circuit in PSIM and MATLAB. The only difference is PSIM considered the non – ideal characteristics of the circuit as oppose to that plotted in MATLAB. The MATLAB plot shows the location of the low-frequency zero and high-frequency pole with high peaking that needs to be cancelled out. This would be done with the help of a modified (second-order) PI current controller which would be designed in the next section.

2.2.4.1.3 Current controller transfer function

A modified PI controller was chosen over the conventional PI controller, due to the better control dynamics it provides and the benefit of not needing a separate low pass filter for the measured current. The transfer function of a conventional PI is given by (2.46).

$$G_{pi} = \frac{K_{pi}s + K_{ii}}{s} \quad (2.46)$$

$$\text{In Laplace form: } G_{pi} = \frac{K_{pi}(1+Ts)}{Ts} \quad (2.47)$$

where the time constant $T = \frac{K_{pi}}{K_{ii}}$

A modified PI controller transfer function consists of a pole at a frequency $f_p = \frac{\omega_p}{2\pi}$ is given by (2.48).

$$G_{\text{pi-mod}} = \frac{K_{\text{pi}}(1+Ts)}{Ts} \times \frac{1}{1+T_p s} \quad (2.48)$$

where $T_p = \frac{1}{2\pi f_p}$

2.2.4.1.4 Open and close loop transfer function

This stage concludes the design of the current control loop and the following criteria below was used.

- a. The value K_{pi} and K_{ii} are selected such that the current loop bandwidth (f_{ci}) in the close system satisfies crossover frequency $f_{ci} \leq 10f_{sw}$.
- b. The pole frequency f_p when using the modified PI must be selected to be $2f_{ci}$.
- c. The phase margin was maintained below 60 degrees. This helps in maintaining the current close-loop response on a 3dB line beyond 100Hz. This behaviour allows the voltage loop to attenuate the part of the 100Hz frequency and adequately track the voltage of the DC – bus.

The open-loop transfer function without the controller is expressed as

$$G_{\text{op}}(s) = K_i \times T_{\text{PWM}_{1,2}} \times G_{id}(s) \quad (2.49)$$

The maximum input current (I_{in}) needed was calculated previously from (2.12) which is 15A. Since all parameters are normalized to 1 therefore $K_i = 1/I_{in}$

The close loop transfer function with the second-order PI controller is given in (2.50)

$$G_{i_clos}(s) = \frac{I_L}{I_{ac_ref}} = \frac{G_{id}(s) G_{\text{pi-mod}}(s)}{1 + G_{id}(s) G_{\text{pi-mod}}(s)} \quad (2.50)$$

$G_{\text{pi-mod}}$ was designed to have a bandwidth of 15KHz with a pole frequency of 30KHz. The transfer function of the current controller $G_{\text{pi-mod}}(s)$ when computed in MATLAB is expressed by (2.51)

$$G_{\text{pi-mod}}(s) = \frac{2.61(1+1.67e-5s)}{1.67e-5s} \times \frac{1}{1+5.31e-6s} \quad (2.51)$$

From (2.51) $K_{\text{pi}} = 2.61$ and $T_i = 16.7\mu\text{s}$ and $T_p = 5.31\mu\text{s}$, $f_p = 30\text{KHz}$

The above values are used to verify the current control design done in SmartCtrl software which give $K_{\text{pi}} = 2.65$ and $T_i = 18.06\mu\text{s}$.

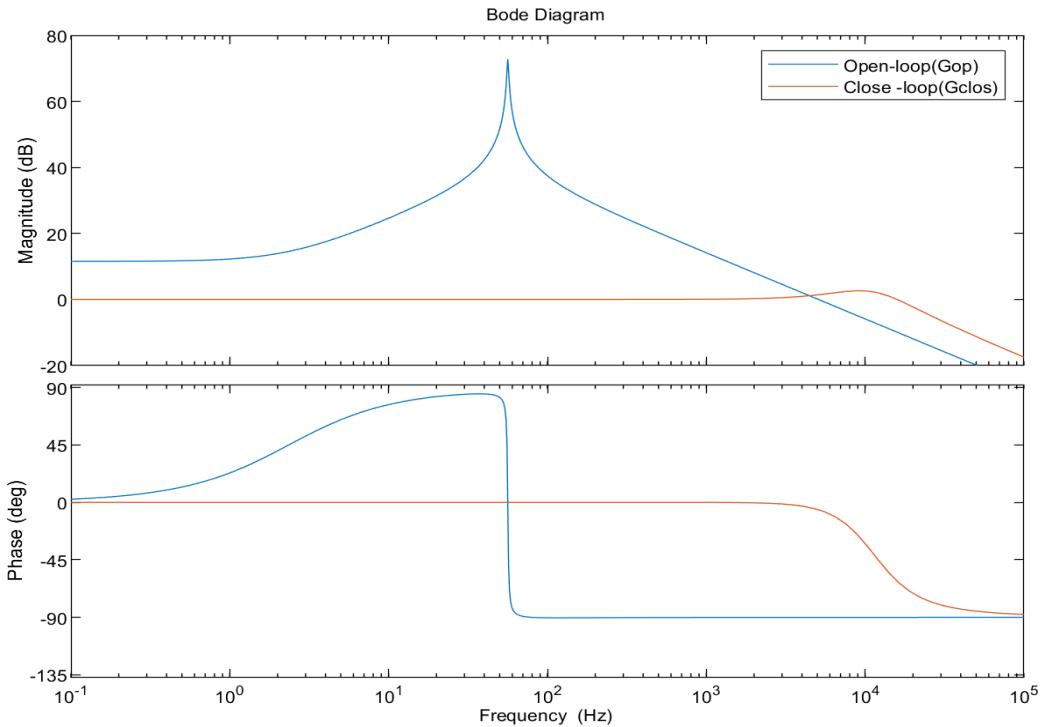


Figure 2.15. Bode plot of the $G_{\text{clos}}(s)$ and $G_{\text{op}}(s)$ using MATLAB

Figure 2.15. allow the comparison between the close and open-loop behaviour of the system. The close- loop reduces the resonance peak while giving a unity gain for frequency below 1KHz. The pole frequency allows the filtering of the switching frequency noise, confirming the functionality of a low pass filter.

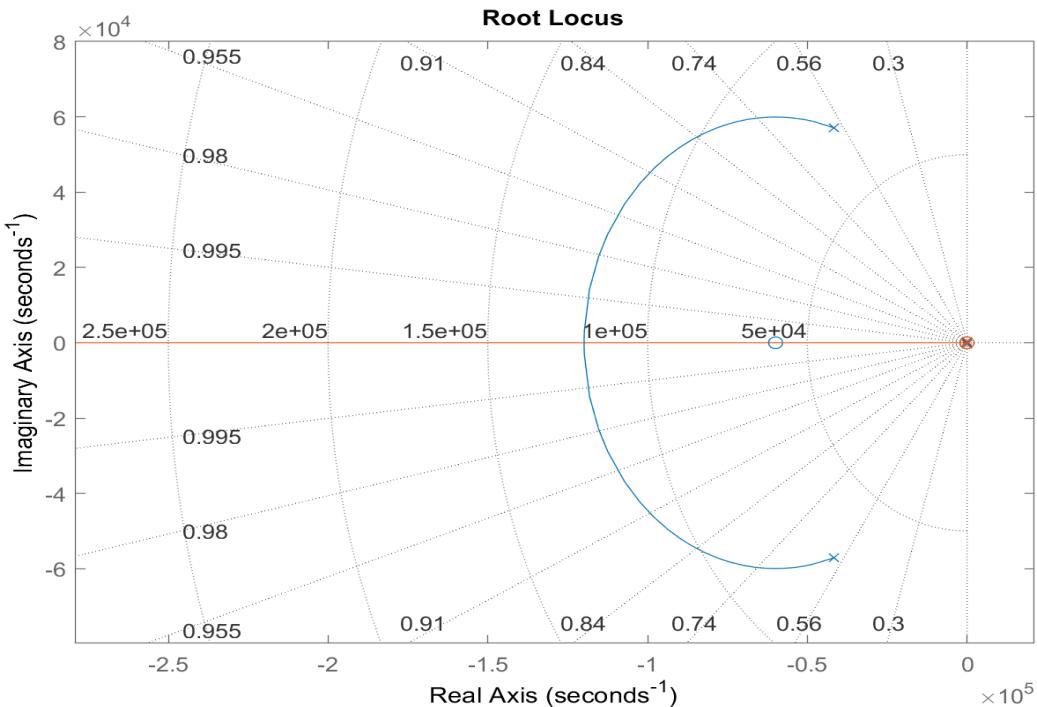


Figure 2.16. Root locus plot of the $G_{\text{clos}}(s)$ in MATLAB

Figure 2.16. shows the close loop eigenvalues are in the left half-plane showing the closed-loop system is stable.

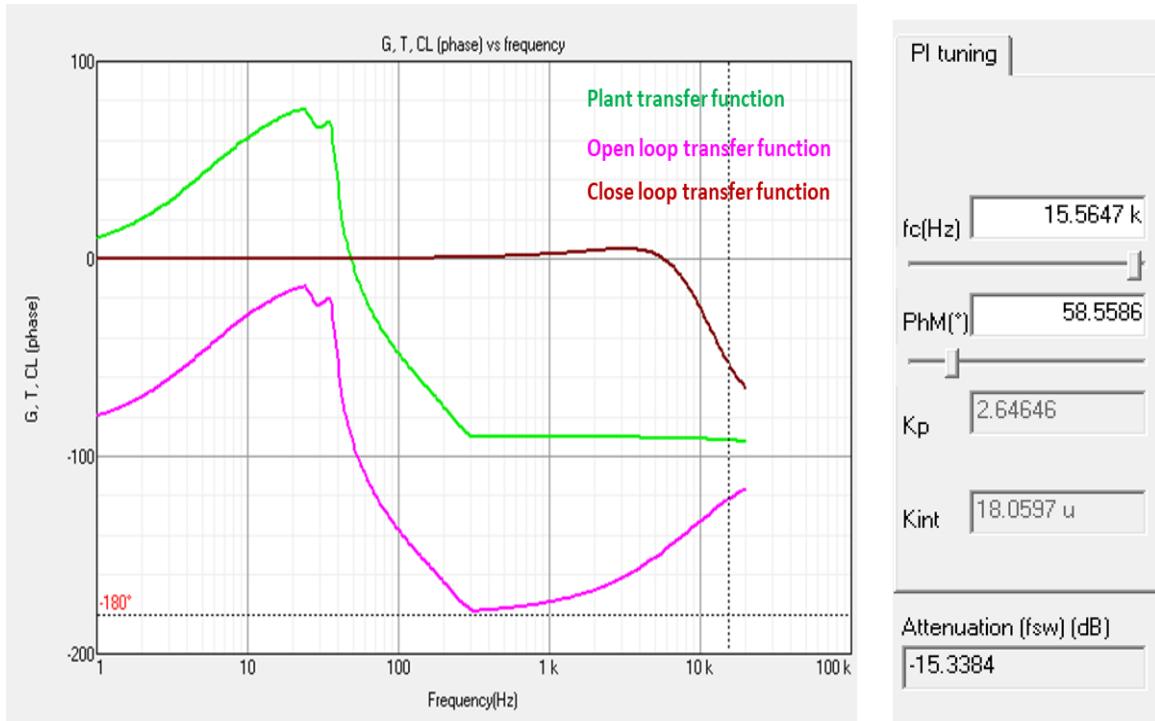


Figure 2.17. Bode plot of the G_{clos} and G_{op} with PI from Smartctrl.

A similar result was obtained when the transfer function text file of figure 2.13 was imported to Smartctrl after which the appropriate controller was selected and tuned quickly and efficiently. However, MATLAB gives the flexibility of designing a specialized controller type by allowing the manual placement of poles and zero using the SISO tool of the control designer toolbox, as seen in figure 2.18. Figure 2.18 shows that the modified PI controller cancels out the low-frequency zero with a low-frequency pole and the high-frequency pole with a high frequency zero. It also shows the location of the pole frequency whose function is to help filter out the high-frequency noise in the duty ratio of the current loop.

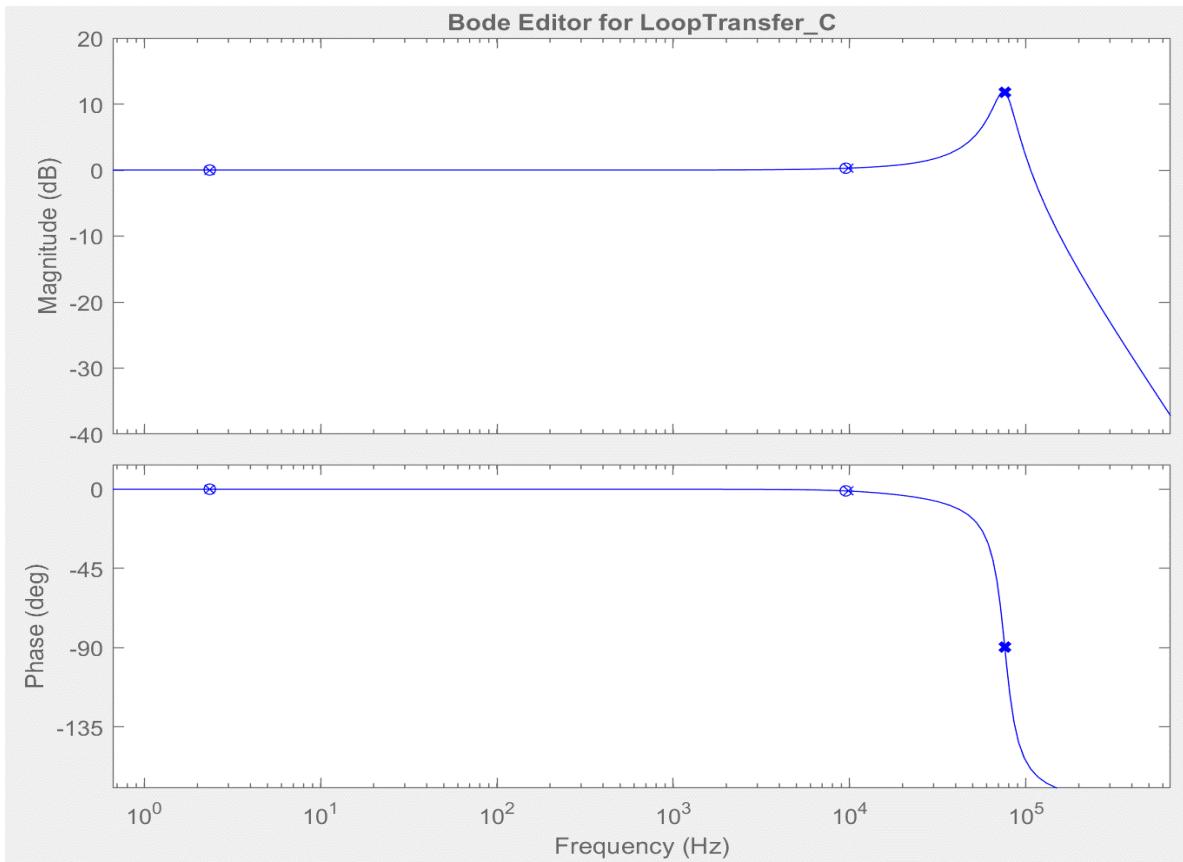


Figure 2.18. Pole/zero location of the G_{i_clos} in MATLAB SISO tool

2.2.4.2 Duty – ratio feedforward control

If a perfect input sinusoidal voltage V_{ac} with an angular frequency ω_{ac} is assumed to be entering the input of the bridgeless boost PFC. Considering only half of a period in the time interval $(0, t_{ac}/2)$ according to figure 2.19, then the input voltage can be expressed as:

$$V_{ac}(t) = \hat{V}_{ac} \sin(\omega_{ac}t) \quad (2.51)$$

The average voltage across the input switches is given by V_{avg_sw} which is needed to make the inductors current(I_{in}) have almost the same waveshape as the input voltage is expressed as:

$$V_{avg_sw} = V_{ac} - j\omega_{ac}L i_L = V_{ac}(1 - j\omega_{ac}L/R_e) \quad (2.52)$$

$R_e = V_{ac}/i_L$ is the emulated resistance at the input of the PFC converter. From experience $\omega_{ac}L/R_e \ll 1$, then V_{avg_sw} becomes

$$V_{avg_sw} = \text{sign}(\sin(\omega_{ac}t)) \hat{V}_{ac} \sin(\omega_{ac}(t - L/R_e)) \quad (2.53)$$

where $\hat{V}_{avg_sw} = \sqrt{1 + (\omega_{ac}L/R_e)^2} \approx \hat{V}_{ac}$

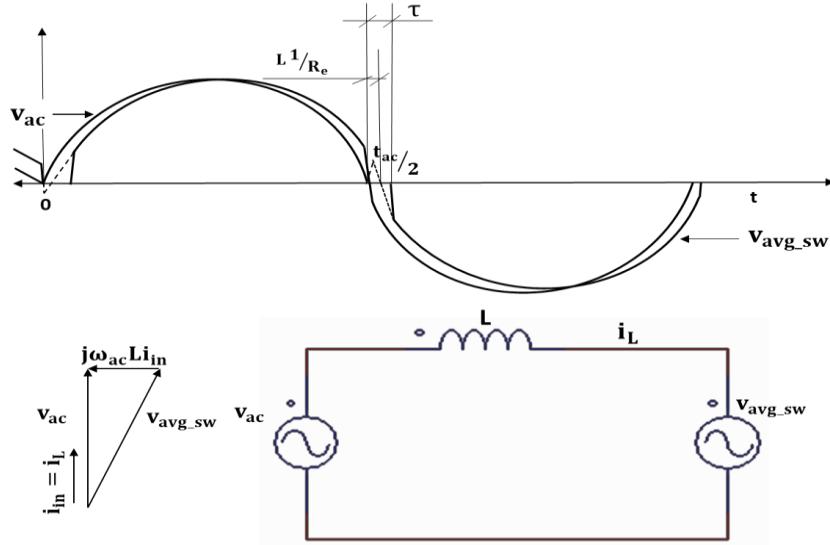


Figure 2.19. PFC waveform for feedforward derivation

From the above V_{avg_sw} is the plot with the dotted line and also shows sinusoidal delay overtime of L/R_e having a magnitude a little bit larger than the input voltage and a discontinuity at zero crossings of V_{ac} . The designed converter is working in CCM and therefore the V_{avg_sw} in terms of duty-ratio is given by (2.54) if only the PFC stage is considered

$$V_{avg_sw} = (1-d) V_{cb} \quad (2.54)$$

According to (2.53) and the shown dotted lines in figure 2.22 V_{avg_sw} has a small delay at zero crossings before turning negative. The time τ is the delay time V_{avg_sw} remains at zero before switching to negative, and this can be evaluated as shown below.

Since the total input current $i_{in} = I_L$, then $L = L_a + L_b$, and the below equation is valid at the input

$$L \frac{di_L}{dt} = V_{ac} \quad (2.55)$$

Integrating (2.54) over time τ gives

$$i_L(\tau) - i_L(0) = \frac{\hat{V}_{ac}}{\omega_{ac} L} (1 - \cos(\omega_{ac} \tau)) \quad (2.56)$$

The desired current of the inductor is V_{ac}/R_e where V_{ac} was given by (2.51), thus the point in the circuit when V_{avg_sw} remains zero before it turns negative is expressed below

$$\frac{\hat{V}_{ac}}{R_e} \sin(\omega_{ac} \tau) = \frac{\hat{V}_{ac}}{\omega_{ac} L} (1 - \cos(\omega_{ac} \tau)) \quad (2.57)$$

According to [15], the above equation is a goniometric function of which a small value of $\omega_{ac} \tau$ can be approximated using their second-order polynomial to give

$$\frac{\omega_{ac} \tau}{R_e} = \frac{1}{\omega_{ac} \tau} \left(1 - \left(1 - \frac{(\omega_{ac} \tau)^2}{2} \right) \right) \quad (2.58)$$

From above $\tau = 2L/R_e$ and this shows that V_{avg_sw} remain zero during time $2L/R_e$ and soon after the zero-crossing V_{ac} it adopts a negative value govern by (2.53). Having affirmed this previously, the goal of the duty-ratio feedforward control is to allow the current -loop controller force the inductor current to be similar as much as possible in waveform with the input voltage. This means τ , which is the delay time, must be as short as possible. This can be achieved easily with the proposed duty – ratio control which involves adding the value of both the decoupling voltage V_{cd} and output voltage V_o to the output of the current – loop controller. The advantage of this process is that the current – loop controller has to compensate for a little difference between V_{ac} and V_{avg_sw} rather than only V_{ac} , thus resulting in smaller inductor current error. The forward switch voltage is shown in (2.59)

$$V_{avg_sw_ff} = V_{ac} \quad (2.59)$$

Referring (2.53) depicting the operation of the boost converter in CCM mode, the forward duty ratio d_{ff} is

$$d_{ff} = 1 - \frac{V_{ac}}{V_{cb}} \quad (2.60)$$

The above only considers the DC bus voltage V_{cb} , therefore a duty-ratio feedforward that would consider V_{cd} and V_o was proposed below

$$d_{ff_new} = 1 - \frac{|V_{ac}|}{V_{cb}} + (V_{cd} - V_o) \quad (2.61)$$

where $|V_{ac}|$ is the absolute value of V_{ac} and together with V_{cb} , V_{cd} and V_o are scaled down to a unitary amplitude. (2.61) shows that a change in the output load is reflected on the duty cycle at the input, which in turn lowers or either increase the DC – bus voltage. Another benefit of this proposed feedforward approach is the drastic reduction in the THDi, thus better power factor. Figure 2.21 shows better control dynamics using a modified PI with feedforward control as oppose to figure 2.20.

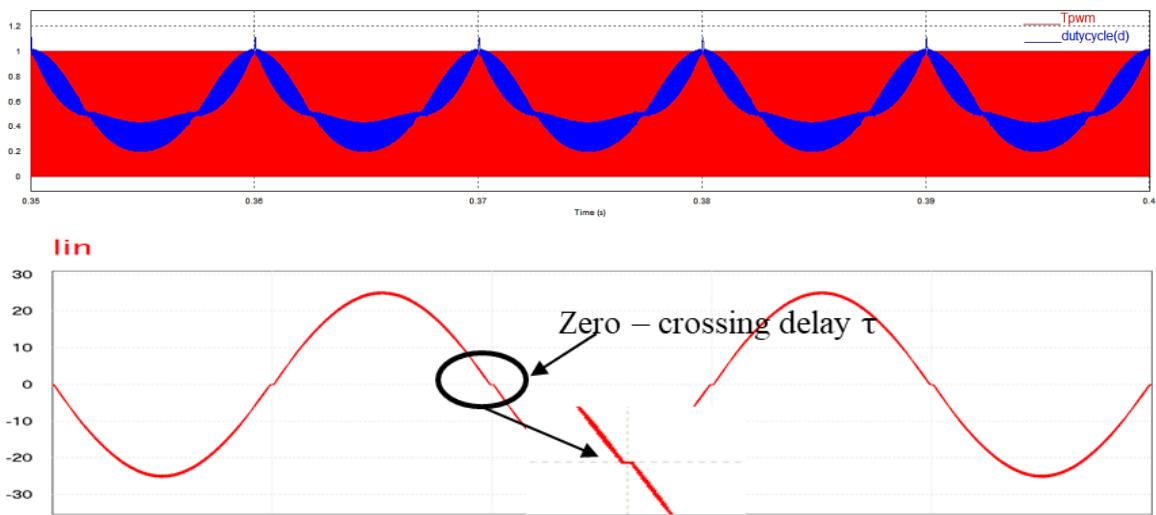


Figure 2.20. Duty cycle and input current with PI without feedforward control.

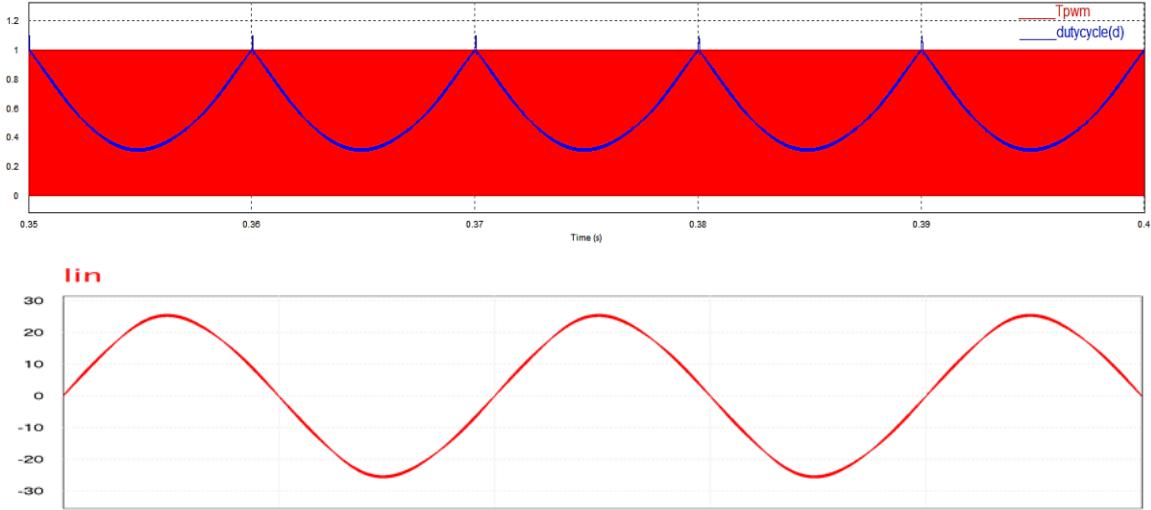


Figure 2.21. Duty cycle and input current with a modified PI with feedforward control.

2.2.4.3 PFC stage voltage control system design

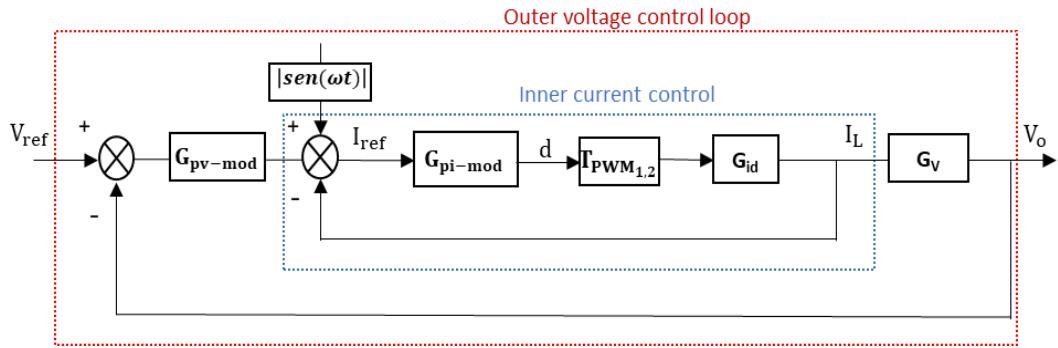


Figure 2.22. Voltage control loop

A low-frequency ripple is present at the output of the PFC stage causing undesired current amplitude variation, and therefore the voltage control must be able to attenuate such ripple. The bandwidth(f_{c_v}) of the voltage loop must be slower than that of the current loop, however, according to experience f_{c_v} must satisfy $f_{c_v} \leq 10f_{c_i}$ and $f_{c_v} \leq 100\text{Hz}$. Since the output ripple would be taking out entirely with the buck circuit topology, the voltage loop can be faster and therefore may not follow $f_{c_v} \leq 10f_{c_i}$ but must still follow $f_{c_v} \leq 100\text{Hz}$. f_{c_v} was chosen to be 62Hz and the second-order PI used in the current control case was still used here with a pole frequency f_{pv} of 100Hz. According to [16] the transfer function of a bridgeless PFC is expressed as

$$G_v(s) = \frac{V_{ac}}{V_{cb}} \frac{R_{cb}}{(R_{cb}C_b s + 1)} = \frac{73.92}{0.1355s + 1} \quad (2.62)$$

The bode plot of $G_v(s)$ plot using MATLAB and PSIM is shown in figure 2.23 and figure 2.24, respectively. The two plot shows similarity, however figure 2.24 shows more gain in amplitude than figure 2.23.

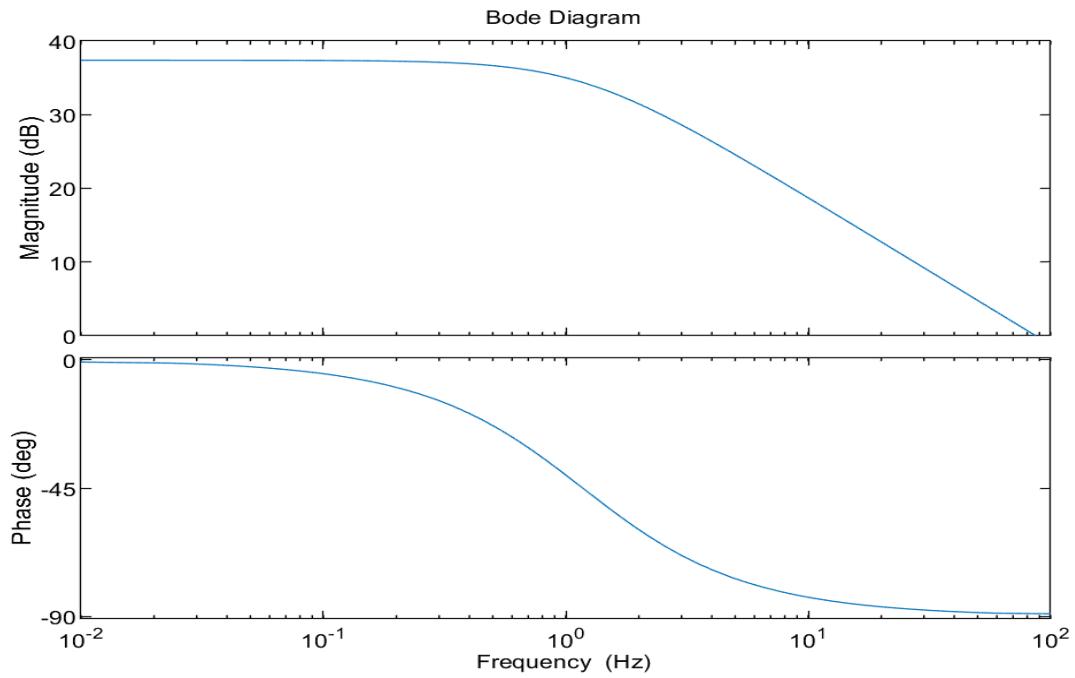


Figure 2.23. $G_v(s)$ bode plot in MATLAB

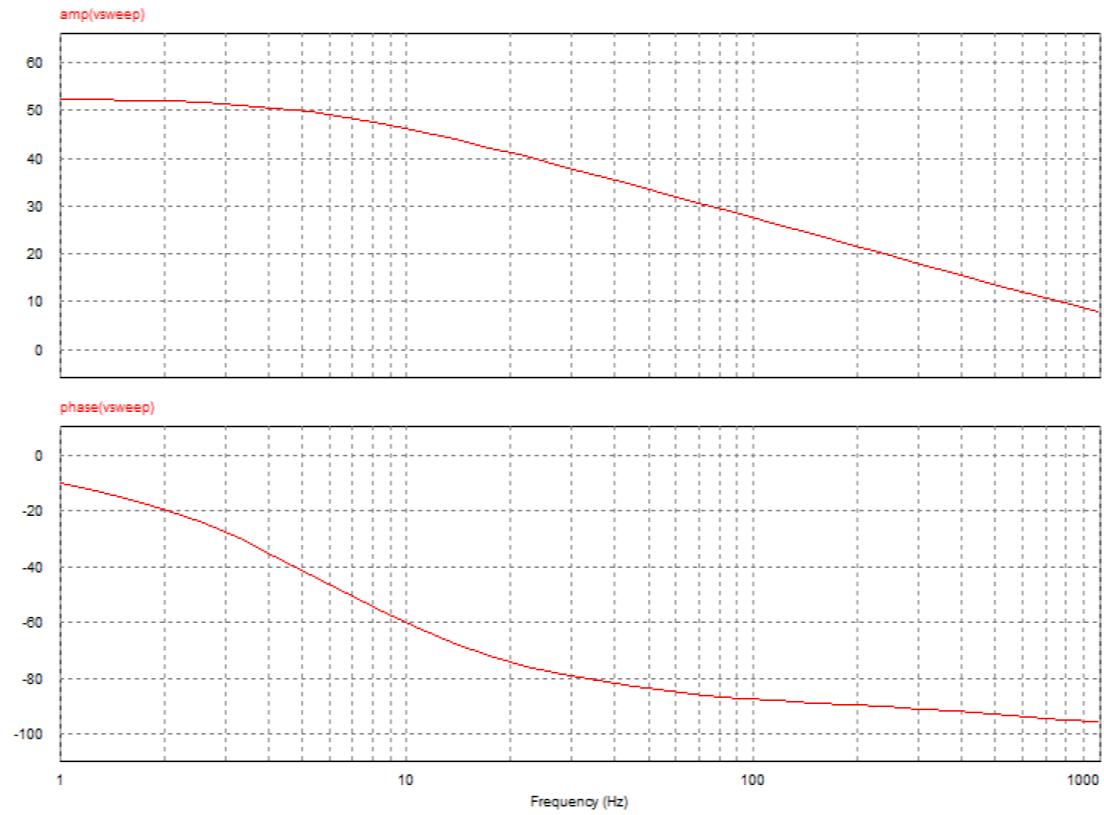


Figure 2.24. $G_v(s)$ bode plot using AC sweep in PSIM

The open-loop transfer function is given by (2.63), and the modified PI controller is also provided by (2.64).

$$G_{v_op}(s) = G_{i_closi}(s) \times G_v(s) \quad (2.63)$$

$$G_{pv-mod}(s) = \frac{K_{pv}(1+T_v s)}{T_v s} \times \frac{1}{1+T_{pv}s} \quad (2.64)$$

$G_{pv-mod}(s)$ was tuned in SmartCtrl to give $K_{pv} = 11.91$, $T_v = 26.92m$, $T_{pv} = 1.59m$ or $f_p = 100Hz$.

$$G_{v_clos}(s) = \frac{G_{i_closi}(s) G_v(s) G_{pv-mod}(s)}{1 + G_{i_closi}(s) G_v(s) G_{pv-mod}(s)} \quad (2.65)$$

Figure 2.25 and 2.26 shows the open-loop response rejecting the 100Hz ripple. PI was selected in smart control to tune the voltage loop due to the absence of a second-order PI. The pole frequency was then added to the chosen second-order PI selected in PSIM. The little difference in the result of each figure is due to the high gain result the voltage transfer function has when an AC sweep simulation was carried out in PSIM

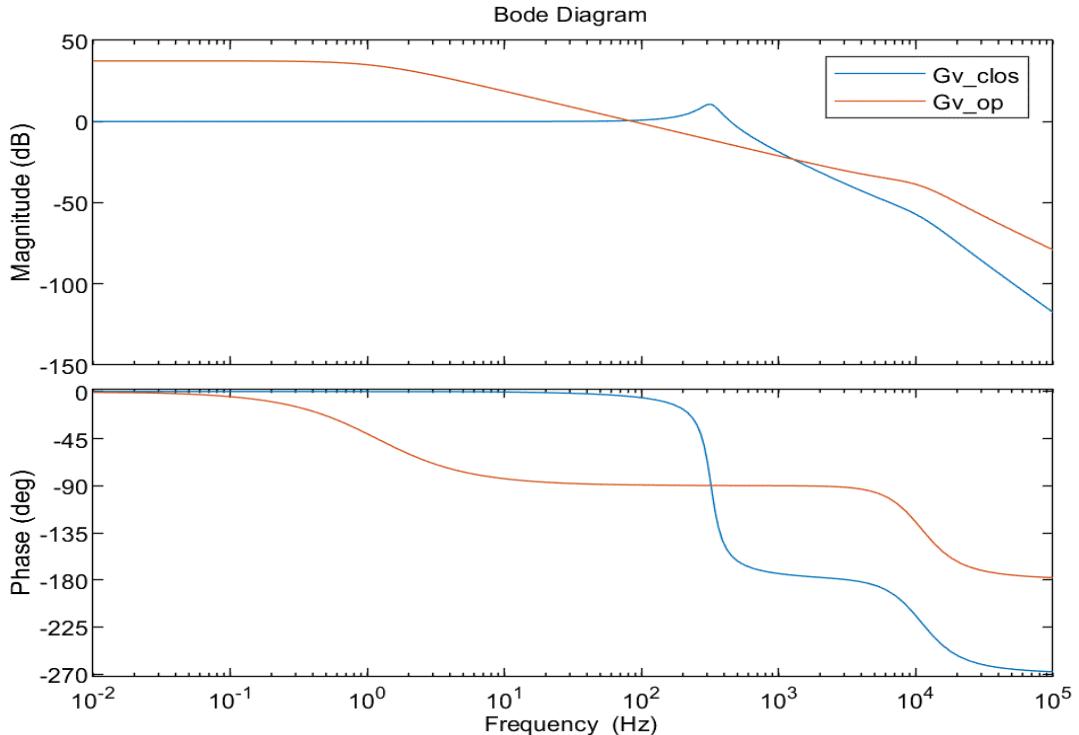


Figure 2.25 close loop and open-loop response with modified PI in MATLAB

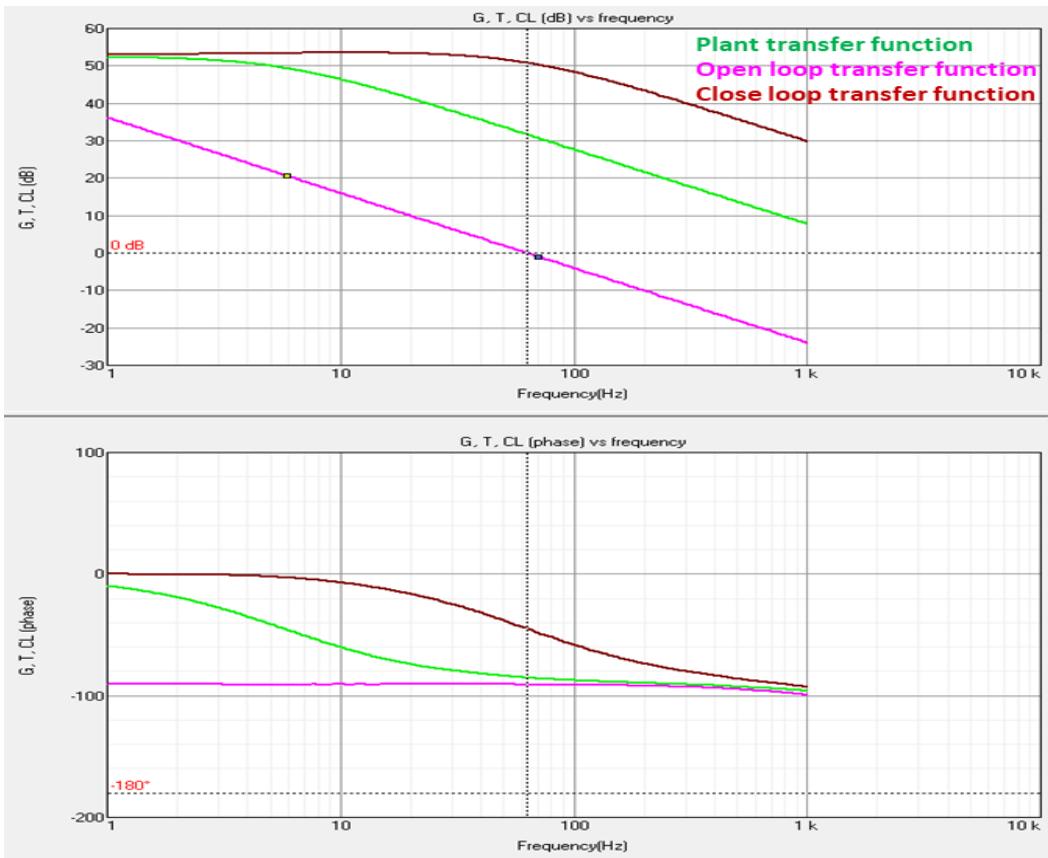


Figure 2.26 close and open-loop response using a PI controller in SmartCtrl

2.2.4.4 Ripple cancellation stage current and voltage control design

This stage consists of two cascaded loops due to the requirement of the research work. The goal with this stage is to cancel out the 100Hz output ripple. Using a two-loop control when compared to one gives a robust and precise control dynamics. Two loop control gives the benefit of quicker recovery when there is a sudden load change, and faster settling time when compared with single loop control. Type 3 controller was used for the current loop due to the desirable attribute of splitting the complex conjugate pole of the filter into two real poles. It also protects the ripple cancellation stage circuit by cycle to cycle current limit, thus offering overload protection. Although the benefit of current control come a drawback of subharmonic oscillation. This occurs when the inductor ripple current is not returning to its initial value in the next switching cycle when the duty ratio greater than 0.5. [17]

This behaviour affirms the need for a voltage loop which helps cancels out the subharmonic oscillation. To this end, a simple PI controller was used for the outer loop to generate a current reference ramp that is compared with the feedback current of the current loop. These two controllers for this stage was designed using the analogue circuit in other to facilitate familiarization of design in the analogue domain.

2.2.4.4.1 Current control system design

The switching frequency of the input side switches is the same as that of the ripple cancellation stage. The small-signal diagram of the current loop is shown in figure 2.27.

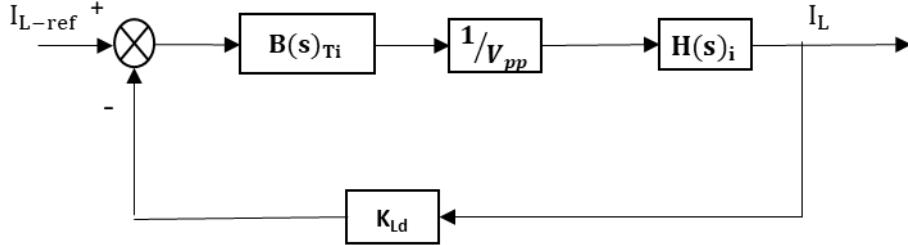


Figure 2.27. Current control loop – ripple cancellation stage

The inductor to duty ratio transfer function of a buck converter is given by $H(s)_i$ which is expressed in (2.66). $H(s)_i$ shows that the transfer function varies with frequency. Thus the transfer function can be combined with the PWM generator as seen in (2.67). $H(s)_p$ is the transfer function of the power stage.

$$H(s)_i = \frac{\widehat{I_{Ld}}}{\widehat{d}} = \frac{V_{cd}}{R_o} \frac{1+sC_oR_o}{(1+\frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2})} = \frac{V_{cd}(1+sC_oR_o)}{s^2L_dC_oR_o + sL_d + R_o} \quad (2.66)$$

where $\omega_o = \frac{1}{\sqrt{L_oC_o}}$ and $Q = \frac{R_o}{\sqrt{L_o/C_o}}$

$$H(s)_p = \frac{1}{V_{pp}} \left(\frac{V_{cd}(1+sC_oR_o)}{s^2L_dC_oR_o + sL_d + R_o} \right) \quad (2.67)$$

The above transfer function is a second-order system having a double pole at the resonance frequency (LC filter) and most usually a zero because of the ESR of the output capacitor. The ESR was not added to the (2.66) due to simplicity but was considered with the design in SmartCtrl. The open-loop gain is therefore given by (2.68)

$$H(s)_{op} = \frac{1}{K_{Ld}} \times H(s)_p \quad (2.68)$$

$\frac{1}{K_{Ld}}$ is the attenuation factor of the output inductor current.

The ripple cancellation circuit must react very fast to be able to quickly cancel out the output ripple and achieve a quick, steady-state. To this end, the crossover frequency (f_{ci}) was selected to be $\frac{1}{7}f_{sw}$ giving a f_{ci} of 20KHz. Type 3 controller was designed to follow a type-3A controller procedure. The criteria for the choice of such design procedure followed (2.69) and was guided by the frequency of the double poles and frequency of the zero given by (2.70) and (2.71) respectively.

$$f_{LC} < f_{ci} < f_{ESR} < f_{sw}/2 \quad (2.69)$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L_dC_o}} = 321\text{Hz} \quad (2.70)$$

$$f_{\text{ESR}} = \frac{1}{2\pi ESR_{\max} C_o} = 22.74 \text{ KHz} \quad (2.71)$$

According to [18] the transfer function in the analogue domain of a type-3 controller is given by

$$B(s)_{Ti} = \frac{(1+sC_2R_2)[(sC_3(R_1+R_3)+1]}{R_1(C_1+C_2)s(sC_{12}R_2+1)(sC_3R_5+1)} \quad (2.72)$$

where $C_{12} = \frac{C_1 C_2}{C_1 + C_2}$

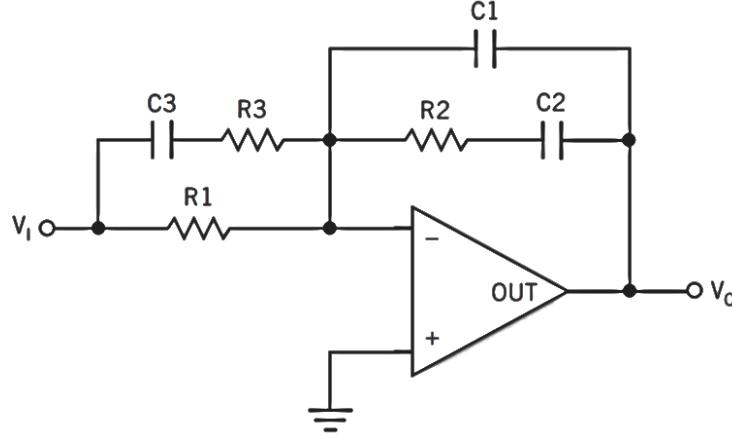


Figure 2.28. A type-3 compensator/controller

The next step is to determine the location of the poles and zeros. For simplicity, a valid assumption is that $C_2 \gg C_1$ and thus, the location of the poles and zeros are expressed in[19] as shown below.

$$f_{po} = \frac{1}{2\pi R_1(C_1+C_2)} \approx \frac{1}{2\pi R_1 C_2} \quad (2.73)$$

$$f_{p1} = \frac{1}{2\pi R_3 C_3} \quad (2.74)$$

$$f_{p2} = \frac{1}{2\pi R_2 C_{12}} \approx \frac{1}{2\pi R_2 C_2} \quad (2.75)$$

$$f_{z1} = \frac{1}{2\pi(R_1+R_3)C_3} \quad (2.76)$$

$$f_{z2} = \frac{1}{2\pi R_2 C_2} \quad (2.77)$$

C_1 , C_2 , C_3 , R_2 and R_3 can be calculated according to the equations below once R_1 is assumed the desired f_{po} , f_{p1} , f_{p2} , f_{z1} and f_{z2} .

$$C_1 = \frac{f_{p2}-f_{z2}}{2\pi R_1 f_{po} f_{p2}} \quad (2.78)$$

$$C_2 = \frac{f_{p1}-f_{z1}}{2\pi R_1 f_{p1} f_{z1}} \quad (2.79)$$

$$C_3 = \frac{f_{z2}}{2\pi R_1 f_{po} f_{p2}} \quad (2.80)$$

$$R_2 = \frac{R_1 f_{po} f_{p2}}{f_{z2}(f_{p2}-f_{z2})} \quad (2.81)$$

$$R_3 = \frac{R_1 f_{z1}}{f_{p1} - f_{z1}} \quad (2.82)$$

Owing to the condition set by (2.69), the calculation process could be simplified further by assuming C_3 to have a starting value from 1nF and after which the poles and zeros as follows.

$$f_{LC} = f_{z1} \quad (2.83)$$

$$f_{z2} = 0.75f_{z1} \quad (2.84)$$

$$f_{p1} = f_{ESR} \quad (2.85)$$

$$f_{p2} = f_{sw}/2 \quad (2.86)$$

$$R_1 = \frac{1}{2\pi C_3 f_{p1}} \quad (2.87)$$

$$R_2 = \frac{2\pi f_{ci} L_d C_o V_{pp}}{V_{cd} C_3} \quad (2.88)$$

$$R_3 = \frac{1}{2\pi C_3 f_{z1}} - R_1 \quad (2.89)$$

$$C_1 = \frac{1}{2\pi R_2 f_{p2}} \quad (2.90)$$

$$C_2 = \frac{1}{2\pi R_2 f_{z2}} \quad (2.91)$$

2.2.4.4.2 Voltage control system design

The function of the voltage controller, in this case, is to provide a reference for the current controller and therefore the needs for a simple controller and in this case, a PI controller designed in the analogue domain was used. The crossover frequency is chosen to be 1KHz, and the small-signal model diagram is shown in figure 2.29.

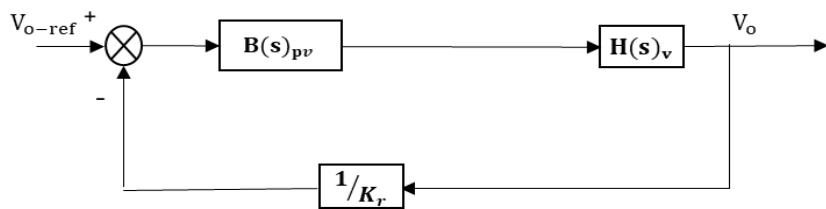


Figure 2.29. Voltage control loop – ripple cancellation stage

The inductor current has already been taken as the control input to the converter and therefore the transfer function $H(s)_v$ between the output voltage and the inductor current is given by (2.92). $H(s)_v$ shows the presence of a pole which would be compensated for with the help of a PI controller.

$$H(s)_v = \frac{R_o}{R_o C_o s + 1} \quad (2.92)$$

The transfer function of the PI controller in analog domain is given by (2.93)

$$B(s)_{pv} = \frac{R_{p2}C_{p1}s + 1}{R_{p1}C_{p1}s} \quad (2.93)$$

The open loop and closed loop gain are expressed by (2.94) and (2.95) respectively where $\frac{1}{K_r}$ is the gain of the resistor divider (R_a, R_b) as shown in figure 2.30.

$$H(s)_{opv} = \frac{1}{K_r} \times H(s)_v \quad (2.94)$$

$$H(s)_{cv} = \frac{V_o}{V_{o-ref}} = \frac{H(s)_v B(s)_{pv}}{1 + H(s)_v B(s)_{pv}} \quad (2.95)$$

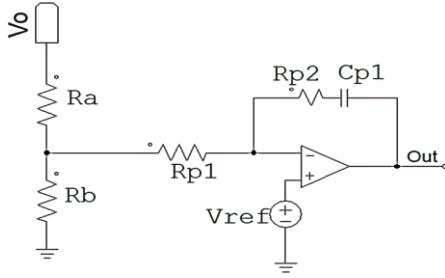


Figure 2.30. Analogue implementation circuit for a PI controller.

The voltage controller has a pole at the origin, and therefore the zero of the controllers should be placed at a frequency lower than f_{LC} as calculated previously. The zero of the controller is placed using equation (2.96) and followed by the calculation procedure for R_{p2} by assuming C_{p1} to be any value from 1-10nF and R_{p1} to be 10KΩ.

$$f_z = 0.75f_{LC} \quad (2.96)$$

$$f_z = \frac{1}{2\pi R_{p2} C_{p1}} \quad (2.97)$$

The output voltage V_o can be scaled using (2.98) and assuming $R_a = 10K\Omega$

$$R_b = \frac{R_a V_{ref}}{V_o - V_{ref}} \quad (2.98)$$

The design of the voltage and the current loop was done in SmartCtrl and figure 2.31 and 2.32 show the magnitude and phase response of the plant, open and close loop of the converter, respectively. The converter design, control system and gate driver are also shown in figure 2.33, 2.34 and 2.35, respectively.

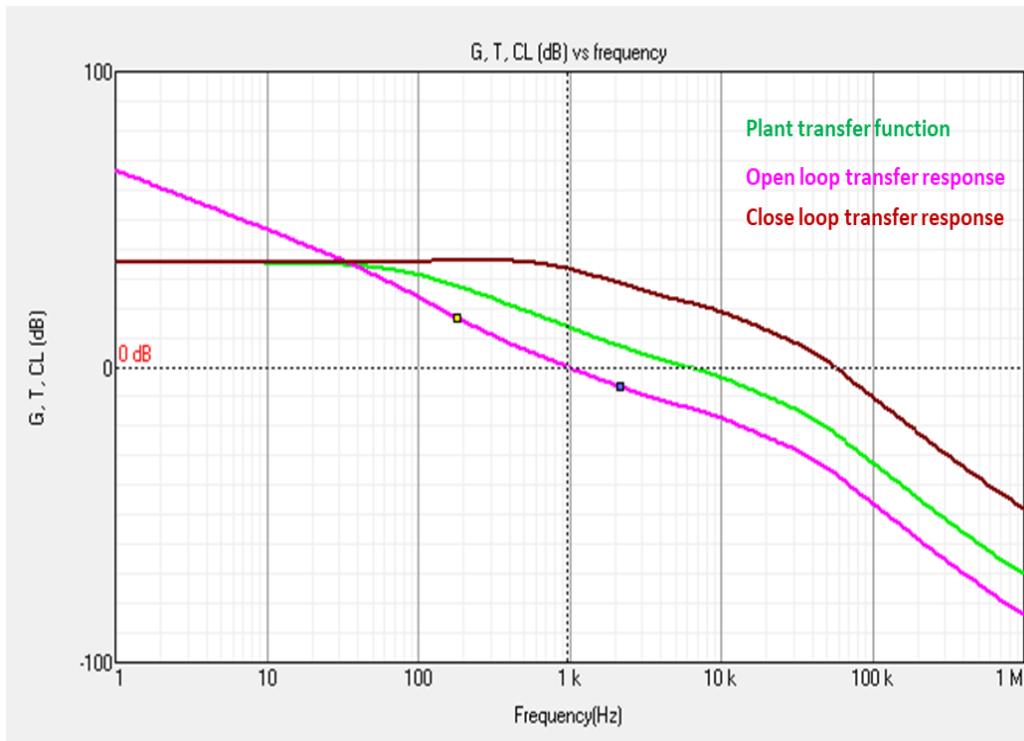


Figure 2.31. Magnitude plot of the plant, open and closed-loop response.

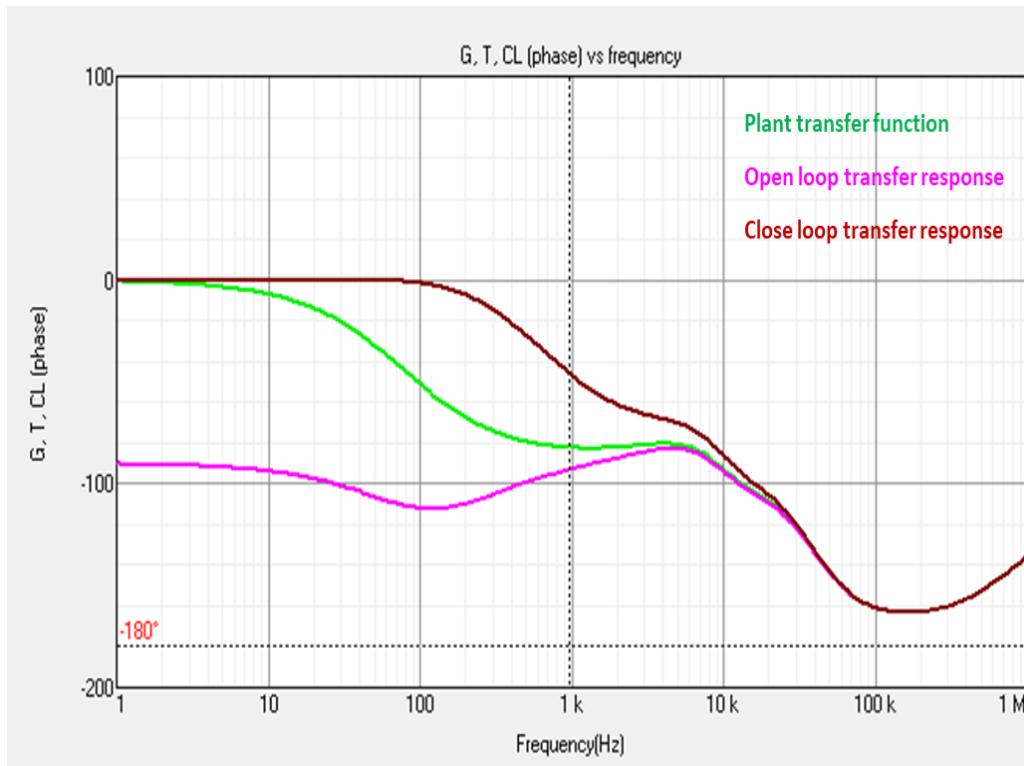


Figure 2.32. Phase plot of the plant, open and closed-loop response.

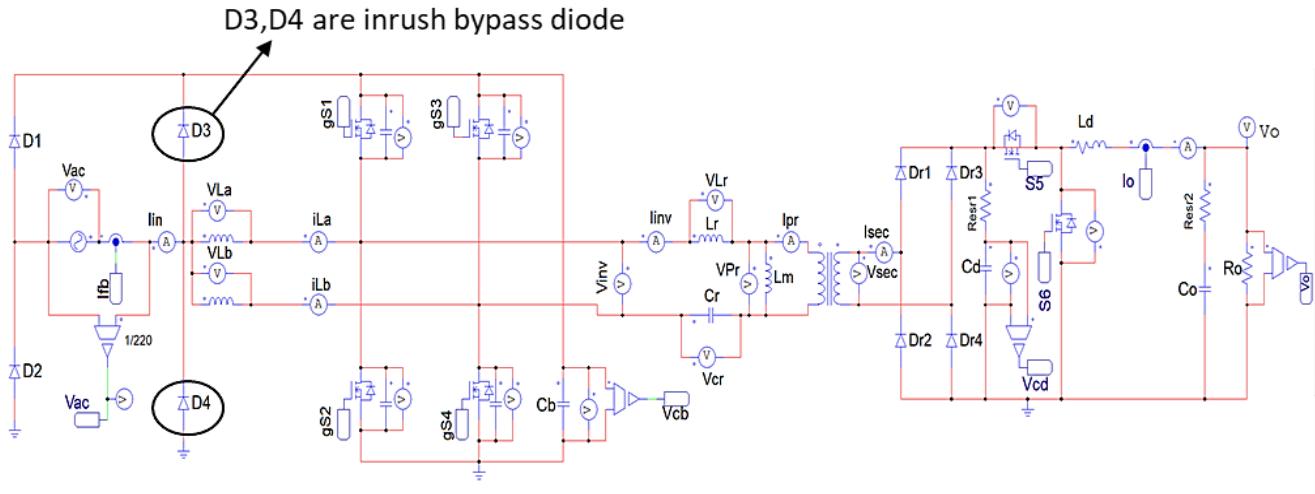


Figure 2.33. Converter design in PSIM

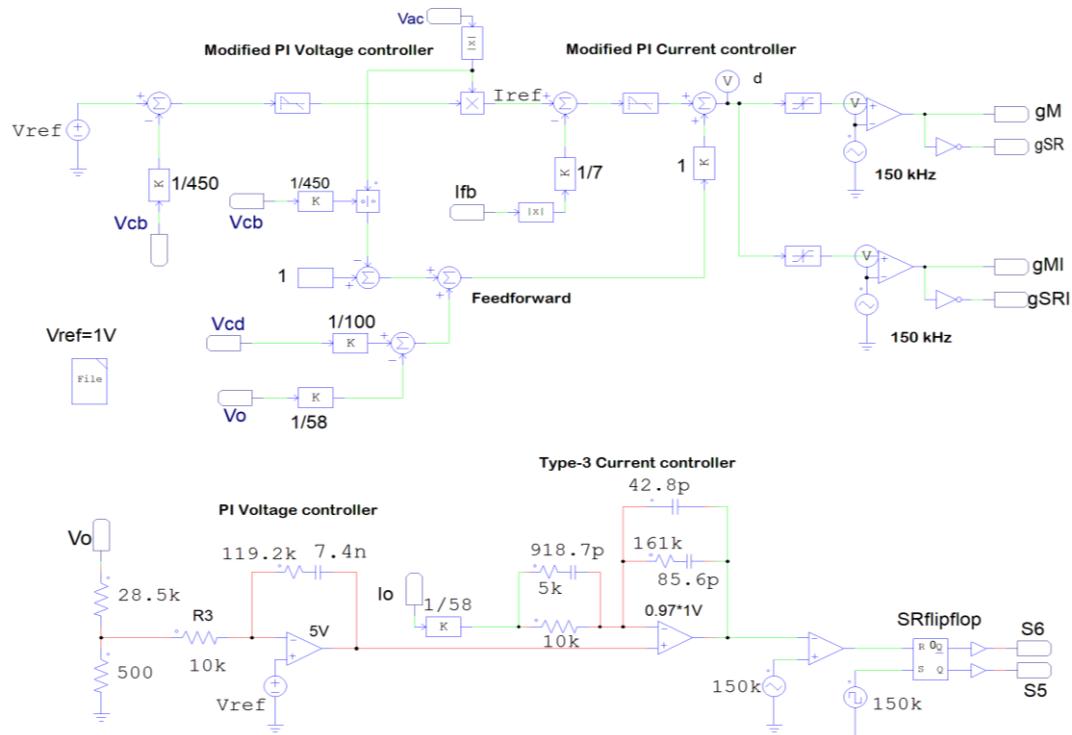


Figure 2.34. Implemented control system in PSIM

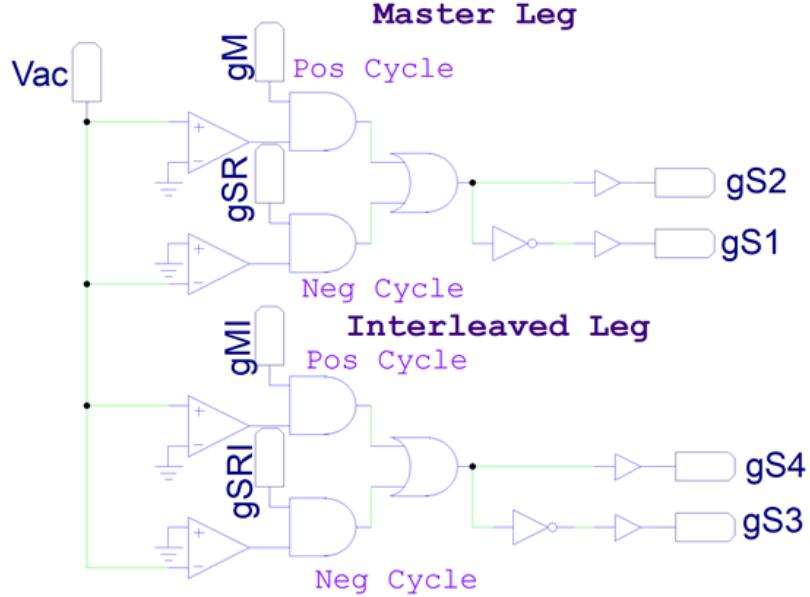


Figure 2.35. Implemented Gate driver system in PSIM

2.2.5. Simulation results

The simulated result in figure 2.36 shows the input current i_{in} following the input voltage V_{ac} at full load giving a PF of 99.96% and THDi of 2.6%. The current flowing through the inductor L_a and L_b shows interleaving and follow the inductor voltages V_{L_a} and V_{L_b} . The input ripple current has significantly reduced since the two input inductor currents are 180 degrees out of phase, allowing them to cancel out each other. This behaviour reduces the input EMI noise, making the need for EMI filter optional. The DC – bus voltage V_{cb} maintain a value between 442V to 455V giving a peak to peak ripple of 13V during the decoupling capacitor voltage V_{cd} varies from 110V to 133V. V_{cb} and V_{cd} voltages are influenced by the peak resonant inductor current.

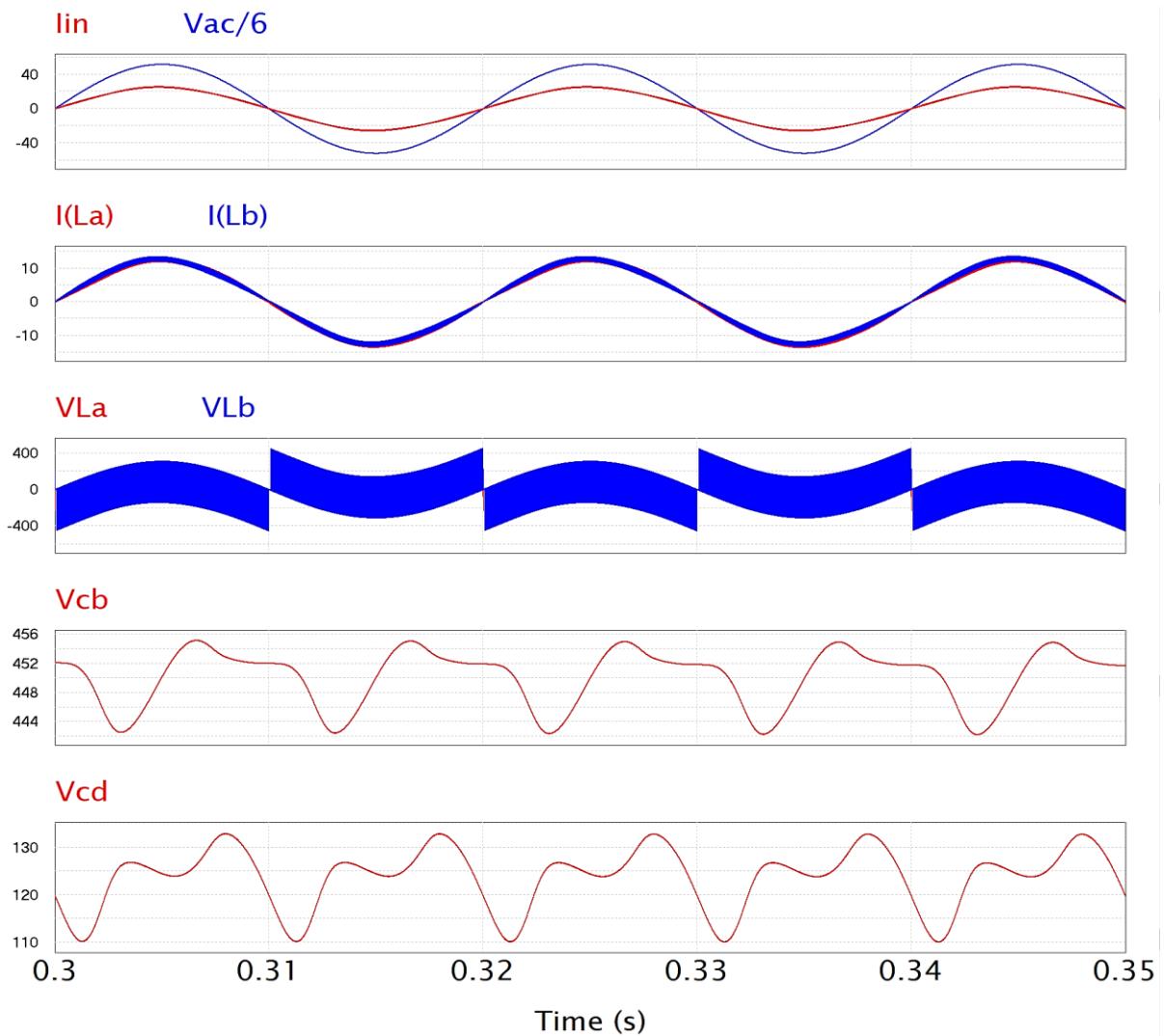
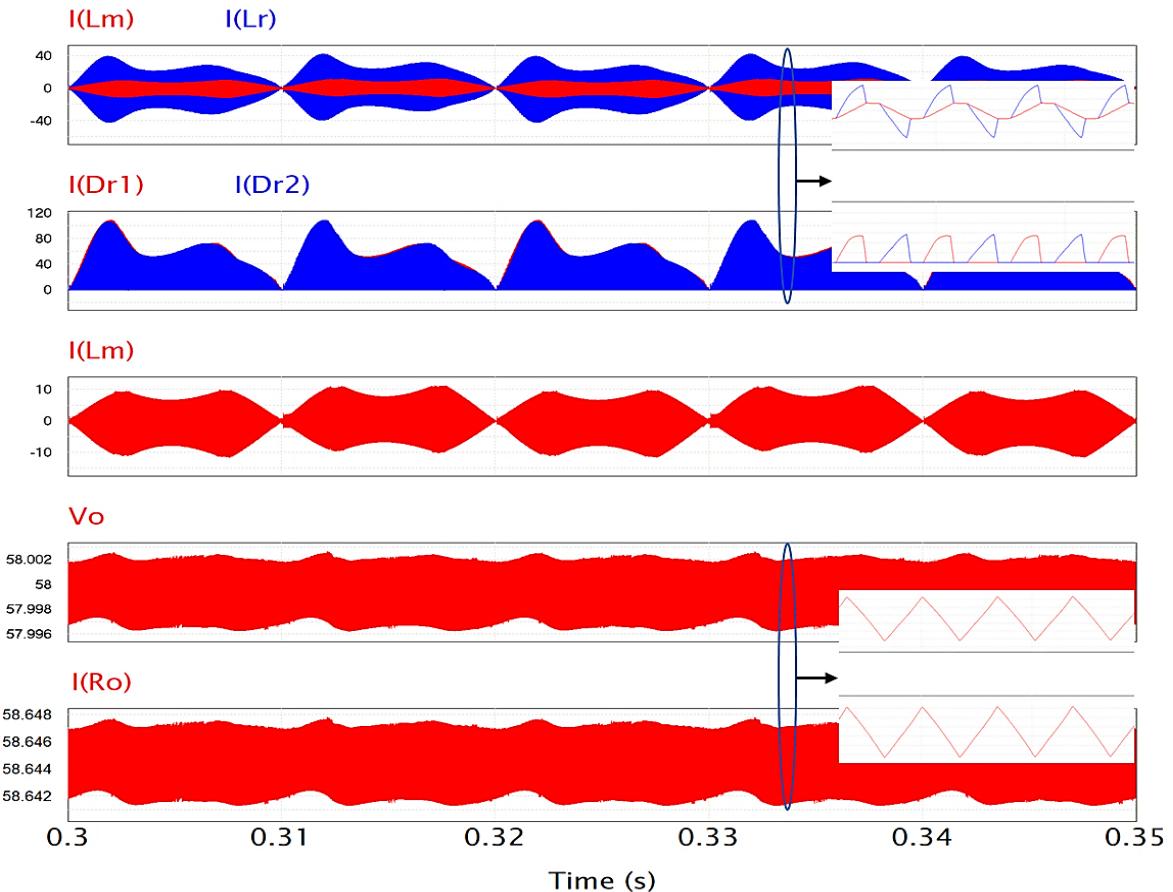
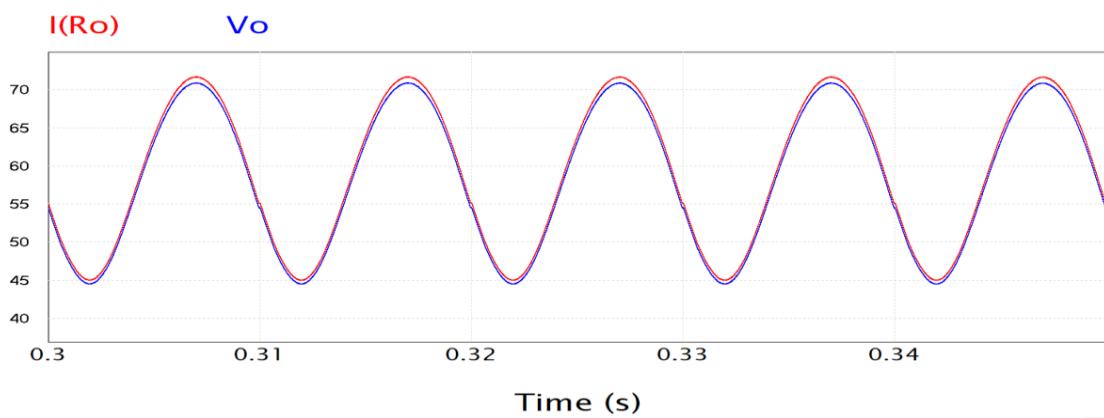


Figure 2.36 Input stage voltages and current with voltage V_{cd} at 220VRMS.

Figure 2.37a present the resonant inductor current i_{Lr} and magnetizing inductor current i_{Lm} . i_{Lm} is 10A, which is low enough to provide a low circulating magnetizing current that helps improve the circuit efficiency. The point of resonance between i_{Lr} and i_{Lm} allows ZCS to be achieved in the output diode bridge as seen in Dr1 and Dr2, The output voltage V_o and current i_{Ro} of the converter exhibit a peak to peak ripple of 6.7mV and 6.7mA respectively, which is way below the peak to peak ripple of 200mV/200mA required by the research work. Figure 2.37b showed the simulation when no ripple cancellation circuit was added despite using a capacitance of 5mF, which is the total capacitance of the output stage. A peak to peak ripple of 26V/26A was present, thus without the ripple cancellation circuit, an output capacitance of 150mF would be needed to meet the demand of the research.

Figure 2.37a Waveform result of i_{Lr} , i_{Lm} , V_o and i_{Ro} Figure 2.37b Waveform of V_o and i_{Ro} without ripple cancellation at $C_o = 5\text{mF}$

The ZVS of the input switches and ZCS of the output diode bridge are shown in figure 2.38 and 2.39. ZVS provides zero power lossless switching transition, which offers high efficiency at the chosen switching frequency. ZCS at the secondary side is short enough to prevent the output diodes from going into discontinuous conduction mode. V_{Pr} and V_{sec} are the transformer primary and secondary voltages, respectively. V_{Pr} and V_{sec} has a maximum voltage value of 380V and 127V, which is not on the high side, thus less transformer design requirement. V_{Pr} benefit from the very well regulated and reduced DC – bus voltage V_{cb} .

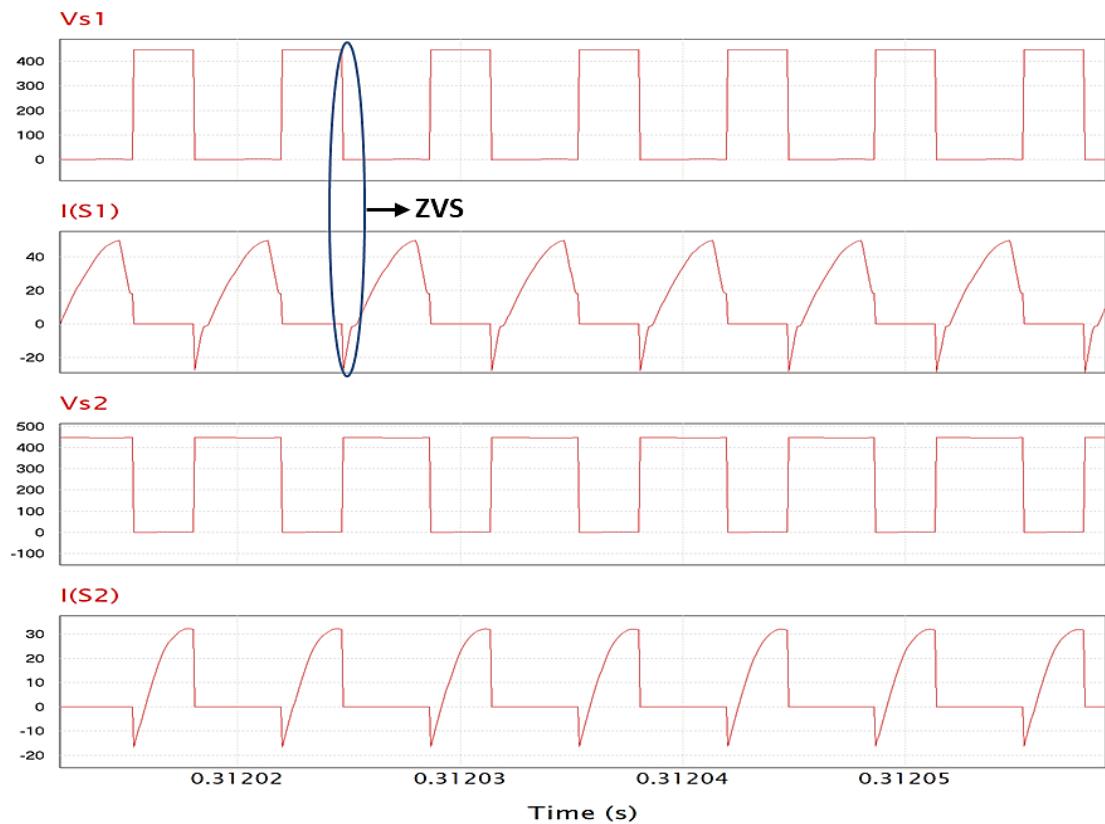


Figure 2.38 Simulated waveform result showing ZVS in switch S1 and S2

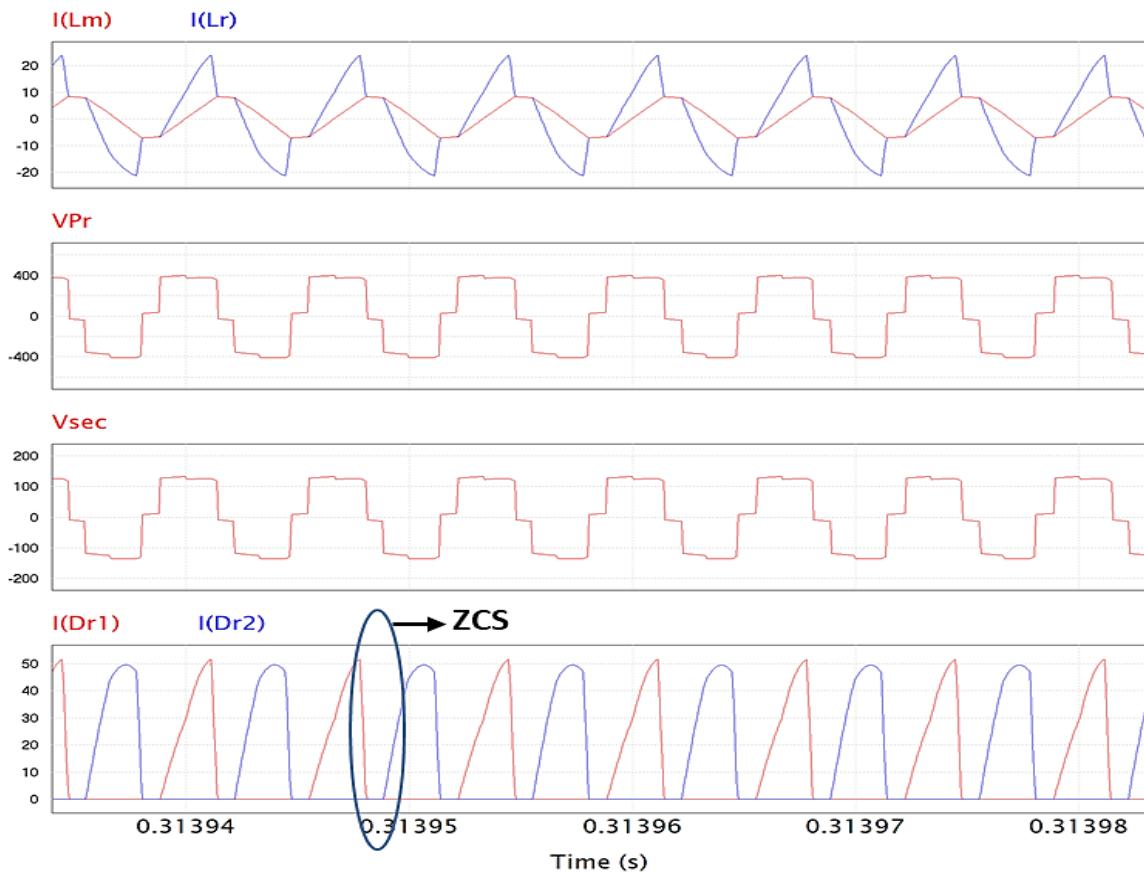


Figure 2.39 Transformer voltages (V_{Pr}, V_{sec}) and output diode exhibiting ZCS

2.2.5.1 Startup and dynamic regulation (load change behaviour)

The inrush current issue common with totem – pole PFC converter has been eliminated with the use of diode D3 and D4. The output voltage and current exhibit a short duration of overshoot before steady-state, and this are due to the little startup delay of the ripple cancellation circuit (buck converter stage).

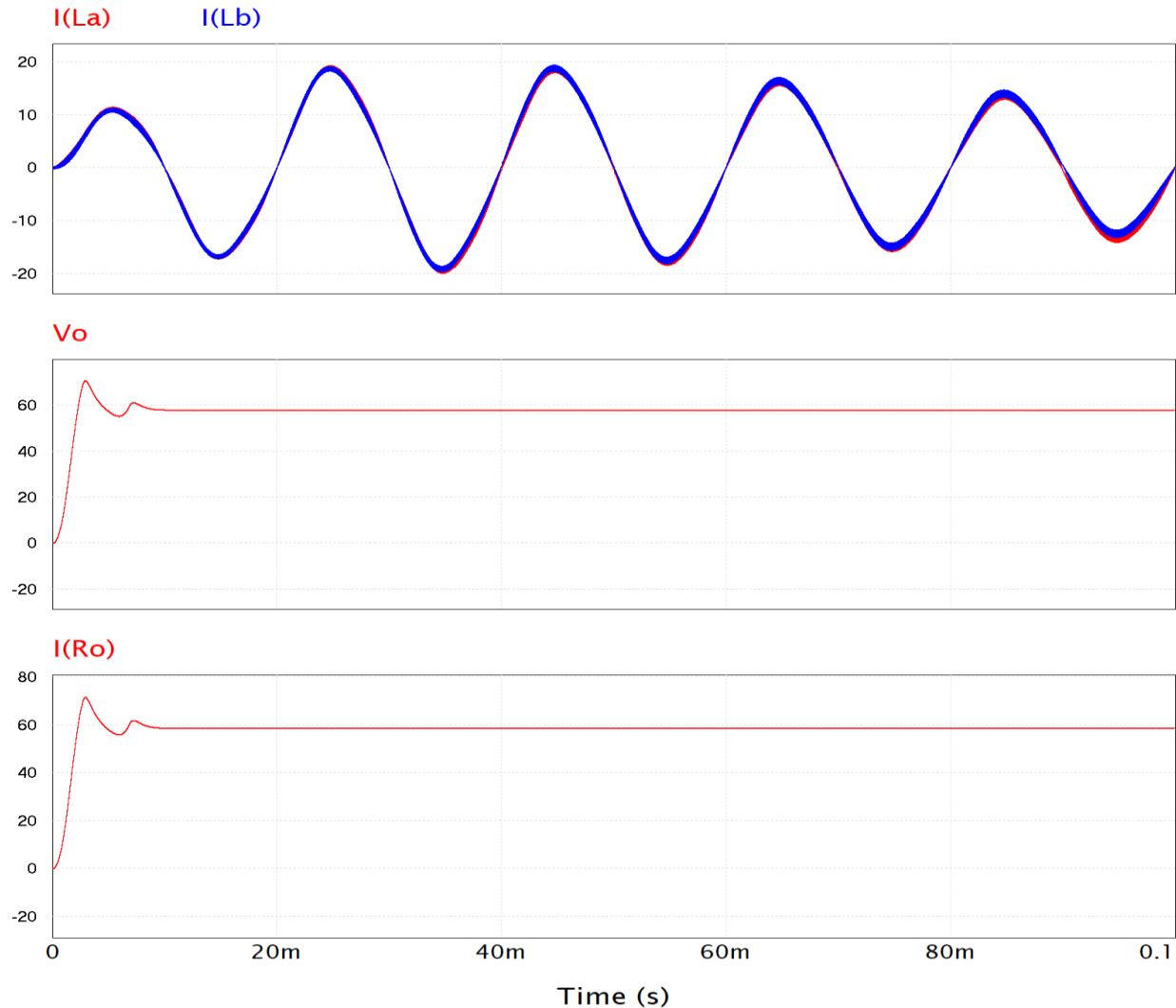


Figure 2.40. Converter startup behaviour impact on inductor current and load

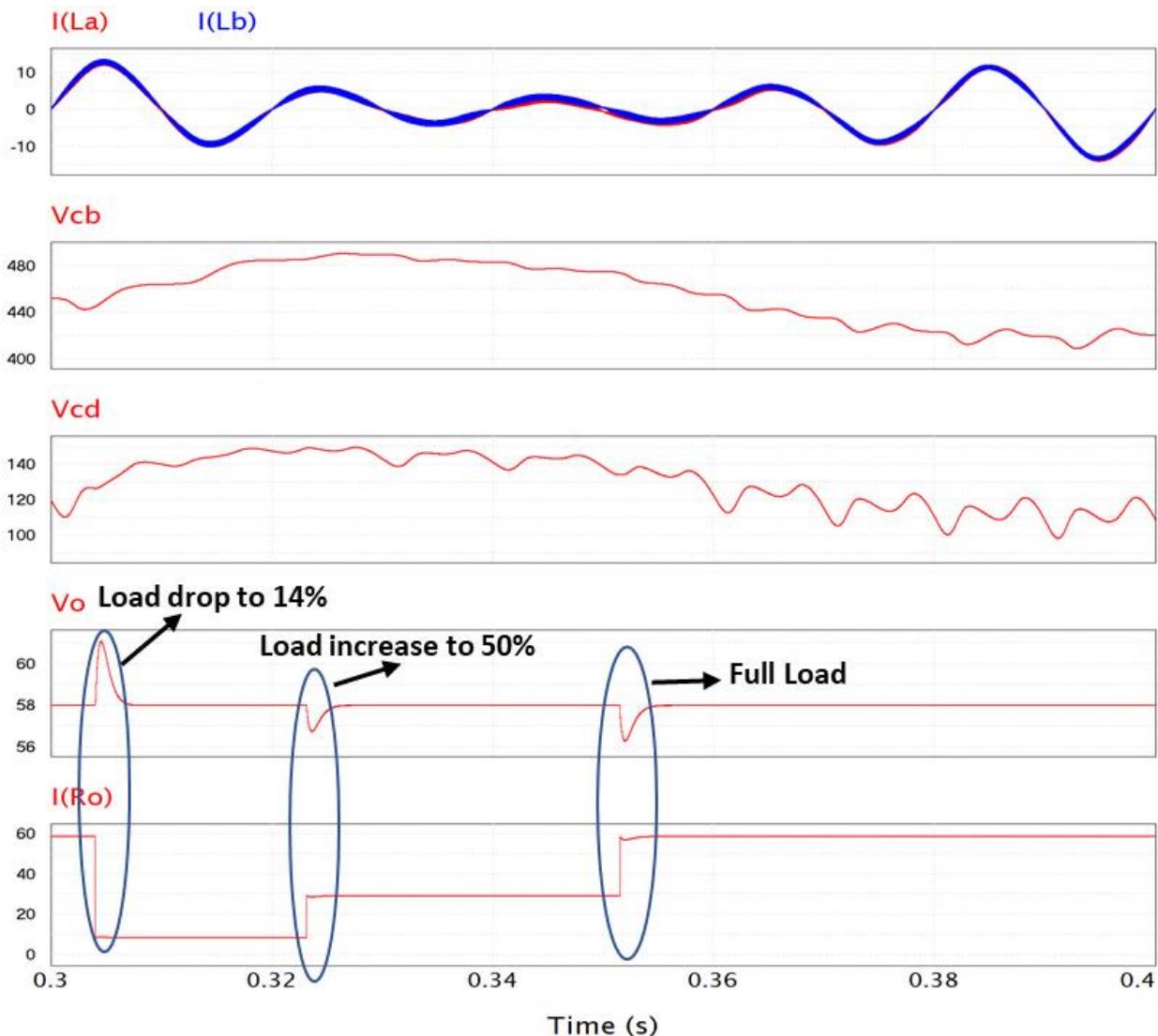


Figure 2.41. Dynamic regulation of inductor current, V_{cb} and V_{cd} due to load change

Figure 2.41 shows a sudden drop in the load to 14% causes a sudden rise in the output voltage and a slow but progressive rise of V_{cb} and V_{cd} . The control system quickly tracks back to the nominal output voltage of 58V within 3ms. The controller reacts extremely fast to a sudden increase in the load with very low impact on the output voltage while maintaining the PFC ability of the converter. This demonstrates the control system is very dynamic and robust when the converter is subjected to sudden load change. At full load, a THDi of 2.60% and a PF of 99.96% was obtained in the research work, and more details are shown in figure 2.42 and 2.43. This makes the converter satisfies the research work and European Standard IEC/EN 61000-3-2, 61000-3-4 requirement. The efficiency was also estimated to be 95.1%, and details about the estimation process are found in appendix B.

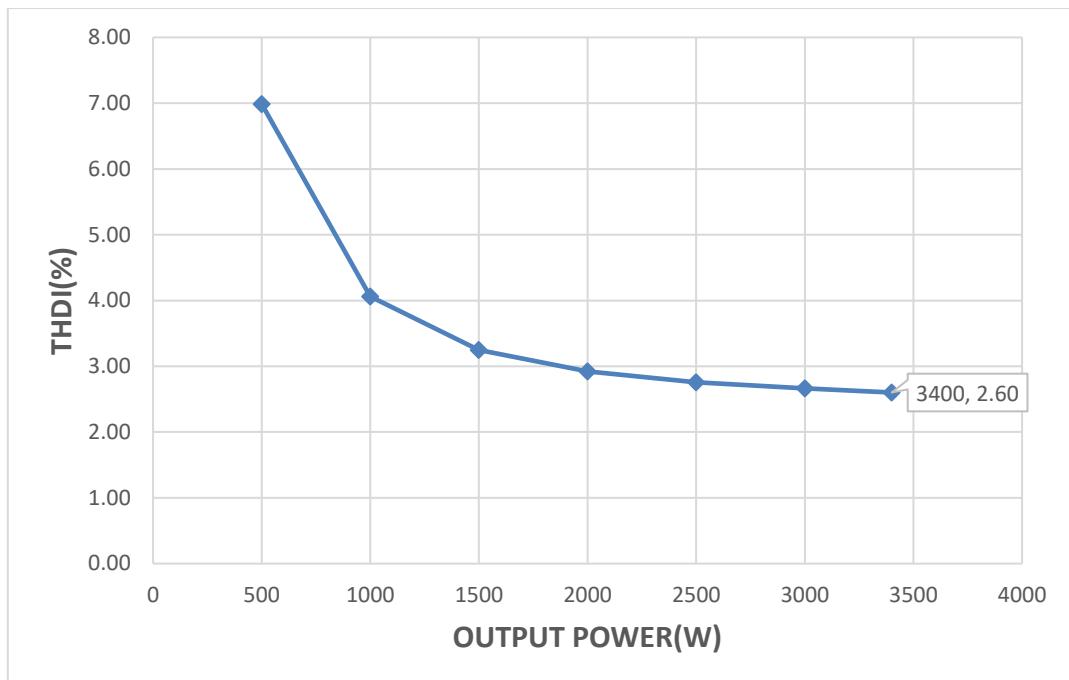


Figure 2.42. Load change behaviour on THDi at 220VRMS

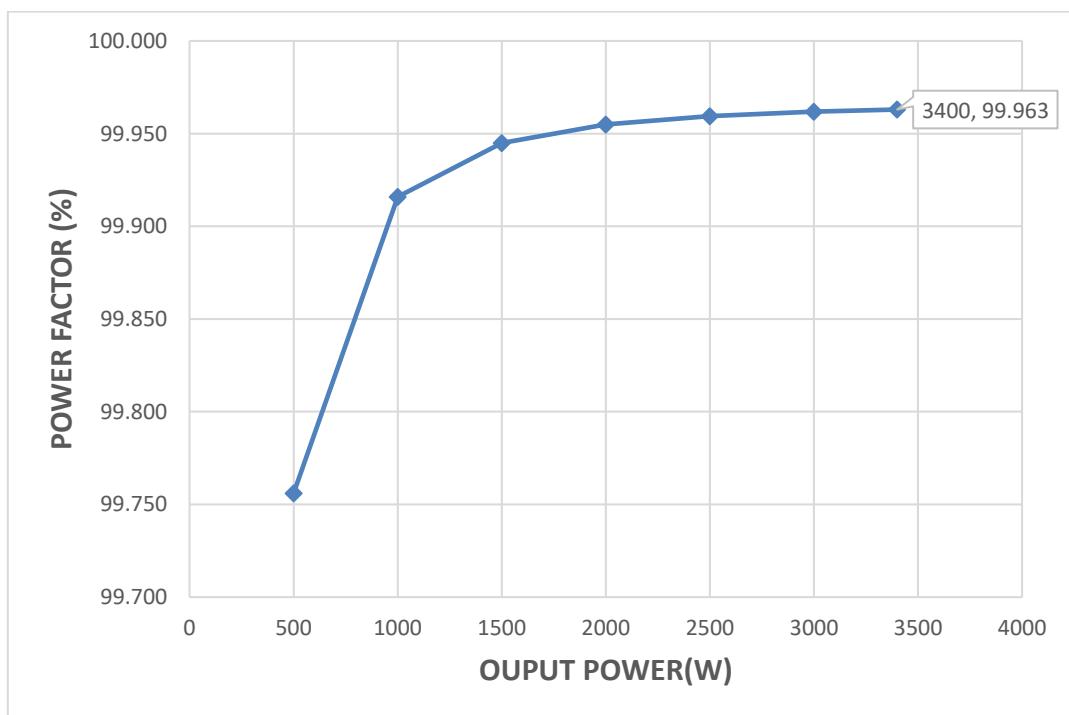


Figure 2.43. Load change behaviour on PF at 220VRMS

CHAPTER 3

7KW SINGLE STAGE ISOLATED INTERLEAVE LLC EV CHARGER DESIGN

3.1 Design and control stage summary

This is the second phase of the research work, which involves adapting the previously proposed converter for the design of a 7KW, 400V outdoor EV charger. The design would be summarized as it follows the same design procedure of case 1. A novel passive ripple cancellation (PRC) circuit was added to the converter in order to reduce the need for a high output capacitance. This PRC circuit offers simplicity in terms of the control design, higher PF leading to extremely low THDi at full load. Figure 3.1. shows the converter with the proposed novel passive ripple cancellation circuit. Only the ripple cancellation stage will be analyzed as other stages of the converter remain the same with the first design case.

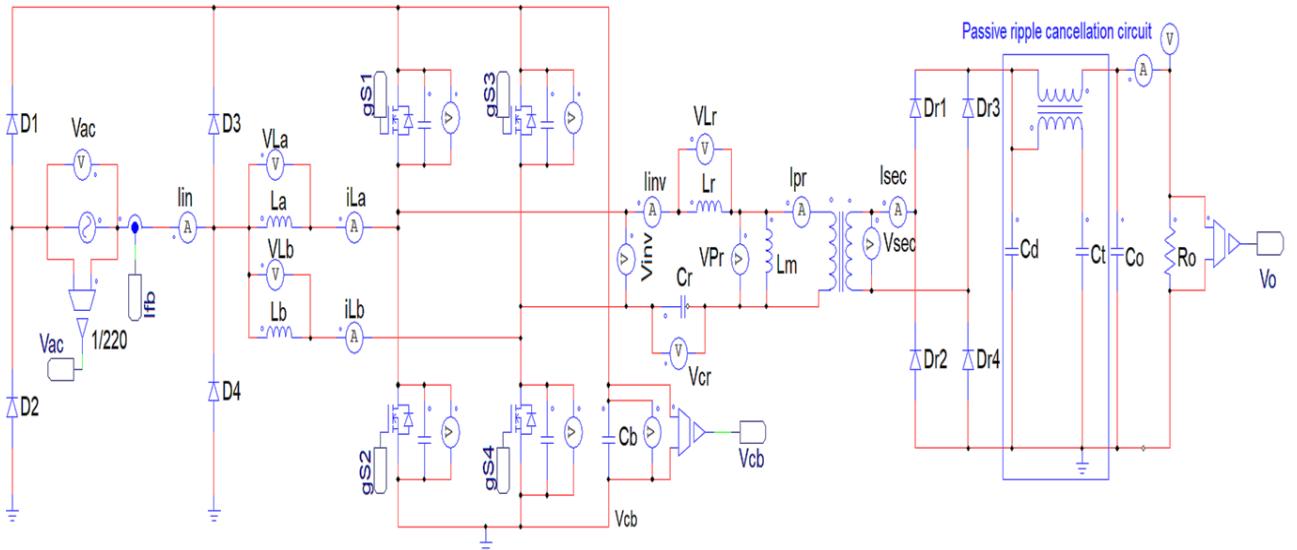


Figure 3.1 Converter design with PRC circuit

The DC-bus capacitance C_b was chosen to be $20\mu F$ at first. This is because the capacitor is decoupled by resonance eliminating the ripple constraint imposed on the DC – bus voltage V_{cb} as explained earlier during the previous design case. The claim by [9] about resonance tank acting as a high pass filter which attenuates the 100Hz low-frequency ripple was evident in this case due to the high voltage level

of the design. The peak current of the resonant inductor is high but would increase further if C_b was increased beyond $50\mu F$. This behaviour is valid for both $f_{sw} = f_o$ and $f_{sw} > f_o$ in this design.

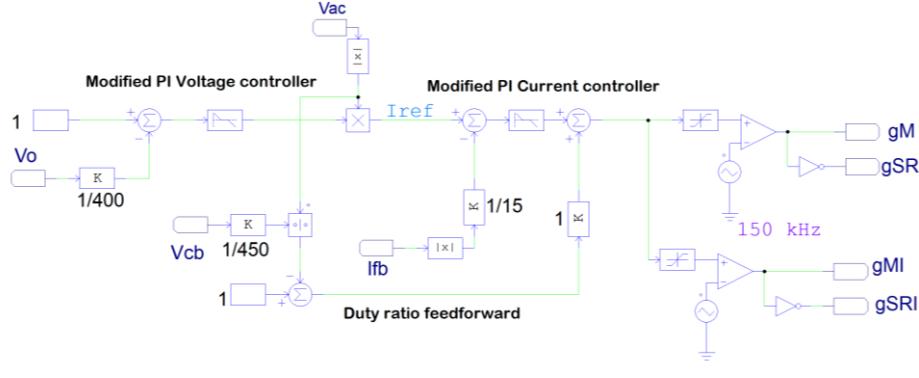


Figure 3.2 Simpler control system with duty-ratio feedforward in PSIM

The implemented duty – ratio feedforward, in this case, was less complicated as it only considers the V_{cb} . This is expressed in (3.1). Table 3.1 shows a summary of the controller parameters used for the simulation

$$d_{ff} = 1 - \frac{|V_{ac}|}{V_{cb}} \quad (3.1)$$

Table 3.1. Control design parameters from SmartCtrl

Current controller	$K_{pi}=6.89$, $T_i = 63.63\mu s$, $T_p = 25\mu s(40KHz)$, $f_{ci}=19KHz$
Voltage controller	$K_{pv}=10.45$, $T_{iv}=13.29m$, $T_{pv} = 10m(100Hz)$, $f_{cv}=22Hz$

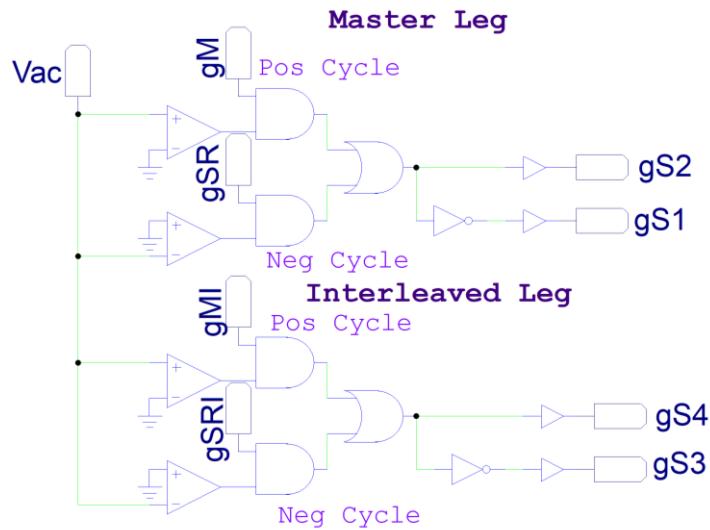


Figure 3.3 Gate driver design in PSIM

3.1.1 Ripple cancellation circuit analysis and design

3.1.1.1 Analysis of the PRC circuit

Looking at the input side of the converter, the voltage and current are assumed to be sinusoidal, therefore

$$v_{ac} = \sqrt{2}V_{ac} \sin(\omega_{ac}t) \quad (3.2)$$

$$i_{in} = \sqrt{2}I_{in} \sin(\omega_{ac}t) \quad (3.3)$$

The instantaneous power at the input is given by (3.4)

$$P_{ac} = \sqrt{2}V_{ac} \sin(\omega_{ac}t) \times \sqrt{2}I_{in} \sin(\omega_{ac}t) = V_{ac}I_{in}(1 - \cos(\omega_{ac}t)) \quad (3.4)$$

Where V_{ac} and I_{in} are the RMS values of the input voltage and current and ω_{ac} is the line angular frequency given by $2\pi f_{ac}$.

For simplicity, the input power is assumed to be equal to the output power and according to [20] the input power of a bridgeless PFC consist of two parts as shown in 3.5

$$P_{ac} = P_L + P_{rec} \quad (3.5)$$

Where P_L is the boost inductor power through L_a , L_b that is transferred to the DC bus (C_b) and the resonant tank and P_{rec} is the rectifier output power.

$$P_L = i_{in}L \frac{di_{in}}{dt} = \omega_{ac}Li_{in}^2 \sin(2\omega_{ac}t) \quad (3.6)$$

The output power of the rectifier is evaluated from (3.5) which is expressed as

$$\begin{aligned} P_{rec} &= P_{ac} - P_L = V_{ac}i_{in}(1 - \cos(\omega_{ac}t)) - \omega_{ac}Li_{in}^2 \sin(2\omega_{ac}t) \\ &= V_{ac}i_{in} - (i_{in}\sqrt{V_{ac}^2 + \omega_{ac}^2 L^2 i_{in}^2}) \sin(2\omega_{ac}t + \varphi) \\ &= V_{ac}i_{in} - P_{rp} \sin(2\omega_{ac}t + \varphi) \end{aligned} \quad (3.7)$$

Where $\varphi = \tan^{-1} \frac{V_{ac}}{\omega_{ac}Li_{in}^2}$ and $P_{rp} = i_{in}\sqrt{V_{ac}^2 + \omega_{ac}^2 L^2 i_{in}^2}$.

Since the converter, in this case, was assumed to be lossless then the output power

$$P_o = V_{ac}i_{in} \quad (3.8)$$

$$P_{ripple} = P_{rp} \sin(2\omega_{ac}t + \varphi) \quad (3.9)$$

P_{ripple} is the ripple component of the output power which is a second-order harmonic that needs to be filtered out by the PRC circuit thereby allowing only P_o to be transferred to the load. Figure 3.4 shows the ripple cancellation circuit extracted out from the circuit for analysis.

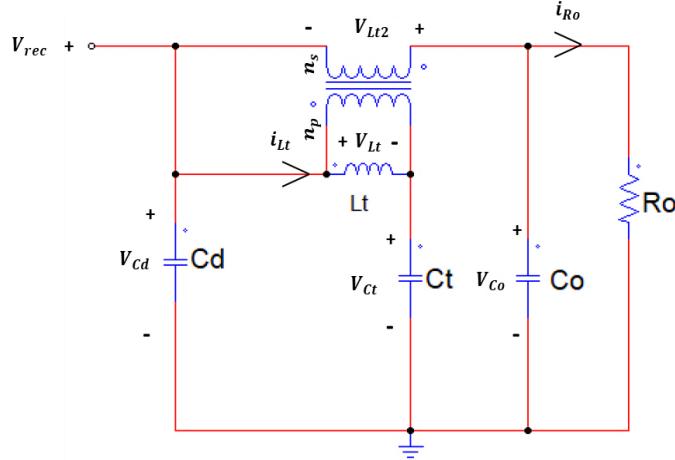


Figure 3.4 Extract of the proposed PRC circuit

\$V_{rec}\$ is the rectified voltage charging the decoupling capacitor \$C_d\$. The idea here is to store all the ripple power in \$C_t\$ such that the ripple voltage \$V_{ct}\$ which is sinusoidal is express as

$$V_{ct} = V_{ct} \sin(2\omega_{ac}t) \quad (3.10)$$

The magnetizing inductance \$L_t\$ also contain the ripple component therefore the current flowing through the magnetizing inductance is given by

$$V_{Lt} = L_t \frac{di_{Lt}}{dt} \quad (3.11)$$

$$di_{Lt} = \frac{V_{Lt}}{L_t} \sin(2\omega_{ac}t) dt = \frac{V_{cd} - V_{ct}}{L_t} \sin(2\omega_{ac}t) dt \quad (3.12)$$

$$V_{Lt2} = \frac{n_s}{n_p} V_{Lt} \quad (3.13)$$

$$V_{Co} = V_{Ro} = V_{cd} - V_{Lt2} \quad (3.14)$$

It could be seen from (3.13) that number of turns (\$n_p: n_s\$) influences the magnitude of the voltage \$V_{Lt2}\$ that would appear on the secondary side of the ripple cancellation circuit transformer. Therefore, at any time \$t\$ in the circuit \$V_{Lt2}\$ can either be negative or positive. If the number of turns is selected properly \$V_{Lt2}\$ can be as low as possible. When \$V_{Lt2}\$ is negative at any time \$t\$ in the circuit the voltage ripple appearing at the output would increase according to (3.15)

$$V_{Co} = V_{cd} - (-V_{Lt2}). \quad (3.15)$$

3.1.1.2. Design of the PRC circuit

The voltage across \$C_t\$ is expressed in (3.10) and if all the ripple power derived in (3.9) are to be stored in \$C_t\$, then the instantaneous power stored in \$C_t\$ is expressed as

$$\frac{1}{2} C_t \frac{dV_{ct}^2}{dt} = P_{ct} \sin(2\omega_{ac}t + \varphi) \quad (3.16)$$

from (3.10) and (3.16) and according to [20], [21] the voltage across \$C_t\$ can be expressed as

$$V_{Ct} = \sqrt{\frac{P_{Ct}}{C_t \omega} [K - \sin(2\omega_{ac}t + \varphi)]} \quad (3.17)$$

where $K \geq 1$ is a constant which was calculated from $K = (\frac{V_{Ct_max}^2 C_t \omega_{ac}}{P_{Ct}}) - 1$. i_{Ct} is also expressed as

$$i_{Ct} = \frac{P_{Ct}}{V_{Ct}} = \frac{P_{Ct} \sin(2\omega_{ac}t + \varphi)}{\sqrt{\frac{P_{Ct}}{C_t \omega_{ac}} [K - \sin(2\omega_{ac}t + \varphi)]}} \quad (3.18)$$

from (3.17) the ripple absorption capacitor C_t can be obtained from (3.19)

$$C_t = \frac{(K+1)P_{Ct}}{\omega_{ac} V_{Ct_max}^2} = \frac{(K+1)V_{Ct_max} i_{Ct_max}}{\omega_{ac} V_{Ct_max}^2} \quad (3.19)$$

According to [20], [21], K needs to be chosen such that the capacitance is minimized and the best choice is between 1 – 1.5. V_{Ct_max} is the maximum ripple voltage that must be absorbed by C_t and this can be estimated according to [22] expressed in (3.20)

$$V_{Ct_max} = \frac{P_o}{2\omega_{ac} C_o V_o} \quad (3.20)$$

L_t and C_t are in series and therefore must be designed to have a resonant frequency which is equal to the twice the grid frequency. This is expressed as

$$f_{rip} = \frac{1}{2\pi\sqrt{L_t C_t}} \quad (3.21)$$

f_{rip} is the ripple frequency, which in the case of this research is 100Hz.

3.1.1.2.1 Design procedure

- Calculate the decoupling capacitor from the equation (3.22), and in this case, the following assumptions were made: $V_{Cd_max} = 400V$, $V_{Cd_min} = 350V$ and $t_{hold} = 3ms$.

$$C_d = \frac{P_o \max t_{hold}}{V_{cd_max}^2 - V_{cd_min}^2} = 560\mu F \quad (3.22)$$

- Choose the output capacitor C_o which in this research was chosen to be $500\mu F$
- Estimate the maximum ripple voltage V_{Ct_max} from (3.20) as shown below

$$V_{Ct_max} = \frac{P_o}{2\omega_{ac} C_o V_o} = \frac{7000}{4\pi \times 50 \times 500 \times 10^{-6} \times 400} = 55.7V \quad (3.23)$$

- Calculate C_t from (3.19), assume $K = 1$ and $i_{Ct} = i_o$ in this case

$$C_t = \frac{(K+1)V_{Ct_max} i_o}{\omega_{ac} V_{Ct_max}^2} = \frac{(1+1) \times 55.7 \times 17.5}{2\pi \times 50 \times 55.7^2} = 2mF \quad (3.24)$$

- L_t is calculated from (3.21) which give $L_t \approx 1mH$
- The number of turns ($n_p : n_s$) is chosen such that V_{Lt2} can be as low as possible, which was selected to be 4:1.

Figure 3.5 validated the design process, and it could be seen that a ripple of 2V was present in V_{Co} . The voltage across V_{Lt} is about 10V which was stepped down to about 2.5V for V_{Lt2} . V_{Lt2} was then subtracted from V_{Cd} giving rise to an output voltage with extremely low ripple.

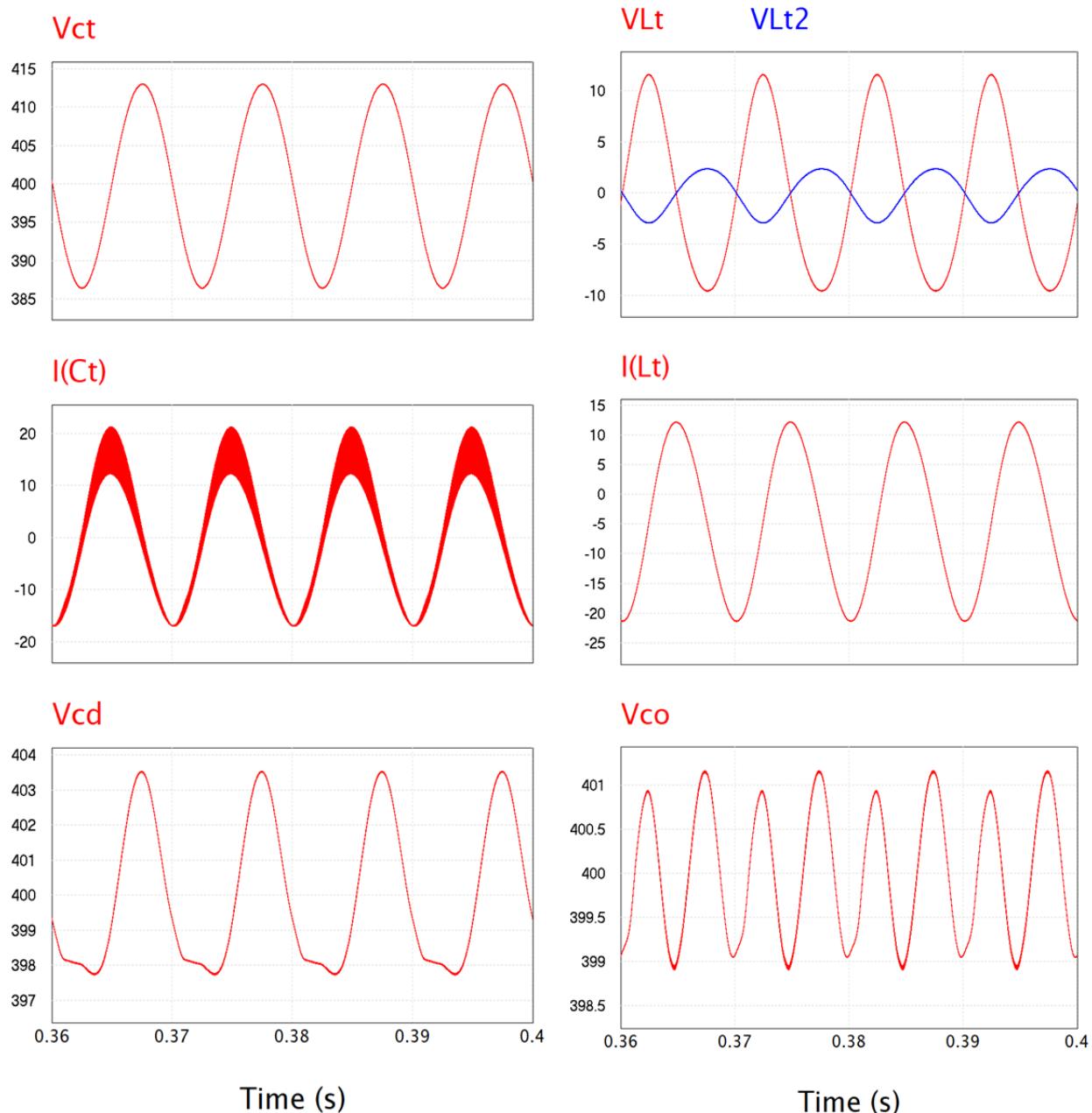


Figure 3.5 Simulation waveform for the ripple cancellation circuit

3.1.1.3 PRC circuit optimization.

The idea here is to reduce the output capacitance as much as possible. It was therefore discovered by trial that as the capacitance of the DC – bus decreased below the initial chosen value of $20\mu F$, the 100Hz attenuation ability of the resonant tank increases. This made it possible to reduce the ripple cancellation capacitor C_t below the $2mF$ previously used in the simulation for figure 3.5. This

reduction also gave room for the further reduction of the transformer number of turns but comes with the increase of the magnetizing inductance. This behaviour applies to the proposed converter topology used in this research work, but other types of converter topology can make use of the design procedure described earlier. The following conclusion was deduced from the discovery:

1. $K < 1$ leading to lower C_t as C_b is reduce further
2. f_{rip} from (3.21) can be a bit higher than the resonance frequency of 100Hz

Choosing $L_t = 1.4\text{mH}$, $C_b = 2\mu\text{F}$, $C_t = 1200\mu\text{F}$, $C_d = C_o = 500\mu\text{F}$ and $n_p : n_s = 2:1$ gave a better result as seen in figure 3.6. The total capacitance used at the output stage has now reduced from 3mF to 2.2mF, and this gave a better result than the previous case due to the lowered C_b . The peak-peak voltage ripple reduced further from 2V to 431mV; however, this comes with a tradeoff of little increased in the magnetizing inductance.

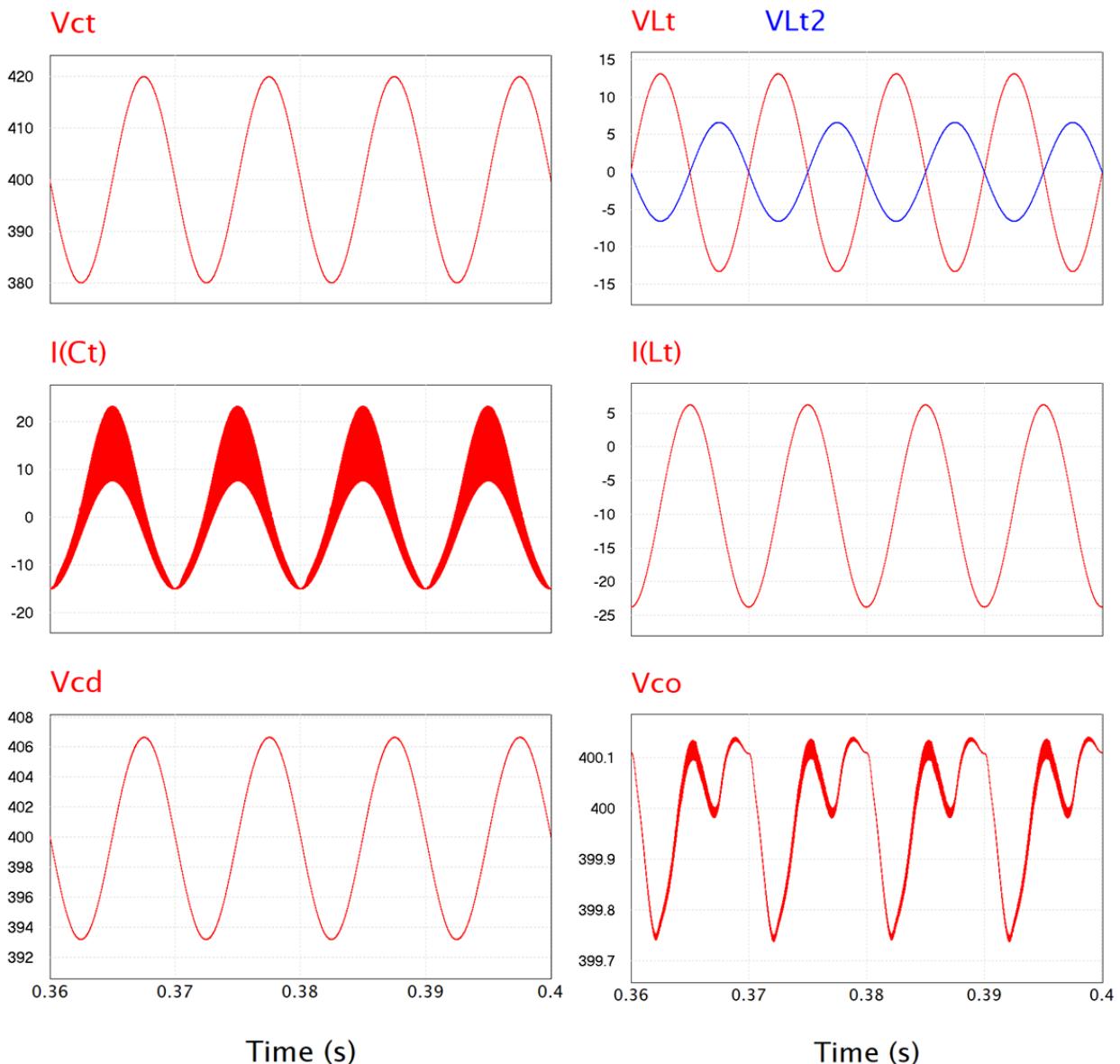


Figure 3.6 The waveform for optimized ripple cancellation circuit components

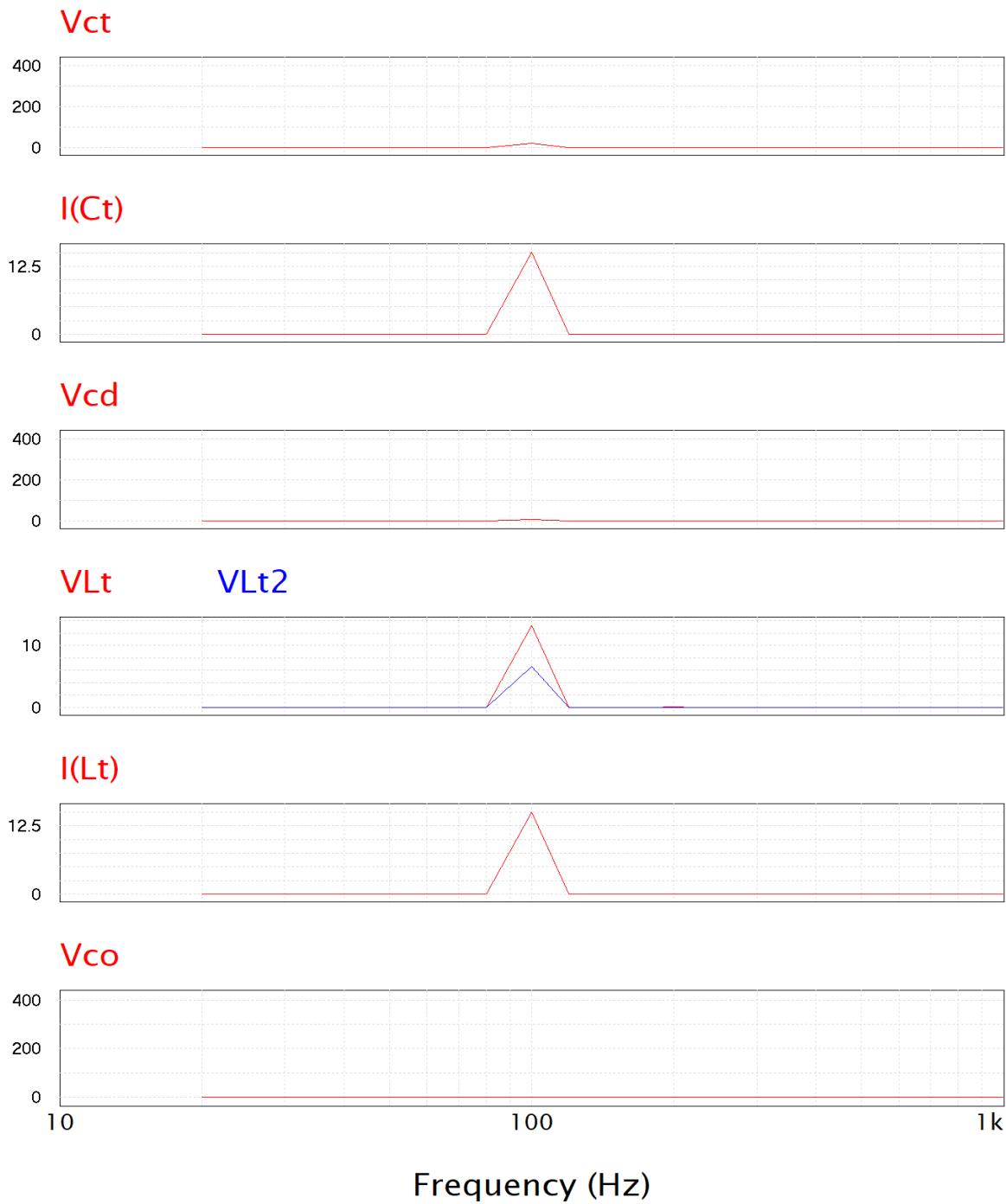


Figure 3.7 FFT of the ripple cancellation circuit section

Table 3.2. EV charger design specification summary

PFC stage component ratings	
Boost inductor (($L_a=L_b$)	300 μ H
DC-link capacitor (C_b)	2 μ F, 600V
Transformer ratings	
Turns ratio ($N_p: N_s$)	1:1
Voltage of primary/Secondary winding:	500/500 VAC
Primary/secondary winding rated current	28/28A
No load frequency	122KHz
Full load frequency	92KHz
LLC and Rectifier stage RMS components ratings	
Quality factor(Q), inductance ratio(K)	0.32, 10
Resonance inductor voltage and current rating (L_r)	2.5 μ H, 500V, 34A
Magnetizing inductor (L_m)	25 μ H, 500V, 15A
Resonance capacitor voltage rating	562nF, 500V
Primary side MOSFETs ratings	600V, 30A
ZVS capacitor ratings ($C_{s1} - C_{s3}$)	600V, 200pF
Output Rectifier diodes ratings (Dr1-Dr4)	400V, 20A
Ripple cancellation stage RMS components ratings	
Decoupling capacitor (C_d)	500 μ F, 450V
Ripple storage capacitor (C_t)	1200 μ F, 450V
Turns ratio ($n_p: n_s$)	2:1
Voltage of primary/secondary winding	15/8VDC
Magnetizing inductor (L_t)	1.4mH, 10V, 13A
Capacitor (C_o)	500 μ F, 450V

3.1.2. Simulation results

The simulated result in figure 3.8 follows the same pattern as the first design case. The input current i_{in} follows the input voltage V_{ac} depicting the characteristics of a PFC converter. A PF of 99.999% and an extremely low THDi of 0.47% was achieved at full load with an estimated peak efficiency of 97.1%. Owing to a better PF, the input ripple current has been eliminated and therefore create no need for an EMI filter. The combination of the low DC bus capacitance and the ripple cancellation circuit eliminated the second-order harmonics completely and reduced further the input current ripple than the first design case. The DC – bus voltage V_{cb} maintain a value between 390V to 470V at full load, eliminating the need for high voltage switches frequent in most high voltage single-stage design today. The magnetizing and resonant inductor has a peak current of 28A and 85A, respectively. The magnetizing inductor current is kept low due to the high K selected.

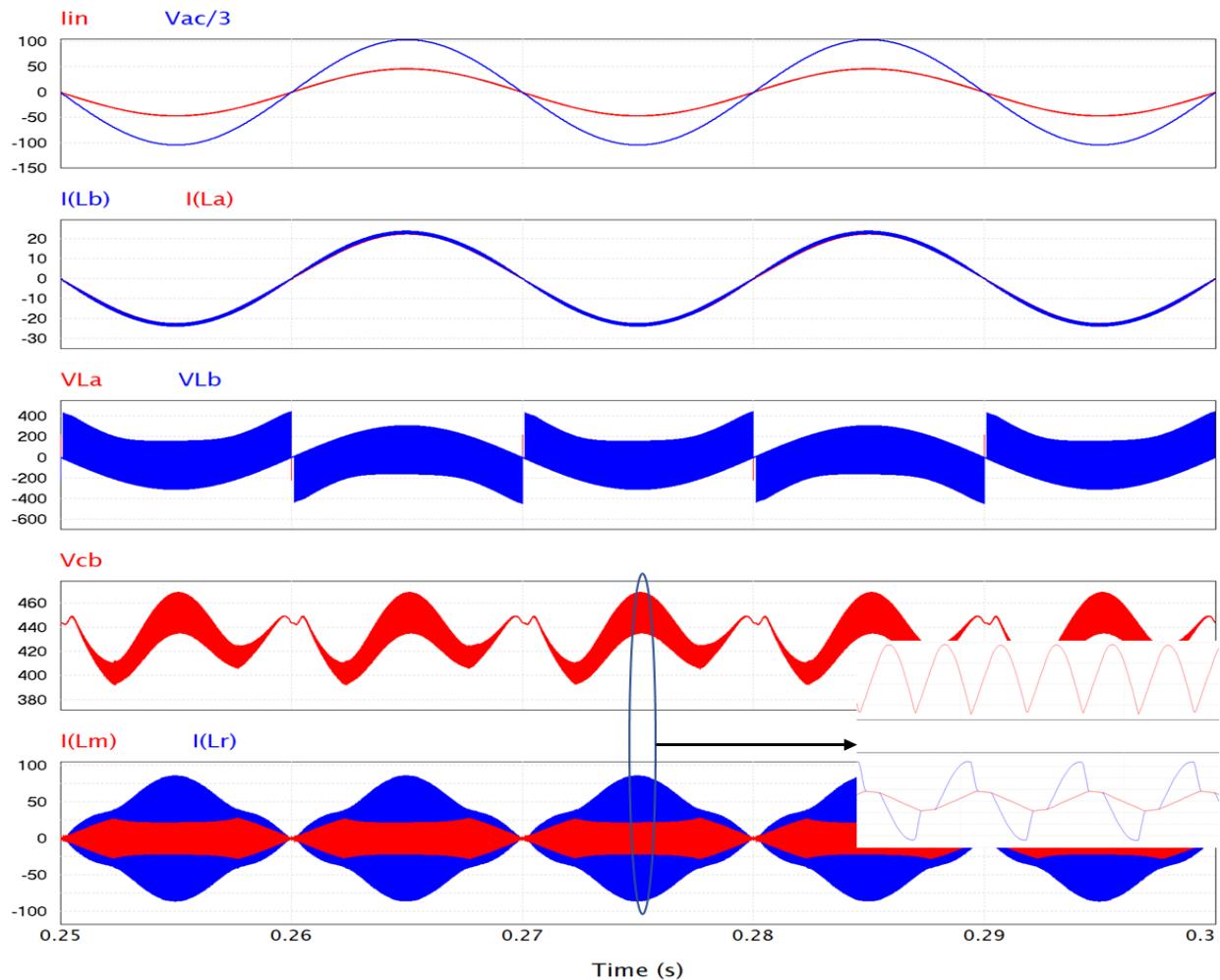


Figure 3.8 Voltage and current waveform on the primary side of the converter

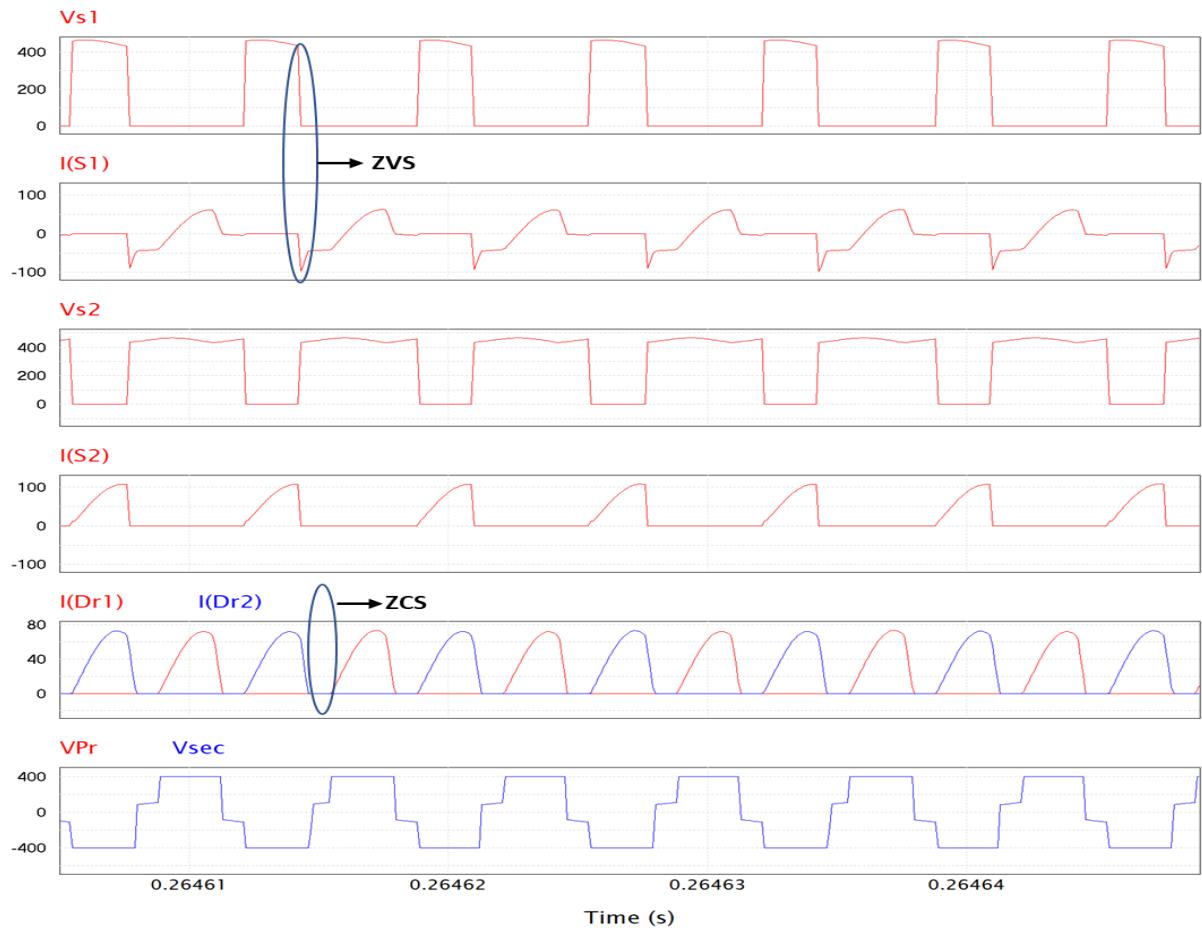


Figure 3.9 Waveform showing ZVS and ZCS of the input switches and output diodes

Figure 3.9 above shows the converter exhibiting ZVS at the input switches and ZCS at the output diodes which occur when energy transfer from the primary to the secondary side of the circuit seized. Figure 3.10 also shows the startup behaviour of the converter, and it could be seen that some ripple is present before dying out at steady state. This is because the reaction of the passive ripple cancellation circuit is slower than the active case because the ripple storage capacitor is charging up. Figure 3.11 shows the response of the converter to a sudden drop to 30% load and back to full load. The controller tracks back to the output voltage but the presence of ripple affirms the slower response of the ripple cancellation technique. This behaviour does not have an impact on an EV application but does for the telecom application due to the sensitivity of their equipment.

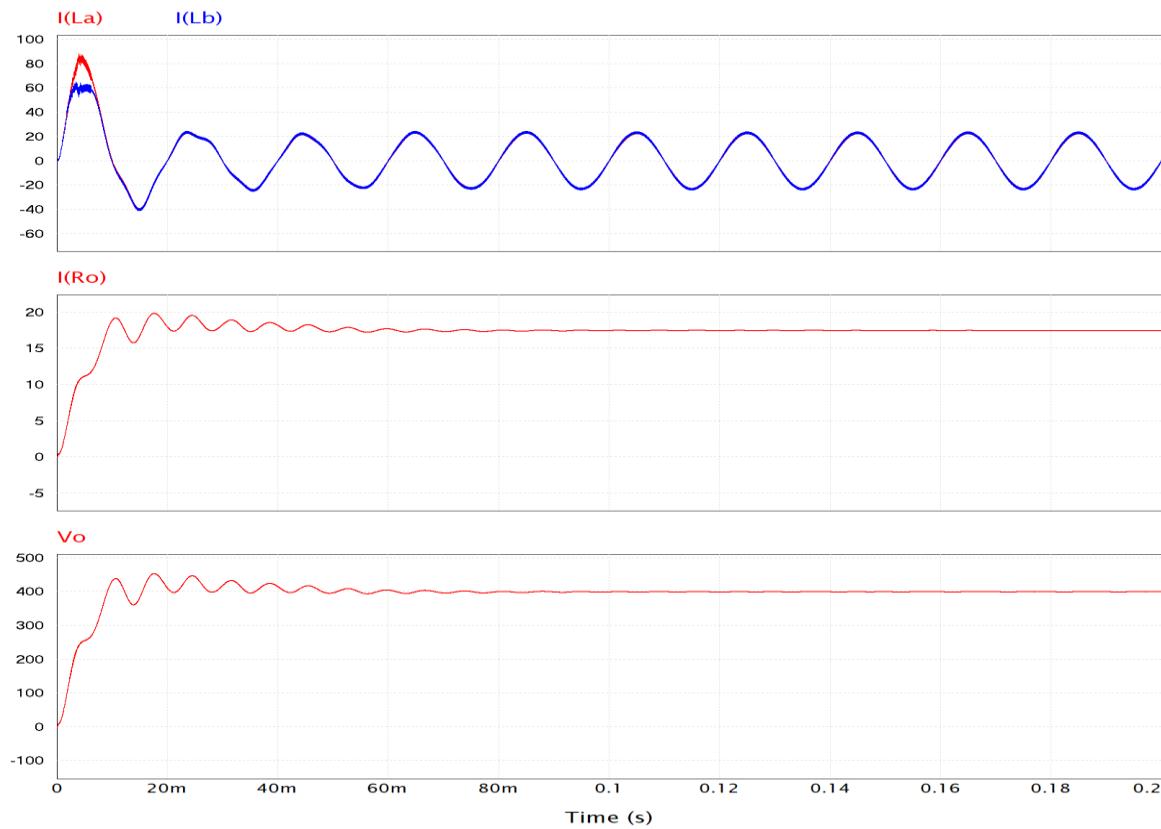


Figure 3.10. The waveform of output voltage and current at startup

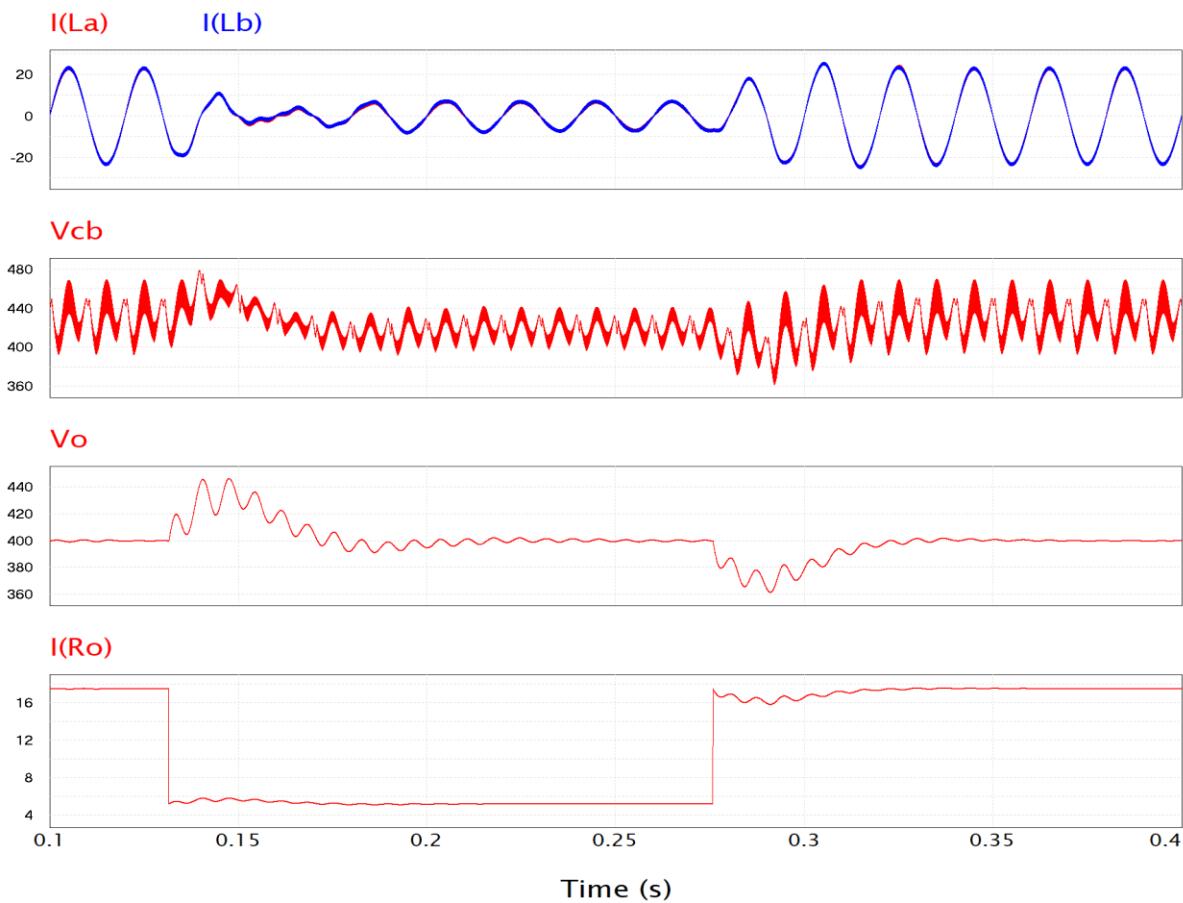


Figure 3.11. Waveform showing dynamic regulation of output voltage and current

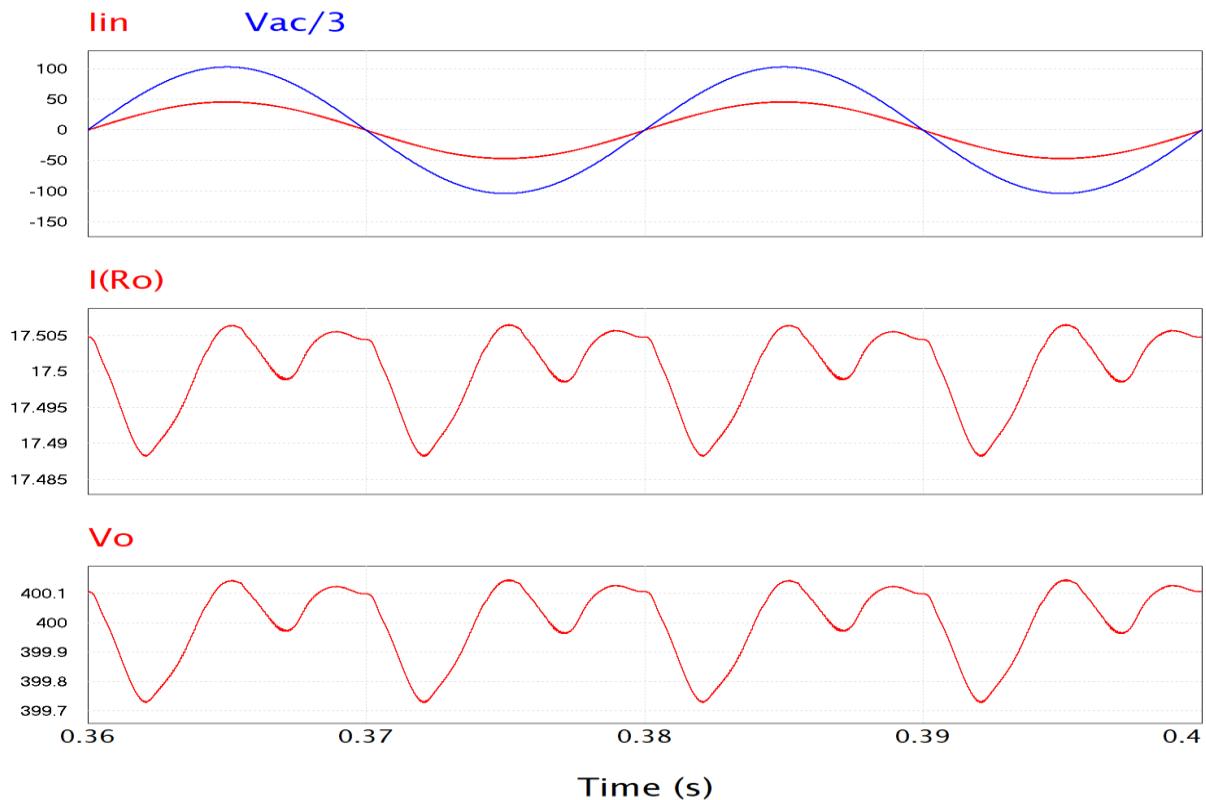


Figure 3.12 Output voltage and current with PRC at $C_{Total} = 2.2\text{mF}$ ($C_d + C_t + C_o$)

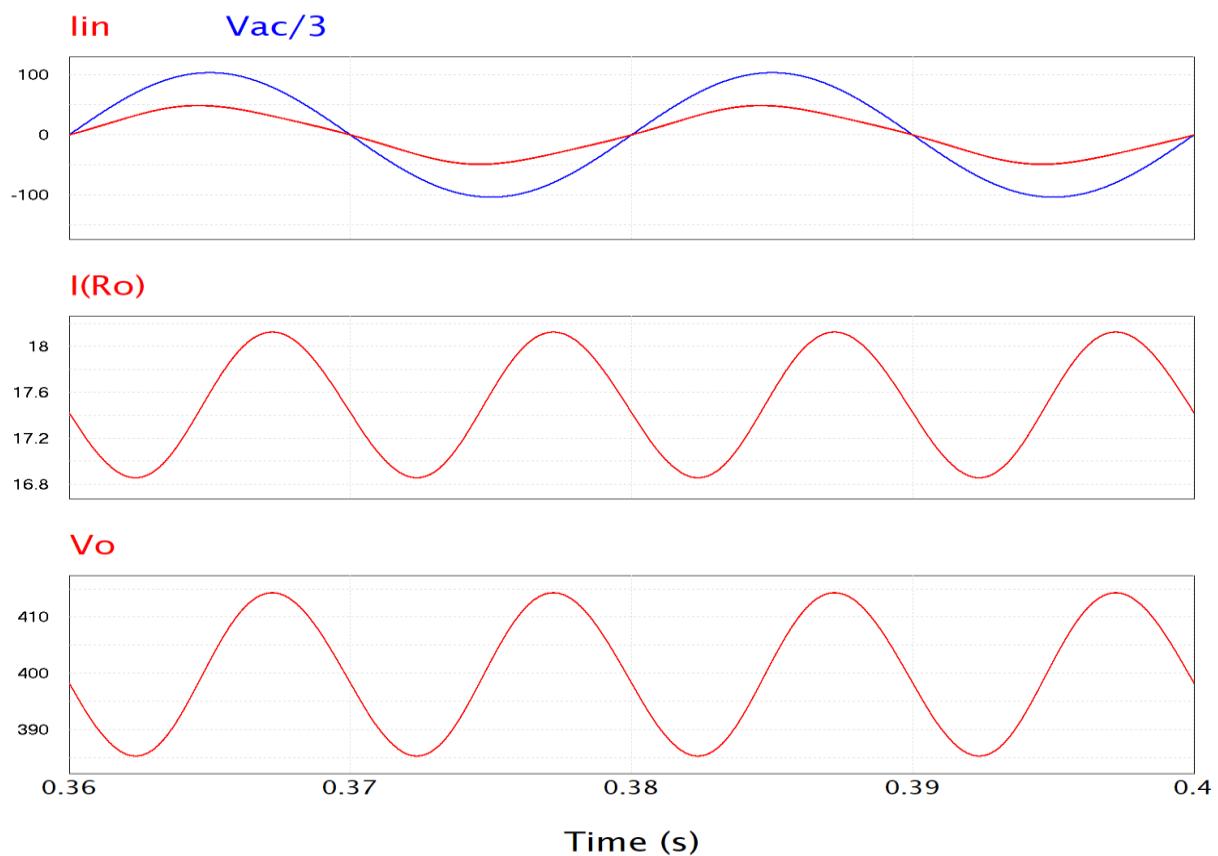


Figure 3.13 Output voltage and current without PRC at $C_o = 2.2\text{mF}$

3.1.4.1. Merits and demerits of the proposed passive ripple cancellation circuit

The passive ripple cancellation circuit provides the following benefits:

1. Very Low output capacitance and this is verified from the design criterion equation below.

$$C_o = \frac{P_{o \max}}{\Delta_v 2\pi \times 50\text{Hz} \times V_o^2} \quad (3.25)$$

Following the requirement of table 2.1, a 2%(8V) maximum output voltage ripple is required, and this gives C_o of 7mF, where $\Delta_v = 2\%$. However, with the proposed ripple circuit, the total capacitance of 2.2mF is used in the output stage to achieve a ripple of 431mV (0.1%). Meanwhile, without the ripple network, a capacitance of 129mF would be needed to achieve the peak to peak ripple of 431mV.

2. Better PF and extremely low THDi, which is evidently shown in figure 3.14 and 3.15. The 100Hz ripple is completely attenuated if the ripple stage is designed properly.
3. Lower voltage stress on the input switches, lower DC – bus voltage.
4. Simpler control, better ZVS and ZCS and lower cost due to need for lower components.

Demerits:

1. Higher magnetics which may lead to bulky size when compared with the active approach. The magnetics may also present higher thermal management requirement.
2. Slower response than the active ripple cancellation approach and this is because the ripple storage capacitor must charge up or discharge during start-up and sudden load change.

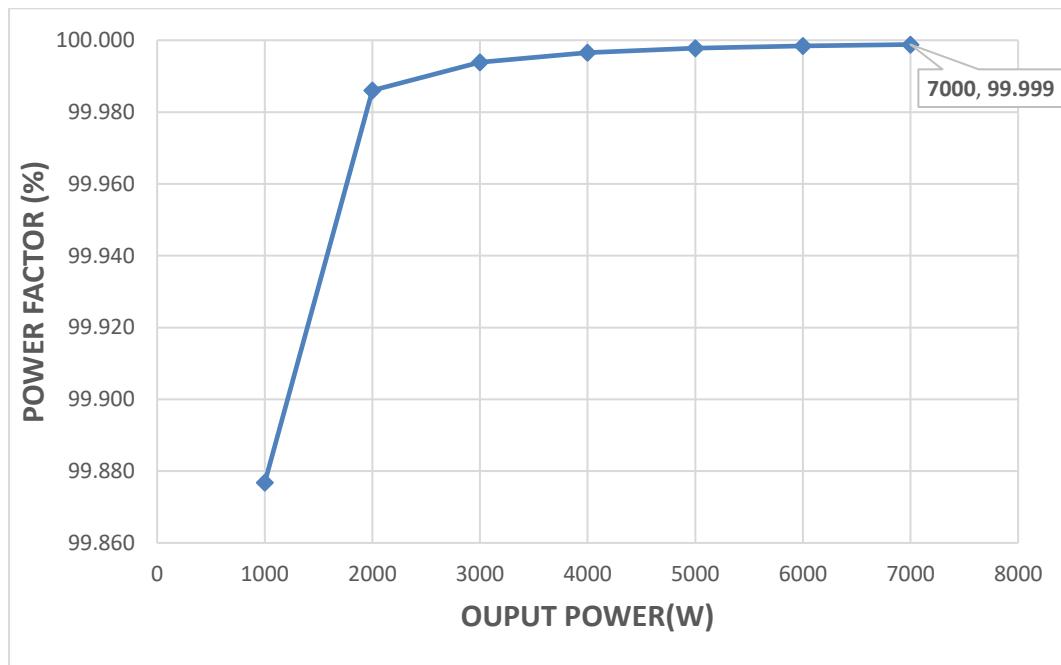


Figure 3.14. Converter load change power factor (PF) at 220VRMS

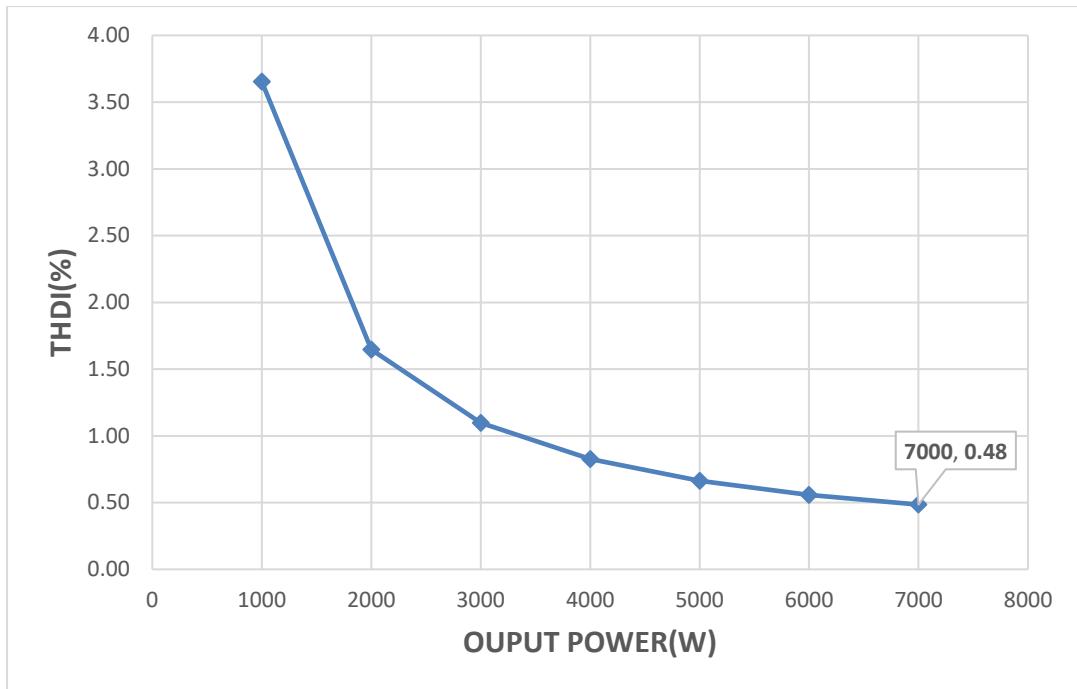


Figure 3.15. Converter load change on THDI at 220VRMS

CHAPTER 4

CONCLUSION AND FURTHER WORK

4.1 Conclusion

The research work presented a simulation model for an isolated single-stage single-phase interleaved resonant PFC rectifier for a telecom power supply and a unidirectional EV charger. The models were implemented in PSIM, and the control systems were designed using SmartCtrl and then verified with MATLAB control toolbox. Some part of the loss analysis like the inductor and transformer losses estimation was done using the Magnetics inductor design tool and Poweresim transformer design tool, respectively.

The first part of the research work was the design of a 3.4KW/58V telecom power supply. The circuit consists of three design stages which are the PFC, LLC, and output active ripple cancellation stage. Accurate equations gotten from literature was used to size correctly component values of the PFC.

However, the LLC stage was modelled practically using a written C code linked with the LLC circuit designed in PSIM. This employed modelling strategy was able to reflect the exact resonant circuit behaviour of the chosen topology, thereby providing an accurate guide in developing an efficient LLC circuit. Through the modelling, it was evidently shown that the converter has a wide region at which it achieves natural ZVS as oppose to theoretical modelling approach that mostly demonstrates a smaller ZVS region.

The active ripple cancellation circuit based on buck topology was able to reduce the output voltage ripple to 6.7mV which is below the maximum allowed ripple of 200mV. ZCS of the output diode was still maintained despite the addition of this ripple circuit. Average current mode control was developed together with a feedforward control for the design of the PFC stage, and a separate two-loop control system was used for the ripple cancellation stage. The feedforward control performed the purpose of eliminating the zero-crossing delay, better tracking of the DC – bus and decoupling capacitor voltage. The output voltage was also synchronized with the PFC control system through the feedforward control; thus, a sudden change in the output load is reflected accurately on the input stage. A THDi of 2.3%, PF of 99.6% with a peak efficiency of 95% was achieved after analysis.

Meanwhile, the second part, which is a 7KW/400V EV charger followed the same design process only that a novel passive ripple cancellation circuit, was used to take out the output voltage ripple. The passive approached was able to reduce a high ripple of 50V to 431mV with extremely low capacitance. It gave the benefit of more straightforward control, lower switching stress due to the lower DC – bus voltage and lower overall system cost. The drawback of the passive ripple cancellation approach is the presence of higher magnetics, making it unsuitable for low voltage high current application.

After analysis, an extremely low THDi of 0.47% with an efficiency of 97.1% was obtained for the EV charger case. This owes to the fact that the DC-bus capacitor attenuates some of the 100Hz ripples and the remaining unattenuated ripple are stored in the ripple cancellation circuit capacitor.

4.2 Further Work

Finally, due to the COVID – 19 pandemic, a real-life implementation was not possible, and therefore further work would be to build a prototype with the suggested specification and components. This would allow the investigation of the real-life behaviour of the two proposed converter, part of such is to investigate the transient behaviour of the GaN transistor, effect of the gate drive circuit on the control system and PCB parasitic effects.

More so, the proposed passive ripple cancellation circuit needs also to be implemented physically in other to verify further the claimed results and determine the thermal requirement owing to the increased magnetics.

The efficiency calculation done in this work is just an estimation, and this can be further improved by investigating the addition of more GaN switches in parallel, and the effect of such addition should also be investigated.

APPENDIX A

Literature Review

PFC Topologies

This section describes a summary of the studied PFC topologies during the research work; it also presents the advantages and drawback observed from the topologies.

A.1 Boost PFC topology

Yung-Sung et al. carried out a comparative performance analysis of four boost PFC topologies namely back-to-back bridgeless boost PFC (BTBBL PFC), semi-bridgeless boost PFC (SBL PFC), interleave boost PFC and Average current mode PFC (ACM PFC). The study demonstrated the ability of all the PFC to attain high efficiencies; however the ACM boost PFC is considered for high efficiency but the diode bridge limits the topology as it accounts for 50% of the losses and this prompted the need for higher efficient PFC which are the other types mentioned earlier. [23]

Of all the four topologies the SBL boost PFC performed better in terms of efficiency, power loss and a more converging PF to 1. The efficiency fluctuation degree for SBL is the lowest, and its average efficiency is the highest, ACM PFC topology performance followed SBL topology. SBL had an efficiency of 98% at heavy load and ACM PFC 96.48% for heavy load making it the second-highest efficiency of all the topologies but with the best Power factor of all of them. The interleave has the lowest variation in ripple due to a 180 degrees phase shift.[23]

The BTBBL PFC have its efficiency decreasing at about 40% load, making the topology the worst mass-capacity specification with respect to other topologies. However, the SBL uses the highest components, thus will be more costly and bulky, the BTBBL uses the fewer components.[23]

A.2 SEPIC PFC topology

A literature review summary of non – isolated and isolated SEPIC PFC topology is presented below:

A.2.1 Non-isolated SEPIC PFC

Ali et al. proposed SEPIC converter was operated in CCM mode due to the advantage of reduced ripple and current stress which occurs when in DCM. An efficiency of about 94% was achieved at high voltage or 100% load; the drawback of his study is the focuses on low power application. Full bridge rectifier with diode was used which account for the low efficiency at low power. No isolation which may make the LEDs prone to EMI.[24]

Al Jabri et al., topology worked in DCM operation, which provides the benefit of a soft turn-on switching. It provided extended voltage gain without stressing the duty cycle. The coupled magnetic configuration used to result in higher efficiency and high-power density. The efficiency achieved was about 98.3% but complex control strategy, no galvanic isolation and high conduction losses due to the number of diodes creating the need for high thermal management requirement. [25]

Kishore and Tipathi, topology is Suitable for very high voltage application due to the cascaded capacitor and diodes and the coupled inductors. The control strategy used is simple as it uses average current mode control. The circuit is susceptible to conduction losses due to the high number of diodes. Increased cost due to the high number of components and isolation would be difficult.[26]

Mahdavi et al., SEPIC converter input current is continuous due to the presence of two inductors which make it to operate in both CCM and DCM mode. The writers compare the SEPIC rectifier with convectional boost PFC in terms of semiconductors in the current flowing path and the design necessary to carry the DC current as well as high-frequency ripple current. The SEPIC topology proposed here eliminate the problem of semiconductors in the current flowing path and reduce high-frequency ripple current. Bridgeless boost PFC has three passive components which add to its weight and volume, also doubles the output voltage thus increased size of output filter while the new bridgeless SEPIC PFC has no extra passive or active components in the current path and therefore reduced size. The converter operates in DCM thus low power, higher cost due to the increased number of switches, bulkier compare to convectional SEPIC.[27]

Sindhuja and Sripriya design provided the advantage of low voltage stress on the switch and simple design, which is desired for high power and voltage application, less component thus reduced cost. Low switching and conduction loss but the drawback are the absence of isolation, the efficiency value not included and high cost due to inductors used.[28]

A.2.2 Isolated SEPIC PFC

One of the aims of this research is to use isolated configuration, and this reason previous work on isolated SEPIC topologies were studied and a summary is presented below:

Swati et al. topology at the input side reduce conduction losses and thermal stress since it is bridgeless. SEPIC converter generally provides the advantage of low input current ripple, inrush current limit during overload and startup conditions and reduced EMI due to operation in DCM. The simple dual control strategy was implemented, and the topology was used for high current and low voltage application. The drawback was reduced efficiency as a result of conduction losses due to the four diodes used in the circuit. A large number of components and since it is SEPIC to buck, it can be concluded that it is a two-stage PFC. Totem pole can be used at the input stage to eliminate the Diode which was proposed for future work by the authors.[29]

Ewerling et al. converter uses a few numbers of components and provides galvanic isolation. SEPIC converter generally offers the benefit of step-up/down features, absence of startup transient and reduced THD due to the PFC as discovered by previous studies. The paper suggested that the topology can be suited for high voltage application; however, the efficiency was about 93% at 200W design which is low. More modification is needed to improve efficiency.[30]

Deliang Wu et al., topology has the advantage of addressing the voltage spikes issues caused by the leakage inductance of the transformer, allow ZVS for both the main switch and active clamp switch, provides a step up and down function thus suitable for wind input and output voltage range. The circuit behaviour of the topology makes it ideal for SiC devices because SiC MOSFET have higher voltages with low R_{ds} . Secondly, the turn-on switching losses of SiC MOSFETs are higher than the turn off switching loss however this issue is eliminated using ZVS and thirdly due to high switching frequency of SiC, the transformer and inductor size can be reduced and lastly the turning off of the output diode is controlled which reduces the reverse recovery losses. The drawbacks are that the transformer operates only in one cycle, thus limiting the power level. There is the presence of higher steady-state voltage stress on the switch due to the parasitic capacitance of the diode. This induces resonance with the resonant inductor and causes oscillation in the voltage across the diode and transformer winding,

thus double voltage stress on the output diode. The topology does not use bridgeless concept hence higher conduction losses in the input current path

Dianli Hou et al. also affirm SEPIC converter provides restraining inrush current when starting and even less ripple at the input current together with low EMI. The author compared all the bridgeless PFC topologies with each other in terms of EMI noise and Highmark on the drawback of them. To conclude, their output voltage must be higher than the input voltage, whereas SEPIC can work as a boost or buck converter. The presented topology here uses fewer components when compared with other bridgeless SEPIC, provides low EMI and galvanic isolation between the input and output. The converter operates in DCM mode; thus, low power and also the efficiency was not included in the research. The output voltage witness variation within 100Hz frequency due to the practical limitation of the output capacitor.

Parag T. et al. study was focused on developing a more robust control strategy which could reduce input current distortion under high line frequency and when the feedback control loop has low bandwidth. A limitation is that it cannot be applied directly to other boost derived topologies like isolated SEPIC due to the inductor voltage is not equal to the difference between the rectified voltage and output voltage.

A.3. H-bridge and buck PFC topology

A combine literature review summary of H-bridge and Buck PFC topology is presented below.

A.3.1 H-bride PFC topology

Chushan Li and Dewei Xu converter type does not make use of DC-link capacitor, thus claimed with this absence, the converter is preferred for high power density. It is a current fed bridge converter with better advantage than boost PFC but behaves like it. The current fed bridge converter has a clamping circuit which eliminates switching transient, high voltage spikes from the switches. IGBT was used in the design due to the feature of longer turning off time than MOSFET.

The drawback is higher conduction losses due to the high number of conductors used together with the switches and also at the input and output of the AC source. An efficiency of 94% was achieved but could improve with the reduction of conduction loss.[31]

Shushan Li, Yu Zhang, paper talk about the usefulness of single-page isolated PFC in high power application due to the advantage of smaller size as a result of input filter capacitor absence. Current fed bridge inverter uses ZCS due to the benefit of eliminating IGBT turn-off losses. Traditional PFC control is used for the circuit. The drawbacks are higher conduction loss due to the increased number of diodes used, higher reverse recovery loss due to resonance thus needs higher diode rating, and too many components and switches leading to higher cost[32]

F. Jauch and J. Biela paper uses a bidirectional switch to eliminated AC/DC conversion using a diode and uses both phase shift and frequency control. The circuit makes use of no diode thus more efficient. Too many switches thus more cost. The control strategy is complex and cannot be easily implemented.[33]

A.3.2 Buck PFC topology

Buck converter is not usually suitable for PFC purpose due to the absence of inductor at the input, thereby making it have a discontinuous input current, but some papers demonstrated the ability of its use in PFC.

R. Kalpana et al. proposed HF isolated buck converter, which has the advantage of less switch stress due to the switch pair operating in half PWM. Easy control strategy as all switches uses a single PWM source and suitable for high voltage application. The drawback is that the duty ratio can't be more than 0.5, and more losses through the diode bridge.[34]

Vitor Fernao Pires and Jose Fernando Silva discoursed a single-stage double buck topology using H-bridge which can operate at higher output voltage than the AC input voltage. This converter type can limit inrush and DC short circuit currents. Complex control strategy as the control system contains two loops. The output loop, which controls the AC input, uses sliding control, and the inner loop uses a PI controller.[35]

Other topologies that could be used for PFC is the CUK converter which has an input inductor with continuous current, but it was not discussed in this research due to the patent-related issues with it.

APPENDIX B

Converter Loss Estimation Analysis

B.1 3.4KW Telecom PSU Power Loss Estimation

The RMS voltage and current value for each component is extracted from the simulation and used to estimate the losses. The required information is extracted from the datasheet and the manufacturer website. Some already design software tools like inductor design tool from magnetics and transformer design tool from Poweresim was used to estimate the transformer losses. The RMS voltage and current used in the calculation was extracted from the simulation carried out.

B.1.1 Boost inductor

The maximum current L_a and L_b must carry was calculated earlier to be 15A but a value of 17A was used as this factor in the worst-case scenario of the current ripple. Two separate inductors of the same ratings are needed, but only one design is done to estimate the losses since they both have the same inductance value. The core and copper losses can be calculated from (B.1) and (B.2).

$$P_{Core.loss} = \rho f^\alpha B_m^\beta V \quad (B.1)$$

Where ρ is loss factor, f is the frequency, α frequency coefficient, B_m is the flux swing, β is magnetic flux density coefficient, V is core volume.

$$P_{Cu.Loss} = I_{in_rms}^2 \times R_{ac} \quad (B.2)$$

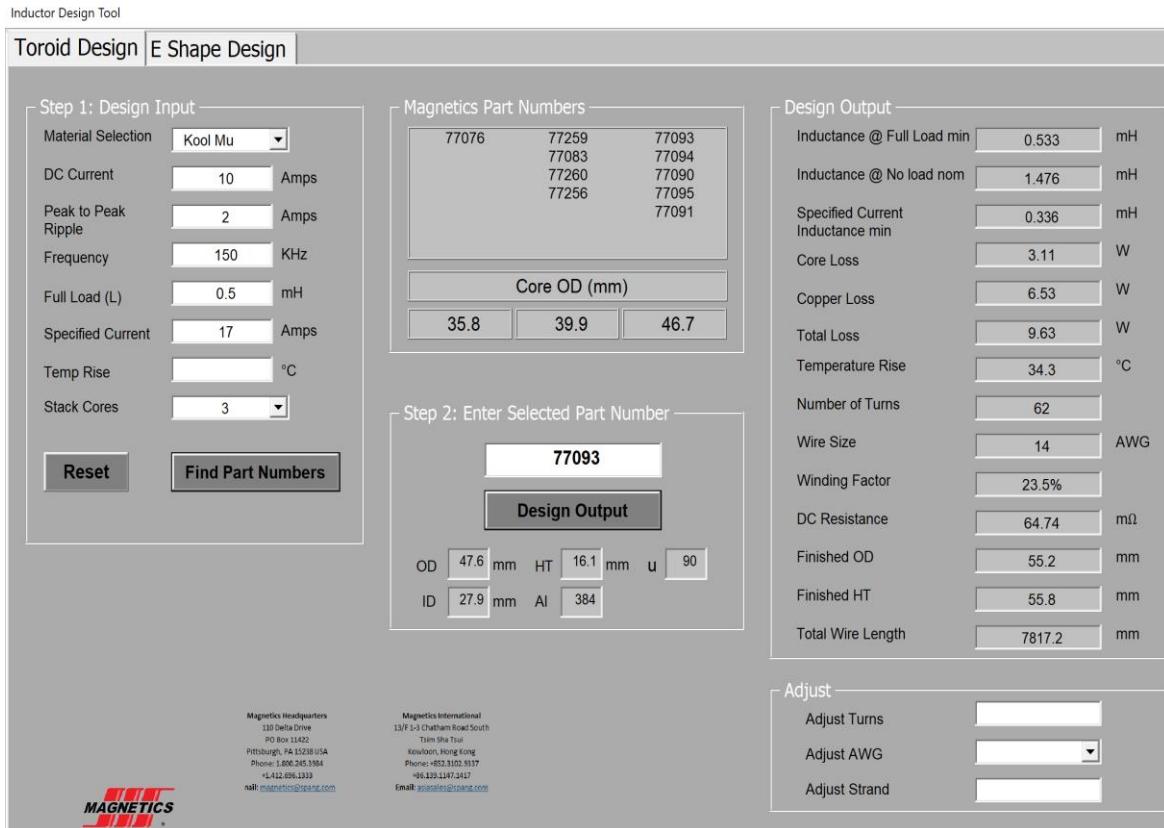


Figure B.1 Input Inductor design using the Magnetics tool

The chosen material is Kool Mu from Magnetics with part number 0077093A7. Toroid design was selected, consisting of 3 stacked cores, and the material permeability is 90 μ . The total loss consisting of the core and copper loss is 9.63W, therefore the two inductors (L_a , L_b) would have a loss of 19.26W.

B.1.2 Line rectifier MOSFET

Diode D1 and D2 are to be replaced with line rectifier MOSFETS. CoolMOS IPT65R033G7 was selected, and it has an R_{on} of 33m Ω . Since each of the MOSFET would conduct for only half of the line cycle, only the conduction loss is considered. $I_{in_rms} = 17.9A$ was extracted from the simulation giving the loss expressed below

$$P_{LineMos.loss} = I_{in_rms}^2 \times R_{on} = 10.57W \quad (B.3)$$

B.1.3 GaN transistor conduction and switching loss.

GS66516B 650V transistor was used to estimate the switching loss. According to [36] the conduction loss is expressed as

$$\begin{aligned} P_{sw.cond} &= P_{c.mos} + P_{s.body} \\ &= 4I_{mos_rms}^2 R_{ds} + 4(V_d I_{anti_ave} + I_{anti_rms}^2 R_{body}) \end{aligned} \quad (B.4)$$

The selected transistor has no body diode making the second part of (B.4) to be zero, and this reduced the loss equation (B.5). An R_{ds} of $32\text{m}\Omega$ was extracted from the datasheet and an RMS current ($I_{mos,\text{rms}}$) of 12.9A was extracted from the simulation.

$$P_{\text{cond}} = P_{c,\text{mos}} = 4I_{\text{mos},\text{rms}}^2 R_{ds} = 21.3\text{W} \quad (\text{B.5})$$

The switching losses of a GaN transistor can be estimated from (6.6) with $V_{\text{mos},\text{rms}}$ of 323V .

$$\begin{aligned} P_{s,\text{sw}} &= 4\left(\frac{f_{\text{sw}} V_{\text{mos},\text{rms}} I_{\text{mos},\text{rms}} (t_r + t_f)}{2}\right) \\ &= 4\left(\frac{150\text{KHz} \times 308.6\text{V} \times 12.9(12.4\text{ns}+22\text{ns})}{2}\right) = 41.08\text{W} \end{aligned} \quad (\text{B.6})$$

$$P_{\text{drive loss}} = 4\left(\frac{1}{2} C_{gs} V_{gs}^2\right) f_{\text{sw}} = 1.94\text{mW} \quad (\text{B.7})$$

The total loss across the switch in a full line cycle is given expressed as

$$P_{\text{Sw.total_loss}} = \frac{P_{\text{sw.cond}} + P_{s,\text{sw}} + P_{\text{drive loss}}}{2} = 31.19\text{W}. \quad (\text{B.8})$$

B.1.4 DC – bus and resonant capacitor loss

Four MKP1849 metallized Polypropylene DC-LINK capacitor rated $500\mu\text{F}/900\text{V}$ from VISHAY was selected due to the extremely low ESR gotten from figure B.2. The capacitors are to be assembled in parallel to add up to $2000\mu\text{F}$. The ESR_{cb} is $1\text{m}\Omega$ at 100Hz in figure B.2 and the capacitor RMS current ($I_{cb,\text{rms}}$) gotten from the simulation is 15.79A . The power loss is expressed by (B.9)

$$P_{cb,\text{loss}} = I_{cb,\text{rms}}^2 ESR_{cb} = 0.25\text{W} \quad (\text{B.9})$$

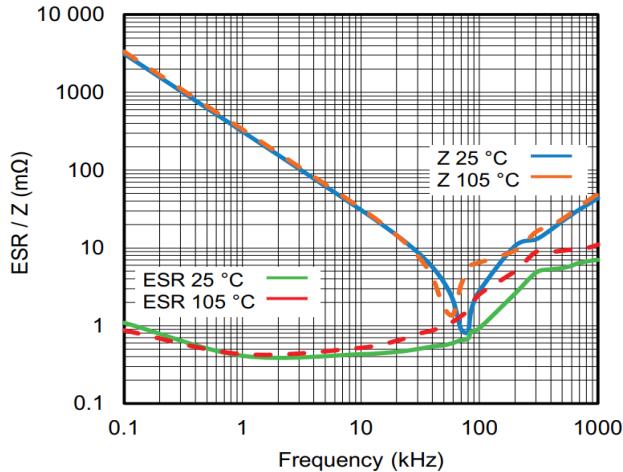


Figure B.2 ESR as a function of frequency at different temperatures.[37]

Panasonic ECWFD2JK capacitor was chosen for the resonant capacitor with a capacitance range of $0.27 - 0.82\mu\text{F}$ at 630V . The dissipation factor ($\tan \delta$) extracted from the datasheet is 0.1% . Therefore the ESR_{cr} is calculated from (B.10) and the loss across the resonant capacitor is calculated from (B.11)

$$ESR_{Cr} = \frac{\tan \delta}{2\pi f_{sw} C_{Cr}} = 2.71 \text{m}\Omega \quad (\text{B.10})$$

$$P_{Cr.loss} = I_{r.rms}^2 ESR_{cr} = 17.19^2 \times 2.71 \text{m}\Omega = 0.8 \text{W} \quad (\text{B.11})$$

B.1.5 Resonant inductor loss

Integrating the transformer with the resonant inductor is usually difficult to implement, and therefore a separate resonant inductor is assumed. The loss was estimated using the same inductor loss estimated software as the boost inductor. MPP material was selected as it has relatively high permeability, low core loss and better temperature stability. From figure B.3, suggest MPP55585 as the best in keeping the losses and temperature as low as possible. The total loss estimated with the tool is 1.70W.

Inductor Design Tool

Toroid Design | E Shape Design

Step 1: Design Input

Material Selection	MPP
DC Current	30 Amps
Peak to Peak Ripple	2 Amps
Frequency	150 KHz
Full Load (L)	0.00648 mH
Specified Current	18 Amps
Temp Rise	°C
Stack Cores	1

Reset **Find Part Numbers**

Step 2: Enter Selected Part Number

55585					
Design Output					
OD	35.2 mm	HT	9.8 mm	u	125
ID	22.5 mm	AI	79		

Design Output

Inductance @ Full Load min	0.007 mH
Inductance @ No load nom	0.020 mH
Specified Current Inductance min	0.012 mH
Core Loss	0.04 W
Copper Loss	1.66 W
Total Loss	1.70 W
Temperature Rise	29.4 °C
Number of Turns	16
Wire Size	9 AWG
Winding Factor	28.2%
DC Resistance	1.84 mΩ
Finished OD	41.8 mm
Finished HT	16.4 mm
Total Wire Length	707.2 mm

Adjust

Adjust Turns
Adjust AWG
Adjust Strand

Magnetics Headquarters
110 Delta Drive
Pittsburgh, PA 15238 USA
Phone: 1.800.245.1984
Fax: 412.699.1333
Email: magnetics@reson.com

Magnetics International
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Kowloon, Hong Kong
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Fax: +852.3391.1417
Email: asiasales@reson.com



Figure B.3 Resonant inductor loss estimation using the magnetics design tool

B.1.6 Transformer design and loss estimation

The transformer was modelled in Poweresim software to be a one-phase three winding transformer. This was done in order to reduce the output diode from 4 to 2, thereby lowering the conduction losses. The dimension and losses were calculated automatically to be 23.43W, as shown in figure B.4.

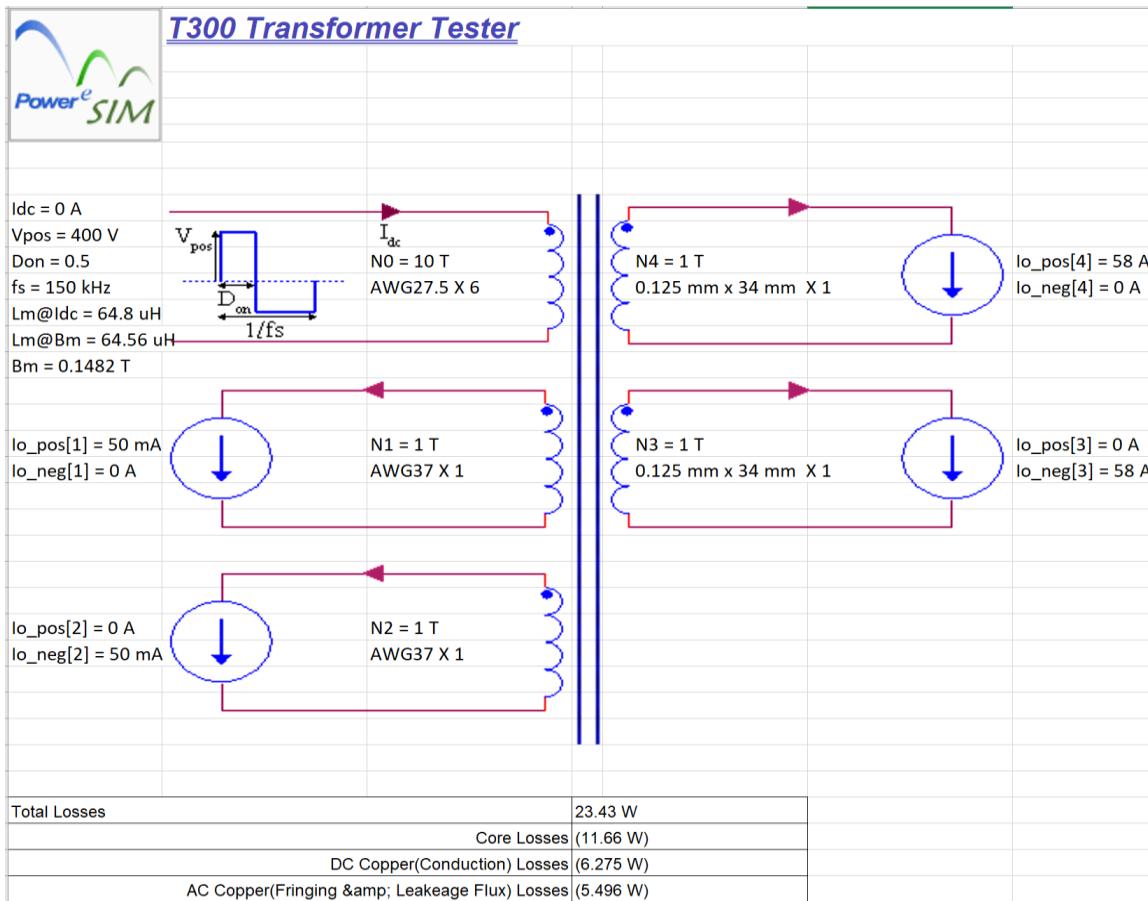


Figure B.4 Transformer losses estimation with Transformer designer in Powersim

B.1.7 Rectifier diode loss estimation

DSA120X200LB Schottky diode bridge with 120A/200V rating was selected. The loss across the diode bridge can be expressed as

$$\begin{aligned}
 P_{C.diode} &= 2\left(\frac{1}{2} \frac{P_o}{V_o} V_f + I_{diode.rms}^2 R_d\right) \\
 &= 2\left(\left(\frac{1}{2} \times \frac{3400}{58}\right) \times 0.82 + 33.94^2 \times 2.7 \text{ m}\Omega\right) = 54.29 \text{ W}
 \end{aligned} \tag{B.12}$$

B.1.8. Decoupling and output capacitor (C_b and C_o) loss estimation

3300μF/350V nichicon electrolytic capacitor with part number LNX2V332MSEF was selected for the decoupling capacitor. It has a $\tan \delta$ of 0.2 and the ESR_{Cb} is calculated from (B.13) and the capacitor RMS current ($I_{cd.rms}$) gotten from the simulation is 39.97A. The power loss is expressed by (B.14)

$$ESR_{Cb} = \frac{\tan \delta}{2\pi f_{sw} C_{Cb}} = 0.06 \text{ m}\Omega \tag{B.13}$$

$$P_{cb.loss} = I_{cb.rms}^2 ESR_{cb} = 0.1 \text{ W} \tag{B.14}$$

1800 μ F/350V nichicon electrolytic capacitor with part number LNX2V182MSEF was selected for the output capacitor C_o . ESR_{co} is calculated to be 0.12m Ω and the RMS current of the capacitor extracted from the simulation is 48A giving a power loss of 0.27W.

B.1.9 Output filter inductor (L_d) and synchronous switch loss

Kool mu material with part number 77586 was suggested by the design tool. Toroid core design was selected in the tool, giving a total loss of 1.72W. GS61008P GaN switch was selected and the total losses estimated is 25.45W.

B.1.10 Efficiency estimation

The total power loss estimated is 168.76W, and the estimated efficiency is expressed as

$$\text{Efficiency} = \frac{P_o - P_{\text{total loss}}}{P_o} = 95\% \quad (\text{B.15})$$

B.2 7KW EV Charger Power Loss Estimation

The losses in the converter are estimated using the same process of the first design case. A suitable component that is closely matched to the specification in Table 3.1 is selected. The RMS voltage and current used in the calculation was extracted from the simulation carried out.

B.2.1 Boost inductor

The chosen material is Kool Mu from Magnetics with part number 0077093A7. Toroid design was selected, consisting of 4 stacked cores, and the material permeability is 90 μ . The total loss consisting of the core and copper loss is 12.32W, therefore the two inductors (L_a , L_b) would have a loss of 24.64W.



Figure B.5 Boost PFC inductor design tool from Magnetics

B.2.2 Line rectifier MOSFET

Diode D1 and D2 are to be replaced with line rectifier MOSFETS. CoolMOS IPT65R033G7 was selected. Since each of the MOSFET would conduct for only half of the line cycle, only the conduction loss is considered. The RMS current I_{d_rms} of the diode extracted from the simulation is 21.6A and R_{Ds} of 33mΩ

$$P_{\text{LineMos.loss}} = I_{d_rms}^2 \times R_{ds} = 15.4W \quad (\text{B.16})$$

B.2.3 GaN transistor conduction and switching loss.

GS66516T 650V transistor, which has no body diode, was used to estimate the switching loss. An R_{ds} of 25mΩ was extracted from the datasheet. Therefore, the loss equation reduced to

$$\begin{aligned} P_{\text{cond}} &= P_{\text{c.mos}} = 4I_{\text{mos_rms}}^2 R_{ds} \\ &= 4 \times 26^2 \times 25 \times 10^{-3} = 67.6W \end{aligned} \quad (\text{B.17})$$

The switching losses of a GaN transistor can be estimated from (B.18)

$$\begin{aligned} P_{s_{\text{sw}}} &= 4 \left(\frac{f_{\text{sw}} V_{\text{mos_rms}} i_{\text{mos_rms}} (t_r + t_f)}{2} \right) \\ &= 4 \left(\frac{150\text{KHz} \times 305.2V \times 26(12.4\text{ns} + 22\text{ns})}{2} \right) \\ &= 81.89W \end{aligned} \quad (\text{B.18})$$

$$\begin{aligned} P_{\text{drive loss}} &= 4 \left(\frac{1}{2} C_{\text{gs}} V_{\text{gs}}^2 \right) f_{\text{sw}} \\ &= 1.94\text{mW} \end{aligned} \quad (\text{B.19})$$

The total loss across the switch in one full line cycle is expressed as

$$\begin{aligned} P_{\text{Sw.total_loss}} &= \frac{P_{\text{cond}} + P_{\text{s_sw}} + P_{\text{drive loss}}}{2} \\ &= 74.75\text{W} \end{aligned} \quad (\text{B.20})$$

B.2.4 DC – bus and resonant capacitor loss

An AC capacitor with part number C4ASMBW4200A3HJ rated $2\mu\text{F}/500\text{VAC}$ is selected. The ESR, which is $2.3\text{m}\Omega$, was extracted from the datasheet. The RMS current of C_b was extracted from the simulation and the loss expressed by (B.21)

$$P_{cb.\text{loss}} = I_{cb.\text{rms}}^2 \text{ESR}_{cb} = 27.3^2 \times 2.3\text{m}\Omega = 1.71\text{W} \quad (\text{B.21})$$

Panasonic ECWFD2JK capacitor was chosen for the resonant capacitor. It has a capacitance range of $0.27 - 0.82\mu\text{F}$ at 630V and the dissipation factor ($\tan \delta$) extracted from the datasheet is 0.1% . Therefore the ESR_{cr} is calculated from (B.22) and the loss across the resonant capacitor is calculated from (B.23)

$$\text{ESR}_{Cb} = \frac{\tan \delta}{2\pi f_{sw} C_{Cr}} = 1.89\text{m}\Omega \quad (\text{B.22})$$

$$P_{Cr.\text{loss}} = I_{r.\text{rms}}^2 \text{ESR}_{cr} = 33.4^2 \times 1.89\text{m}\Omega = 2.11\text{W} \quad (\text{B.23})$$

B.2.5 Resonant inductor loss

MPP material was also selected in this case due to the benefit discussed previously. Figure B.6 suggest MPP55439 as the best in keeping the losses and temperature as low as possible. The total loss estimated with the tool is 4.62W .

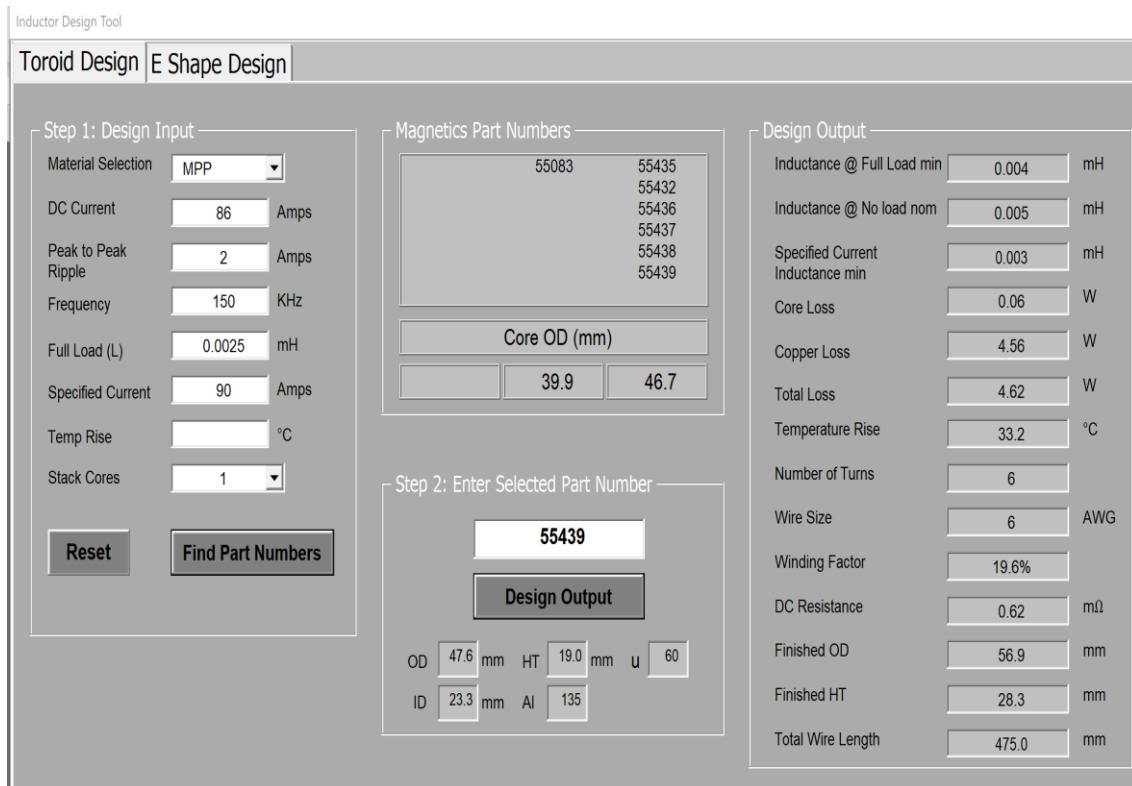


Figure B.6 Resonant inductor loss estimation using magnetics inductor design tool

B.2.6 Transformer design and loss estimation

The primary and ripple cancellation transformer was modelled in Poweresim software, and the losses were calculated automatically, shown in figure B.7 and B.8

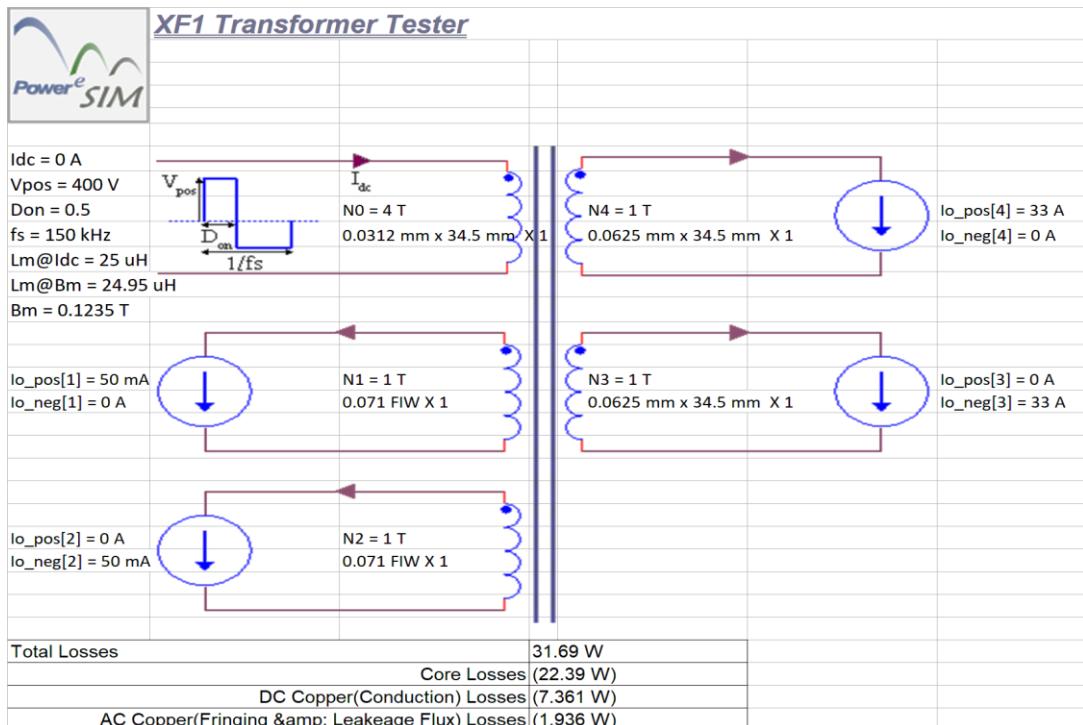


Figure B.7 Main transformer losses estimation in Poweresim

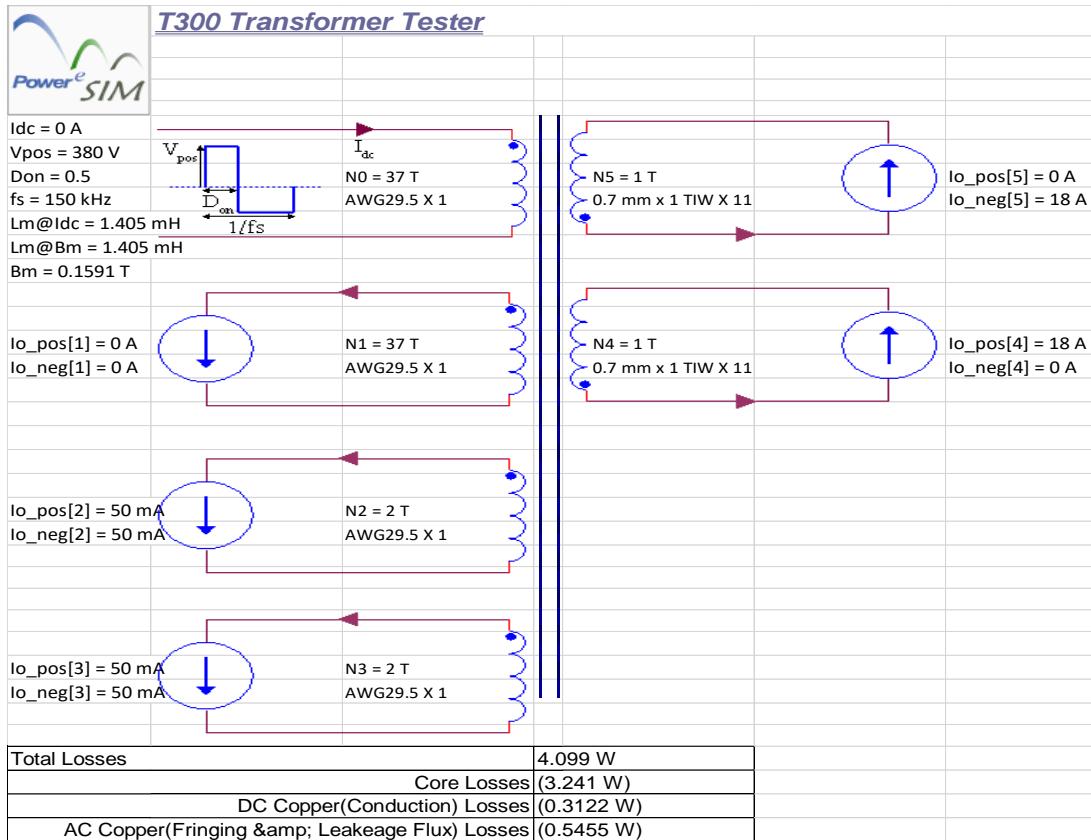


Figure B.8 PRC transformer losses estimation with Powersim

B.2.7 Rectifier diode loss estimation

KBPC3504 bridge rectifier diode with 35A/400V rating was selected. The loss across the diode bridge can be expressed as

$$\begin{aligned}
 P_{C,diode} &= 4\left(\frac{1}{2} \frac{P_o}{V_o} V_f + I_{diode_rms}^2 R_d\right) \\
 &= 4\left(\frac{1}{2} \times \frac{7000}{400} \times 1.1 + 19.4^2 \times 3.91 \text{m}\Omega\right) = 44.3 \text{W}
 \end{aligned} \tag{B.24}$$

B.2.8 Decoupling, output, and ripple storage capacitor loss estimation

The decoupling capacitor C_d and the output capacitor C_o were designed to have a capacitance of $500\mu\text{F}$. Therefore, two Vishay MKP1849, metallized Polypropylene DC-LINK capacitor, rated $500\mu\text{F}/900\text{V}$ was selected due to their very low ESR. The selected capacitor ESR is $1\text{m}\Omega$ and the total loss across C_d and C_t is expressed as

$$\begin{aligned}
 P_{Cd,Co,loss} &= I_{o,rms}^2 (ESR_{Cd} + ESR_{Co}) \\
 &= 17.5^2 \times 2\text{m}\Omega = 0.61 \text{W}
 \end{aligned} \tag{B.25}$$

The ripple cancellation capacitor with part number LNX2W122MSEF rated 450V/1200 μ F was selected. The displacement factor ($\tan \delta$) is 0.2 from the datasheet, and the ESR is calculated using (B.26) to be 0.18m Ω

$$\begin{aligned} P_{Ct.loss} &= I_{ct.rms}^2 ESR_{Ct} \\ &= 10.6^2 \times 0.18m\Omega = 19.86mW \end{aligned} \quad (\text{B.26})$$

The total power loss, therefore, is expressed by adding all the above estimated individual losses together which gives $P_{total.loss} = 203.95W$ and this gives an estimated efficiency of 97.1%.

B.2.9 Other simulation results

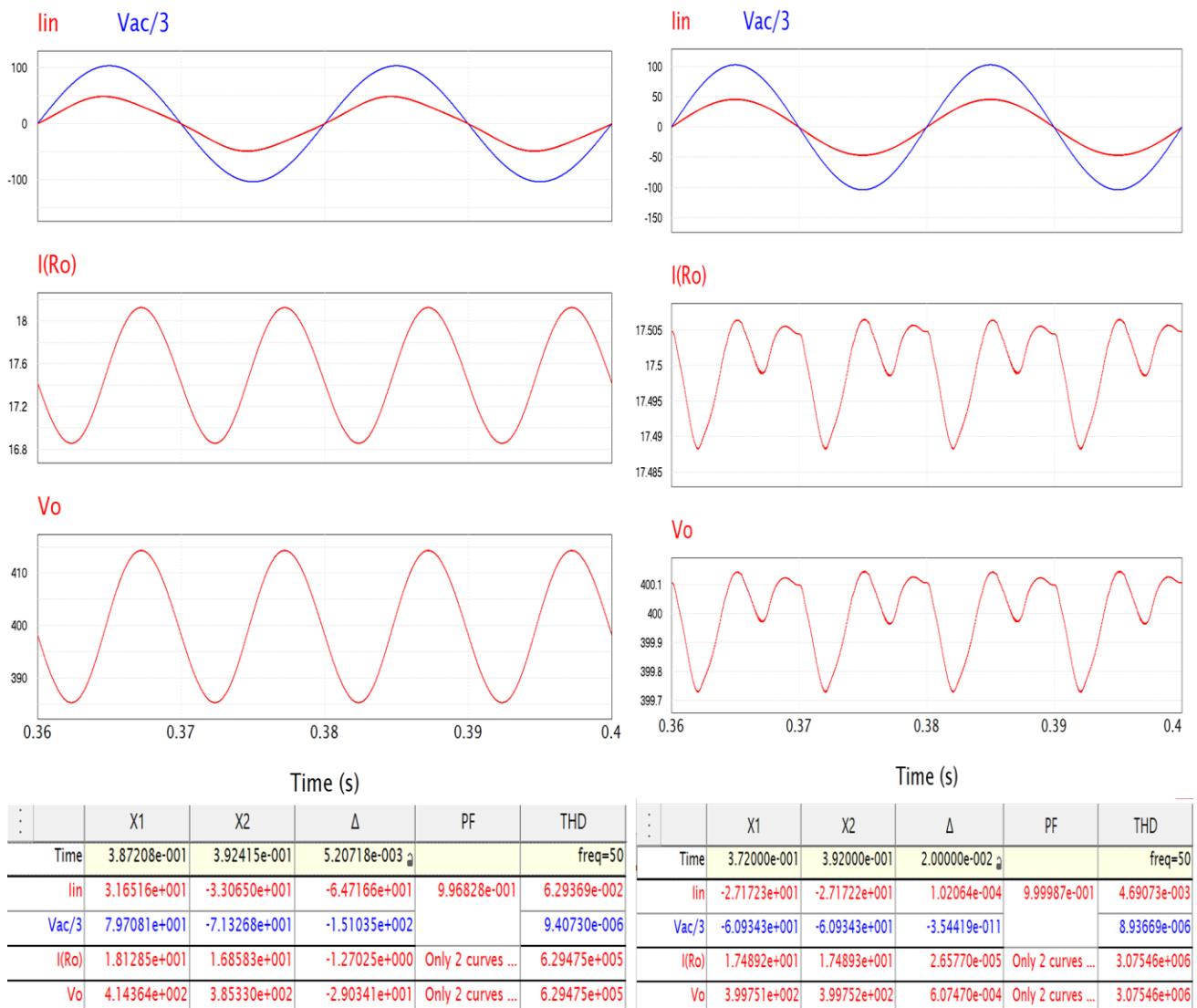


Figure B.9 Ripple cancellation THDi and PF comparison and verification plot

APPENDIX C

Simulation Model Code

LLC gain script with C code in PSIM

```

//*****
// Define The file paths, and the target simulation needs to be defined
// The script and the target simulation need to be
// saved in the same folder location
//*****
filepath = getlocal("ParamPath");
simname = "LLC_100kHz_ideal gain script.psimsch"
outpath = filepath+"outputs ideal\";

//*****
// Define input voltage, output voltage, target resonant frequency variables which are used to
// calculate Ls = Lr, Cs=Cr, and Lm
//*****
//Input variables
Vmin=400
Vnom=480
Vmax=500
//Output variables
Po=3400
Vo=80
fres=100000
// Full load impedance calculation
Ro=Vo*Vo/Po
// Multiply the converter operating frequency with fres in simulation
f_in = 1;
n = Vo/Vnom           // transformer turns
ro=Ro/(n*n)           // reflected full load output impedance to primary
percentageload=100
actualoutputload=(100/percentageload)*ro*n*n
//*****
// Testing arrays of Quality factor(Q) and magnetics ratio ratio(K) for magnetics ratio of Lm vs Ls
// Each new Q value adds N_k*N_freq simulations and each new K value add N_q*N_freq
// simulations
//*****
Q = {0.2,0.25,0.3,0.35,0.4,0.45,0.5,0.55}; // test values for Q
//ar_Q = {.4,.7};
K = {6,8,10};           // test values for K
fo = {.2,.4,.45,.47,.48, .49,.5,.52,.53,.54,.545,.548,.549,
.55,.56,.57,.58,.59,.6,.62,.65,.7,.76,.8,.9,1,1.2,1.3,1.4,1.6,1.8,2}; // test frequencies
//*****
// define loop variables which changes based on the size of the arrays above
//*****

```

```

runs_freq = sizeof(fo);
i_freq = 0;
runs_q = sizeof(Q);
i_q = 0;
runs_k = sizeof(K);
i_k = 0;
//*****
// Defining the arrays for storing the arrays
//*****
ar_gain = array(0);           //array stores the gain at each freq. for a selected Q and then reset for
                                //each new Q
ar_Qgain = array(0);          // array stores each Q vs freq. curve and each curve is a new entry in
                                //the array
ar_f_in = array(0);           // array stores the frequencies used, not used as it is the same as ar_freq
maxGain = 0;                  // array tracks the max gain for each Q and K values, and then reset for
                                //each K sweep
ar_maxGain = array(0);         //array stores results with each entry being a gain vs Q for each K.
ar_Q_K = array(0);             // array for the curves plots for each gain vs Q
//*****
// parameters test to prevent simulations from running if changes to the script needs checking
//*****
test = 0; // test variable toggle this to 1 to pre
if(test == 1){
    runs_k = 2;
    runs_q = 3;
    runs_freq = 5;
}
//*****
// The first while loops, contain three nested loops - inner loop - sweep a fixed Q and K through all
elements defined in ar_freq, middle loop - changes Q while K is fixed, outer loop - changes K
//*****
while(i_k < runs_k){
    Ka = K[i_k]; // outer K loop and K for this set of runs is defined

    while( i_q < runs_q){           // middle loop changes Q for a given K
        Qa = Q[i_q];
        Ls=(Qa*ro)/(2*pi*fres) // Defined the Ls and Cs for the Q curve
        Cs=1/(2*pi*fres*Q*ro)
        Lm=Ka*Ls

        while( i_freq<runs_freq){   // inner loop for changing frequency
            f_in = fo[i_freq];
            TimeStep = 1/(fres*f_in*100);
            TotalTime = 200/(fres*f_in);

// from above timestep is 100 points per period of control freq. Total time is 200 cycles of control
freq. and assuming steady state occurs within 35 cycles. An identification string for each simulation
run.

            outstring = "freq =" + string(f_in) +

```

```

"; Qa = " + string(Qa) +
"; Ka = " + string(Ka);
// Simulate defined below check if there is a bug present simulation output is not displayed. the array
of curves "g1" stores the simulation results

simulate(filepath+simname,outpath+"test.smv",,g1);
Graphwrite(outpath+ outstring+".smv", g1);

// compute the data points that contain the start and finish of the last 2 cycles
last_cycle_e = sizeof(g1["Vo"])-1; // end point

// start point 100 points per cycle defined by the TimeStep parameter
last_cycle_s = last_cycle_e - 200;
// copy out the last 2 cycles
cur_Vo = copy( g1["Vo"],last_cycle_s,last_cycle_s);
t = copy( g1["Time"],last_cycle_s,last_cycle_s);

avg_Vo = sum(cur_Vo)/200; // calculate the average
gain = avg_Vo/Vo;           // calculate the gain

// track if this is the max gain achieved for a given Q and K

if( gain > maxGain){

    maxGain = gain;

}

addtoarray( ar_gain, gain); // store the gain computed gain

// this is redundant and will only recreate the original freq array it is not used.

addtoarray( ar_f_in, f_in);

i_freq++;

addtoarray(ar_maxGain,maxGain); // array of maxgain as a function of Q

// store the gain as function of frequency as a curve with a unique title for each Q
addtoarray(ar_Qgain,MakeCurve("Qa=" + string(Qa), ar_gain));

//reset temp variables for next sweep
ar_gain = array(0);
i_freq = 0;
maxGain = 0;

i_q++;
// store the max gain as a function of Q as a curve with a unique title for each K

addtoarray(ar_Q_K,MakeCurve("K=" + string(K), ar_maxGain));

```

```
// plot and store the graph
plot("gain k = " + string(K), ar_freq, ar_Qgain);
Graphwrite(outpath+"1 Gain k = " + string(K)+".smv", ar_freq, ar_Qgain);

//reset temp variables for next sweep
ar_Qgain = array(0);
ar_maxGain = array(0)
i_q = 0;

i_k++;}

// plot and store the graph
plot( "Gain vs Q", ar_Q, ar_Q_K);
Graphwrite( outpath + "1 Gain vs Q", ar_Q, ar_Q_K);
```

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