Input Filter Design for Power Factor Correction Converters Operating in Discontinuous Conduction Mode

Vlad Grigore, Jorma Kyyrä

Institute of Intelligent Power Electronics
Helsinki University of Technology
P.O.Box 3000
FIN-02015 HUT, Finland

Jyri Rajamäki

Safety Technology Authority
P.O. Box. 123 (Lönnrotinkatu 37)
FIN-00181 Helsinki, Finland

Abstract: Power Factor Correction (PFC) converters operating in Discontinuous Conduction Mode (DCM) are very attractive for use in low-cost and low-power applications, due to simpler control when compared with Continuous Conduction Mode (CCM) operation. Design of the EMI input filter for DCM operation has different constraints in certain aspects, when compared with the CCM case. This paper focuses on particularities of the input filter design in the DCM case.

INTRODUCTION

In recent years requirements for power quality in power supply systems have been rising. Various international and national standards limiting the harmonic content of input current of equipment connected to the public network have come or will come into force [1]. For these reasons, producers of power supply systems have had to reduce the harmonic content of the input current of their rectifier systems by introducing a supplementary Power Factor Correction (PFC) stage.

Typical configuration of a power supply with PFC and output voltage regulation is shown in Figure 1. The PFC stage consists of a DC-DC converter whose average input current tracks a sinusoidal waveform. The Boost converter, presented in Figure 2a) is widely used for this purpose. Continuous Conduction Mode (CCM) is used for power levels exceeding few hundred watts (e.g. 300W), and the corresponding input current is shown in Figure 2b). A current loop in the control circuit is needed to make the average input current track a sinusoidal reference. For lower power, Discontinuous Conduction Mode (DCM) is attractive. Input current in DCM is shown in Figure 2c). In this operation mode the converter has inherent PFC properties, meaning that, at constant duty-cycle $D = T_{ON}/T_S$, the average input current automatically tracks to some extent the sinusoidal shape of the input voltage [2]. This is realized without the need of sensing and controlling the input current, thus simplifying control circuit. Moreover, such feature can be used to integrate the PFC stage with the output voltage regulation stage into a single-switch converter. Several integrated topologies are reported [3], [4], and [5], in which the Boost inductor is operated in DCM. This approach is deemed to be a low-cost one, since one switch and its control circuit are saved.

The PFC stage has pulsating input current, which gives EMI levels above the limits specified in [6] virtually in all practical cases. An input filter is needed to restrict EMI. At same power level, it is expected that this problem is more severe in DCM when compared with CCM, because of the larger high frequency ripple. This paper aims to provide design criteria for the input filter of a PFC stage based on Boost converter in DCM, and to compare these criteria with the CCM case. Generation of differential-mode conducted EMI is analyzed, based on the waveform of the input current.

Firstly, we describe the models used in the analysis and characterize the differential-mode EMI without an input filter.

Secondly, we analyze the requirements for the input filter: attenuation level to meet regulatory specifications, low input displacement angle between filter input voltage and current, minimum interaction with the PFC stage and system stability.

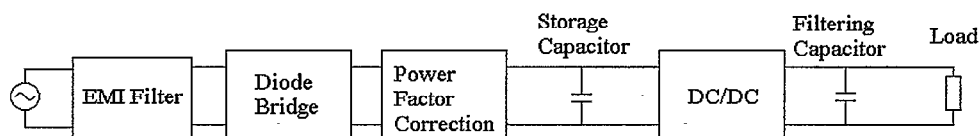Finally, conclusions are presented.

Figure 1. Typical configuration of a power supply with PFC and output voltage regulation.
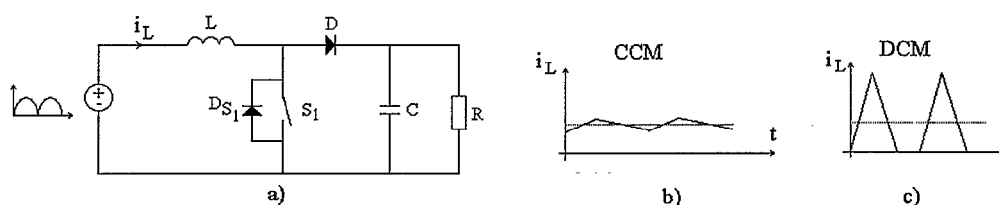

Figure 2. Boost converter for PFC: a) Schematic; b) Input current in CCM; c) Input current in DCM.

CHARACTERIZATION OF CONDUCTED NOISE GENERATION

The pulsating input current of a switching converter generates differential-mode EMI [7]. If the PFC stage is omitted from the configuration presented in Figure 1, then differential-mode EMI generated by the output voltage regulation stage is less perturbing. Firstly, the differential-mode EMI flows through the storage capacitor, which has very low impedance at frequencies of interest, compared with the line impedance. Secondly, due to the peak detection rectification, the rectifier bridge conducts only during a small part of the line-cycle. Thus the differential noise source is connected to the network only during these intervals, reducing its effect. An interesting approach based on this idea is presented in [8]. However, when the PFC stage is used, the differential noise source is connected to the line during entire line-cycle. All the high-frequency current flows towards the line, and causes a voltage drop on the high-frequency impedance of the line, which can be several tens to hundreds of ohms [9].

Common-mode EMI components originate as a result of secondary, parasitic effects [7]. Parasitic capacitances between points of the circuit where high dv/dt is present are the main cause of common-mode EMI.

The EMI level obtained by simulation is compared with composite IEC (CISPR), FCC and VDE conducted EMI limits, which are presented in Figure 3. Although limits and simulation results are presented over the 10kHz-30MHz interval, we have to take into consideration that in reality the dominant noise is differential-mode below 2MHz and common-mode above 2MHz [10]. Differential mode noise above 2MHz is mostly filtered by circuit layout capacitances and inductances.
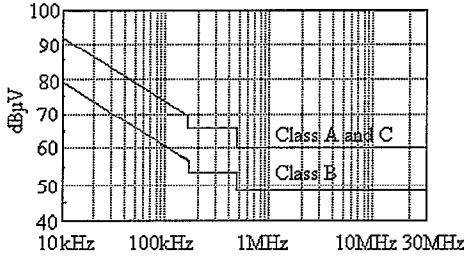

Figure 3. Composite IEC (CISPR), FCC and VDE conducted EMI limits.

This paper analyses only differential-mode EMI generation due to the pulsating input current. Parasitic elements are not taken into account and the common-mode EMI is not analyzed. Hence, only results below 2MHz should be taken into account.

SPICE simulation was used to perform the analysis. The model of a 50Ω/50μH Line Impedance Stabilization Network (LISN) was included in the simulation, as shown in Figure 4.
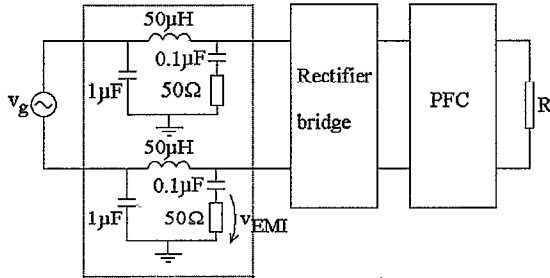

Figure 4. LISN model included in the SPICE model.

The Boost converter operating modes that are analyzed are presented next. Negligible losses, 100W input power, rectified sinusoidal input voltage $v_i = 220\sqrt{2}|\sin 100\pi\, t|$ and 380Vdc output voltage are considered for all three cases. Thus, the load resistance is $R = 1444\Omega$. Output capacitor is $C = 470\mu F$. Switching frequency f_S, on-time t_{ON} and inductor value L are chosen according to each particular case.

CCM with average current control

This operation mode was considered for comparison purposes. Reference [11] presents a more detailed analysis of CCM. Switching frequency is fixed $f_S = 100\text{kHz}$ and inductance is $L = 4\text{mH}$. A model for an average current mode controller was used. Duty-cycle $d = t_{ON}/T_S$ is controlled in order to make input current track a sinusoidal reference. Input current is shown in Figure 5a). The EMI level is shown in Figure 5b) and is well above the limits. The EMI voltage was calculated applying FFT to the v_{EMI} voltage across one of the 50Ω resistors in LISN, as shown in Figure 4.

DCM, constant on-time and constant switching frequency

In this operating mode the switching frequency is fixed. In presented case, $f_S = 100\text{kHz}$. The duty-cycle is controlled in a slow loop (cut-off frequency several times lower than 100Hz) in order to keep output voltage constant when the RMS input voltage changes. Thus, the duty-cycle can be considered constant during half line-cycle. Average input current doesn't track perfectly a sinusoid [2]. The inductance L and duty-cycle $D = T_{ON}/T_S$ are calculated to obtain the desired output power and to ensure operation in DCM over entire line-cycle. In the presented case, $L = 305\mu H$ and $D = 0.18$. Input current is shown in Figure 5c), with zoomed parts at peak line voltage and at lower line voltage. The peak of the current follows a sinusoid, switching frequency and rise time are constant but fall time is not constant, over half line-cycle. EMI level is shown in Figure 5d). It is about 20dBμV above the CCM case, with same input power.

DCM, constant on-time and variable switching frequency

In this operating mode the switch is turned-on for a fixed time T_{ON} and the inductor current starts to increase. After T_{ON} the switch is turned-off and the current decreases. When inductor current reaches zero, the switch is turned-on again. The switching frequency varies over line cycle as:

$$f_S = \frac{v_o - v_i}{v_o} \frac{1}{T_{ON}},\qquad\qquad (1)$$

where V_i and V_o are the input and output voltages, considered constant over a switching cycle. Average input current tracks a sinusoid, at the expense of variable switching frequency. In the analyzed case $T_{ON} = 5\mu s$. Thus, the switching frequency is $f_S = 200\text{kHz}$ at line zero crossings ($V_i = 0, V_o = 380\text{V}$) and $f_S = 36.8\text{kHz}$ at peak line ($V_i = 310\text{V}, V_o = 380\text{V}$). The inductance is $L = 1.21\text{mH}$, in order to obtain the desired output power. The peak of the current follows a sinusoid, rise time is constant but fall time and switching frequency are not constant, over half line-cycle [12]. Input current is shown in Figure 5e) and EMI level in Figure 5f). EMI level is slightly lower than in previous cases, but it extends to lower frequencies, also.
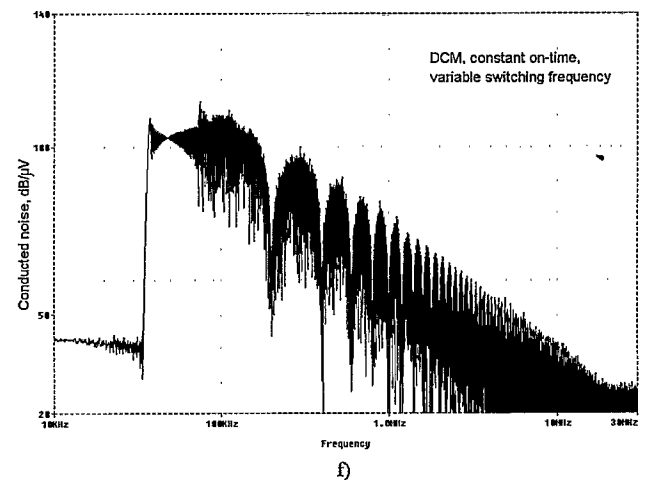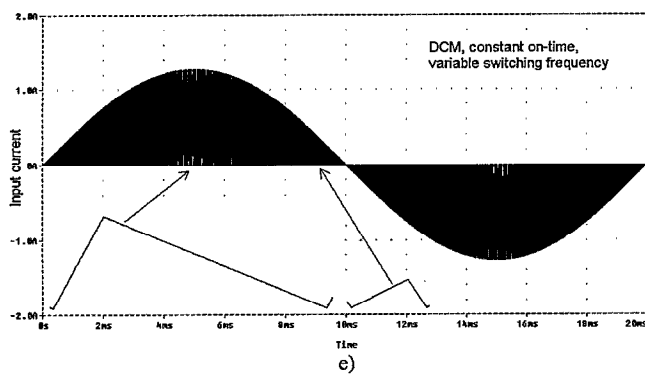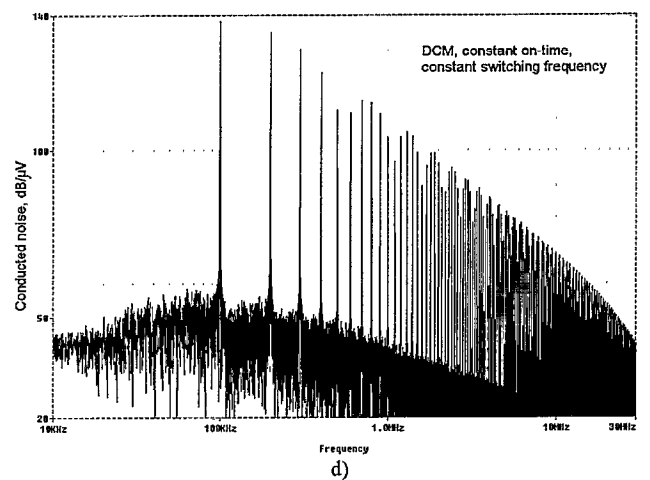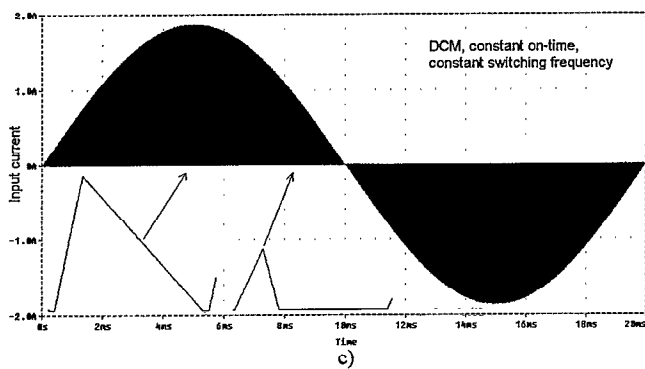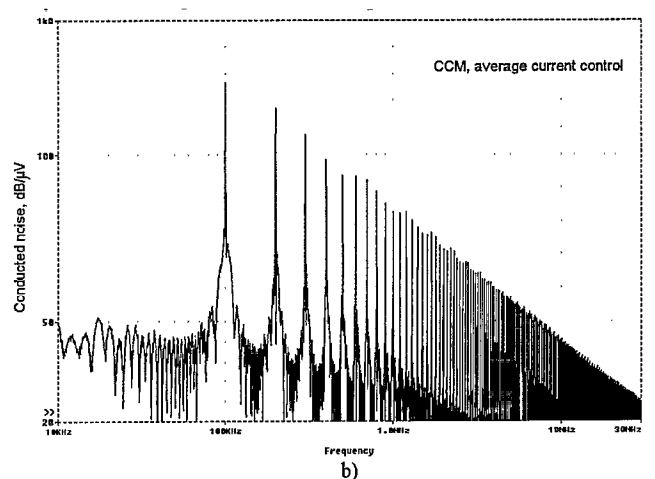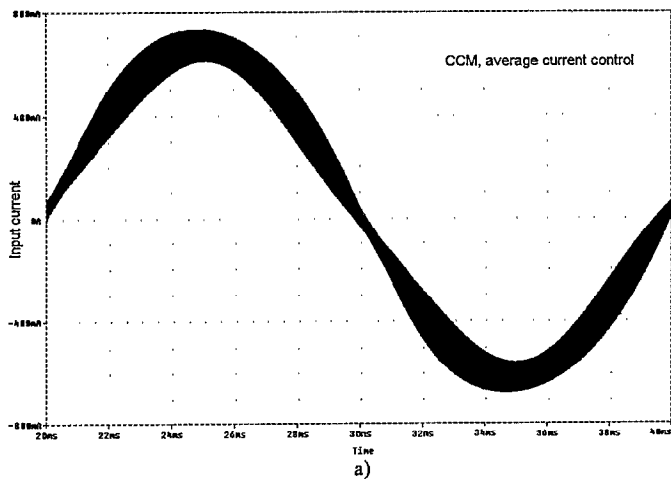
Figure 5. Simulation results.

CCM with average current control: a) Input current, b) EMI level;
DCM with constant on-time, constant switching frequency: c) Input current, d) EMI level;
DCM with constant on-time, variable switching frequency: e) Input current, f) EMI level.

INPUT FILTER DESIGN CRITERIA

The requirements for the input filter are: attenuation level to meet regulatory specifications, low input displacement angle between filter input voltage and current, minimum interaction with the PFC stage and system stability. The problem is studied in [13] for PFC stage based on Boost converter in CCM. Reference [14] addresses DCM case in a more general frame, related to the design of high power factor rectifier based on flyback converter.

REQUIRED DIFFERENTIAL-MODE ATTENUATION LEVEL

Based on differential-mode EMI level obtained for the analyzed converter we can determine the necessary differential-mode attenuation level to meet regulatory specifications. From this point of view, DCM and CCM cases are similar. The difference consists in the fact that DCM usually requires a higher attenuation when compared to CCM, for the same power level. For the LC filter shown in Figure 6, the product $L_f C_f$ is given by the required attenuation level at switching frequency. Since L_f should be small in order to minimize the size of the filter, then C_f should be large to obtain desired $L_f C_f$ product. Thus, the attenuation level gives the lower limit of the value that C_f can take.
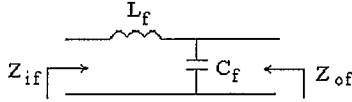

Figure 6. LC input filter.

INPUT CURRENT DISPLACEMENT ANGLE

The purpose of the PFC stage is to obtain a good power factor, so the EMI filter should not introduce distortion of the input current at line-frequency. This means that the input impedance Z_{if} should show low phase shift at line-frequency, which for the filter shown in Figure 6, imposes an upper limit on C_f. The same design constraint is, of course, valid for CCM case.

STABILITY

The equivalent circuit of the input filter - PFC stage interconnection is presented in Figure 7. If H_F is the filter attenuation, then we obtain:

$$\frac{v_g}{v_i} = \frac{H_F}{1 + \dfrac{Z_{of}}{Z_{ic}}} = \frac{H_F}{1 + T_F}, \tag{2}$$

where $T_F = Z_{of}/Z_{ic}$. Generally speaking, the interaction between output impedance of the filter and input impedance of the converter should be minimized. This is obtained if $|Z_{of}| \ll |Z_{ic}|$. It is also well
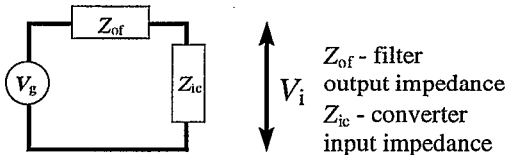

Z_{of} - filter output impedance
Z_{ic} - converter input impedance

Figure 7. Input filter – PFC stage interconnection.

know that stability problems may appear in CCM [13], [15]-[17], because T_F doesn't satisfy Nyquist stability criterion due to the resonance peaking of the filter output impedance.

In view of these problems, we study the input impedance of the Boost converter operating in DCM.

We need a time-invariant circuit in order to calculate the input impedance. The time-invariant model can be obtained using an averaging method. Available averaged models for PFC circuits in DCM [2], [14], [18], are obtained by averaging signals over half line-cycle $T_{line}/2$. Hence, they are low-frequency models, valid for frequencies lower than the line frequency, and were developed for design of the output voltage regulation loop. The resonant frequency of the input filter is usually decades above the line-frequency. Therefore, we should have a PFC converter model valid at those frequencies. We can obtain such a model by averaging signals over one switching cycle. After that we can calculate the input impedance of the converter using the quasi-static approach mentioned in [2]. A local analysis is made, considering the input voltage in a particular point of the sinusoidal input, as illustrated in Figure 8.
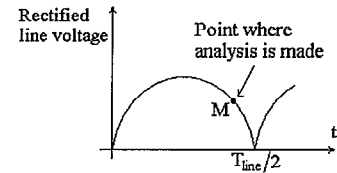

Figure 8. Local analysis in point M.

We determine the average model of the converter, we linearize it in point M and we calculate the input impedance. Converter behavior over entire line cycle can be checked repeating the analysis for several points. The frequencies where we want to calculate the input impedance are above the control loop gain crossover frequency, so we can neglect the effect of an eventual loop for controlling the output voltage.

In the following subsections we present input impedance calculations for the two DCM cases we analyze.

DCM, constant on-time, constant switching frequency

Input current of Boost converter in this case is shown in Figure 9, for one switching cycle T_S. We consider that the filtering capacitor of the converter is large enough so that output voltage v_0 can be considered constant. Also, the variation of the line voltage v_i over one switching cycle is very small, so we can approximate it as constant. Consequently, the analysis is similar to that of a DC-DC converter operating with input voltage $v_i = V_i + \hat{v}_i$ and output voltage $v_0 = V_0 + \hat{v}_0$. V_i is the DC component of input voltage v_i
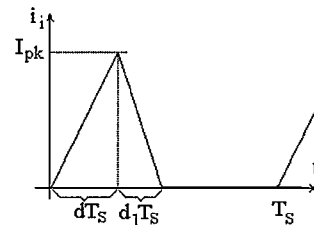

Figure 9. Input current in DCM, constant on-time and constant switching frequency.

and is equal to the line voltage at point M, where analysis is made. V_0 is the DC component of output voltage v_0 and we will consider it known, for now. $\hat{v}_i$ and $\hat{v}_0$ are small perturbations around DC operating point.

When switch S_1 is turned-on (see Figure 1a), voltage v_i is applied across inductor L, so the input current i_i rises linearly. The on-time is constant $T_{ON} = DT_S$. Hence, the peak current can be calculated as:

$$I_{pk} = \frac{v_i \cdot DT_S}{L} .$$ (3)

From the volt-seconds balance for inductor L, we obtain that:

$$v_i D = (v_0 - v_i) d_1 .$$ (4)

The input current, averaged over one switching cycle T_S, is:

$$\bar{i}_i = \frac{I_{pk} \cdot (D + d_1)}{2} .$$ (5)

From (3), (4) and (5) we obtain:

$$\bar{i}_i = \frac{D^2 T_S}{2L} \frac{v_0 v_i}{v_0 - v_i} = \frac{1}{R_D} \frac{v_0 v_i}{v_0 - v_i} ,$$ (6)

where the following notation is made:

$$R_D = \frac{2L}{D^2 T_S} .$$ (7)

An average input resistance can also be calculated from (6):

$$\bar{r}_i = R_D \frac{v_0 - v_i}{v_0} .$$ (8)

We can also consider the balance of instantaneous input and output powers:

$$v_i \bar{i}_i = v_0 \bar{i}_0 .$$ (9)

Equations (6) and (9) can be translated into the averaged model presented in Figure 10, where:

$$\bar{i}_0 = \bar{i}_R + \bar{i}_C ,$$ (10)

$$v_0 = \bar{i}_R \cdot R .$$ (11)

However, the model described by (6), (9), (10) and (11) is not in stationary state, because the DC component of the current through C is not zero:

$$\bar{I}_C \neq 0 .$$ (12)

Indeed, when the converter operates as PFC, capacitor C accumulates energy during intervals of the line cycle where the available instantaneous power is larger than the instantaneous power drawn by load, and releases it during the other times. Model in Figure 10 can
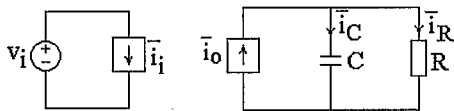

Figure 10. Averaged model, non-stationary state.

be modified into an equivalent stationary state model, which is presented in Figure 11.
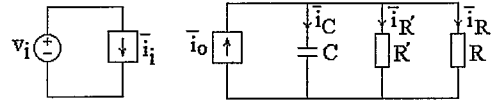

Figure 11. Averaged model, stationary state.

Resistance R' in Figure 11 accounts for the DC current flowing through C in the model presented in Figure 10. We obtain that:

$$\bar{i}_0 = \bar{i}_R + \bar{i}_{R'} + \bar{i}_C ,$$ (13)

$$v_0 = \bar{i}_{R'} \cdot R' .$$ (14)

Now,

$$\bar{I}_0 = \bar{I}_R + \bar{I}_{R'} ,$$ (15)

$$\bar{I}_C = 0 .$$ (16)

Considering DC components in (6), (9), (11), (13) and (14), we obtain the equivalent resistance

$$R_e = R \| R' = R_D \frac{V_0 (V_0 - V_i)}{V_i^2} .$$ (17)

After this step, R and R' are replaced by R_e in the model shown in Figure 11, equations describing it are linearized and Laplace transformation is applied. This procedure is well-known [2] and it will not be explained further.

The input impedance is found to be:

$$Z_i(s) = M \frac{1 + \dfrac{s}{\omega_Z}}{1 + \dfrac{s}{\omega_P}} ,$$ (18)

where

$$M = R_D \frac{V_0 - V_i}{V_0} ,$$ (19)

$$\omega_Z = \frac{1}{R_D C} \frac{V_i^2 (2V_0 - V_i)}{V_0 (V_0 - V_i)^2} ,$$ (20)

$$\omega_P = \frac{1}{R_D C} \frac{V_i^2 (2V_0 - V_i)}{V_0^2 (V_0 - V_i)} .$$ (21)

The modulus and phase characteristics for the chosen example ($L = 305\mu H$, $C = 470\mu F$, $D = 0.18$, $T_S = 10\mu s$, $V_0 = 380V$, $P = 100W$) are presented in Figure 12, for three points of the line voltage: $V_i = 50V$, $V_i = 150V$ and peak line $V_i = 310V$. As we can see from the equation (18), illustrated by Figure 12, no phase shift occurs starting from a low frequency (e.g. 100Hz in the analyzed case). This frequency is primarily determined by R_D and C. Thus, the input impedance Z_{ic} is resistive at frequencies where resonant peaking of the filter output impedance occurs.
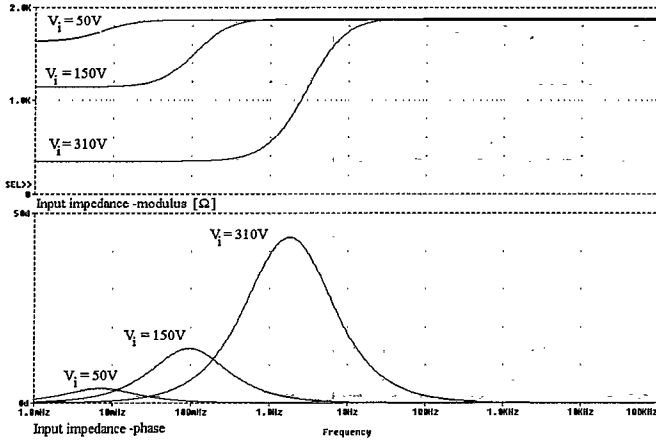
Figure 12. Converter input impedance.

Hence, there is no supplementary phase shift that could make so that Nyquist criterion for $T_F = Z_{of}/Z_{ic}$ is not satisfied in equation (2). Hence, in this case we don't have the problem of possible instability due to interaction with the input filter.

However, $|Z_{of}| \ll |Z_{ic}|$ is still a condition to be fulfilled, in order to minimize the effect of input filter on operation of the converter. Considering the LC filter in Figure 6, this condition means that the minimum value that C_f can take is limited. The presented model gives the possibility to check this condition.

In the beginning of this subsection we considered that the output voltage V_0 is known. It can be obtained by equating the input and output energies of the converter, calculated over half line-cycle.

$$\int_0^{T_{line}/2} v_i \bar{i}_i dt = \frac{V_0^2}{R} \tag{22}$$

where $v_i = V_{i,rms}\sqrt{2}\sin\omega_{line}t$ and $\bar{i}_i$ is expressed by (6).

DCM, constant on-time, constant switching frequency

It is straightforward to show that the input impedance is purely resistive in this case and equal to the average input resistance:

$$Z_i(s) = \bar{r}_i = \frac{2L}{T_{ON}}. \tag{23}$$

Unlike previous case, the average input resistance is constant over the line cycle. Also in this case, the condition $|Z_{of}| \ll |Z_{ic}|$ should be checked.

CONCLUSIONS

Input filter design for PFC based on DCM Boost converter is similar in many respects with CCM case. Required differential-mode attenuation is usually higher in DCM. A low input current displacement at line-frequency must be ensured in order to obtain good power factor and output filter impedance should be much lower than input impedance of the converter to minimize interaction between filter and converter. Unlike CCM, in DCM there is no stability problem due to interaction of input filter with PFC stage.

REFERENCES

[1] IEC standard 1000, part 3, section 2: *Limits for harmonic current emissions (equipment input current$\leq$ 16A per phase)*, 1995.

[2] R. W. Erickson, *Fundamentals of power electronics*, New York: Chapman & Hall, 1997.

[3] M. Madigan, R. Erickson, E. Ismail, "Integrated high quality rectifier-regulators", in *IEEE Power Electronics Specialists Conf., 1992 Rec.*, pp. 1043-1051.

[4] L. Huber, M. Jovanovic, "Single-stage, single switch, isolated power supply technique with input-current shaping and fast output-voltage regulation for universal input-voltage-range applications', in *IEEE Applied Power Electronics Conf. Proc. 1997*, pp.272-280.

[5] J. Qian, "Advanced single-stage PFC techniques", Ph. D. dissertation, Virginia Polytechnic Institute and state University, Blacksburg, VA, 1997.

[6] CISPR 16: *Specification for radio disturbance and immunity measuring apparatus and methods.*

[7] L. Tihanyi, *Electromagnetic compatibility in power electronics*, Sarasota, Florida: J. K. Eckert & Co, Inc., 1995.

[8] M. Albach, "How to avoid filters in off-line power supplies", in *European Conference on Power Electronics and Applications, Conf. Proc. 1993*, pp. 52-57.

[9] R. Redl, "Power electronics and electromagnetic compatibility", in *IEEE Power Electronics Specialists Conf., 1996 Rec.*, pp. 15-21.

[10] M. K. W. Wu, C. K. Tse, "A review of EMI problems in switch mode power supply design", *Journal of Electrical and Electronics Engineering, Australia*, vol. 16, no. 3&4, pp.193-204.

[11] J. Mahdavi, M. Tabandeh, A. K. Shahriari, "Comparison of conducted RFI emission from different unity power factor AC/DC converters", in *IEEE Power Electronics Specialists Conf., 1996 Rec.*, pp. 1979-1985.

[12] S. Ahmed, "Controlled on-time power factor correction circuit with input filter", M. Sc. thesis, Virginia Polytechnic Institute and state University, Blacksburg, VA, 1990.

[13] V. Vlatkovic, D. Borojevic, F. C. Lee, "Input filter design for power factor correction circuits", *IEEE Trans. on Power Electronics*, vol. 11, no. 1, pp. 199-205, Jan. 1996.

[14] J. S. Glaser, A. F. Witulski, "Design issues for high power factor AC-DC converters systems", in *IEEE Power Electronics Specialists Conf., 1995 Rec.*, pp. 542-548.

[15] Y. Jang, R. W. Erickson, "Physical origins of input filter oscillations in current programmed converters", *IEEE Trans. on Power Electronics*, vol. 7., no. 4, pp. 725-733, Oct. 1992.

[16] R. Redl, A. S. Kislovski, "Source impedance and current-control loop interaction in high-frequency power-factor converters", in *IEEE Power Electronics Specialists Conf., 1992 Rec.*, pp. 483-488.

[17] G. Spiazzi, L. Rossetto, J. Pomilio, "Analysis of EMI filter induced instabilities in Boost power factor preregulators", in *IEEE Power Electronics Specialists Conf. 1998 Rec.*, pp.1048-1053.

[18] R. B. Ridley, "Average small signal analysis of the Boost Power Factor Correction Circuit", in *Virginia Power Electronics Center Seminar Proceedings,* 1989.