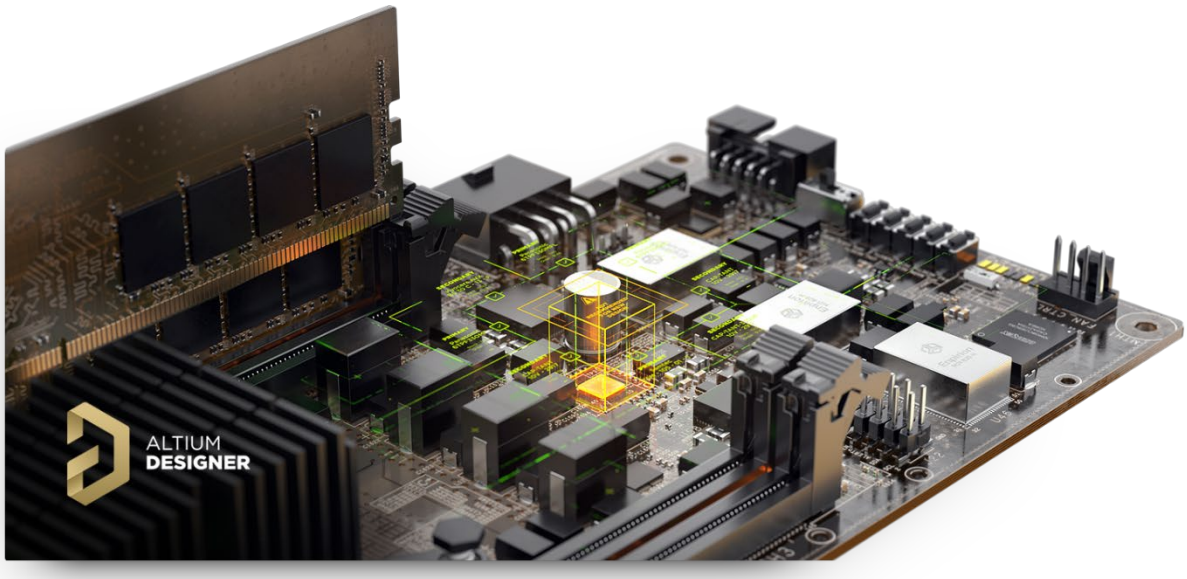

Altium Designer

Advanced Course

Module: Clearance Checking in 3D

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Clearance Checking in 3D

1.1 Purpose

In this exercise, the supplied design has 3D bodies attached to most of the components. You will be working with the Xilinx Spartan-IIE FPGA (U1) and the 16-character two-line LCD display (LCD1) to investigate the interaction of the component 3D bodies in clearance checking and experiment with the Component Clearance rule constraints.

If a 3D Mouse / Space Navigator

is available feel free to use the 3D Mouse in the Altium Designer 3D environment.

1.2 Shortcuts

Shortcuts when working with Clearance Checking in 3D

F1:	Help – Shortcut Key List
2:	2D Mode
3:	3D Mode
L:	View Configuration Panel
R:	Component Placement - **c**hange Pushing Mode

In 3D Mode

8:	Isometric View
0:	Top View

SHIFT + Right Mouse Button: Navigation Ball / Orb to rotate the 3D View

1.3 Preparation

1. **Close all existing projects and documents.**
2. Open the `Clearance Checking in 3D.PrjPCB` project found in its respective folder of the Advanced Training.

1.4 Positioning Components

1.4.1 Viewing the Component Bodies in 3D

3. Open the PCB `SL1 Xilinx Spartan-Component Clearance.PcbDoc.`
4. View the PCB design in 3D, access the command **View » 3D Layout Mode** or use the shortcut key **3** on the alpha keyboard.
5. Press the **8** key to rotate the board to an isometric view.

6. Press and hold the **Shift** key. A golden Navigation ball will appear allowing us to move the board in 3D, Figure 1.
7. Keeping the **Shift** key held down, press and hold the **Right Mouse Button**. With both buttons held down, move the mouse to rotate the PCB.

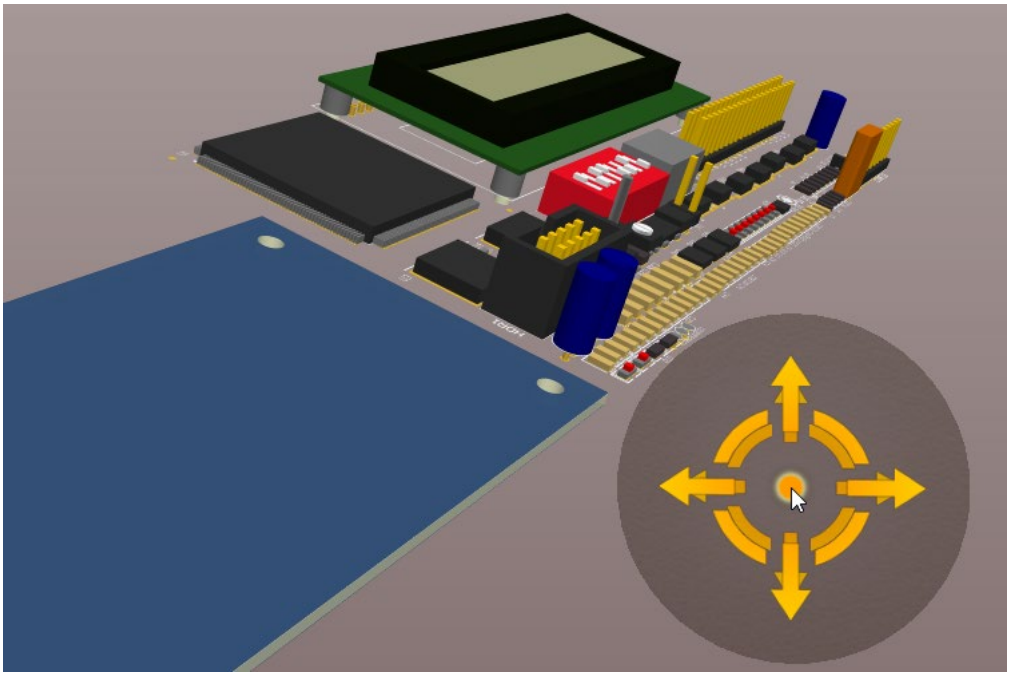

Figure 1. Navigation Orb used to navigate in 3 dimensions

Orient the PCB so you can see the clearance between the bottom of the LCD display (LCD1) and the top of the FPGA (U1).

8. Press the **0** (zero) key on the alpha keyboard to rotate the PCB to a facing surface.
9. Switch the view back to 2D mode: **View » 2D Layout Mode** or use the shortcut key **2** on the alpha keyboard.
10. In the **Preferences - PCB Editor - General:**
    a) Verify the **Snap To Center** option is enabled, and the **Smart Component Snap** is disabled. This configuration will snap the mouse cursor to a component's reference point. The **Smart Component Snap** will snap the cursor to the nearest hotspot object of the component when left clicking and holding.
    b) Ensure the **Online DRC** is enabled, the option is located just above the Object Snap Options.
    c) Click **OK** to close the *Preferences.*
11. To make Component Reference points visible:
    a) Press **L** to open the *View Configuration* panel. If opening for the first time, it may need docking.
    b) In the *Layers & Colors* Tab, scroll down to the *System Colors* section.
    c) Ensure the Visibility icon  next to the **Component Reference Point** is enabled.
12. To position the LCD display component:
    a) **Left Mouse Click** and hold on the component `LCD1` and drag it on your cursor.
    b) With the Left Mouse still pressed and the component on your cursor type **J-L** on your keyboard (shortcut for Jump To Location).
    c) Release the left mouse button when the *Jump To Location* dialog opens and enter the values X = `53mm` Y = `43mm`.

d) Once you have entered the X and Y values, press the **Enter** key twice. The first enter press will move the component to the location, the second enter will anchor the component at this location. It is important that you do not move the mouse between Enter presses.

13. Next, we will position the FPGA `U1` under the body of the LCD display at location X = `85mm` and Y = `21mm`, using the *Properties* panel.
    a) Ensure the **Double Click Runs Interactive Properties** option is enabled in the *General* section of the PCB Editor *Preferences*.
    b) Select `U1` using left mouse click if the *Properties* panel is already open. Double left mouse click if it is not, and it will pop up (it may need to be docked after it opens).
    c) Enter the new coordinates in the *Location* section of the *General* tab and press **Enter**.
14. Since there is enough vertical clearance, this does not generate any DRC violations, as shown back in 3D mode in Figure 2 (switching to 3D mode not required yet).

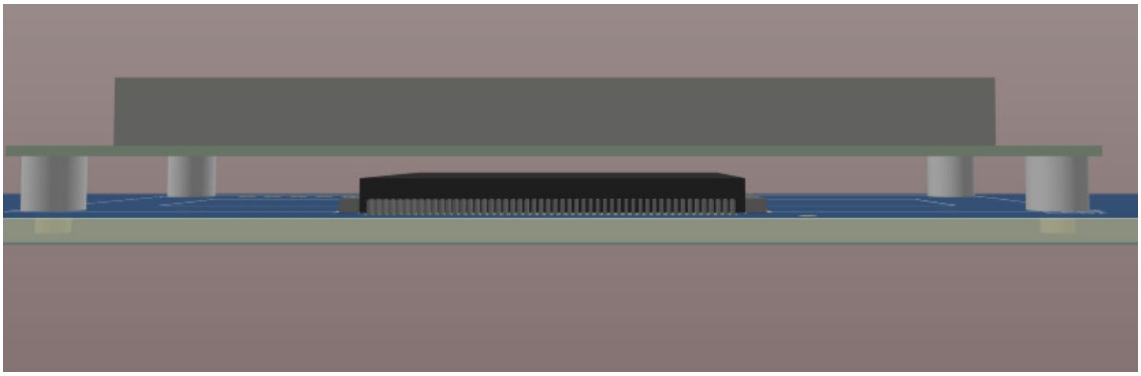

Figure 2 : Sufficient vertical clearance

15. Move the FPGA to a new location using the Move By… Selection command:
    a) Click on `U1` to select it.
    b) Select **Edit » Move » Move Selection by X, Y...** and enter *X Offset:* `-2mm` and *Y Offset:* `5.5mm`.
    c) Click **OK**. This should cause the pads of the LCD display and the FPGA to violate and will highlight in the online DRC violation color, Figure 3. This is an Electrical Clearance rule violation and not a Component Clearance rule violation.

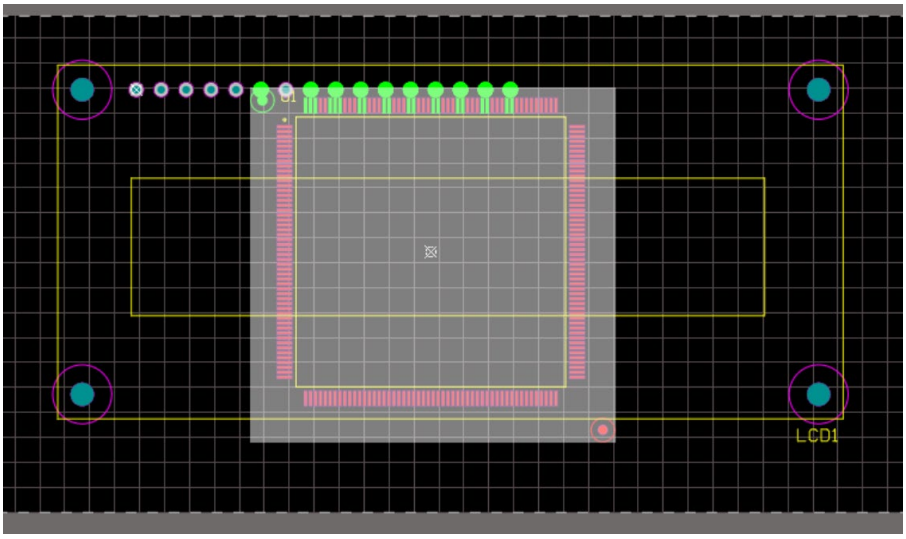

Figure 3: Pads violating

1.4.2 **Component Body Clearance**

16. Switch to the 3D view by pressing the **3** key.
17. Open the *PCB* panel *(if not already open)* from the **Panels** button or with **View » Panels » PCB**.
    a) Set the scope of the *PCB* panel (using the drop-down arrow at the top) to **3D Models**.
    b) In the *Component Classes* section, select the **<All Components>** class.
    c) Scroll down through the components in the center area of the *PCB* panel to the LCD display, `LCD1`, and select it as shown in Figure 4.

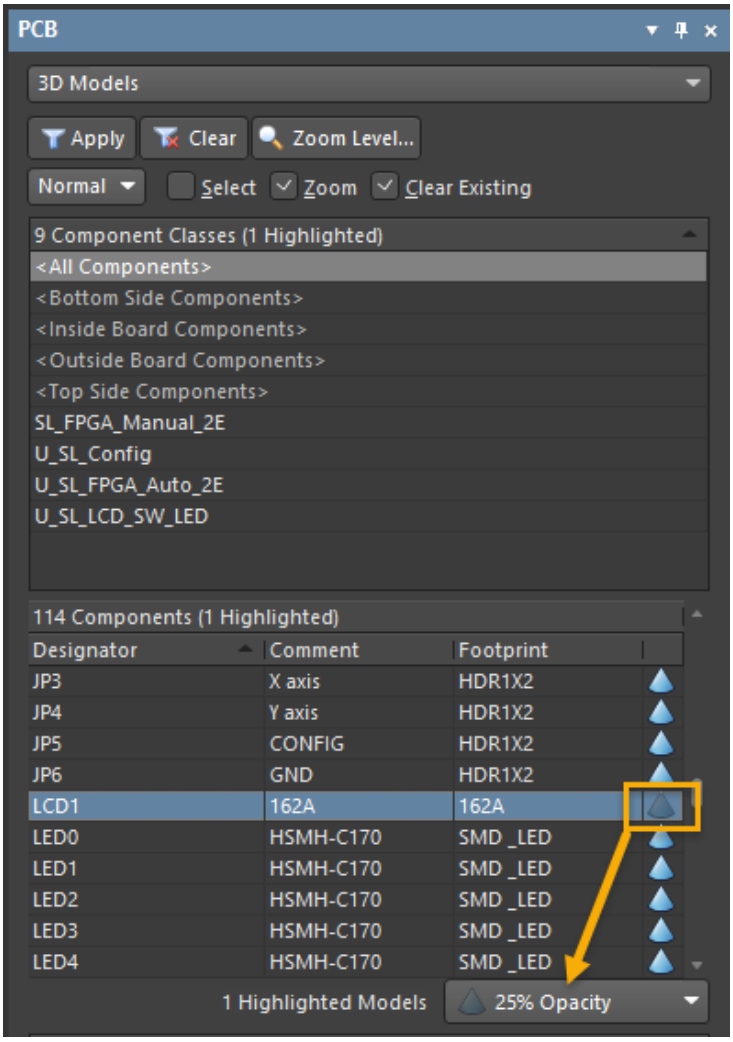

Figure 4. Locate LCD1 using the PCB panel

    d) Click on the blue cone shaped ICON to the right of `LCD1` to toggle the opacity of the LCD 3D body between Solid 100%, Hide, 75%, 50%, and 25%. Set the opacity of the LCD display to 25% so that you are able to see through it and view the FPGA underneath. (Manually changing the Highlighted Models drop-down allows setting the opacity for the selected components).
18. Select `U1` and move it to the left until it highlights in the DRC violation color. This is the Component Clearance rule violation.
    If `U1` is jumping outside the Board, or the `LCD1` is pushed change the Component Pushing mode by pressing **R** on the keyboard
19. Move `U1` back to the right until the violation is removed.

1.4.3 **Component Clearance Rules**

20. Open the *PCB Rules and Constraints Editor* by accessing the command **Design » Rules**.
21. In the pane on the left side of the dialog browse to the *Placement - Component Clearance* branch and select the rule `ComponentClearance_LCD_U1`, Figure 5.
22. Note the scope of the two queries **Component - LCD1** and **Component - U1**. This scopes the rule to a Component Clearance specifically between `LCD1` and `U1`.

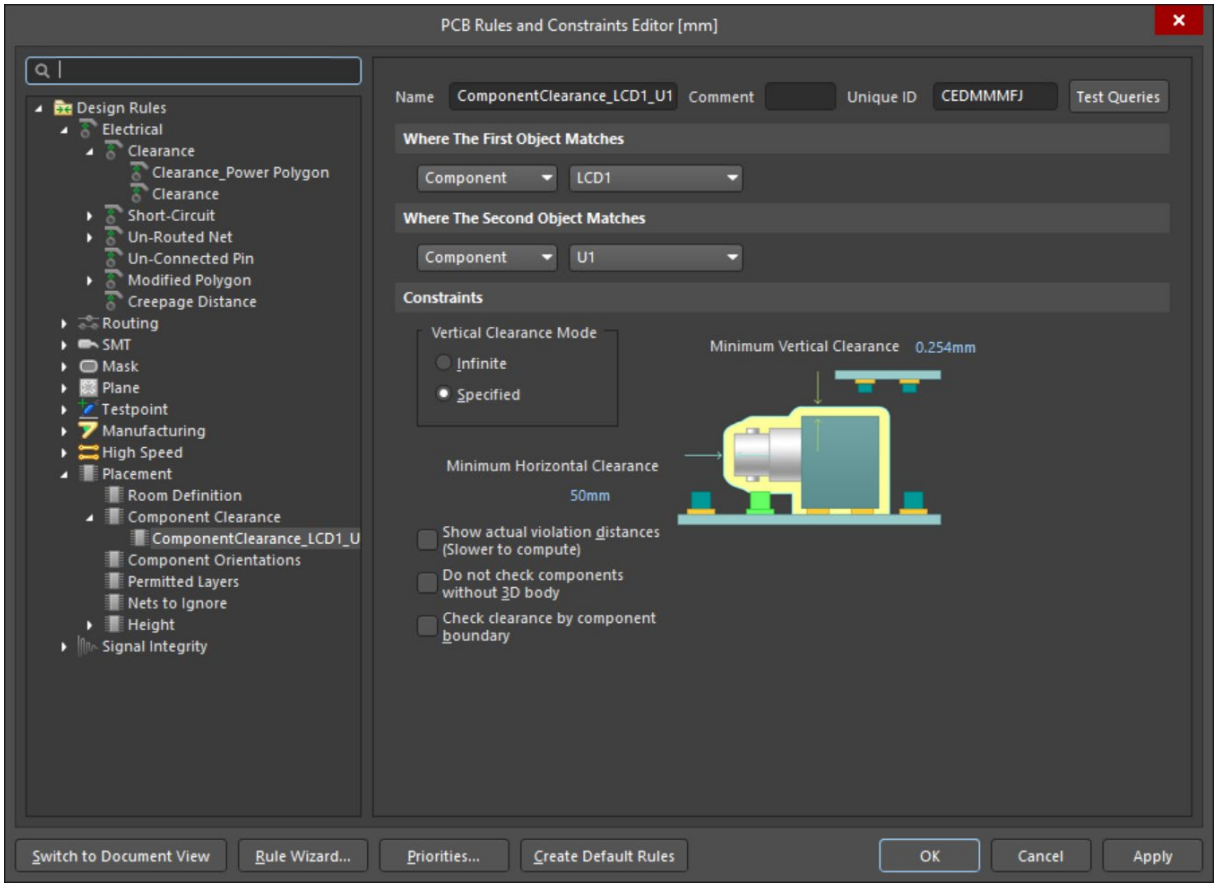

Figure 5. Component Clearance Design Rule for LCD1 and U1

23. Change the **Minimum Vertical Clearance Constraint** to `10mm` and click **OK**.
24. In the PCB, both the LCD display and the FPGA will be highlighted in the DRC violation color as illustrated in Figure 6.

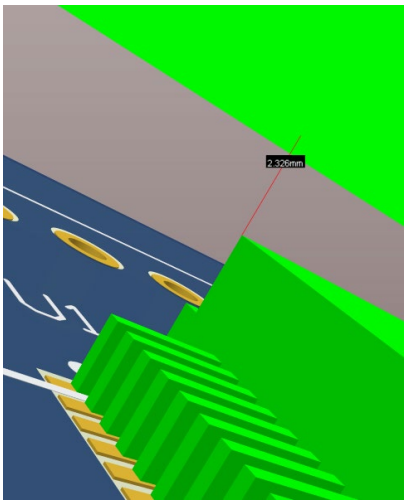

Figure 6. DRC Violation indicated by LCD and FPGA highlighted in green

25. Zoom in on the black collision indicator. This may require rotating the PCB to view the clearance between the two components. Note how the collision is indicated in the Z axis with a fine vertical line.
26. This next step will modify the clearance rule to remove the vertical violation and introduce a new horizontal violation. Open the *PCB Rules and Constraints Editor* and modify the Component Clearance rule for `LCD1` to `U1` setting the **Minimum Vertical Clearance** back to `0.254mm` and set the **Minimum Horizontal Clearance** to `50mm`.
27. Note how the collision is now indicated in the X and Y Axis with a fine horizontal line as shown in Figure 7.

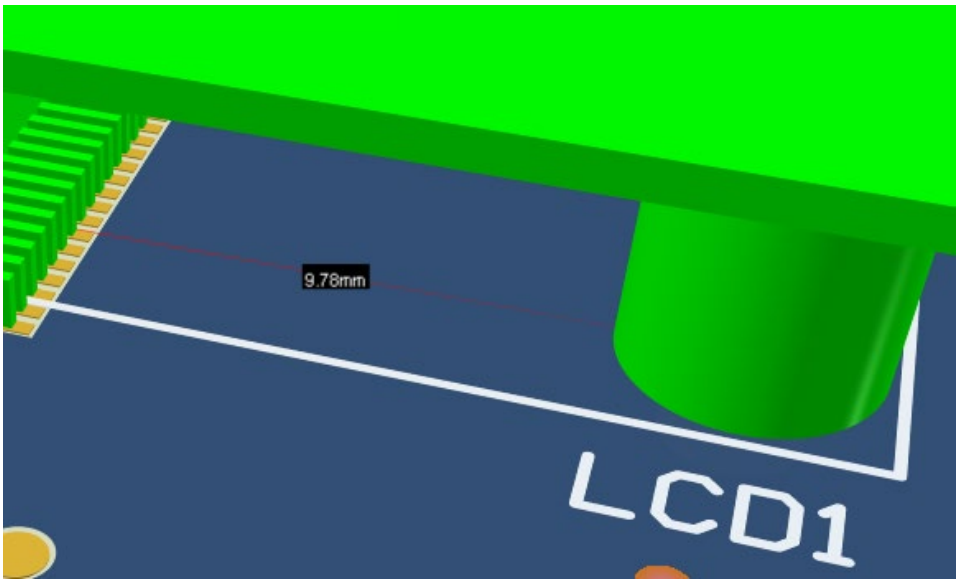

Figure 7. Collision between FPGA and LCD is indicated by a fine horizontal line

1.5 Conclusion

Component clearance is achieved independently from the Electrical Clearance rules. 3D component bodies are used to determine the clearance between components and the Component Clearance rule constraints adjust the minimum gap between 3D bodies of components.

28. Feel free to save the modifications.

29. Close the project and any open documents.

Congratulations on completing module:

Clearance Checking in 3D

from the

Altium Designer Advanced Course

Thank you for choosing Altium Designer