

Altium Designer

Advanced Course

Module: Pin Swapping

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Pin Swapping

1.1 Purpose

Working in harmony with Altium Designer's interactive routing and BGA escape routing capabilities is the pin, differential pair, and part swapping system. This feature provides all the benefits of traditional pin-swapping systems but takes advantage of Altium Designer's intimate understanding of the net assignments in the design. During a pin swap operation, Altium Designer analyzes the net assigned to the chosen pin, and dynamically reassigns the net on the pin and any connected copper. This exercise shows how to set up pin swapping in preparation for interactive routing.

1.2 Shortcuts



Shortcuts when working with Pin Swapping

F1:	Help
C-O:	Project Options
T-W-C:	Swap Configuration
T-W-A:	Automatic Net/Pin Optimizer...
CTRL+S:	Save Document

1.3 Preparation

1. **Close all existing projects and documents.**
2. Open the `Pin Swapping.PrjPCB` project found in its respective folder of the Advanced Training.

1.4 Pin Swapping

1.4.1 Overview

Preliminary routing consists of creating net stubs for escape routing from configured components that have swappable pins and/or routing components that connect to the swappable nets. These routes, while not making the full routed connection, are close enough so that the Net/Pin optimization can then be performed to help uncross the traces to provide a direct route completion path, as shown in Figure 1.

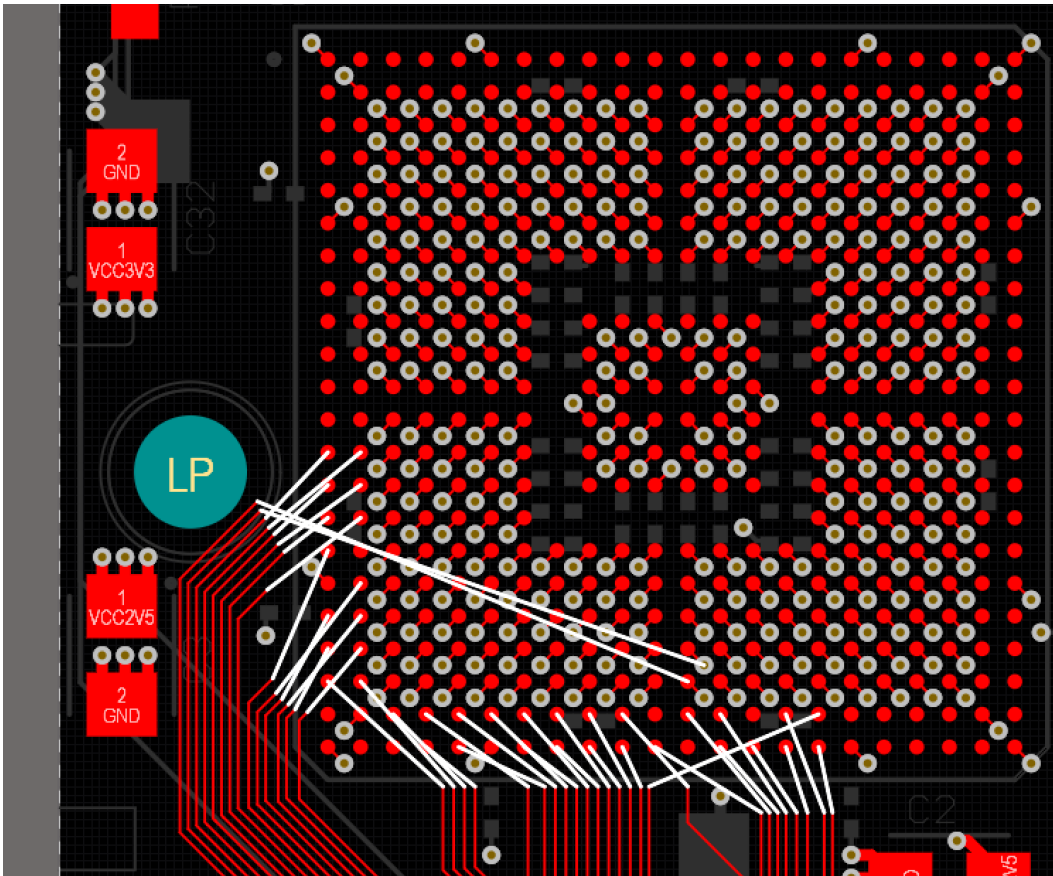


Figure 1. Direct route completion with Pin Swapping



Pin swaps must be configured for the component before running the Net/Pin optimizer.

After the Fanout process is complete, the Net cross-status can be quite severe. This is due to the fact the Net allocation and component placement was largely determined during schematic portion of the design process. Resolving this routing complexity has been a major challenge in the past.

Fortunately, Altium Designer has powerful Pin/Net Swapping features that help designers redefine the FPGA's I/O Net configurations automatically, and the changes can be updated back to the schematic.

1.4.2 Pin Swapping configuration

3. Open the PCB by double-clicking on the NBP-28 Pin_Swap_Example.PcbDoc in the *Projects* panel, as well as the FPGA.SchDoc.
4. First, restrict the swapping allowed to exclude moving Schematic Pins. This prevents the component on the schematic becoming out of sync with the original library definition. Select **Project » Project Options** from the main menu.
 - a) In the *Options* tab: locate the *Allow Pin Swapping Using These Methods* section and make sure only **Adding/Removing Net-Labels** is checked as shown in Figure 2. **Changing Schematic Pins** should not be selected.
 - b) Click **OK** to quit the dialog.

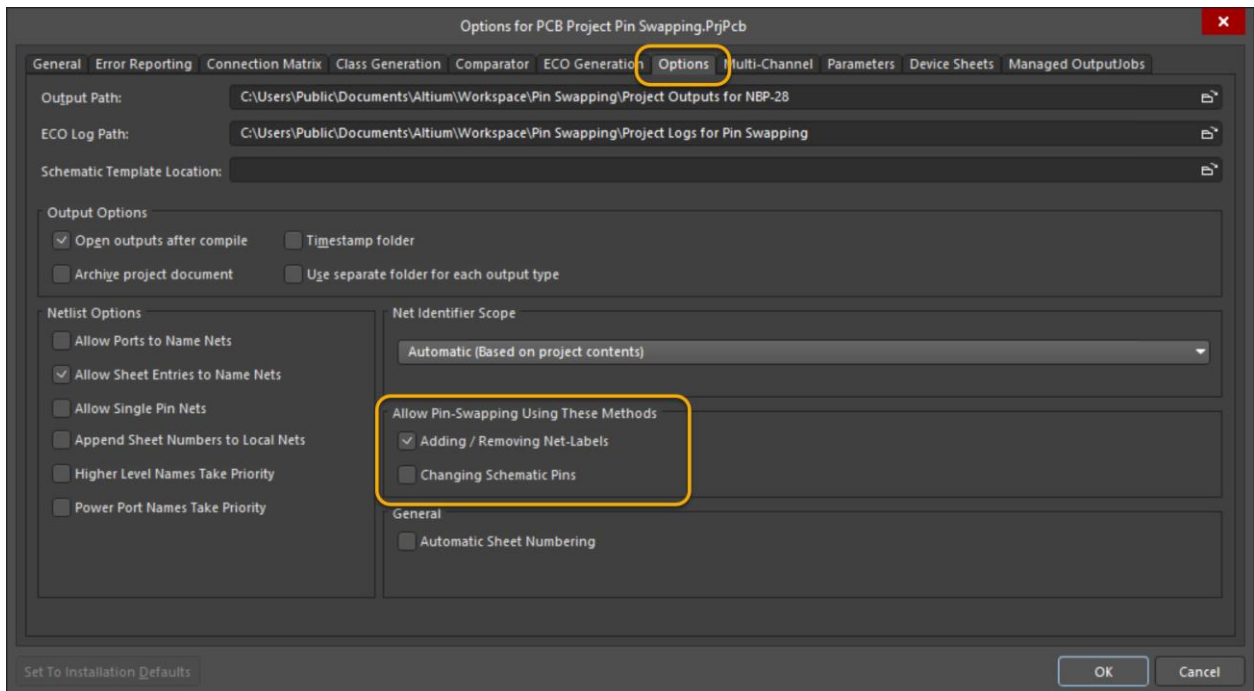


Figure 2. Project Options, Options Tab

5. Locate the FPGA device U1, in the PCB Editor.
6. Zoom in and put the FPGA in the center of the viewable area.
7. Double click on the device to open its properties.
8. Look for the Swapping Options section and tick the **Enable Pin Swaps** checkbox as shown in Figure 3 below.



This can also be done in the Pin/Part dialog after the swap groups are defined.

9. Click **OK** to close the dialog.

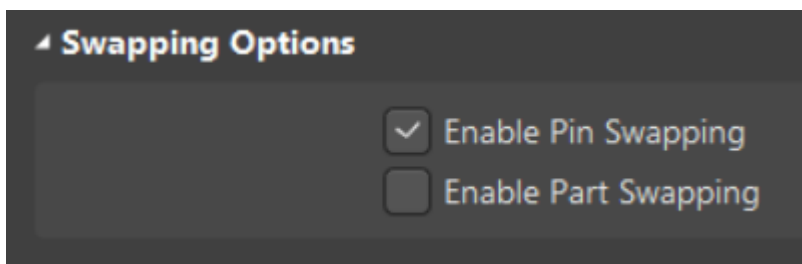


Figure 3. Component Properties U1

10. Click **Tools » Pin/Part Swapping » Configure** to open the *Configure Swapping Information In Components* dialog. Locate and select the FPGA (U1A) in the list and click the **Configure Component** button (lower left) as shown in Figure 4. If the FPGA is not listed, be sure that the **Only Show Components with Swap Information** checkbox is unchecked.

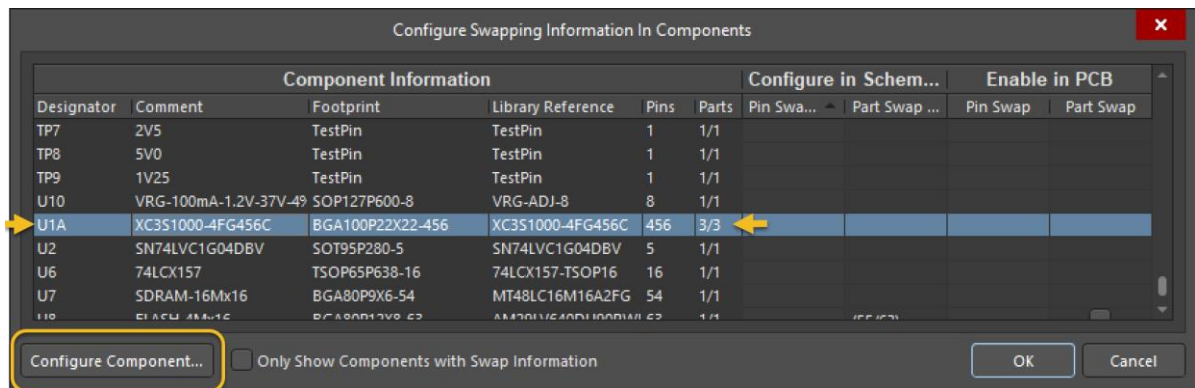


Figure 4. Configure Swapping Information In Components

- The *Configure Pin Swapping* information for U1 appears as shown in Figure 5. Be sure to select the *Pin Swapping* tab located in the upper left corner.

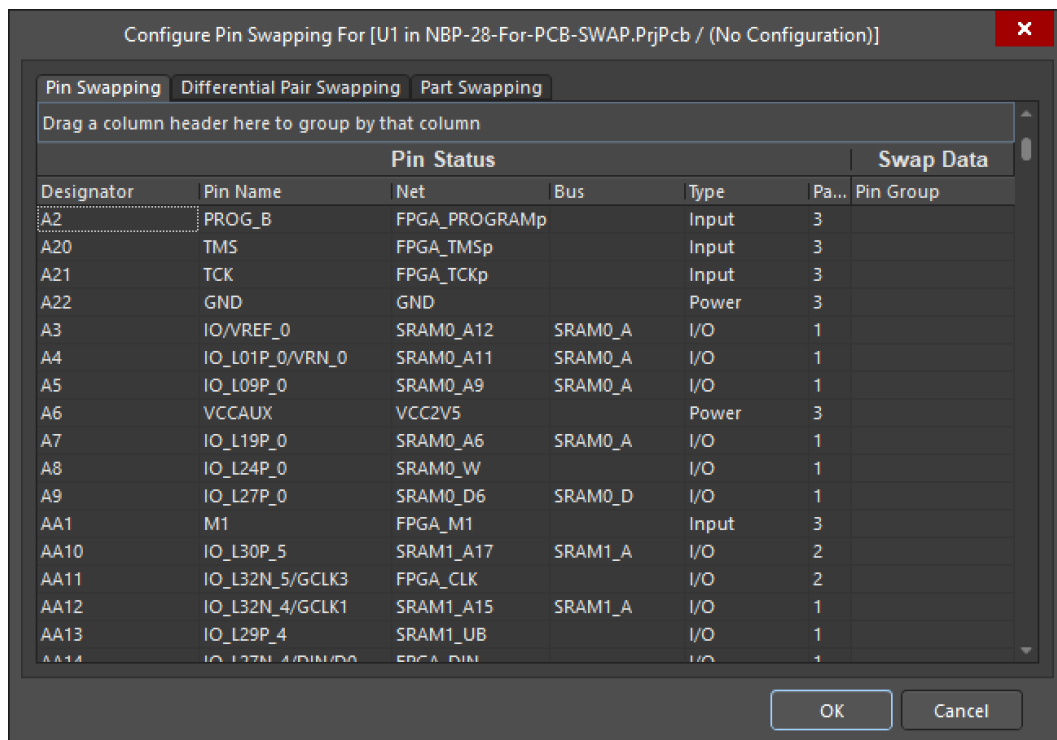


Figure 5. Pin Swapping Configuration

- Click the *Pin Name* header label at the top to sort the list by pin name. All the pins with prefix IO will be listed together. Select all the rows with the IO_ prefix with the **Shift + Click** keys.
- Right-click the list and select **Add To Pin-Swap Group » New**. Note that those pins are now allocated to Group 1, as shown in the Pin Group column.



All FPGA pins enabled for swapping are included in Group 1 and can be freely swapped within this group. Make sure pins that shouldn't have their net changed (swapped) are not included in the group.

- Remove the pin with net FPGA_CLK, FPGA_Done, FPGA_CCLK from Group 1, right-click on its row and select **Remove From Pin Swap Group**.

15. Click **OK** to finalize the Pin Swapping configuration.

16. Ensure that the **Pin Swap** checkbox is enabled for U1A as shown in Figure 6, then click **OK**.

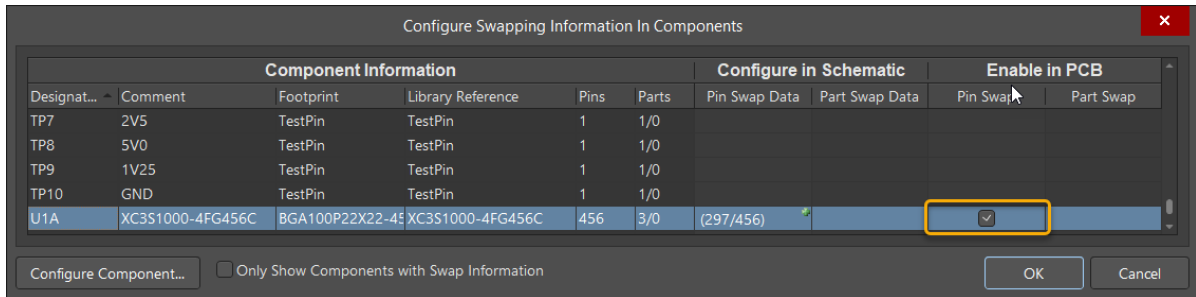


Figure 6. Pin Swap Enabled for U1A in Configure Swapping Information In Components Dialog

17. Click **OK** when prompted to update 3 Sub-Parts in Schematic Sheets, as shown in Figure 7.

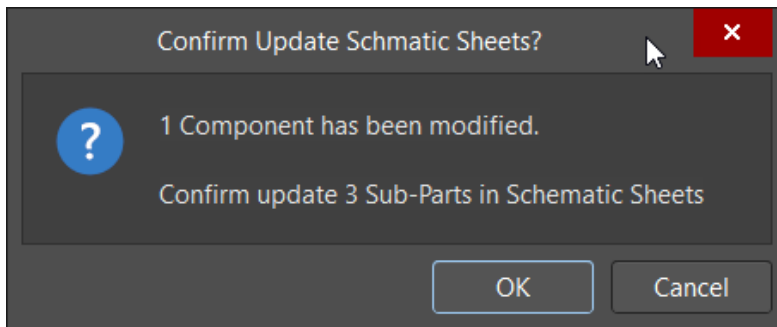


Figure 7. confirm Update Schematic Sheets

18. Select **File » Save All**.

1.4.3 Automatic Pin Swapping

19. Now run the pin swapping optimizer by selecting **Tools » Pin/Part Swapping » Automatic Net/Pin Optimizer**.

- Click **Yes** to continue with the iterative optimizer when prompted.
- Results of the optimization are summarized in Figure 8.



To re-optimize the connections the Net/Pin Optimizer can be re-run again if there are any changes in the copper layout.

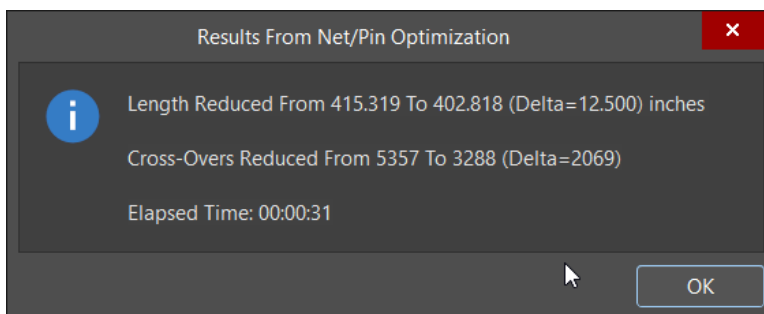


Figure 8. Results from Net/Pin Optimization



Check the PCB and note what changes have occurred to the FPGA nets and wiring. Is this the result you expected? How long would this process have taken if manual pin swapping methods had been used to simplify the connections?

1.4.4 Swap information in the Schematic

20. For the last step, from the PcbDoc, select **Design » Update Schematics in NBP-28-For-PCB-SWAP.PrjPcb** and click **Yes** when prompted by the *Comparator*.
21. Click **Execute Changes** in the *Engineering Change Order* dialog.
22. Once the *ECO* is finished, close the dialog and select **File » Save All**.
23. Switch to the `FPGA.SchDoc` to see that the Net labels have changed by executing **Edit » Undo** and then **Edit » Redo**.
24. Save all your work and close all design files.



The assigned pin swaps in this example were arbitrary, and valid swappable pins should be set and verified as defined in the manufacturer's datasheet.

25. **Close the project and any open documents.**

Congratulations on completing module

Pin Swapping

from the
Altium Designer Advanced Course

Thank you for choosing Altium Designer