

Altium Designer

Advanced Course

Module: Testpoints

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Altium Designer - Advanced Training

Testpoints

Table of Contents

1.1 Purpose	3
1.2 Shortcuts	3
1.3 Preparation	3
1.4 Setting up Testpoint Design Rule	3
1.5 Creating Testpoints	5
1.6 Generating Testpoint Reports	e

Testpoints

1.1 Purpose

Testpoints enhance the testability of boards, whether you want to test the connections on a bare board, and/or one that has already been populated. Altium Designer provides a powerful way to handle testpoints. Testpoints can be assigned manually or, in a more streamlined and automated fashion, using the *Testpoint Manager*. In this exercise, we will create PCB testpoints automatically from design rules.

1.2 Shortcuts



Shortcuts when working with Testpoints

F1: Help

D-R: PCB Rules and Constraint Editor

CTRL+S: Save Document

1.3 Preparation

- 1. Close all existing projects and documents.
- 2. Open the Testpoints. PriPCB project found in its respective folder of the Advanced Training.

1.4 Setting up Testpoint Design Rule

- 3. From the *Project* panel, open Testpoint.PcbDoc.
- 4. Access **Design** » **Rules** to open the *PCB Rules and Constraints Editor*.
- 5. Expand and access the *Testpoint* and *Assembly Testpoint Style* branches on the right and continue to the *Assembly Testpoint Style* rule.
- 6. Click the **Test Queries** button to see the objects the query applies to, Figure 1. Note that objects in the *Test Queries Results* dialog will be further constrained by the clearance settings, but this rule will still not be applied to these objects until assigning as Testpoints in the Testpoint Manager.
- 7. Close the Test Queries Results dialog.

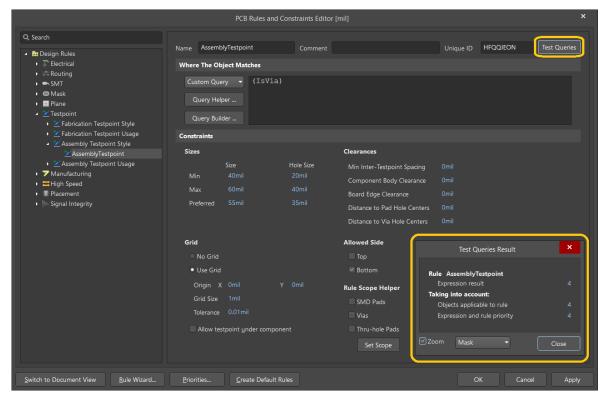


Figure 1. Assembly Testpoint Rule

- 8. It is important to understand that the assembly testpoint query only applies its testpoints to vias, specifically the constraints of the copper expansion and hole sizes of the objects. Since there are only 4 vias in the design, there will be a maximum of 4 Assembly Testpoints that will be assigned in the Testpoint Manager.
- 9. Next, under the *Testpoint* Design Rule section, expand the *Fabrication Testpoint Style* branch to access the *FabricationTestpoint* rule.
- 10. Notice the fabrication testpoint query only applies to multi-layer pads and is further constrained by the copper expansion and hole size.
- 11. Click the **Test Queries** to see the applicable items. Note all thru hole pads have been targeted.
- 12. Close the Test Queries Result dialog.
- 13. Click **OK** to close the *PCB Rules and Constraints Editor*.

1.5 Creating Testpoints

- 14. To access the Testpoint Manager, access Tools » Testpoint Manager.
- 15. Create the fabrication and assembly testpoints by clicking the buttons shown in Figure 2 and selecting **Assign All**.

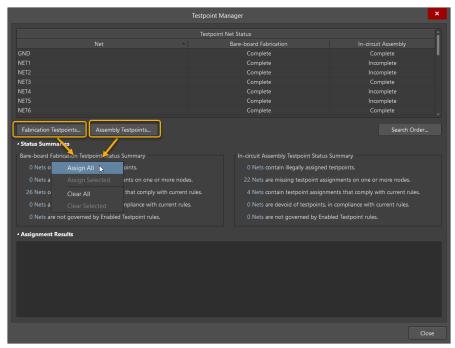


Figure 2. Generating Fabrication and Assembly Testpoints

- 16. Note that the Fabrication Testpoints will be placed only on multilayer pads which will result in coverage of the entire 26-net design. However, the Assembly testpoint usage rule query only includes vias.
- 17. Click the **Close** button to exit the *Testpoint Manager* dialog.

1.6 Generating Testpoint Reports

- 18. Open the Testpoint Reports.OutJob file from the Settings folder located in your Projects panel.
- 19. In the Outjob section, double-click the Test Point Report output in the Fabrication Outputs.
- Enable the IPC-D-356A dialog box to generate this report format as part of your outjob, see Figure 3.
- 21. Click **OK** when finished.
- 22. Click the **Generate Content** button to begin creating the output files. These files are usually created where the project folder resides, see Figure 4.
- 23. Two tabs in the editor window will be created for the testpoint reports. These files will also appear in the *Generated* section of the *Projects* panel, see Figure 5.
- 24. Close all files when done. Do not save anything.



One of the three flavors of testpoint report output formats is an IPC-D-356A netlist file. This file is typically used to target the bare-board fabrication testing mode. The IPC file is parsed into commands that drive a flying probe testing device.



Regardless of which features are specifically identified as test point locations in an IPC-D-356A file, board fabrication houses can generally use the file data to achieve whatever type of testing they need. That being said, depending on the circumstances and the content of the file, some manual intervention may be required to accomplish this.



Figure 3. Generating an IPC-D-356A Netlist

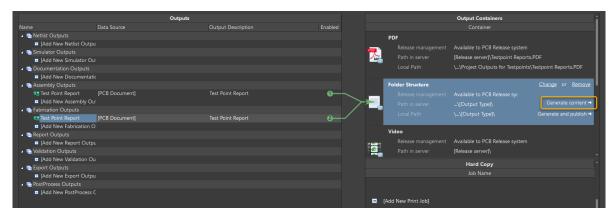


Figure 4. Generating output files

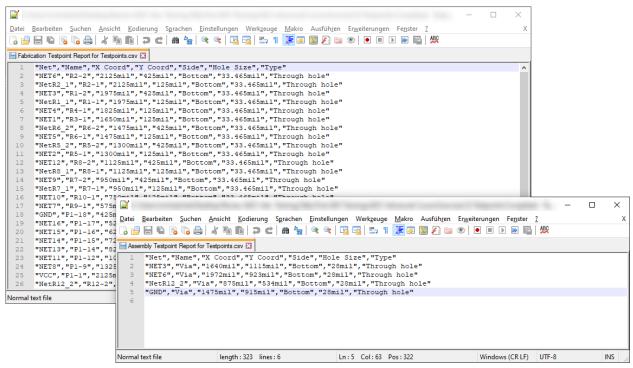


Figure 5. Testpoint Reports as CSV

1. Close the project and any open documents.

Congratulations on completing module

Testpoints

from the **Altium Designer Advanced Course**

Thank you for choosing Altium Designer