

# Altium Designer

## Advanced Course

Module: Differential Pair Routing  
with Impedance Profile

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# Differential Pair Routing with Impedance Profile

## 1.1 Purpose

A differential signaling system is one where the signal is transmitted through a pair of tightly coupled carriers, with one carrying the signal and the other carrying an inverted (equal but opposite) image of the signal.

Differential signaling is inherently immune to common-mode electrical noise, which the most common interference artifact present in electronic products. Another major advantage of differential signaling is that it minimizes the electromagnetic interference (EMI) generated from the signal pair.

## 1.2 Shortcuts



Shortcuts when working with Differential Pair Routing with Impedance Profile


<b>F1:</b>	Help
<b>D-R:</b>	PCB Rules and Constraint Editor
<b>U-I:</b>	Differential Pair Routing
<b>Spacebar:</b>	Routing Angle
<b>Shift+Spacebar:</b>	Routing Corner Style
<b>CTRL+S:</b>	Save Document

## 1.3 Preparation

1. Close all existing projects and documents.
2. Open the `Differential Pair Routing.PrjPCB` project found in its respective folder of the Advanced Training.
3. Open the `Diff Pair Routing.PcbDoc` document.
4. Open the `Differential Pair Setup.SchDoc` document.

## 1.4 Defining the Differential Pair

Next we will create the differential pair signals and add Differential Pair Directives, it is also possible to add net and differential pair classes in the schematic, as well as design rules. In this exercise, we will predominantly use the Active Bar menu, although the same features are available from the Place dropdown menu.

5. If not already the active document, change focus to the schematic document.
6. From the *Active Bar* select **Net Label** as shown in Figure 1, hit the **Tab** key to access the *Properties* panel whilst the net label is attached to the cursor, and change the name to `D1_N`. Press **Escape** or select the Pause  to place the net label on connection between `U1-Pin1` and `L1-Pin2`.
7. Repeat Step 6 to place net label `D1_P`. Final placement of net labels should look like as shown in Figure 2.

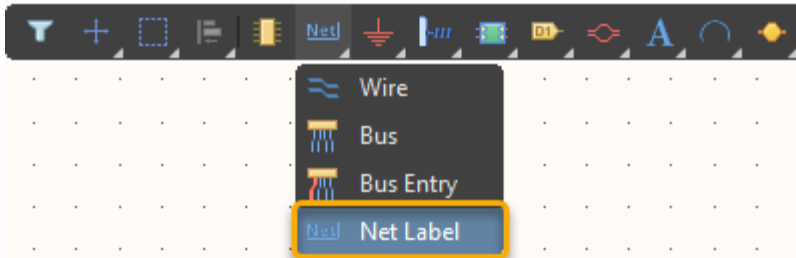


Figure 1. Place Net Label

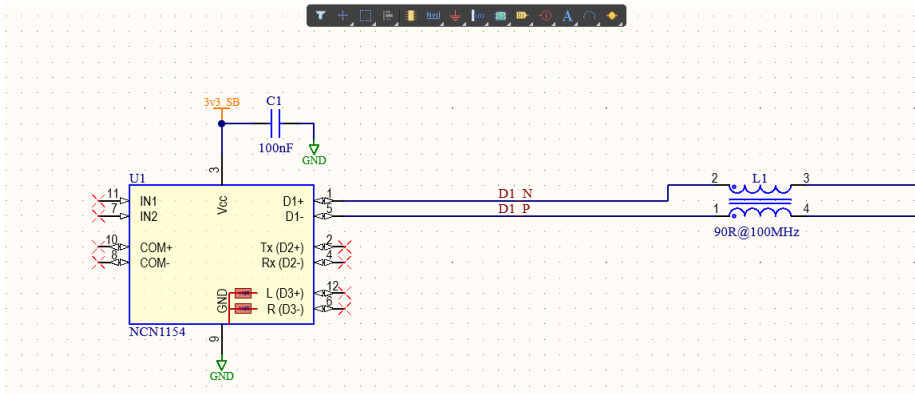


Figure 2. Differential Signals

Notice other net labels have already been placed, this is to speed up the process. However, we will add the Differential Pair and Parameter Set directive, and also utilize the Blankets feature, this will enable us to add a single directive to a group of signals rather than one to each net.



The default suffix for differential pair signals is \_P and \_N, it is also possible to add custom suffix characters in the Diff Pairs section in the *Project Options*.

8. From the *Active Bar* place a **Blanket** (Figure 3) over the net labels, the first left mouse click will anchor the blanket, now move the mouse diagonally across to cover the net labels, second left mouse click to size the blanket, finally right mouse click to finish the placement. The finished placement should look like Figure 4.

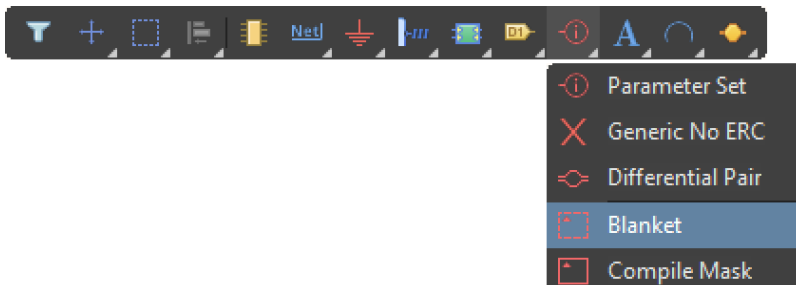


Figure 3. Blanket

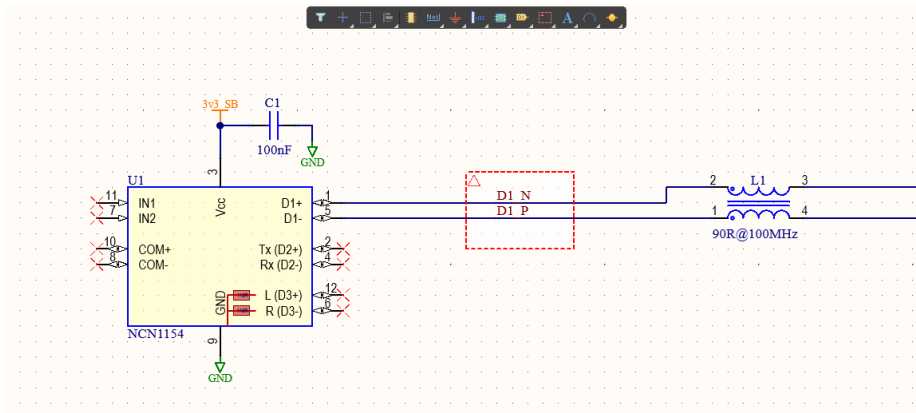


Figure 4. Blanket Placement

9. Next, from the *Active Bar* select the **Differential Pair** directive Figure 5, before placing hit the **Tab** key to access the *Properties* panel and edit the Label to 90R\_DIFF, as shown Figure 6.

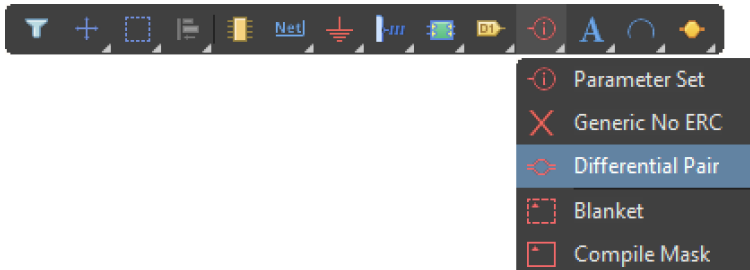


Figure 5. Differential Pair Directive

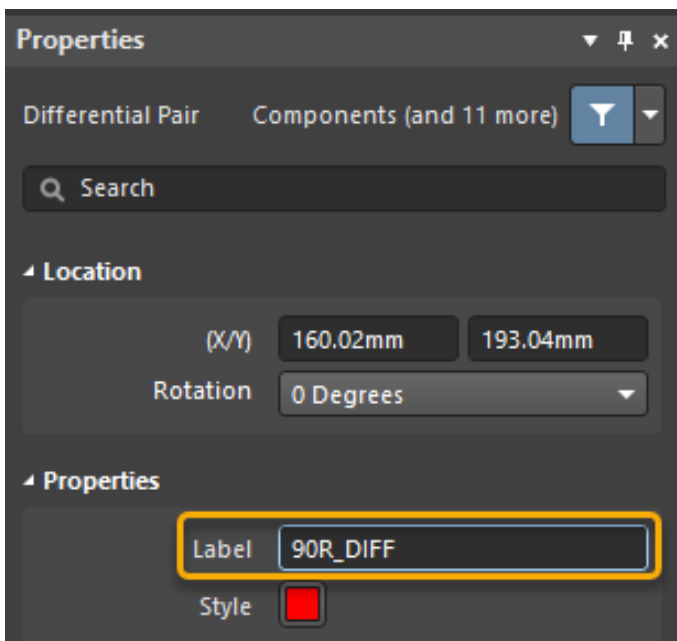


Figure 6. Label for Differential Pair Directive

10. Still in the *Properties* panel, as shown in Figure 7

- Select the **Add...** button at the bottom of the *Parameters* section, and add a **Diff Pair Net Class** and type 90R\_DIFF in the Value section.
- Staying in the *Parameter* section, add a **Matched Net Lengths** design rule, change the *Tolerance* for *Within Differential Pair Length* to 0.5mm.
- Enable the visibility of the **Matched Length Rule** and **Diff Pair Class** with the eye icon.

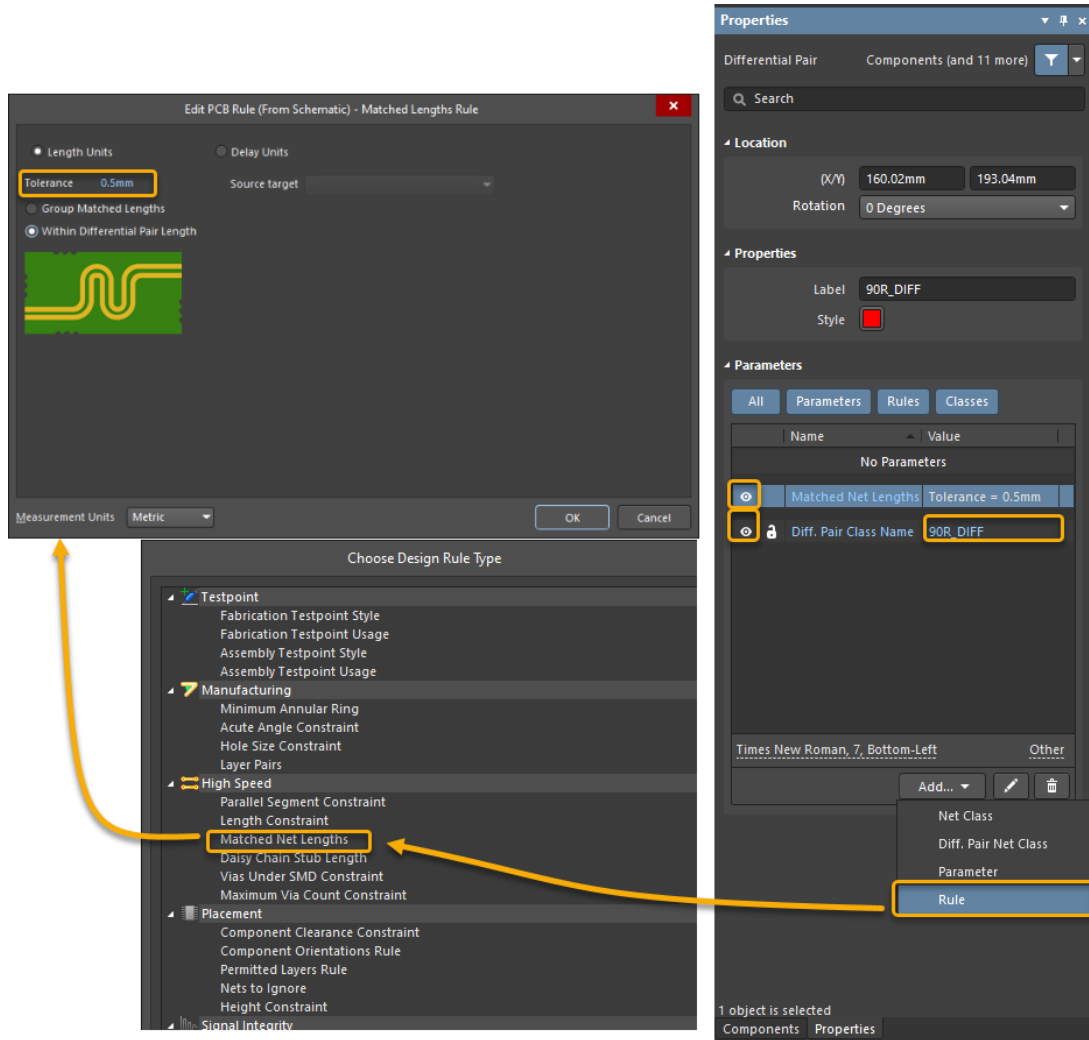


Figure 7. Differential Pair Class and Design Rule

- Now place the Directive on the Blanket. Feel free to change the position of the strings, as shown in Figure 8.

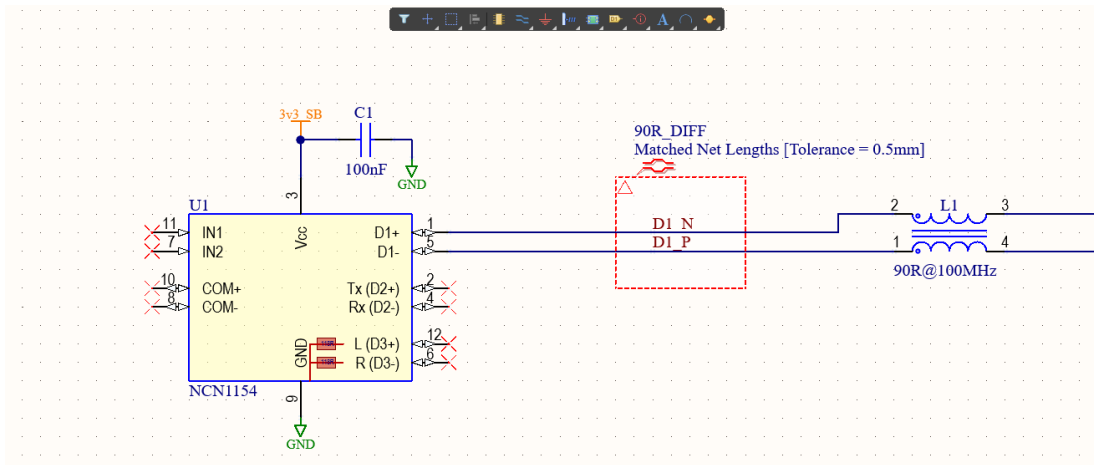


Figure 8. Blanket Directive

12. Copy the Blanket together with the directives and place them over the remaining differential signal, as shown in Figure 9

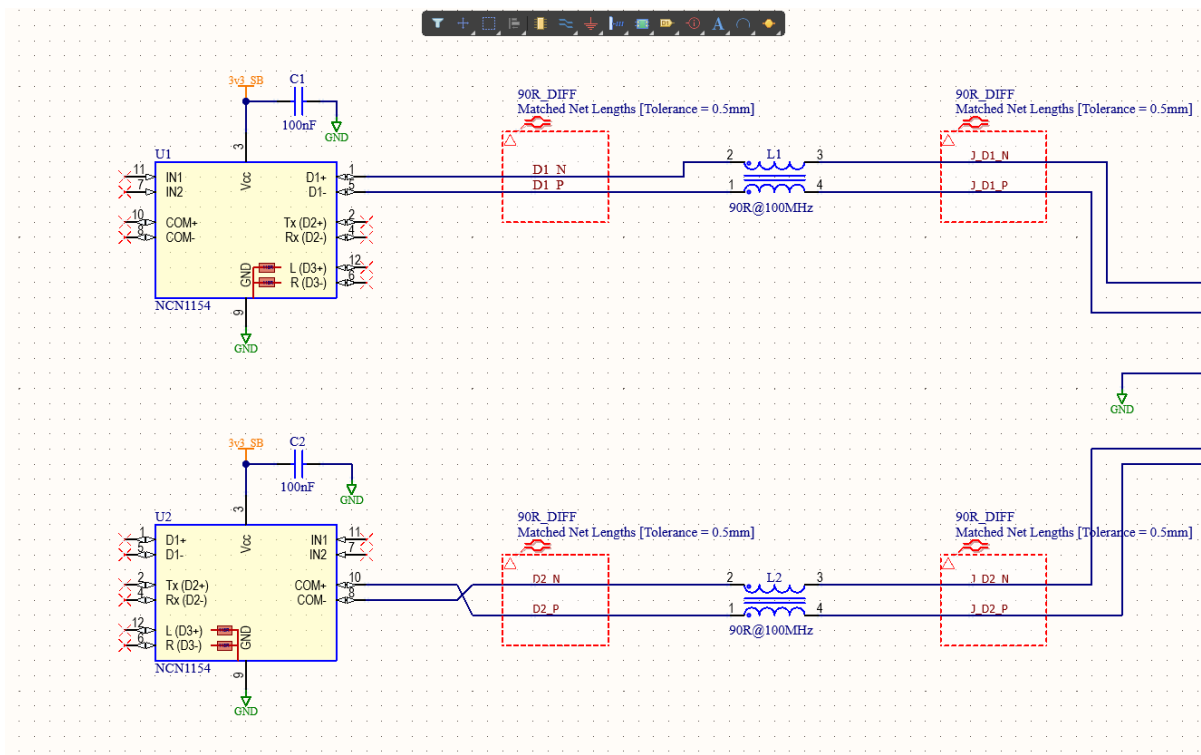


Figure 9. Copied Directives



At this stage it is advisable to run the electrical rules check by validating the project.

13. Run validation either by using the right mouse button over the project name in the *Project* panel or using the Project dropdown menu.
14. Open the *Messages* panel to check for any errors or warnings.





The messages panel only pops open if there are errors, and does not pop open if there are just warnings, but it is always advisable to open the messages panel even if it does not open automatically.

15. Ensure the compile is successful and there are no errors or warnings, as shown in Figure 10.

Class	Document	Source	Message
[Info]	Differential Pair Routing.PrjPcb	Compiler	Compile successful, no errors found.

Figure 10. Project Validation

16. Now transfer the design to the PCBs, by either updating the PCB from the Schematic using the **Design » Update PCB...** menu or by opening the PCB and running the Import from the PCB using the **Design » Import Changes from ...** menu.



It is always a good idea to look at the ECO and understand what information is being transferred.

17. Select **Execute Changes** to transfer the schematic updates to the PCB document, Figure 11.

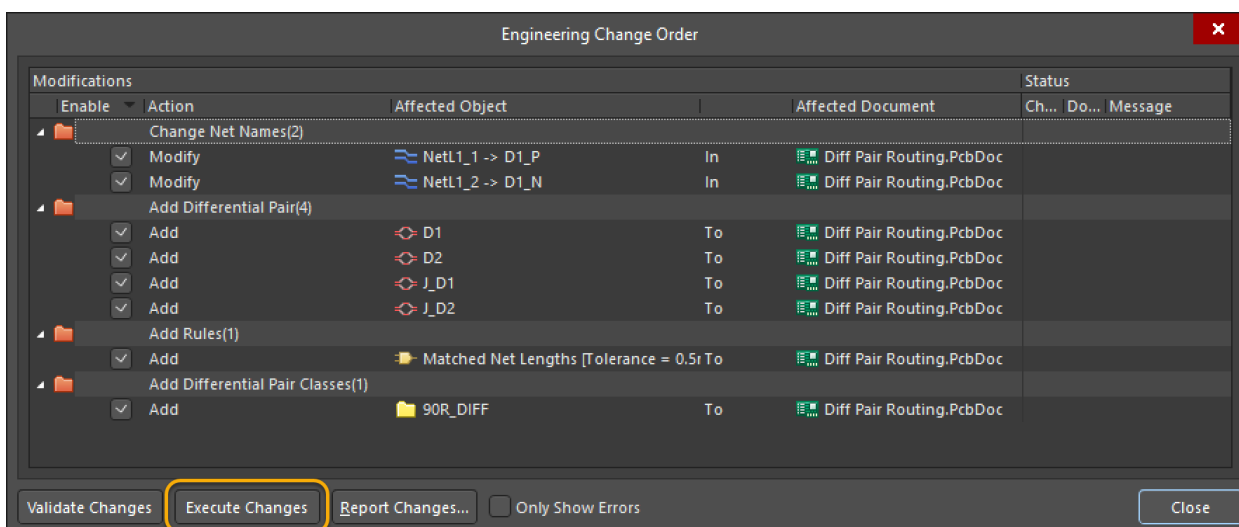


Figure 11. Engineering Change Order

18. If not already, change the focus to the PCB document.
19. Using the *PCB* panel, first let's check what information has been transferred to the PCB.
20. Select the **Differential Pairs Editor** from in the *PCB* panel, and notice the four differential pairs in the PCB, Figure 12.

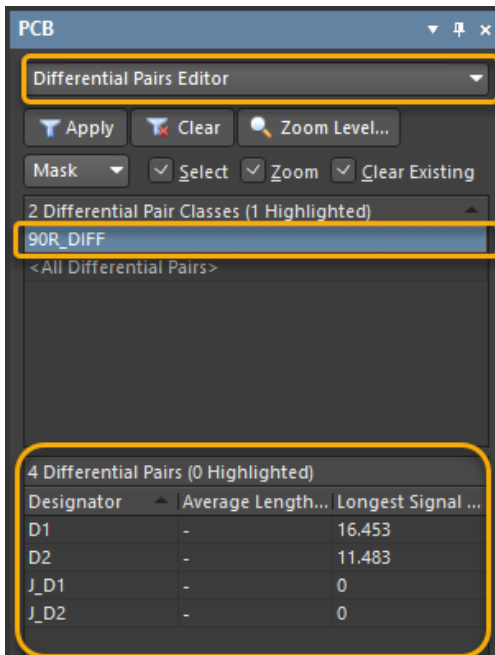


Figure 12. Differential Pairs Editor

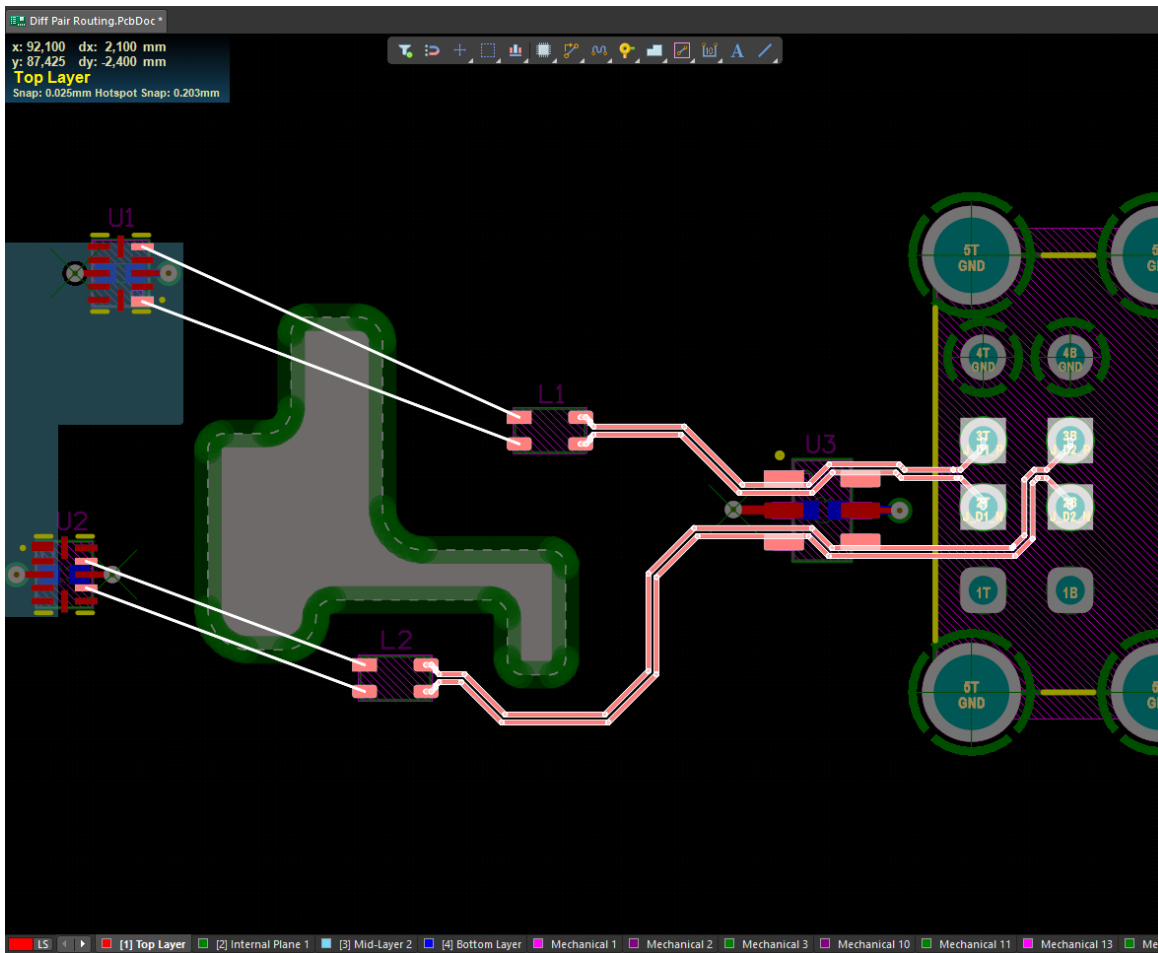


Figure 13. Differential Pair – 90 Ohm

## 1.5 Defining the Impedance Profile

Before routing the differential pair signals, we need to create the design rule for track and gap. The track and gap of differential pairs is determined by certain key factors, some of these are; the layer stack, and the required target impedance. One of the ways of obtaining the track and gap information is by consulting your board manufacturer, and providing details of your requirements. Another way is, is to use Altium's Layer Stack Manager to calculate the required Impedance Profile.

21. Open the *Layer Stack Manager* (LSM) **Design » Layer Stack Manager...** and select the *Impedance* tab at the bottom left, Figure 14.

22. Click the **Add...** button at the upper left to create a new Impedance profile, Figure 14.

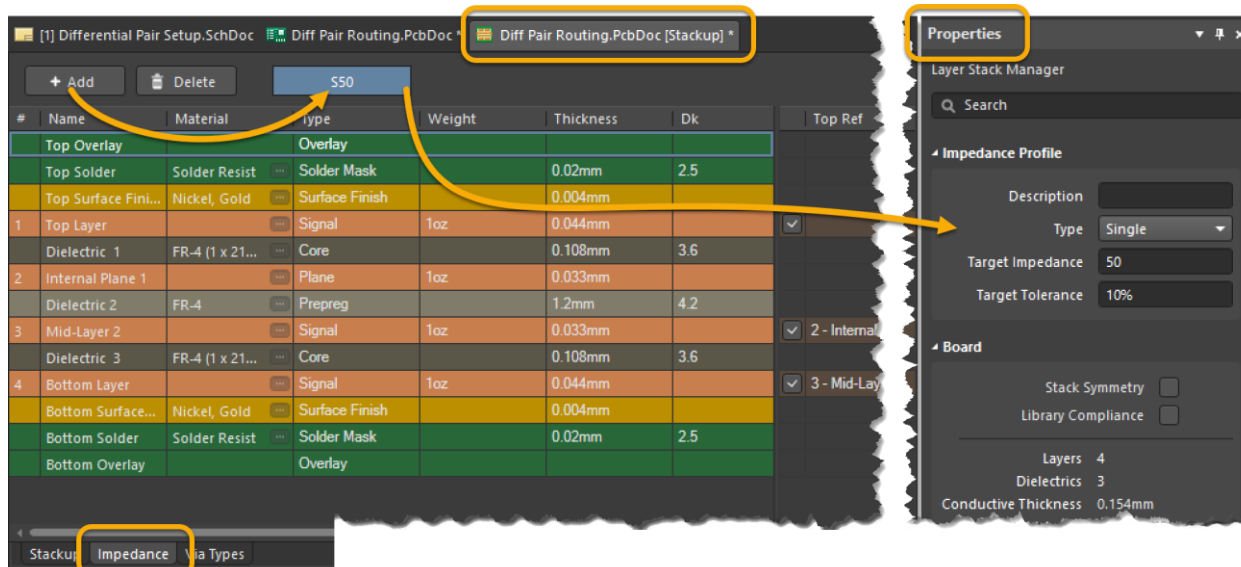


Figure 14. New Impedance profile with default 50 Ohm

23. Dock the LSM *Properties* panel on the left, if not already docked, and enter the following information, Figure 15:

- Description*: USB Differential Signals
- Type*: **Differential**
- Target Impedance*: 90
- Target Tolerance*: 10%

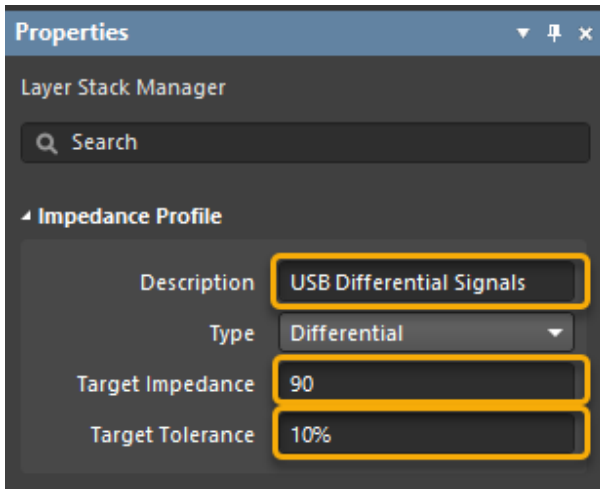


Figure 15. Target Impedance

Next we need to calculate the track and gap for the differential pairs. As we already have some routed differential pairs on the PCB, we want to be able use the same values for Gap and Trace Width for the remaining differential pairs. When starting with a new PCB, the Impedance Profile will already start with default values for Track and gap, these values may change as you make modifications to the layer stack, and to the required target impedance.

24. Select the individual routing layers from the layer stack table one layer at a time, to see the track and gap calculations in the *Properties* panel, as shown in Figure 16. and Figure 17

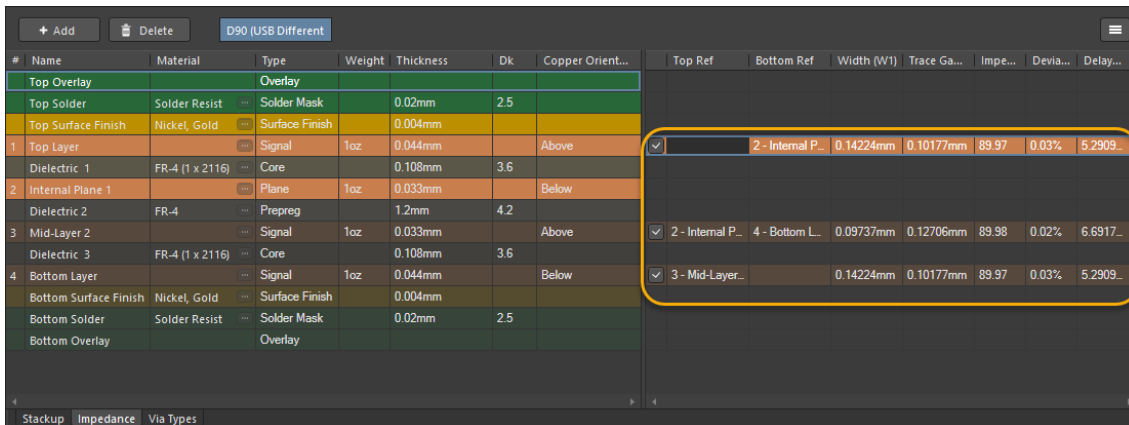



Figure 16. Routing Layers

- Select the **Top Layer**
- Click the Calculate Button  next to the Trace Width. From now on Altium Designer will calculate the Trace with automatically for a given Gap.
- Add 0.102mm as *Trace Gap (G)* at the *Properties* Panel and press **Enter** to save the changes.
- The trace width is automatically updated (0.142...)
- Repeat the steps a) to d) for the Bottom Layer.

**Properties**

Search

**Impedance Profile**

Description: USB Differential Signals

Type: Differential

Target Impedance: 90

Target Tolerance: 10%

**Transmission Line**

Simulated with SIMBEOR® software

Use Surface Finish: ☐

Use Solder Mask: ☒

Trace Inverted: ☐

Etch (?): 0

Width (W1): 0.14224mm

Width (W2): 0.14224mm

Covering (C1): 0.02mm

Covering (C2): 0.02mm

Trace Gap (G): 0.102mm

Impedance (Zdiff): 90.03

Deviation: 0.03%

Delay (Tp): 5.29117ns/m

Inductance: 476.21079nH/m

Capacitance: 58.77941pF/m

**Board**

Stack Symmetry: ☐

Library Compliance: ☐

Layers: 4

Dielectrics: 3

Conductive Thickness: 0.154mm

Components Design Reuse Properties

#3 Width is calculated

#1 automatic calculation for Width is active

#2 Enter Trace Gap

Figure 17. Trace Width and Trace Gap Calculations

## 1.6 Interactive Differential Pair Routing

We will use the new impedance profile for creating the design rules required for routing the differential pairs.

### 1.6.1 Design Rules

25. Save the layer stack in order to update the PCB, now change focus back to the PCB document.
26. Using the **Design » Rules..** menu open the *Design Rules and Constraints Editor*.
27. Expand the *Routing - Differential Pair Routing* section.
28. Add a new Differential Pairs Routing rule and change or select required fields, see Figure 18.
  - a) **Name:** DiffPairsRouting\_90R\_DIFF
  - b) **Where The Objects Matches:** **Diff Pair Class** (select from dropdown list)
  - c) **Select:** **90R\_DIFF**
  - d) **Use Impedance profile:** **Enable** (check selection box), select **D90(USB Differential Signals)** from the dropdown list.
  - e) **Max Uncoupled Length:** 15mm  
(Specifies the value for the maximum permissible uncoupled length between positive and negative nets within the differential pair), Figure 18.

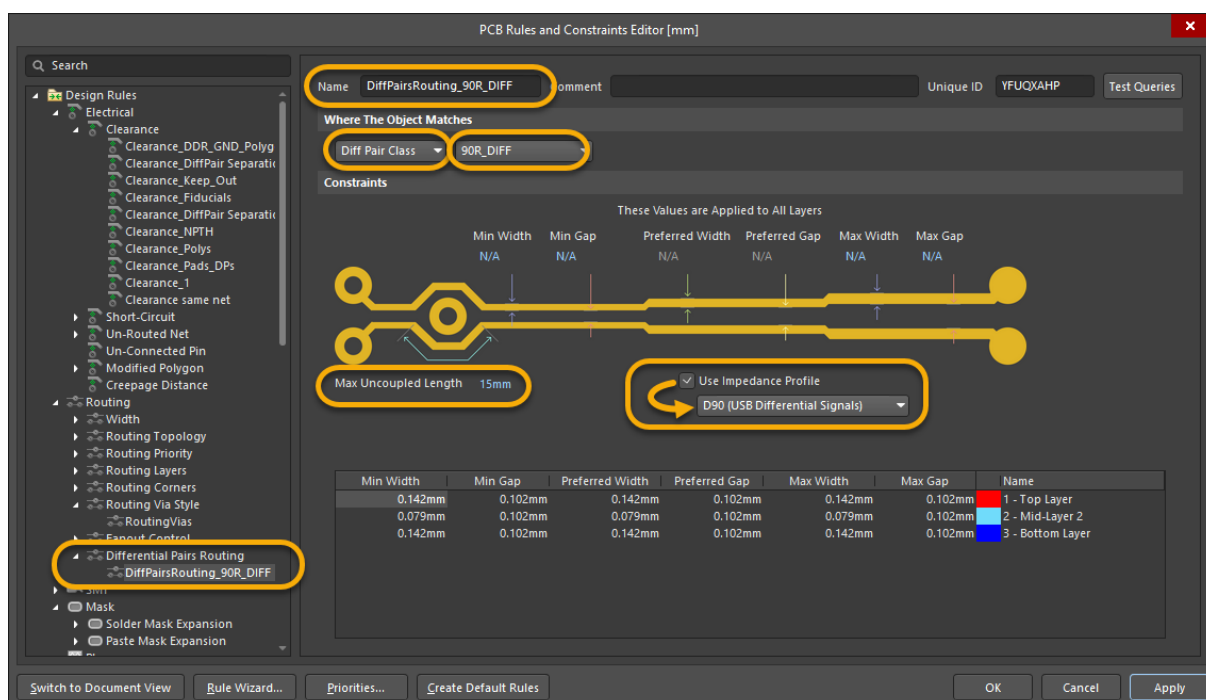


Figure 18. Differential Pair Routing Rule Using Impedance Profile

29. The rule is divided into three sections: **Minimum**, **Preferred**, and **Max** values. However, in most cases, the track and gap values for differential signals should be the same across the same layer, but these may differ from layer to layer depending on the chosen layer stack.
30. Review the values in the design rule table section, these have been pulled in from the Impedance profile.
31. Expand the *Matched Lengths* rule in the *High Speed* section, and review the Matched Length rule transferred from the schematic. Figure 19

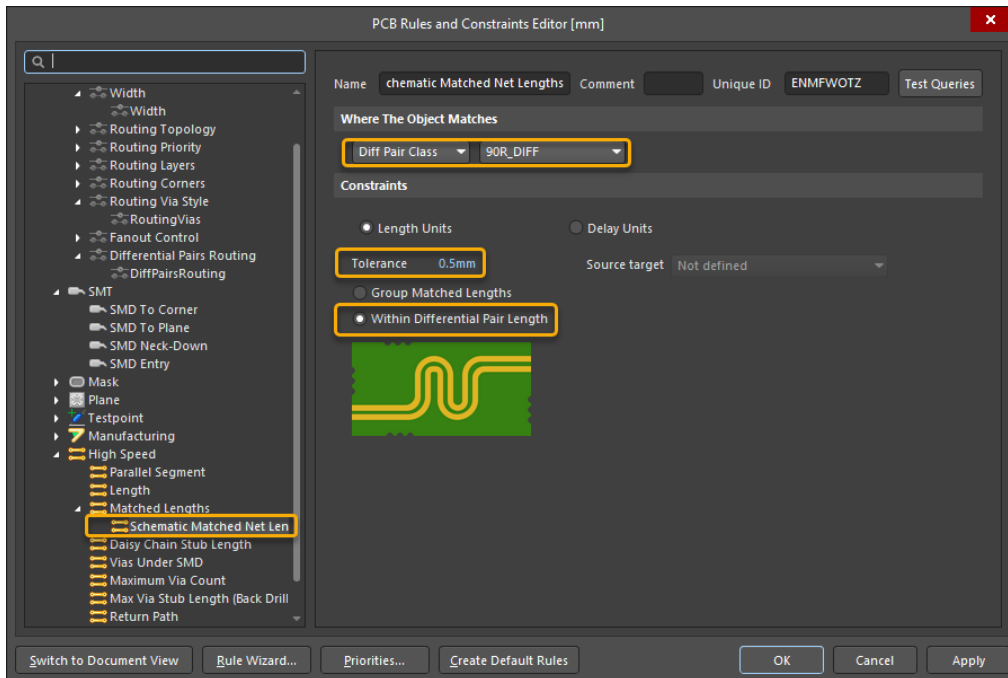


Figure 19. Matched Net Length Rule

32. Select **OK** to save and apply the new design rules.

## 1.6.2 Differential Pair Routing

Prior to routing, ensure the **Smart Track Ends** option is enabled. This option forces connections lines on the end of a track, and overrides the net topology. This is preferred for differential pair routing in the case you suspend a route and leave dangling tracks.

33. Open the *Preferences* from the gear icon  in the top-right corner of Altium Designer.

34. Under *PCB Editor* section, in the *General* page, verify the **Smart Track Ends** checkbox is enabled as shown in Figure 20. Click **OK** to continue.

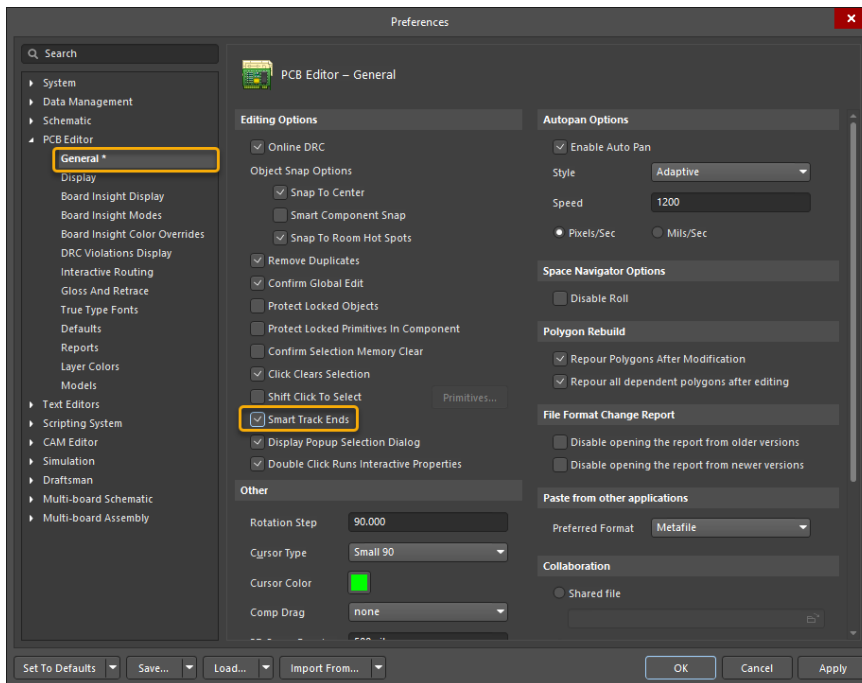


Figure 20. PCB Preferences

35. To start the routing select Interactive Differential Pair Routing from the Active Bar.

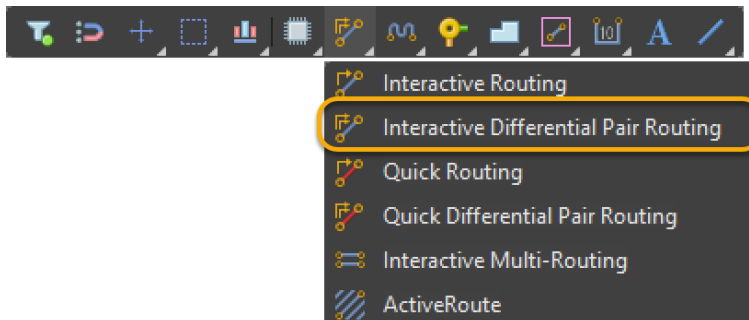


Figure 21. Interactive Differential Pair Routing

36. Start routing by first selecting Pin5 of U1.

37. Press the **Spacebar** during routing to cycle through the different routing angles. Use **Shift+Spacebar** to change the corner style.

38. When the differential pair routing approaches the target, left-click on the target pad or **Ctrl+Left-Click** the target pad to finish the routing automatically.

39. Use the same method, route the other differential pair.

40. The final routing should look similar to Figure 22.



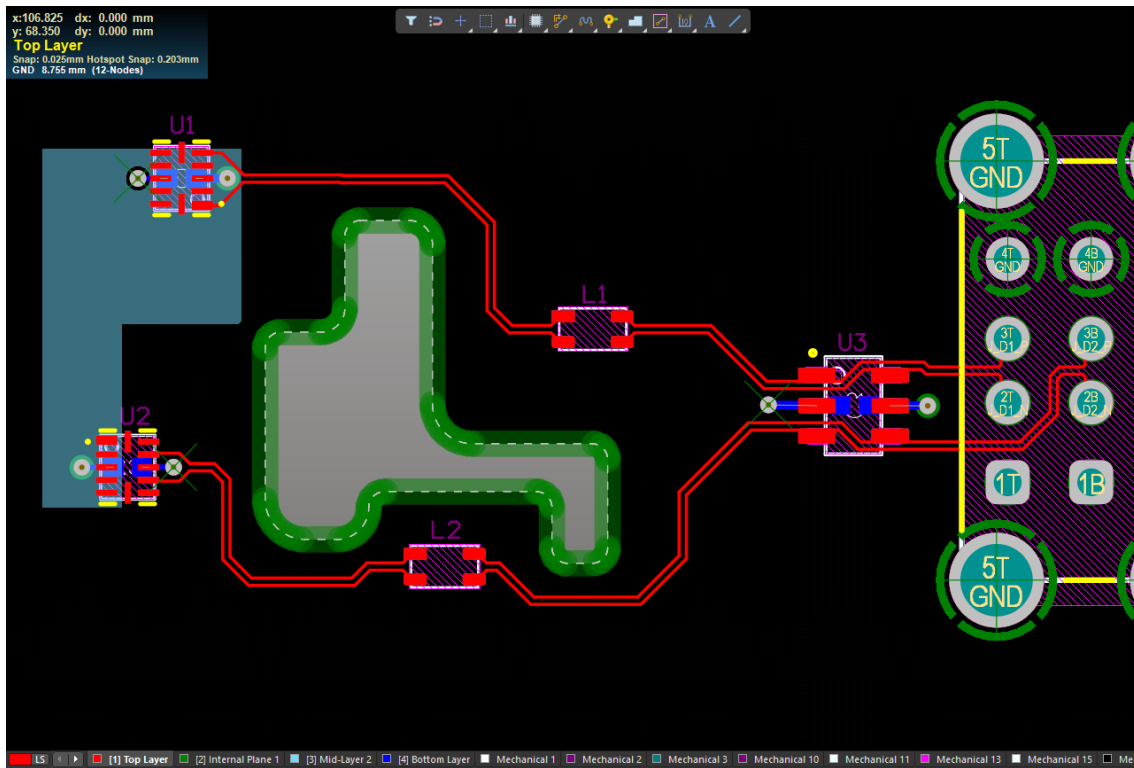


Figure 22. Final Routing



The two traces should be of equal length, within tolerances of the logic family. We will cover this in an additional training module.

41. Feel free to save your changes.
42. **Close the project and any open documents.**

**Congratulations on completing module**

Differential Pair Routing with Impedance Profile

**from the**

**Altium Designer Advanced Course**

**Thank you for choosing Altium Designer**