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ORIGINAL RESEARCH

Improved simulation modelling and its verification for SiC MOSFET

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Abstract

Of crucial importance is to accurately simulate its switching characteristics for the application of SiC MOSFET. Due to the ultrafast switching capability, SiC MOSFET is dependent on interelectrode capacitances and extremely sensitive to parasitics. Therefore, accurate modelling of interelectrode capacitances and knowledge of parasitics are required. Here, an improved SiC MOSFET model driven by an empirical formula with three segments for the non-linear drain-to-gate capacitance in relationship with the drain-to-source voltage is developed. In this way, the capacitance fitting at the inflection point that has a great impact on the switching delay is much improved. By simple self-made high-voltage C–V measurement systems, the accuracy of the proposed formula is verified. More importantly, intruded parasitics by the commonly-used coaxial shunt current measurement loop is analysed in detail. The equivalent circuit of the current measurement loop is incorporated into the device simulation circuit to compensate measurement errors. In this way, the improved model can be more reliably verified and evaluated. A double pulse test is built to verify the proposed model. By comparison of simulation and experimental results, the proposed model works well at different voltage and current operating conditions and offers a reliable and accurate modelling approach.

1 | INTRODUCTION

In recent years, the fast development of SiC power devices has been bringing about advanced power electronic equipment with lower power losses, higher power density and higher operating temperature. SiC MOSFET, as the most popular wide bandgap power device, has been extensively developed, researched and widely used in switching power supplies, motor drives and photovoltaic generation [1–3]. An accurate SiC MOSFET model to accurately simulate the current and voltage switching transients is of great significance in order to estimate switching power losses, predict the EMI, analyse switching ringing and et al. [3].

There are a handful of SiC MOSFET models that have been proposed and a review of these SiC MOSFET models has been presented in [4]. The physical models of SiC MOSFET presented in [5–7] demonstrated good accuracy but are less inefficient in implementation, since those physical SiC MOSFET models are dependent on the device parameters. Parameter extraction procedures are required additionally. Thus, behavioural models of SiC MOSFET become more convenient and have been receiving great research interests.

In behavioural models, the non-linear interelectrode capacitances require accurate modelling or fitting in order to accurately characterize the fast switching transient. Ref. [8] mainly describes the nonlinear gate-to-drain capacitance C_{gd} with a modified switch-model capacitor based on the "switch model" of SIEMENS. The effect of negative gate drive voltage on the gate-to-source C_{gs} capacitance was particularly discussed in [9, 10]. The three nonlinear interelectrode capacitances are meticulously modelled and the nonlinearity of the drain-to-source capacitance is studied in detail [11, 12]. Customized formulas were used to model the gate-to-drain miller capacitance [13, 14]. In most models [11, 13–15], only a junction capacitance of the SiC MOSFET body diode is used to model the drain-to-source capacitance C_{ds}, which is prone to inaccuracy. Ref. [15] uses empirical formulas to describe C_{gd} by hyperbolic tangent and arctangent functions, which greatly improves the simulation convergence. Further C_{gd} and C_{ds} fitting improvement is presented in [16–19]. In the latest publications, efforts are

constantly made to improve the SiC model to consider ultralow turn-off losses precisely in the condition of small driver resistance and small load current [20, 21]. To balance the trade-off between accuracy and efficiency, analytic models for more accurate switching loss prediction are developed in [22–24]. A universal SPICE model for field-effect transistors, independent from technology and semiconductor material, is developed in [25]. Through careful evaluation of model accuracy and run-time, specific recommendations for optimal implementations of interelectrode capacitances was offered in SPICE [26]. Comprehensive characterization of these non-linear interelectrode capacitances are carried out in [27] to develop accurate simulation models and to improve understanding of the device behaviour. As it can be seen, improvement for more accurate modelling of interelectrode capacitances is still the main pursuit for power electronic researchers and engineers.

More importantly, the influence of parasitics introduced by measurement probes is normally ignored for verification of SiC MOSFET modelling, which has been proven to introduce measurement errors and even worse, impedance-oriented transient instability [28–30]. The critical parametric inaccuracies and the measurement errors will considerably undermine the evaluation of the SiC MOSFET models. At present, coaxial shunts are widely used to measure the current of SiC MOSFET with a demanded wide bandwidth. Ref. [28] measured the parasitic inductance of the coaxial shunt power loop and the measurement loop, and provided its equivalent circuit. Refs. [29, 30] provided experimental evidence that voltage probes mainly contribute to the potential instability and the measurement delay mainly caused by additional stray elements of the coaxial shunt is very comparable to the fast switching duration of SiC MOSFET.

In this paper, an improved SiC MOSFET SPICE model is proposed developed by the EKV MOSFET model. Both static characteristics and interelectrode capacitances of SiC MOSFET from Wolfspeed C2M0080120D are intentionally measured for the proposed model. Non-linear interelectrode capacitances are carefully modelled and verified by simple self-made high-voltage C–V measurement systems. Both the non-linear gate-to-drain capacitance and drain-to-source capacitance fitting are optimized. In this way, the capacitance fitting at the inflection point that has a great impact on the switching delay is much improved. Furthermore, the parasitic parameters of the current measurement loop are accounted for better evaluation of the proposed SiC MOSFET model. The improved model is implemented in LTspice circuit simulation. In order to verify the accuracy of the proposed SiC MOSFET SPICE model, a double pulse test is built. The simulation results are in excellent agreement with the experimental results under different operating voltage and current conditions.

2 | IMPROVED SPICE MODEL FOR THE SIC MOSFET

Figure 1a shows the cross section of one cell in a SiC MOSFET. The main dielectrics for inducing interelectrode capacitances are the depletion layer formed in the N-region and the gate oxide. These capacitances including C_m, C_{oxs}, C_{oxc} and C_{oxd} arising from the gate oxide have nearly constant values, irrespective of the gate voltage applied across it. C_c is dependent on the depletion layer under the gate. However, the capacitances (C_{gdj} and C_{dsj}) resulted from the depletion layer will change with the applied drain voltage across it. The capacitance components that reside in the SiC MOSFET are integrated into the interelectrode capacitances C_{gs}, C_{gd}, and C_{ds}:

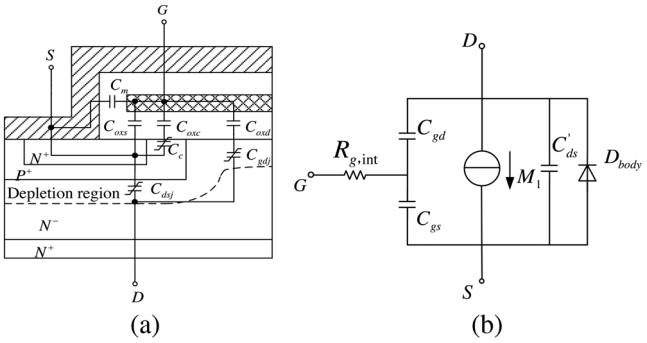

FIGURE 1 The structure and model of SiC MOSFET. (a) Cross section of a MOSFET cell. (b) Behavioral model of SiC MOSFET

$$\begin{cases} C_{gs} = C_m + C_{oxs} + \dfrac{1}{1/C_{oxc} + 1/C_c} \\ C_{gd} = \dfrac{1}{1/C_{oxd} + 1/C_{gdj}} \\ C_{ds} = C_{dsj} \end{cases} \tag{1}$$

The typical SiC MOSFET behavioural model can be shown in Figure 1b. The model contains the voltage control current source M_1 used to describe the lateral MOS channel, the body diode D_{body}, the internal gate resistance $R_{g,int}$, and the interelectrode capacitances Cgs, Cgd, and C_{ds}'. In addition, the critical parasitic package inductance at the drain terminal L_d, at the source terminal L_s and at the gate terminal L_g, all of which can be measured with a network analyser based on two-port S-parameters measurement [31].

2.1 | Static characteristics modelling of SiC MOSFET

M_1 and $R_{g,int}$ are used to describe the static characteristics of SiC MOSFET. The internal gate resistance $R_{g,int}$ is 4.6 Ω as provided in the datasheet of Wolfspeed C2M0080120D [38]. The traditional Shichman–Hodges model is adopted in [8, 10, 15]. Although the simulated curves seem to match closely with those in the datasheet, the model has a smaller number of coefficients for adjustment. Thus, its accuracy under certain conditions is limited. According to [13, 32–33], the Enz–Krummenacher–Vittoz (EKV) model is able to predict MOSFET static behaviours all over the weak, moderate and strong inversion regions with a single expression. Compared with models in [10–15], its parameter extraction process is more straightforward.

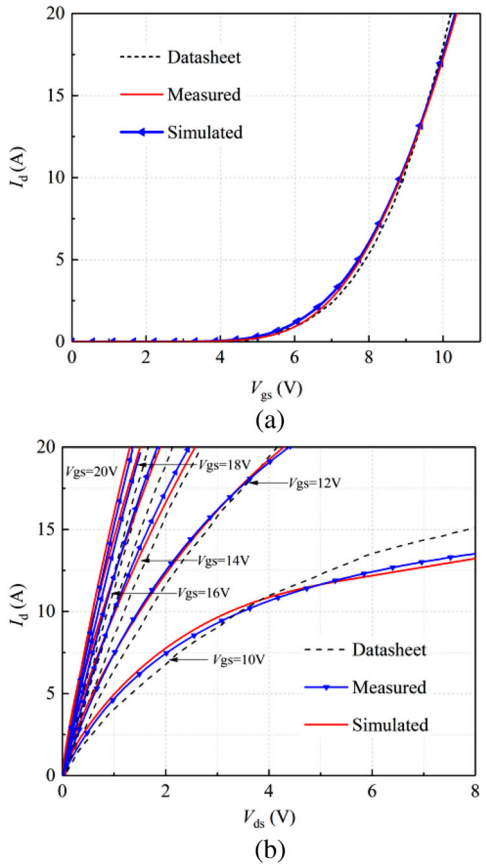

FIGURE 2 Static characteristic curves comparisons at 25 °C. (a) Transfer characteristic. (b) *I–V* Output characteristic

Here, we still use the improved EKV model proposed in [32, 33] to describe M_1. The drain current I_d is determined by the drain-to-source voltage V_{ds} and the gate-to-source voltage V_{gs}, as shown in Equation (2). For the transfer characteristic curve and output characteristic curves, a comparison between the measured results using Agilent B1505A Power Device analyser/curve tracker and the datasheet curves is shown in Figure 2. It can be clearly seen that measured data have appreciable discrepancies with those in the datasheet. In Figure 2b, the differences between measured and datasheet's *I–V* curves differ greatly. Therefore, the fitting coefficients in Equation 2 must be extracted according to the measured data, as shown in Table 1 of the Appendix. The simulation curves are compared with the measured curves as shown in Figure 2. It can be found that, at different V_{gs}, the simulation static characteristic curves match accurately with the measured curves:

$$I_d = 2g_m\phi_t^2 k_s \left\{ \left[\ln\left(1 + e^{\frac{(V_{gs}-V_{th})}{2k_s\phi_t}}\right)\right]^k - \left[\ln\left(1 + e^{\frac{(V_{gs}-V_{th})-nV_{ds}^a}{2k_s\phi_t}}\right)\right]^k \right\} (1 + \lambda V_{ds}) \quad (2)$$

TABLE 1 Parameters in EKV model

Parameters	Description	Value
g_m	Transconductance	0.6585
ϕ_t	Thermal voltage	0.7802
K_s	Sub-threshold slope parameter	0.6468
V_{th}	Threshold voltage	5.4084
k	Law exponent	1.9669
λ	Channel lengthmodulation parameter	0.0357
n	Triode region parameters	1.3048
a	Triode region parameters	0.7929

2.2 | Dynamic characteristics modelling of SiC MOSFET

The three non-linear interelectrode capacitances C_{gs}, C_{gd}, C_{ds} and body diode D_{body} play an important role in describing the dynamic characteristics. These interelectrode capacitances of SiC MOSFET determine the switching waveforms and oscillation of the device, so it must be accurately modelled. Therefore, an accurate C-V characterization system of SiC MOSFET under different operating voltages is the foundation of device modelling.

These three measurement circuits are developed to measure the *C–V* curve of C_{ds} (contain the junction capacitance of D_{body}), C_{gd} and C_{gs} respectively as shown in Figure 3. A voltage bias is added between drain and source of SiC MOSFET in Figure 3a. In Figure 3b, the gate of the SiC MOSFET is grounded by a large resistor R_3, which can be seen as a voltage bias between the drain and the gate. A voltage bias is applied between the gate and source of a SiC MOSFET in Figure 3c. They are connected to the impedance analyser E4990A respectively so as to obtain three sets of *C–V* curves following a similar operating principle in [34]. In the C_{gs} measurement circuit as shown in Figure 3a, $R_{1,3} = 78\ \text{k}\Omega$ and $C_{2,3} = 1000$ pF form a low-pass filter with a cut-off frequency of 2 kHz. $R_{2,4} = 39\ \text{k}\Omega$ is to prevent excess current. $C_1 = 1\ \mu$F is the high voltage capacitor, to isolate the AC part and the DC part. $L_1 = 1$ mH allows DC signal to pass through while blocking small AC signal. $C_4 = 1\ \mu$F enables small signals through C_{gc} and C_{ge} to flow to the ground, ensuring that only AC current through C_{ce} can be collected by the impedance analyser. The zener diode 1N4739 $ZD_{1,2}$ and the rectifier diode 1N4004 $D_{1–10}$ are used to protect the measuring terminals of the impedance analyser from overvoltage. Compared with [34], the circuit in this paper saves several protection diodes and a high voltage capacitor. The device parameters in Figure 3b,c are the same as those in Figure 3a. The diodes in the measurement circuit are used to protect the measuring instrument from overvoltage. Three simple high-voltage measurement circuits as shown in Figure 4a–c are self made. Figure 4d shows the experimental platform and self-made circuit boards for measuring the interelectrode capacitances. The measured curves for the interelectrode capacitances are presented in Figure 5.

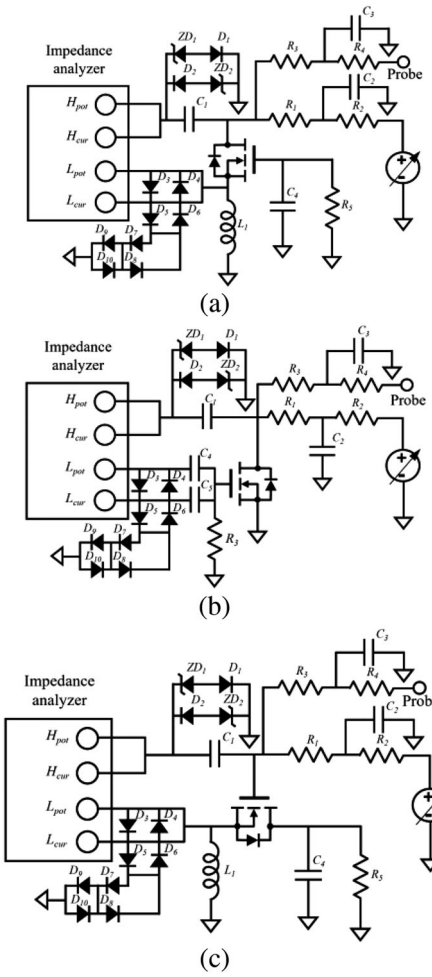

FIGURE 3 The schematic for interelectrode capacitance measurement. (a) The PCB for measuring C_{gs}. (b) The PCB for measuring C_{gd}. (c) The PCB for measuring C_{ds}

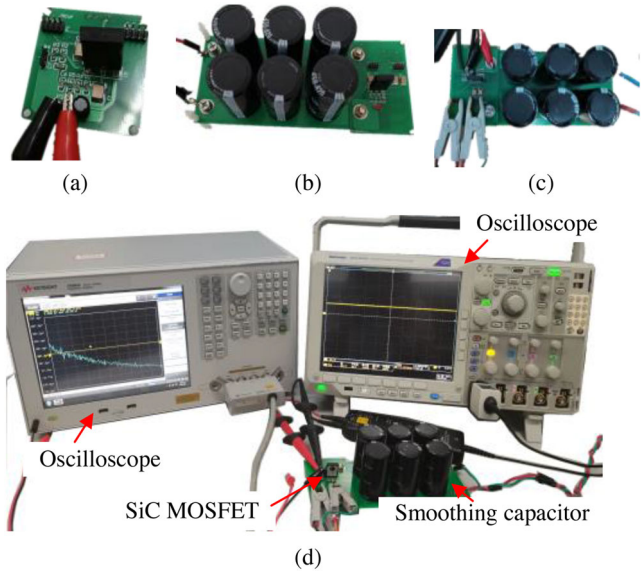

FIGURE 4 Test platform. (a) The PCB for measuring C_{gs}. (b) The PCB for measuring C_{gd}. (c) The PCB for measuring C_{ds}. (d) Test layout

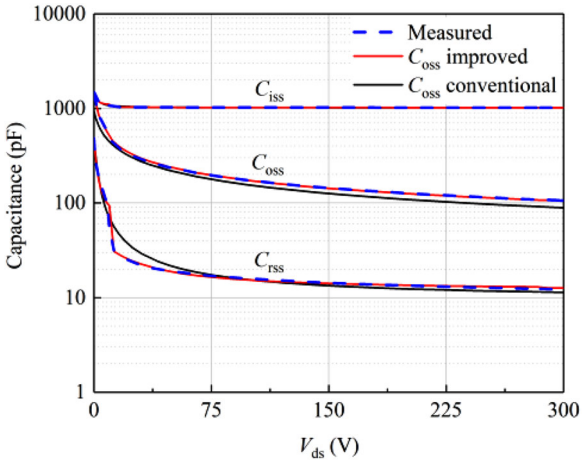

FIGURE 5 Values of terminal capacitances in relationship with the drain–source voltage. Adding the inflection point to the graph

Considering the influence of negative V_{gs}, C_{gs} can be modelled by the hyperbolic tangent function proposed in [15]:

$$C_{gs} = 0.5C_{gsm}(1 - \tanh(V_{gs})) + C_{gs\,\min} \tag{3}$$

where C_{gsmin} is the gate-to-source capacitance at which V_{gs} is positive. C_{gsm} is the gate-to-source capacitance increment when the V_{gs} is negative.

The variable capacitance can be implemented using a voltage controlled current source [14–16], where C is the expression of curve-fitted functions and V is the voltage on the capacitance. This variable capacitance model is widely-used in SiC MOSFET modelling as it can avoid the risk of non -convergence.

C_{gd} is formed by the series connection of the oxide capacitance C_{ox} and the depletion region capacitance C_{gdj} as mentioned. When the drain voltage is forward biased and V_{gs} is greater than the threshold voltage, the miller capacitance is physically C_{ox}, representing the maximum value of C_{gd}. As the drain voltage increases and V_{gs} is below the threshold voltage, the depletion region expands and C_{gdj} decreases correspondingly. The final C_{gd} is determined by the series of C_{ox} and C_{gdj}, representing the minimum value of C_{gd}. This can be clearly reflected in the C_{rss} curve of Figure 5.

When $V_{gd} < 0$, there are two different decay rates of C_{gd} with V_{ds} increasing, which forms a clear inflection point in the typical C_{rss} curve as shown in Figure 5. The inflection point is one of the main contributors to the switching transients as it directly determines the gate delay of switching behaviours. A single mathematical function can have difficulties in simulating such a change in the capacitance here [15]. To achieve as good fitting as possible, this paper separates the C_{gd}–V_{ds} curve into two parts at the inflection point and models the C_{gd} piecewise fitting. According to the measurement in Figure 4, the decaying rate changes when V_{ds} is approximately equal to 10 V. The capacitance C_{gd} model with $V_{gd} < 0$ is divided into two parts,

and the improved fitting formula is shown as:

$$C_{gd} = \begin{cases} \mathrm{A}\tanh(GV_{gd}) + \mathrm{B} & V_{gd} > 0 \\ \mathrm{Catan}(GV_{gd}) + \mathrm{D} & -10 < V_{gd} < 0 \\ \mathrm{Eatan}(HV_{gd}) + \mathrm{F} & V_{gd} < -10 \end{cases} \quad (4)$$

where A, B, C, D, E, F, G and H are all constants, $V_{gd} = -V_{ds}$.

The junction capacitance C_j of the body diode and C_{ds} are both depletion layer capacitances at the PN junction of the P+ region and the N-region. Previously, most conventional works only employ C_j as Equation (5) to describe C_{ds}. However, the junction capacitance of the SiC MOSFET body diode cannot represent the actual C_{ds} during the MOSFET switching. An auxiliary capacitance C_{ds}' is introduced to correct the C_{ds} curves, which can improve the C_{ds} modelling [18]. The C_{ds}' is obtained by fitting the difference between C_{ds} and C_j. The fitting expression is shown as Equation (6).

$$C_j = C_{j0}\left(1 - \frac{V_D}{V_J}\right)^{-m} \quad (5)$$

$$C'_{ds} = C_{ds} - C_j = \frac{p_7(V_{ds})^{1.5} + p_5 V_{ds} + p_3(V_{ds})^{0.5} + p_1}{p_8(V_{ds})^2 + p_6(V_{ds})^{1.5} + p_4 V_{ds} + p_2(V_{ds})^{0.5} + 1} \quad (6)$$

The simulated results compared with the measured curves for V_{ds} of 0–300 V is shown in Figure 5. Compared with the curves of conventional C_{oss} ($C_{oss} = C_{gd} + C_{ds}$) simulated model, the improved simulated model better match with the measured curves, especially for reverse transfer capacitance C_{rss}. The gate-to-drain capacitance fitted by Equation (4) follows perfectly to the measured data, especially near the inflection point. The accuracy of the proposed method can also be verified.

2.3 | Circuits for parasitics in current measurement loop

Due to the fast switching characteristics, a wide-bandwidth coaxial shunt is normally utilized to capture the fast current transients. However, using such a coaxial shunt to measure current, additional stray elements will be introduced to the measurement loop. As shown in Figure 6, a parasitic inductance will be introduced to the main power processing loop, which is in series connection with the coaxial shunt resistor R_{shunt} contributed by the inner and outer coaxial conductor [35, 36]. Another parasitic inductance is introduced to its output side. A SSDN-005(400 MHz) coaxial shunt from T&M Research Products Inc. is used here, whose electrical specifications of parasitics are shown in Figure 6. The coaxial shunt is then connected to the oscilloscope by a coaxial cable with BNC connecters. The coaxial cable demonstrated a typical property of transmission line, which can be presented by a line-parameter model as shown in Figure 6. The parasitic parameters of the equivalent

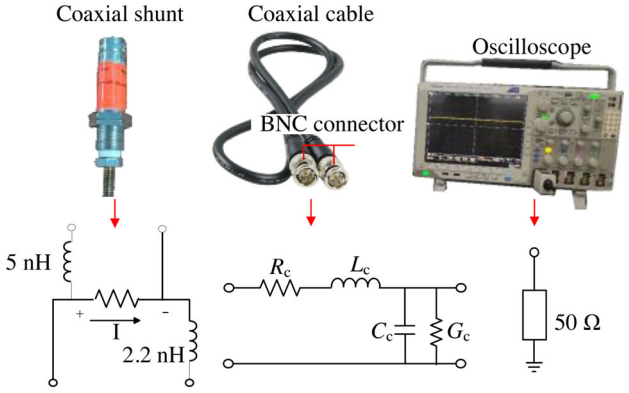

FIGURE 6 The model of the coaxial shunt current measurement loop

circuit of a coaxial cable per unit length are shown in Equation (7) [37]. Rc, Lc, Gc, and Cc represent the primary resistance (Ω/m), inductance (H/m), conductance (S/m) and capacitance (F/m) per unit length, respectively:

$$R_c = \sqrt{\frac{f\mu_1}{4\pi\sigma_1}}\left(\frac{1}{a} + \frac{1}{b}\right)$$

$$L_c = \frac{\mu}{2\pi}\ln\left(\frac{b}{a}\right)$$

$$C_c = \frac{2\pi\varepsilon}{\ln\left(\frac{b}{a}\right)} \quad (7)$$

$$G_c = \frac{2\pi\sigma}{\ln\left(\frac{b}{a}\right)}$$

where a is radius of the inner conductor, b is inner radius of the outer conductor. μ, ε, and σ are the permeability, permittivity, and conductivity of the dielectric filled between the inner and outer conductors, respectively. μ_1 and σ_1 are the permeability and conductivity of the inner and outer conductors.

The input resistor of the oscilloscope is chosen to be 50 Ω to match the impedance of the current measurement loop. Finally, the parasitic model of the overall shunt current measurement loop (including the coaxial shunt, coaxial cable and oscilloscope) can be built as shown in Figure 7 a, which can be integrated into a device simulation model of a double-pulse test circuit.

3 | COMPARISONS OF EXPERIMENTAL AND SIMULATION RESULTS

The simulation circuit is implemented in LTspice in Figure 7b. The simulation circuit for the current measurement loop is also built. The rise and fall time of the drive voltage V_g are considered, which can be regarded as about 10 ns. The switching loop inductance L_{loop} is calculated from the turn-off switching oscillation frequency. V_{DC} is the DC bus voltage, R_{shunt} is the

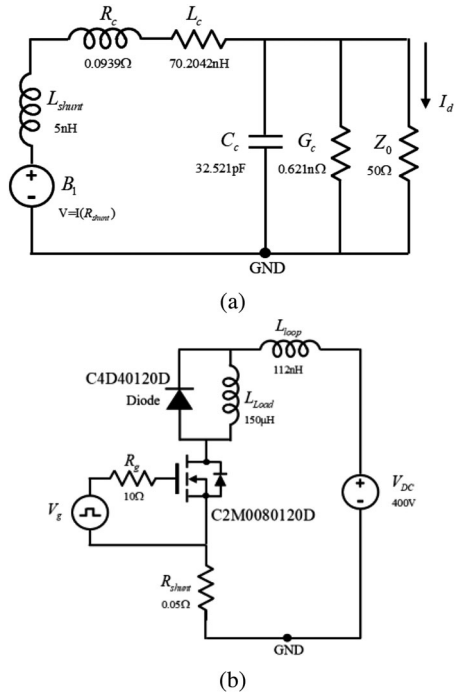

FIGURE 7 (a) The simulation circuit of the measurement loop of the coaxial shunt

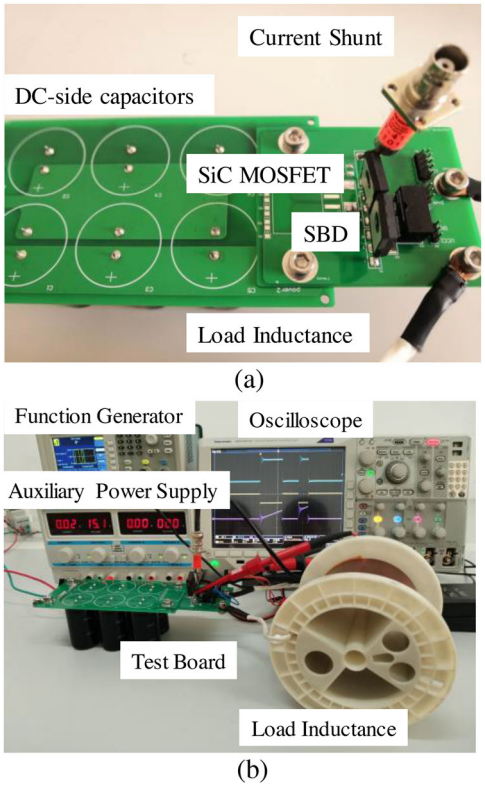

FIGURE 8 Double pulse test platform. (a) Circuit board. (b) Platform layout

coaxial shunt inner resistor, which is connected in series with the SiC MOSFET. B_1 is the voltage on R_{shunt}, L_{shunt} is the parasitic inductance of coaxial shunt, Z_0 is the input resistance of oscilloscope, which is 50 Ω for impedance matching as mentioned in Section 2.3. It should be noted the simulated I_d is on the current measurement loop as shown in Figure 7 a, instead of the drain current through the SiC MOSFET.

To verify the SiC MOSFET SPICE model proposed in Section 2, a typical double pulse test platform is built. Tests are completed at a room temperature of 25 °C. Figure 8 is the photograph of the test platform. The SiC MOSFET used here is CREE C2M0080120D (1200 V, 36 A) and the diode is CREE C4D40120D (1200 V, 54 A). The gate driver is 1EDI60N12AF from Infineon. The gate drive voltage is 20 V/−5 V. The external gate resistance R_g is 10 Ω and a self-made 150 μH air inductor L_{load} is used as the load. The high-speed switching transients of the SiC MOSFET require that the measurement equipment should have sufficient bandwidth to capture the fast rise and fall edges of the switching waveforms. The effective bandwidth of the measurement system is determined by the bandwidth of the oscilloscope and the bandwidth of the probe. The used oscilloscope is MDO4054C (500 MHz) from Tektronix. The voltage probe THDP0200 (1500 V/150 V, 200 MHz) is used to measure V_{ds}, and THDP0200 (6000 V/600 V, 100 MHz) is used to measure the drain–source voltage V_{gs}. A SSDN-005 (400 MHz) coaxial shunt is used to measure the drain current I_d. All the experiments are carried out at room temperature, as the temperature characteristics are not concerned in this study.

To start with, the line characteristics resulted by the coaxial cable is investigated as the length of coaxial cables would affect the I_d measurement results. Three different cables with different lengths are used and connected into the measurement loop respectively to capture the current transients of SiC MOSFET switching. It can be seen that there are appreciable measurement delays between the results of three different cables at both turn-on and turn-off in Figure 9. The measurement delays of I_d waveform measured by the 0.3 m-in-length and 0.5 m-in-length coaxial cables is significantly greater than that of the 0.15 m-in-length coaxial cable. As the length of the coaxial cable increases, the phase delay of I_d increases. The greatest difference occurs at the turn-off as shown in Figure 9a, reaching 6 ns. It should be noted that the overall fall time of I_d is only 20 ns. In other words, the line property of the measurement loop can considerably affect the accuracy of the measured switching transient of SiC MOSFET. Therefore, the influence of the current measurement loop to the device modelling ought to be considered.

Figure 10 shows the measurement waveforms, the simulation waveforms of the improved model (presented in Section 2) and the simulation of the unimproved model at turn-off and turn-on, respectively. The unimproved model (improved fitting of C_{oss}) is presented in [18] without considering the influence of current measurement loop, which is developed by fitting the datasheet curves. It can be seen that the simulation with the improved model matches the experiment results much better than the simulation with the unimproved model, especially for turn-off where the SiC MOSFET modelling dominates. The ringing amplitude of V_{ds} and I_d of the unimproved model is significantly lower than the experimental results, while the improved model show excellent agreement.

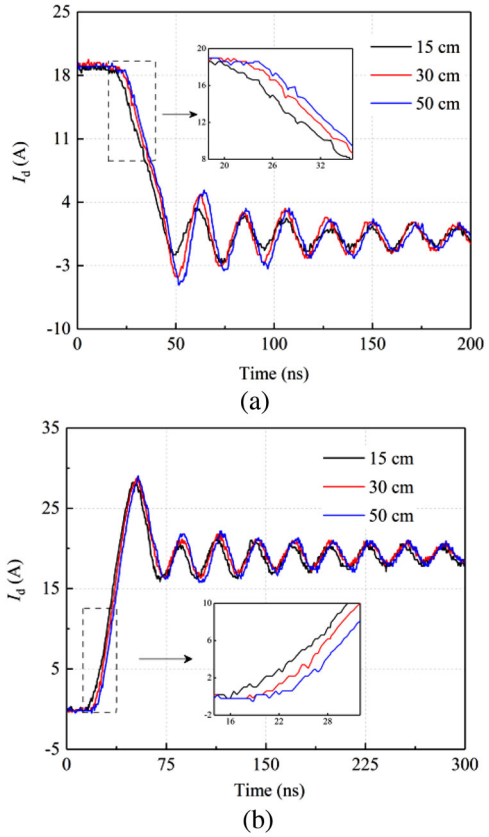

FIGURE 9 I_d waveforms measured by coaxial cables of different lengths. (a) Turn-off waveforms. (b) Turn-on waveforms

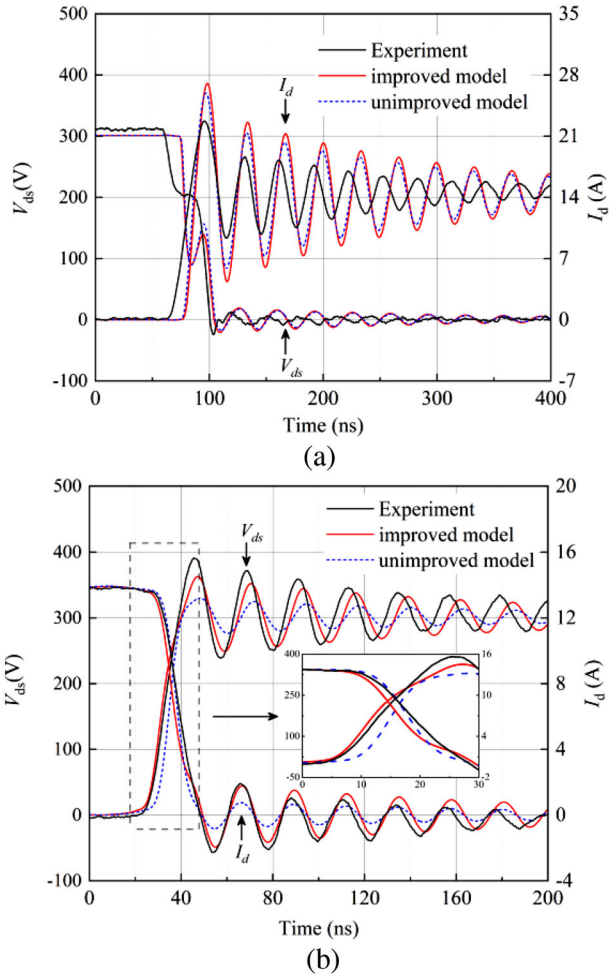

FIGURE 10 Comparisons of simulated and experimental waveforms of the improved model and unimproved model at 25 °C. (a) Turn-on waveforms. (b) Turn-off waveforms

This is mainly contributed by the interelectrode capacitance optimization described in Section 2.2. In addition, the I_d slope and switching delay time of the improved model are closer to the experiments, which is resulted by the addition of the coaxial shunt measurement loop model. Similar improvement can also be seen in Figure 10a for turn-on. The discrepancies are resulted by the imperfection of the diode model used in this paper.

In order to further verify the applicability of the model at different DC voltages, the DC side voltage is changed to 400 and 500 V in Figures 11 and 12. It can be seen that the simulation waveforms match closely with the experimental results at turn-off. Ringing at the simulated V_{ds} and I_d is almost in the same pace with the experimental result, which are contributed by accurate modelling of C_{gd} and C_{ds}. At turn-on, the improved model simulates nicely the ringing amplitude of V_{ds} and I_d, but there are slight deviations in the di/dt of I_d and the voltage drop of V_{ds}, which are also caused by the diode modelling, which is not optimized in this paper.

To verify the model under different gate resistance, double pulse test results when $R_g = 20\ \Omega$ are shown in Figure 13. It can be found that the V_{ds} simulation waveform can still be aligned nicely with the experimental waveform as previous results.

Twenty different operating conditions (DC-link voltage/switching current) are selected and tested to further validate the feasibility of the model under a variety of operation conditions.

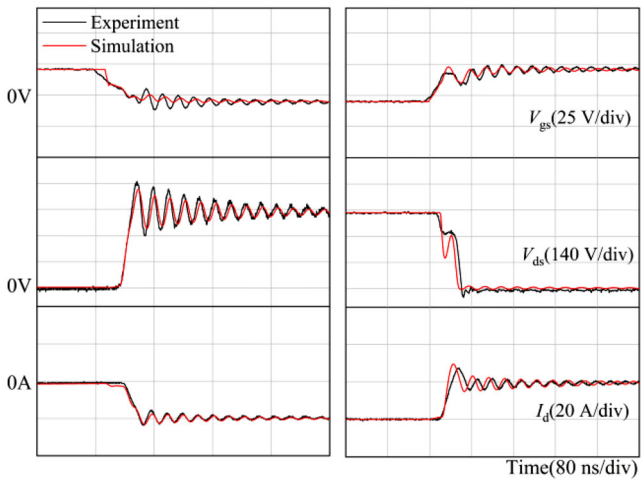

FIGURE 11 Comparisons of simulated and experimental waveforms when $V_{DC} = 400$ V, $I_d = 19$ A, $R_g = 10\ \Omega$, $V_{gs} = 20$ V/−5 V

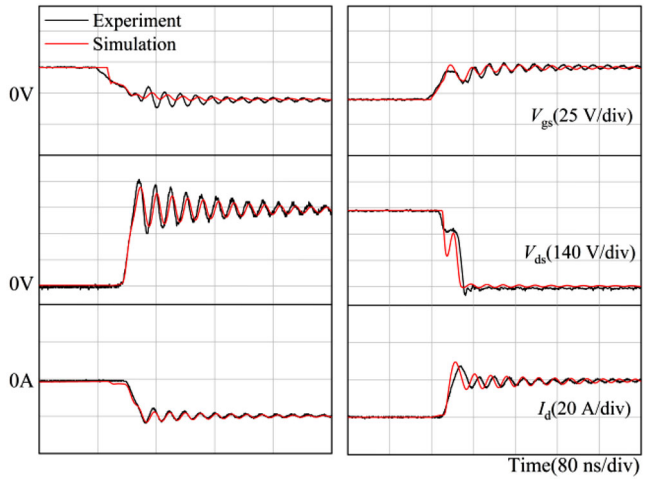

FIGURE 12 Comparisons of simulated and experimental waveforms when $V_{DC} = 500$ V, $I_d = 23$ A, $R_g = 10\ \Omega$, $V_{gs} = 20$ V/−5 V at 25 °C

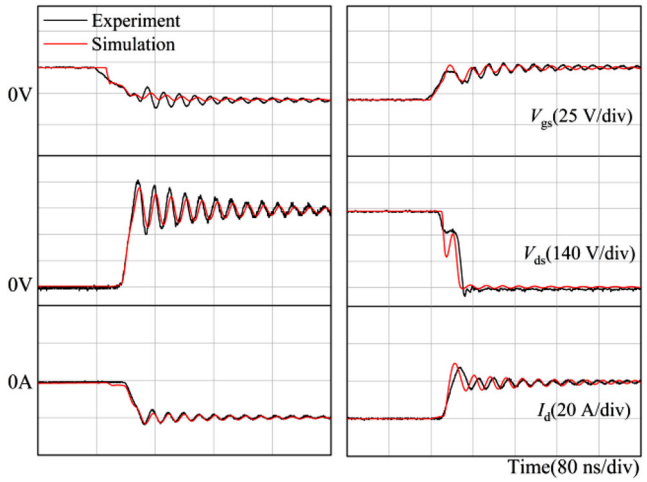

FIGURE 13 Comparisons of simulated and experimental waveforms at 25 °C. when $V_{DC} = 400$ V, $I_d = 19$ A, $R_g = 20\ \Omega$, $V_{gs} = 20$ V/−5 V

R_g is set to 10 Ω. The gate drive voltage is 20 V/−5 V. At the different levels of DC voltages, the switching power losses can be calculated by integral operation of voltage and current waveforms. It can be seen that at different DC voltages. The results are quite satisfactory in both turn-on and turn-off losses profile in Figure 14. At all test points, the switching power loss errors between simulation and tests are mostly less than 10% while the errors in [18] can reach as high as 29%. The results prove that the proposed SiC MOSFET model has very high accuracy on switching transient and power losses prediction.

In summary, for the switching waveforms and switching power loss at turn-off and turn-on, the improved model considering the influence of the current measurement loop shows an excellent agreement with the experimental results. All the parameters of the model are derived from measurement, including the state characteristic curves and interelectrode capacitances. The process of modelling is simple, fast and effec-

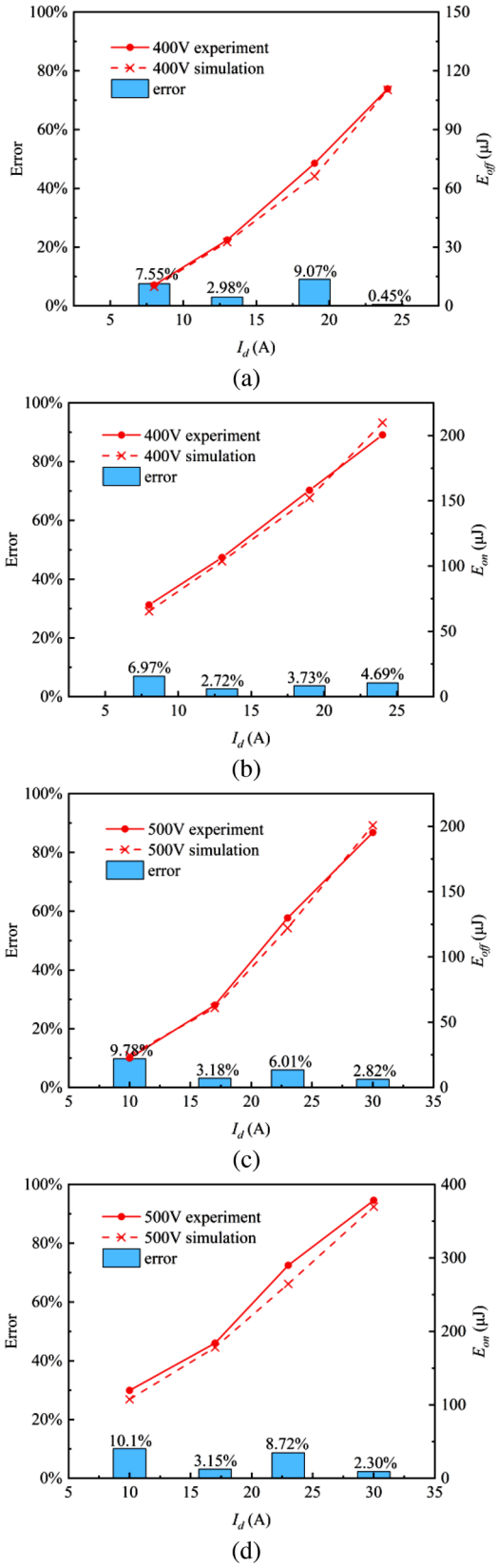

FIGURE 14 Comparisons between simulation and experiment of the switching losses for SiC MOSFET. (a) Turn-off loss at 400 V. (b) Turn-off loss at 400 V. (c) Turn-off loss at 500 V. (d) Turn-off loss at 500 V

tive. The proposed model with nice simulation convergence produced a reliable and accurate set of results.

4 | CONCLUSION

In this paper, an improved SiC MOSFET model driven by an empirical formula with three segments for the non-linear drain-to-gate capacitance in relationship with the drain–to-source voltage is developed. In this way, the capacitance fitting at the inflection point that has a great impact on the switching delay is much improved. The static characteristics and interelectrode capacitances of SiC MOSFET from Wolfspeed C2M0080120D are measured to verify the proposed formulation. Based on the EKV model, the static characteristics are modelled by fitting the measured static characteristic curves. Compared with the unimproved model, the improved model can represent the transient waveforms more correctly by optimized C_{gd} and C_{ds}, especially when MOSFET is turned off. More importantly, the critical parasitics of the current measurement loop are meticulously investigated. Experimental evidence shows that the greatest measurement delay resulted by the current measurement loop can occupy over 40% errors. In our proposed model, the I_d slope and switching delay time are closer to the experiments, which is contributed by the successful addition of the coaxial shunt measurement loop model. In this way, the proposed SiC MOSFET can be more accurately evaluated. Finally, a double pulse test platform is built to test the SiC MOSFET. The simulation waveforms and switching losses match closely with the experimental results under different operational conditions. The excellent results display that the improved model can provide an accurate modelling and verification approach.

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CONFLICT OF INTEREST

None.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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