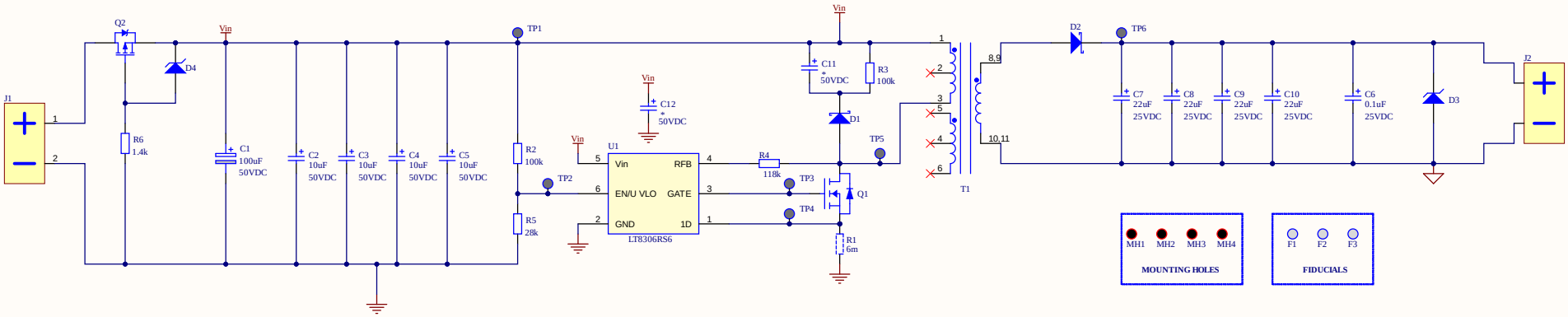
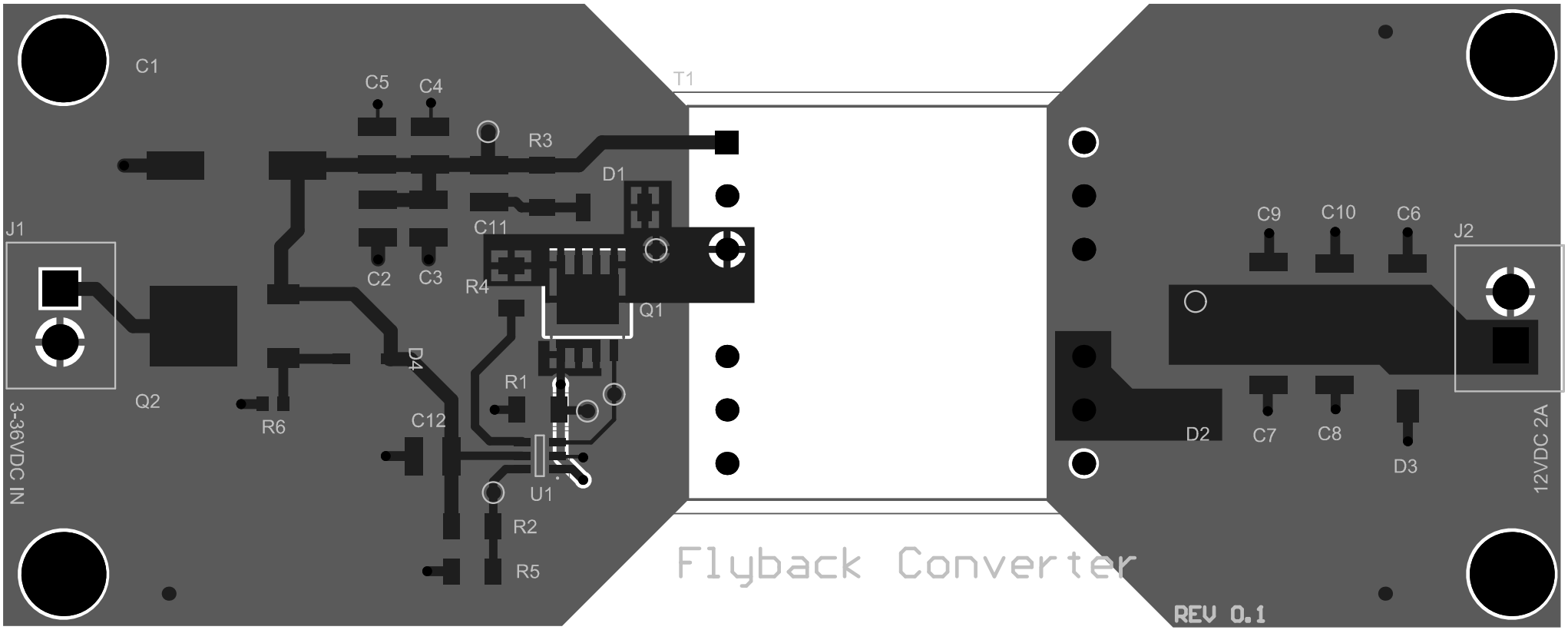


Title	**Flyback Converter**	
Size: B	Number: 1	Revision: 1.0
Date: 8/21/2024	Sheet 1 of 1	
File: D:\4 WORKSPACE\..\flyback.SchDoc	Drawn By: MOHAMED GUENI	


C1
C5
C4
T1
R3
D1
J1
C11
C9
C10
C6
J2
C2
C3
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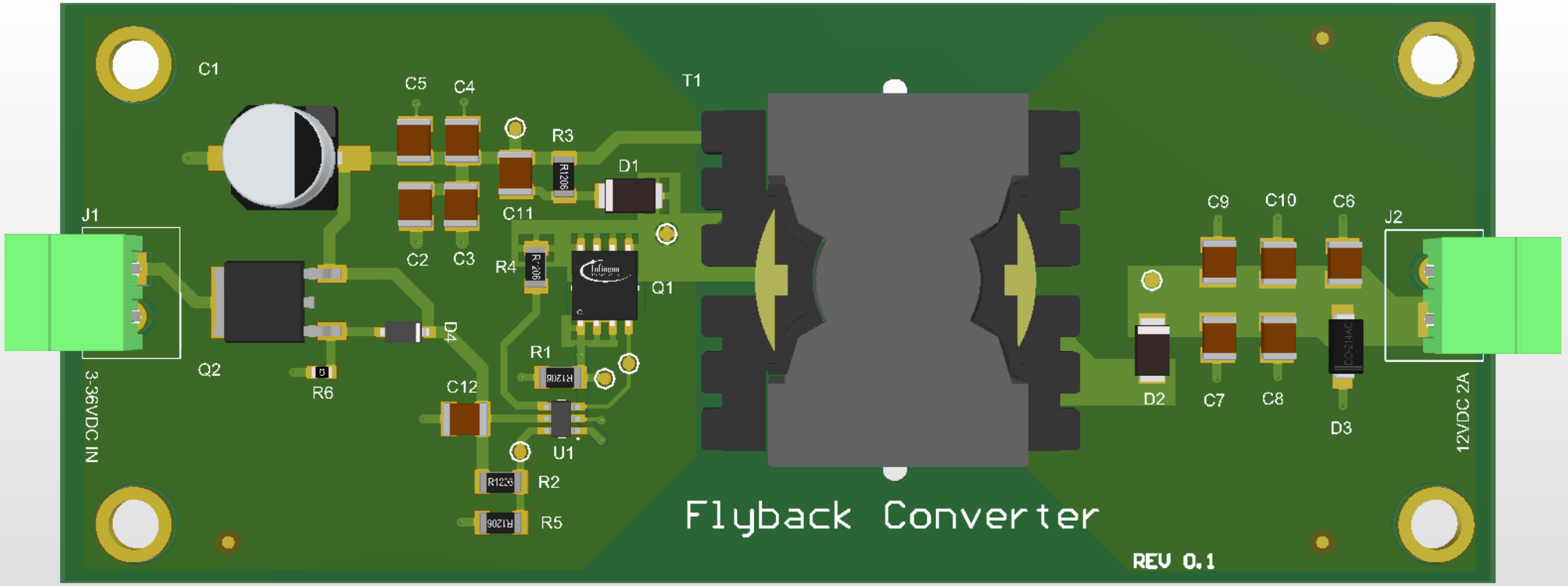
Q1
D4
R1
Q2
R6
C12
D2
C7
C8
D3
3-36VDC IN
12VDC 2A
U1
R2
R5
Flyback Converter
REV 0.1


C1
C5
C4
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R3
D1
J1
C11
C2
C3
R4
Q1
D4
Q2
R6
R1
C12
U1
R2
R5
C9
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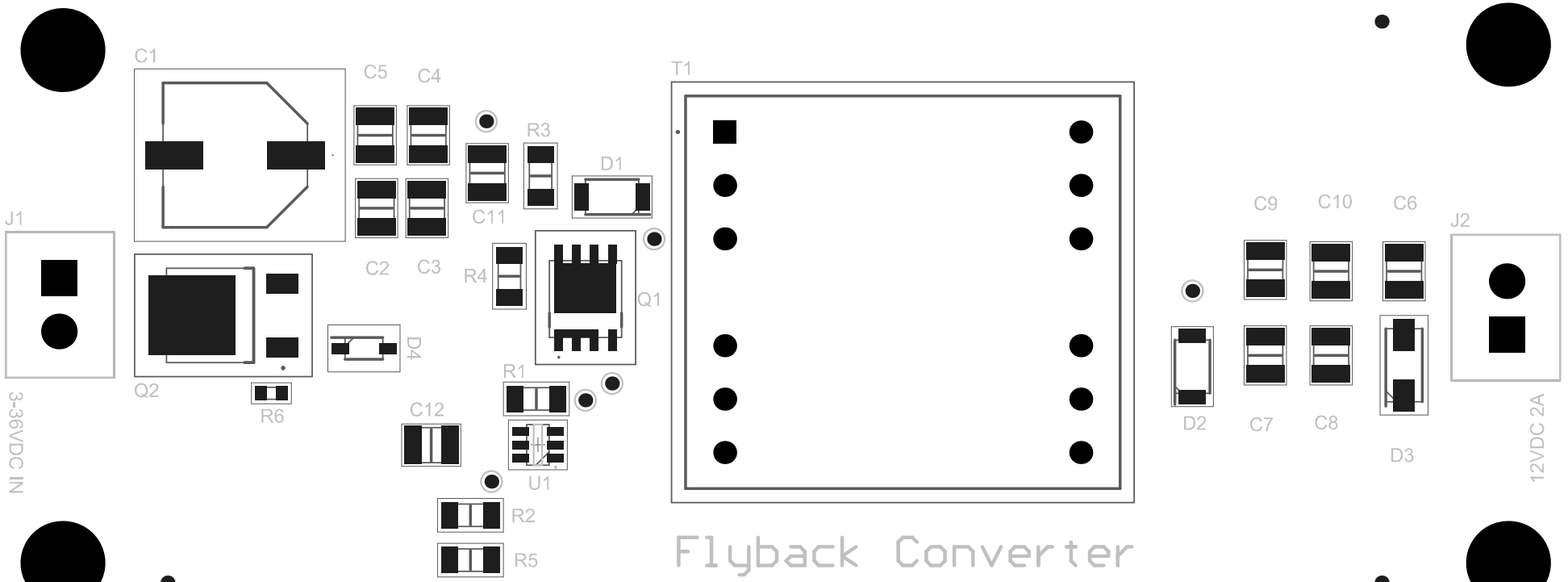
D3
3-36VDC IN
12VDC 2A
Flyback Converter
REV 0.1


C1
C5
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T1
R3
D1
J1
C11
C9
C10
C6
J2
C2
C3
R4
Q1
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D2
C7
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D3
U1
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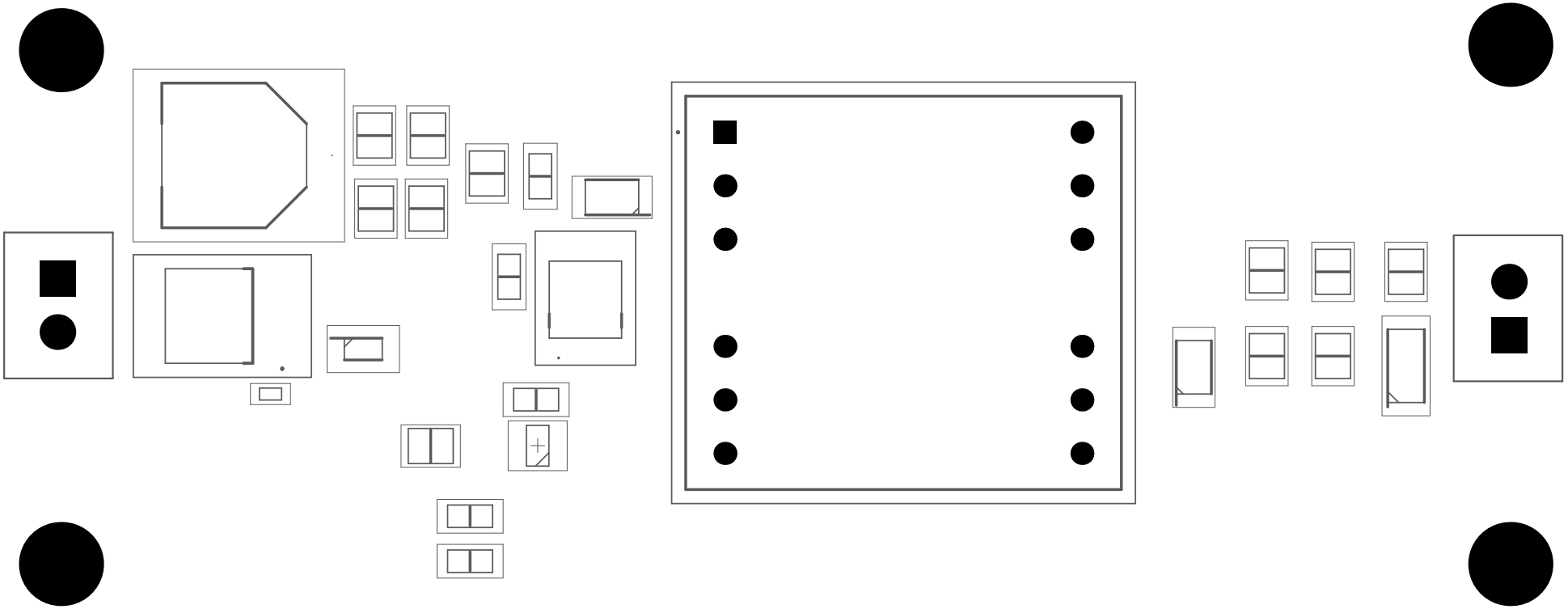
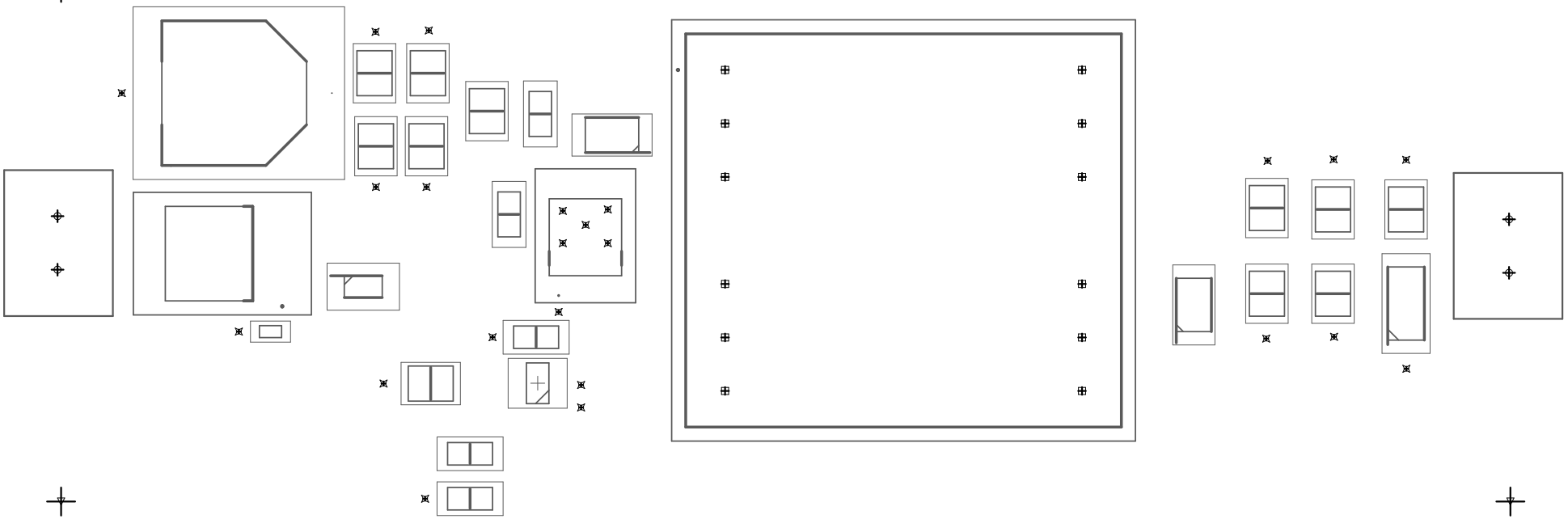
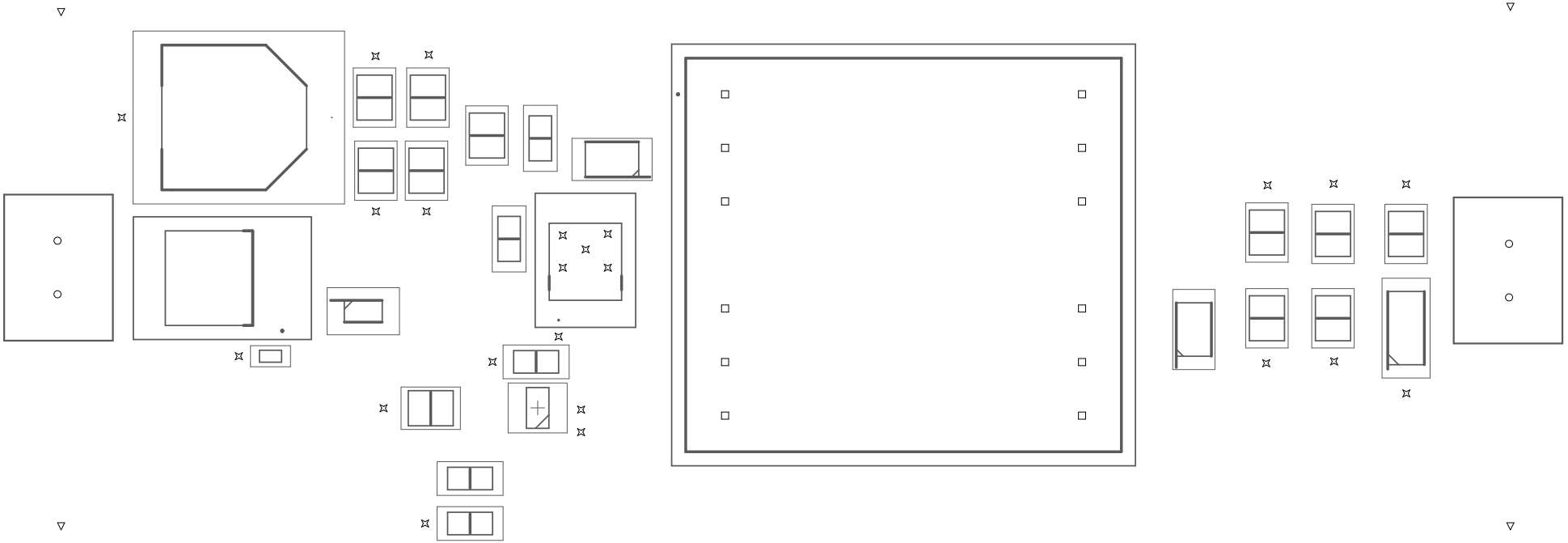
12VDC 2A
R2
R5
Flyback Converter
REV 0.1

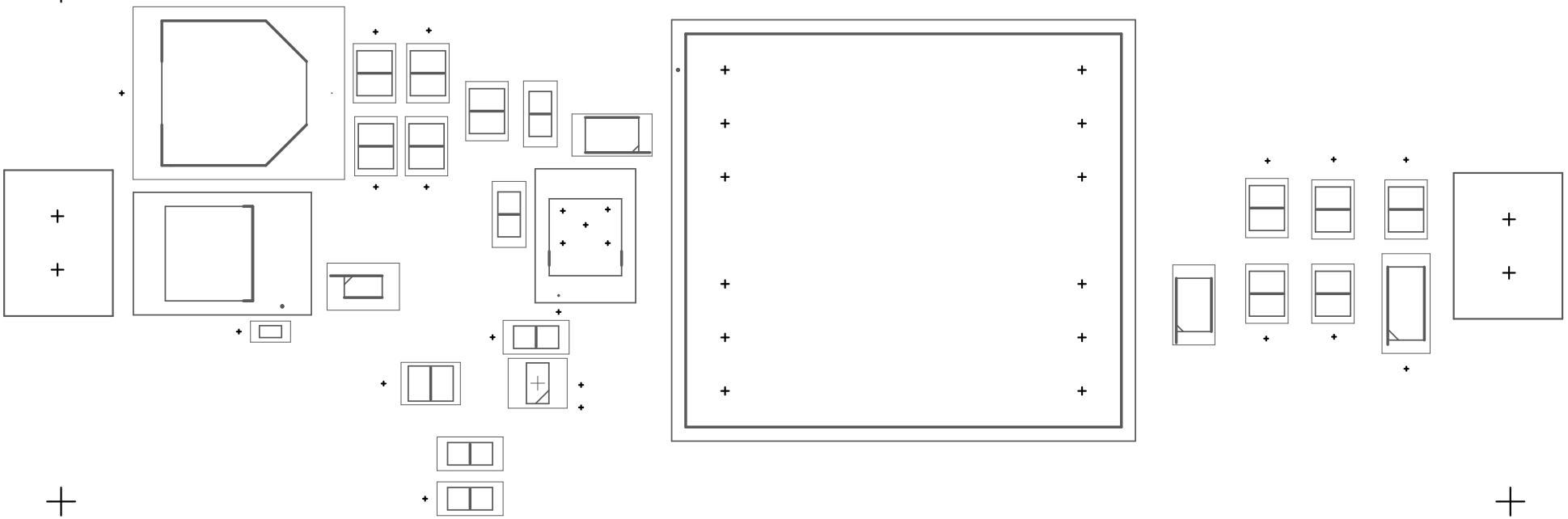


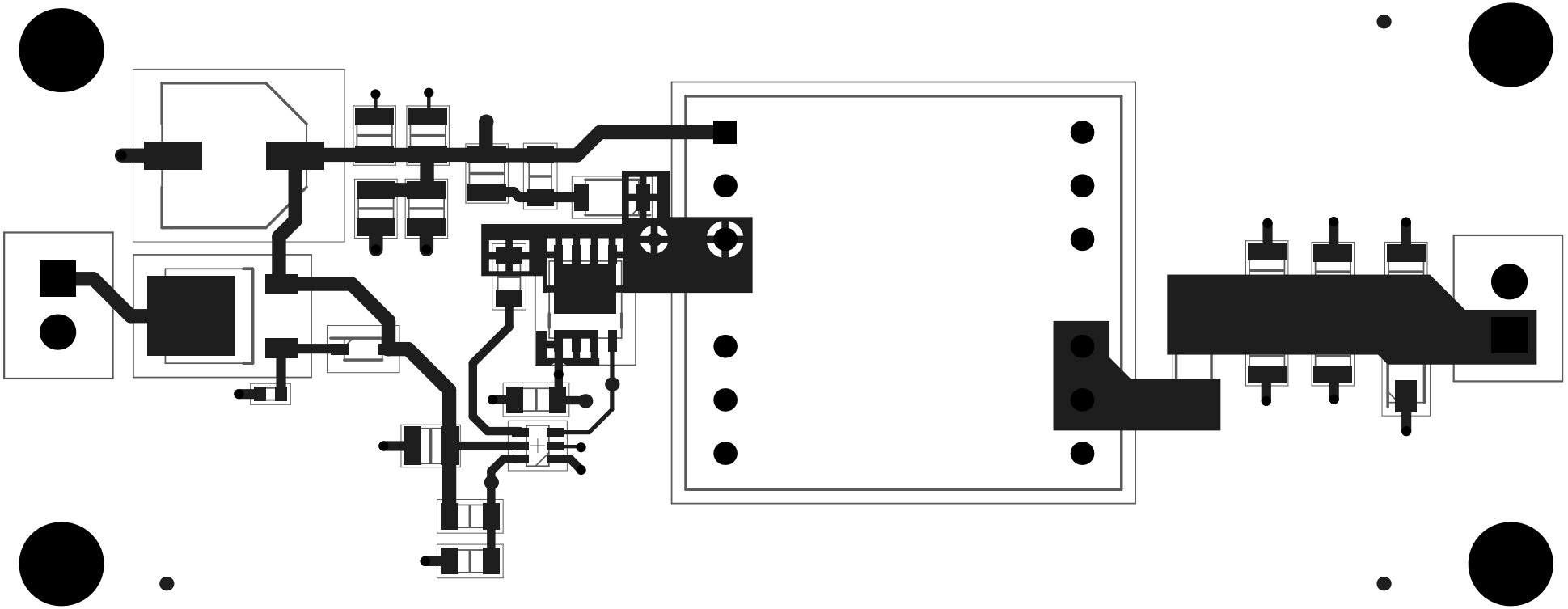
Board Stack Report

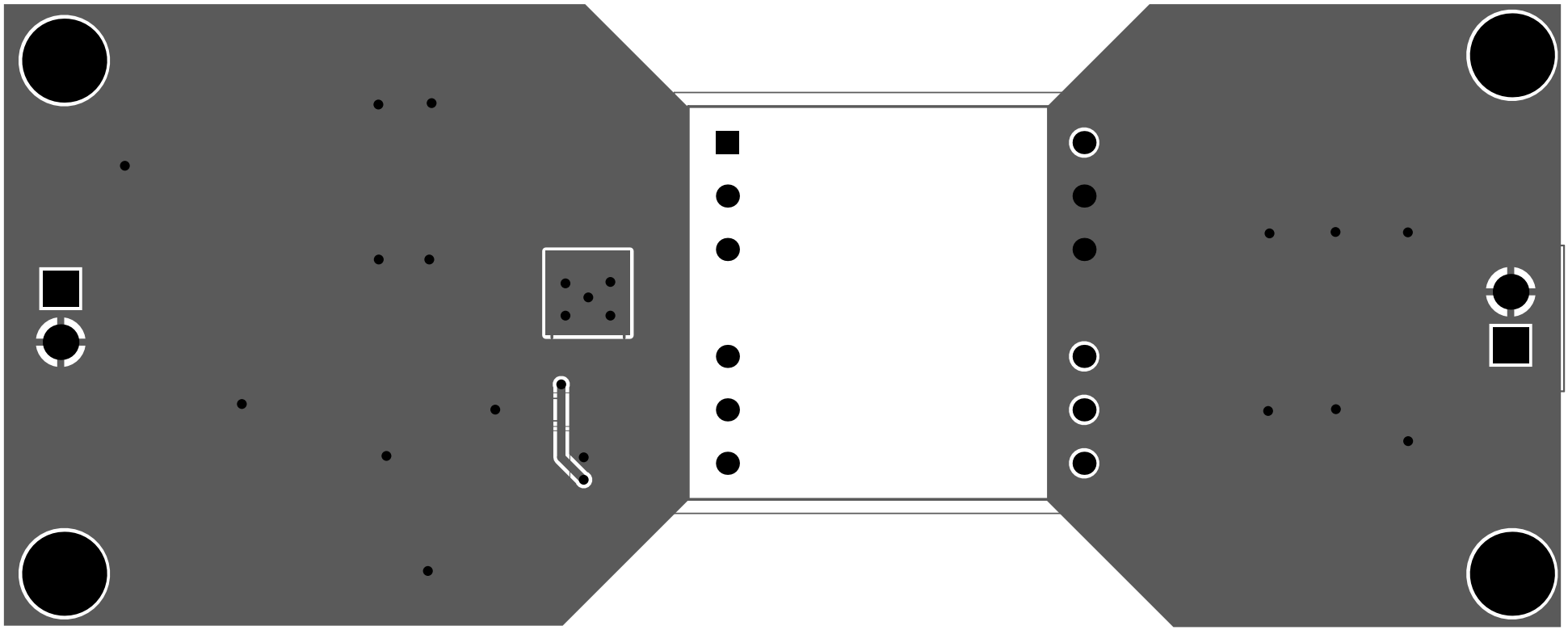
Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Overlay		0mil	
2		Top Solder	Solder Resist	0.4mil	3.5
3		Top Layer	CF-004	1.4mil	
4		Dielectric 1	Core-043	59mil	4.3
5		Bottom Layer	CF-004	1.4mil	
6		Bottom Solder	Solder Resist	0.4mil	3.5
7		Bottom Overlay		0mil	
	Height : 62.6mil				

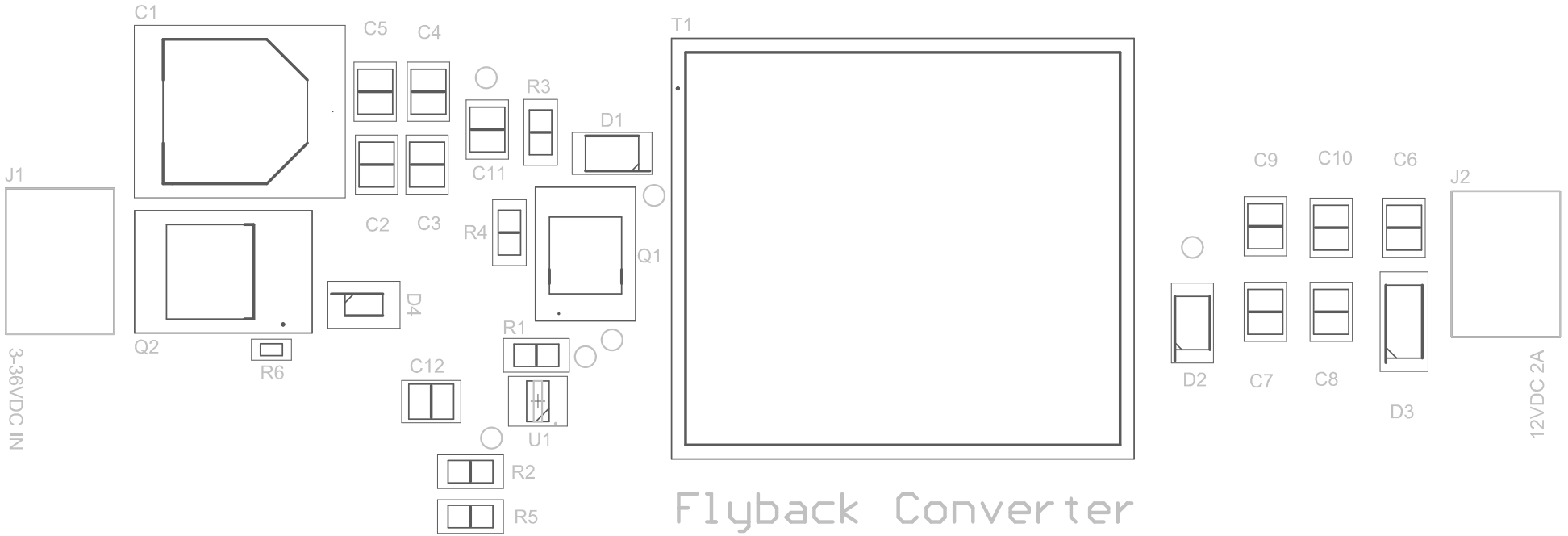


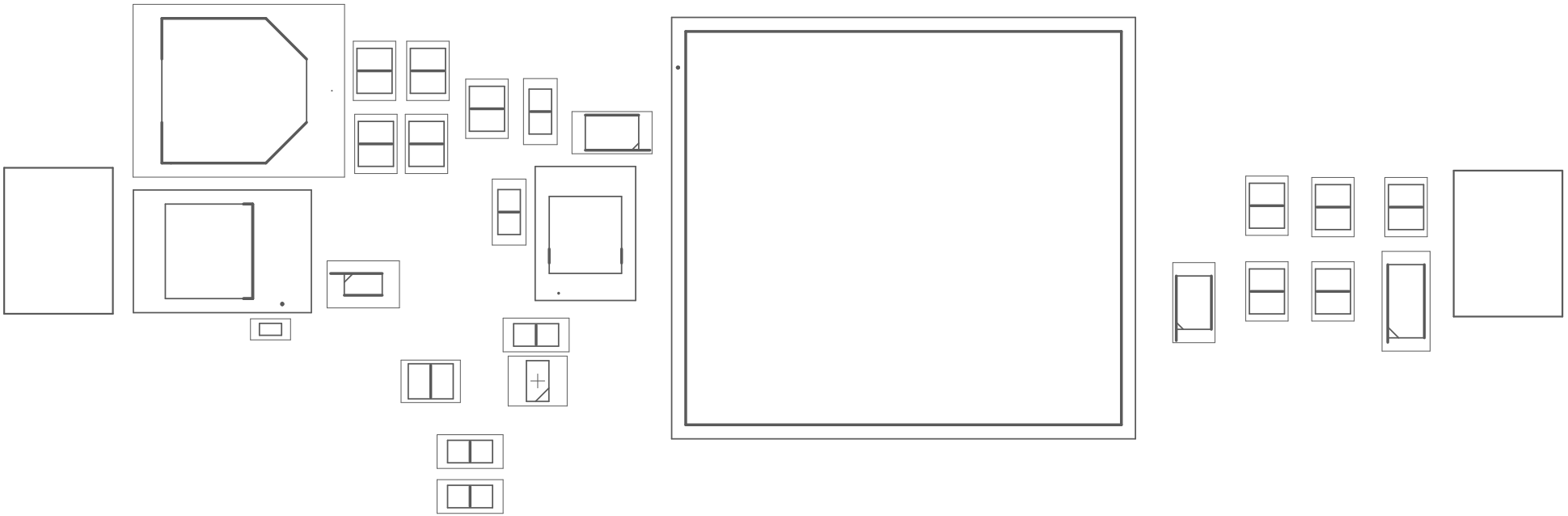


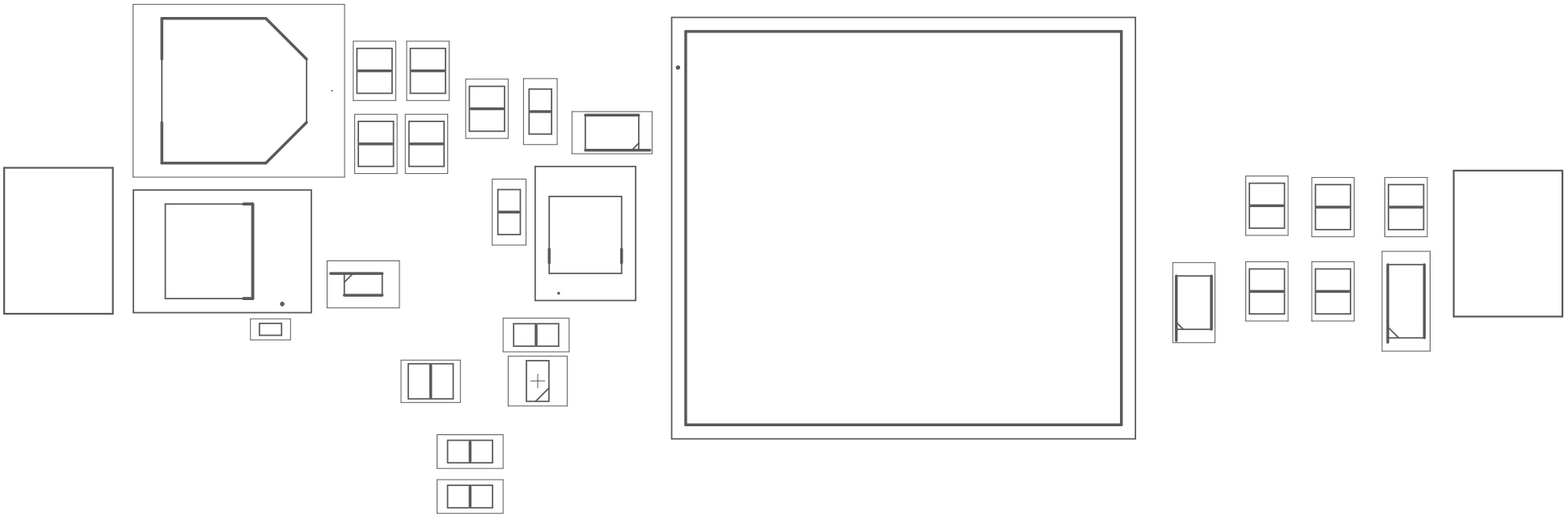


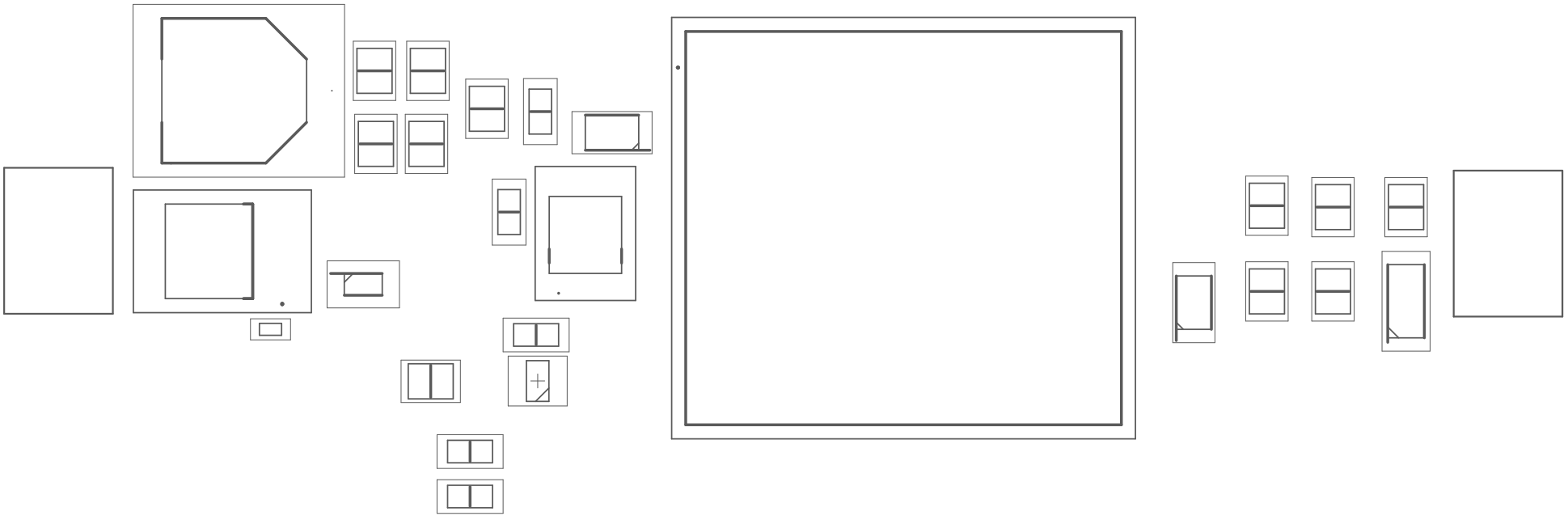


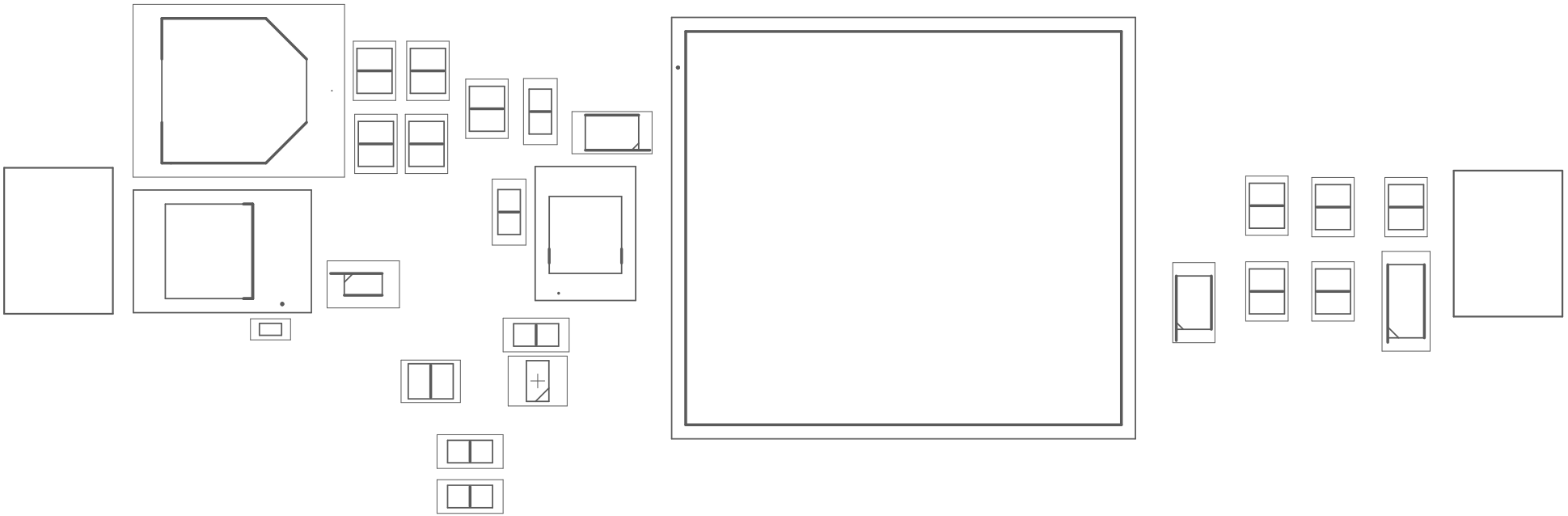


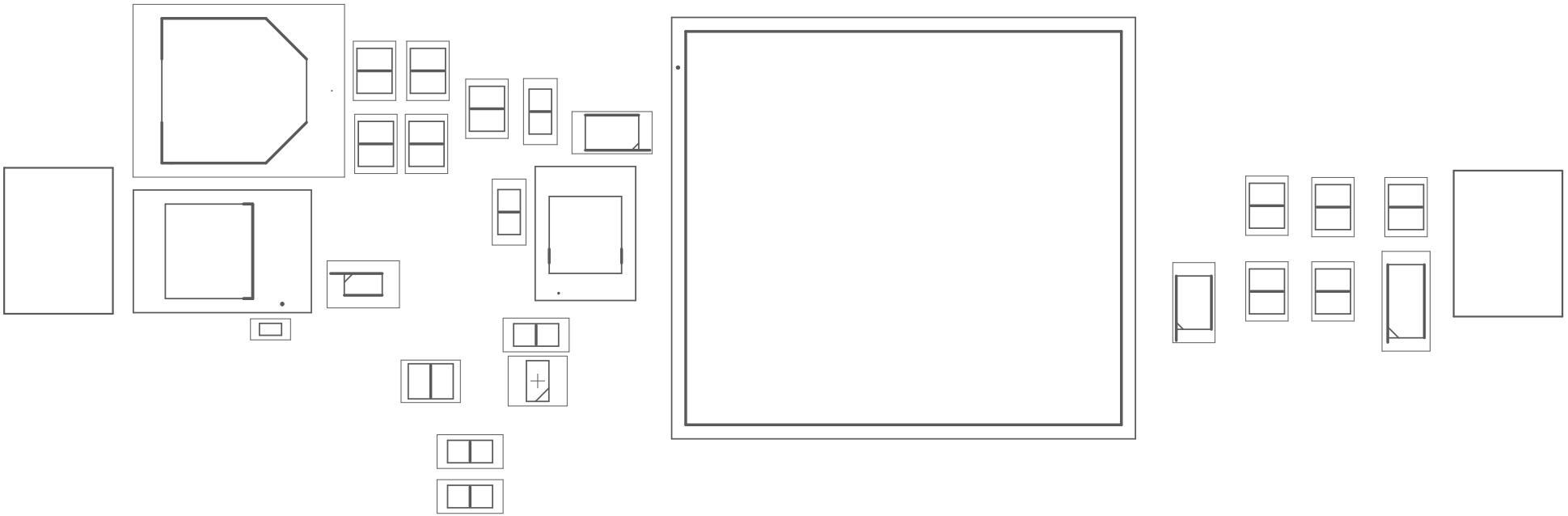

C1
C5
C4
T1
R3
D1
J1
C11
C9
C10
C6
J2
C2
C3
R4
Q1
D4
R1
Q2
R6
C12
D2
C7
C8
D3
U1
3-36VDC IN
12VDC 2A
R2
R5
Flyback Converter
REV 0.1

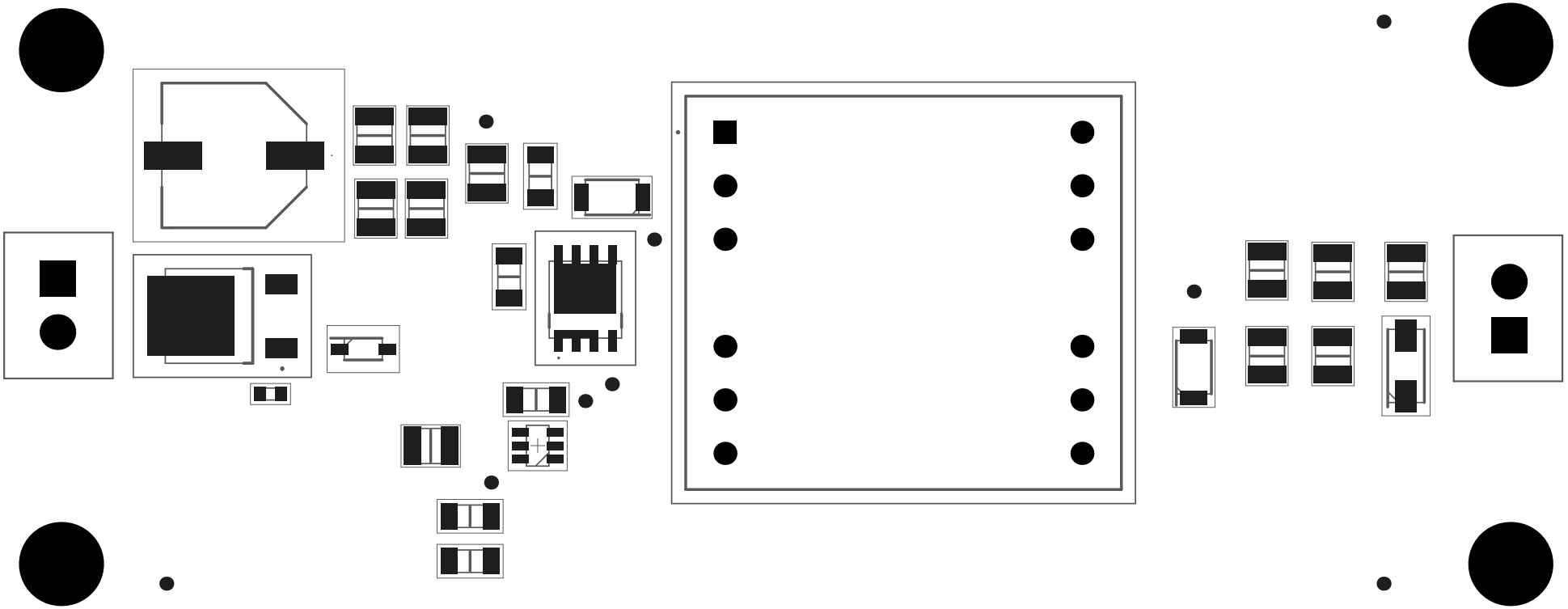


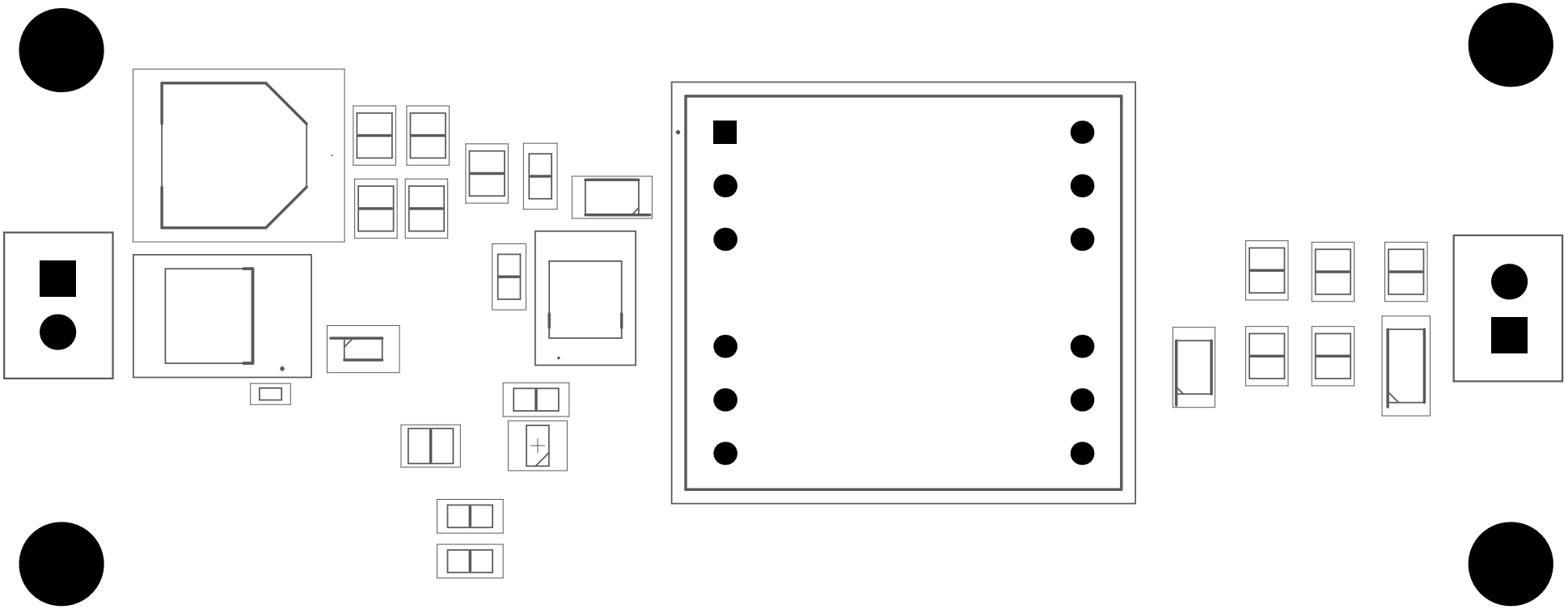


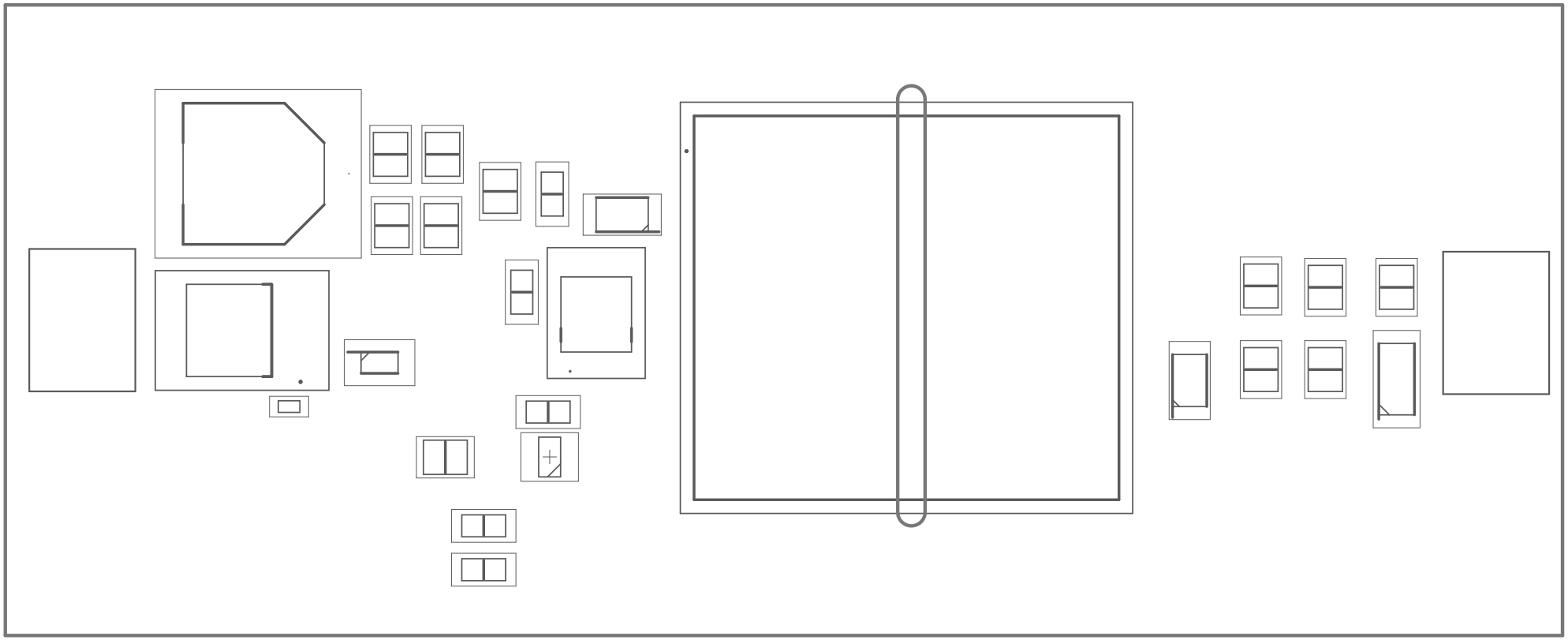


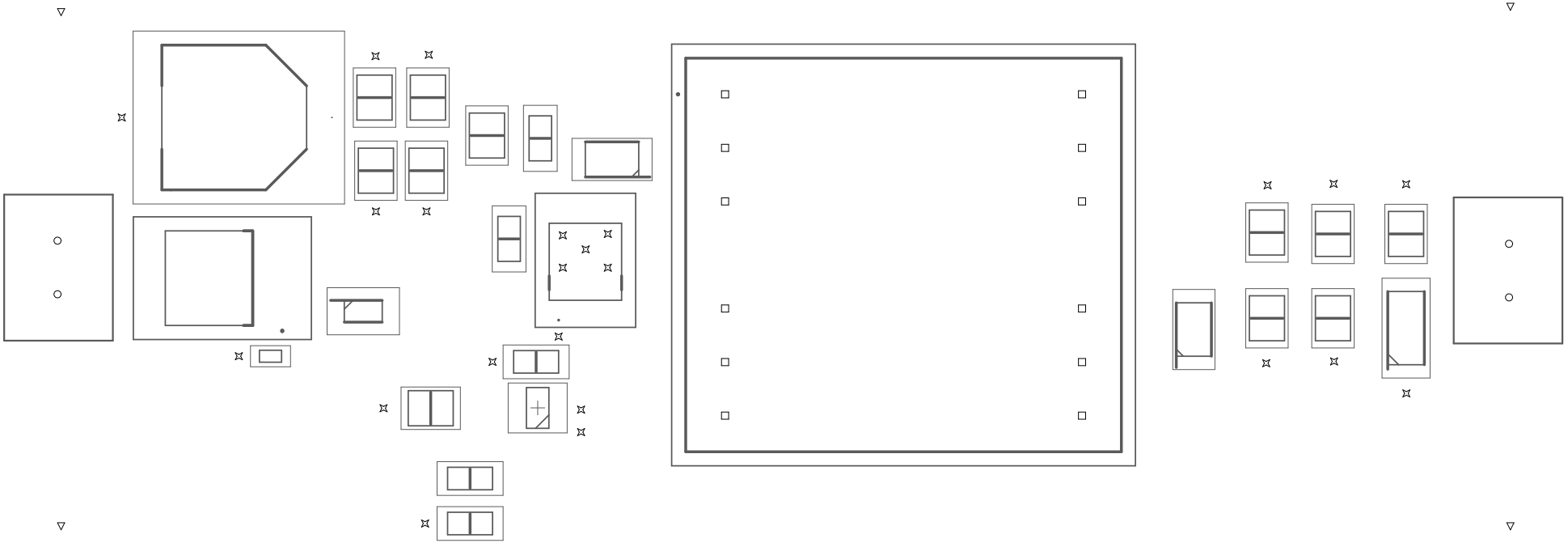


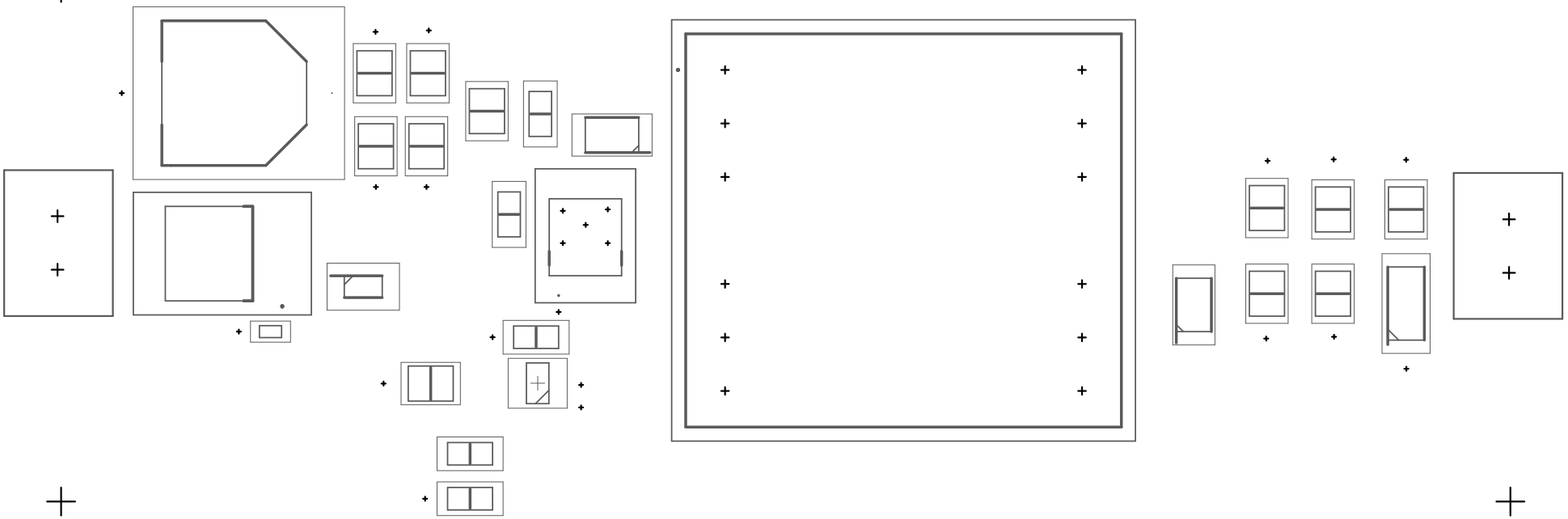


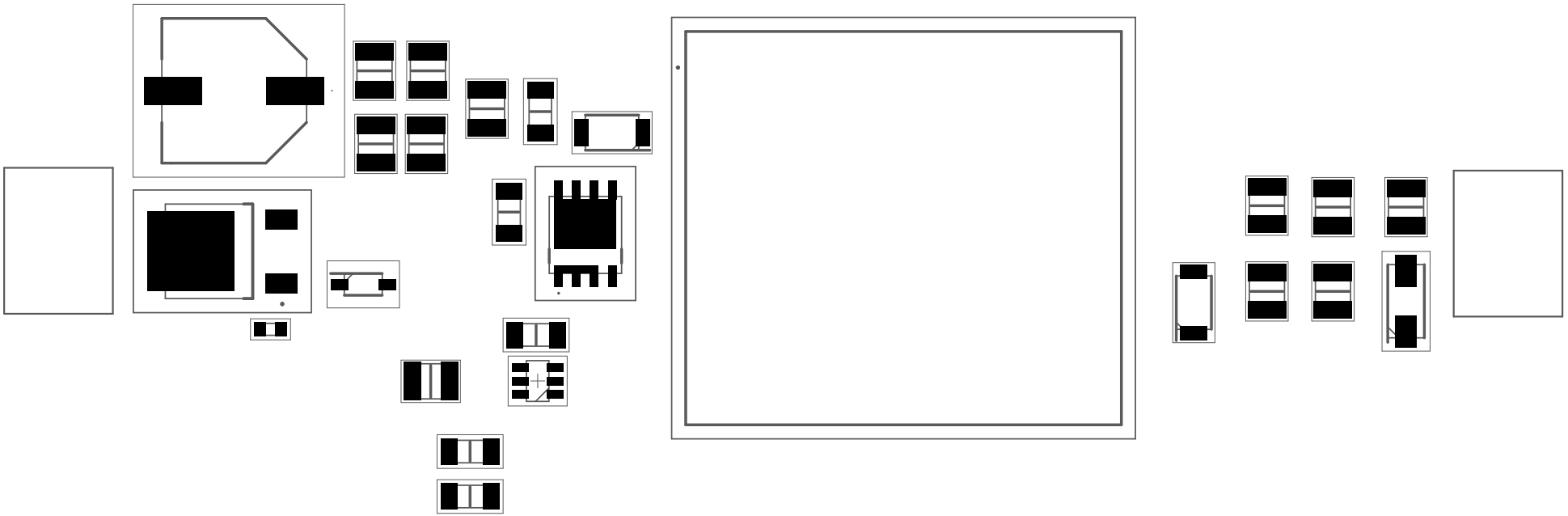


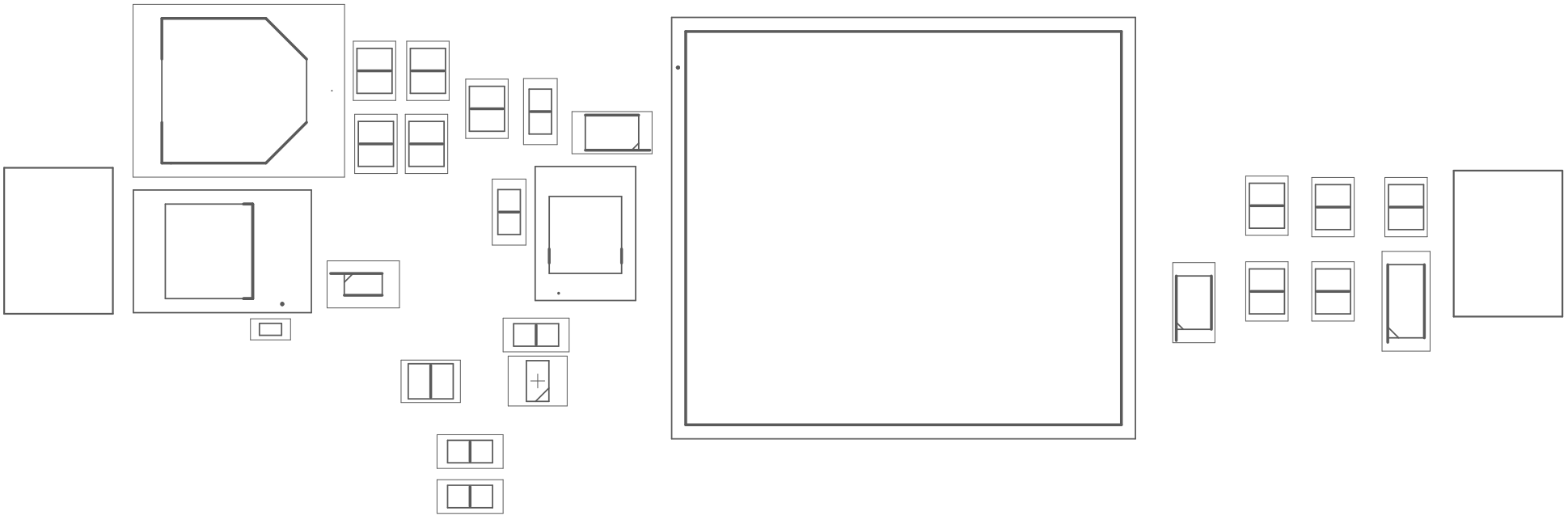


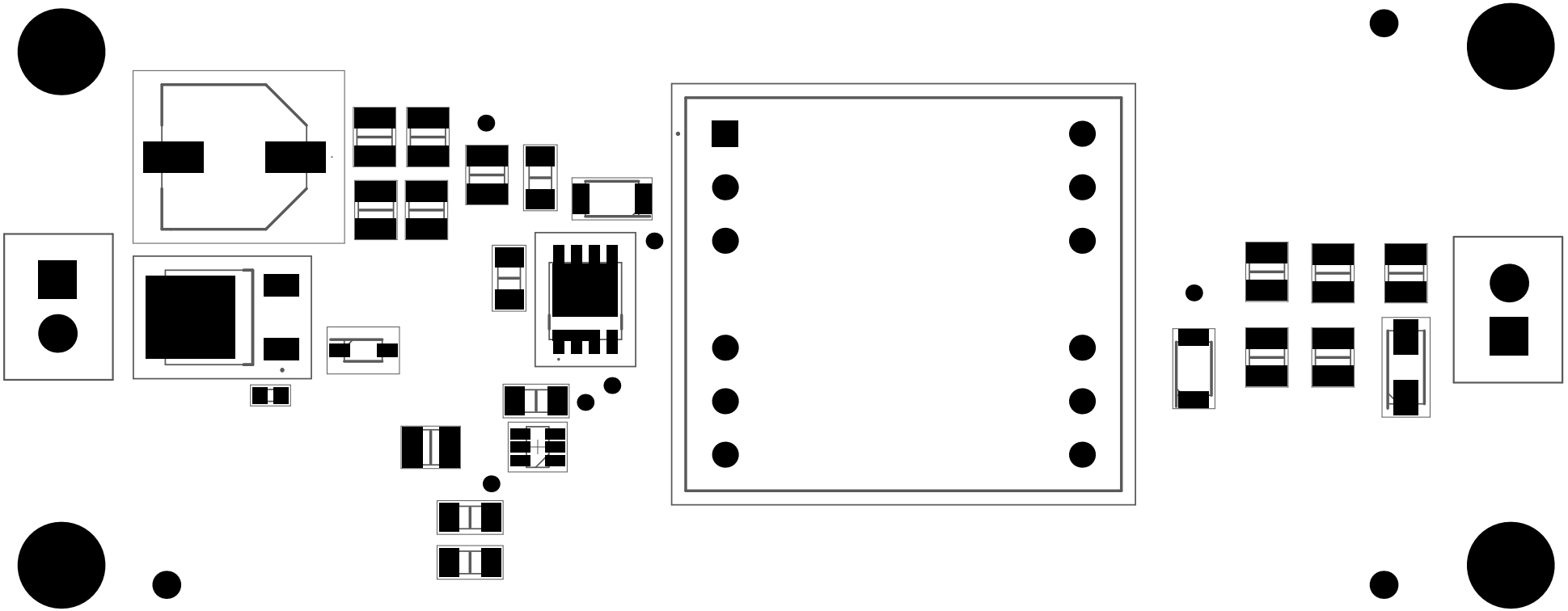


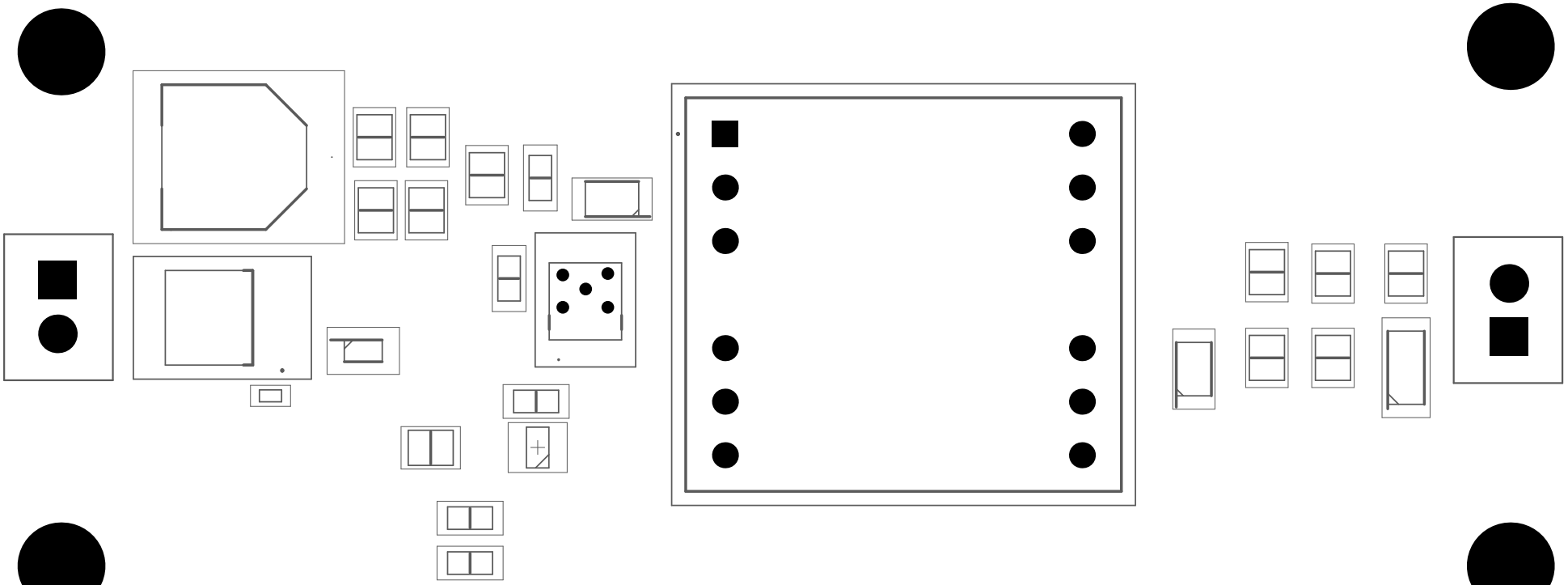












Design Rules Verification Report

Filename : D:\4 WORKSPACE\Flyback-Converter-Mosfet_model\0100 PCB Design\flyback.Pc

Warnings 0
Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=1.27mm) (Preferred=0.6mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.3mm) (Max=10mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.127mm) (All),(All)	1
Silk To Solder Mask (Clearance=0.127mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	1

Minimum Solder Mask Sliver (Gap=0.127mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.127mm) Between Pad Q1-8(35.402mm,22.019mm) on Top Layer And Via (35.7mm,20.7mm) from

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for

Component Classes With Extra Members	
Schematic Object	PCB Object
[D1]	
[TP6]	