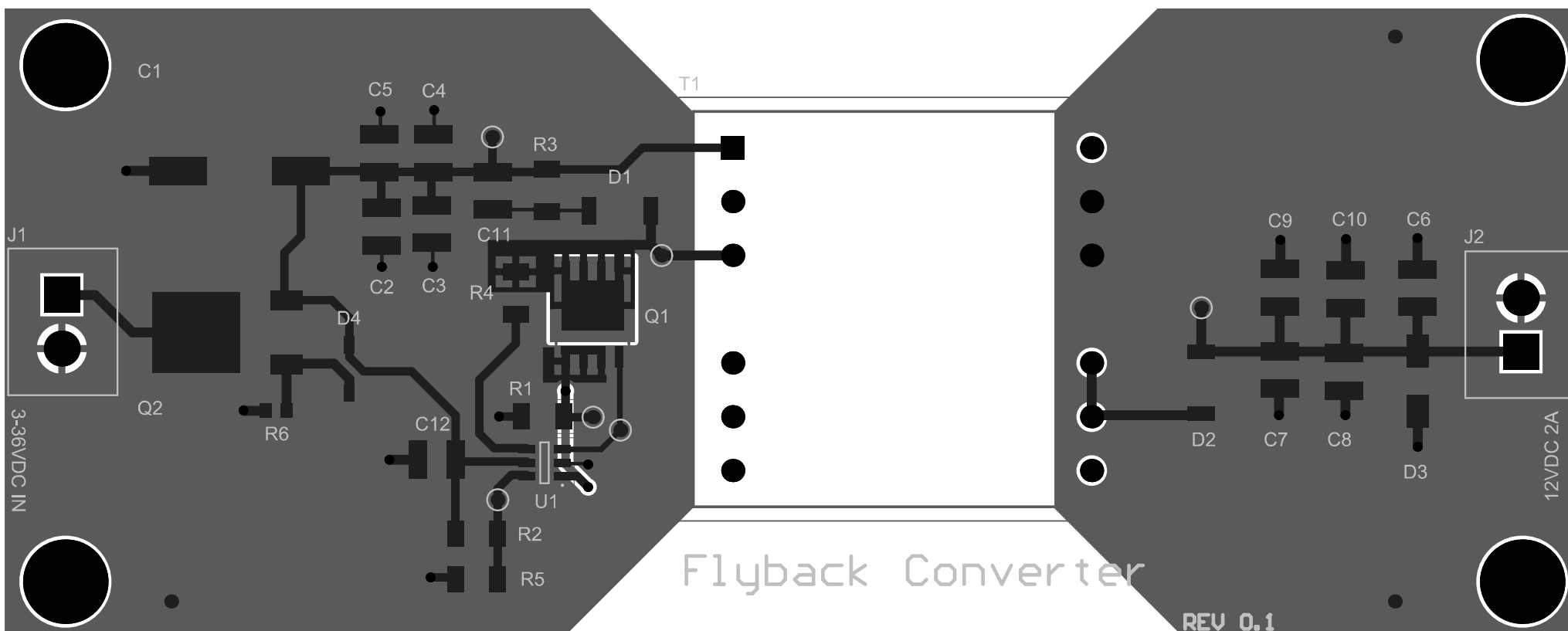
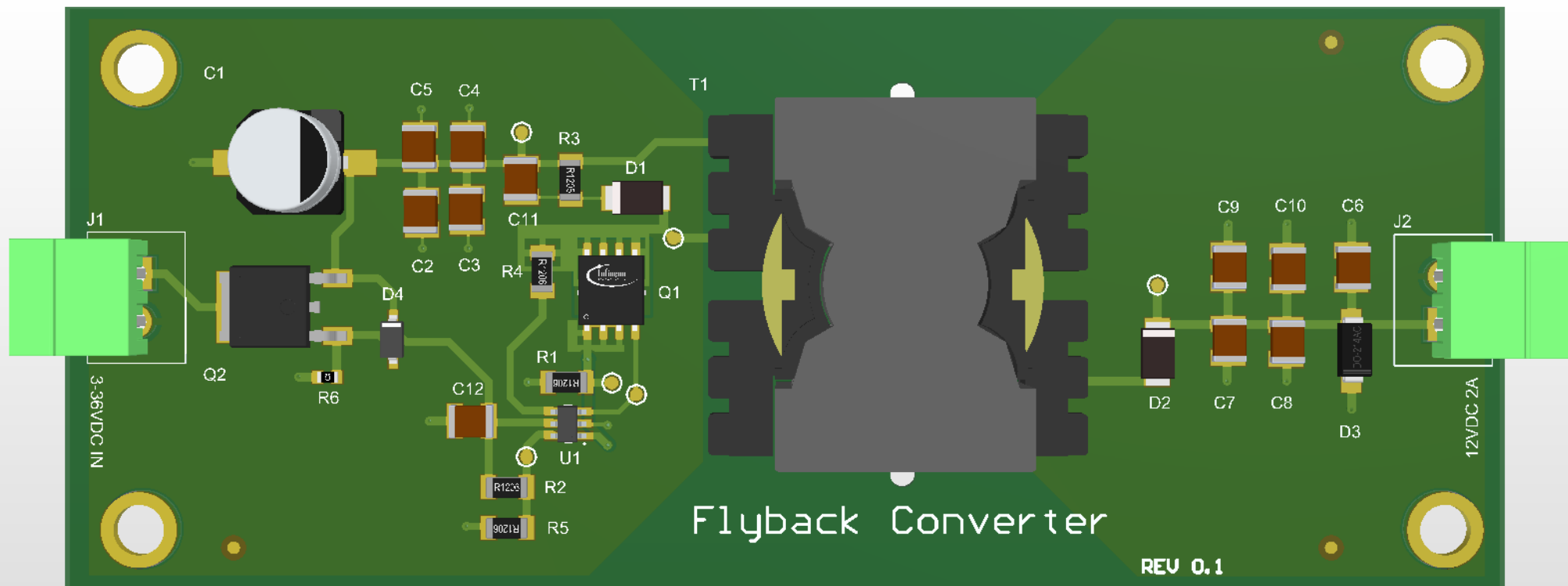
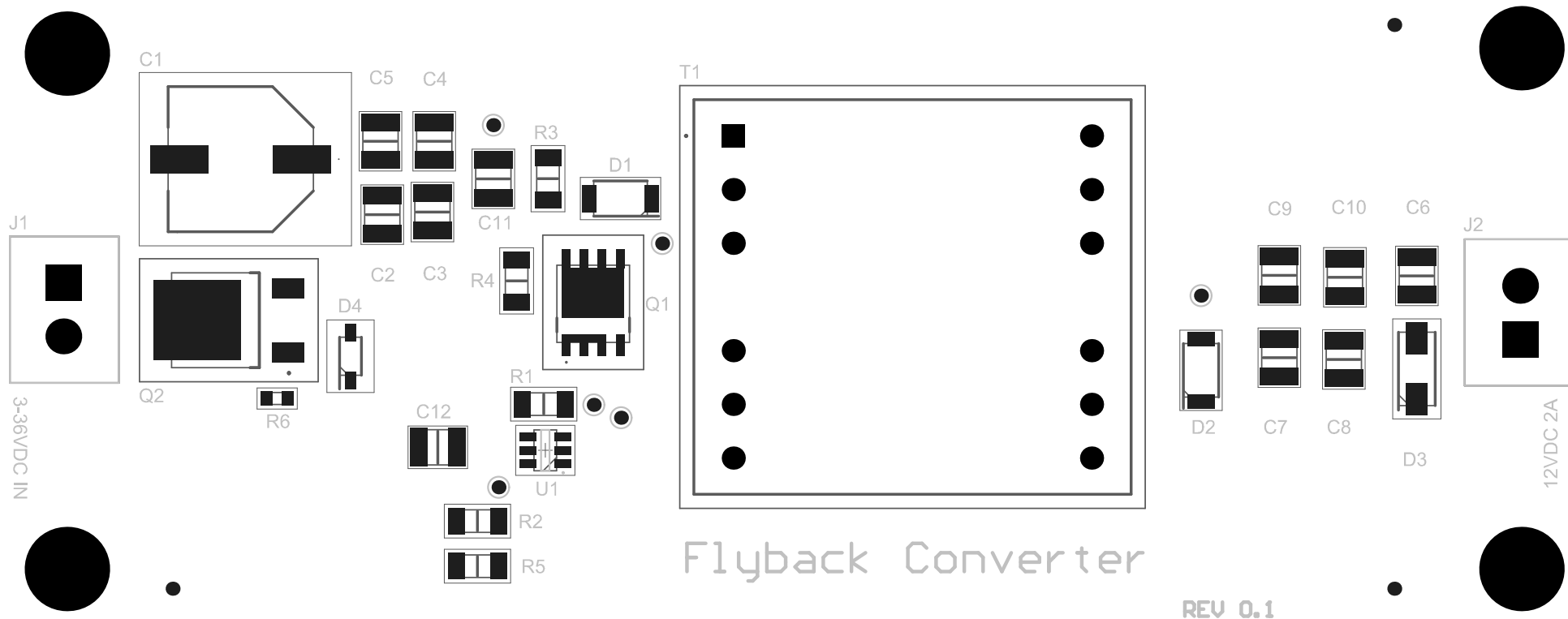


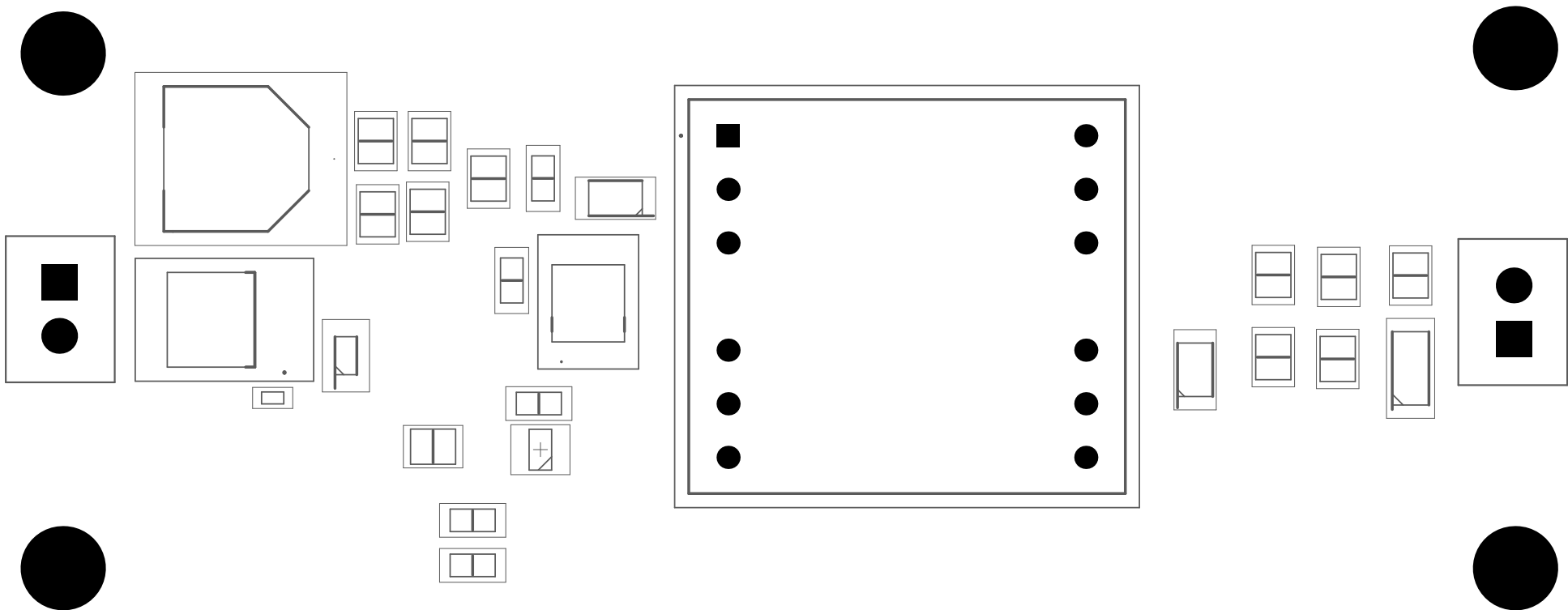
Title		
Flyback Converter		
Size	Number	Revision
B	1	1.0
Date:	8/21/2024	Sheet 1 of 1
File:	D:\4 WORKSPACE\..flyback.SchDoc	Drawn By: MOHAMED GUENI
	2	1





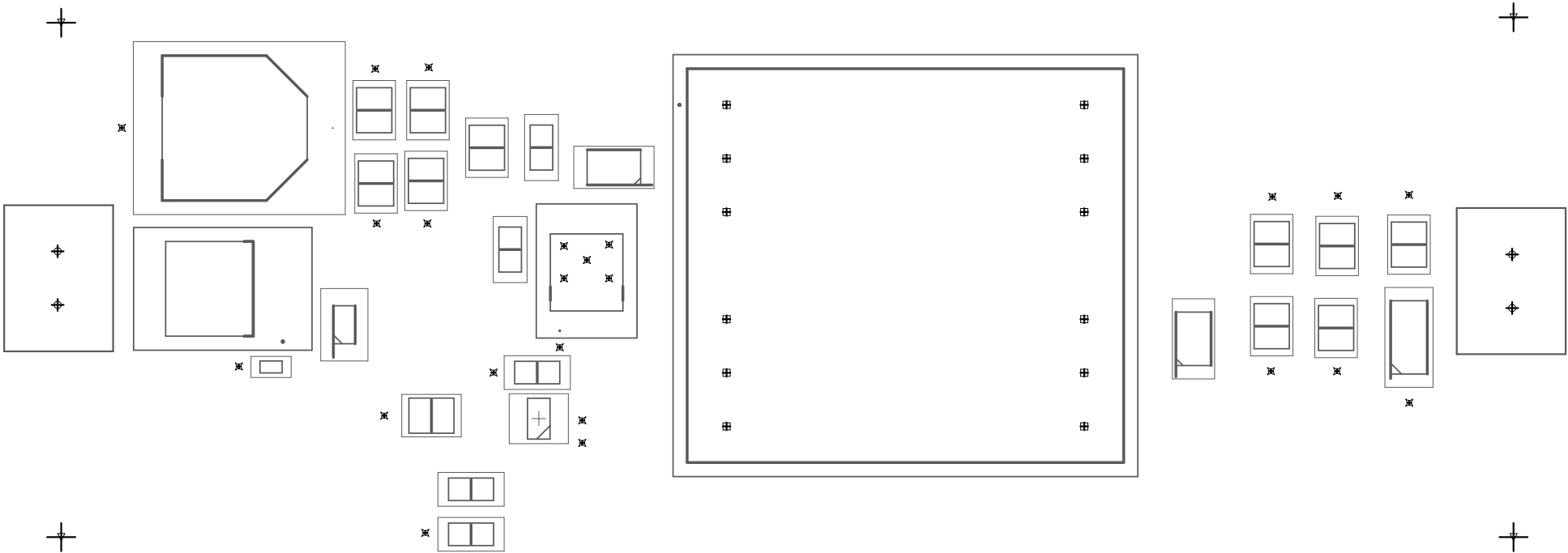




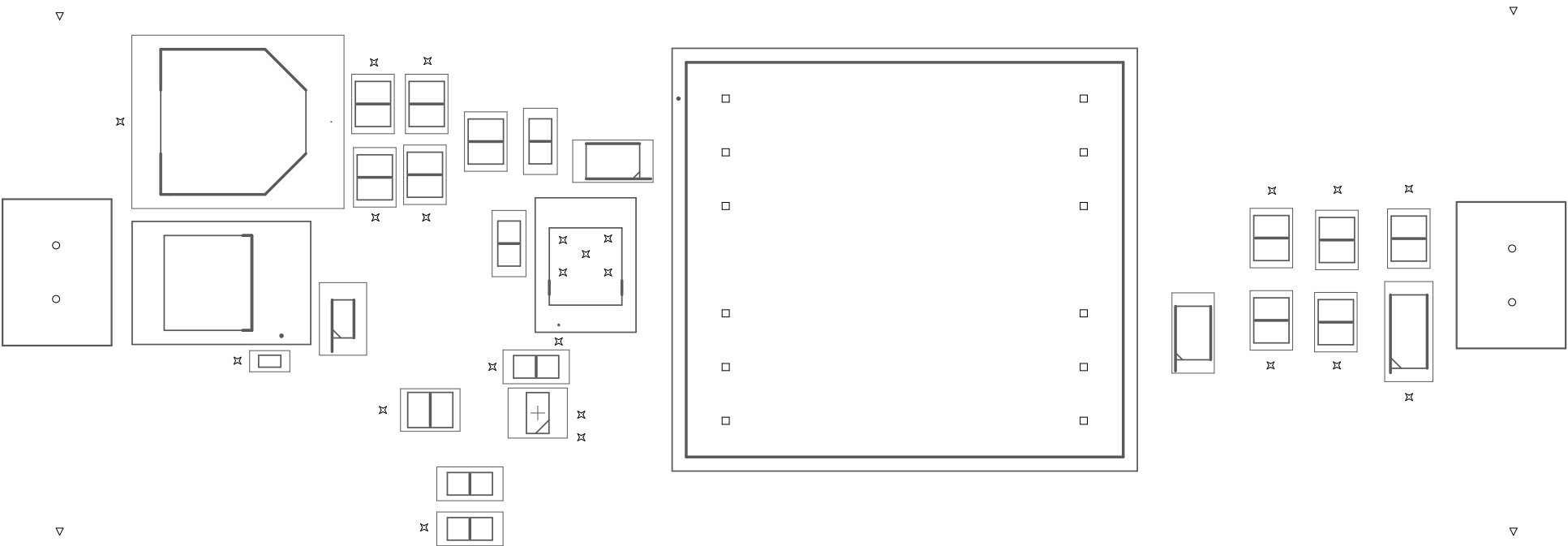


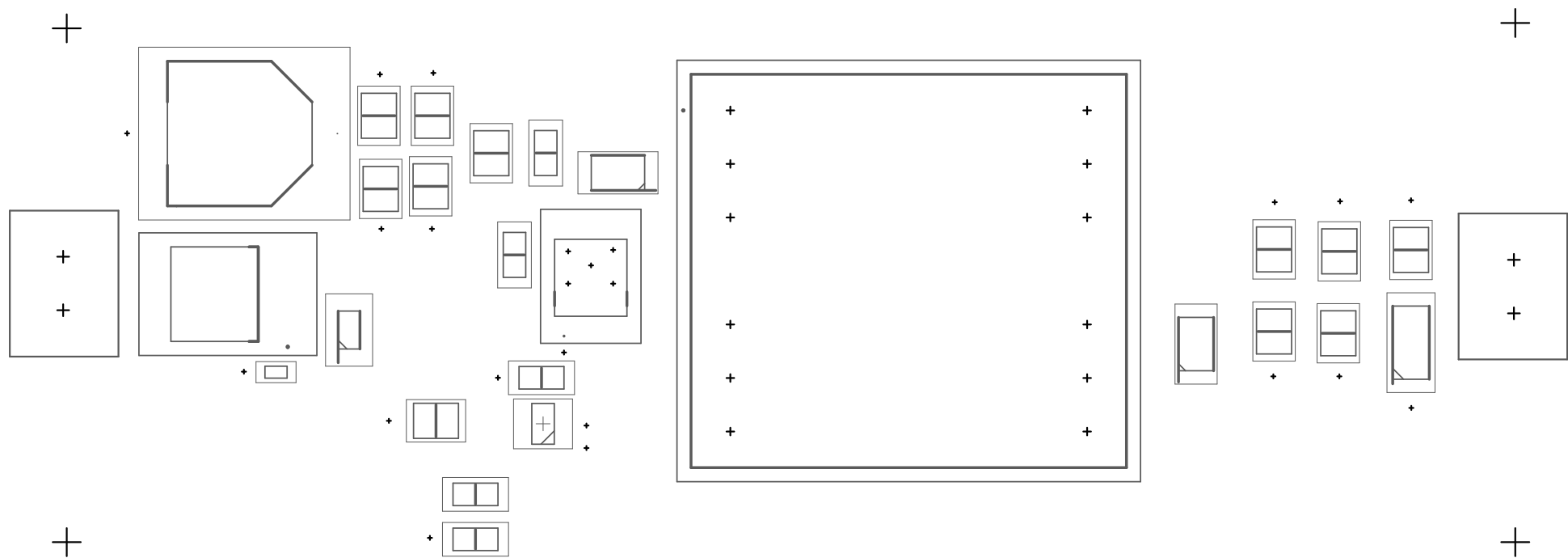
# Board Stack Report

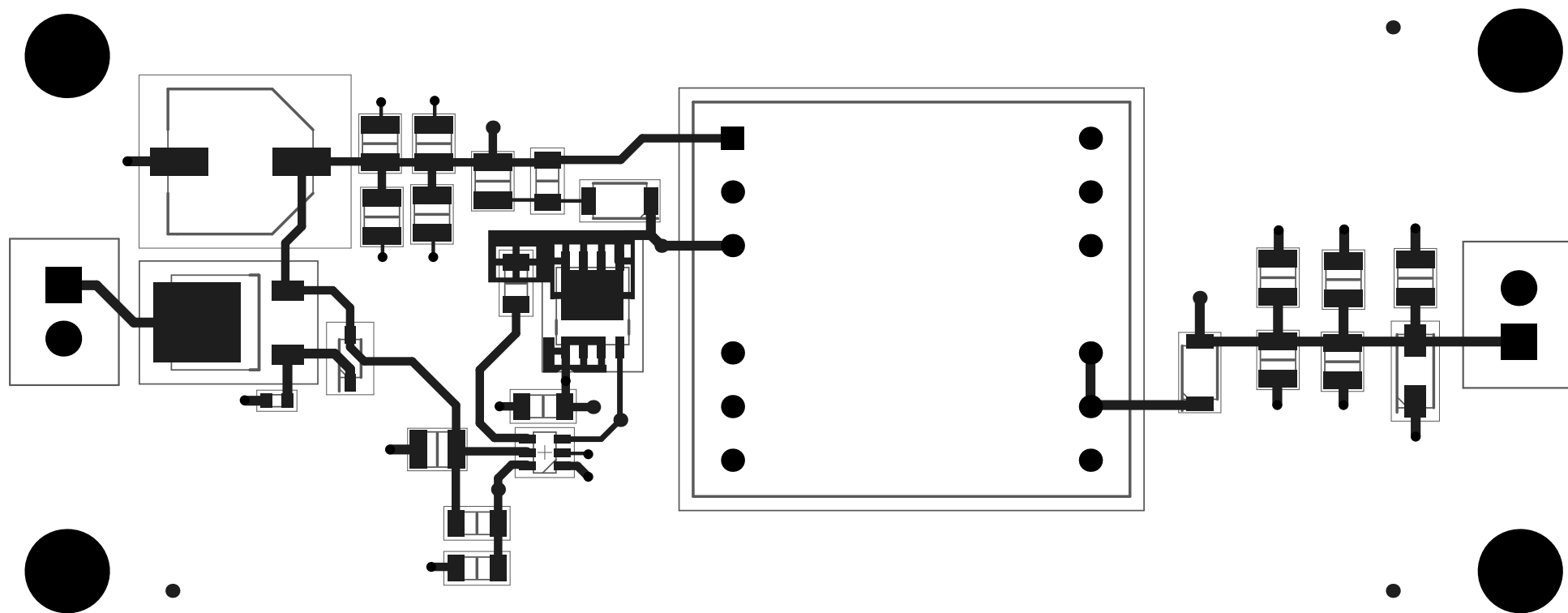
Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Overlay		0mil	
2		Top Solder	Solder Resist	0.4mil	3.5
3		Top Layer	CF-004	1.4mil	
4		Dielectric 1	Core-043	59mil	4.3
5		Bottom Layer	CF-004	1.4mil	
6		Bottom Solder	Solder Resist	0.4mil	3.5
7		Bottom Overlay		0mil	
	Height : 62.6mil				

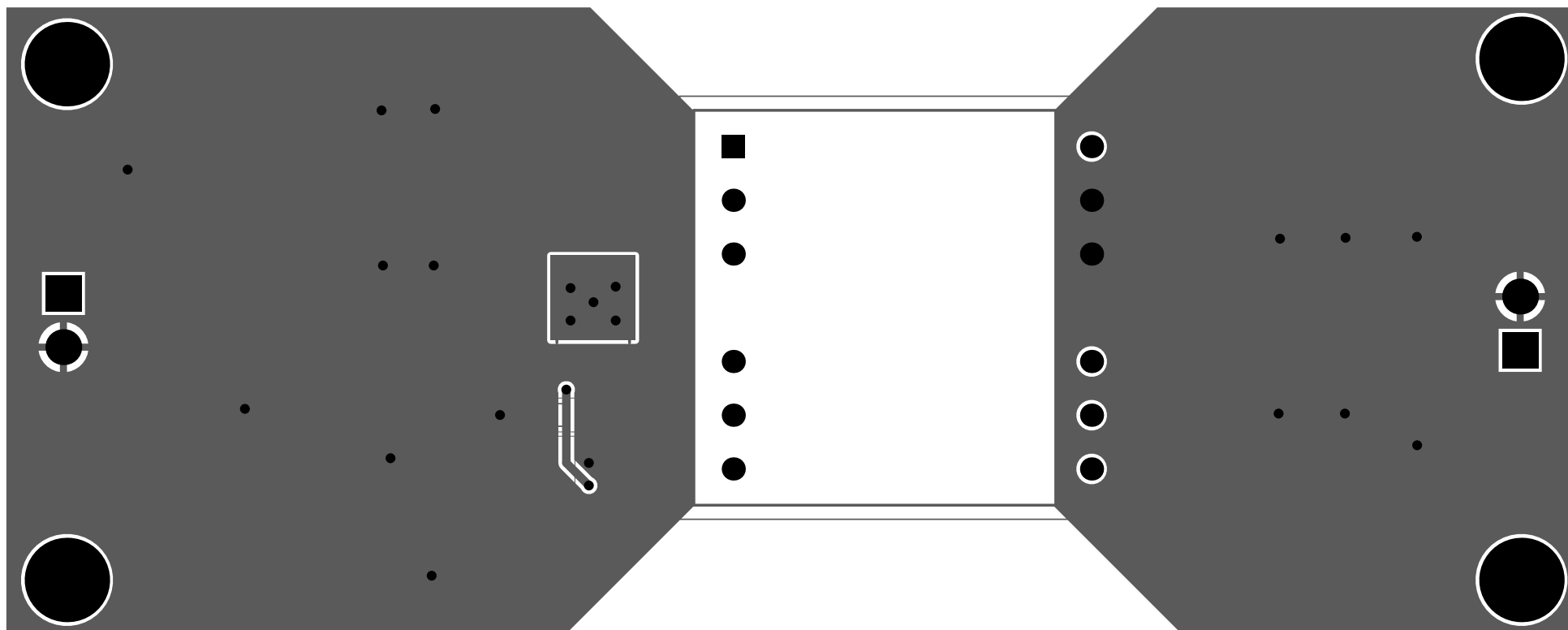


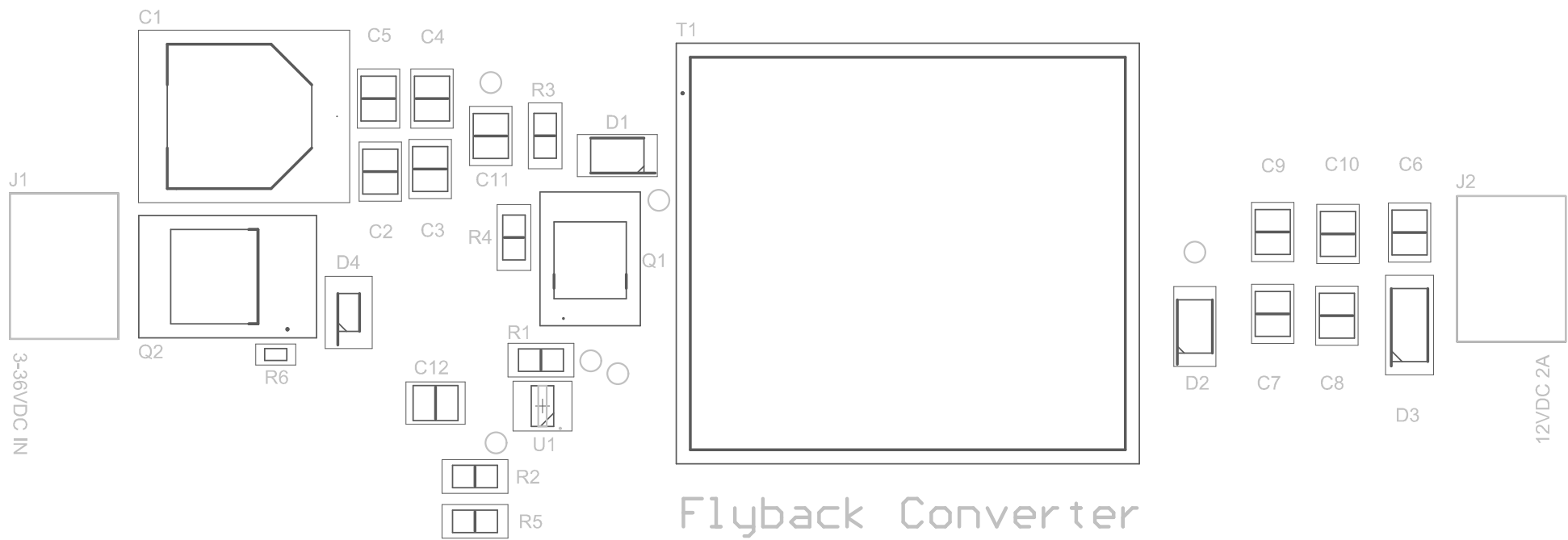




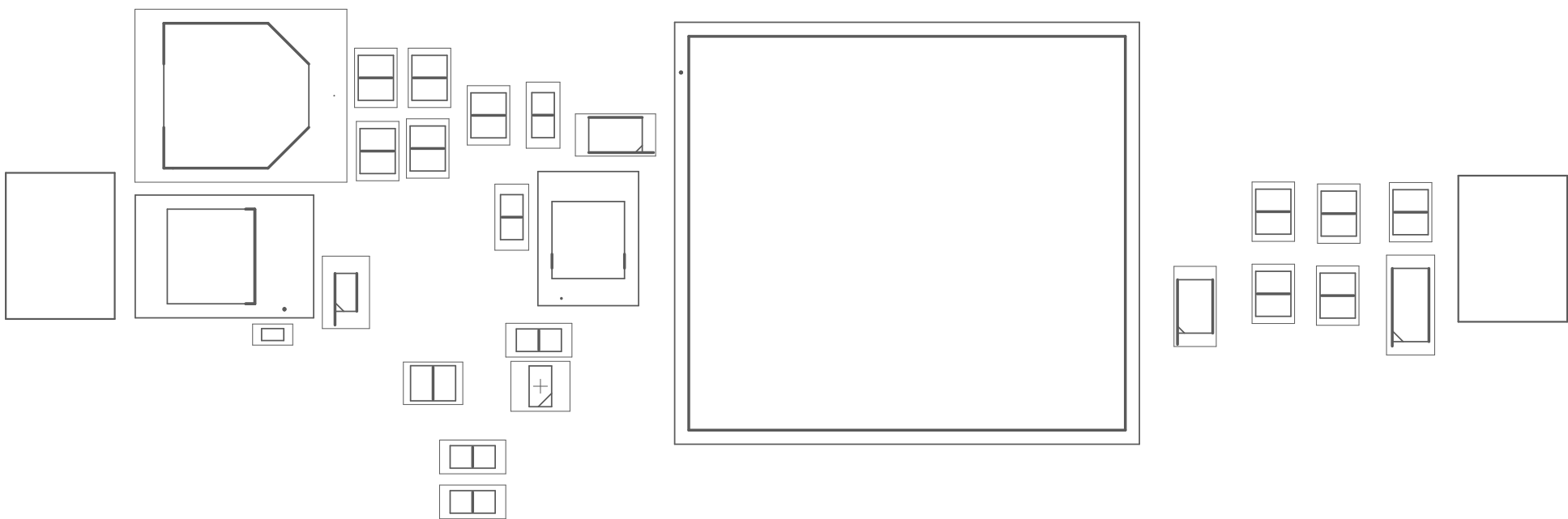


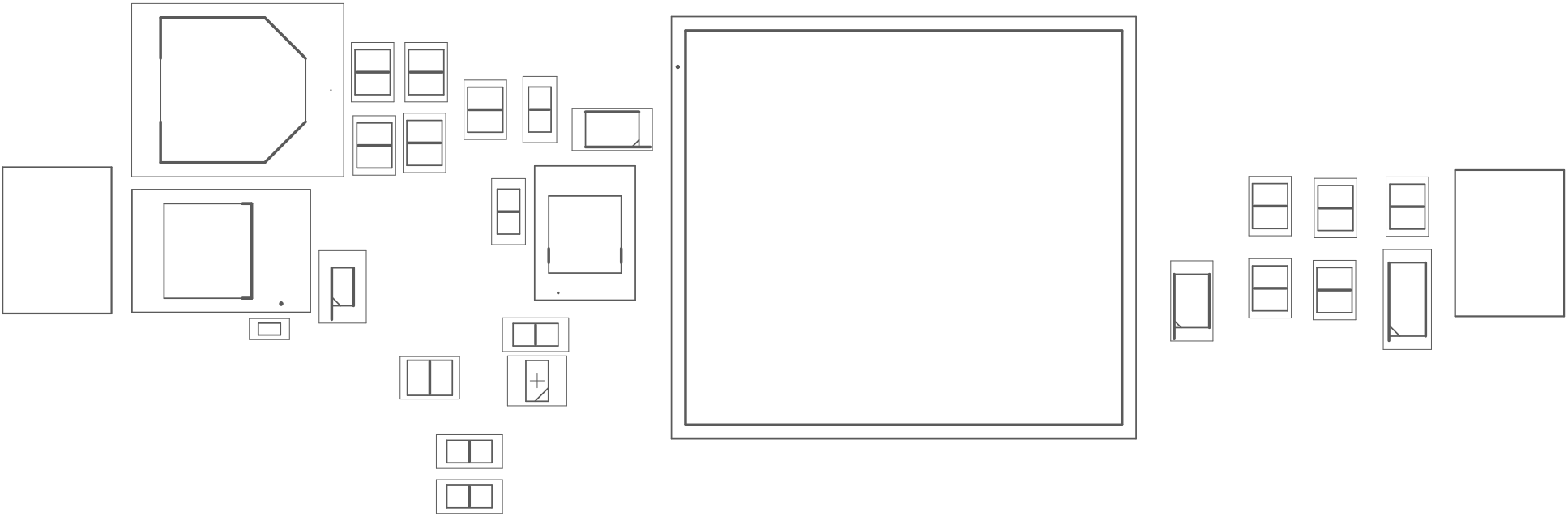


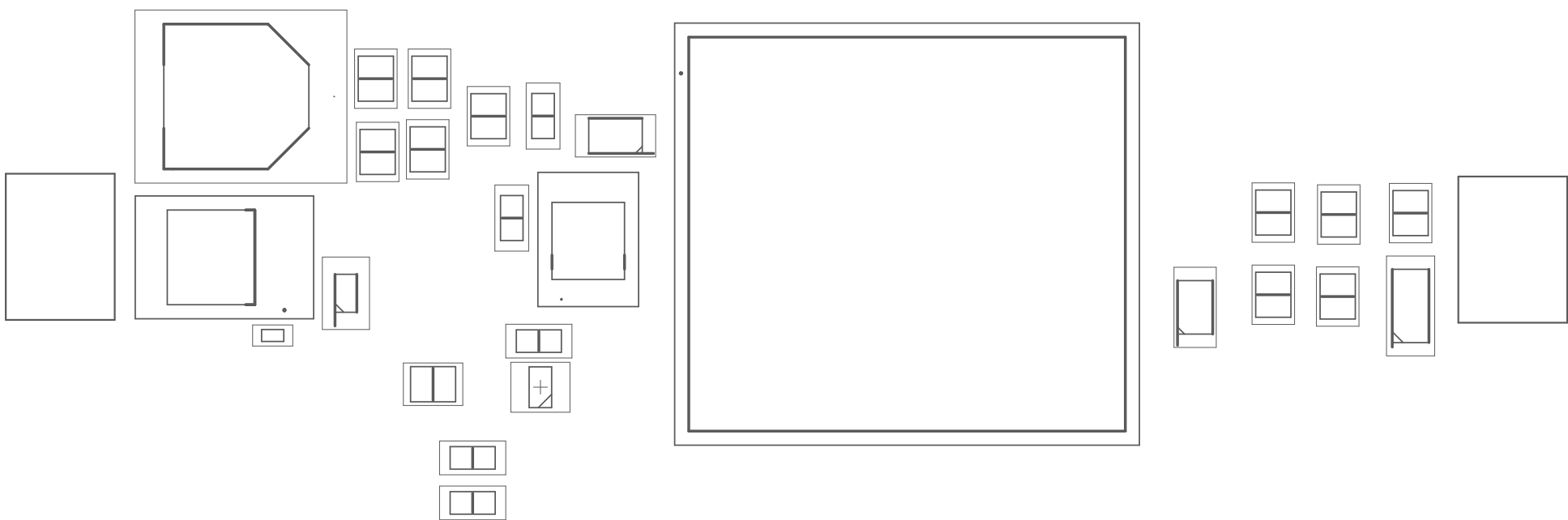




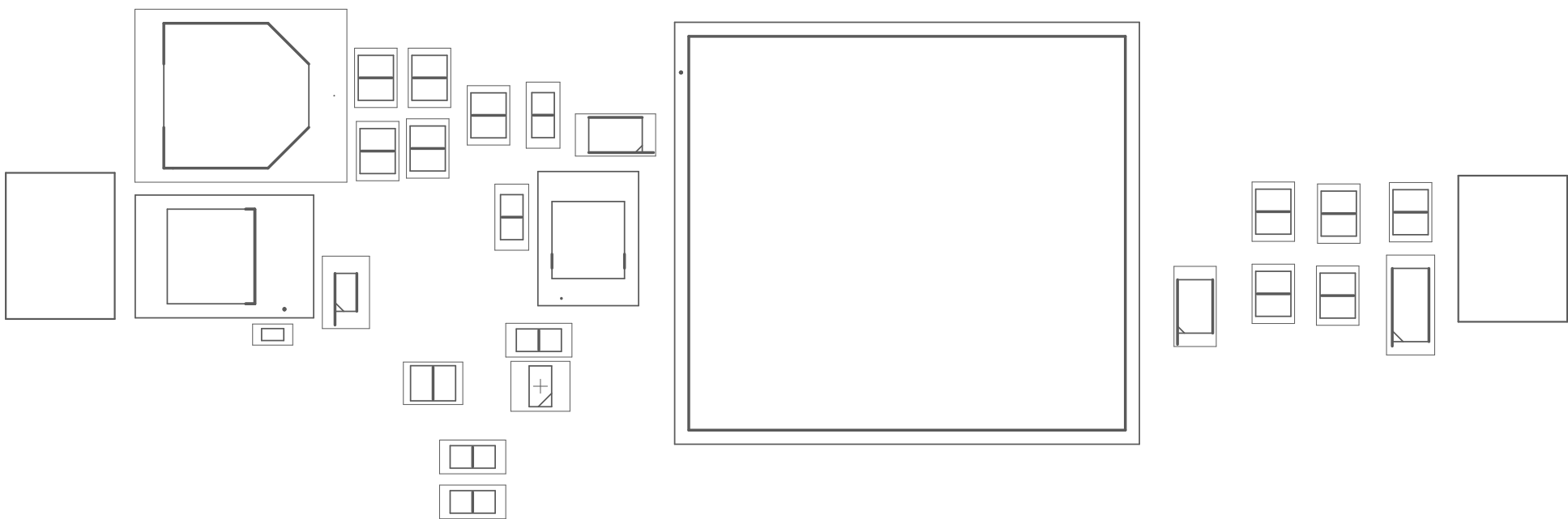
REV 0.1

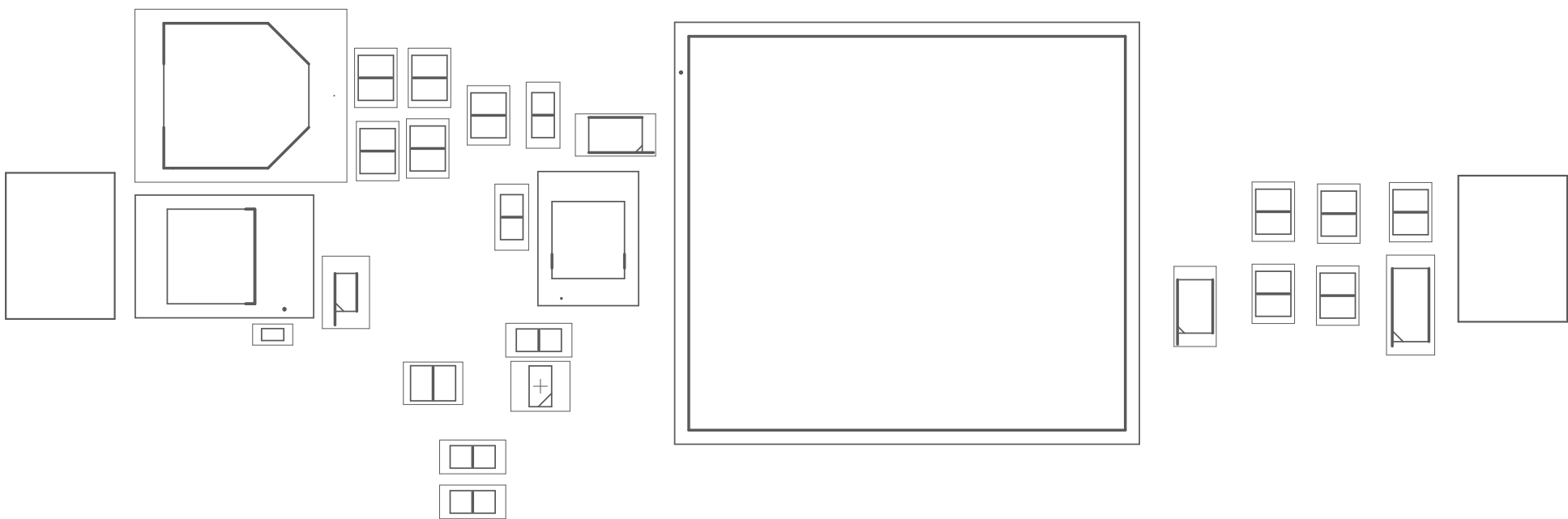


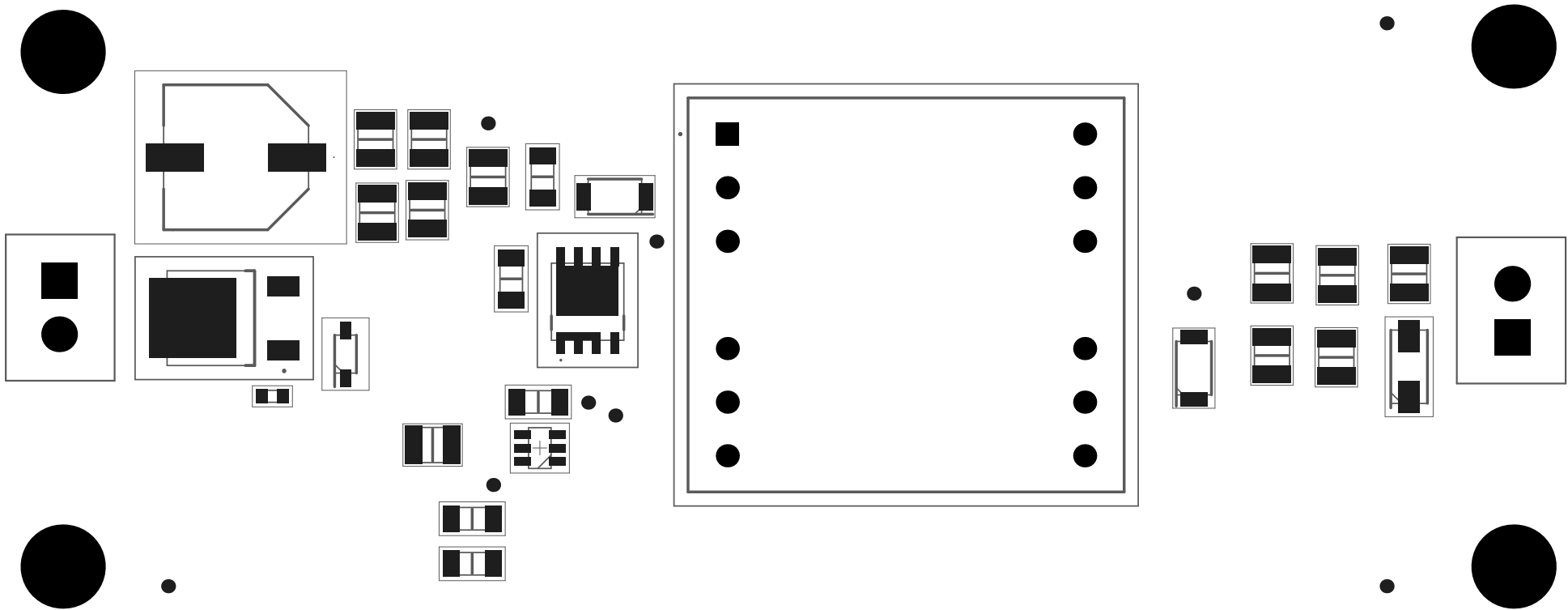


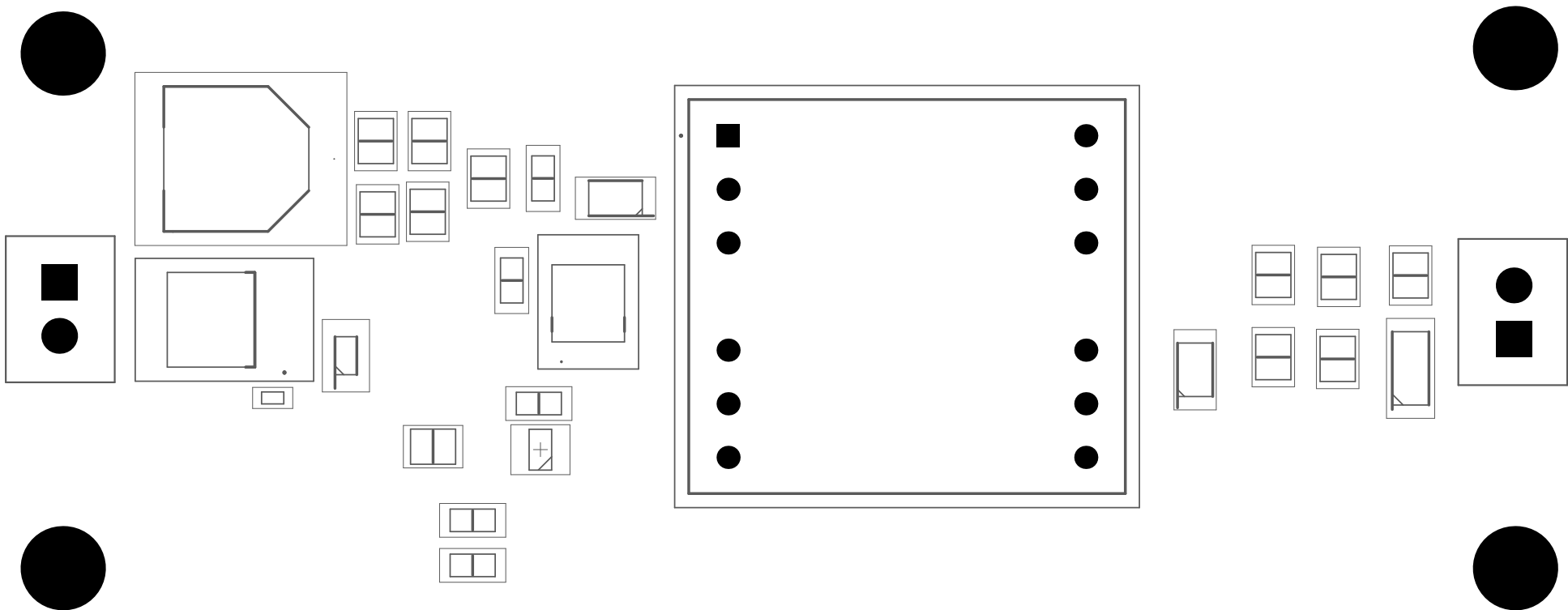


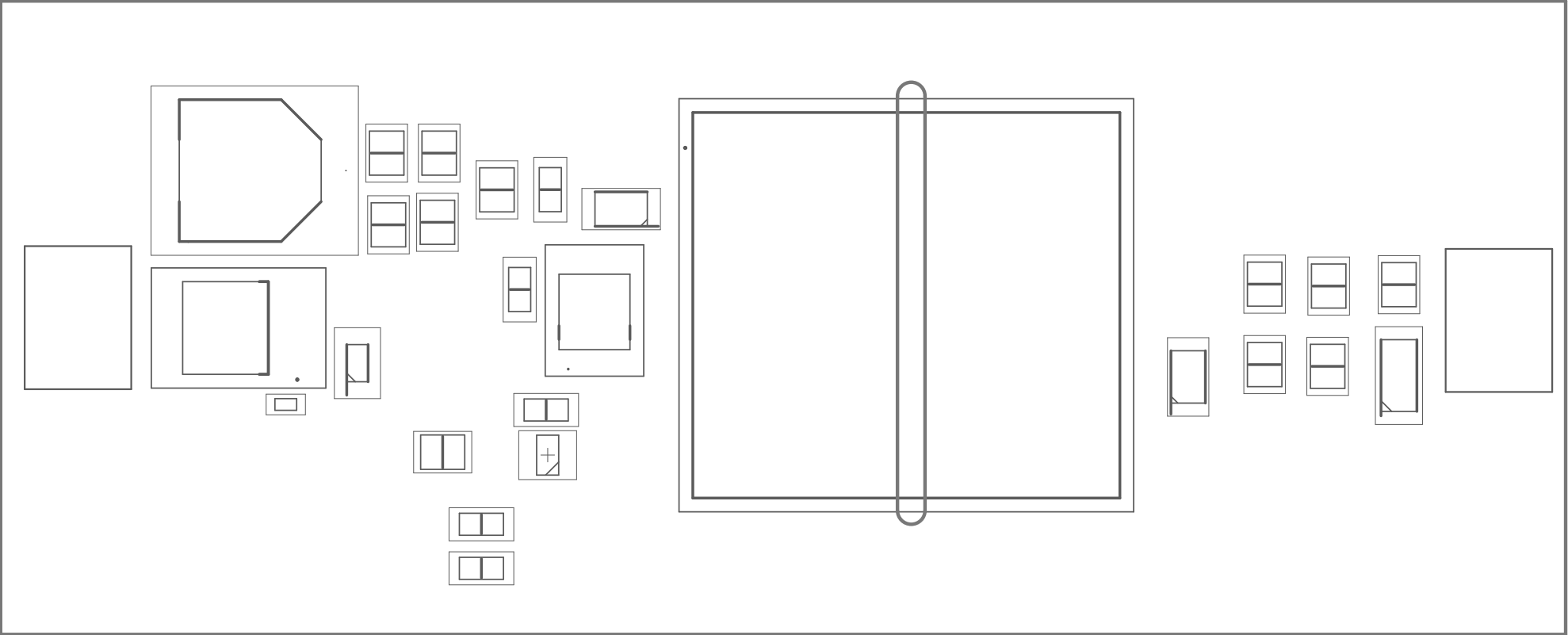


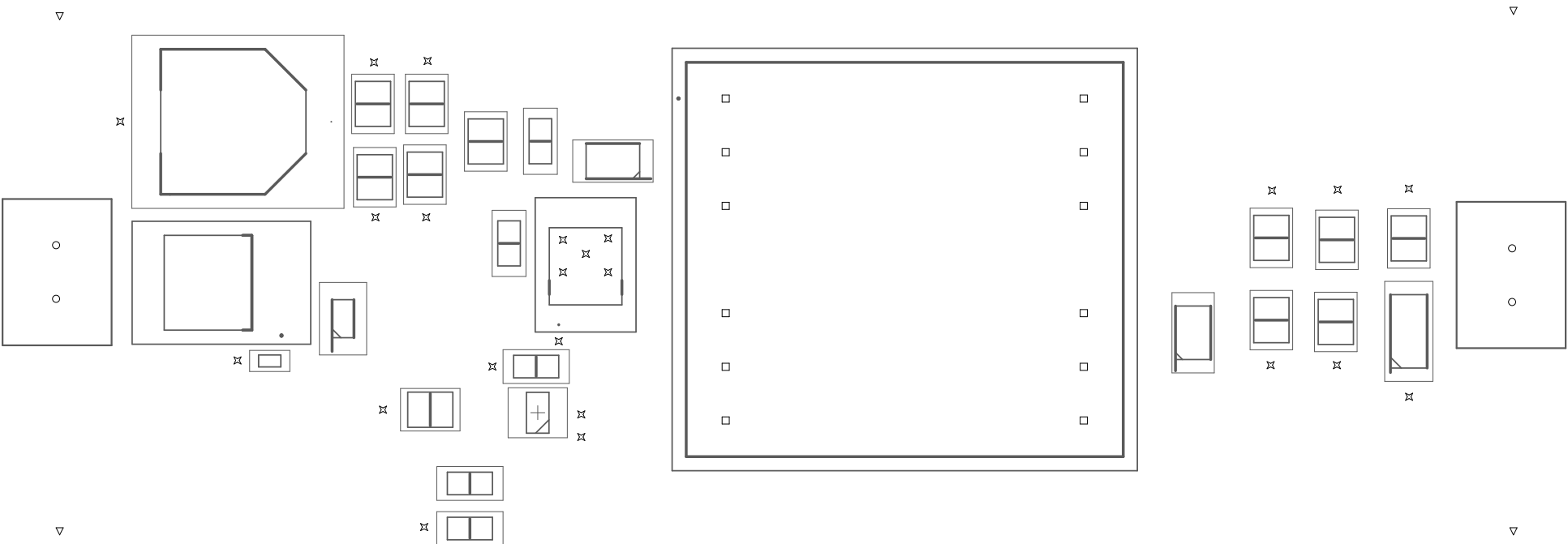


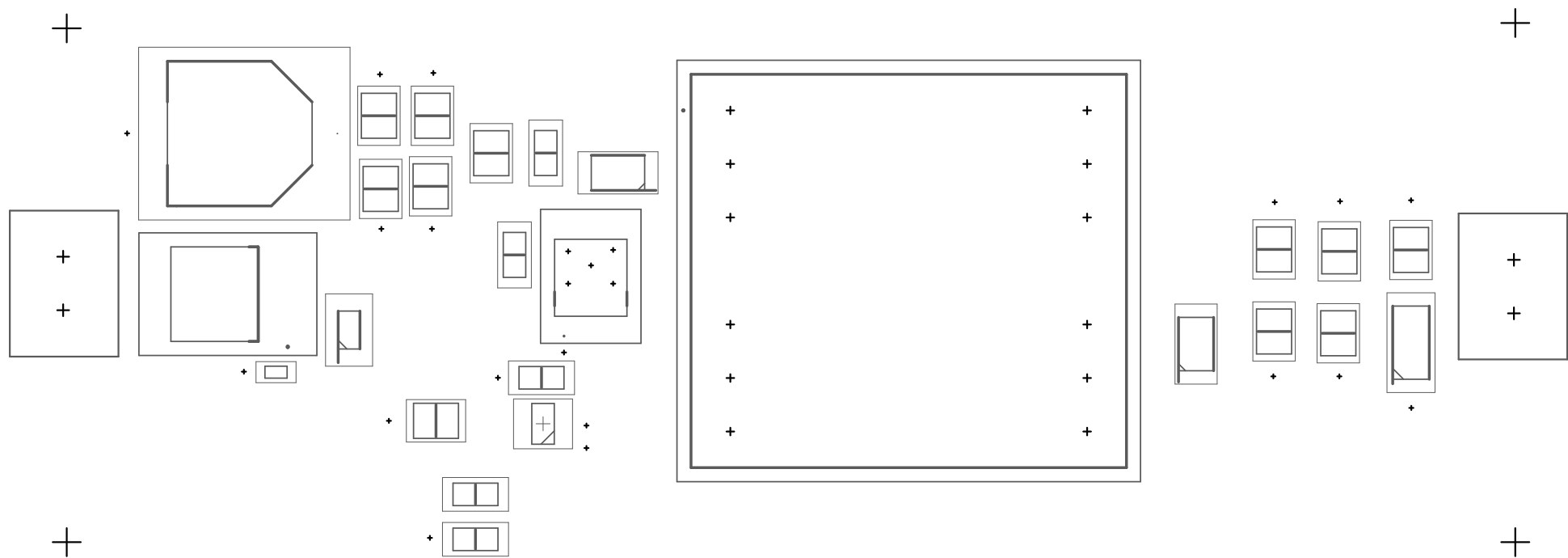


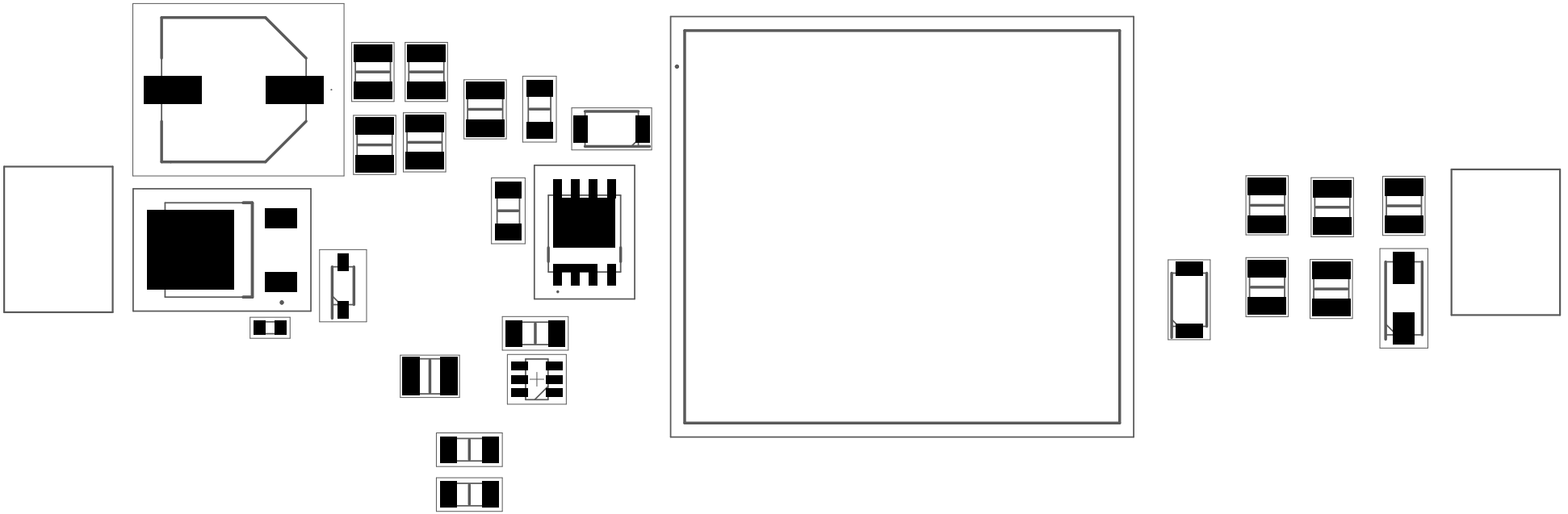




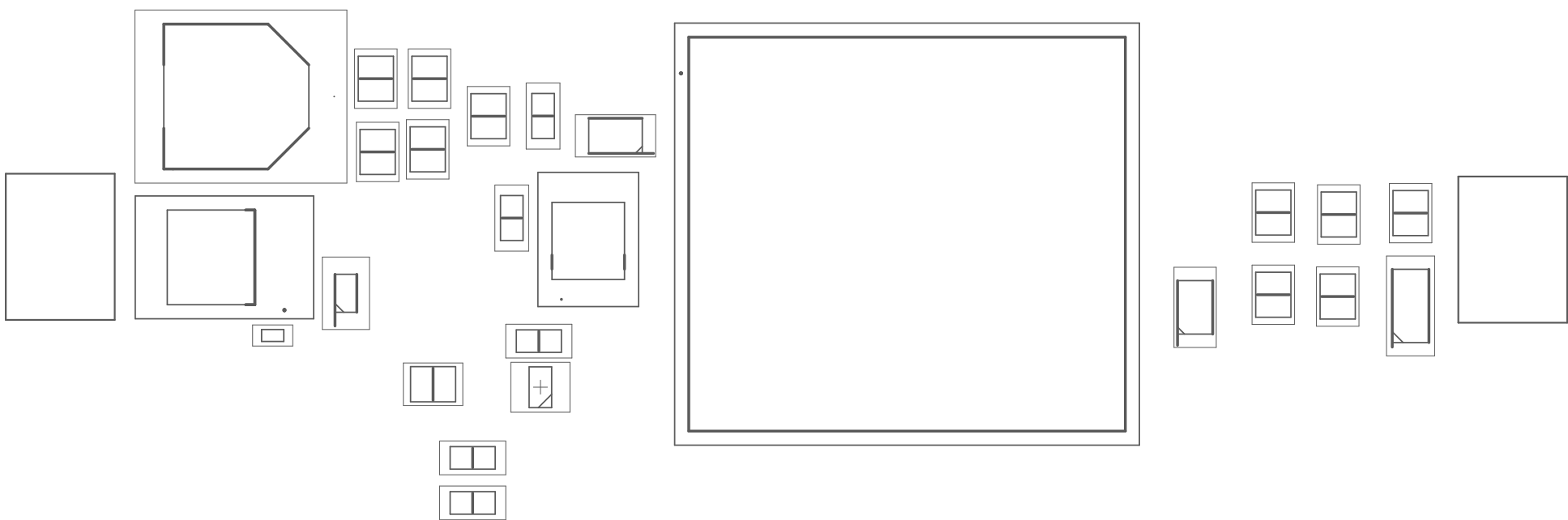


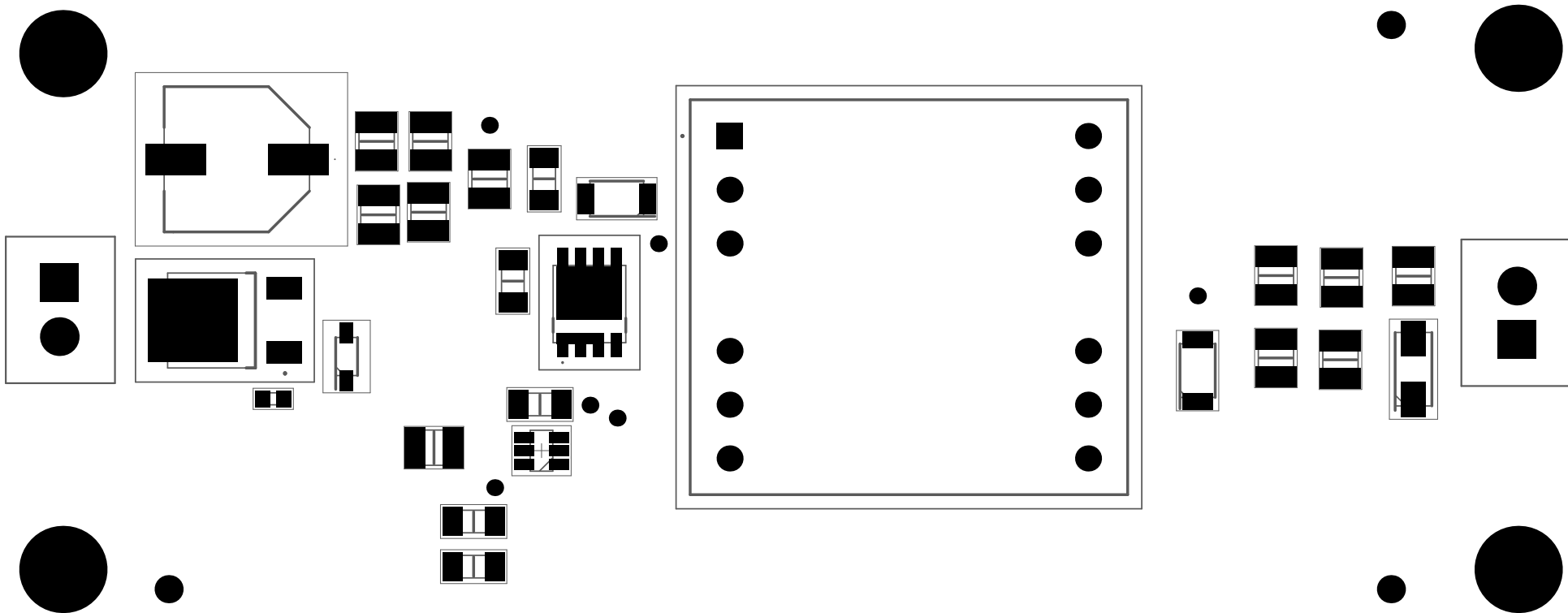


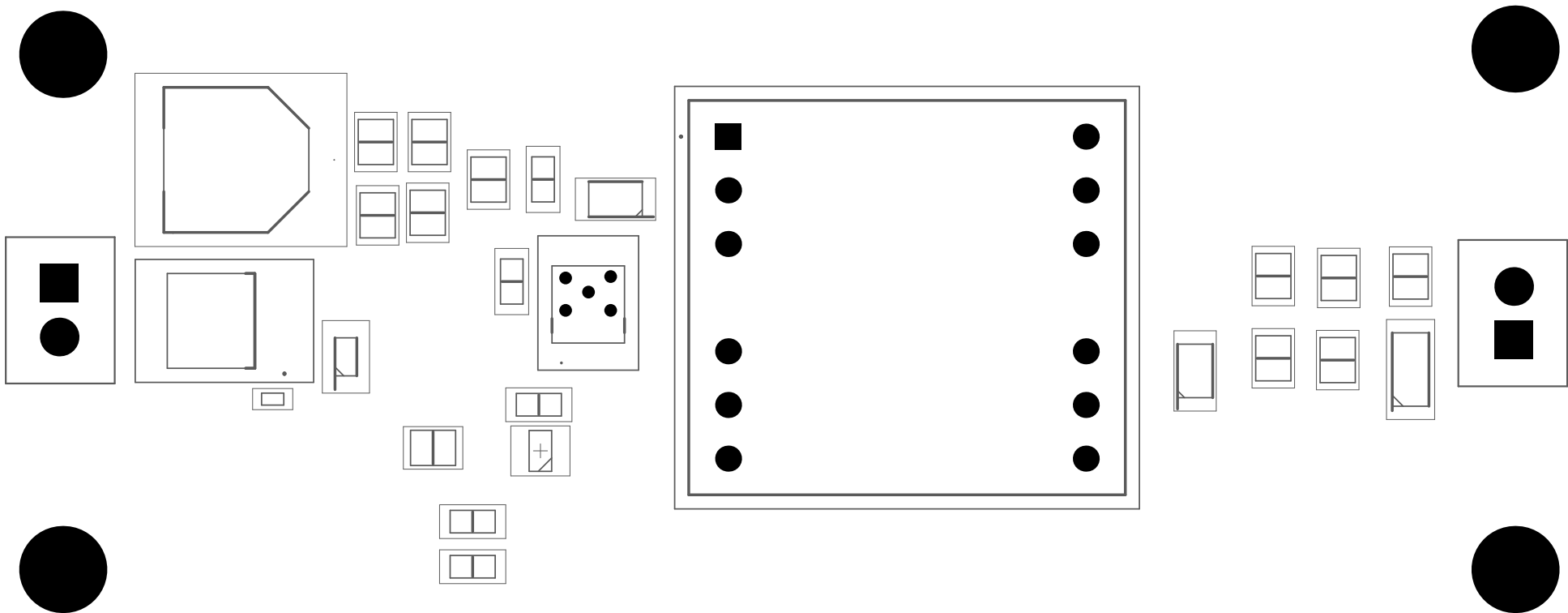














## Design Rules Verification Report

Filename : D:\4 WORKSPACE\Flyback-Converter-Mosfet\_model\0100 PCB Design\flyback.Pc

Warnings 0  
Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=1.27mm) (Preferred=0.6mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.3mm) (Max=10mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.127mm) (All),(All)	1
Silk To Solder Mask (Clearance=0.127mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	1

Minimum Solder Mask Sliver (Gap=0.127mm) (All),(All)	
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.127mm) Between Pad Q1-8(35.402mm,22.019mm) on Top Layer And Via (35.7mm,20.7mm) from	

**Electrical Rules Check Report**

Class	Document	Message
		Successful Compile for

Component Classes With Extra Members	
Schematic Object	PCB Object
[TP6]	