CHINNAPATLOLA NISHANTH REDDY | 21EC10014

ELECTRONICS & ELEC. COMM.ENGG. (B.Tech 4Y)

EDUCATION

Year	Degree/Exam	Institute	CGPA/Marks
2025	B.TECH	IIT Kharagpur	8.03 / 10
2021	TSBIE	Sri Chaitanya Junior Kalasala, Hyderabad	98.4%
2019	TSBE	Sri Chaitanya Techno School, Hyderabad	9.8 / 10

INTERNSHIPS

FPGA Implementation of 256-Point FFT for Keyword Spotting | IISc Bangalore **[May 2024 - July 2024]**

(Guide: Prof.Viveka)

- Implemented 8-stage **serial pipelined FFT** on the Nexys A7 Artix-7 FPGA, for a low-power keyword spotting chip
- Utilized the Radix-2^2 **Single-path delay feedback (SDF)** architecture with bit-width extension at each stage
- Analyzed FFT output using the **Google Speech Command dataset** reducing output bit-width from **31-bit** to **20-bit**
- Developed highly **parameterized Verilog code** for the FFT, enabling customization for various bit-widths
- Utilized IP cores such as **VIO** and **ILA** for real-time I/O monitoring and single port **RAM** for twiddle factor storage

PROJECTS

32-Bit Pipelined RISC Processor **[July 2024 - Aug 2024]**

- Implemented 32-bit pipelined RISC processor with **forwarding unit**, stall, flush control to handle pipeline hazards
- Integrated with **32 General purpose registers (GPRs)** along with the dedicated **Instruction** and **data memory**
- Designed to support **22 instructions** such as Arithmetic &Logic, Immediate addressing, Load &Store, and Branch
- Executed machine-level programs to compute the **GCD of two numbers** and **sort 10 integers** using bubble sort

Log Function Hardware **[Jan 2024]**

- Designed Log function hardware using digital circuits by leveraging the **Taylor expansion** and its approximation.
- Incorporated key components such as a **Leading One Detector (LOD)**, Adders, Subtractors, and Multipliers.
- Implemented a scaling mechanism using LOD to limit input values within [1,2], ensuring the design works effectively

Pulse Width Modulation for Laser Communication **[Dec 2023 - Jan 2024]**

- Designed and experimented with the transmitter and receiver using the **Pulse width modulation** technique
- Designed a **transmitter** with sawtooth and square wave generators, sample and hold circuit, and comparator
- Generated a PWM signal by comparing the **sampled signal** with the **sawtooth wave** using a comparator
- Designed a **receiver** with an **active low-pass filter** to demodulate and recover the transmitted message signal

COURSEWORK INFORMATION

Core: Digital Electronic Circuits* | Architectural Design of ICs | Analog Electronic Circuits* | VLSI Engineering* | Advanced Computer System Architecture | Analog Communication* | Digital Communication* | Digital Signal Processing* | Semiconductor Devices* | Network Theory* | Fundamentals of Embedded Control and Software | VLSI Interconnects | Computer Architecture
Programming: Programming and Data Structures | Algorithms | High Performance Computing and its Applications
Mathematics: Probability and Statistics | Advanced Calculus | Linear Algebra and Optimization
[*Indicates Courses with Laboratory Component]

SKILLS AND EXPERTISE

Programming Languages/Libraries: C | C++ | Python | HTML | CSS | Assembly Language | Fortran | OpenMPI
Hardware Description Languages: Verilog
EDA/Software Tools: Xilinx Vivado | MATLAB | LTspice | TINA TI | Arduino IDE

AWARDS AND ACHIEVEMENTS

JEE Mains 2021: Secured All India Rank of **1699** under top 0.15% amongst more than 10 lakh candidates
JEE Advanced 2021: Secured All India Rank of **2425** under top 1.6% amongst more than 1.5 lakh candidates
EAMCET Telangana 2021: Secured State Rank of **616** amongst more than 1.6 lakh candidates

EXTRA CURRICULAR ACTIVITIES

- Responsible (partially) for association of Entrepreneurship Cell IIT Kharagpur with **T-Hub Hyderabad** (Business incubator) as venue partner for conducting local startups meet (LSM) Hyderabad 2022
- Active volunteer of National Social Service (NSS) and participated in NSS winter camp for the duration of 7 days
- Actively participated in many social activities like Plantations, Education/Teaching in schools as part of NSS