**E0 217 Project Report (Aug 2023)**

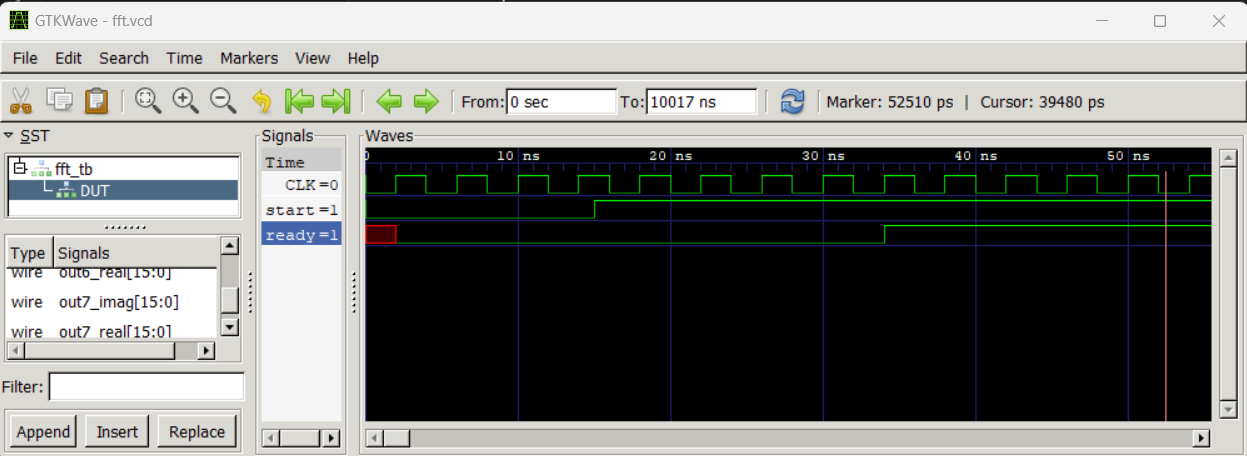
**Names and IISc Email IDs of Group Members:**

|  |  |  |
| --- | --- | --- |
|  | **Name** | **IISc Email ID** |
| 1. | **Guhan Rajasekar** | **guhanr@iisc.ac.in** |
| 2. | **Ujjwal Chaudhary** | **ujjwalc@iisc.ac.in** |

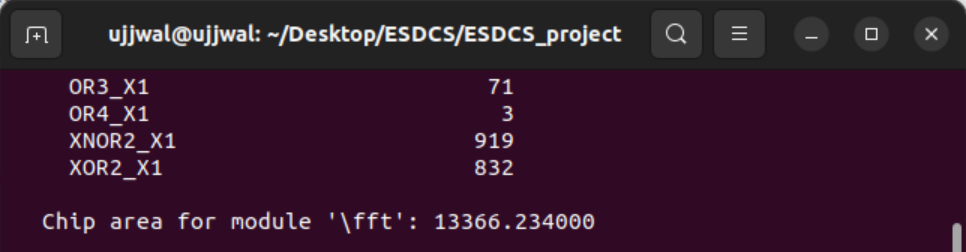
**Individual Contributions**

|  |  |  |
| --- | --- | --- |
|  | **Name** | **Contributions** |
| 1. | **Guhan Rajasekar** | * Implementation of FFT code ( without control signals) * Error computation between obtained and desired results * Report compilation |
| 2. | **Ujjwal Chaudhary** | * Optimization of code ( changing combinational blocks to sequential blocks) and making the code compatible with CLK signal and control signals like RST, WRITE, START , READY * Creation of test bench and simulation of design in GTK Wave. * Performed area, power and speed analysis. |

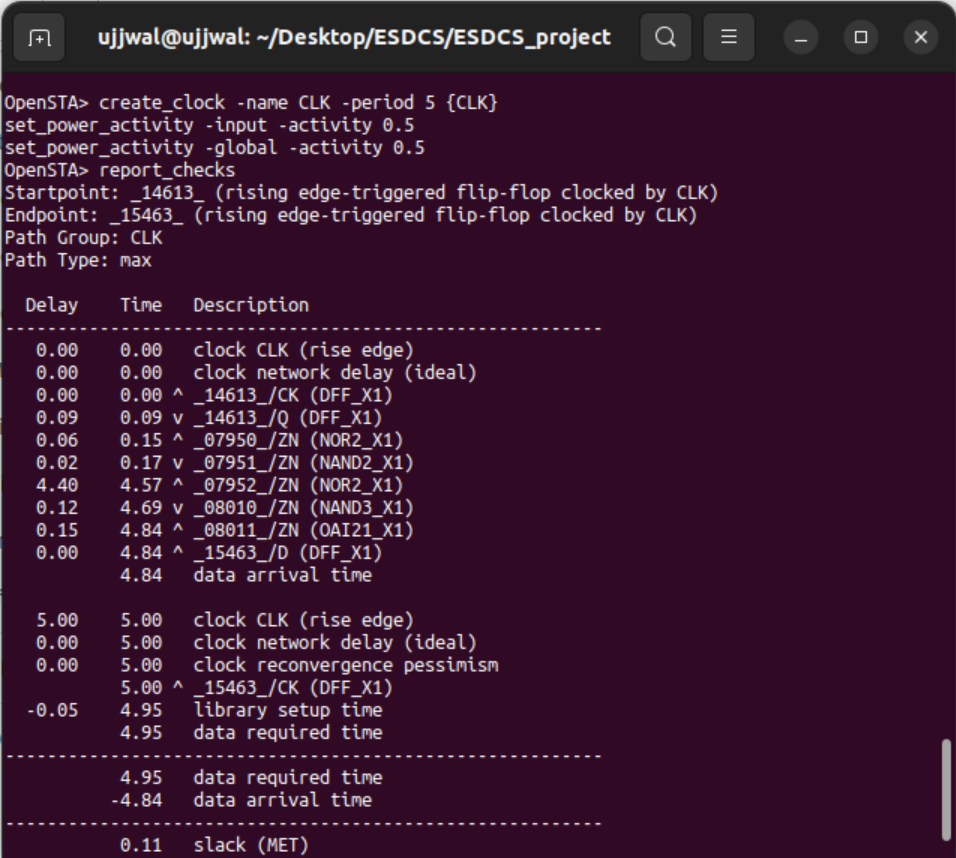
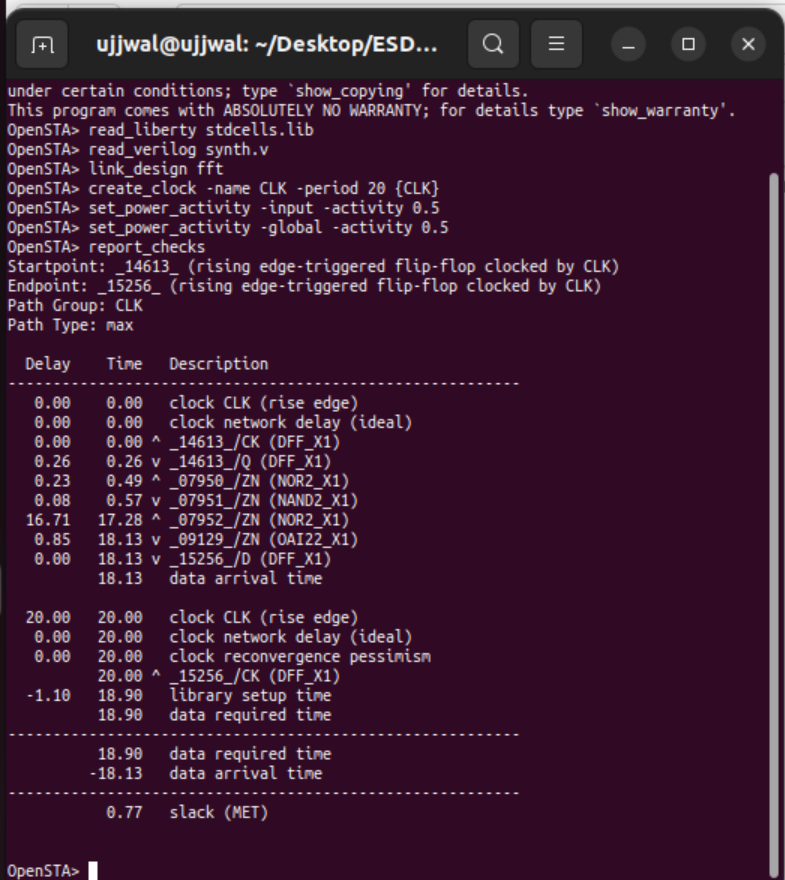
**Number of clock cycles per FFT computation:**

* Number of clock cycles between beginning of start and beginning of ready signal = 4.5
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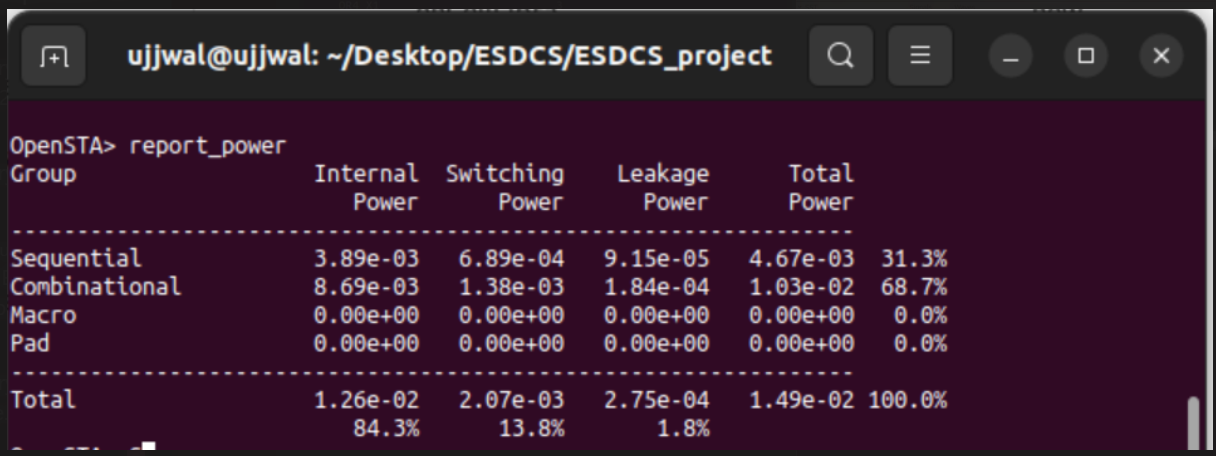
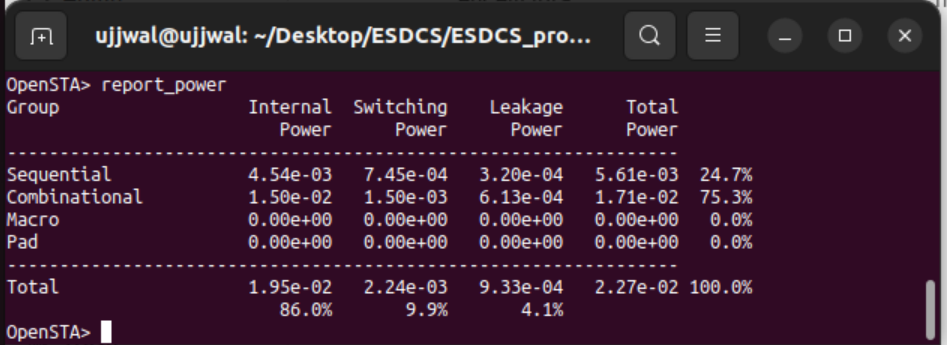
**Area of synthesized design:**

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* **13366.234 µm2**.

**Max clock frequency supported by the synthesized design:**

* **Typical corner, 25℃ and 1V**
* 
* This result is for typical corner, 25℃ and 1V.
* Here the clock period is 5ns – 0.11ns = **4.89ns**
* Here the slack period is 0.11ns.
* Operating frequency is **204.49 MHz**.
* **Slow corner, 25℃ , 1V**
* 
* This is for slow corner, 25℃ and 1V.
* Here the time period is 20ns – 0.77ns = 19.23ns
* Operating frequency = **52.002 MHz.**

**Power Consumption of the synthesized design:**

* **Power Consumption in typical corner, 25℃ and 1V:**
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* The total power consumed at typical corner, 25℃ and 1V is **14.9mW**.
* **Power Consumption in FF corner,25℃ and 1V.**
* 
* Total power consumption at FF corner, 25℃ and 1V is **22.7mW**.

**Energy Consumption of synthesized design:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Corner Case** | **Power Consumption** | **Operating Frequency** | **Energy Consumption** |
| Typical , 25℃ , 1V | 14.9mW | 204.49MHz | 72.86μJ |

**Dependence of Energy Consumption of the synthesized design on the clock frequency:**

* For a given simulation case, energy consumed is inversely related to the operating frequency.
* As the operating frequency increases, the energy consumed decreases and vice-versa.

**Maximum absolute error when computing FFT of {0, 1, 2, 3, 4, 5, 6, 7}**

* Let the 8-point FFT result be denoted as X(0), X(1), X(2), X(3), X(4), X(5), X(6) and X(7)
* Here a **decimal point has been added in the obtained results to indicate there are 8 bits for the fractional part, 7 bits for the decimal part and MSB is the sign bit.** This holds true for both real and imaginary parts.
* In the calculation of error, is considered as **1.414**.

1. **X(0) :**

* Expected = 28 + j0
* Obtained = (1c.00 + j00.00)H = 28 + j0
* Absolute Error = 0

1. **X(1)**

* Expected = -4.0 + j 9.656
* Obtained = (fc.00 + j09.a0)H = -4 + j9.625
* Absolute Error = |(-4.0 + j 9.656) – (-4 + j9.625) | = 0.031

1. **X(2)**

* Expected = -4 + j4
* Obtained = (fc.00 + j04.00)H = (-4 + j4)
* Absolute Error = 0

1. **X(3)**

* Expected = -4 + j1.656
* Obtained = (fc.00 + j01.a0)H  = -4 + j1.625
* Absolute Error = |(-4 + j1.656) – (-4 + j1.625) | = 0.031

1. **X(4)**

* Expected = -4 + j0
* Obtained = (fc.00 + j00.00)H = -4 + j0
* Absolute Error = 0

1. **X(5)**

* Expected = -4 – j1.656
* Obtained = (fc.00 + jfe.60)H = (-4 – j1.402)
* Absolute Error = |(-4 – j1.656 ) – (-4 – j1.402) | = 0.254

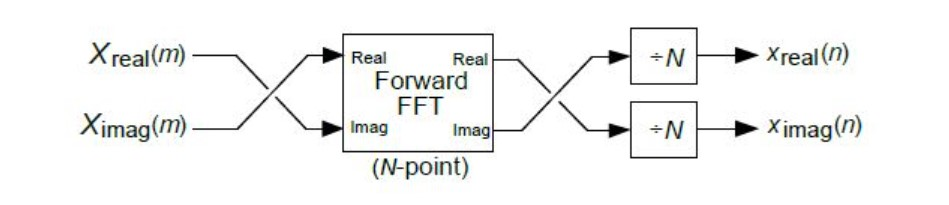
1. **X(6)**

* Expected = -4.0 – j4.0
* Obtained = (fc.00 + jfc.00)H = -4 - j4
* Absolute Error = 0

1. **X(7)**

* Expected = -4 – j9.656
* Obtained = (fc.00 + jf6.60)H = -4 – j9.625
* Absolute Error = | (-4 – j9.656 ) – (-4 – j9.625) | = 0.031

**Modifying the fft circuit to compute inverse fft**

* Inverse fft can be computed using Data Swapping technique, as shown below:
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* The real part of FFT input is fed as imaginary input to the circuit and the imaginary part of FFT is fed as real input to the circuit.
* The real portion of the output gives imaginary part of expected time domain sequence scaled by N and the imaginary part of the output gives the real part of the time domain sequence scaled by N.
* To get the desired outputs, we divide them by N.

**Design Details:**