E3: 231 Digital Systems Design with FPGAs

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The objective of these Lab exercises is to get used to the Verilog constructs and the different Tool features, along with implementing useful combinational and sequential logic.

1. Write Verilog code to implement a 4-bit, 4-to-1 multiplexer. Do the functional and timing simulation. Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1)

   Submit the source Verilog codes, RTL blocks, Resource utilization, Timing report, and timing (functional and post-route) simulation waveforms.

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2. Write Verilog model with continuous assignment for a 4-bit carry look-ahead adder. Do the functional and timing simulation. Target Device is Xilinx Artix-7 XC7A35T-ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1)

   Show the source Verilog codes, RTL blocks, Resource utilization, Timing report, and timing (functional and post-route) simulation waveforms.

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3. a) Design a synchronous mod-10 up counter (with synchronous active low reset) using Verilog. Simulate and test with a testbench.
   b) Add the following functionalities as discussed in the class:
      a. Hold previous value
      b. Count up
      c. Count down
      d. Count up-down (first up, then down)
      e. Load an input value
      f. Local synchronous reset
   c) Parameterize and make the counter behave as a mod-N up-down counter ($N \leq 16$).
   d) Now, let us implement the design on the FPGA. To visualize the counter you designed using the LEDs on the Basys3 board, the clock frequency must be reduced from 100MHz (default Basys3 board frequency) to ~1 Hz. Design a clock frequency divider block (basic implementation) to achieve this. Map N to

the switches available on the board. Also, convert the output to thermometric code for better visualization with the LEDs.

e) This internally generated clock is not part of the clock tree synthesis and might cause timing violations as dedicated FPGA clock generators do not generate it. Hence, a slower clock enable signal is recommended, which allows all logic in the design to be driven by the same clock. Design this circuit and demonstrate the results on the FPGA.

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Think about the schematic of the circuit before coding in each case. Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). Do the functional simulation. After synthesis, verify the RTL schematic. Do the Implementation and generate bitstream. Note down the resource utilization in terms of LUTs and FFs in each case.

Submit the source Verilog codes, timing simulation waveforms, a brief report on the resource utilization, and the timing reports.

[60]

Resource utilization in terms of the number of slices used could be found in Implemented Design => Report Utilization or in Project Summary (Menu => Window => Project Summary). Worst case delay could be found in Implemented Design => Report Timing Summary