E3: 231 Digital Systems Design with FPGAs

DESE, Indian Institute of Science, Bangalore

Final Project

Include the following sections in your final project report (overall 6-8 pages):

1. Introduction and Motivation
2. Background Study
3. Design Space Exploration and Design Strategies (explain the strategies used for coding optimizations for datapath and control flow – pipelining, loop unrolling, clock gating, etc)
4. Implementation Challenges
5. Results
6. Conclusion
7. References

Demo needs to be shown on the FPGA along with the team presentation. Submit the Verilog codes, test bench, and constraints file along with this report in a zipped folder. Do not include the codes in the report – you may include necessary post-implementation timing simulation waveforms/results and power, area, and performance numbers in the report.