E3: 231 Digital Systems Design with FPGAs

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The objective of this Lab exercise is to learn about pipelining of Datapath and handling asynchronous inputs that are encountered in many real-world scenarios. Try to code concisely.

1. Do the pipelining of the signed 8-bit Radix-4 Booth Recoded Array Multiplier in HW-2 for maximum throughput.

Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). Do the functional simulation. After elaboration, verify the RTL schematic. Do the implementation, timing analysis and the timing simulation.

Compare the area (resource utilization in terms of LUTs, Flip-flops and slices), delay performance, and throughput of the pipelined Radix-4 Booth Recoded Array multiplier with the non-pipelined Radix-4 Booth Recoded Array multiplier of HW-2.

Note the area (resource utilization) and performance (delay).

Submit the source Verilog codes, post-route timing simulation waveforms, and a brief report on the resource utilization in terms of Slices/LUTs and delay performance.

2. For the up-down counter designed in HW1 (Question 3e), instead of generating the enable internally, take it as input from a push button on the board. Whenever you press the push button (asynchronous input), the counter should increment/decrement with the 100MHz clock.
a) Implement this and report if you observe any anomaly (bouncing effects/metastability) with the counter behavior.
b) Implement a debouncing circuit that converts the asynchronous input into a narrow pulse. Use a 2-stage synchronizer and a counter circuit (count till ~20ms for the input to settle) to implement this debouncer.

Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). Do the functional simulation. After synthesis, verify the RTL schematic. Do the Implementation and generate bitstream. Note down the resource utilization in terms of LUTs and FFs in each case.

Demo needs to be shown on the FPGA. Submit the source Verilog codes, timing simulation waveforms, a brief report on the resource utilization, and the timing reports.