Digital System Design with FPGA Assignment 1

Guhan Rajasekar, guhanr@iisc.ac.in, MTech ESE, 22410, DESE, IISc

I FOUR BIT 4:1 MUX

1.1 RTL Block

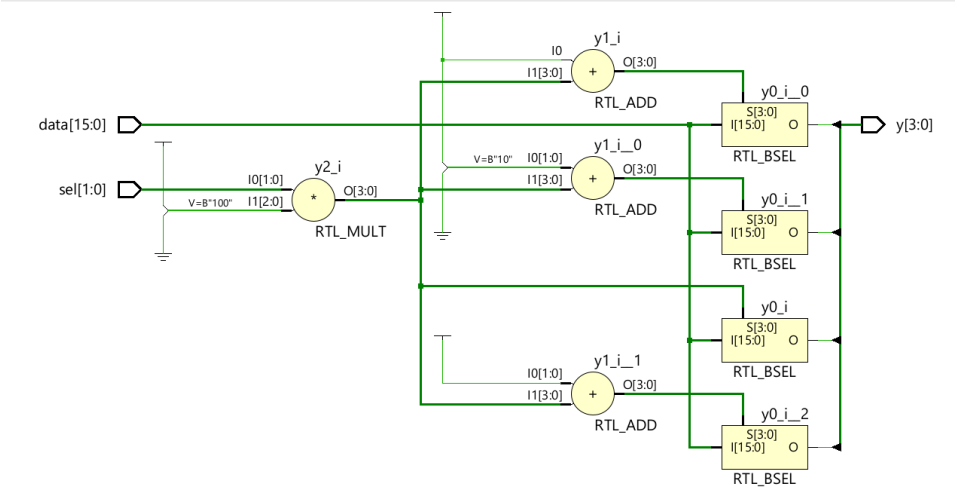

Figure 1: RTL Block of four bit wide 4:1 MUX

1.2 Resource Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)
mux4	4	1	4	22

Figure 2: Resource Utilization of four bit 4:1 Mux

1.3 Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	4	Total Number of Endpoints:	4	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Figure 3: Timing Summary of 4 bit wide 4:1 MUX

Total Negative Slack of Setup time and *Total Hold Slack* are 0ns each. This implies no timing violations. As this is a combinational circuit, this result is expected.

1.4 Functional Simulation Waveform

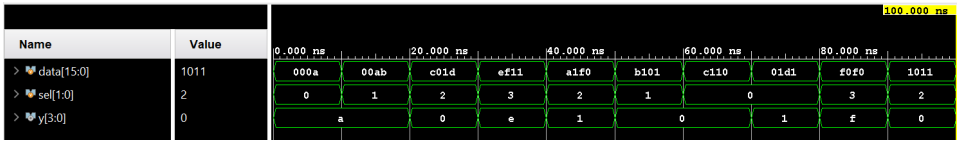

Figure 4: Functional Simulation Waveform of four bit wide 4:1 Mux

1.5 Post Route Simulation Waveform

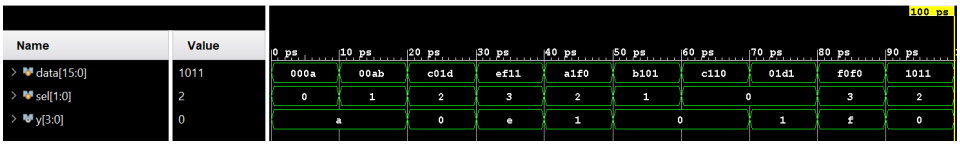

Figure 5: Post Route Simulation Waveform of four bit wide 4:1 Mux

1.6 Design Summary of four bit wide 4:1 MUX

Data flow style of programming was used to implement the four bit wide 4:1 MUX. Data was a 16 bit vector. The output was a 4 bit wire. The output wires were assigned values using the *assign* statement based on the value of the select lines.

II FOUR BIT CARRY LOOK AHEAD ADDER

2.1 RTL Block

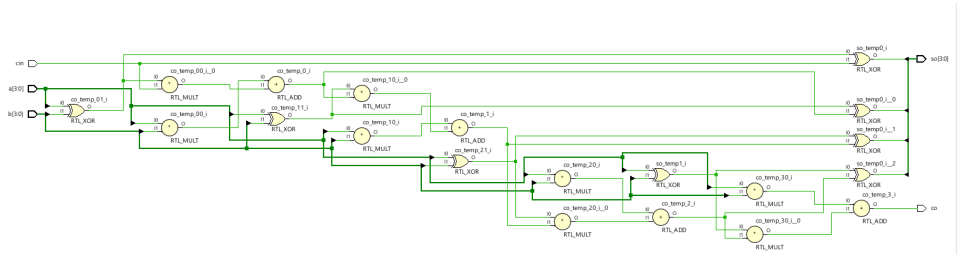

Figure 6: RTL Block of CLA

2.2 Resource Utilization

Name 1	Slice LUTs (20800)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)
N cla	4	1	4	14

Figure 7: Resource Utilization of CLA

2.3 *Timing Report*

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	5	Total Number of Endpoints:	5	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Figure 8: Timing Report of 4 bit Carry Look Ahead Adder

The Carry Look Ahead Adder is a combinational circuit. Hence the *Total Negative Slack of Setup Time* and the *Total Hold Slack* are 0ns each. This implies no timing violations.

2.4 *Functional Simulation Waveform*

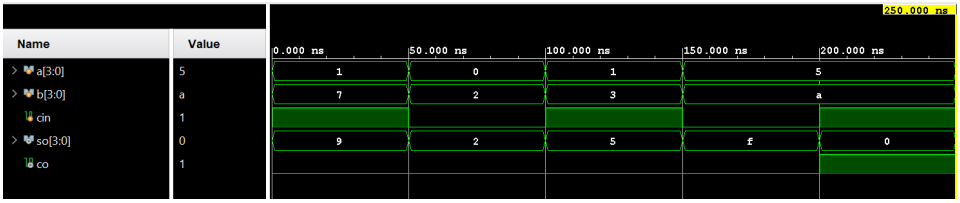

Figure 9: Functional Simulation waveform of CLA

2.5 *Post Route Simulation Waveform*

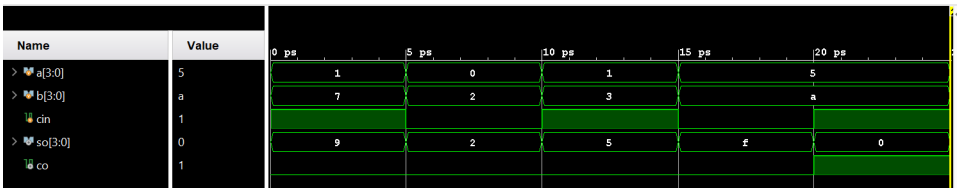

Figure 10: Post Route Simulation waveform of CLA

2.6 *Design summary of 4 bit Carry Look Ahead Adder*

As per the requirement, continuous assign statements were used to implement the sum and carry output bits. The results were stored in a register at the end, to avoid the design having only assign statements. Design was tested with appropriate inputs given from a testbench verilog code.

III MOD N COUNTER WITH SYNCHRONOUS ACTIVE LOW RESET

3.1 RTL Block

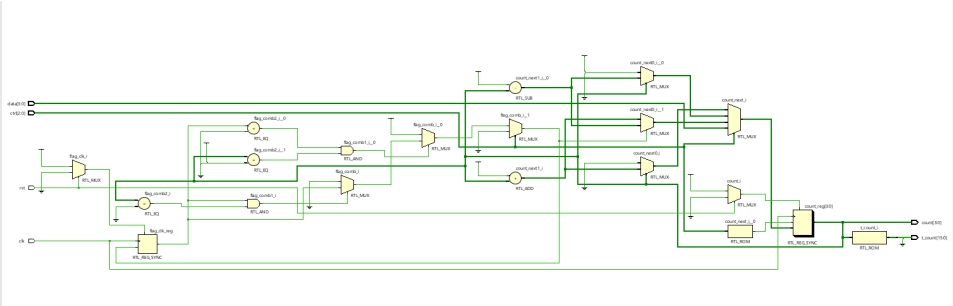

Figure 11: RTL Block of Counter

3.2 Resource Utilization

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)	BUFGCTRL (32)
modcounter	30	5	18	30	29	1

Figure 12: Resource Utilization of Counter

3.3 Timing Summary

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.510 ns	Worst Hold Slack (WHS):	0.065 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	32	Total Number of Endpoints:	32	Total Number of Endpoints:	6

All user specified timing constraints are met.

Figure 13: Timing Summary of Counter

Total Negative Slack of Setup time and *Total Hold Slack* are 0ns each. This implies no timing violations.

3.4 Functional Simulation

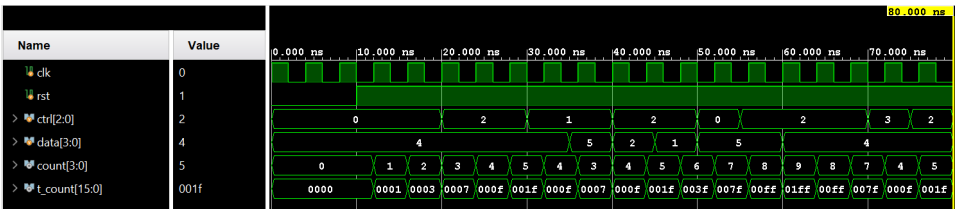

Figure 14: Functional Simulation of Counter

3.5 Post Route Simulation

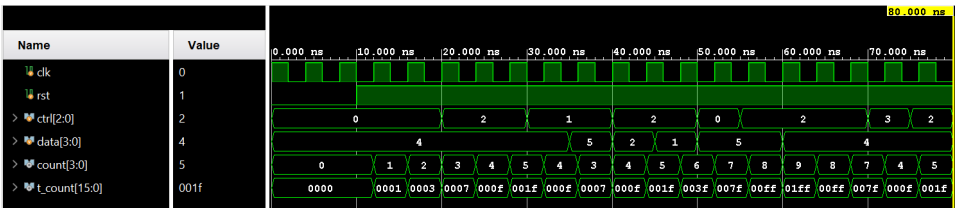

Figure 15: Post Route Simulation of Counter

3.6 Desgin Summary of Counter

A Mod N counter was implemented in Verilog with the following features:

- Local Synchronous Reset
- Up Count (Ctrl = 000)
- Down Count (Ctrl = 001)
- Up Down Count (Ctrl = 010)
- Load Data (Ctrl = 011)
- Hold Data (Ctrl = 100,101,110,111)

A combinational always block was used to calculate the next count value and a clocked always block was used to update the count value with the value that was computed in the combinational always block. Variable N was parameterized. This makes it possible to vary the counter's functionality by just changing the value of N in the code.

To implement the code in FPGA, another register variable was used to implement a scaled down version of the original clock signal. The frequency of the default clock signal of the FPGA board is 100MHz. For visualization on FPGA, another clock signal with frequency 1Hz was used.