FPGA Assignment 3

Guhan Rajasekar, Mtech ESE , 22410, DESE, IISc

I INTRODUCTION

- This report is a summary on assignment 3 of the course *Digital System Design with FPGA*.

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II PIPELINED BOOTH MULTIPLIER

2.1 Pipelined Architecture

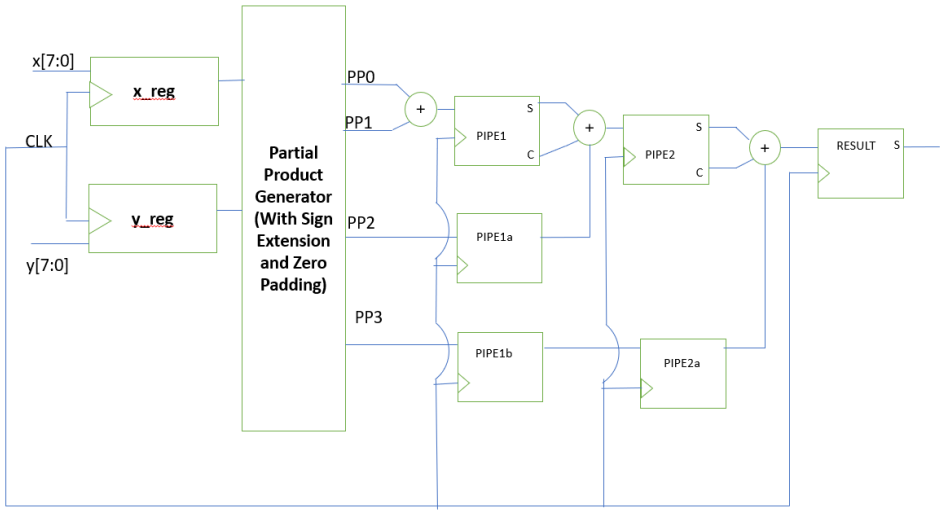

Figure 1: Block Diagram of Pipelined Booth Multiplier

- In the above block diagram, the reset signal has been omitted to keep the block diagram simple. However, all the clocked elements in the circuit also have a synchronous active low reset.

2.2 Post Route Timing Simulation Waveform

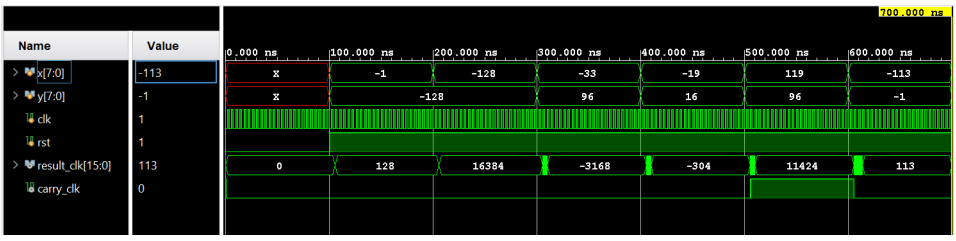

Figure 2: Post Route Timing Simulation of Pipelined Booth Multiplier

- The above waveform shows the simulation results that were obtained after implementation.

2.3 *Resource Utilization of Un-pipelined Booth Multiplier*

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)	BUFGCTRL (32)
N booth_multiplier	70	33	24	70	35	1

Figure 3: Resource Utilization Of Un-pipelined Booth Multiplier

2.4 *Resource Utilization of Pipelined Booth Multiplier*

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)	BUFGCTRL (32)
N booth_multiplier	67	64	29	67	35	1

Figure 4: Resource Utilization Of Pipelined Booth Multiplier

- The number of slice registers in the pipelined multiplier is more when compared with the number of slice registers in the un-pipelined booth multiplier.

2.5 *RTL Schematic of the Pipelined Booth Multiplier*

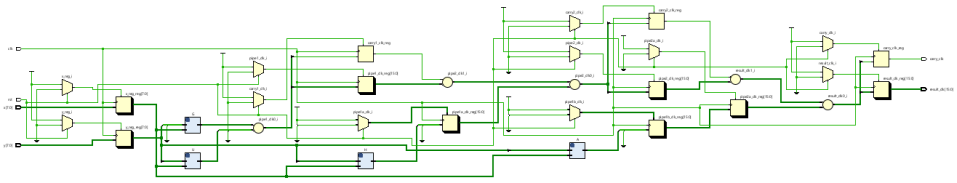

Figure 5: RTL Schematic of Pipelined Booth Multiplier

2.6 *Delay Performance of Un-Pipelined Booth Multiplier*

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.048 ns	Worst Hold Slack (WHS):	0.070 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	83	Total Number of Endpoints:	83	Total Number of Endpoints:	34

All user specified timing constraints are met.

Figure 6: Timing Summary of Un-pipelined Booth Multiplier

2.7 *Delay Performance of Pipelined Booth Multiplier*

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.250 ns	Worst Hold Slack (WHS):	0.062 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	188	Total Number of Endpoints:	188	Total Number of Endpoints:	95

All user specified timing constraints are met.

Figure 7: Timing Summary of pipelined Booth Multiplier

- Minimum possible T_{clk} of un-pipelined booth multiplier = 10ns - 0.048ns = 9.952ns.
- Maximum operating frequency of un-pipelined booth multiplier = (1/9.952ns) = 100.482MHz.
- Minimum possible T_{clk} of pipelined booth multiplier is 10ns - 5.25ns = 4.75ns.
- Maximum operating frequency of pipelined booth multiplier = (1/9.849ns) = 210.526MHz.
- As we can observe, the pipelined booth multiplier offers higher operating frequency than the un-pipelined booth multiplier.

2.8 Throughput of Pipelined Booth Multiplier

- Here, we define the throughput of the multiplier as the number of outputs that can be produced in unit time (1 second).
- At steady state, we can say that we get one output (one result) for every clock cycle.
- Hence we get one output for every 4.75ns.
- So, the number of outputs obtained per unit time (in 1 second) is given by :

$$\frac{1}{4.75n} = 210.526 * (10^6). \tag{1}$$

III UP-DOWN COUNTER WITH SYNCHRONIZER AND DE-BOUNCER

3.1 Architecture of the Up-Down Counter

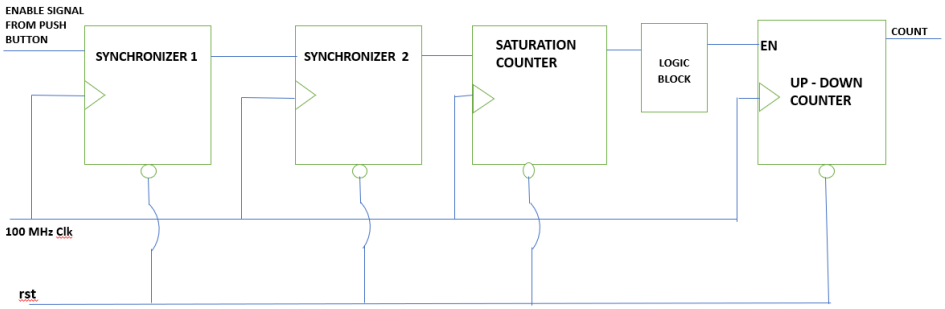

Figure 8: Architecture of Up-Down Counter

3.2 RTL Schematic

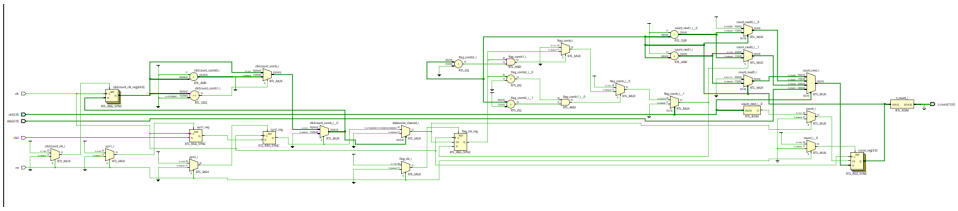

Figure 9: RTL Schematic of Up-Down Counter

- For clarity purposes, the RTL schematic is also submitted along with the report

3.3 *Simulation Waveform of Up-Down Counter*

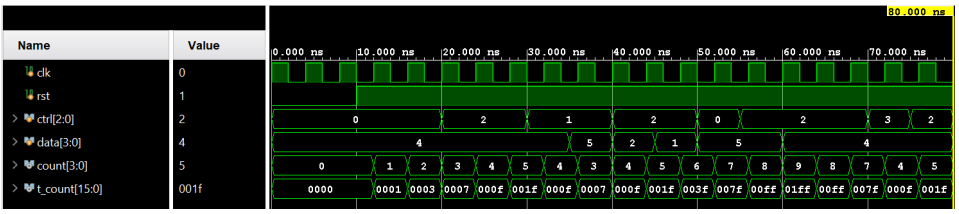

Figure 10: simulation Waveform of Up-Down Counter

3.4 *Timing Performance*

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.237 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	59	Total Number of Endpoints:	59	Total Number of Endpoints:	29

All user specified timing constraints are met.

Figure 11: Timing Report of the Up-Down Counter

- Minimum T_{clk} is(10ns-4.237ns) = 5.763ns.
- As the slack is positive, we see that there are no timing violations

3.5 *Resource Utilization of Up-Down Counter*

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)	BUFGCTRL (32)
N modcounter	76	28	26	76	26	1

Figure 12: Resource Utilization of the Up-Down Counter

3.6 *Design and Observations*

- First the enable signal was given through one of the push buttons on the FPGA board.
- When this was done, it was observed that the count was incremented and decremented in a very erratic manner. This is due to mechanical de-bounce present in the switches of the FPGA board.
- First, to synchronize the asynchronous input, we used a two stage synchronizer.
- Then to overcome the de-bounce effect, the output of the synchronizer circuit was passed through a saturating counter.
- Whenever the button signal was read as high, this counter used to count up. And whenever the singal was low, the counter value was reset.
- At the end of 20ms, the status of enable signal was checked again. If it was high, it was considered as a valid press and appropriate action was taken.