

## TSDxx Unidirectional TVS Diodes in SOD-323

### 1 Features

- IEC 61000-4-2 ESD protection:
  - $\pm 30\text{kV}$  contact discharge
  - $\pm 30\text{kV}$  air gap discharge
- IEC 61000-4-5 surge protection:
  - 7-60A (8/20 $\mu\text{s}$ )
- IO capacitance < 20pF (typical)
- Ultra low leakage current: 50nA (maximum)
- Industrial temperature range:  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$
- Industry standard SOD-323 leaded package (2.65mm  $\times$  1.3mm)

### 2 Applications

- I/O Protection
- Power Line Protection
- [USB VBUS](#)
- Grid infrastructure
- Portable electronics

### 3 Description

The TSDxx are a family of unidirectional TVS protection diodes designed for clamping harmful transients such as ESD and surge. The TSDxx devices are rated to dissipate ESD strikes up to  $\pm 30\text{kV}$  (contact and air gap discharge) and also meets the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

Combining the robust clamping performance and low capacitance of this device, TSDxx are excellent TVS diodes to protect both data and power lines in many different applications.

The TSDxx family is offered in the industry standard, leaded SOD-323 package to enable easy solderability.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TSDxx	DYF (SOD-323, 2)	2.65mm $\times$ 1.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Pin Configuration and Functions

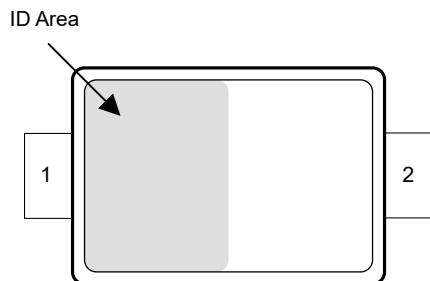


Figure 4-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	IO	I/O	Protected Channel
2	GND	GND	Ground. Connect to ground.

(1) I = input, O = output. GND = ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

Parameter		DEVICE	MIN	MAX	UNIT
$P_{PP}$	IEC 61000-4-5 power ( $t_p - 8/20\mu s$ ) at 25°C	TSD03		170	W
		TSD05		529	W
		TSD12		300	W
		TSD15		300	W
		TSD18		300	W
		TSD24		250	W
		TSD36		300	W
$I_{PP}$	IEC 61000-4-5 current ( $t_p - 8/20\mu s$ ) at 25°C	TSD03		25	A
		TSD05		60	A
		TSD12		18	A
		TSD15		15	A
		TSD18		15	A
		TSD24		9	A
		TSD36		7	A
$T_A$	Ambient Operating Temperature		-55	150	°C
$T_{stg}$	Storage Temperature		-65	155	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings - JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2500$	V
		Charged device model (CDM), per JEDEC specification JS-002 <sup>(2)</sup>	$\pm 1000$	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 ESD Ratings - IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	$\pm 30000$	V
		IEC 61000-4-2 air-gap discharge	$\pm 30000$	

### 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$T_A$	Operating free-air temperature	-55		150	°C

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TSD03	TSD05	TSD12 / TSD15 / TSD18 / TSD24 / TSD36	UNIT
		DYF (SOD-323)	DYF (SOD-323)	DYF (SOD-323)	
		2 PINS	2 PINS	2 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	739.2	672.0	693.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	287.7	230.5	254.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	605.5	541.4	566.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	118.4	64.4	78.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	591.1	527.5	552.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 5.6 Electrical Characteristics - TSD03

At T<sub>A</sub> = 25°C unless otherwise noted <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>RWM</sub>	Reverse stand-off voltage	I <sub>IO</sub> < 50nA, across operating temperature range			3.6	V
V <sub>BR</sub>	Breakdown voltage	I <sub>IO</sub> = 1mA, IO to GND		4.5		V
I <sub>LEAK</sub>	Reverse leakage current	V <sub>IO</sub> = 3.6V, IO to GND		5	50	nA
V <sub>FWD</sub>	Forward voltage	I <sub>IO</sub> = 1mA, GND to IO		0.8		V
V <sub>CLAMP</sub>	Surge clamping voltage, t <sub>p</sub> = 8/20μs <sup>(2)</sup>	I <sub>PP</sub> = 12A, IO to GND		6.3		V
		I <sub>PP</sub> = 25A, IO to GND		7.7		V
		I <sub>PP</sub> = 12A, GND to IO		3		V
		I <sub>PP</sub> = 25A, GND to IO		4.9		V
	TLP clamping voltage, t <sub>p</sub> = 100ns	I <sub>PP</sub> = 16A, IO to GND		6.5		V
		I <sub>PP</sub> = 16A, GND to IO		3.4		V
C <sub>L</sub>	Line capacitance	V <sub>IO</sub> = 0V, V <sub>p-p</sub> = 30mV, f = 1MHz, IO to GND		4.5		pF

- (1) Typical parameters are measured at 25°C

- (2) Nonrepetitive current pulse 8 to 20μs exponentially decaying waveform according to IEC 61000-4-5

## 5.7 Electrical Characteristics - TSD05

At  $T_A=25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage $I_{IO} < 50\text{nA}$ , across operating temperature range			5.5	V
$V_{BR}$	Breakdown voltage $I_{IO} = 1\text{mA}$ , IO to GND	6			V
$I_{LEAK}$	Reverse leakage current $V_{IO} = 5.5\text{V}$ , IO to GND		5	50	nA
$V_{FWD}$	Forward voltage $I_{IO} = 1\text{mA}$ , GND to IO		0.7		V
$V_{CLAMP}$	$I_{PP} = 24\text{A}$ , IO to GND		8	11.5	V
	$I_{PP} = 60\text{A}$ , IO to GND		9	15	V
	$I_{PP} = 60\text{A}$ , GND to IO		5.5		V
	$I_{PP} = 16\text{A}$ , IO to GND		7.5		V
	$I_{PP} = 16\text{A}$ , GND to IO		2.5		V
$C_L$	$V_{IO} = 0\text{V}$ ; $f = 1\text{MHz}$ , IO to GND		19		pF

(1) Typical parameters are measured at  $25^\circ\text{C}$

(2) Nonrepetitive current pulse 8 to  $20\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5

## 5.8 Electrical Characteristics - TSD12

At  $T_A=25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage $I_{IO} < 50\text{nA}$ , across operating temperature range			12	V
$V_{BR}$	Breakdown voltage $I_{IO} = 10\text{mA}$ , IO to GND		12.7		V
$I_{LEAK}$	Reverse leakage current $V_{IO} = 12\text{V}$ , IO to GND		2	20	nA
$V_{FWD}$	Forward voltage $I_{IO} = 1\text{mA}$ , GND to IO		0.7		V
$V_{CLAMP}$	$I_{PP} = 1\text{A}$ , IO to GND			18	V
	$I_{PP} = 5\text{A}$ , IO to GND			19	V
	$I_{PP} = 18\text{A}$ , IO to GND			23	V
	$I_{PP} = 18\text{A}$ , GND to IO			8	V
	$I_{PP} = 16\text{A}$ , IO to GND		17		V
	$I_{PP} = 16\text{A}$ , GND to IO		3		V
$C_L$	$V_{IO} = 0\text{V}$ ; $f = 1\text{MHz}$ , IO to GND		12		pF

(1) Typical parameters are measured at  $25^\circ\text{C}$

(2) Nonrepetitive current pulse 8 to  $20\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5

## 5.9 Electrical Characteristics - TSD15

At  $T_A=25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
$V_{RWM}$	Reverse stand-off voltage			15	V	
$V_{BR}$	Breakdown voltage	$I_{IO} = 10\text{mA}$ , IO to GND	18.3		V	
$I_{LEAK}$	Reverse leakage current	$V_{IO} = 15\text{V}$ , IO to GND		2	20	nA
$V_{FWD}$	Forward voltage	$I_{IO} = 10\text{mA}$ , GND to IO		0.7	V	
$V_{CLAMP}$	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ <sup>(2)</sup>	$I_{PP} = 1\text{A}$ , IO to GND		25	V	
		$I_{PP} = 5\text{A}$ , IO to GND		26	V	
		$I_{PP} = 15\text{A}$ , IO to GND		31	V	
		$I_{PP} = 15\text{A}$ , GND to IO		7	V	
	TLP clamping voltage, $t_p = 100\text{ns}$	$I_{PP} = 16\text{A}$ , IO to GND		23	V	
		$I_{PP} = 16\text{A}$ , GND to IO		3	V	
$C_L$	Line capacitance	$V_{IO} = 0\text{V}$ ; $f = 1\text{MHz}$ , IO to GND		12	pF	

(1) Typical parameters are measured at  $25^\circ\text{C}$

(2) Nonrepetitive current pulse 8 to  $20\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5

## 5.10 Electrical Characteristics - TSD18

At  $T_A=25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
$V_{RWM}$	Reverse stand-off voltage			18	V	
$V_{BR}$	Breakdown voltage	$I_{IO} = 10\text{mA}$ , IO to GND	18.5		V	
$I_{LEAK}$	Reverse leakage current	$V_{IO} = 18\text{V}$ , IO to GND		2	20	nA
$V_{FWD}$	Forward voltage	$I_{IO} = 10\text{mA}$ , GND to IO		0.7	V	
$V_{CLAMP}$	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ <sup>(2)</sup>	$I_{PP} = 1\text{A}$ , IO to GND		25	V	
		$I_{PP} = 5\text{A}$ , IO to GND		26	V	
		$I_{PP} = 15\text{A}$ , IO to GND		31	V	
		$I_{PP} = 15\text{A}$ , GND to IO		7	V	
	TLP clamping voltage, $t_p = 100\text{ns}$	$I_{PP} = 16\text{A}$ , IO to GND		23	V	
		$I_{PP} = 16\text{A}$ , GND to IO		3	V	
$C_L$	Line capacitance	$V_{IO} = 0\text{V}$ ; $f = 1\text{MHz}$ , IO to GND		12	pF	

(1) Typical parameters are measured at  $25^\circ\text{C}$

(2) Nonrepetitive current pulse 8 to  $20\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5

## 5.11 Electrical Characteristics - TSD24

At  $T_A=25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage $I_{IO} < 50\text{nA}$ , across operating temperature range			24	V
$V_{BR}$	Breakdown voltage $I_{IO} = 10\text{mA}$ , IO to GND	24.8			V
$I_{LEAK}$	Reverse leakage current $V_{IO} = 24\text{V}$ , IO to GND		2	20	nA
$V_{FWD}$	Forward voltage $I_{IO} = 10\text{mA}$ , GND to IO		0.7		V
$V_{CLAMP}$	$I_{PP} = 1\text{A}$ , IO to GND			32	V
	$I_{PP} = 5\text{A}$ , IO to GND			36	V
	$I_{PP} = 9\text{A}$ , IO to GND			39	V
	$I_{PP} = 9\text{A}$ , GND to IO			4	V
	$I_{PP} = 16\text{A}$ , IO to GND		33		V
	$I_{PP} = 16\text{A}$ , GND to IO		3		V
$C_L$	Line capacitance $V_{IO} = 0\text{V}$ ; $f = 1\text{MHz}$ , IO to GND	12			pF

(1) Typical parameters are measured at  $25^\circ\text{C}$

(2) Nonrepetitive current pulse 8 to  $20\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5

## 5.12 Electrical Characteristics - TSD36

At  $T_A=25^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage $I_{IO} < 50\text{nA}$ , across operating temperature range			36	V
$V_{BR}$	Breakdown voltage $I_{IO} = 10\text{mA}$ , IO to GND	37.1			V
$I_{LEAK}$	Reverse leakage current $V_{IO} = 36\text{V}$ , IO to GND		2	20	nA
$V_{FWD}$	Forward voltage $I_{IO} = 10\text{mA}$ , GND to IO		0.7		V
$V_{CLAMP}$	$I_{PP} = 1\text{A}$ , IO to GND			44	V
	$I_{PP} = 5\text{A}$ , IO to GND			59	V
	$I_{PP} = 7\text{A}$ , IO to GND			67	V
	$I_{PP} = 7\text{A}$ , GND to IO			4	V
	$I_{PP} = 16\text{A}$ , IO to GND		53		V
	$I_{PP} = 16\text{A}$ , GND to IO		3		V
$C_L$	Line capacitance $V_{IO} = 0\text{V}$ ; $f = 1\text{MHz}$ , IO to GND	12			pF

(1) Typical parameters are measured at  $25^\circ\text{C}$

(2) Nonrepetitive current pulse 8 to  $20\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5

## 5.13 Typical Characteristics

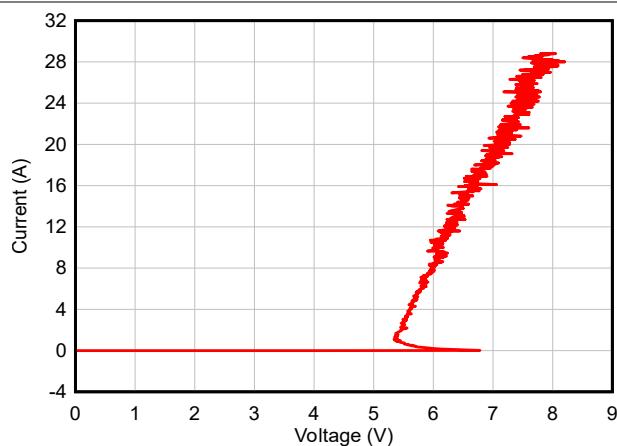


Figure 5-1. Positive TLP Curve - TSD03

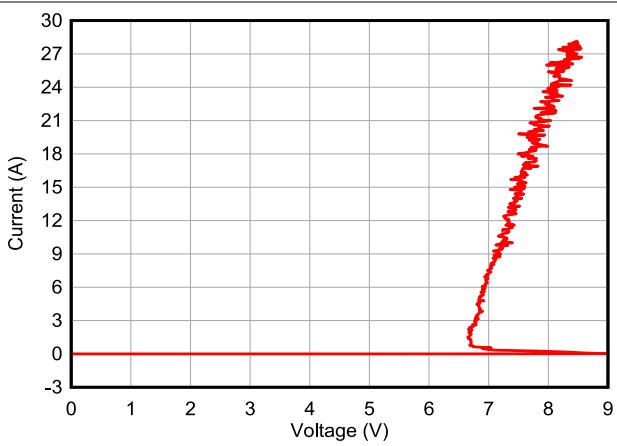


Figure 5-2. Positive TLP Curve - TSD05

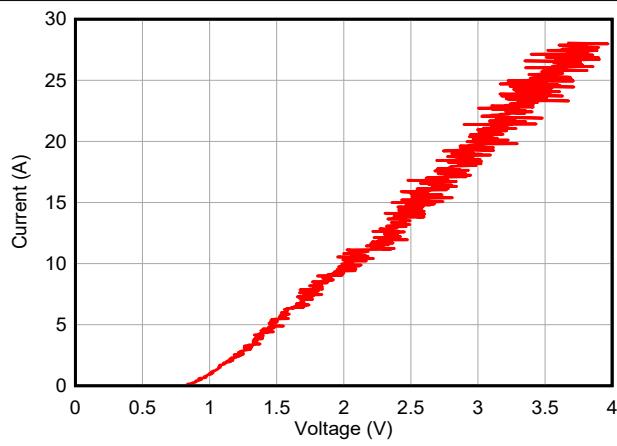


Figure 5-3. Negative TLP Curve - TSD05

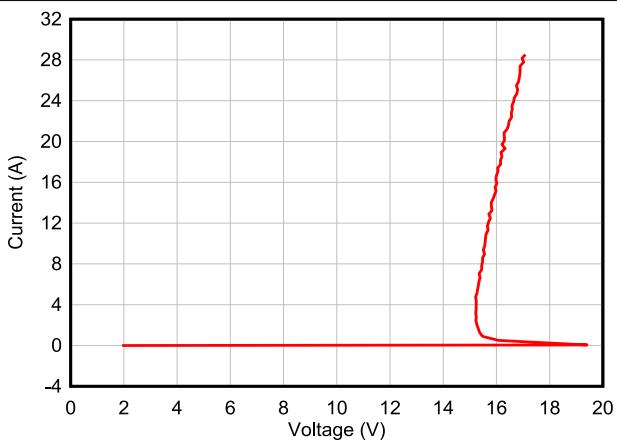


Figure 5-4. Positive TLP Curve - TSD12

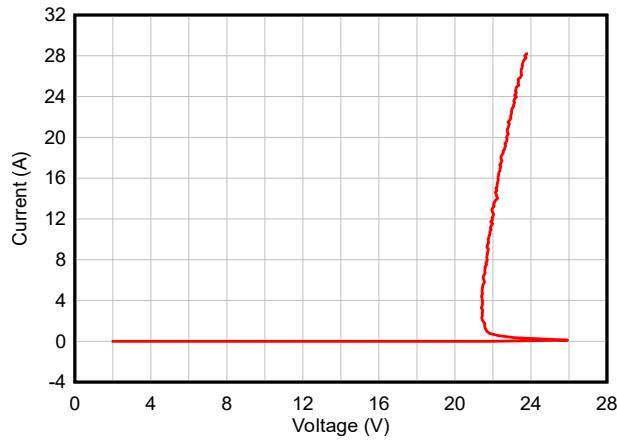


Figure 5-5. Positive TLP Curve - TSD15

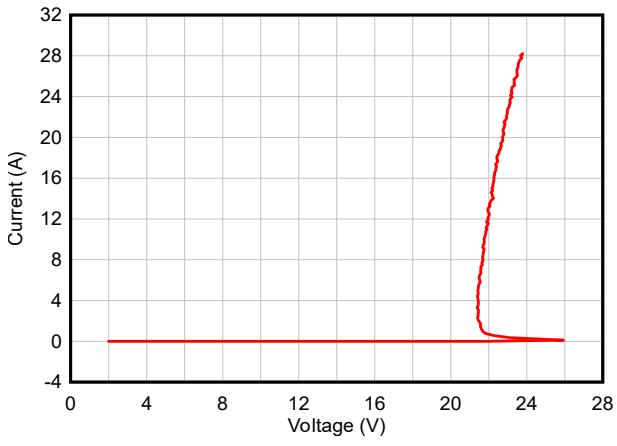


Figure 5-6. Positive TLP Curve - TSD18

## 5.13 Typical Characteristics (continued)

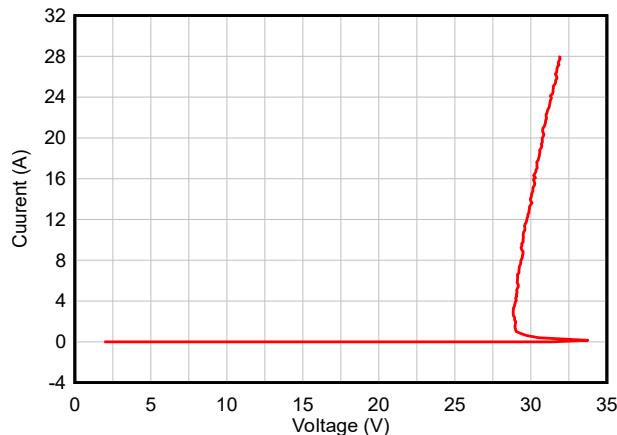


Figure 5-7. Positive TLP Curve - TSD24

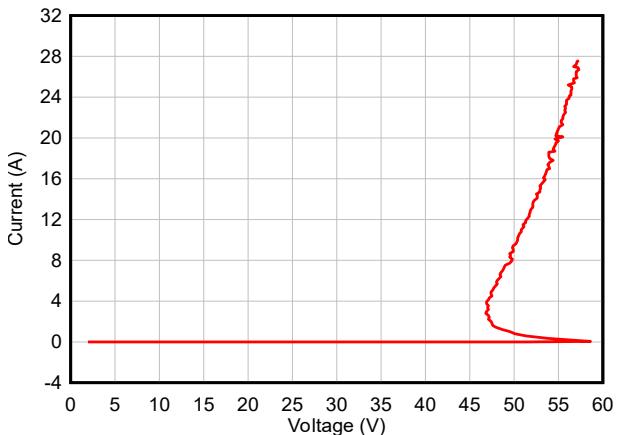


Figure 5-8. Positive TLP Curve - TSD36

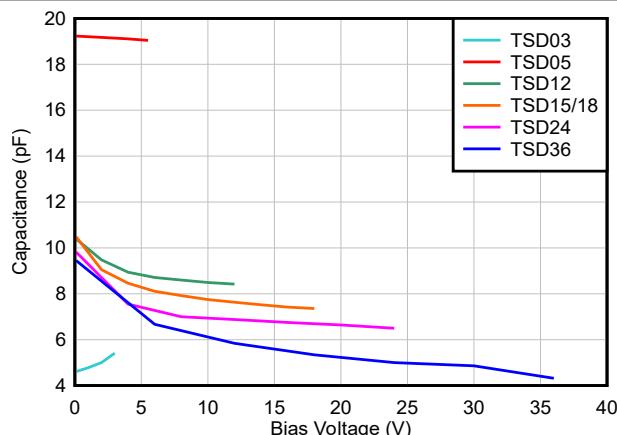


Figure 5-9. Capacitance vs Bias Voltage

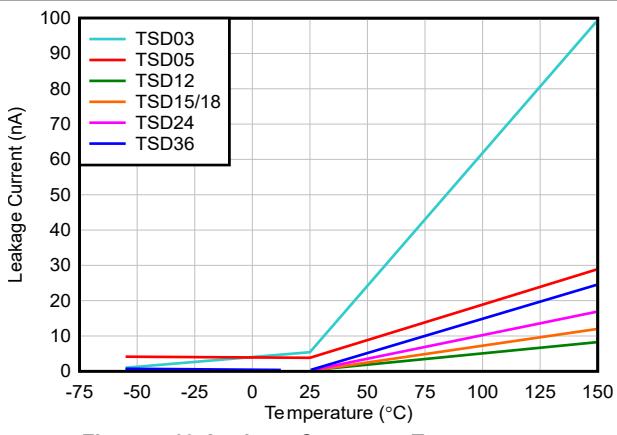


Figure 5-10. Leakage Current vs Temperature

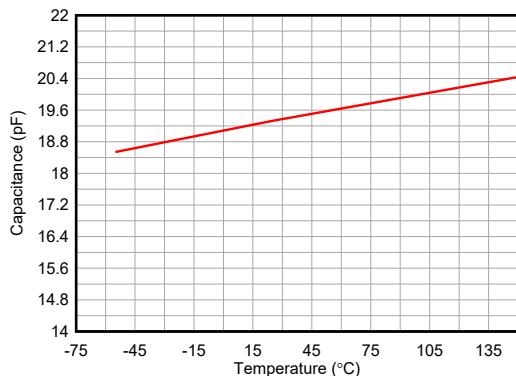


Figure 5-11. Temperature vs Capacitance - TSD05

## 6 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 6.1 Application Information

The TSDxx family are TVS diodes that provide a path to ground for dissipating transient voltage spikes (such as ESD or surge) on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. The small voltage drop is presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#).

## 7 Device and Documentation Support

### 7.1 Documentation Support

#### 7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide](#) application reports
- Texas Instruments, [Generic ESD Evaluation Module](#) user's guide
- Texas Instruments, [Reading and Understanding an ESD Protection](#) data sheet

### 7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 7.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.6 Glossary

#### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### **Changes from Revision B (March 2025) to Revision C (May 2025)** Page

- |  |                   |
|--|-------------------|
| • Added TSD12, TSD15, TSD18, TSD24, and TSD36 devices..... | <a href="#">1</a> |
|--|-------------------|

### **Changes from Revision A (January 2025) to Revision B (March 2025)** Page

- |                           |                   |
|---------------------------|-------------------|
| • Added TSD03 device..... | <a href="#">1</a> |
|---------------------------|-------------------|

### **Changes from Revision \* (July 2023) to Revision A (January 2025)** Page

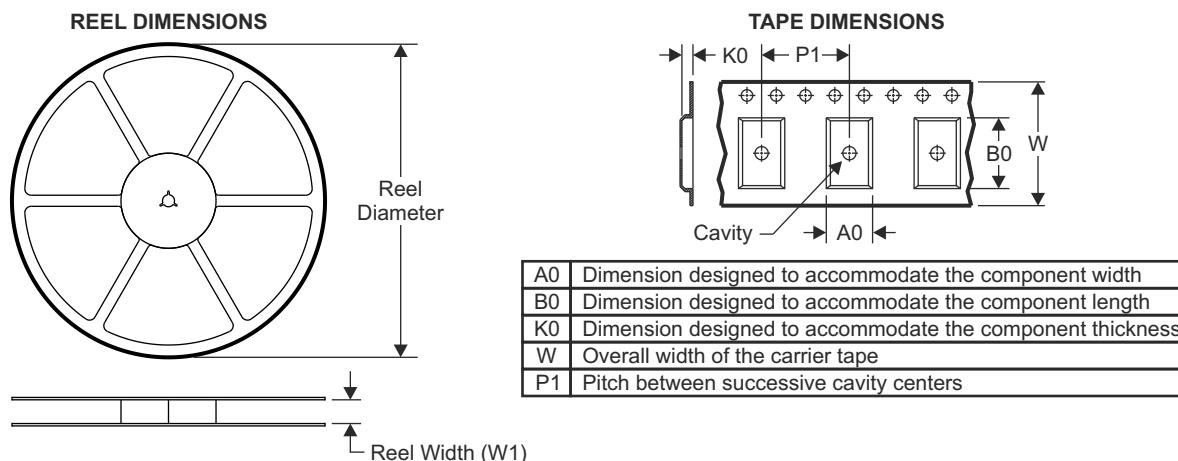
- |   |                   |
|---|-------------------|
| • Updated electrical characteristics..... | <a href="#">6</a> |
|---|-------------------|

DATE	REVISION	NOTES
July 2023	*	Initial Release

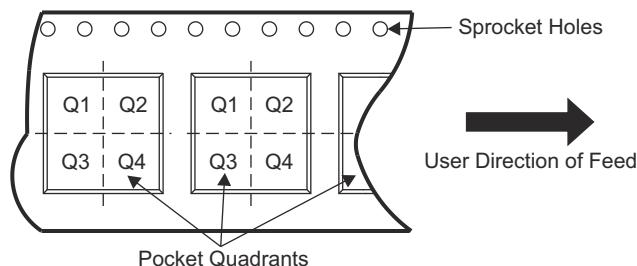
## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 9.1 Tape and Reel Information

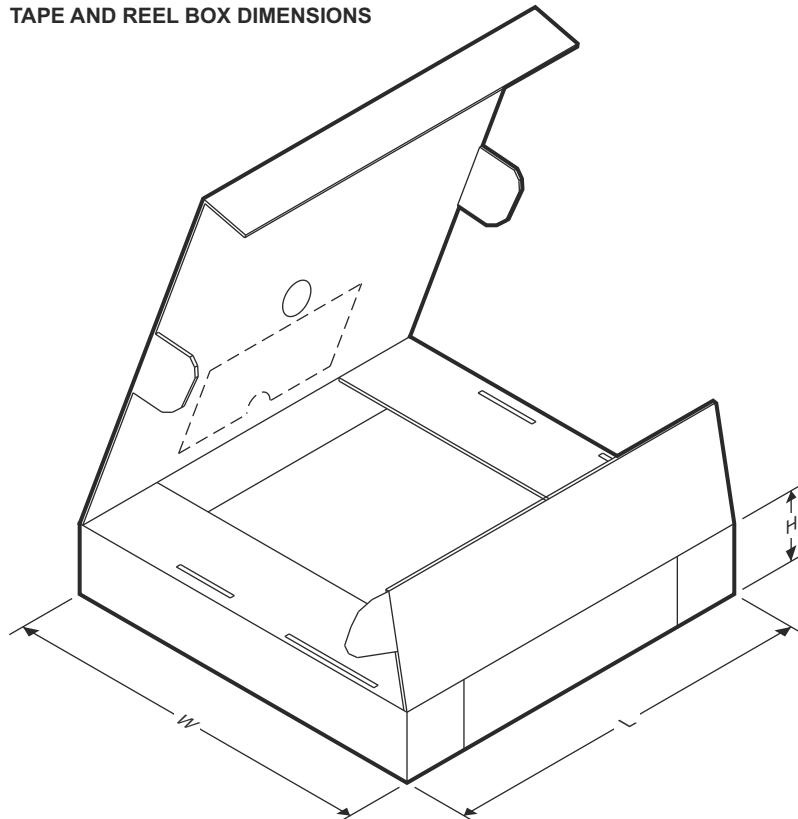


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD05DYFR	SOD-323	DYF	2	15000	178	8.4	0.36	0.66	0.33	0.2	8	Q1

**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD05DYFR	SOD-323	DYF	2	15000	205	200	33

## 9.2 Mechanical Data

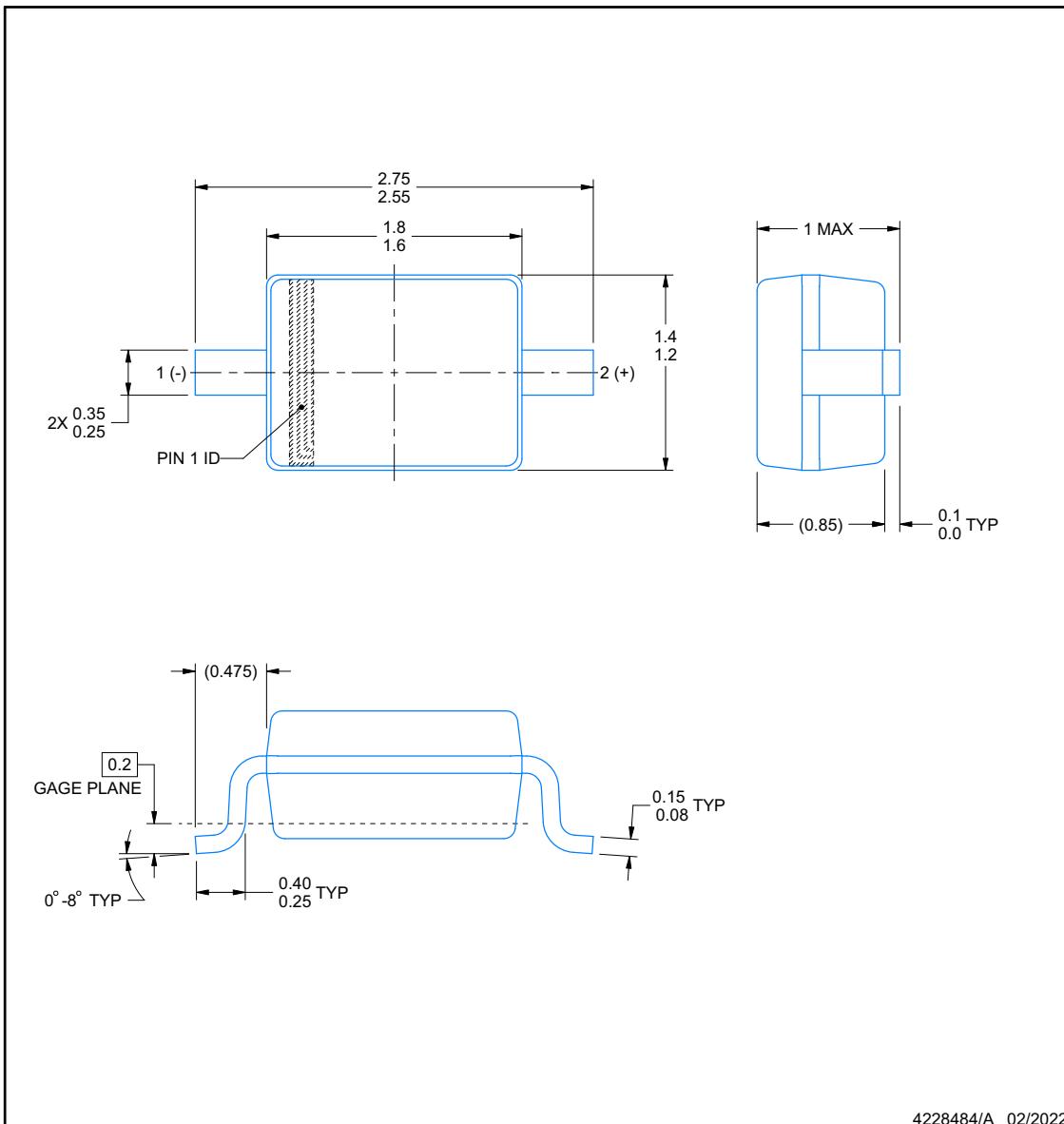
**DYF0002A**



### PACKAGE OUTLINE

**SOT(SOD-323) - 1 mm max height**

SMALL OUTLINE TRANSISTOR



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#### NOTES:

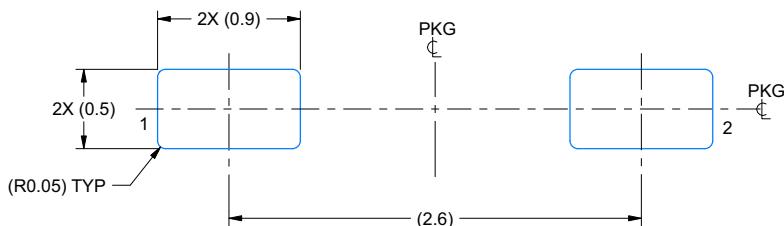
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

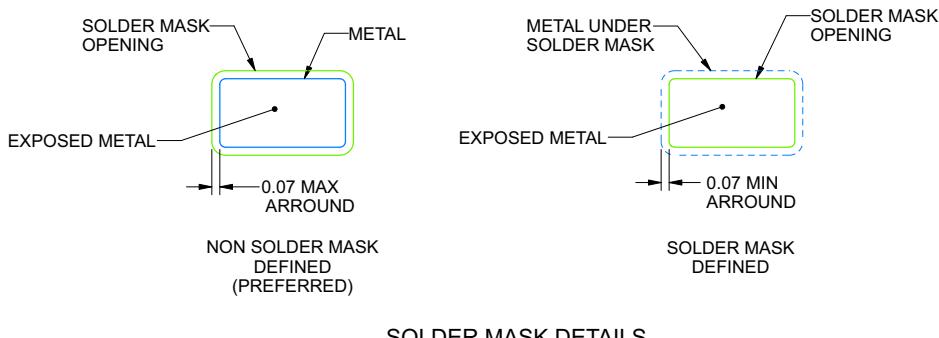
DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



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NOTES: (continued)

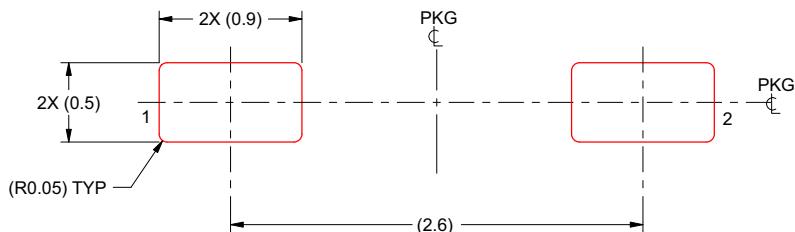
3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSD03DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	3N5F
TSD03DYFR.B	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	3N5F
TSD05DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	33MF
TSD05DYFR.B	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	33MF
TSD12DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3JIF
TSD15DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3MOF
TSD18DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3JLF
TSD24DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3H2F
TSD36DYFR	Active	Production	SOT (DYF)   2	3000   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3GJF

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TSD12, TSD15, TSD18, TSD24, TSD36 :**

- Automotive : [TSD12-Q1](#), [TSD15-Q1](#), [TSD18-Q1](#), [TSD24-Q1](#), [TSD36-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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