Worst-Case Static Noise Margin Criteria for Logic Circuits and Their Mathematical Equivalence

JAN LOHSTROH, MEMBER, IEEE, EVERT SEEVINCK, MEMBER, IEEE, AND JAN DE GROOT

Abstract—**Various criteria have been formulated in the past for analytically calculating the worst-case static noise margins of logic circuits. Some of these criteria are based on infinitely long chains of gates, others on flip-flop circuits. It is shown that the flip-flop approach is equivalent to an infinitely long chain with respect to the worst-case static noise margin. Furthermore, the formal equivalence of four criteria for this worst-case static noise margin is demonstrated. Additionally, a method for computer simulation is discussed.**

I. Introduction

ABOUT 10 years after publication of Hill's paper [1], several papers appeared dealing with static noise margins of logic circuits and methods to determine the worst-case static noise margins [2]–[6].

Involuntarily suggesting a discrepancy between these methods, these papers give different criteria for the worst-case noise margins, such as maximum square between the normal and mirrored transfer characteristic [1], loop gain in a flip-flop is equal to unity [3], [4], Jacobian of the Kirchhoff equations of a flip-flop is equal to zero [5], and the existence of two coinciding roots of a flip-flop equation [6].

No comparison of these methods has been published so far.

In this paper, a comparison will be made and it will be shown theoretically that when these criteria are applied properly, they are all equivalent. Depending on the type of circuit, one of the criteria may be preferable; when an analytical calculation is too cumbersome, quasi-static computer simulations can be done [2], [7], [8].

II. Best-Case and Worst-Case Static Noise Margins; The Transition From an Infinitely Long Chain of Identical Gates to a Flip-Flop

Static noise is dc disturbance that is present in logic gates. This noise can be either series-voltage noise, parallel-current noise, voltage noise at the ground line, voltage noise at the power supply line, or a combination of these [2].

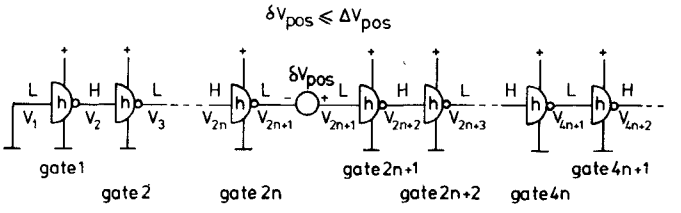

Fig. 1. Setup to determine the best-case static series-voltage noise margin of a logic gate.

The *best-case* (sometimes considered as typical) *static noise margin* for one of the four noise sources is the maximum noise magnitude that does not disturb the proper logic operation when this type of noise is considered to be concentrated somewhere in a point sufficiently far in an infinitely long chain of identical logic gates. Fig. 1 shows such a case for series-voltage noise in an infinitely long chain of inverters. The transfer characteristic is given by

$$V_{\text{out}} = h(V_{\text{in}}) \tag{1}$$

where $h(V_{\text{in}})$ represents the voltage transfer characteristic *including the loading effect of the next gate*. Fig. 2 shows that when the input of the chain is at ground potential, the logic low and high voltages converge to V_L and V_H (see crosspoint A in Fig. 2) when $n \to \infty$; now a positive series-voltage noise source not exceeding $\Delta V_{\text{pos}} = V_{\text{co}} - V_L$ may be applied because in the next series of gates the logic voltages again converge to crosspoint A (V_{co} is the crossover voltage of the transfer characteristics; in earlier literature this is called V_{th}, but this symbol is avoided here to preclude confusion with the threshold voltage of MOS transistors). Similarly, ΔV_{neg} (to be applied between an odd and even gate) equals $V_H - V_{\text{co}}$. In general, $\Delta V_{\text{pos}} \neq \Delta V_{\text{neg}}$; the lower value is in general considered as the best-case noise margin (for series-voltage noise in this case).

Worst-case static noise is defined as dc disturbance which is adversely present in *all* logic gates in an infinitely long chain of gates [1], [2]. Thus, worst-case in this context

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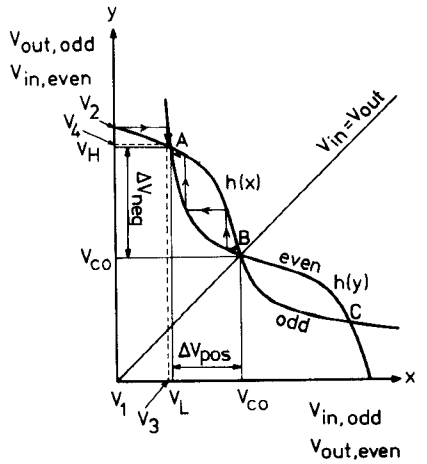

Fig. 2. Voltage transfer characteristics of the gates of Fig. 1.

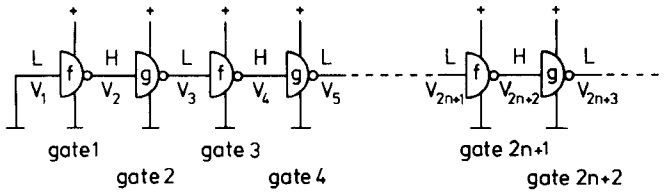

Fig. 3. Setup to determine a worst-case static noise margin of a logic gate. The noise is adversely present in the even and odd gates. The influence of the noise is mathematically incorporated in the transfer characteristics.

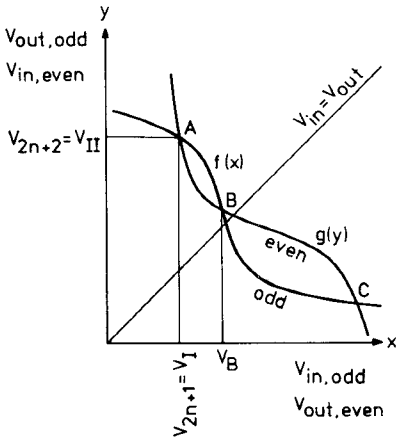

Fig. 4. Transfer characteristics of the gates of Fig. 3 when worst-case noise is applied.

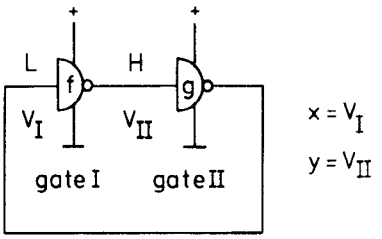

Fig. 5. Flip-flop composed of similar gates as in Fig. 3.

means that, for a given type of noise, the noise is adversely present in *all* gates in exactly the same way; it does *not* mean that it represents the worst *type* of noise as suggested in [5]; for all the four types of noise there exists a worst-case noise margin (ΔV_{series}, $\Delta i_{\text{parallel}}$, ΔV_{gnd}, and ΔV_{supply}) [2].

When the noise sources are mathematically incorporated in the logic gates, then the transfer characteristic for the *odd* gates with adverse noise can be formulated as

$$V_{\text{out}} = f(V_{\text{in}}) \tag{2}$$

and the transfer characteristic for the *even* gates with adverse noise can be formulated as

$$V_{\text{out}} = g(V_{\text{in}}). \tag{3}$$

The functions f and g are different because the noise sources are incorporated into them in different ways in order to have adverse effects in the even and odd gates.

Fig. 3 shows a chain of inverters with worst-case noise. The logic operates properly as long as at the end of the chain (when $n \to \infty$) $V_{2n+z} > V_{2n+1}$ *and* $V_{2n+3} < V_{2n+2}$, which means that V_{2n+2} and V_{2n+4} are logic high levels H, and V_{2n+1} and V_{2n+3} are logic low levels L; see Fig. 3. For this chain we can write

$$V_{2n+1} = g(f(V_{2n-1})), \qquad n = 1,2,\cdots. \tag{4}$$

If $V_I < V_B$ (for V_B see Fig. 4), the sequence (V_{2n+1}) converges if the transfer characteristics f and g intersect at a point A located above the line $V_{\text{in}} = V_{\text{out}}$. Then we have

$$\lim_{n\to\infty} V_{2n+1} = V_I \quad \text{and} \quad \lim_{n\to\infty} V_{2n} = V_{II}. \tag{5}$$

The behavior of V_{2n+1} in the chain for $n \to \infty$ can be considered to be equivalent to that of successive approximations V_k for $k \to \infty$ to a steady state of a flip-flop. This equivalence was also suggested by Mead and Conway [9]. To understand this, consider the flip-flop circuit in Fig. 5, consisting of two successive gates of the chain. Steady states of this flip-flop circuit satisfy the equation

$$V = g(f(V)). \tag{6}$$

The solution of (6) can be computed numerically by Picard iteration [10] as follows:

$$V_{k+1} = g(f(V_k)), \qquad k = 1,2,\cdots. \tag{7}$$

One easily sees that for the characteristics f and g, shown in Fig. 4, the sequence (V_k) converges to $V_I(A)$ or $V_I(C)$ as $k \to \infty$. An analytical criterion for convergence to V_I is known [10] as

$$\left|\frac{\partial f}{\partial x} \cdot \frac{\partial g}{\partial y}\right| < 1, \qquad \text{with } y = f(x) \tag{8}$$

for all values of x sufficiently close to V_I. So, if a state of the flip-flop is approximated by the Picard sequence (7), for large k, V_k is behaving in a similar way as V_{2n+1} in the chain for large n.

The discussion of the behavior of V_{2n} for large n, generated by

$$V_{2n+2} = f(g(V_{2n})), \qquad n = 1,2,\cdots. \tag{9}$$

is fully analogous to the above approach.

So far the situation with $F = \text{fan-in} = \text{fan-out} = 1$ has been discussed. As shown in [2], with the flip-flop method one can easily create situations with $F > 1$.

III. Equivalent Analytical Criteria to Determine the Worst-Case Static Noise Margins

The discussion will be in terms of a flip-flop circuit as depicted in Fig. 5. It was shown in the preceding section that the results are applicable to long chains of gates.

As discussed in Section II, the logic operates properly as long as the cross point A (see Fig. 4) remains above the line $V_{in} = V_{out}$ (then $V_I < V_{II}$). This will be true until the noise is so large that point A (stable point) and point B (metastable point) coincide when marginal noise is applied (see Fig. 6); with a little more noise the transfer characteristics have only one intersection (C) which, moreover, is located below the line $V_{in} = V_{out}$. Then the flip-flop will have switched to the wrong state ($V_I > V_{II}$).

The criteria for the noise margin are now easily derived.

A. Coincidence of Roots of the Flip-Flop Equation

The network equation in terms of any node voltage of a flip-flop will be cubic for binary logic, fifth degree for ternary logic, etc; correspondingly, there will be at most three, five, etc. real roots, respectively.

When we consider the flip-flop of Fig. 5, the equation for x is represented by

$$F(x) \equiv x - g(f(x)) = 0 \tag{10}$$

where $x = V_I$ and $y = f(x) = V_{II}$ and again $x = g(y)$. Two roots coincide when $F(x) = 0$ and $\partial F/\partial x = 0$, so

$$1 - \frac{\partial g}{\partial f} \cdot \frac{\partial f}{\partial x} = 0 \quad \text{and} \quad x = g(f(x))$$

or

$$\frac{\partial f}{\partial x} \cdot \frac{\partial g}{\partial y} = 1. \tag{11}$$

See also Fig. 6.

B. Small-Signal Closed-Loop Gain is Unity

A fundamental result of linear systems theory is that any system is on the verge of instability when the small-signal loop gain is unity. For a flip-flop this means that a particular stable state will become metastable when the small-signal loop gain is unity.

Referring to Fig. 5, this criterion is mathematically expressed as $(\partial f/\partial x)\cdot(\partial g/\partial y) = 1$, which is the same as condition (11).

C. Jacobian of the Kirchhoff Equations is Zero

In the flip-flop of Fig. 5 the following two equations can be found:

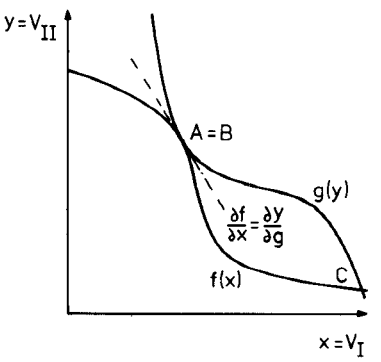

Fig. 6. As Fig. 4, but now with marginal worst-case noise applied.

$$\begin{aligned} F_1 &\equiv x - g(y) = 0 \\ F_2 &\equiv y - f(x) = 0 \end{aligned} \tag{12}$$

The Jacobian of (6) is

$$J = \begin{vmatrix} \frac{\partial F_1}{\partial x} & \frac{\partial F_1}{\partial y} \\ \frac{\partial F_2}{\partial x} & \frac{\partial F_2}{\partial y} \end{vmatrix} = \begin{vmatrix} 1 & -\frac{\partial g}{\partial y} \\ -\frac{\partial f}{\partial x} & 1 \end{vmatrix} = 1 - \frac{\partial f}{\partial x} \cdot \frac{\partial g}{\partial y}.$$

When equated to 0 we get again

$$\frac{\partial f}{\partial x} \cdot \frac{\partial g}{\partial y} = 1$$

which is identical to (11).

D. Maximum Square Between Normal and Mirrored Voltage Transfer Characteristic (for Series-Voltage Noise Only and When $R_{out} \ll R_{in}$)

Only when $R_{out} \ll R_{in}$, the shape of the voltage transfer characteristic is invariant with respect to the loading, and then the worst-case series voltage noise margin can be found geometrically by considering the maximum possible square between the normal and mirrored transfer characteristic [see Fig. 7(a)].

The square has a maximum size when the length of its diagonal is maximum. In the (u, v) coordinates [45° rotated with respect to (x, y); see Fig. 7(a)] the normal and mirrored characteristics are described by the functions $u = f_1(v)$ and $u = f_2(v)$. The length of the diagonal (which is in the u-direction) is found by $D \equiv f_2(v) - f_1(v)$, and has its maximum when $\partial D/\partial v = 0$. This occurs when

$$\frac{\partial f_1(v)}{\partial v} = \frac{\partial f_2(v)}{\partial v}. \tag{13}$$

In fact, (13) indicates that the tangents at the points P and Q, where the maximum square touches the characteristics, are parallel (although not necessarily parallel to the v axis); the sides of the square are defined as ΔV_{series}. When now marginal worst-case series voltage noise is applied, by assuming equal but opposite noise voltages in series with two subsequent gates, the transfer characteristics change

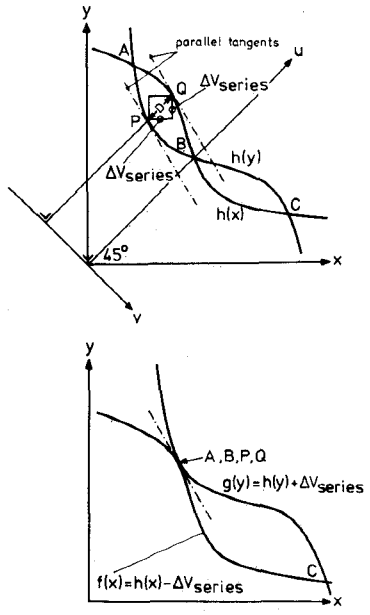

Fig. 7. (a) Maximum square method to determine the worst-case static series-voltage noise margin (only valid when $R_{out} \ll R_{in}$). (b) When this static series-voltage noise is applied, the voltage transfer characteristics are just touching.

into $f(x) = h(x) - \Delta V_{series}$ and $g(y) = h(y) + \Delta V_{series}$. Hence, the points P and Q coincide [see Fig. 7(b)], yielding the same situation as in Fig. 6 and again

$$\frac{\partial f}{\partial g} \cdot \frac{\partial g}{\partial y} = 1.$$

This criterion is again identical to (11).

When in the opposite case $R_{out} \gg R_{in}$, this method can be used to find the worst-case parallel current noise margin by using the current transfer characteristics [2], [11].

IV. Computer Simulations

When, due to the complexity of the analytical description of the logic gates, the analytical methods are cumbersome, intractable, or they yield results that are difficult to interpret, computer simulations can be carried out when accurate models of the gates are available.

The best way is to carry out quasi-static transient simulations by starting with all noise sources being zero and by increasing the amplitudes of the noise sources slowly compared to the switching speed of the flip-flop. The worst-case noise margin is then found as the noise amplitude(s) at which the flip-flop switches to the wrong state.

This method has been used successfully to determine the noise margins of I^2L, SI^2L, ISL, and STL [7], [8].

V. Discussion and Conclusions

The worst-case static noise margins of infinite chains of gates can be determined by studying the considerably simpler equivalent network represented by a flip-flop.

The equivalence between the following criteria which can be used to calculate analytically the worst-case static noise margins of logic circuits has been formally demonstrated:

1) coincidence of roots of the flip-flop equations;

2) the small-signal closed-loop gain of the flip-flop is unity;

3) the Jacobian of the Kirchhoff equations of the flip-flop is zero;

4) maximum square between normal and mirrored voltage or current transfer characteristics.

The latter method is only valid when $R_{out} \ll R_{in}$ or $R_{out} \gg R_{in}$ and can be used to determine the worst-case series voltage noise margin or the worst-case parallel current noise margin, respectively.

In practice, the criteria 2) and 3) are the most handy ones, although criterion 2) requires a careful examination of all the current and voltage loops [3], [5]. In fact, criterion 3) delivers the most straightforward approach with the smallest chance of making mistakes [5], [8].

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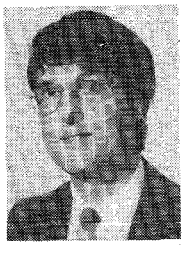

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A High Performance 256K (512K) Static ROM

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Abstract—**A 256K ROM, fully expandable to 512K, has been fabricated. The ROM utilizes a 2.5 μm NMOS multiple threshold technology. It has a typical access time of 120 ns and uses push–pull circuitry to achieve an active current of 60 mA and a standby current of 1.0 mA. Total chip size is 39K mil^2 for the 256K version. A modified X cell has been chosen which requires 7.5 μm $\times$7.5 μm. Current sensing was chosen to optimize access time.**

Introduction

The performance of MOS ROM's has increased extensively in the past five years, from 16K densities ten years ago to a 4 Mbit version for character generation reported in 1980 [1]. Access times have ranges from 45 ns to several hundred nanoseconds, depending on the density and application. Although EPROM's and EEPROM's have made significant advancements in the past few years, ROM's will remain dominant where the requirements of high volume, high density, high reliability, and low cost are of primary concern. The ROM described in this paper is a general-purpose ROM, and thus compromises were made to optimize overall performance. The 256K (32K$\times$8) ROM is fully expandable to 512K with minimum changes. It has a 60 mA typical active power with a 1.0 mA standby. The low standby power is attributed to the extensive use of push–pull circuitry and a novel back bias generator. Because of its low standby power, it is feasible for battery-operated equipment. The ROM is fully static and is programmed via an ion implantation which increases the threshold voltage of selected cells in the memory array. This technique is more economical than the traditional diffusion technique which must occur early in the processing sequence and thus extend lead time.

The architecture of the chip is shown in Fig. 1, with the die photo of the 256K version shown in Fig. 2(a). It is organized in eight 512$\times$64 groups for the 256K version and eight 1024$\times$64 groups for the 512K version. Through the use of predecoding, there are 128 NOR X-decoders (256 for the 512K), one for every four rows of cells. The cell chosen is a modified X cell [2] configuration requiring only 7.5 μm$\times$7.5 μm. To optimize access time, current sensing was incorporated as described by Wong *et al.* [3].

Process Technology

The ROM is fabricated on a basic 2.5 μm gate length, 500 Å NMOS polysilicon technology. Although CMOS would require less power, it was considered too costly, and the loss in density would not meet the requirements mentioned previously. Five thresholds are available, which include a hard depletion (−2.5 V), a soft depletion (−0.7), a soft enhancement (0.0 V), a hard enhancement (0.7 V), and a high threshold (+7.0) for programming. A polysilicon-to-diffusion contact is also available.

Address Buffer

The address buffers consist of three inverter stages driving a push–pull output stage. The requirements of low power, minimum propagation delay, and in specific cases, high V_{out} are important. Probably the most critical stage is the first inverter in that it must be TTL compatible, even with variations in supply and process. To ensure TTL compatibility, the device dimensions of the first stage were designed conservatively.

The difference in this buffer is in the output stage. To conserve active power, soft enhancement devices were used as the output pull-ups. Unfortunately, this limits the maximum output level. If only soft enhancements were used, the maximum voltage for a HIGH level would be $2V_{TSE}$

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