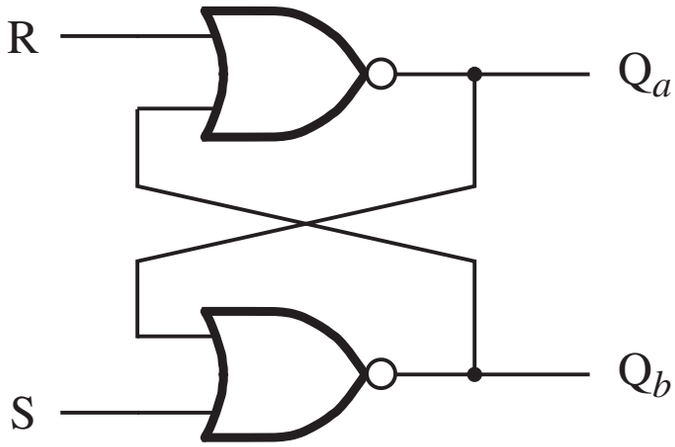
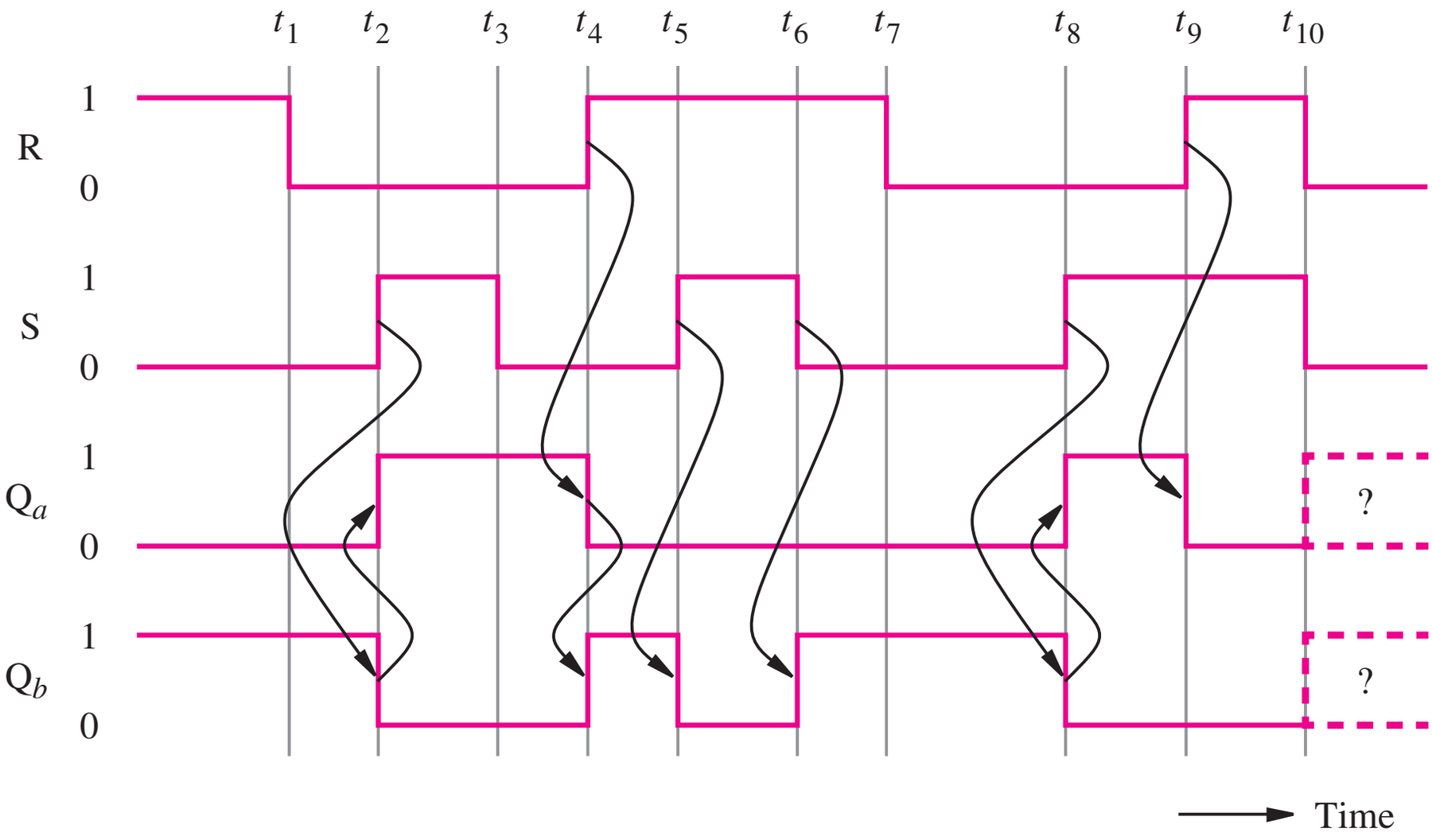



(a) Circuit

| S | R | $Q_a$ | $Q_b$ | |
|---|---|---|---|---|
| 0 | 0 | 0/1 | 1/0 | (No change) |
| 0 | 1 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | |

(b) Truth table




(c) Timing diagram

**Figure 7.5** A basic latch built with NOR gates.