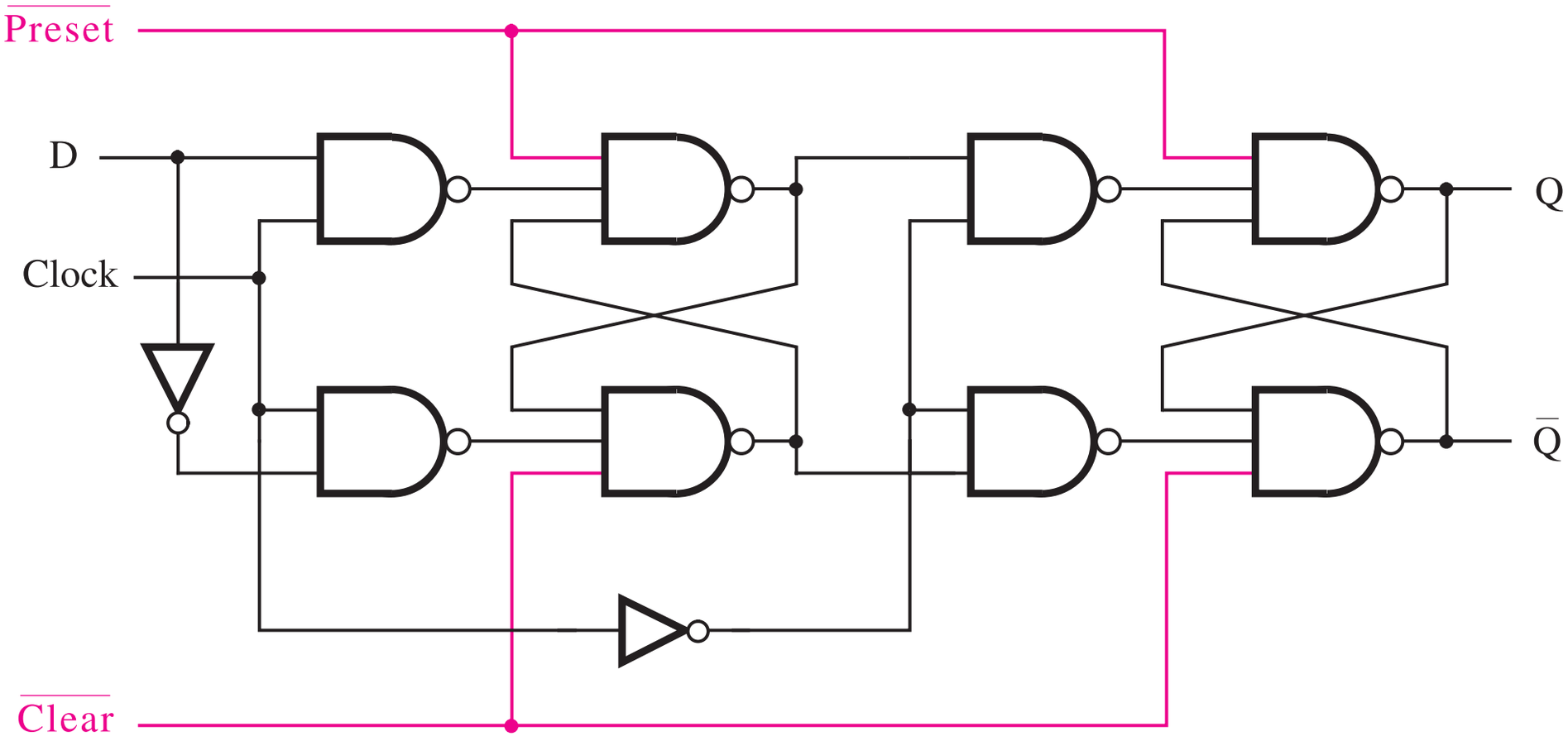
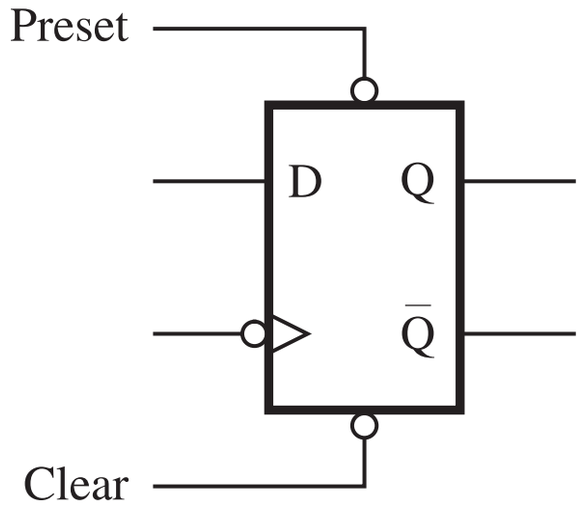


(a) Circuit



(b) Graphical symbol

Figure 7.13 Master-slave D flip-flop with *Clear* and *Preset*.