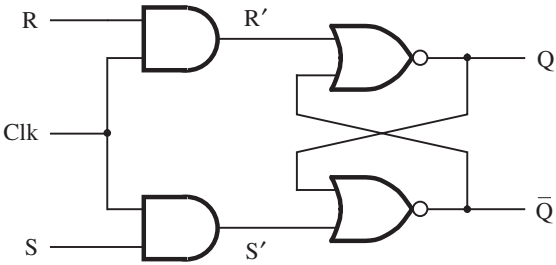
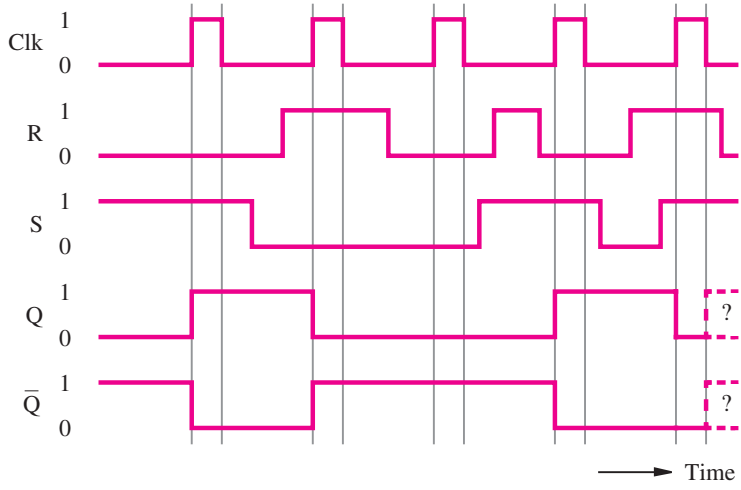


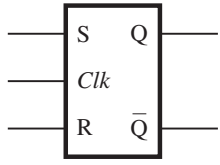
(a) Circuit

Clk	S	R	Q(*t* + 1)
0	x	x	Q(*t*) (No change)
1	0	0	Q(*t*) (No change)
1	0	1	0
1	1	0	1
1	1	1	x

(b) Truth table



(c) Timing diagram



(d) Graphical symbol

Figure 7.6 Gated SR latch.