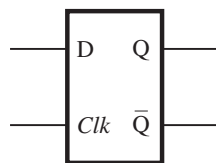


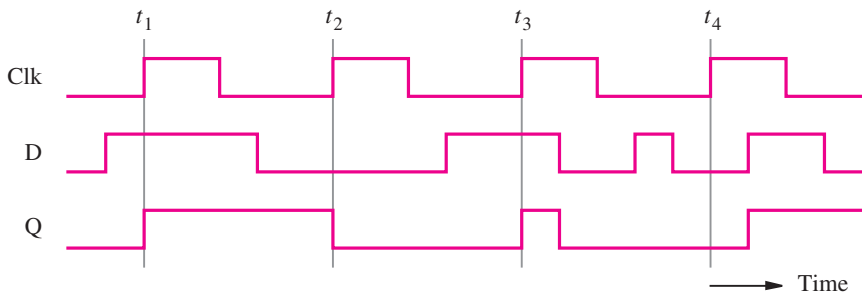
(a) Circuit

Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbol



(d) Timing diagram

**Figure 7.8** Gated D latch.