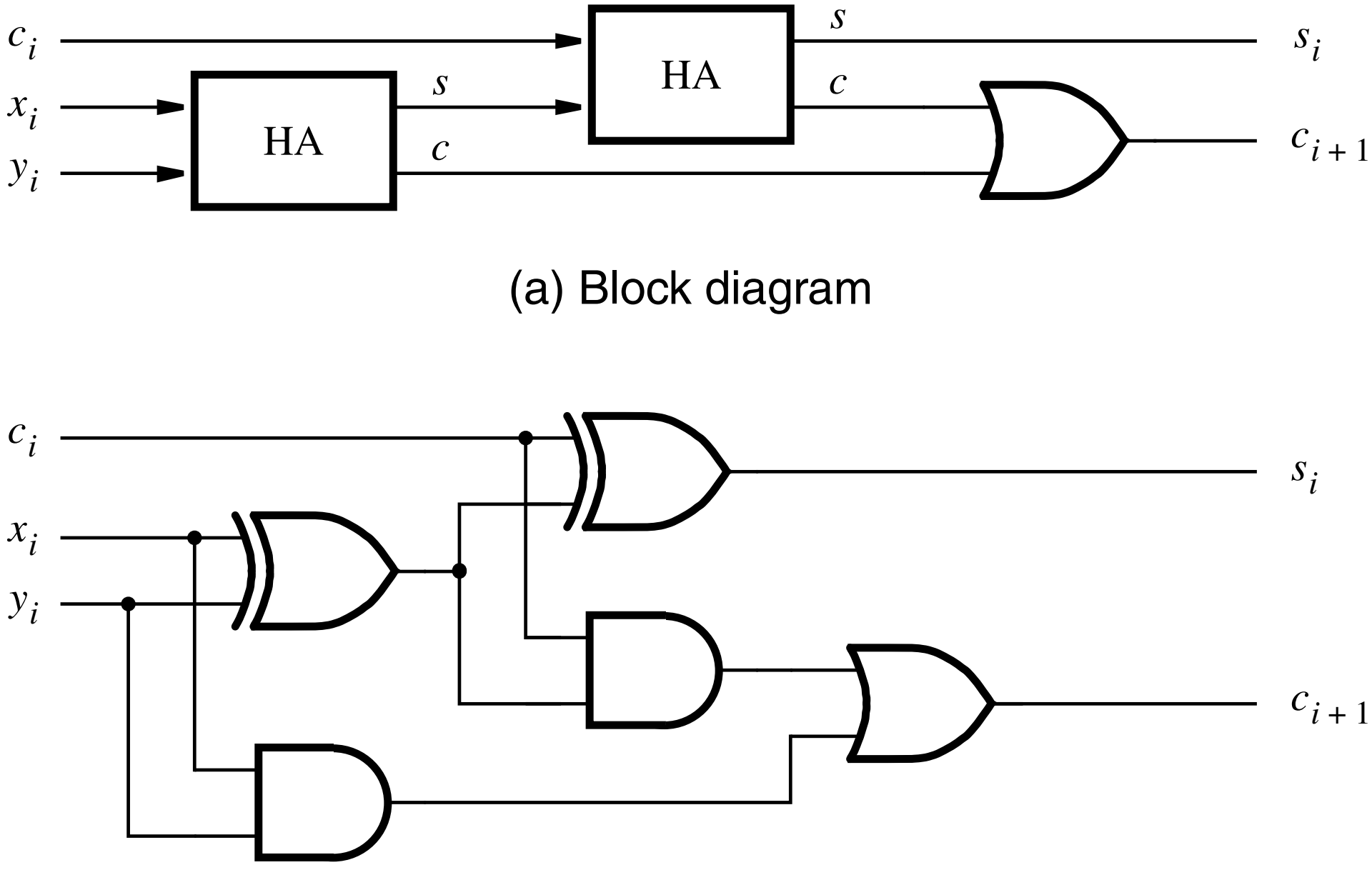

Figure 3.4 A decomposed implementation of the full-adder circuit.