Ensimag 3A - filière SLE

Liquid Crystal Display Controller (LCDC) Documentation

The LCDC is an *Advanced Microcontroller Bus Architecture* (AMBA) master-slave module which connects to the *Advanced High-performance Bus* (AHB). The LCDC is an AMBA-compliant *System-on-a-Chip* (SoC) peripheral developed, tested and licensed by the SLE department of Grenoble INP Ensimag.

Features

The LCDC provides all the necessary control signals to interface directly with a variety of monochrome LCD panels. The controller supports the following video parameters :

- 320 x 240 pixels resolution
- 8 bits depth (256 grayscales)

Inputs/Outputs

The LCDC provides the following inputs/outputs :

- AMBA compliant slave interface for configuration
- AMBA compliant master interface
- Display interrupt signal (`display_int`)
- LCD interface signals (pixel clock, control signals)

Figure 2 shows a simplified block diagram of the LCDC.

Operations

After reset, the LCDC is initially idle. Beginning of operation is triggered by writing into the `START_REG` register. The LCDC then performs read accesses to an external AMBA memory device holding the video buffer via its master interface. Adresses start at the value stored in the `ADDR_REG` register and increment until reaching the end of the buffer. Video data are supposed to be stored contiguously in memory, in big endian format (see figure 1). After reading the video buffer and sending appropriate signals on its LCD outputs, the controller asserts its `display_int` interrupt signal. The signal is supposed to be deasserted before next refresh (see `INT_REG` register reference).

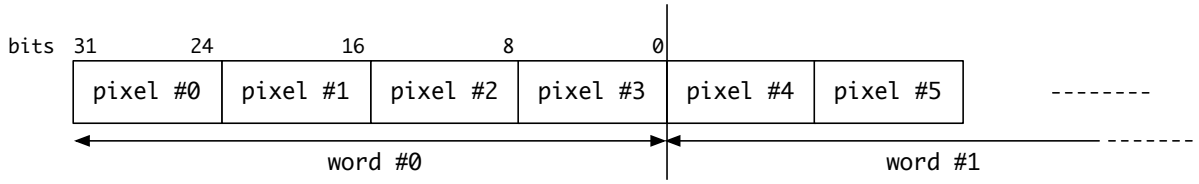

FIGURE 1 – Video data as expected in memory

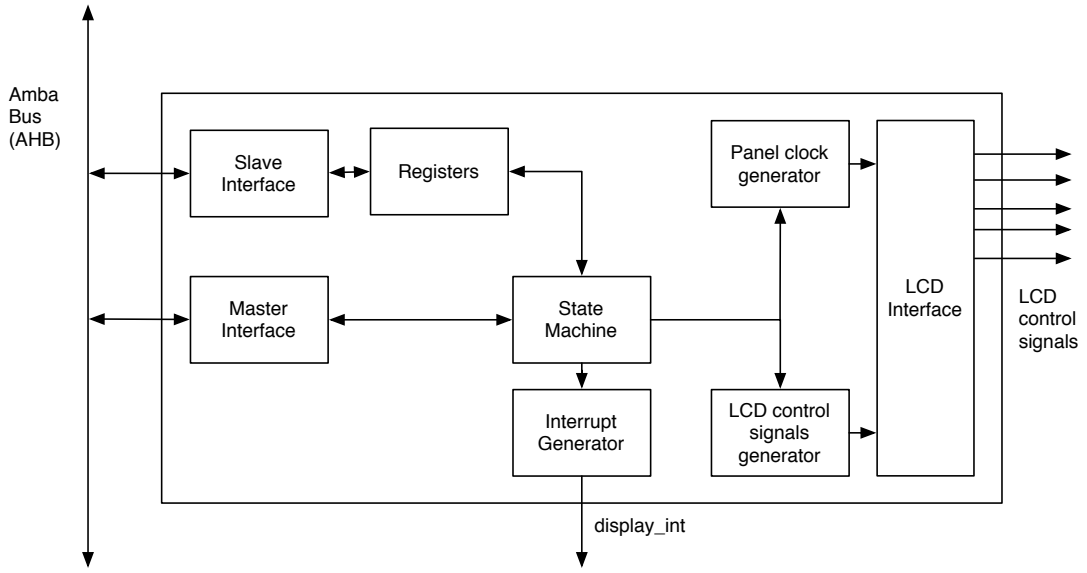

FIGURE 2 – Simplified block diagram of the LCDC

Registers Summary

Address offset	Type	Width	Reset value	Name	Description
0x00	Read/Write	32	0x00000000	ADDR_REG	Start address register
0x04	Write only	32	N/A	START_REG	Start register
0x08	Read/Write	32	0x00000000	INT_REG	Interrupt register

Registers Reference

Start address register (ADDR_REG)

The start address register holds the base address of the video memory buffer as accessed on the AMBA master interface. The value should not be modified while the controller is operating.

Start register (START_REG)

The start register is used to trigger the beginning of controller operation. Writing 0x00000001 into the register starts the LCDC.

Interrupt register (INT_REG)

The interrupt register stores a value depending on the display_int interrupt signal. After display_int is asserted, the register's value is 0x00000001. Writing 0x00000000 into the register deasserts the interrupt, which is required after each assertion for proper operation of the controller.