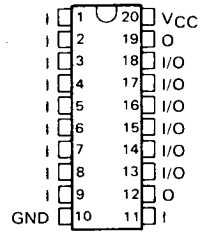
D2972, MARCH 1987—REVISED DECEMBER 1987

- **Mask-Programmed Version of 20-Pin PAL® Family**
- **Virtually Zero Standby Power**
- **35-ns Maximum Propagation Delay**
- **HC, HCT, and TTL Compatible**
- **Choice of 20-Pin DIP, 20-Pin SO (Small Outline) or 20-Pin PLCC Packages**
- **Low-Power Replacement for 20-Pin 'A' PAL® Devices**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	INPUTS	3-STATE Q OUTPUTS	REGISTERED OUTPUTS	I/O PORTS
'HAL16L8	10	2	0	6
'HAL16R4	8	0	4 (3-state)	4
'HAL16R6	8	0	6 (3-state)	2
'HAL16R8	8	0	8 (3-state)	0

TICHAL16L8
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



TICHAL16L8
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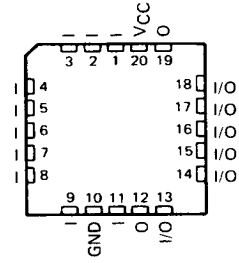

description

These high-speed CMOS Hard Array Logic (HAL®) circuits are mask-programmed versions of the 20-pin PAL® devices. They provide reliable, high-speed, low-power substitutes for conventional TTL and HCT logic. They are also compatible with HC logic over V_{CC} range of 4.5 volts to 5.5 volts.

This family of CMOS HAL® circuits provide the flexibility of using integrated circuits with virtually zero standby power and lower operating power than those currently achieved by bipolar PALs. Prototyping can be done using standard PAL® devices before converting to CMOS HAL® circuits for production.

The TICHAL16' circuits have internal electrostatic discharge (ESD) protection circuits and have been classified with a 2000-volt ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

The C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 75°C.

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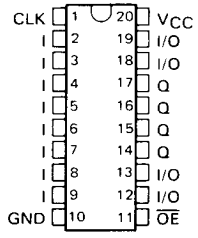
TICHAL16R4
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



TICHAL16R4
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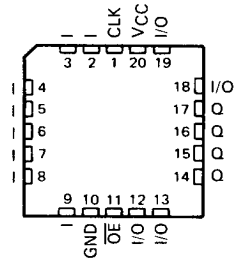
(TOP VIEW)



TICHAL16R6
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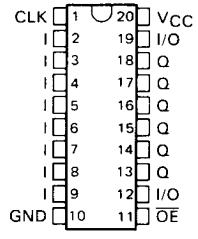
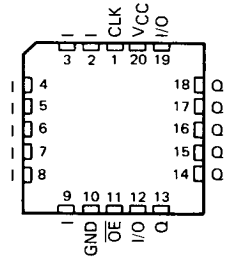
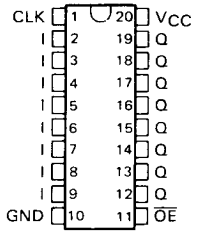
(TOP VIEW)



TICHAL16R6
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TICHAL16R8
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



TICHAL16R8
C SUFFIX . . . FN PACKAGE
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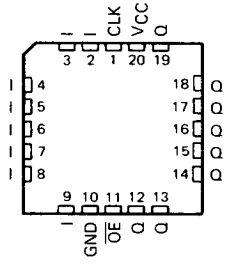

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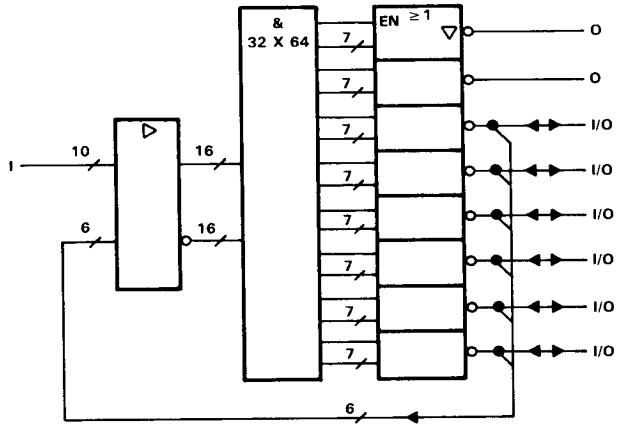
functional block diagrams (positive logic)

TICHAL16L8



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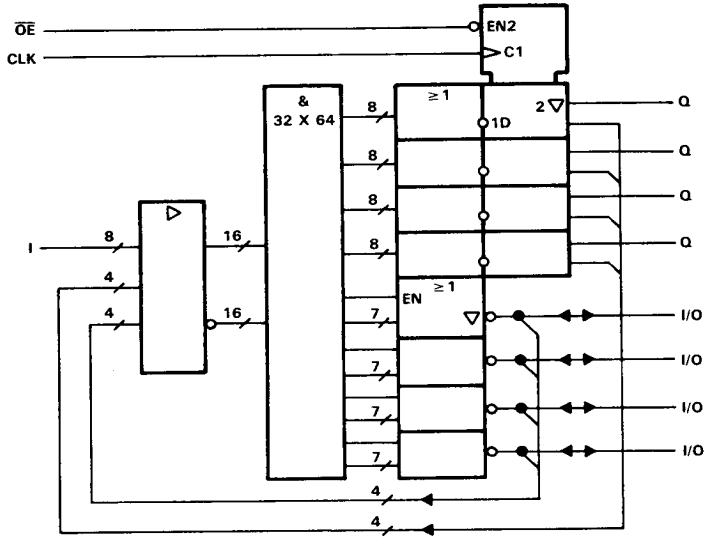
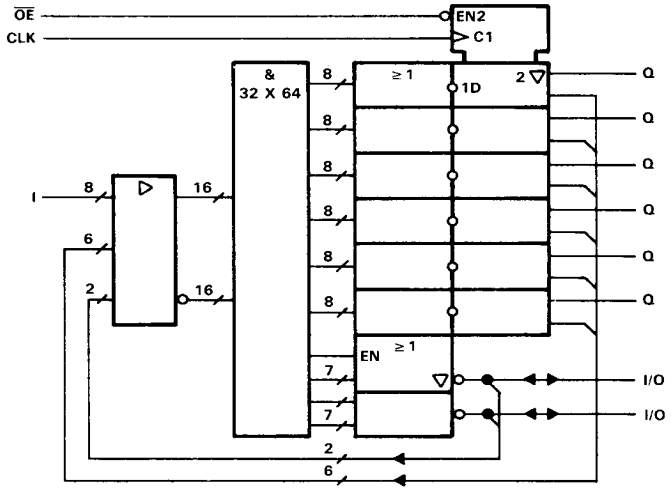


functional block diagrams (positive logic)

TICHAL16R6



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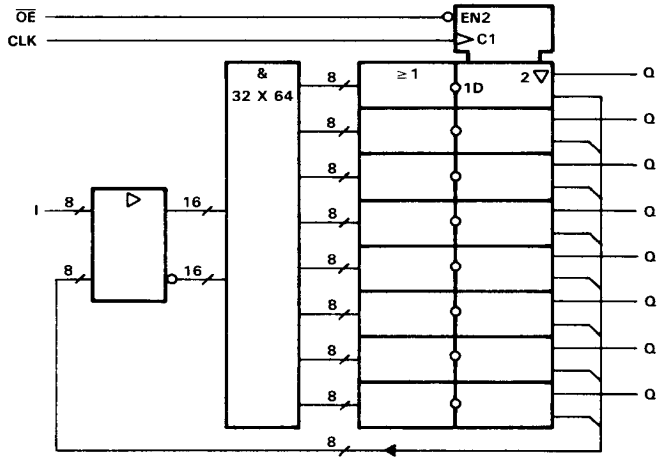

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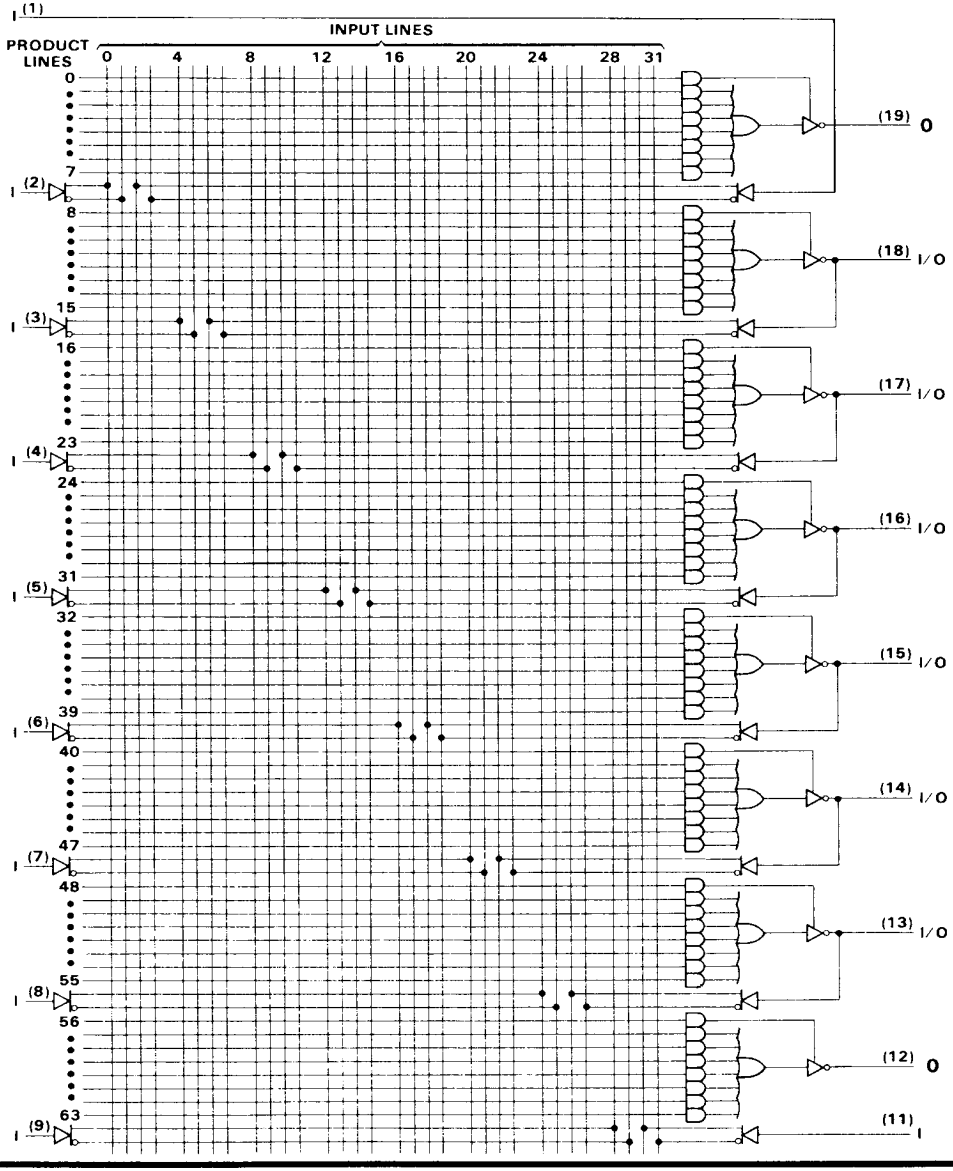
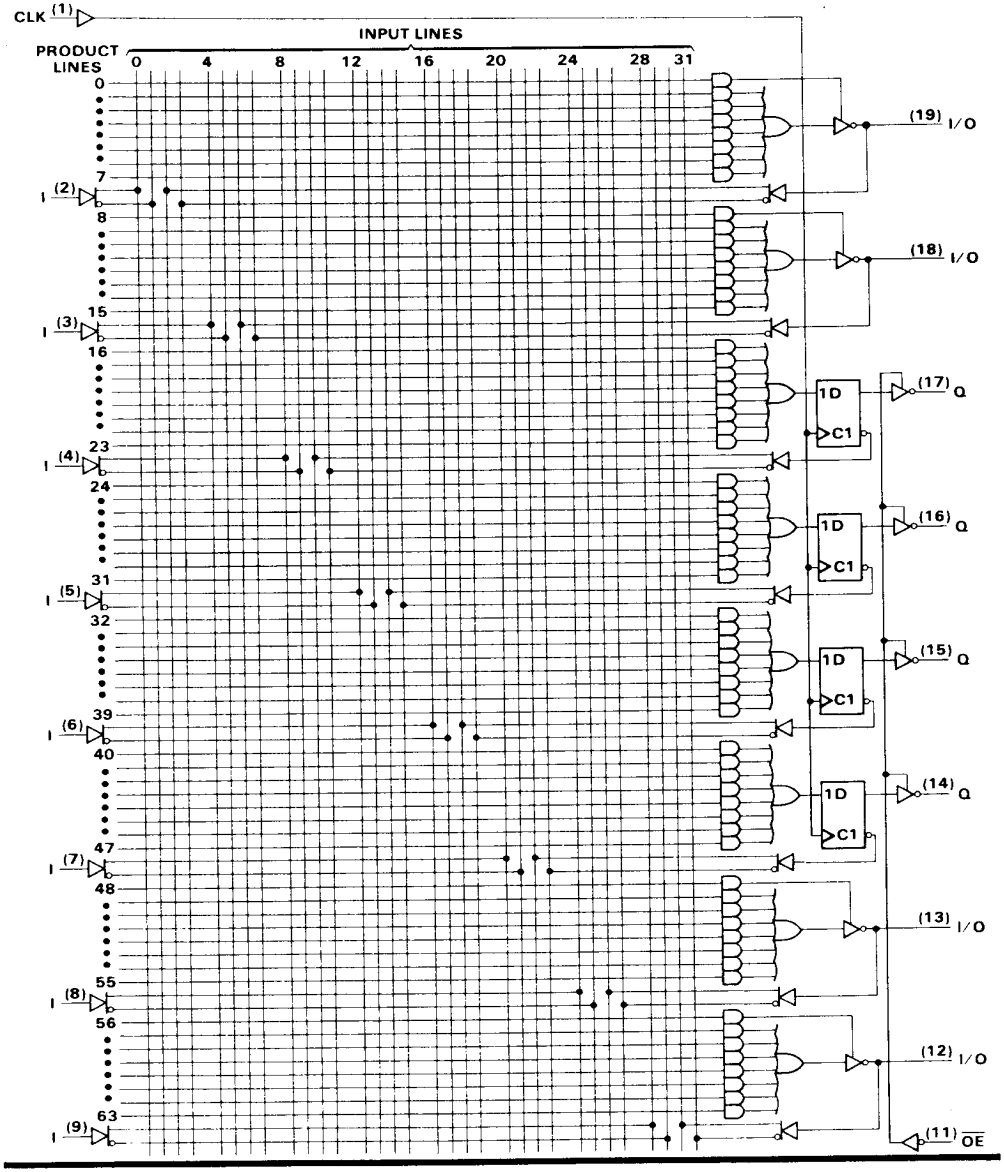
logic diagram (positive logic)



logic diagram (positive logic)



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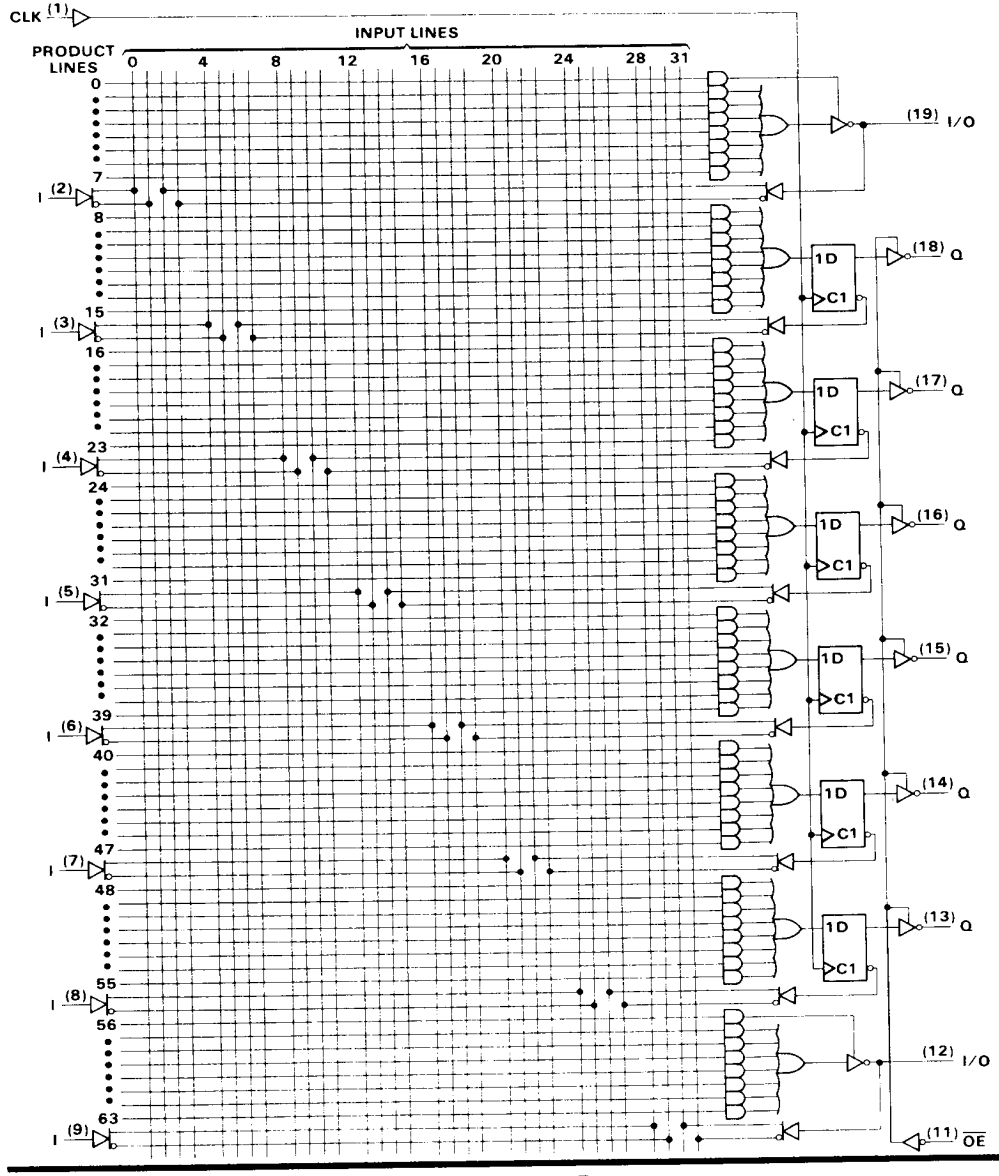

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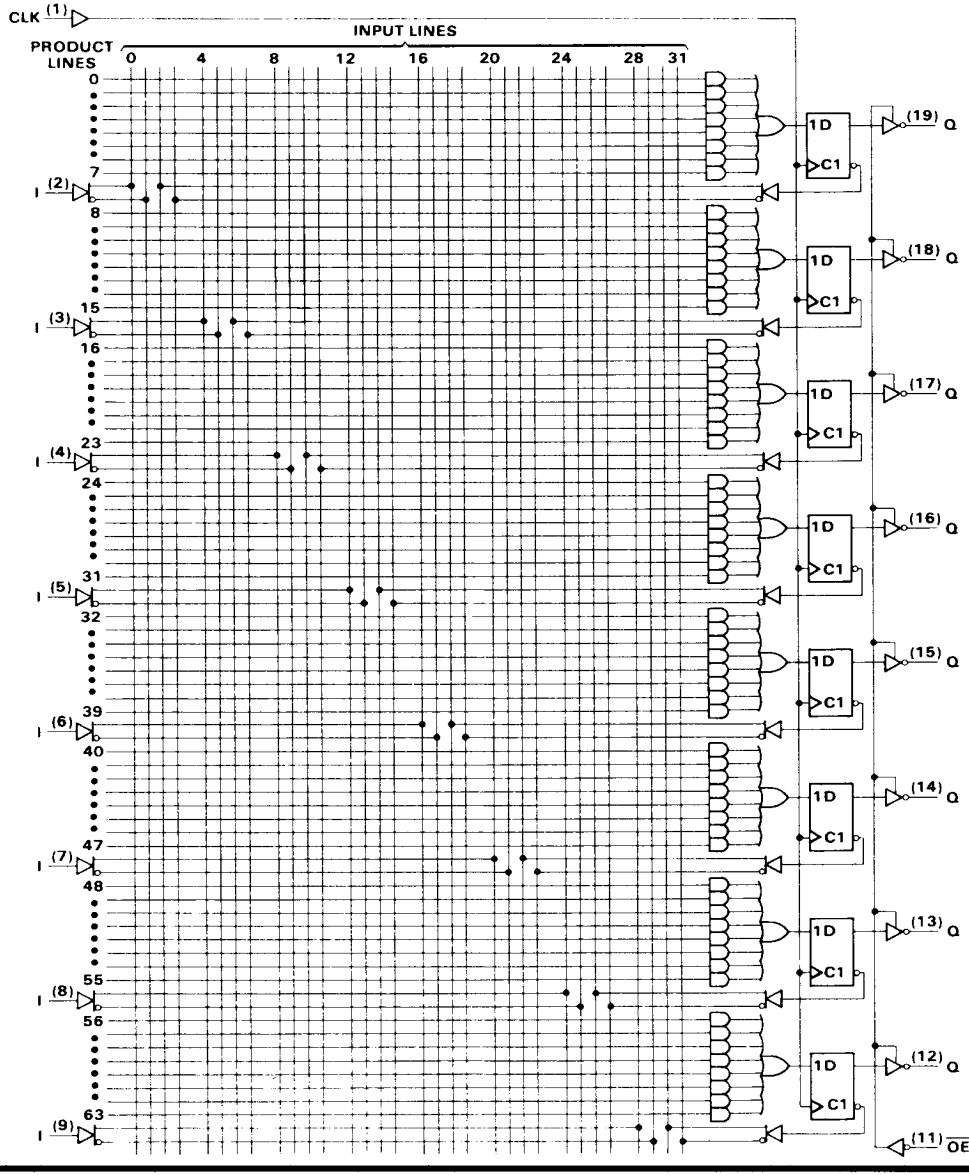

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} pin . . . . . 70 mA
Continuous current through GND pin . . . . . −200 mA
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			C-SUFFIX			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
t_w	Pulse duration	Clock high	20			ns
		Clock low	20			
t_{su}	Setup time, input or feedback before CLK↑		30			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature range		0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		C-SUFFIX MIN	C-SUFFIX TYP†	C-SUFFIX MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −6 mA	3.76			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.4	V
I_{OZH}	Off-state output current with high-level voltage applied	V_{CC} = 5.5 V,	V_O = V_{CC}			10	μA
I_{OZL}	Off-state output current with low-level voltage applied	V_{CC} = 5.5 V,	V_O = 0			−10	μA
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = V_{CC}			1	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0			−1	μA
I_{CC}	Standby supply current	V_{CC} = 5.5 V, I_O = 0	V_I = 0 or V_{CC},			100	μA
I_{CC}	Operating supply current	V_{CC} = 5.5 V, f ≥ 1 MHz,	V_I = 0 or V_{CC}, I_O = 0		2		mA/MHz
ΔI_{CC}‡	Change in supply current	V_{CC} = 5.5 V, Other inputs at 0 or V_{CC}	V_I = 0.5 V or 2.4 V,		1.4	3	mA
C_i	Input capacitance	T_A = 25°C,	f = 1 MHz			10	pF
C_o	Output capacitance	T_A = 25°C,	f = 1 MHz			10	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	C-SUFFIX MIN	C-SUFFIX TYP†	C-SUFFIX MAX	UNIT
f_{max}§		with feedback	R_1 = 200 Ω, R_2 = 390 Ω, C_L = 50 pF	18			MHz
		without feedback		25			
t_{pd}	I, I/O, or feedback	O or I/O			18	35	ns
t_{pd}	CLK↑	Q			10	25	ns
t_{en}	$\overline{OE}$↓	Q			12	25	ns
t_{dis}	$\overline{OE}$↑	Q			12	25	ns
t_{en}	I or I/O	O or I/O			14	35	ns
t_{dis}	I or I/O	O or I/O			16	35	ns

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 or V_{CC}.

§ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$; f_{max} (without feedback) = $\frac{1}{t_w\text{(high)} + t_w\text{(low)}}$

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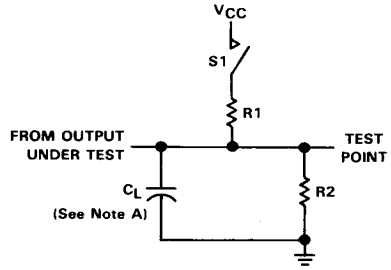
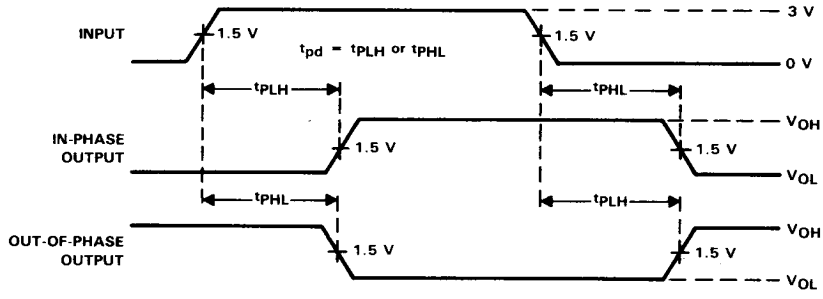
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L = includes probe and jig capacitance.
B. When measuring propagation times of 3-state outputs, S1 is closed.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS

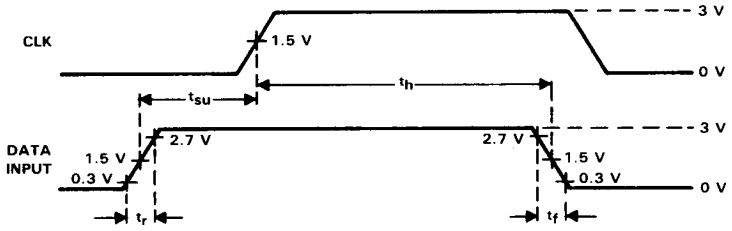


VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns.

FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

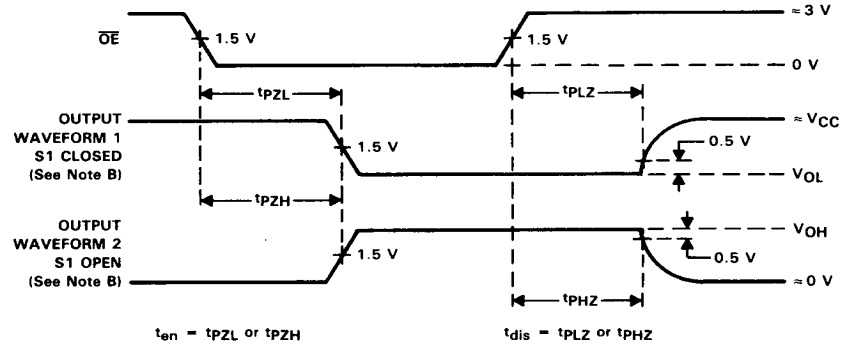
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE: Phase relationship between waveforms was chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = t_r = 6 ns, t_f = 6 ns.

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

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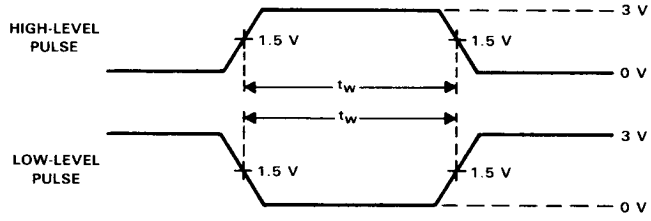
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 6 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%.

FIGURE 5. PULSE DURATIONS