1. Requirements and Installation

2. Usage

Design Template
Configuration file
Factorial configurations

Run: python XilinxSynt.py configuration.xml
For instance:

```
ILYA@ILYA-PC /cygdrive/c/Release/FactorialDesign/Python
$ python XilinxSynt.py ./Configs/config_MC8051.xml
```

Wait for completion, for monitoring refer to monitoring module.

Main Results (implementation properties):

summary_power_estimated (.csv/.xml)
summary_power_simulated (.csv/.xml)
config_pattern.xml – for later use by SBFI tools

Per-configuration results

./design_dir/design_label_[Index]/netgen/
./Log/
./par/
./map/…
./synthesis/…

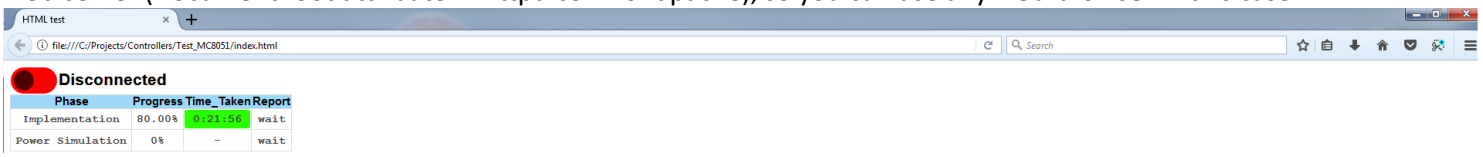
User Interface: monitoring module

Connected, Last Update (13:06:38): 0.162 Kb

Phase	Progress	Time_Taken	Report
Implementation	40.00%	0:19:11	wait
Power Simulation	0%	-	wait

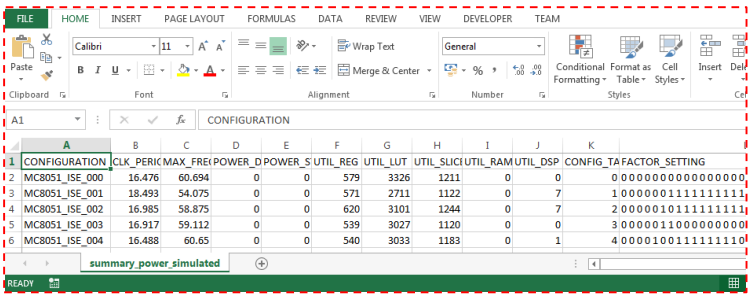
Label	FREQ	POWER_DYN	SLICE	REG	LUT	DSP	RAMB	Progress	Iteration	Clock	Converged	Synthesis	Translate	Map	PlaceRoute	TimingAnalysis	NetlistBuilder	Fuse_Compile	Simulation_ISIM	PowerAnalysis
MC8051_ISE_000	-	-	-	-	-	-	-	PlaceRoute	5	16.5	Yes	100%: 0:00:02	100%: 0:00:05	100%: 0:01:10	In progress	100%: 0:00:22	-	-	-	-
MC8051_ISE_001	54.08	69.64	1122	571	2711	7	0	Completed: 2017-10-19 12:56:53	1	18.5	Yes	100%: 0:00:01	100%: 0:00:05	100%: 0:01:17	100%: 0:01:14	100%: 0:00:23	100%: 0:00:30	-	-	100%: 0:00:16
MC8051_ISE_002	-	-	-	-	-	-	-	Power Analysis	4	17.0	Yes	100%: 0:00:01	100%: 0:00:05	100%: 0:01:21	100%: 0:01:17	100%: 0:00:22	100%: 0:00:29	-	-	Inprogress
MC8051_ISE_003	59.11	77.92	1120	539	3027	0	0	Completed: 2017-10-19 13:04:52	4	17.0	Yes	100%: 0:00:01	100%: 0:00:05	100%: 0:01:12	100%: 0:01:13	100%: 0:00:22	100%: 0:00:27	-	-	100%: 0:00:16
MC8051_ISE_004	-	-	-	-	-	-	-	MAP	3	17.0	No	100%: 0:00:01	100%: 0:00:06	In progress	100%: 0:01:15	100%: 0:00:21	-	-	-	-
MC8051_ISE_Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

If the connection status is ‘Disconnected’ – click the switchbox, once connected it will be highlighted in green. If the connection status is ‘Connection error’ – check that you are using Firefox browser; otherwise make this folder accessible for web-server (DocumentRoot attribute in httpd.conf for apache), so you can use any web-browser in this case.



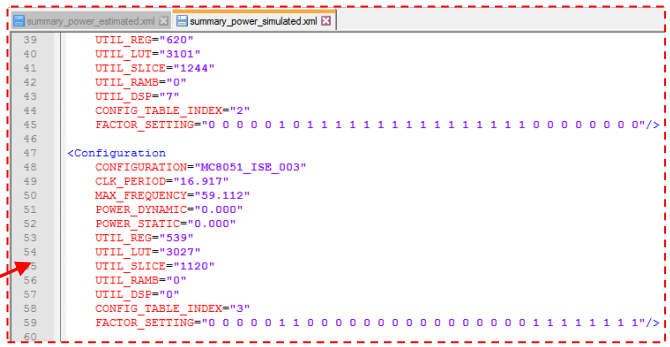
Phase	Progress	Time_Taken	Report
Implementation	80.00%	0:21:56	wait
Power Simulation	0%	-	wait

*Result in *.csv format*



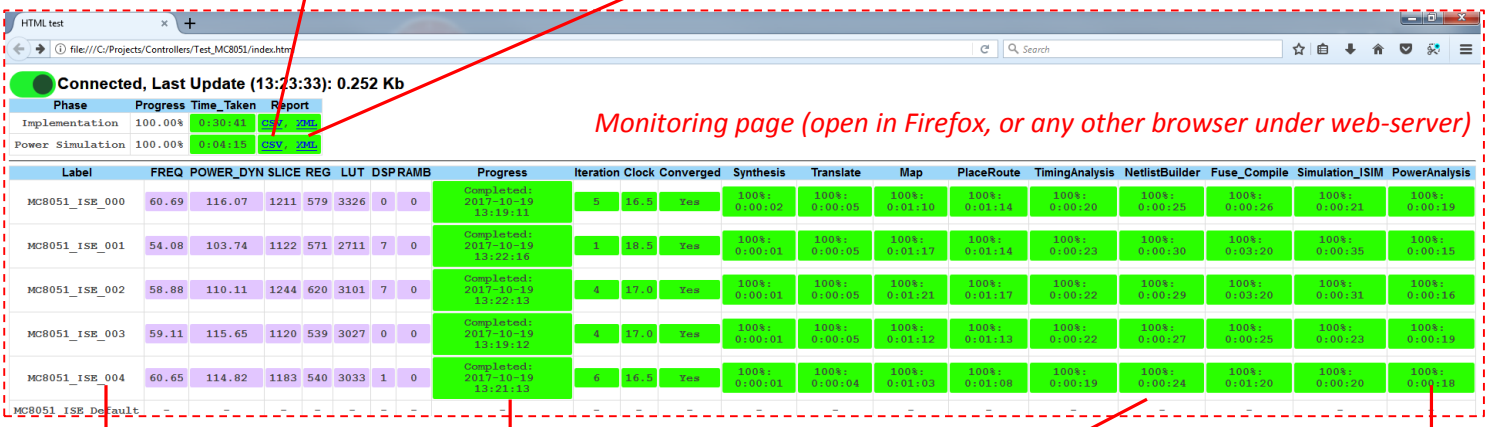
CONFIGURATION	CLK_PERIO	MAX_FRE	POWER_D	POWER_S	UTIL_REG	UTIL_LUT	UTIL_SLICE	UTIL_RAM	UTIL_DSP	CONFIG_TA	FACTOR_SETTING
MC8051_ISE_000	16.476	60.694	0	0	579	3326	1211	0	0	0	00000000000000000
MC8051_ISE_001	18.493	54.075	0	0	571	2711	1122	0	7	1	00000011111111111
MC8051_ISE_002	16.985	58.875	0	0	620	3101	1244	0	7	2	00000101111111111
MC8051_ISE_003	16.917	59.112	0	0	539	3027	1120	0	0	3	00000110000000000
MC8051_ISE_004	16.488	60.65	0	0	540	3033	1183	0	1	4	00001001111111110

*Result in *.xml format*



```
    UTIL_REG="620"
    UTIL_LUT="3101"
    UTIL_SLICE="1244"
    UTIL_RAMB="0"
    UTIL_DSP="7"
    CONFIG_TABLE_INDEX="2"
    FACTOR_SETTING="0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0"/>

<Configuration
    CONFIGURATION="MC8051_ISE_003"
    CLK_PERIOD="16.917"
    MAX_FREQUENCY="59.112"
    POWER_DYNAMIC="0.000"
    POWER_STATIC="0.000"
    UTIL_REG="539"
    UTIL_LUT="3027"
    UTIL_SLICE="1120"
    UTIL_RAMB="0"
    UTIL_DSP="0"
    CONFIG_TABLE_INDEX="3"
    FACTOR_SETTING="0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1"/>
```

Monitoring page (open in Firefox, or any other browser under web-server)

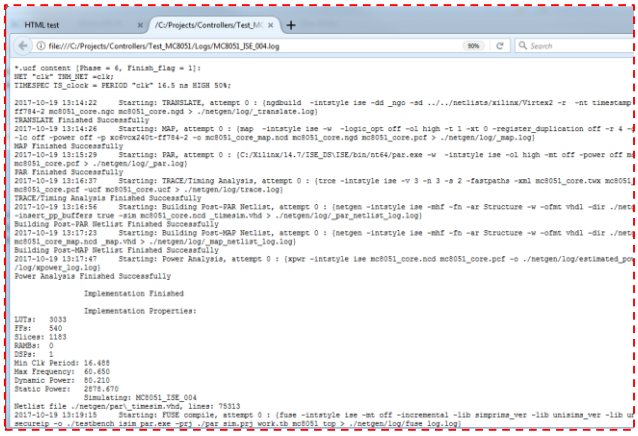


Connected, Last Update (13:23:33): 0.252 Kb

Phase	Progress	Time_Taken	Report
Implementation	100.00%	0:30:41	CSV, XML
Power Simulation	100.00%	0:04:15	CSV, XML

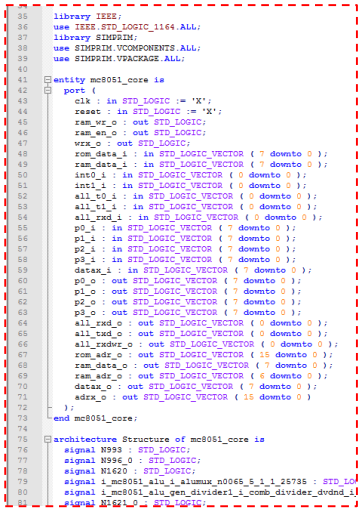
Label	FREQ	POWER_DYN	SLICE	REG	LUT	DSP	RAMB	Progress	Iteration	Clock	Converged	Synthesis	Translate	Map	PlaceRoute	TimingAnalysis	NetlistBuilder	Fuse_Compile	Simulation_ISIM	PowerAnalysis
MC8051_ISE_000	60.69	116.07	1211	579	3326	0	0	Completed: 2017-10-19 13:19:11	5	16.5	Yes	100%: 0:00:02	100%: 0:00:05	100%: 0:01:10	100%: 0:01:14	100%: 0:00:20	100%: 0:00:25	100%: 0:00:26	100%: 0:00:21	100%: 0:00:19
MC8051_ISE_001	54.08	103.74	1122	571	2711	7	0	Completed: 2017-10-19 13:22:16	1	18.5	Yes	100%: 0:00:01	100%: 0:00:05	100%: 0:01:17	100%: 0:01:14	100%: 0:00:23	100%: 0:00:30	100%: 0:03:20	100%: 0:00:35	100%: 0:00:15
MC8051_ISE_002	58.88	110.11	1244	620	3101	7	0	Completed: 2017-10-19 13:22:13	4	17.0	Yes	100%: 0:00:01	100%: 0:00:05	100%: 0:01:21	100%: 0:01:17	100%: 0:00:22	100%: 0:00:29	100%: 0:03:20	100%: 0:00:31	100%: 0:00:16
MC8051_ISE_003	59.11	115.65	1120	539	3027	0	0	Completed: 2017-10-19 13:19:12	4	17.0	Yes	100%: 0:00:01	100%: 0:00:05	100%: 0:01:12	100%: 0:01:13	100%: 0:00:22	100%: 0:00:27	100%: 0:00:25	100%: 0:00:23	100%: 0:00:19
MC8051_ISE_004	60.65	114.82	1183	540	3033	1	0	Completed: 2017-10-19 13:21:13	6	16.5	Yes	100%: 0:00:01	100%: 0:00:04	100%: 0:01:03	100%: 0:01:08	100%: 0:00:19	100%: 0:00:24	100%: 0:01:20	100%: 0:00:20	100%: 0:00:18
MC8051_ISE_Default	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Detailed log



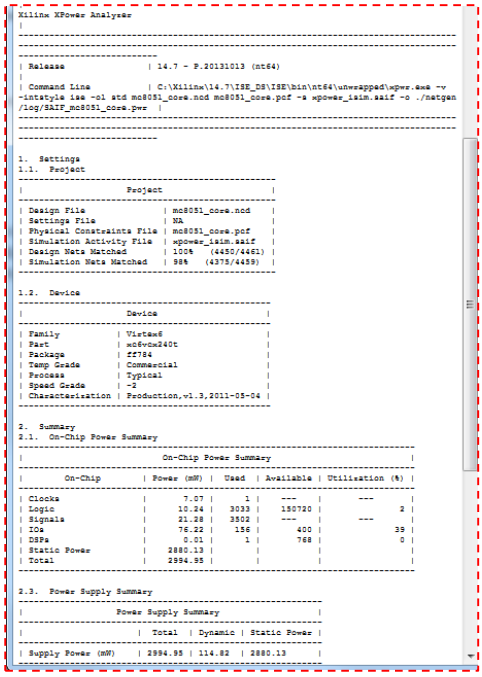
```
*.ucf content {Phase = 6, Finish_flag = 1}:
NET "clk" TNM_NET =clk;
TIMESPEC TS_clock = PERIOD "clk" 16.5 ns HIGH 50%;

2017-10-19 13:14:22     Starting: TRANSLATE, attempt 0 : {ngdbuild  -intstyle ise -dd _ngo -sd ../../netlists/xilinx/Virtex2 -r  -nt timestamp
ff784-2 mc8051_core.ngc mc8051_core.ngd > ./netgen/log/_translate.log}
TRANSLATE Finished Successfully
2017-10-19 13:14:26     Starting: MAP, attempt 0 : {map  -intstyle ise -w  -logic_opt off -ol high -t 1 -xt 0 -register_duplication off -r 4 -
-lc off -power off -p xc4vux240t-ff784-2 -o mc8051_core_map.ncd mc8051_core.ngd mc8051_core.pcf > ./netgen/log/_map.log}
MAP Finished Successfully
2017-10-19 13:15:29     Starting: PAR, attempt 0 : {C:/Xilinx/14.7/ISE_DS\ISE/bin/nt64/par.exe -w  -intstyle ise -ol high -mt off -power off m
mc8051_core.pcf > ./netgen/log/_par.log}
PAR Finished Successfully
2017-10-19 13:16:37     Starting: TRACE/Timing Analysis, attempt 0 : {trce -intstyle ise -v 3 -n 3 -s 2 -fastpaths -xml mc8051_core.twx mc8051
mc8051_core.pcf -ucf mc8051_core.ucf > ./netgen/log/trace.log}
TRACE/Timing Analysis Finished Successfully
2017-10-19 13:16:56     Starting: Building Post-PAR Netlist, attempt 0 : {netgen -intstyle ise -mhf -fn -ar Structure -w -ofmt vhdl -dir ./net
-insert_pp_buffers true -sim mc8051_core.ncd _timesim.vhd > ./netgen/log/_par_netlist_log.log}
Building Post-PAR Netlist Finished Successfully
2017-10-19 13:17:23     Starting: Building Post-MAP Netlist, attempt 0 : {netgen -intstyle ise -mhf -fn -ar Structure -w -ofmt vhdl -dir ./net
mc8051_core_map.ncd _map.vhd > ./netgen/log/_map_netlist_log.log}
Building Post-MAP Netlist Finished Successfully
2017-10-19 13:17:47     Starting: Power Analysis, attempt 0 : {xpwr -intstyle ise mc8051_core.ncd mc8051_core.pcf -o ./netgen/log/estimated_po
/log/xpower_log.log}
Power Analysis Finished Successfully

                Implementation Finished

                Implementation Properties:

LUTs:   3033
FFs:    540
Slices: 1183
RAMBs:  0
DSPs:   1
Min Clk Period: 16.488
Max Frequency:  60.650
Dynamic Power:  80.210
Static Power:   2878.670
                Simulating: MC8051_ISE_004
Netlist file ./netgen/par\_timesim.vhd, lines: 75313
2017-10-19 13:19:18     Starting: FUSE compile, attempt 0 : {fuse -intstyle ise -nt off -incremental -lib simprims_ver -lib unisims_ver -lib u
secureip -o ./testbench isim_par.exe -prj ./par_sim.prj work.th_mc8051_top > ./netgen/log/fuse_log.log}
```

Resulting netlist



```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library SIMPRIM;
use SIMPRIM.VCOMPONENTS.ALL;
use SIMPRIM.VPACKAGE.ALL;

entity mc8051_core is
  port (
    clk : in STD_LOGIC := 'X';
    reset : in STD_LOGIC := 'X';
    ram_wr_o : out STD_LOGIC;
    ram_en_o : out STD_LOGIC;
    wrx_o : out STD_LOGIC;
    rom_data_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    ram_data_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    int0_i : in STD_LOGIC_VECTOR ( 0 downto 0 );
    int1_i : in STD_LOGIC_VECTOR ( 0 downto 0 );
    all_t0_i : in STD_LOGIC_VECTOR ( 0 downto 0 );
    all_t1_i : in STD_LOGIC_VECTOR ( 0 downto 0 );
    all_rxd_i : in STD_LOGIC_VECTOR ( 0 downto 0 );
    p0_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    p1_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    p2_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    p3_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    datax_i : in STD_LOGIC_VECTOR ( 7 downto 0 );
    p0_o : out STD_LOGIC_VECTOR ( 7 downto 0 );
    p1_o : out STD_LOGIC_VECTOR ( 7 downto 0 );
    p2_o : out STD_LOGIC_VECTOR ( 7 downto 0 );
    p3_o : out STD_LOGIC_VECTOR ( 7 downto 0 );
    all_rxd_o : out STD_LOGIC_VECTOR ( 0 downto 0 );
    all_txd_o : out STD_LOGIC_VECTOR ( 0 downto 0 );
    all_rxdwr_o : out STD_LOGIC_VECTOR ( 0 downto 0 );
    rom_adr_o : out STD_LOGIC_VECTOR ( 15 downto 0 );
    ram_data_o : out STD_LOGIC_VECTOR ( 7 downto 0 );
    ram_adr_o : out STD_LOGIC_VECTOR ( 6 downto 0 );
    datax_o : out STD_LOGIC_VECTOR ( 7 downto 0 );
    adrx_o : out STD_LOGIC_VECTOR ( 15 downto 0 )
  );
end mc8051_core;

architecture Structure of mc8051_core is
  signal N993 : STD_LOGIC;
  signal N996_0 : STD_LOGIC;
  signal N1620 : STD_LOGIC;
  signal i_mc8051_alu_1_alumux_n0065_5_1_1_25735 : STD_LO
  signal i_mc8051_alu_gen_divider1_i_comb_divider_dvdnd_i
  signal N1621_0 : STD_LOGIC;
```

Detailed Power report



```
Xilinx XPower Analyzer
|
------------------------------------------------------------------------------
------------------------------------------------------------------------------
--------------------------
| Release          | 14.7 - P.20131013 (nt64)
|
| Command Line     | C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\xpwr.exe -v
-intstyle ise -ol std mc8051_core.ncd mc8051_core.pcf -a xpower_isim.saif -o ./netgen
/log/SAIF_mc8051_core.pwr  |
------------------------------------------------------------------------------
------------------------------------------------------------------------------
--------------------

1.  Settings
1.1.  Project
-------------------------------------------------
|                Project                |
-------------------------------------------------
| Design File             | mc8051_core.ncd   |
| Settings File           | NA                |
| Physical Constraints File | mc8051_core.pcf |
| Simulation Activity File | xpower_isim.saif |
| Design Nets Matched     | 100%  (4450/4461) |
| Simulation Nets Matched | 98%   (4375/4459) |
-------------------------------------------------

1.2.  Device
-------------------------------------------------
|                Device                 |
-------------------------------------------------
| Family          | Virtex4             |
| Part            | xc4vux240t          |
| Package         | ff784               |
| Temp Grade      | Commercial          |
| Process         | Typical             |
| Speed Grade     | -2                  |
| Characterization | Production,v1.3,2011-05-04 |
-------------------------------------------------

2.  Summary
2.1.  On-Chip Power Summary
-------------------------------------------------------------------------------
|                On-Chip Power Summary                |
-------------------------------------------------------------------------------
|      On-Chip      | Power (mW) |  Used  | Available | Utilization (%) |
-------------------------------------------------------------------------------
| Clocks            |       7.07 |      1 |       --- |             --- |
| Logic             |      10.24 |   3033 |    150720 |               2 |
| Signals           |      21.28 |   3302 |       --- |             --- |
| IOs               |      76.22 |    156 |       400 |              39 |
| DSPs              |       0.01 |      1 |       768 |               0 |
| Static Power      |    2880.13 |        |           |                 |
| Total             |    2994.95 |        |           |                 |
-------------------------------------------------------------------------------

2.3.  Power Supply Summary
-------------------------------------------------------------
|              Power Supply Summary              |
-------------------------------------------------------------
|                | Total  | Dynamic | Static Power |
-------------------------------------------------------------
| Supply Power (mW) | 2994.95 | 114.82 | 2880.13 |
-------------------------------------------------------------
```