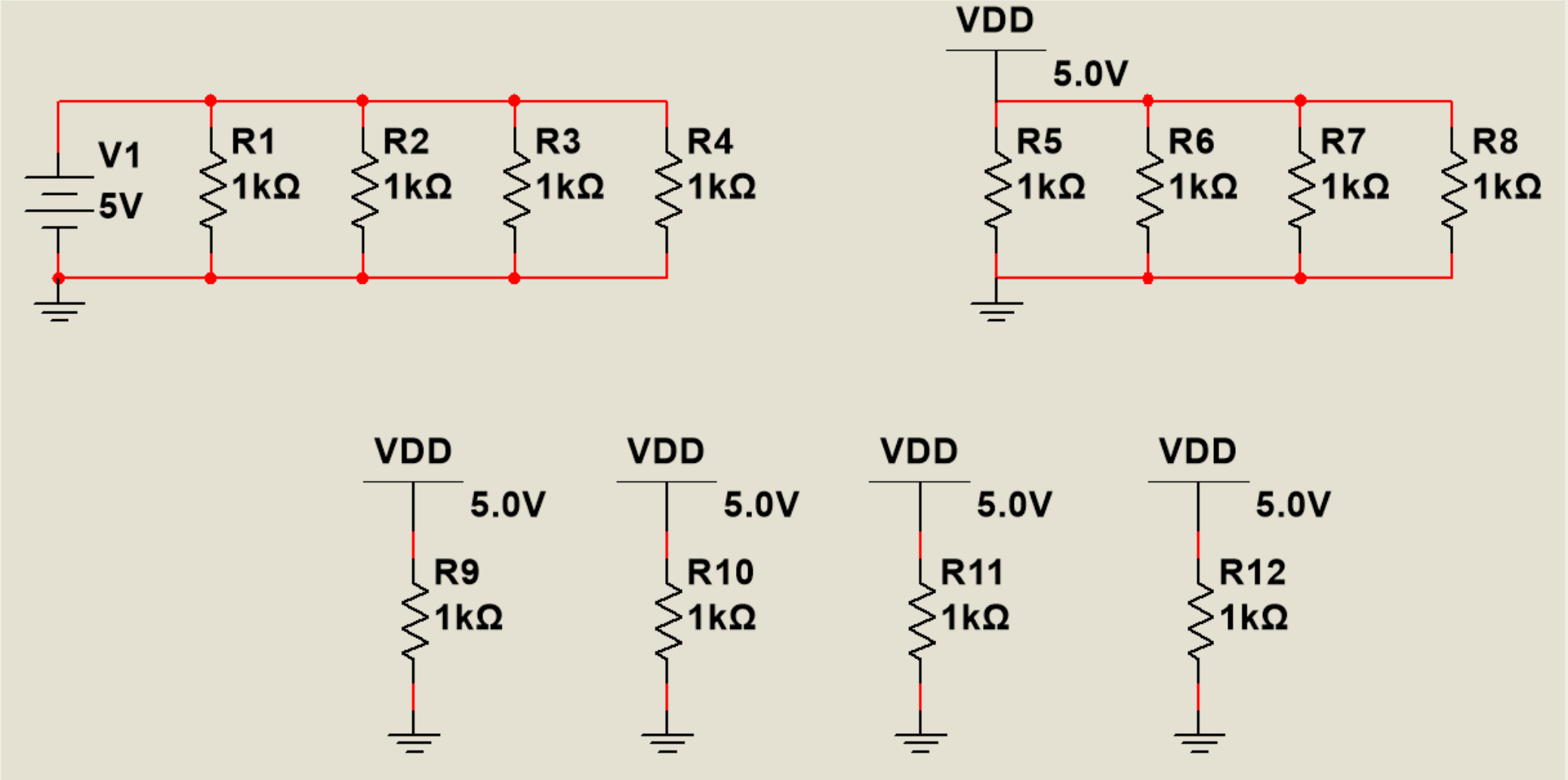
SI100B TUTOURIAL-2

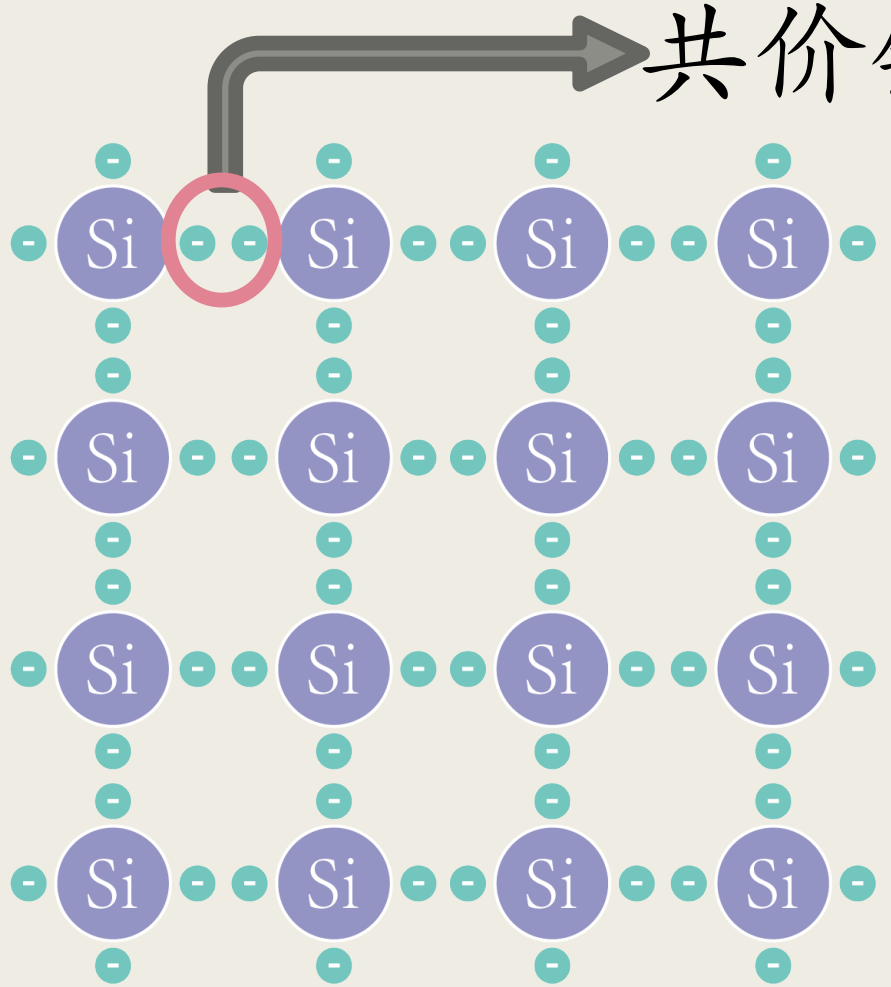
Semiconductor, Devices, and Transistor-level Logic Gates

Li Teng, Jiangting Xia, Haochuan Wan

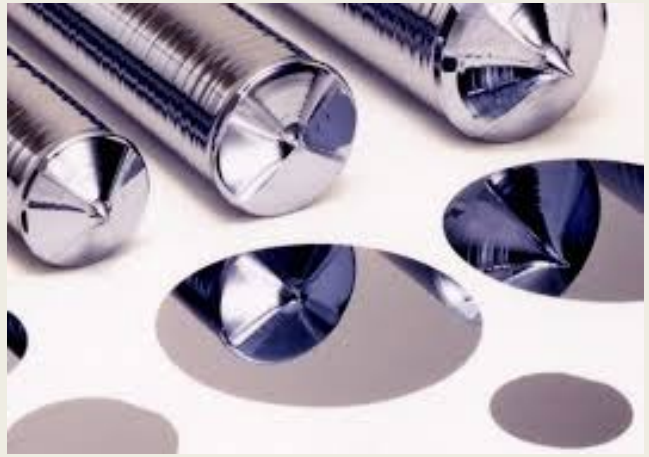
Voltage Rail



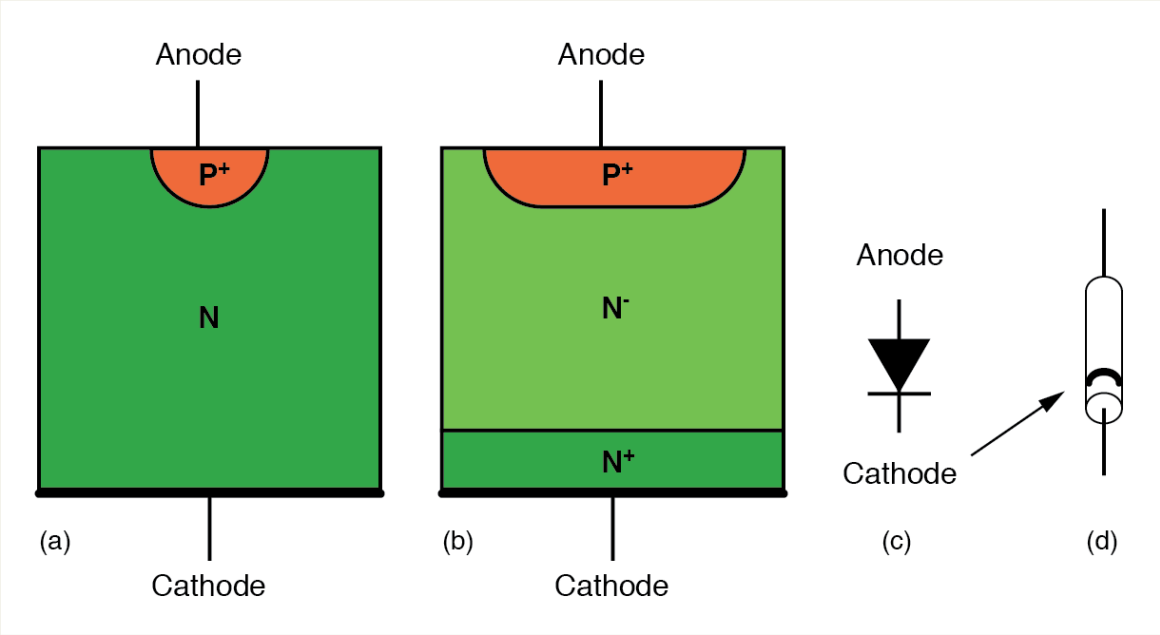
Silicon (硅)

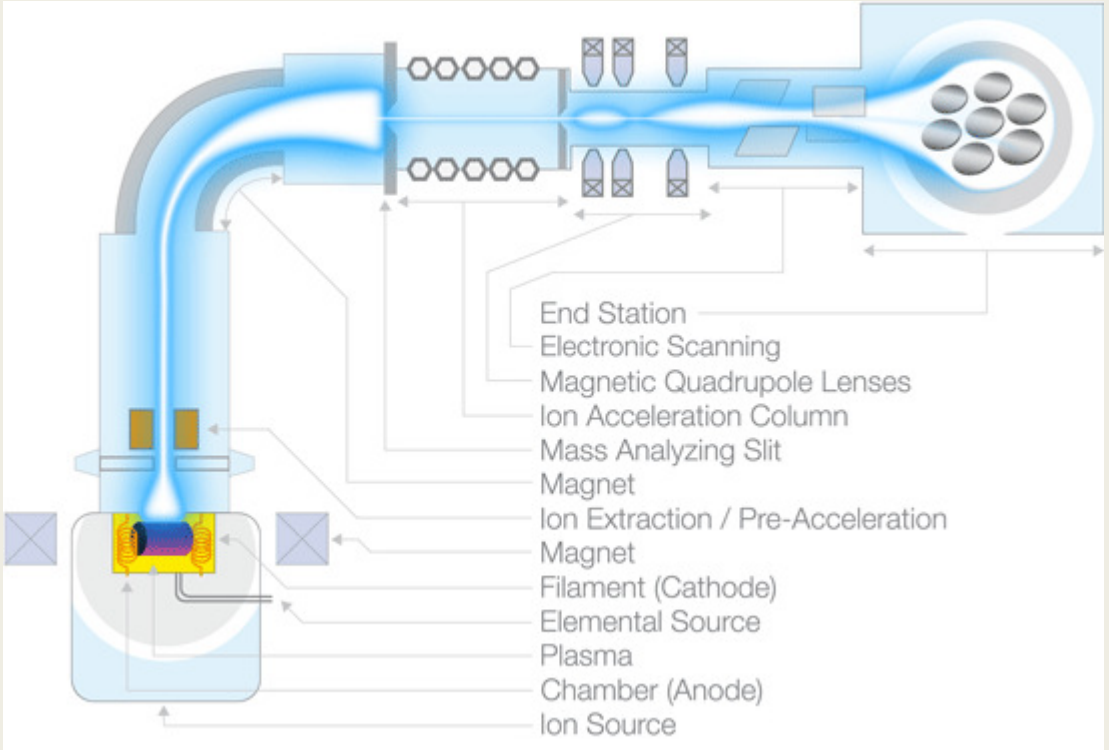


5 B 硼	6 C 碳	7 N 氮
13 Al 铝	14 Si 硅	15 P 磷



PN Junction and Semiconductor Doping (PN结与半导体掺杂)

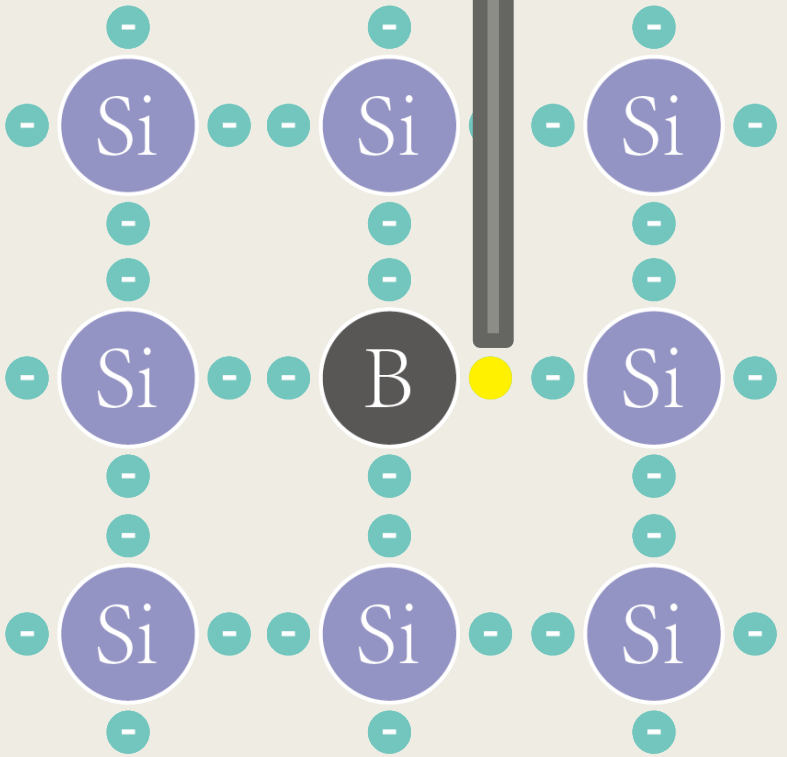




P-type Semiconductor
(P型半导体)

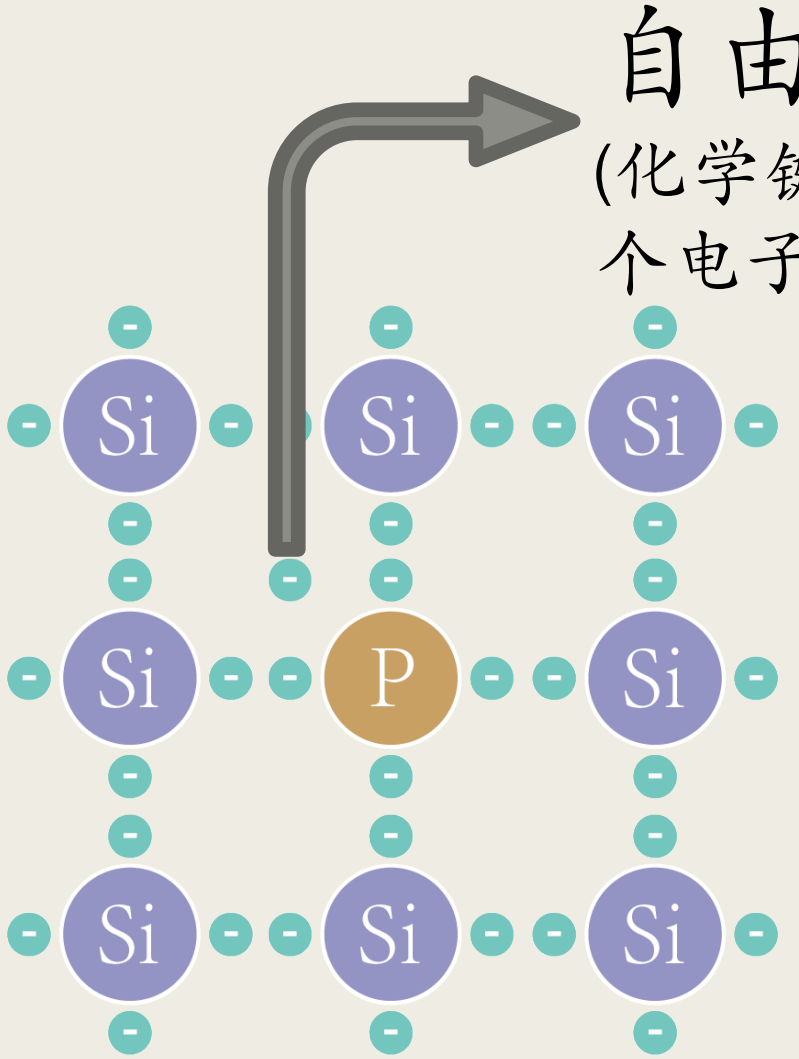
5 B 硼	6 C 碳	7 N 氮
13 Al 铝	14 Si 硅	15 P 磷

空穴
(化学键缺
失一个电子)

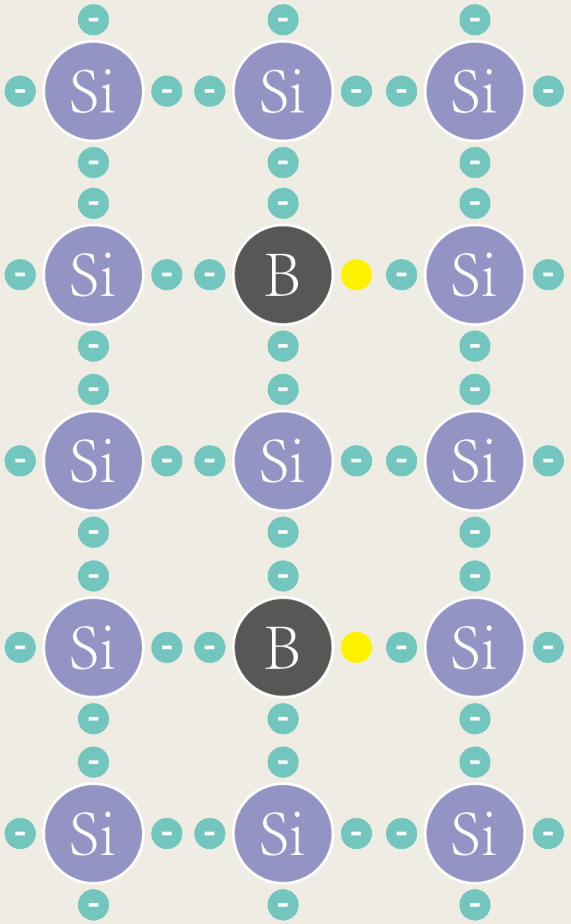


N-type Semiconductor (N型半导体)

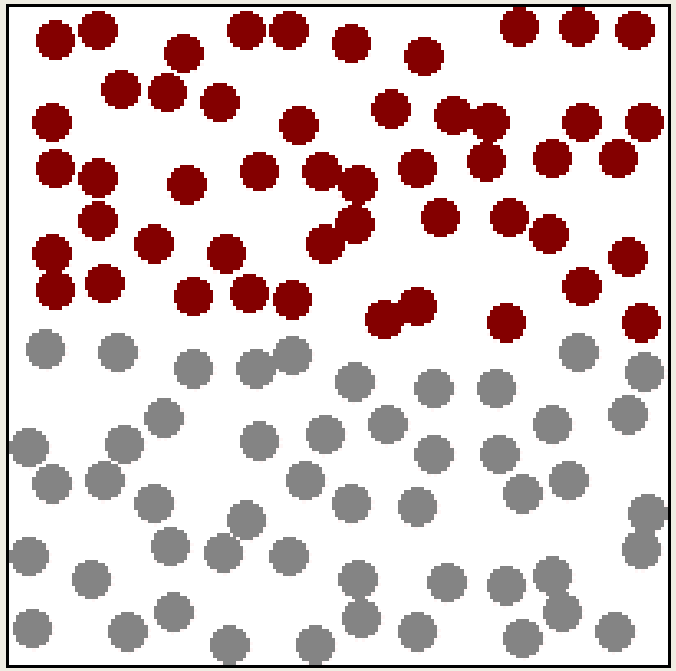
5 B 硼	6 C 碳	7 N 氮
13 Al 铝	14 Si 硅	15 P 磷

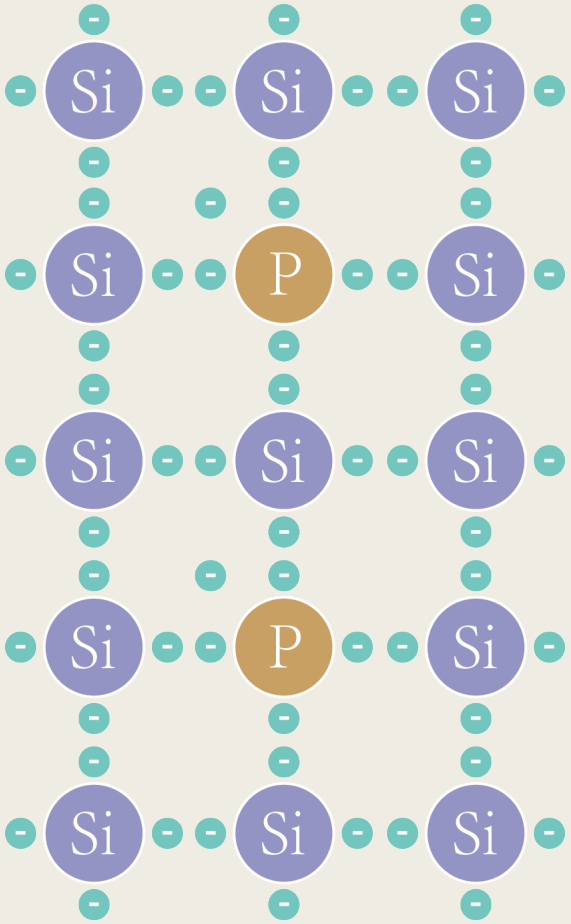


PN Junction



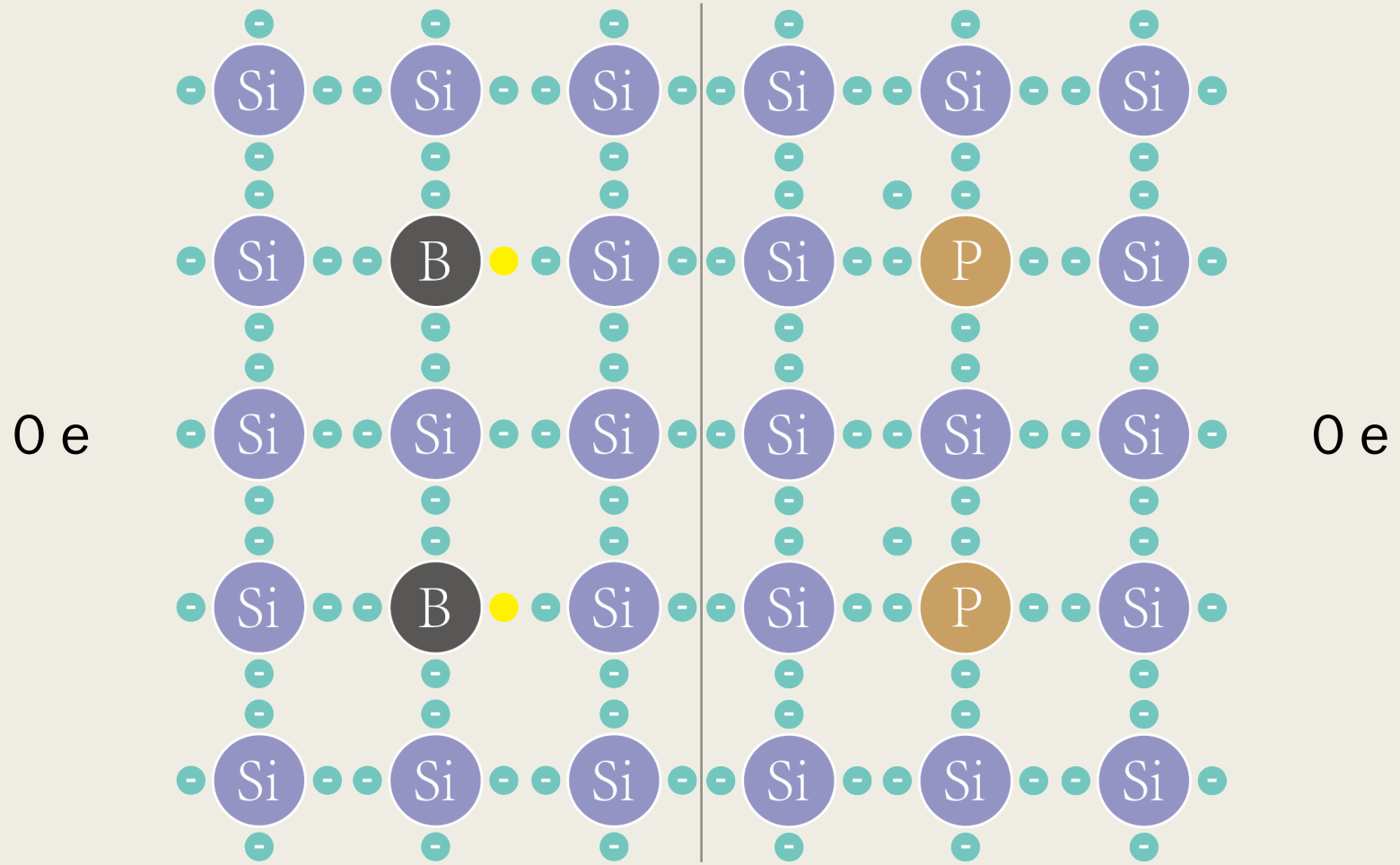
P-type



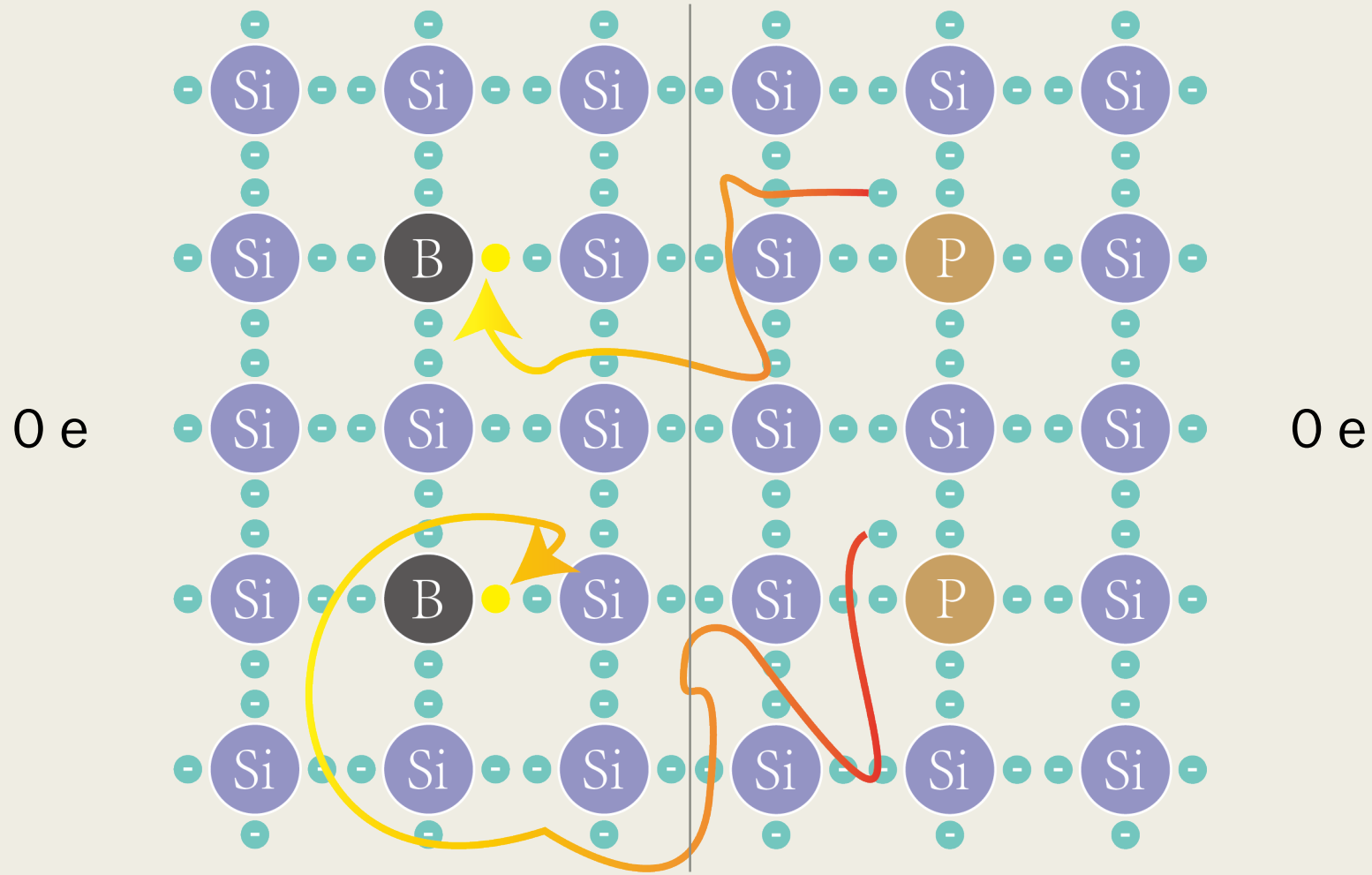


N-type

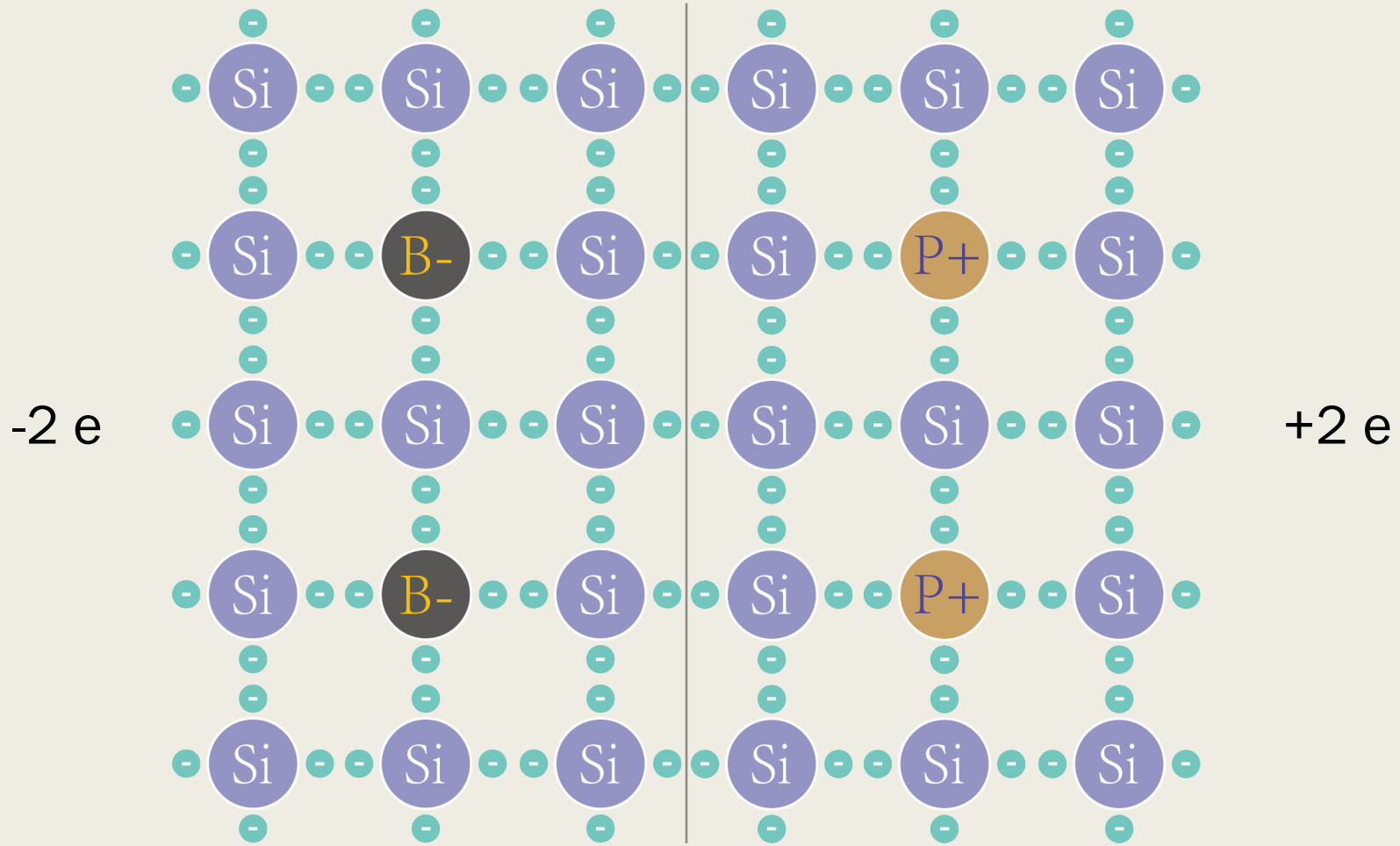
Diffusion & Combination in PN Junction
PN结中的载流子扩散与复合



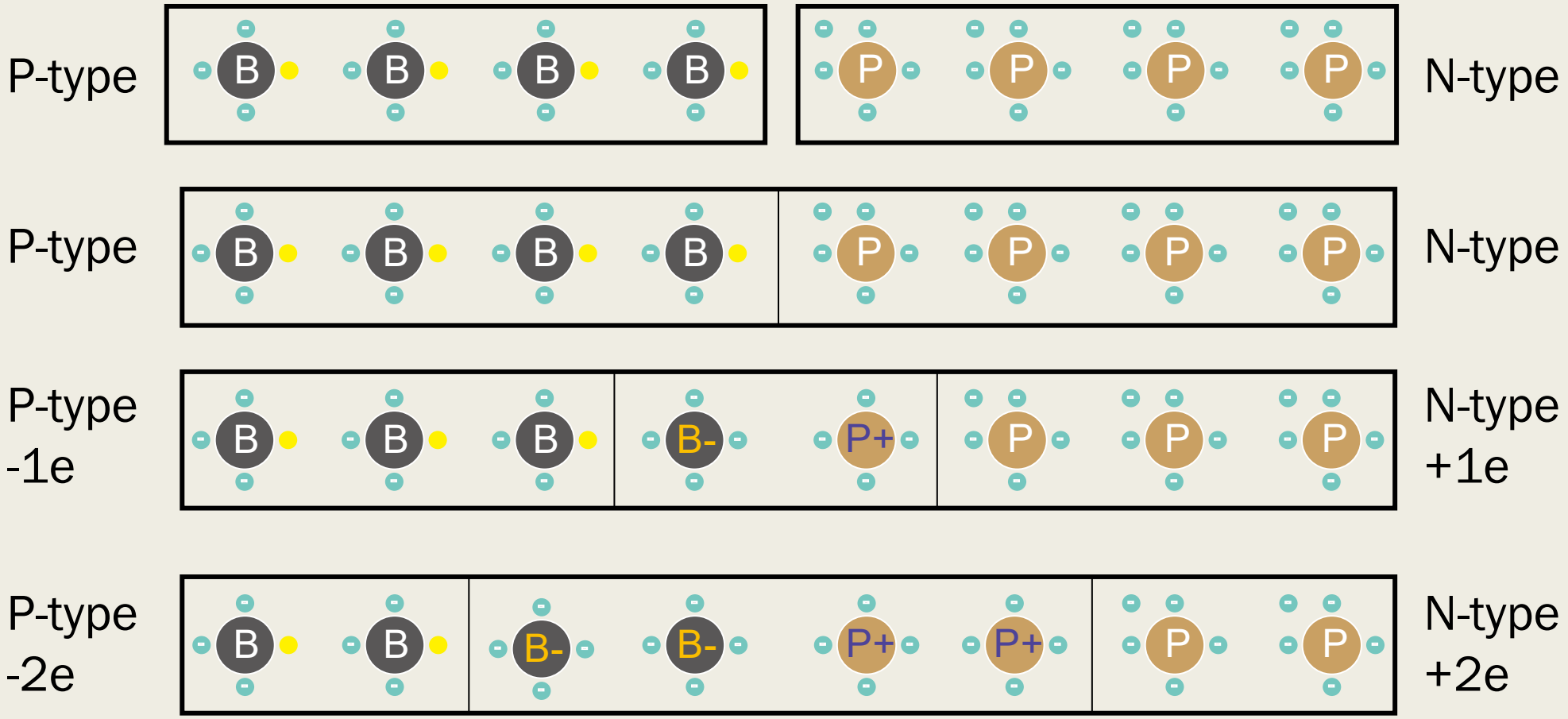
Diffusion & Combination in PN Junction
PN结中的载流子扩散与复合



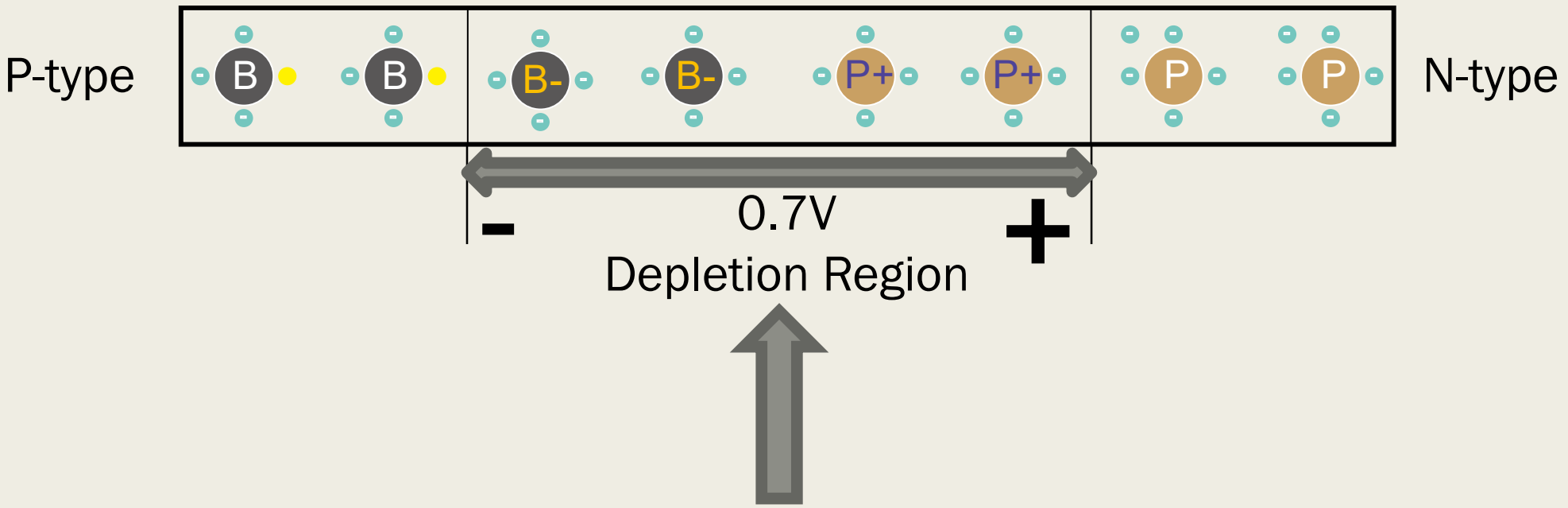
Diffusion & Combination in PN Junction
PN结中的载流子扩散与复合



Diffusion & Combination in PN Junction
PN结中的载流子扩散与复合

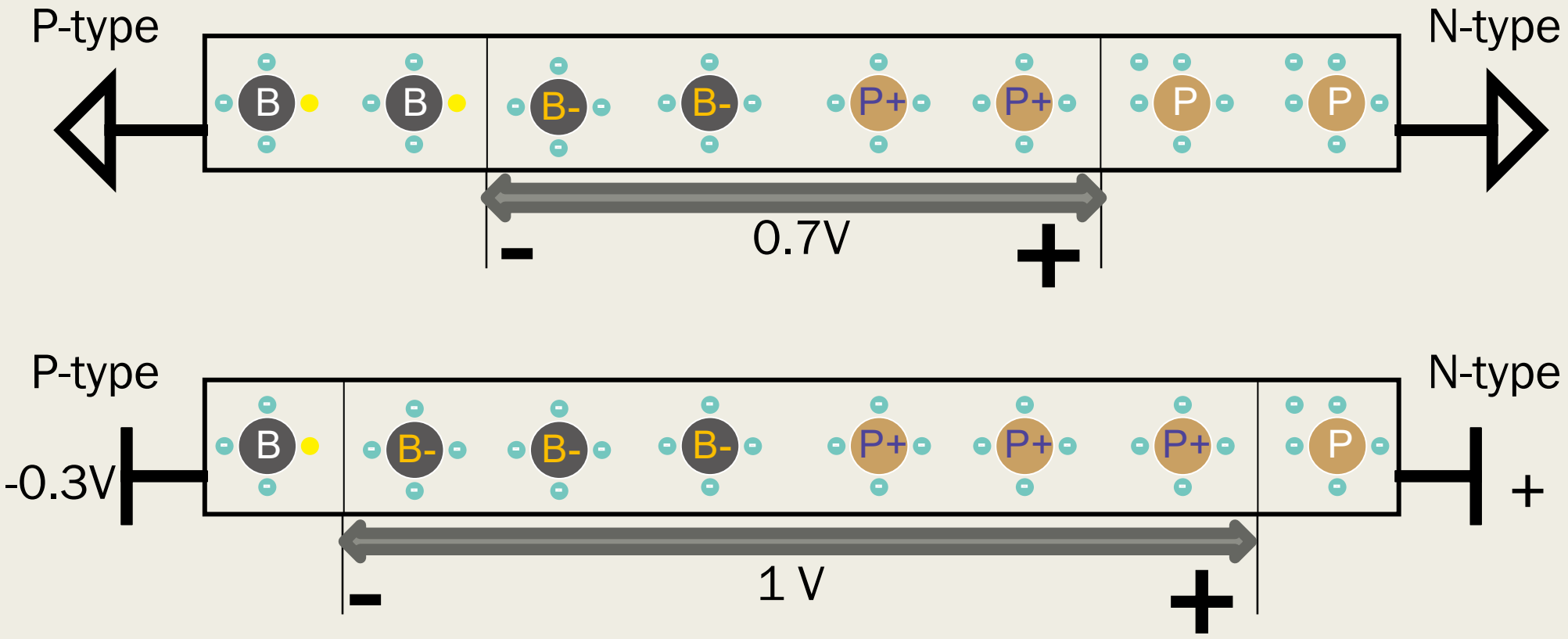


Electric Field inside PN Junction
PN结中的内建电场

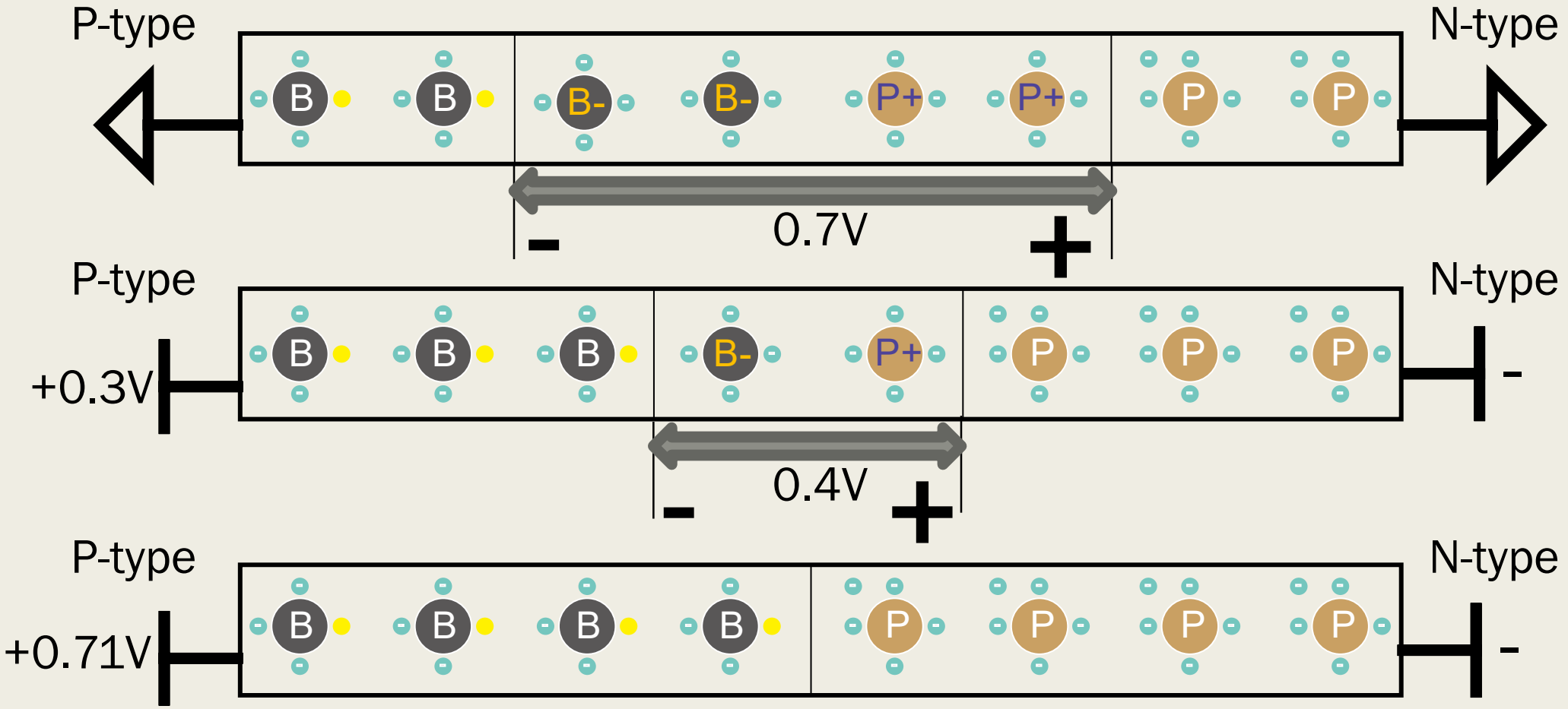


- 由于电子的扩散和与空穴的耗尽，PN结中间形成约0.7V电势的内建电场，称为耗尽层。
- 耗尽层中没有自由电子和空穴，因此为绝缘体，电阻值很大。

PN Junction under Reverse Voltage Bias
反向电压偏置的PN结

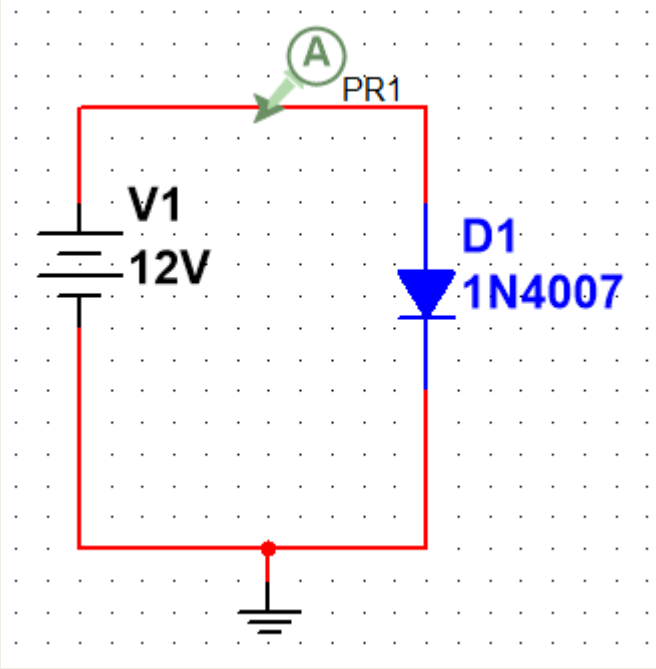


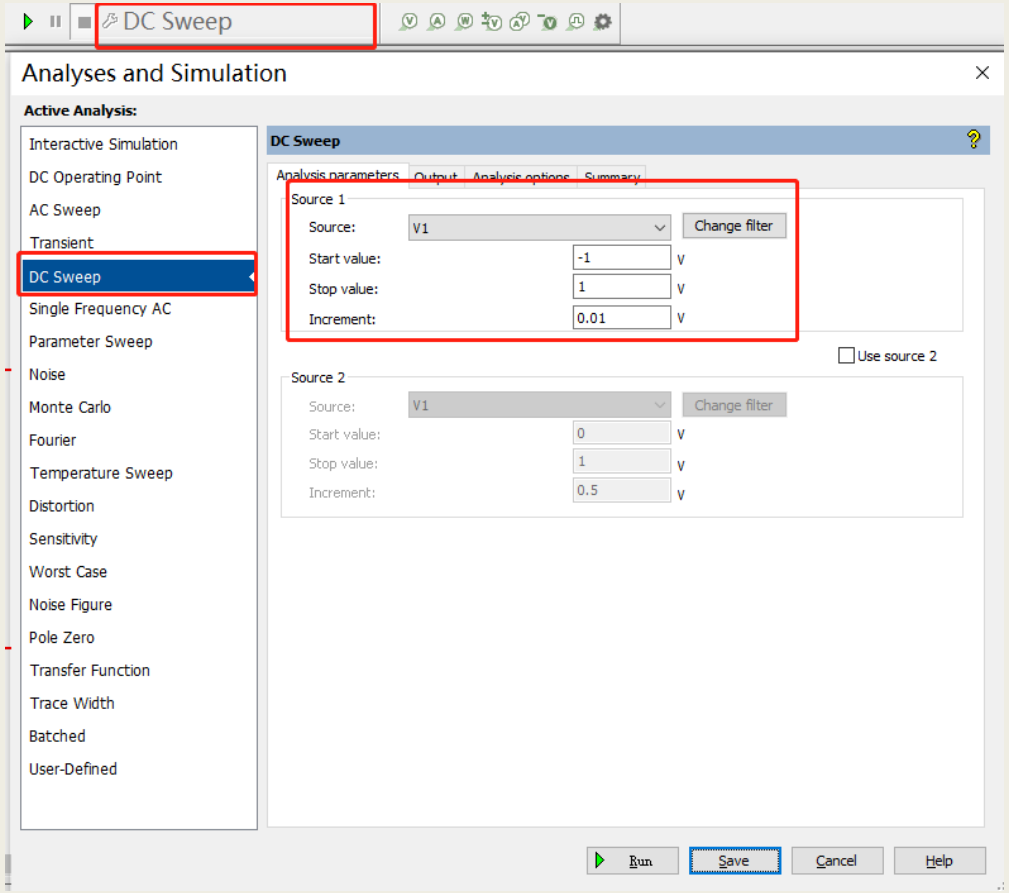
PN Junction under Reverse Voltage Bias
反向电压偏置的PN结

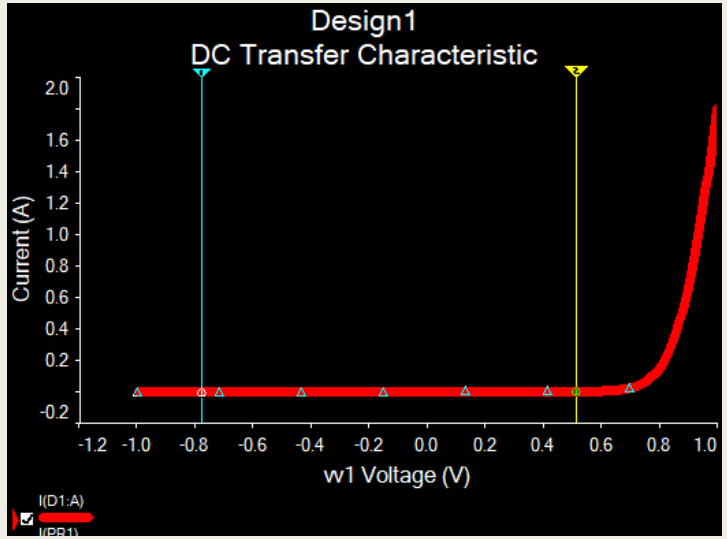


耗尽层电场被完全抵消，高电阻区域消失

I/V Curve of Diode (PN Junction)
二极管的伏安特性曲线

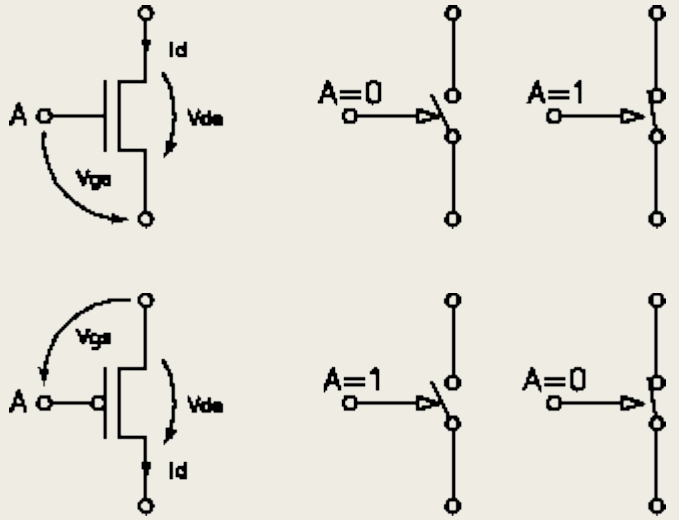


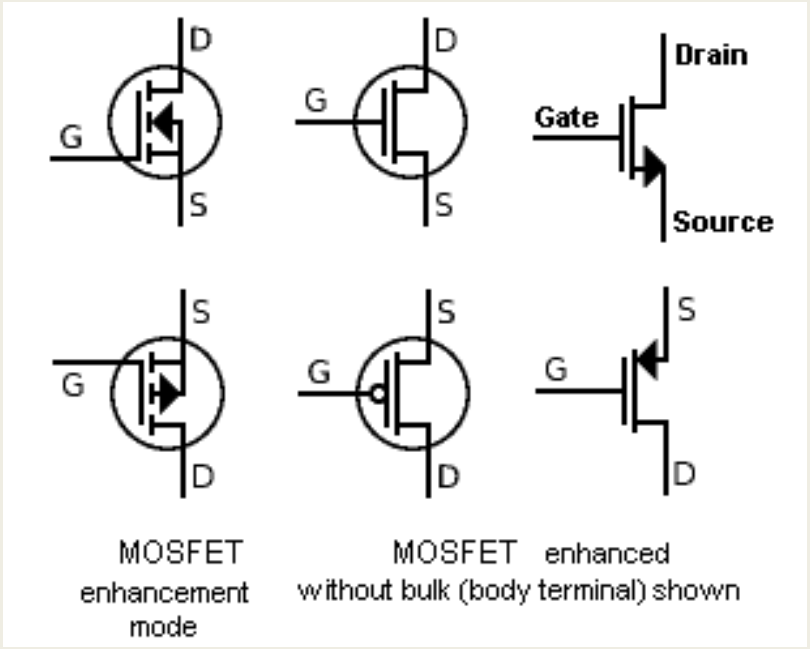


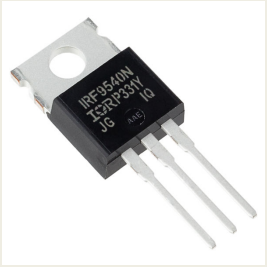


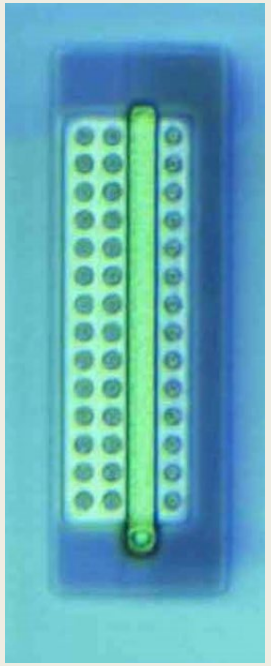
MOSFET

Metal-Oxide-Semiconductor Field Effect Transistor (金属-氧化物-半导体 场效应晶体管)

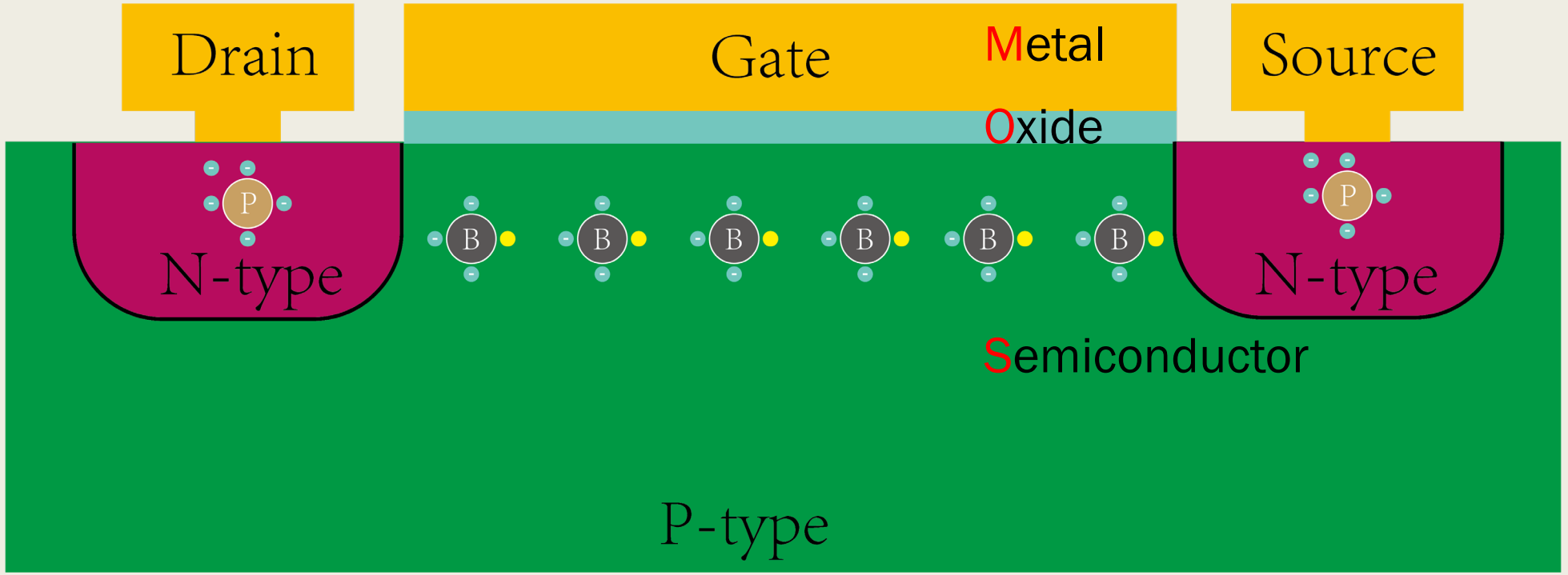




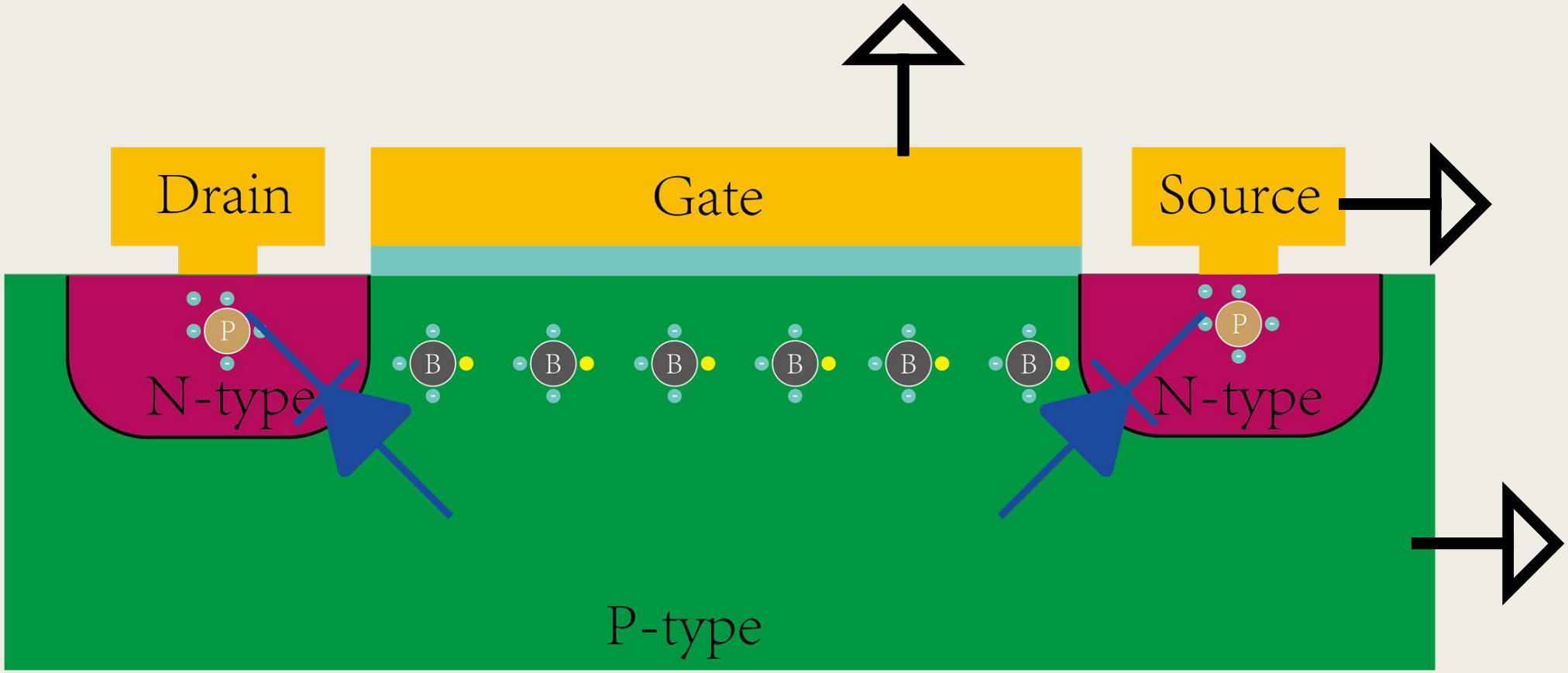




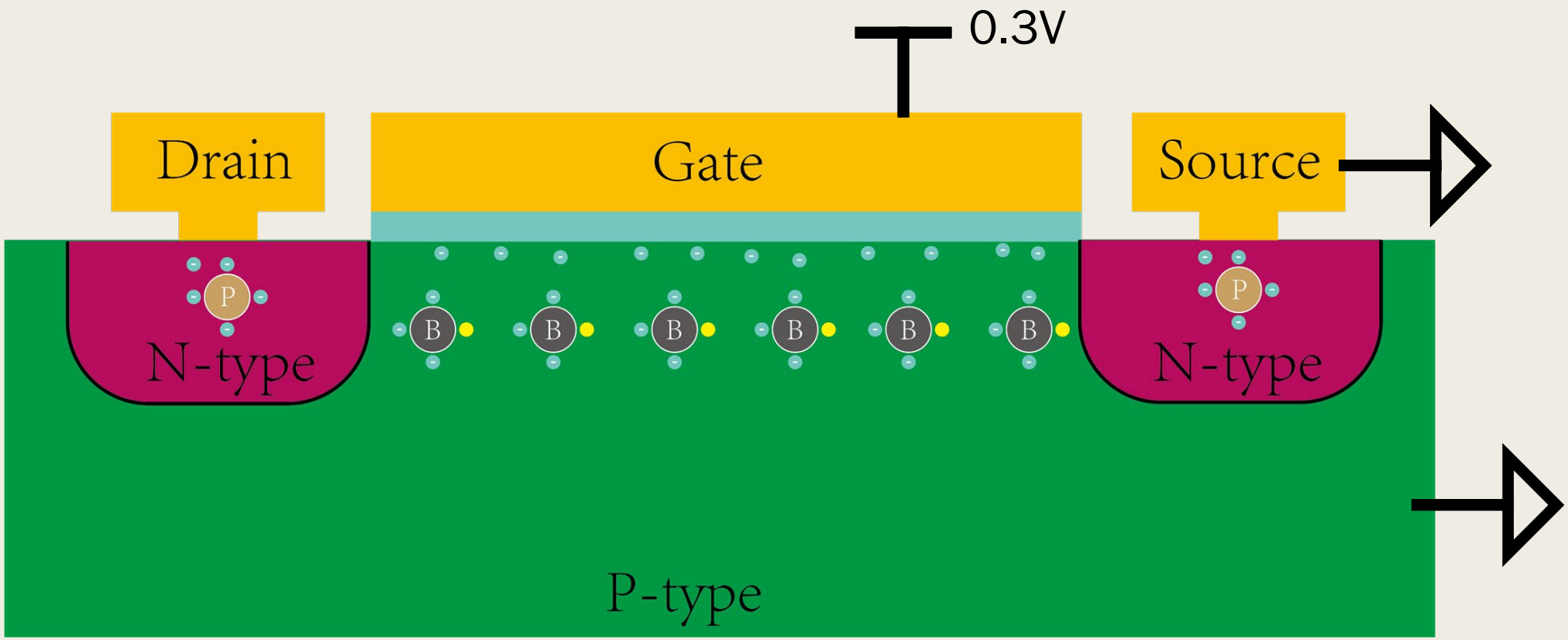
Simple Working Principle of MOSFET (金属-氧化物-半导体场效应晶体管)



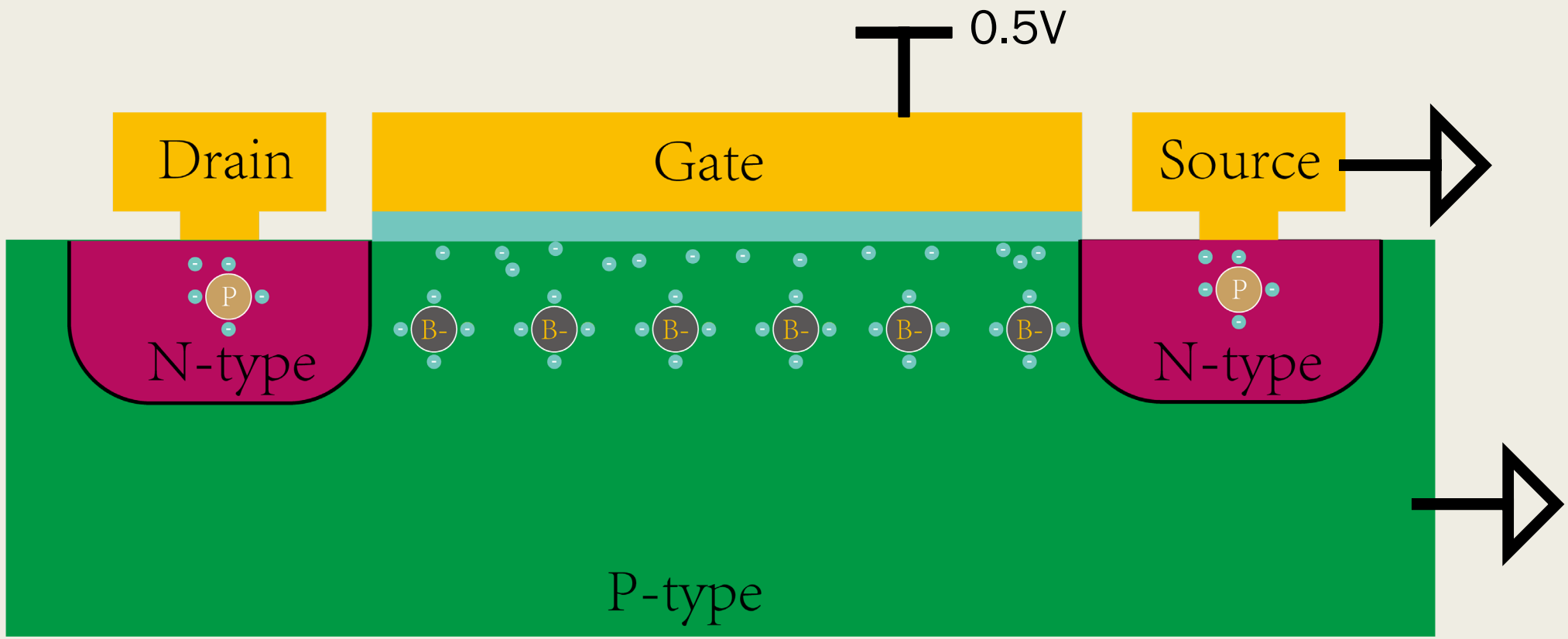
MOSFET的关断状态



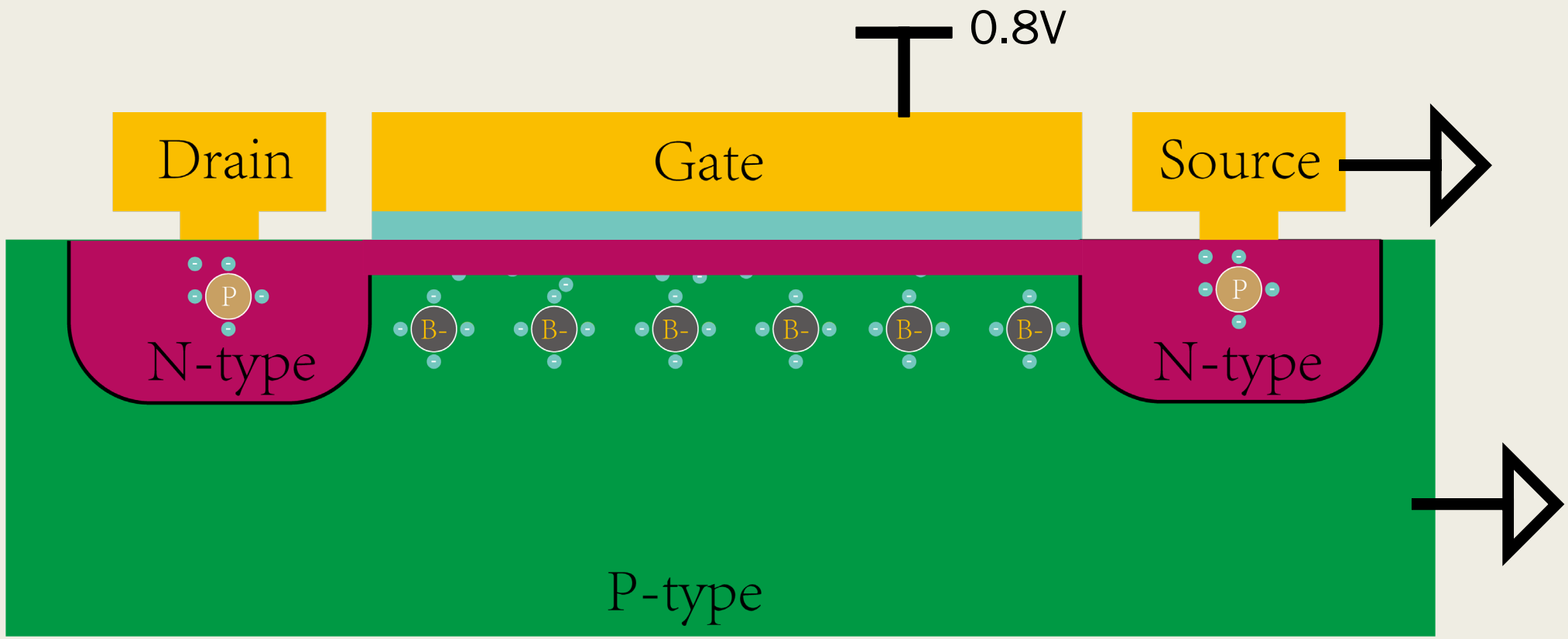
MOSFET的电荷累积过程



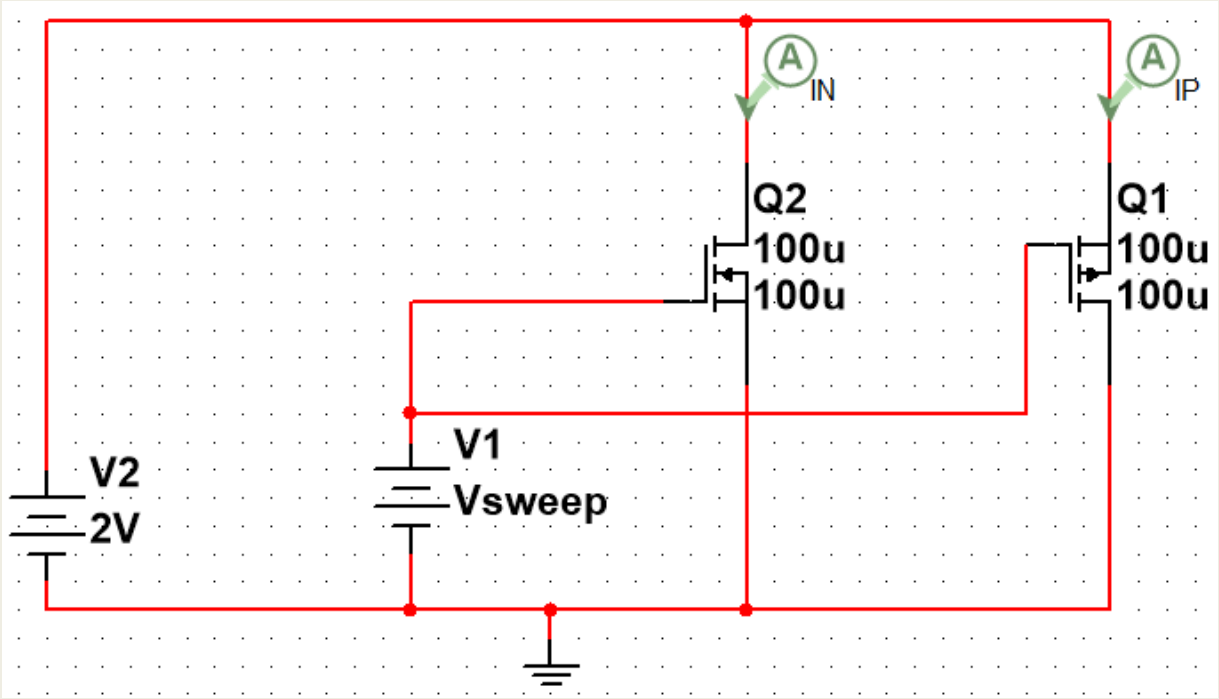
MOSFET耗尽过程

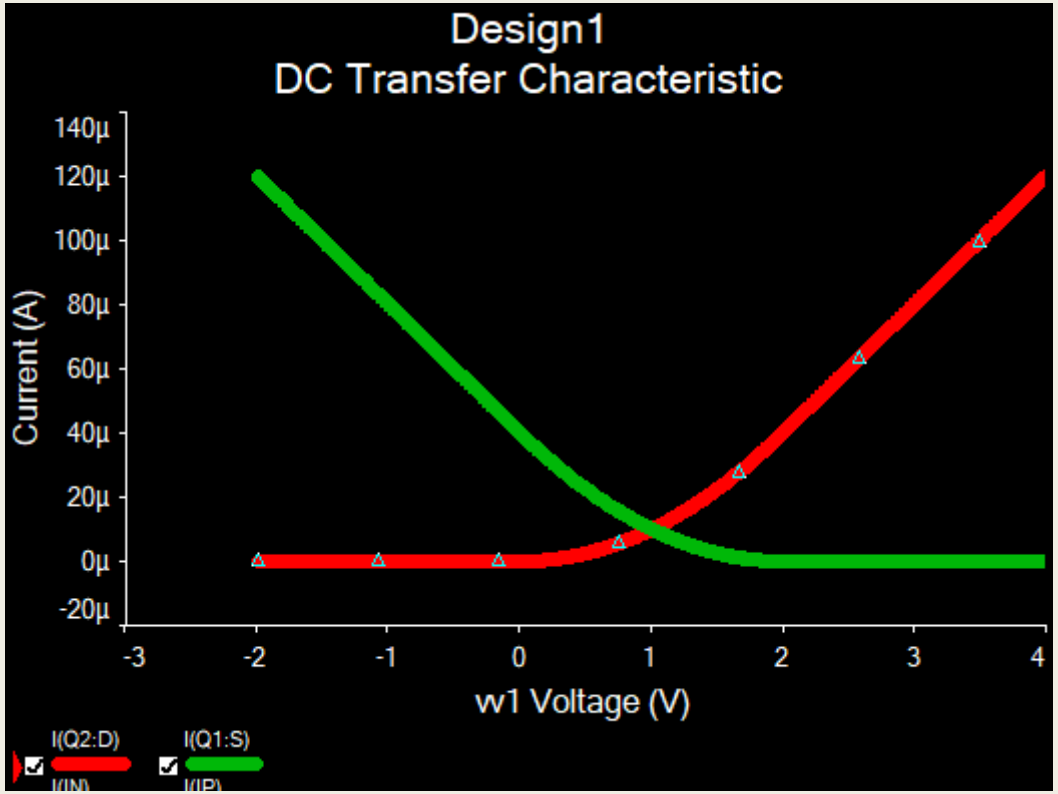


MOSFET 的导通态 (反型)



I-V_{GS} Curve of NMOS and PMOS



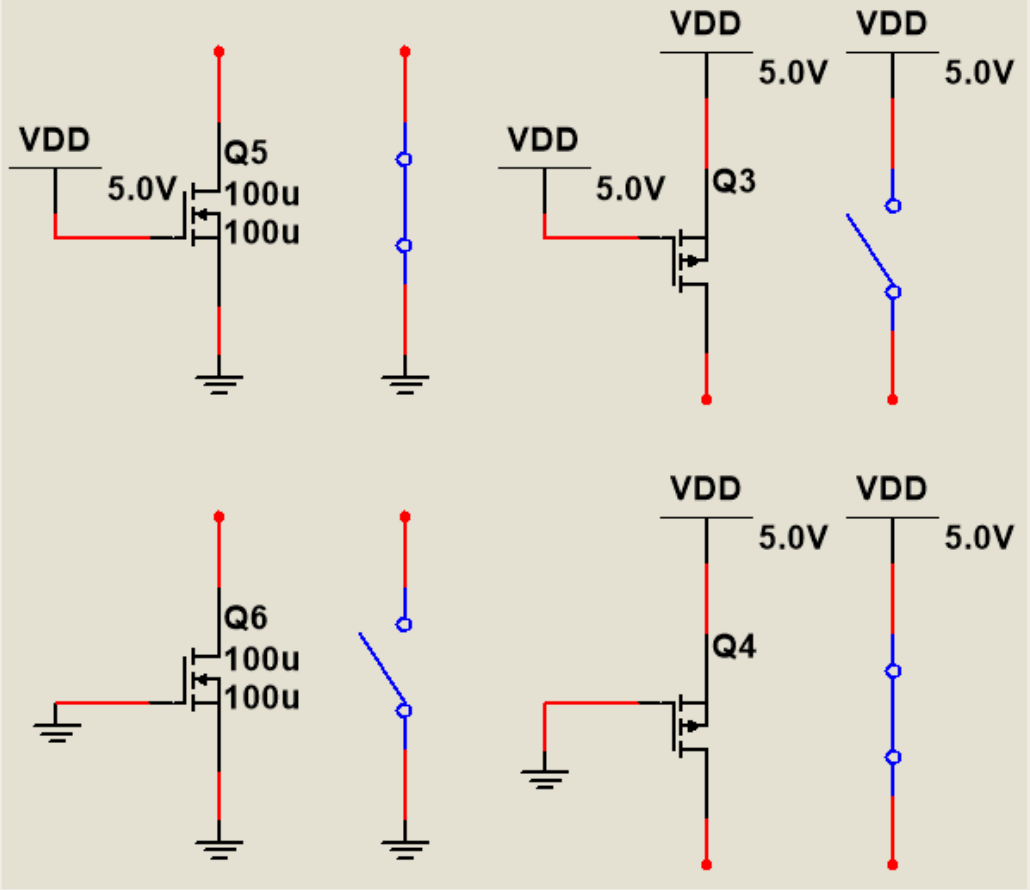


From MOSFETs to Logic Gate

NMOS:

if(input=1)
output=0

if(input=0)
output=?



PMOS:

if(input=1)
output=?

if(input=0)
output=1

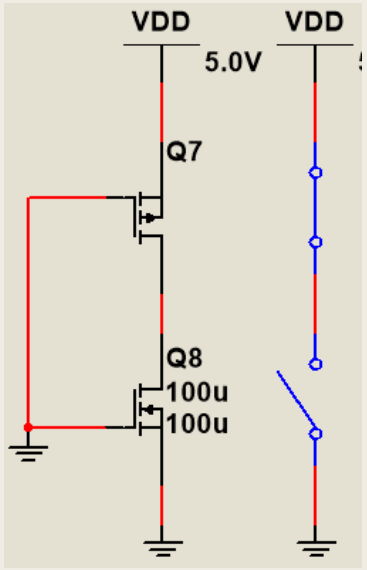
From MOSFETs to Logic Gate

PMOS:

if(input=0)
output=1

NMOS:

if(input=0)
output=?

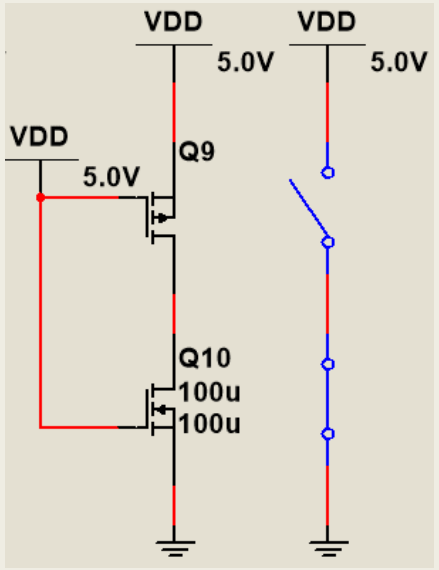


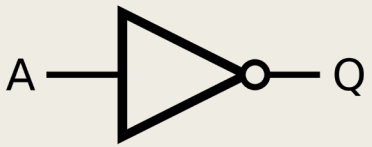
PMOS:

if(input=1)
output=?

NMOS:

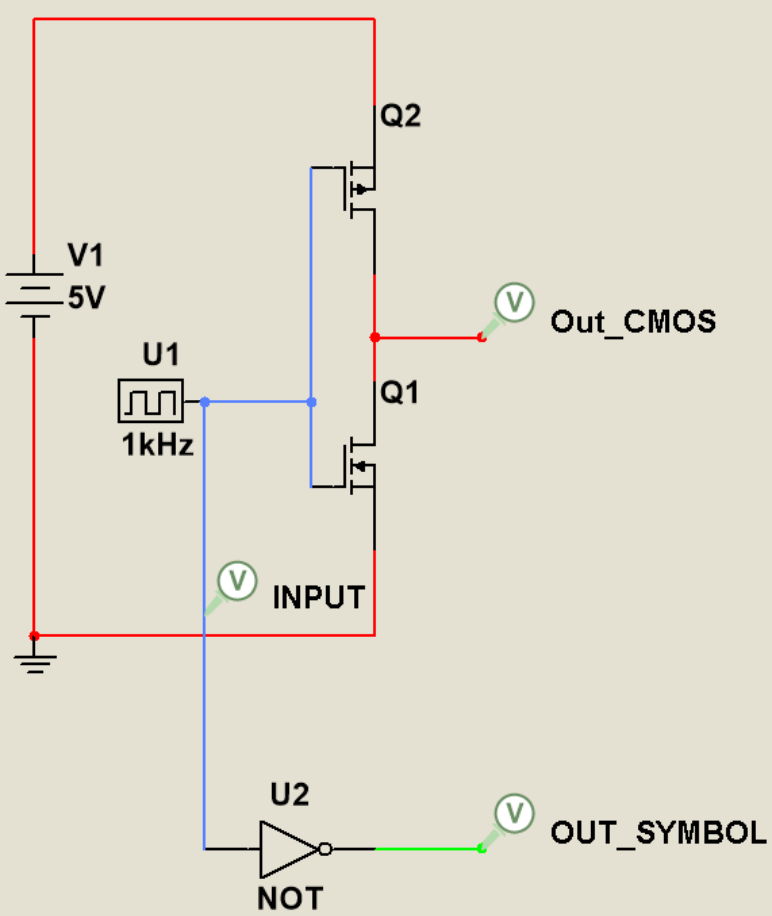
if(input=1)
output=0

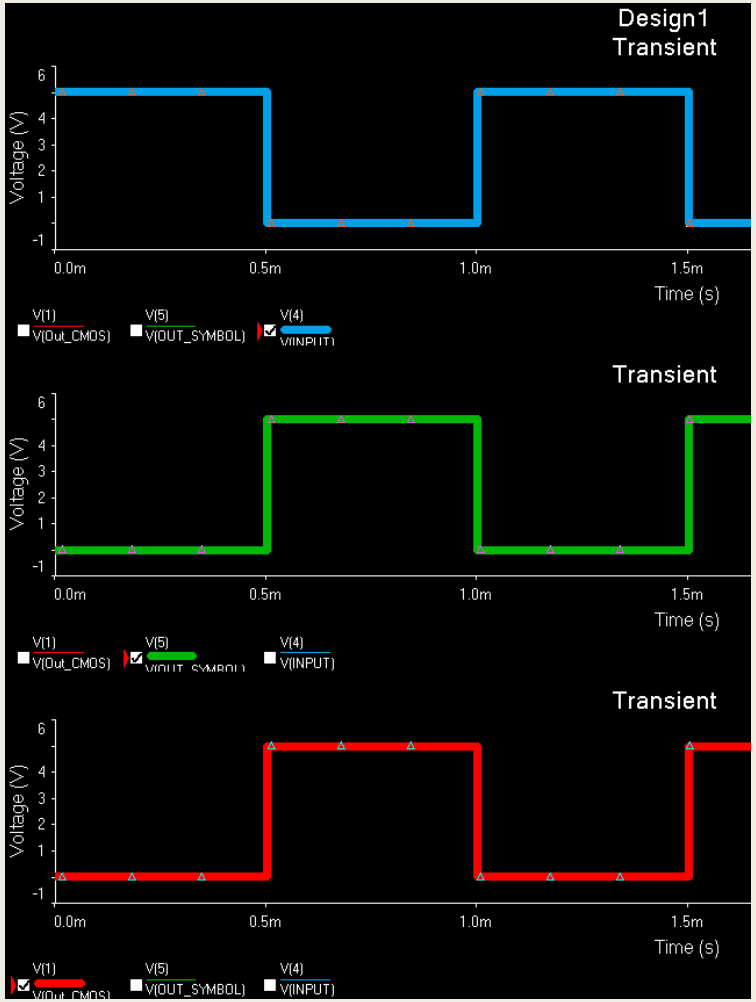




IN	OUT
A	Q
0	1
1	0

From MOSFETs to Logic Gate



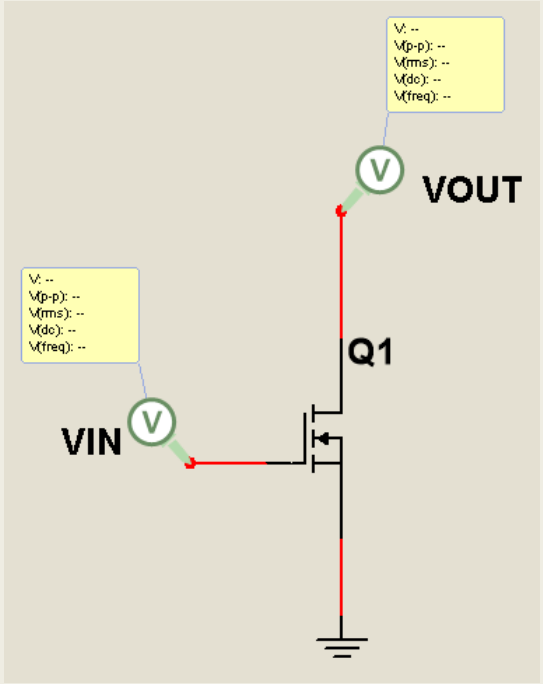


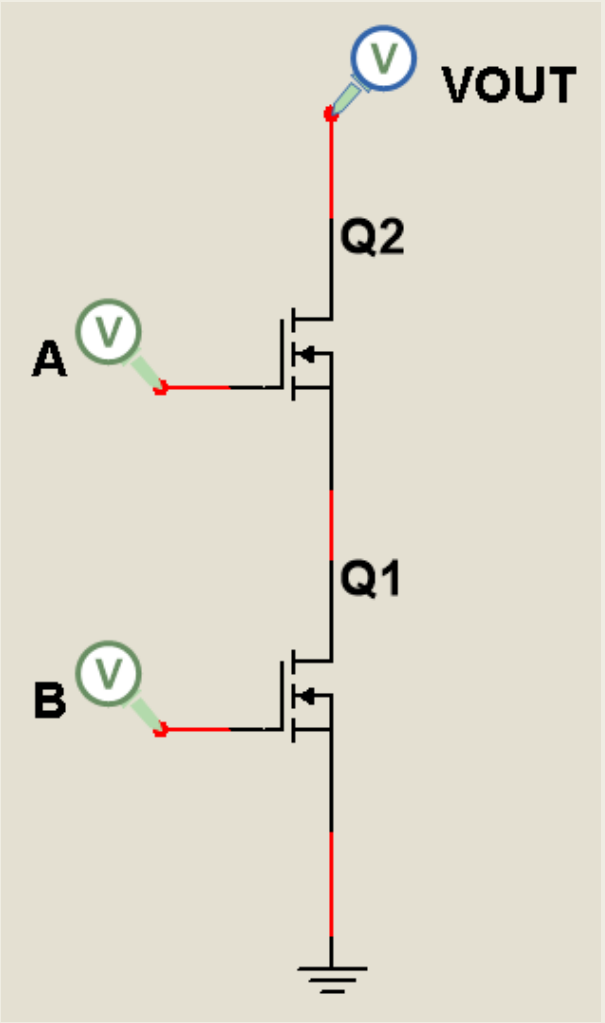
Pull-down NMOS in Logic Gates

Single NMOS,
if VIN=1, VOUT=0.

In series:

- When A=1 and B=1, VOUT =0.
- VOUT=(AB)’
- NAND??



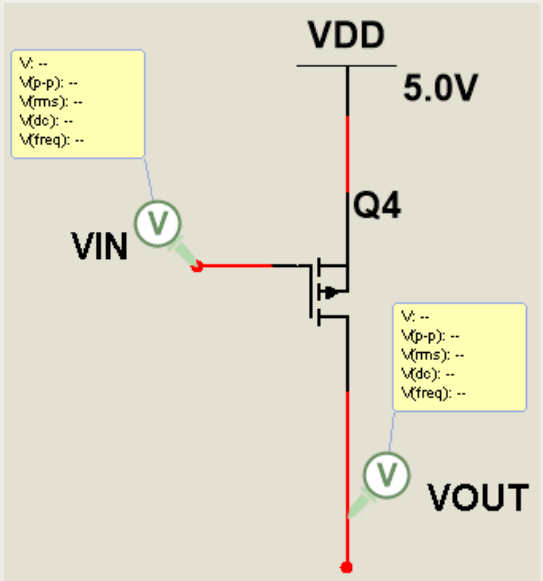


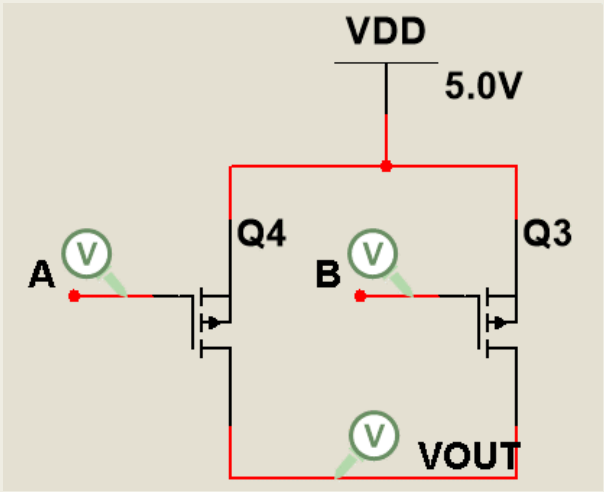
Pull-up PMOS in Logic Gates

Single PMOS
if VIN=0, VOUT=1.

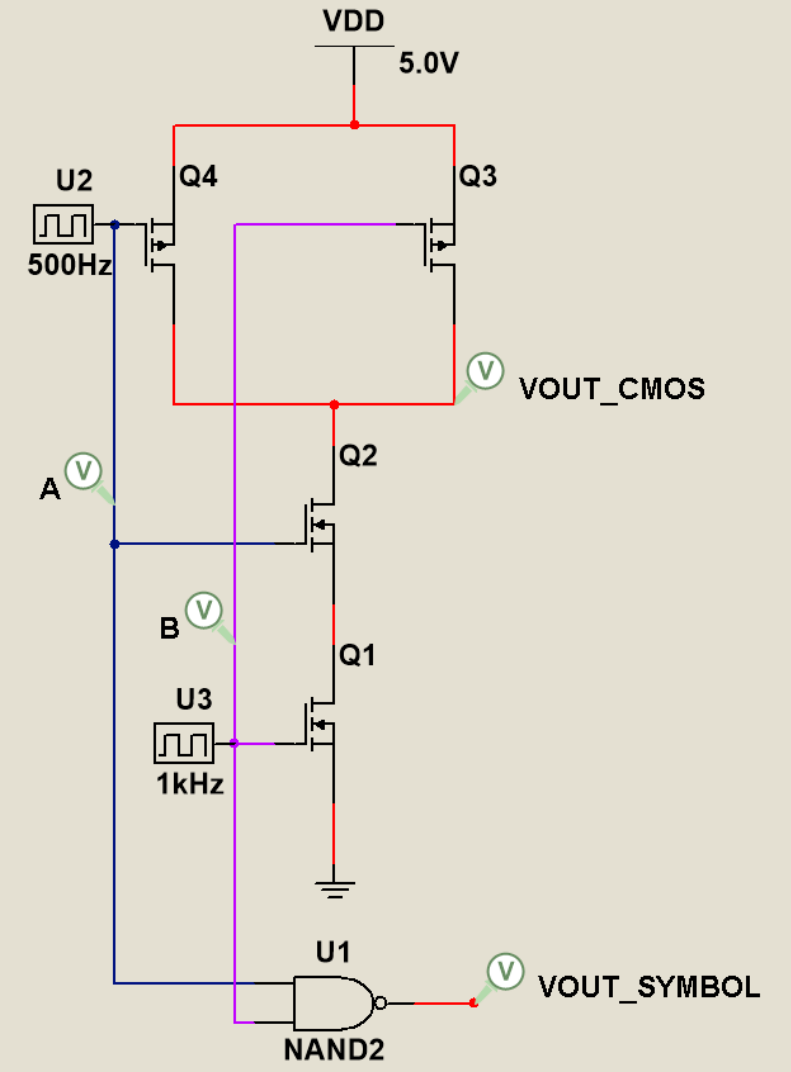
In parallel:

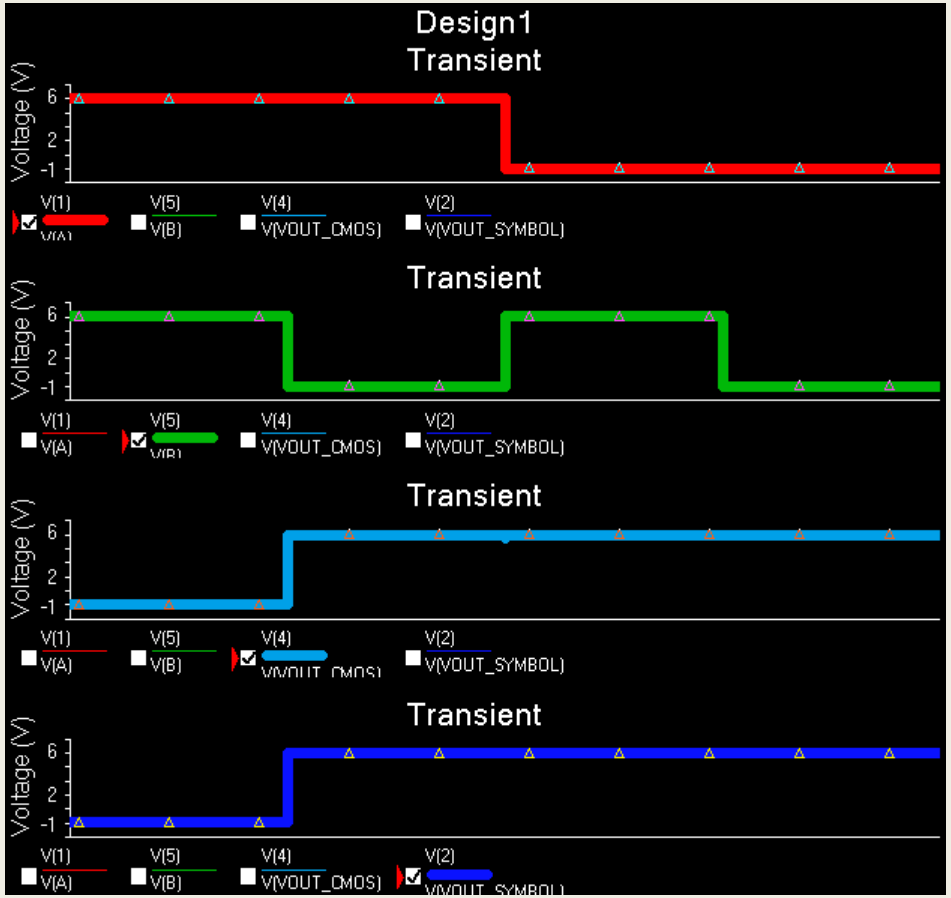
- When A=0 or B=0, VOUT =1.
- VOUT=A'+B'
- A'+B'=(AB)'
- Also NAND!





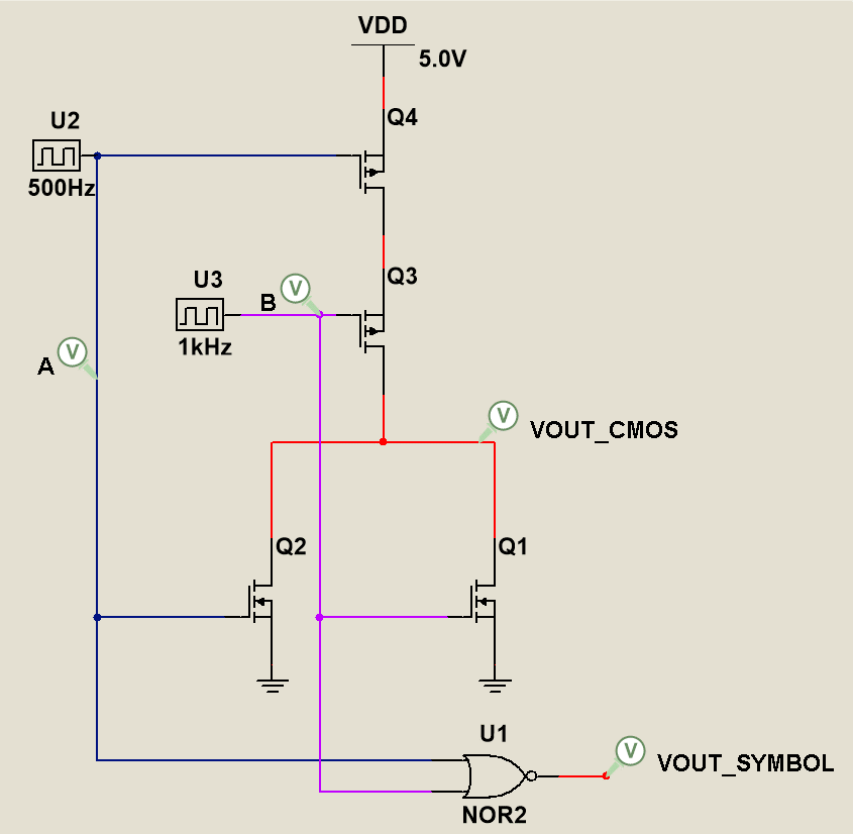
Full CMOS NAND Gate

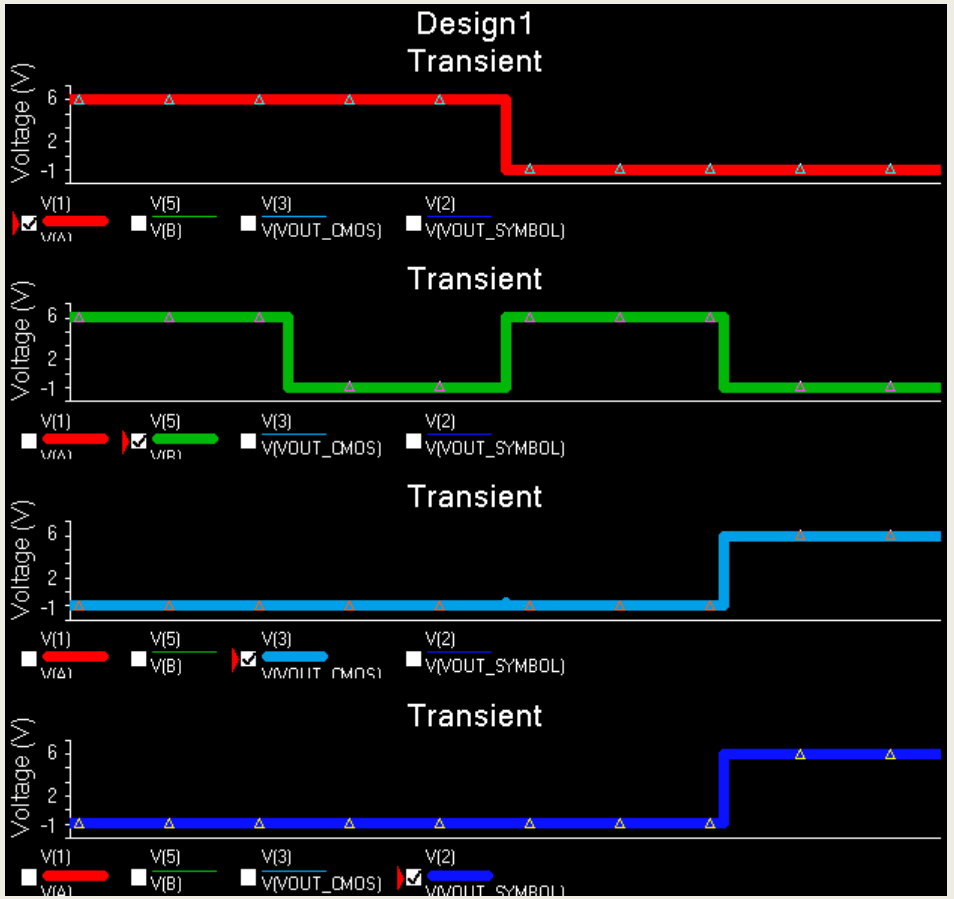




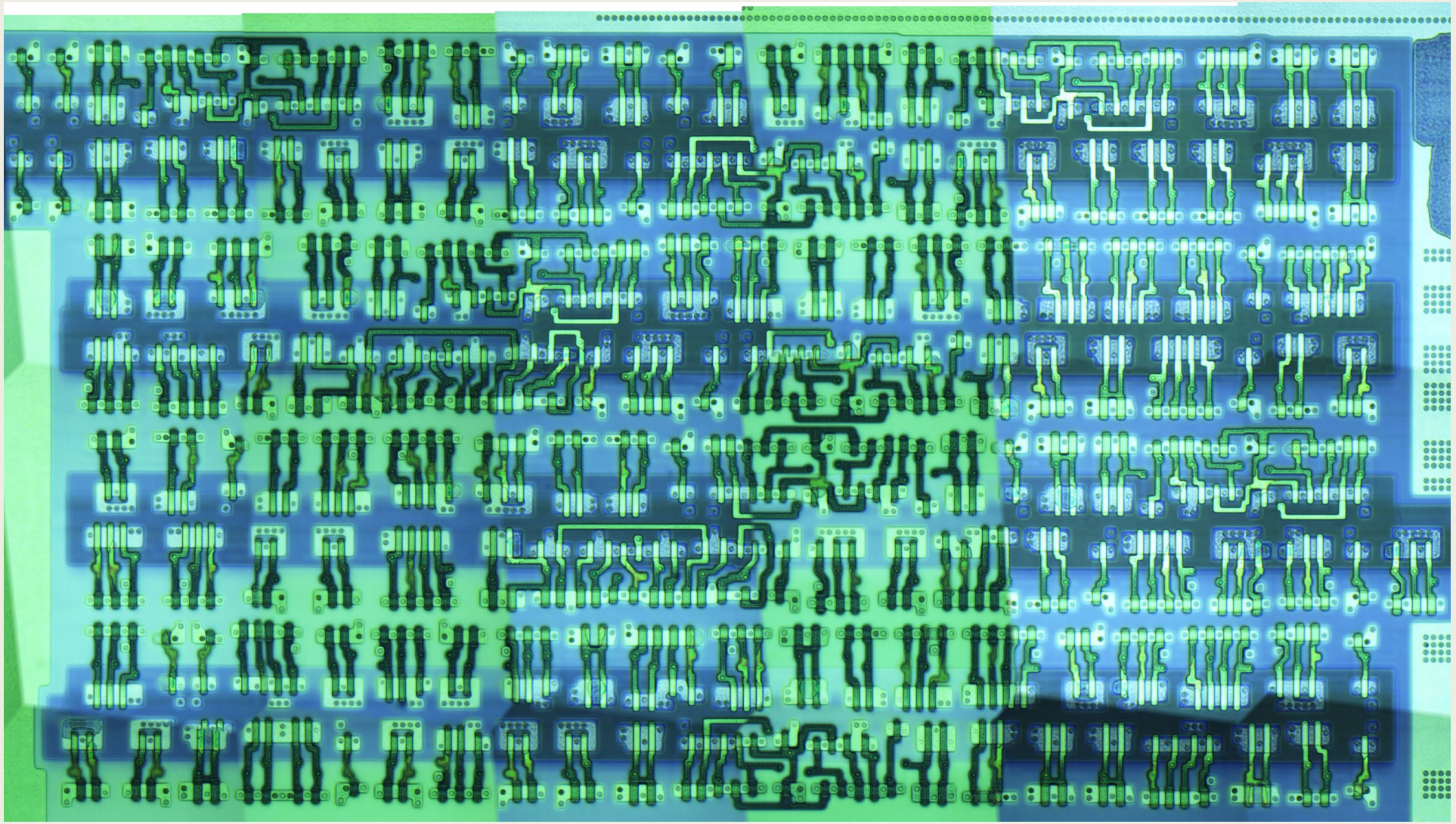
Full CMOS NOR Gate

- For NMOS, VOUT=(A+B)’ 👉 Parallel NMOS
- For PMOS, VOUT=(A+B)’=A’B’ 👉 Series PMOS





MOSFETs in Digital IC (0.18um)



Thanks!

Q&A