Problem Set #2, EE part

Issue date: Nov. 14, 2020; Deadline: 23:59, Nov. 22, 2020

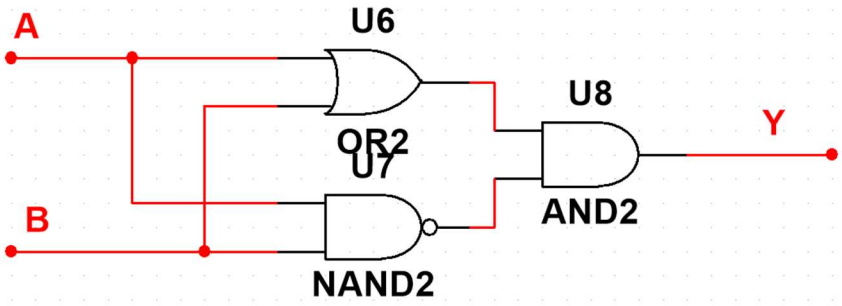
Student Name: _____ Student No.: _____

1. CMOS logic gate

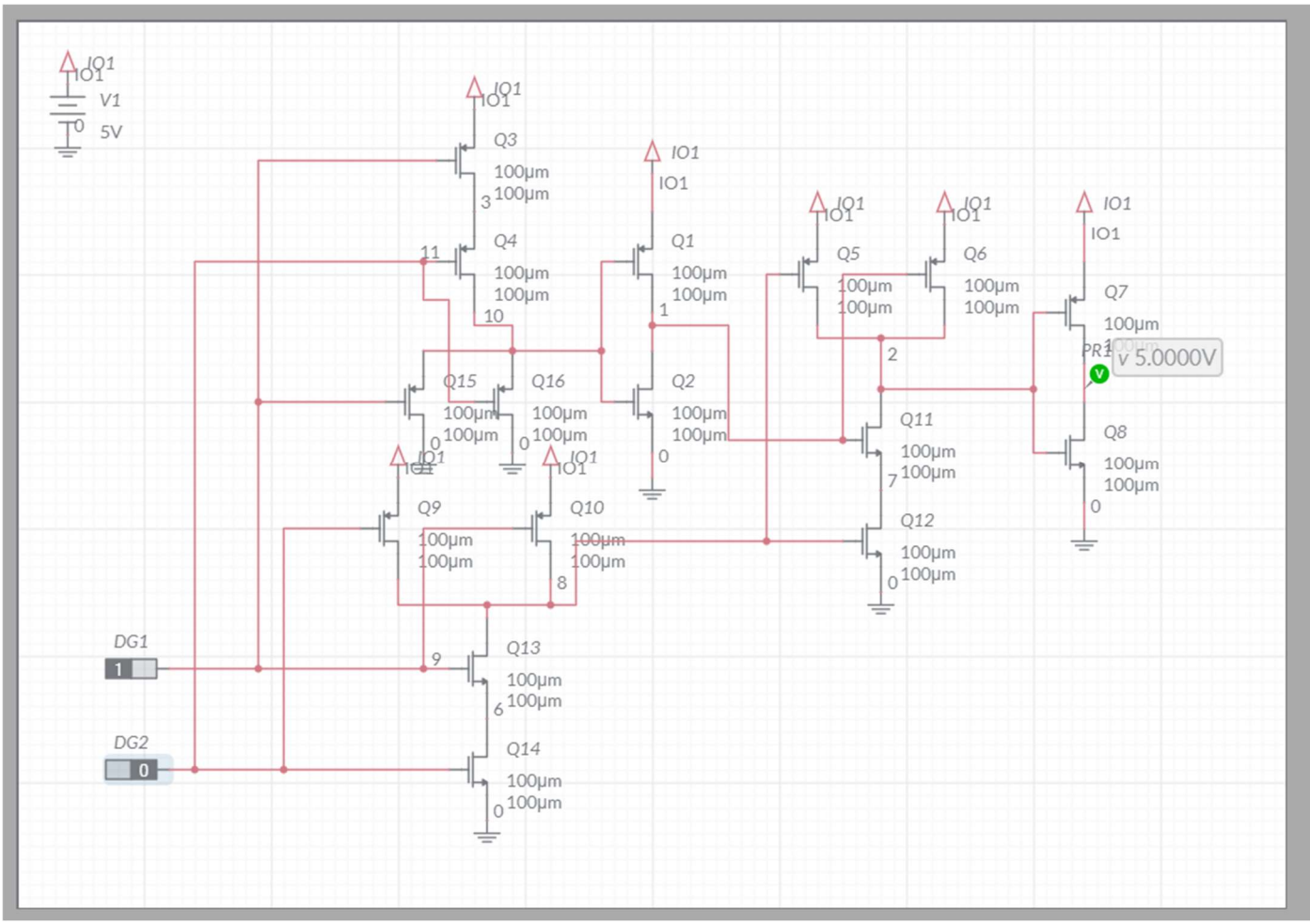
Use the fundamental CMOS logic circuit units, such as NOT, AND, OR, to build a XOR gate

- Truth table and logic circuit (gate level) design. (10')

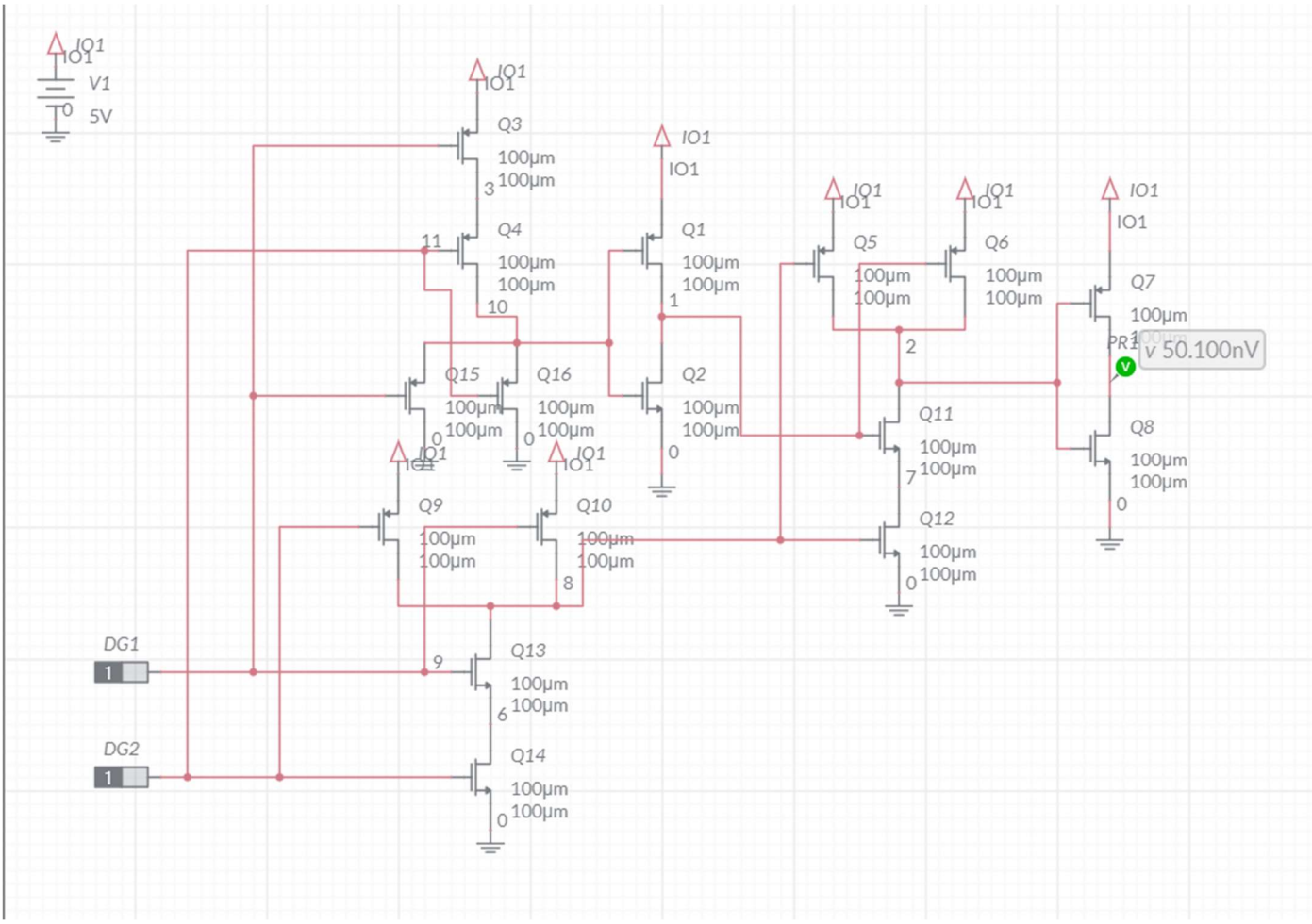
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

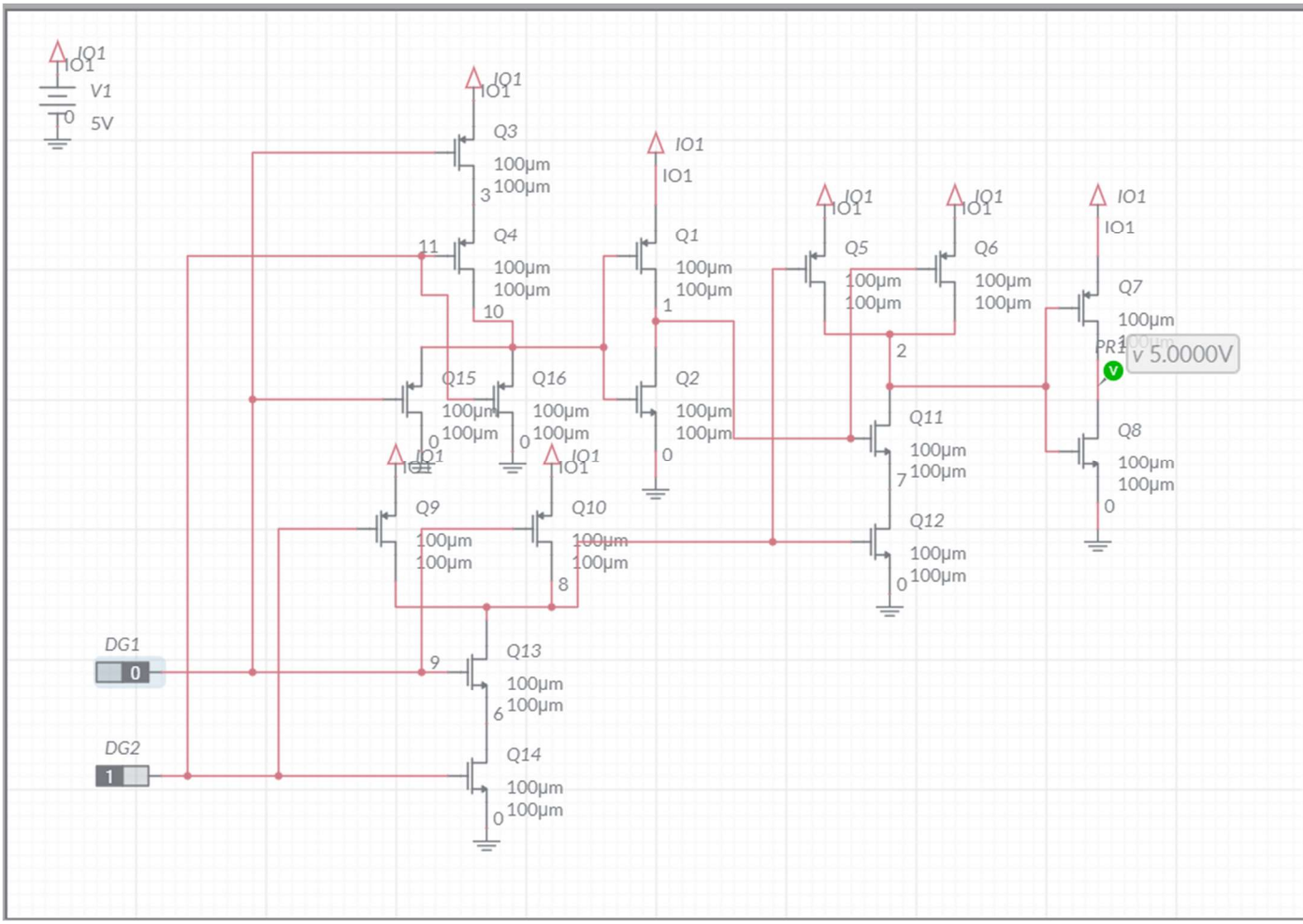


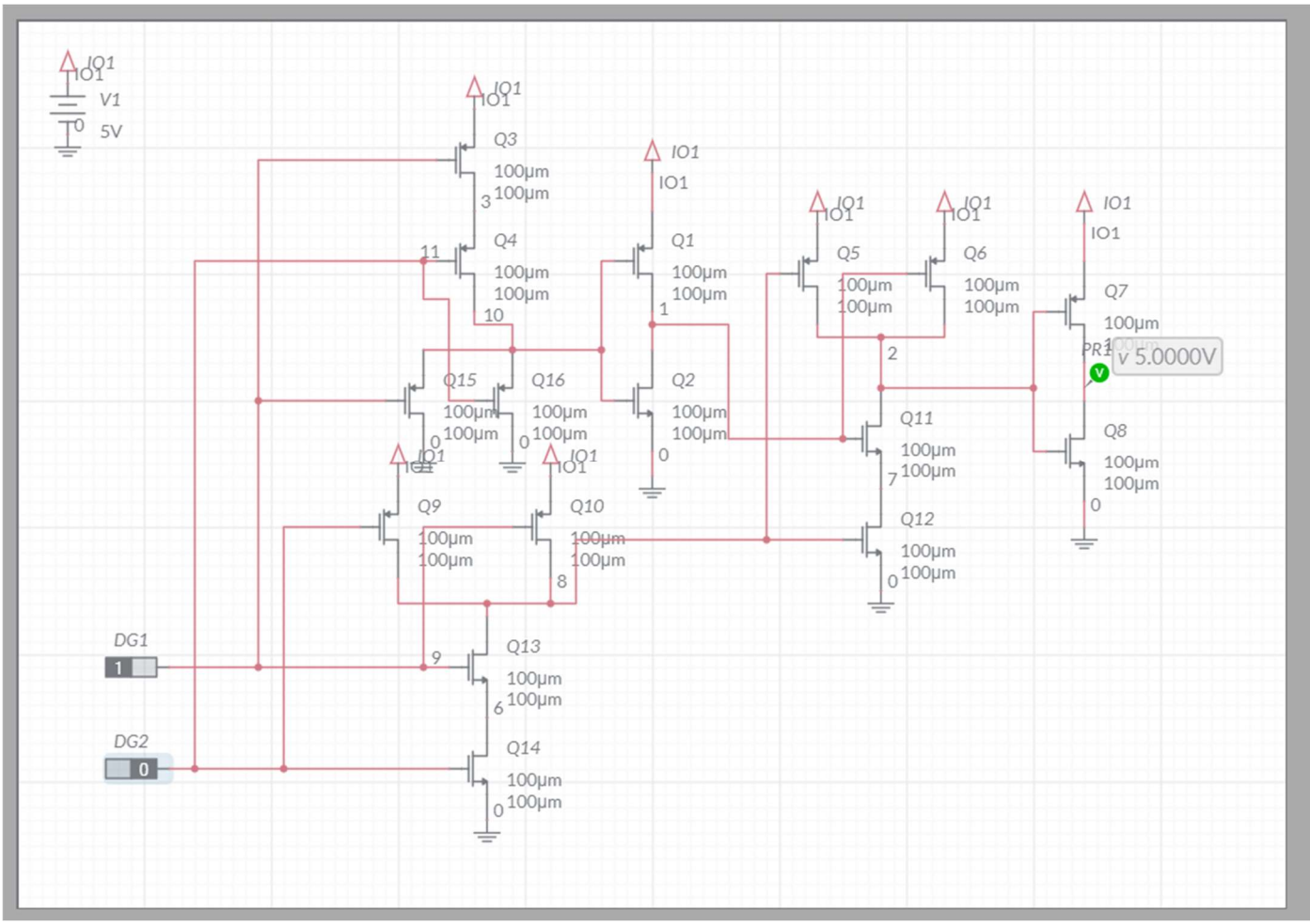
- CMOS-level implementation (15')



- Measurement results (5')


IO1
V1
0
5V
Q3
100µm
100µm
3
Q4
11
10
Q1
1
Q2
0
Q5
2
Q6
Q7
PR1
v 50.100nV
Q8
7
Q11
Q12
Q15
Q16
Q9
Q10
8
DG1
1
9
Q13
6
DG2
Q14


IO1
V1
0
5V
Q3
100µm
100µm
3
Q4
11
10
Q1
1
Q2
0
Q5
2
Q6
Q7
PR1
v 5.0000V
Q8
7
Q11
Q12
Q15
Q16
Q9
Q10
8
DG1
0
9
Q13
6
DG2
1
Q14



2. Combinational logic circuit exercises

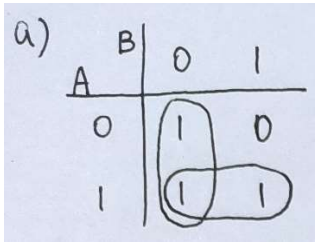
- Write the Boolean equations in sum-of-products canonical form for each of the truth tables (2' * 5)
  a) $Y = \overline{A}\,\overline{B} + A\overline{B} + AB$
  b) $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC$
  c) $Y = \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}C + \overline{A}BC + \overline{A}B\overline{C} + ABC$

d) $Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,\overline{B}\,C\,D + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,\overline{D} + A\,B\,C\,\overline{D}$

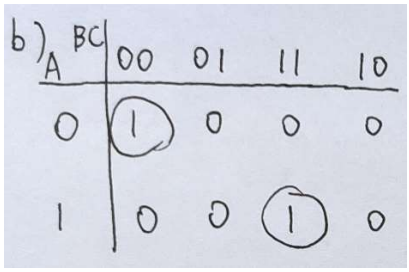
e) $Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,\overline{D} + A\,B\,\overline{C}\,\overline{D} + A\,B\,C\,D$

- Simplify the logic using the K-map (2' * 5)

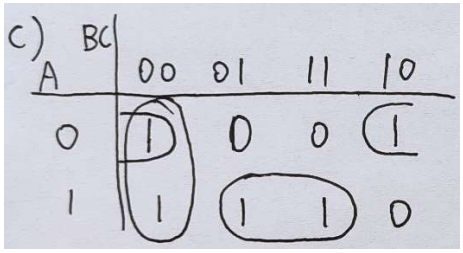
a) $Y = A + \overline{B}$



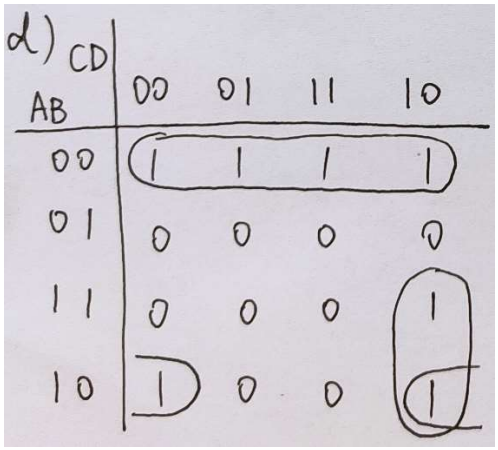
b) $Y = ABC + \overline{A}\,\overline{B}\,\overline{C}$



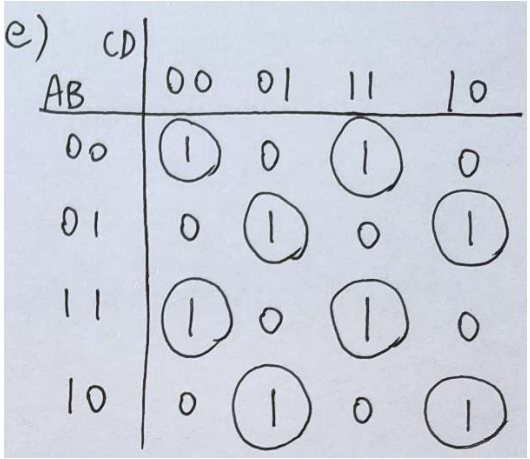
c) $Y = \overline{B}\,\overline{C} + AC + \overline{A}\,\overline{C}$



d) $Y = \overline{A}\,\overline{B} + AC\overline{D} + A\overline{B}\,\overline{D}$

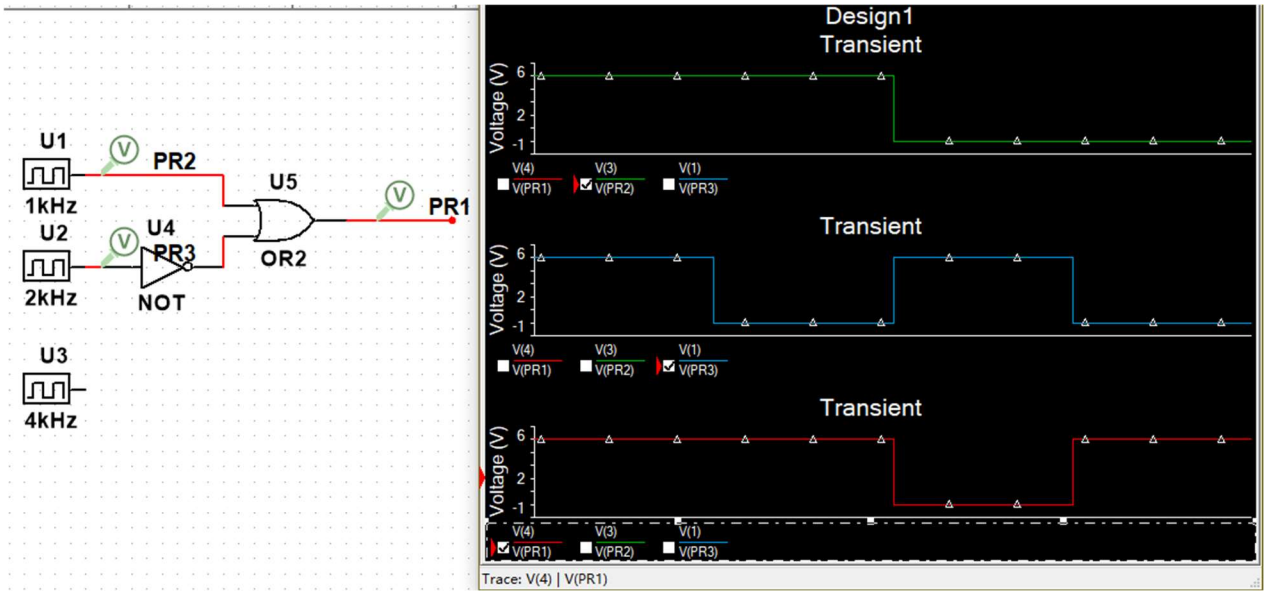


e) $Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,\overline{D} + A\,B\,\overline{C}\,\overline{D} + A\,B\,C\,D$

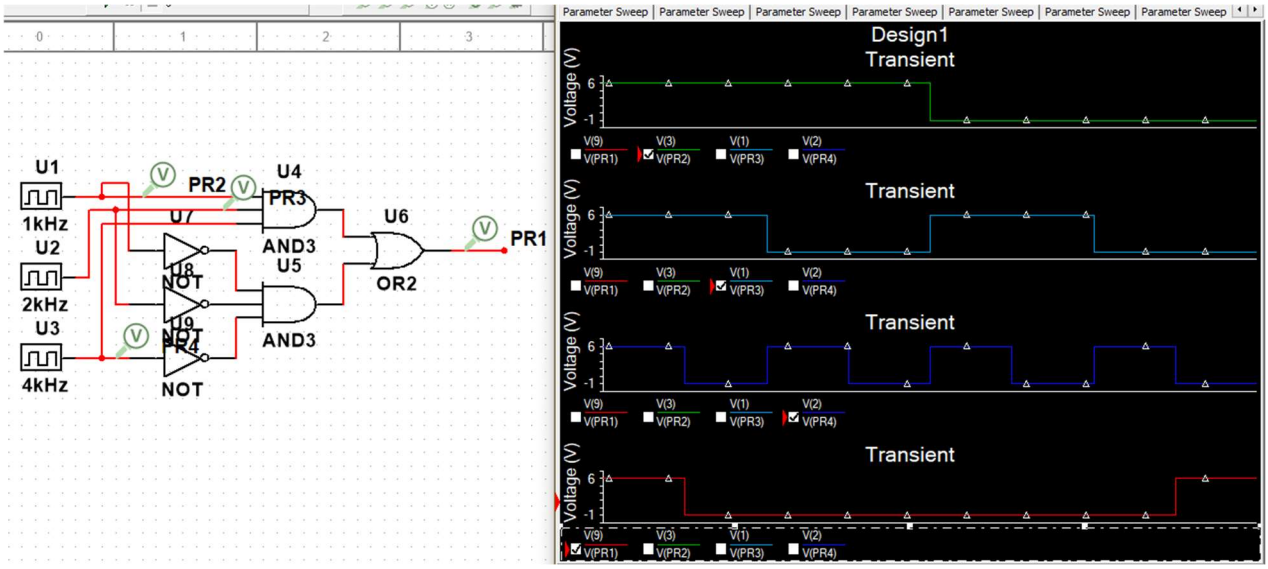


- Implement the circuits in Multisim and test their performance (2' * 5)

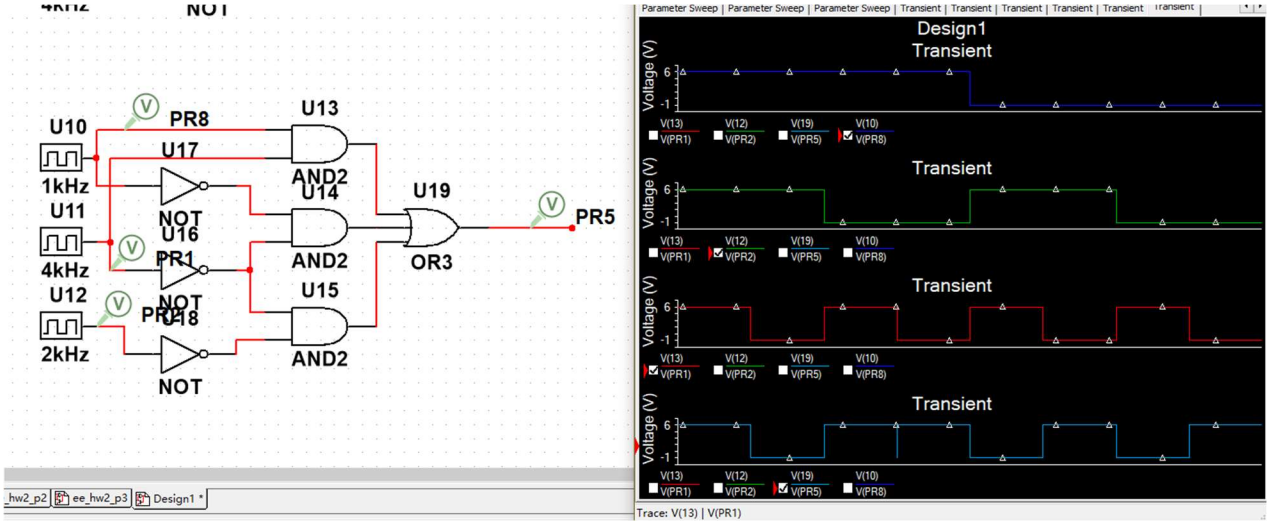
a)



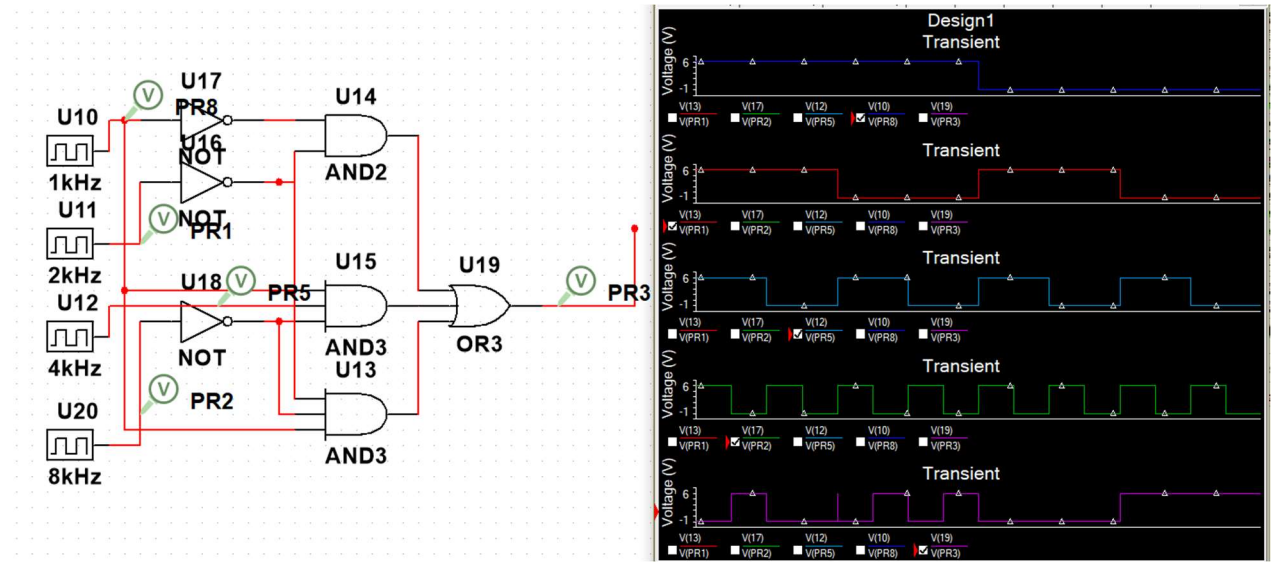
b)



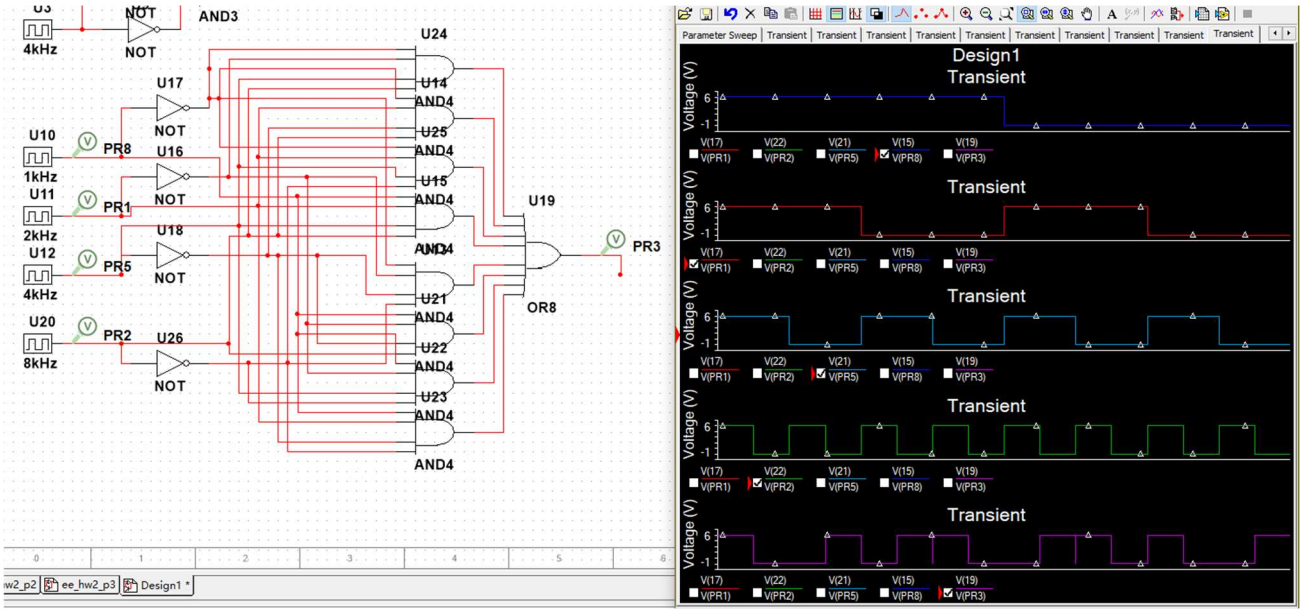
c)



d)



e)



(a)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

(b)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(c)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(d)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

(e)

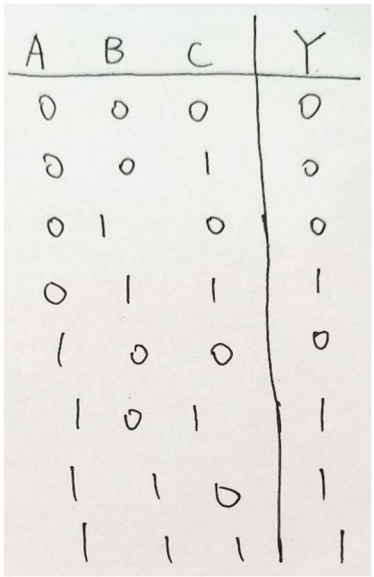
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

3. Majority voting and 14-segment alphabet display

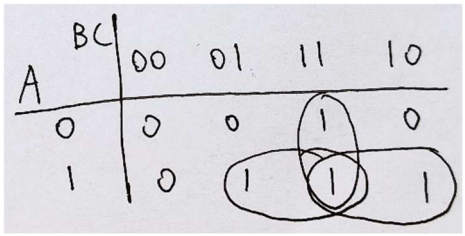
Referring to the majority voting system introduced in the lecture, design a logic circuit with Multisim and show the voting result with a 14-segment display as follows (T for Trump and B for Biden).

- Show the design procedures and final circuit schematic. (15')

1. Connect pin CA to Vcc.
2. Notice that for any display, LED [A J M] is **always on**. Connect them to GND.
3. When Biden wins, LED [B C G2 D] should be on. Since we use **common anode** alphanumeric display, we should have low input level for these pins.
4. According to 3, make the truth table. (1 for Trump and 0 for Biden)

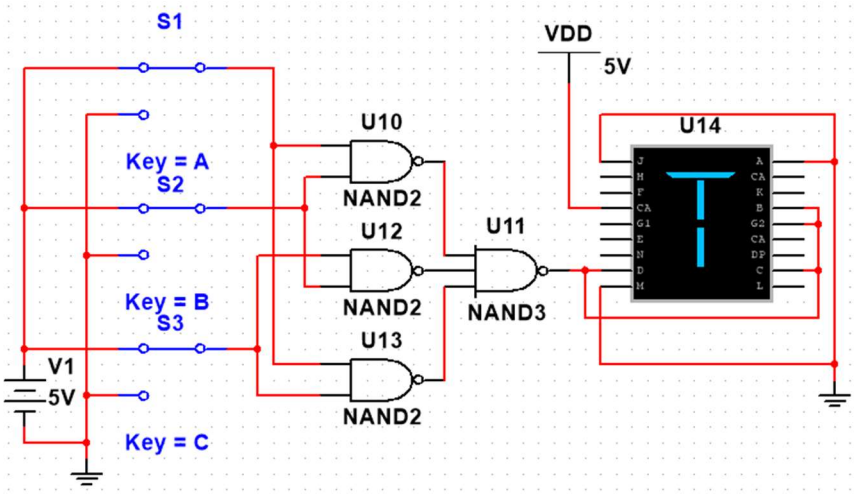


5. Use K-map to simplify.

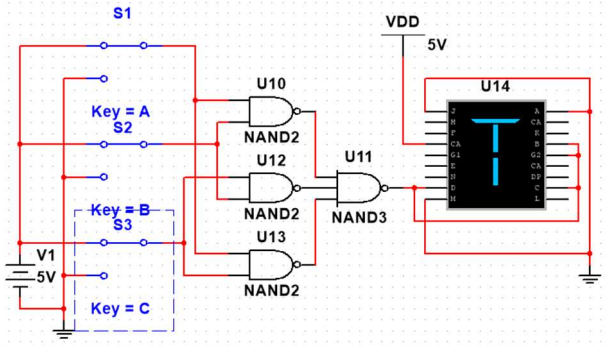


We got: $Y = AB + AC + BC = \overline{\overline{AB}\,\overline{BC}\,\overline{AC}}$

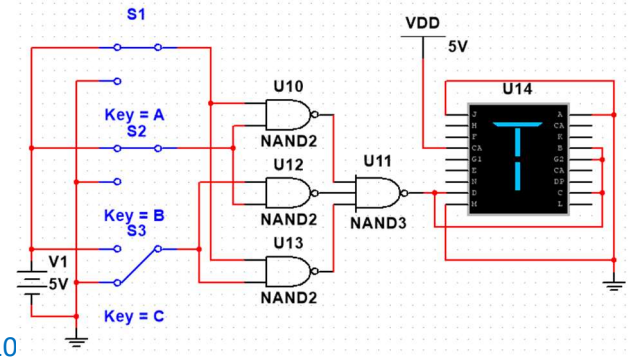
6. We have got the logic equation. Now create the circuit according to it.



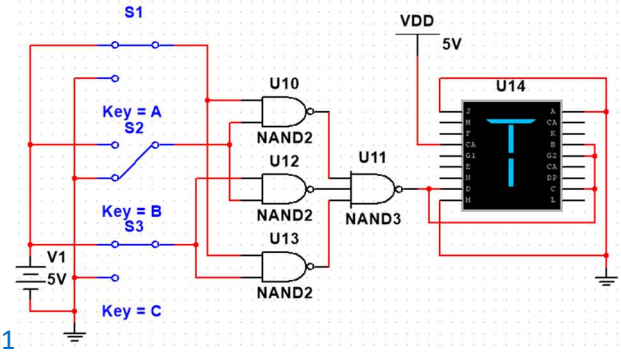
- Show the result pictures of six input conditions. (5')



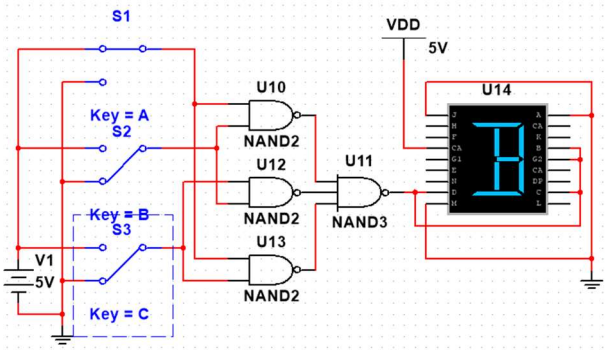
111



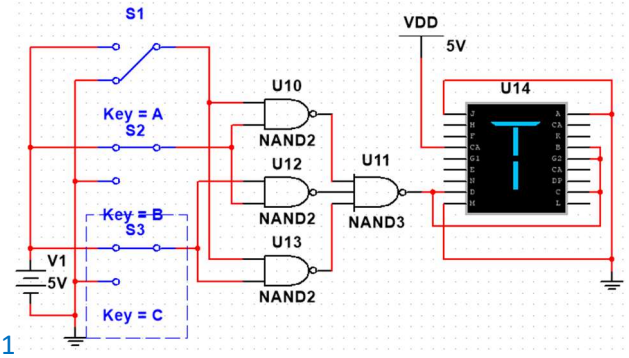
110



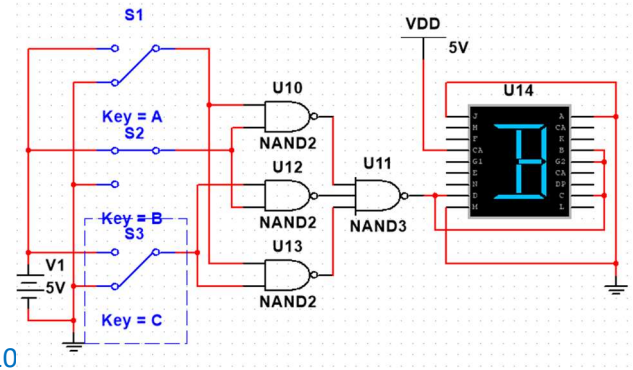
101



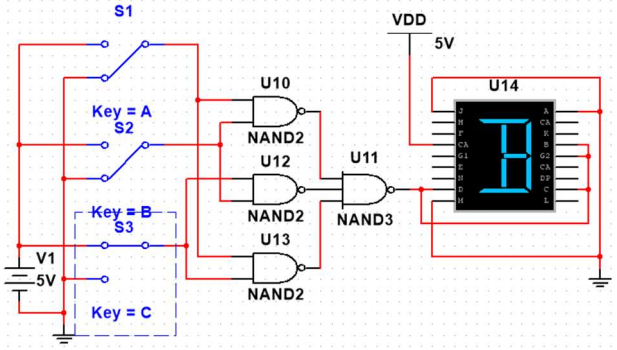
100



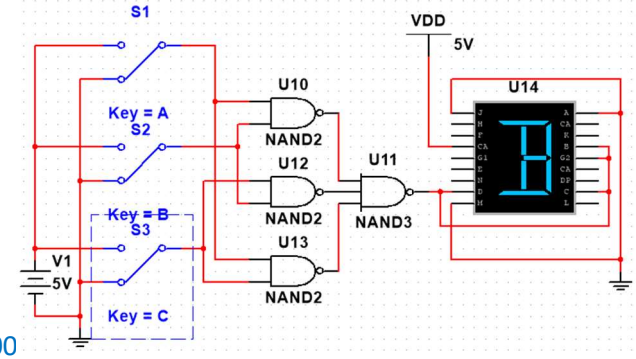
011



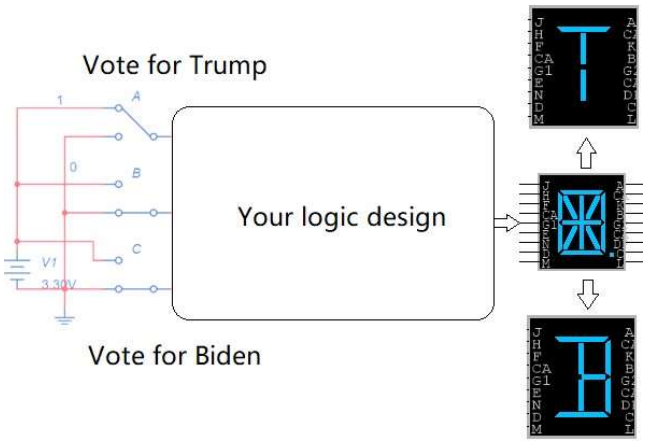
010



001

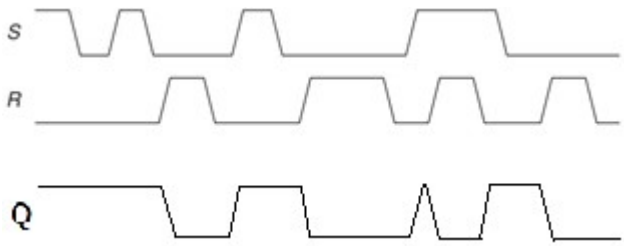


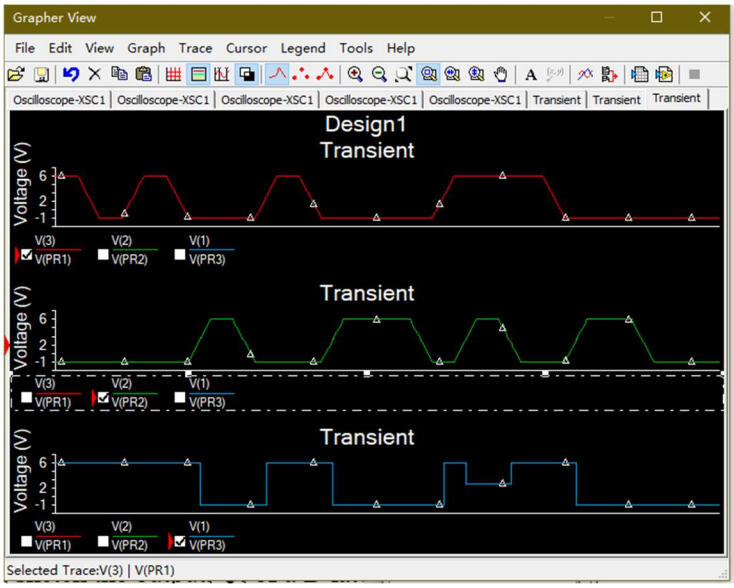
000

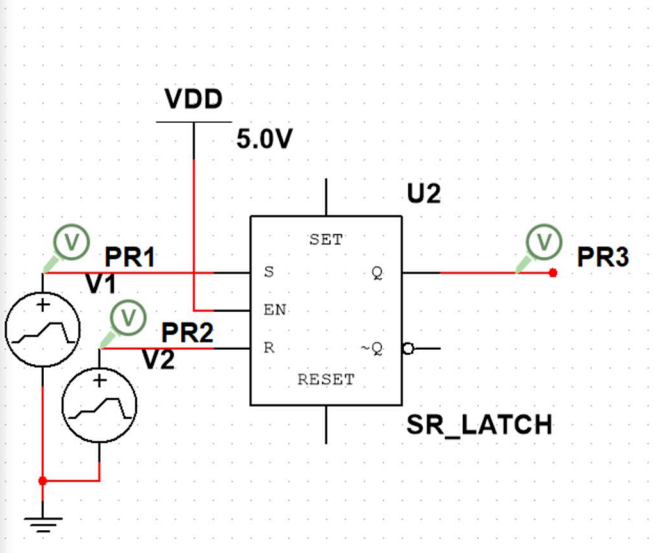


4. Sequential logic circuit exercises

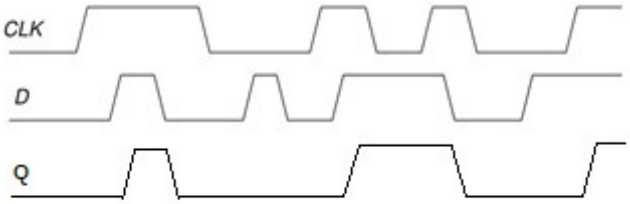
- Given the input waveforms shown in the following figure, sketch the output, Q, of an SR latch. Check it out with Multisim and show the schematic and simulation result. (10')

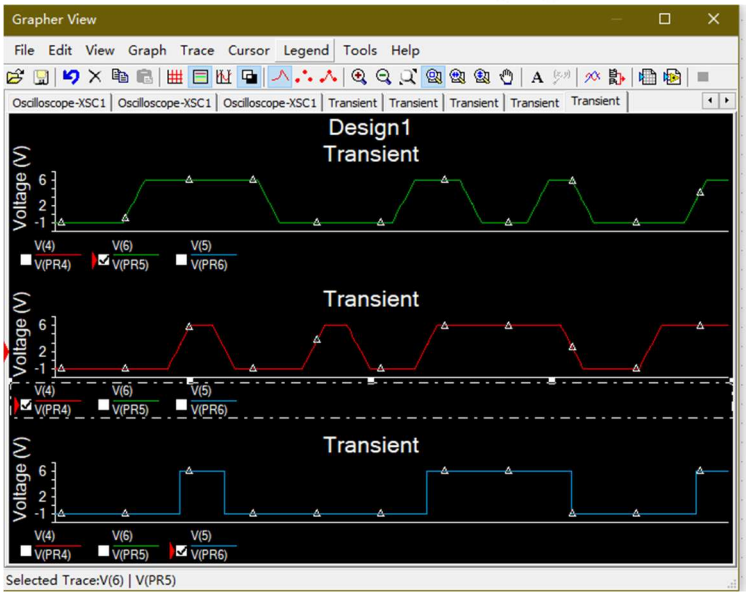


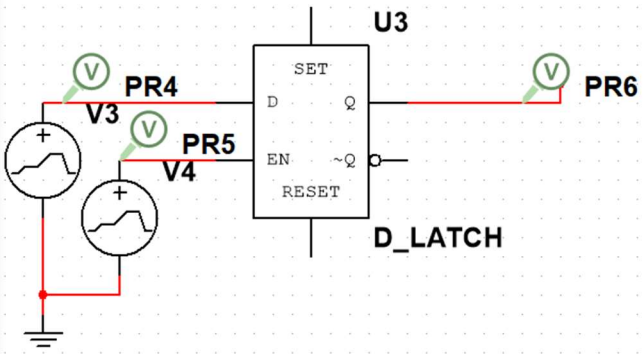




- Given the input waveforms shown in the following figure, sketch the output, Q, of a D latch. Check it out with Multisim and show the schematic and simulation result. (10')







** Please submit the softcopy of your solutions to the problems on gradescope.*

** All flow charts and codes should be enclosed in your solutions.*

** Discussion on methodology is allowed, yet, the assignment should be done individually. Plagiarism, once found, grades zero for the whole homework assignment!!*