SI100B: Introduction to Information Science and Technology Fall 2020

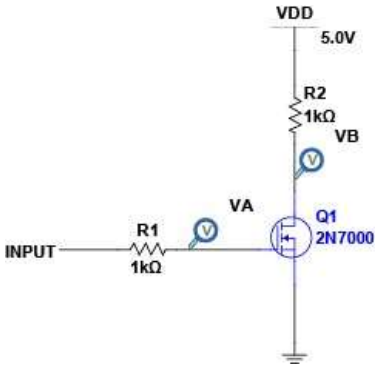
Problem Set #4, EE part

Issue date: Nov. 28, 2020; Deadline: 23:59, Dec. 6, 2020

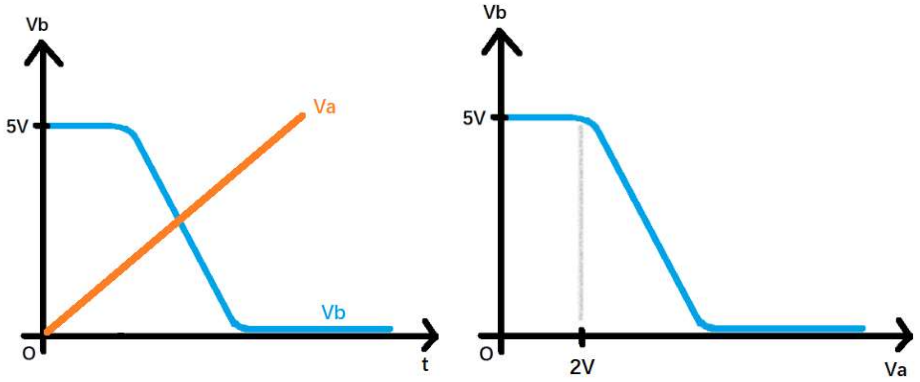
Student Name: _____ Student No.: _____

1. *Transistor circuit*

A MOSFET amplification circuit is given below. The datasheet of NMOS 2N7000 can be found here: https://www.onsemi.com/pub/Collateral/2N7000-D.PDF



- If the input voltage rises from 0 to 5V very slowly, please guess and sketch the waveform of V_A and V_B, and explain the reason (For example, why does the output voltage change when the input voltage reaches a certain value). (10')



- Qualitative analysis:

  When Vgs reaches gate threshold voltage, the channel between two P-type area (D and S) opens.

  Then currents I_{ds} (or IB) begin to flow through the channel.

  For the 1kΩ resistor R_2 , $U_2 = I_{ds} \cdot R_2$. $V_B = VDD - U_2$.

  So VB will begin to decrease.

  After input reaching a certain value, the channel is saturation.

  So VB will decrease to the voltage drop of NMOS (饱和时 DS 间压降) and almost remain the same.

- Quantitative analysis (based on datasheet):

  According to the datasheet of 2N7000, the typical value of threshold voltage is 2.1V.

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
Part Number	$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)	$V_{GS(th)}$ (V)	I_D (A)
2N7000	60	5 @ V_{GS} = 10 V	0.8 to 3	0.2
2N7002		7.5 @ V_{GS} = 10 V	1 to 2.5	0.115
VQ1000J		5.5 @ V_{GS} = 10 V	0.8 to 2.5	0.225
VQ1000P		5.5 @ V_{GS} = 10 V	0.8 to 2.5	0.225
BS170		5 @ V_{GS} = 10 V	0.8 to 3	0.5

FEATURES
- Low On-Resistance: 2.5 Ω
- Low Threshold: 2.1 V
- Low Input Capacitance: 22 pF
- Fast Switching Speed: 7 ns
- Low Input and Output Leakage

BENEFITS
- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

APPLICATIONS
- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

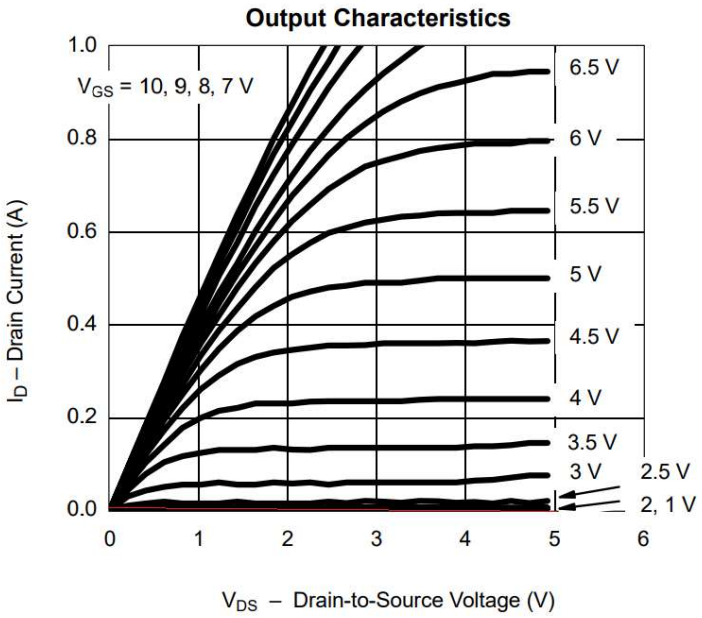
When the input is between 0v and 2.1v, the MOS is in cut-off region, namely the channel between DS is closed, then $I_{ds} \approx 0$. The MOS can be seen as open circuit, then $VB = 5$V.

When the input reaches 5V, the channel between two P-type area (D and S) opens.

Then currents I_{ds} (or IB) begin to flow through the channel.

For the 1kΩ resistor R_2 , $U_2 = I_{ds} \cdot R_2$. $V_B = VDD - U_2$.

So VB will begin to decrease until reaches the voltage drop of NMOS (饱和时 DS 间压降).

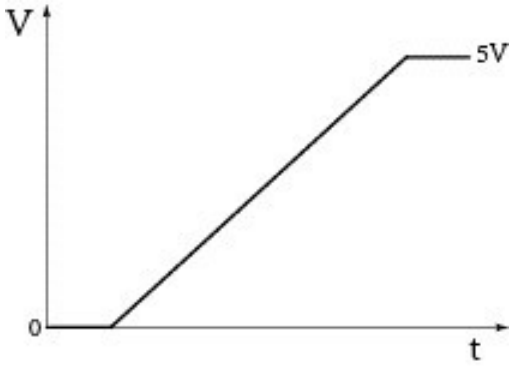


Overlay the characteristic of the 1kΩ resistor R_2 to the plot given in datasheet (red line on the graph above).

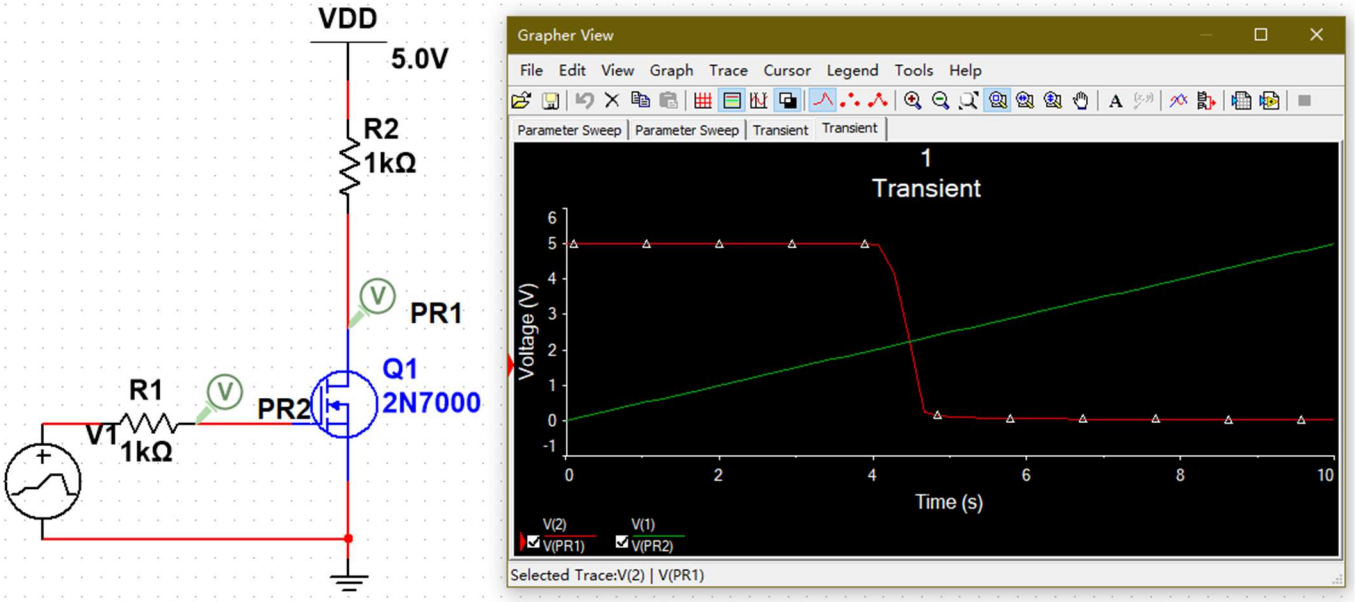
Then VB $= VDD - V_{DS}$ is the x value of the intersection point.

We can know that when the V_{gs} reaches about 2.5V, VB approaches about 0.

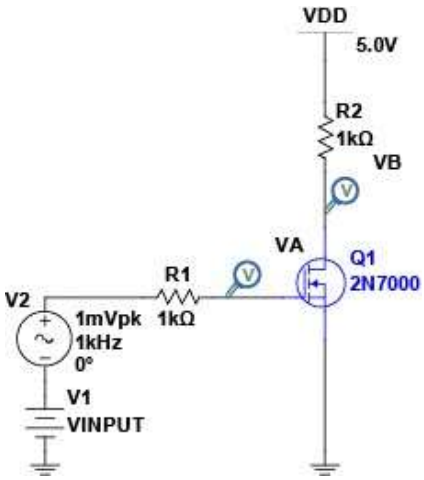
(Limited to the number of V_{gs} given on datasheet, the result in rather inaccurate.)



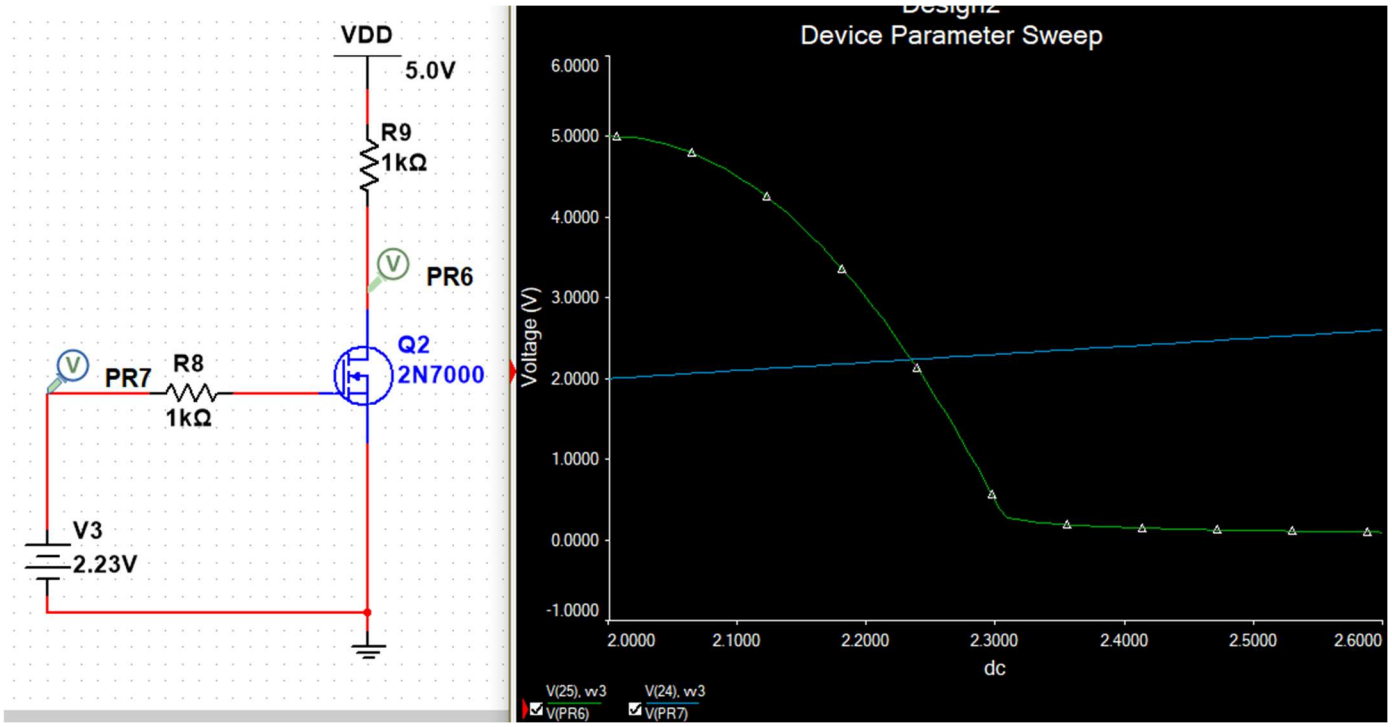
- Build the circuit in Multisim, use 'DC sweep' or 'transient' simulation to validate your guess. (10')
  Use a Piecewise Linear Voltage whose input waveform is $V = 0.5t$.



- Find the input value, when $V_B \approx 2.5V$ based on your result in the last question. Then apply an AC voltage (1mV peak voltage) on the DC input. Find the output waveform of V_B, and calculate the voltage gain (neglecting the DC offset, only consider the AC) of this circuit based on your simulation data. (10')

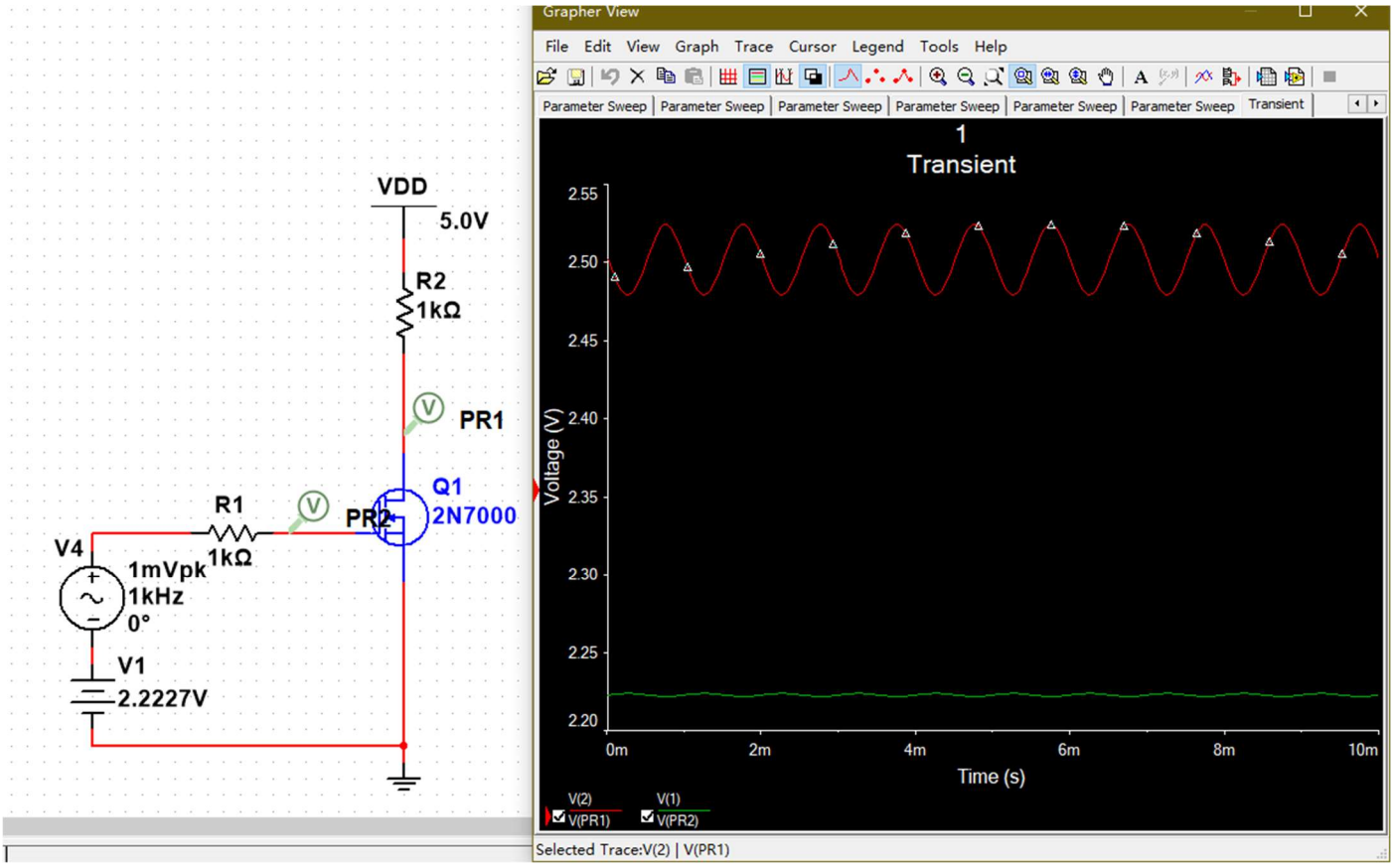


Do Parameter sweep on V_{input}.



According to the graph, the input is about 2.223V.

After applying the AC voltage, the waveform of VB is

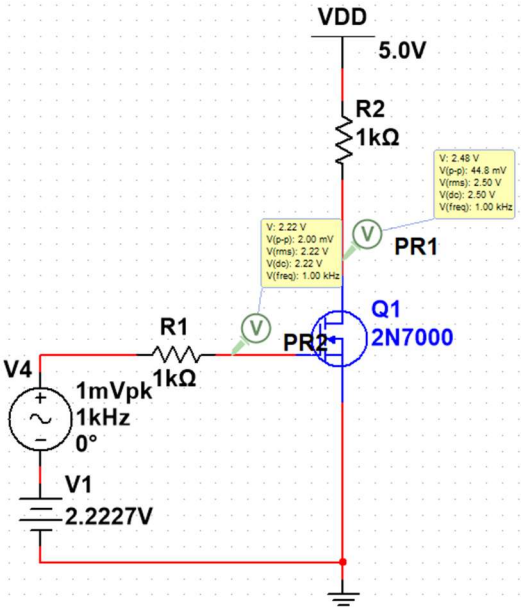


To calculate the gain, just compare the amplitude of the AC components (交流成分的振幅 翻译可能不太对 见谅) of VA and VB.

From both the transient graphic above and the voltage parameter value V_{p-p} below, we can know that the gain

$$Gain = \frac{A_A}{A_B} = 22.4$$

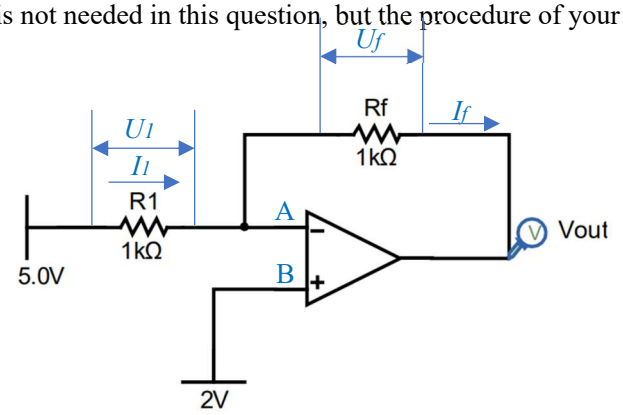
In which A represents amplitude.



2. *Operational amplifier*

Virtual ground is an important method to analyze the circuits with operational amplifiers. (link: https://baike.baidu.com/item/虚短). Based on the method of virtual ground, please analyze the output voltage of following circuits. Simulation is not needed in this question, but the procedure of your calculation is necessary.

- Circuit #1 (15')



First, use the virtual ground method. We have $V_A = V_B = 2\text{V}$.

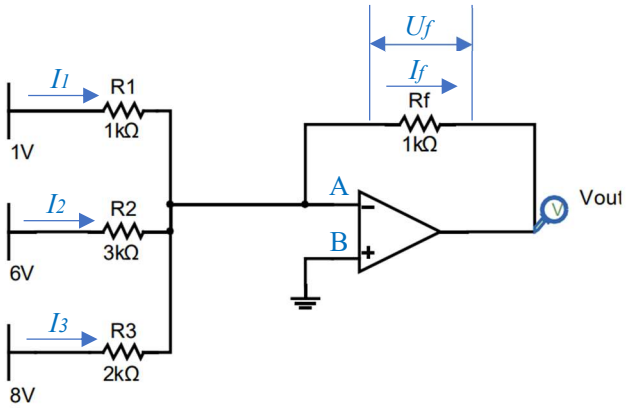
Then calculate circuit through R1 (I_1). We have $I_1 = \frac{U_1}{R_1} = \frac{V_{input} - V_A}{R_1} = 3\text{mA}$.

From the characteristic of operational amplifier (虚断) , we have $I_A = 0$. Then $I_f = I_1$.

$U_f = I_f \cdot R_f = 3\text{V}$.

So finally, $V_{OUT} = V_A - U_f = -1\text{V}$.

- Circuit #2 (15')



Actually, this is a summing amplifier circuit.

First, use the virtual ground method. We have $V_A = V_B = 0\text{V}$.

Then calculate circuit through R1. We have $I_1 = \frac{U_1}{R_1} = \frac{V_{input} - V_A}{R_1} = 1\text{mA}$.

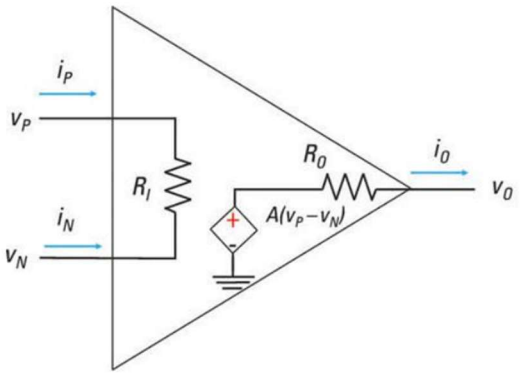
The same, we have $I_2 = 2\text{mA}$, $I_3 = 4\text{mA}$.

From the characteristic of operational amplifier (虚断) , we have $I_A = 0$.

So $I_f = I_1 + I_2 + I_3 = 7\text{mA}$. $U_f = I_f \cdot R_f = 7\text{V}$.

So finally, $V_{OUT} = V_A - U_f = -7\text{V}$.

- Bonus



Consider the equivalent circuit of the ideal amplifier.

Let

$$v_d = v_p - v_n .$$

We have the basic relation

$$v_0 = A(v_p - v_n) = Av_d .$$

From the characteristic of amplifier, we have

$$A \to \infty$$

$$R_i \to \infty$$

$$R_o \to 0$$

The output v_o is finite.

Thus $v_d = \frac{v_o}{A} \to 0$.

Namely $(v_p - v_n) \to 0$.

Thus, the two input can be seen as short circuited.

If v_p is connected to GND, then input v_n can be seen as virtual ground.

3. *Analog-to-digital converter (ADC)*

- Build a 2-bit flash analog-to-digital converter (ADC) in Multisim, the function should confirm to the rule in the following table. Please write down your procedures of design, including your design thought, the simplifications of digital circuit, and the final simulation. (40')

Input voltage	digital output
0<Vin<1	11
1<Vin<2	10
2<Vin<3	01
3<Vin<4	00

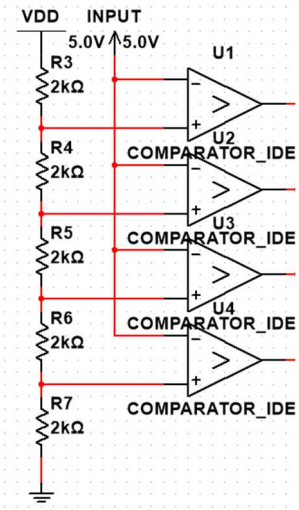
Hints: 1. The ADC example can be found in the slides of lecture #6. 2. Ideal comparator can be found in Analog/ANALOG_VIRTUAL/COMPARATOR_IDEAL

First, build the basic part of ADC -- Input Quantization of the circuit.

Since we need a 2-bit ADC, 4 comparators are required.

According to the table, the reference voltage is 1V, 2V, 3V and 4V.

Thus, we select a 5V VDD and 5 resistors of same value to obtain the reference voltage.



Then consider the logical part.

Mark the digital output as $S_{1:0}$, mark the four output of comparators as $Z_{0:3}$ (from below to above).

Then we have truth table.

Input	Z0	Z1	Z2	Z3	S0	S1
0v~1V	1	1	1	1	1	1
1v~2V	0	1	1	1	1	0
2v~3V	0	0	1	1	0	1
3v~4V	0	0	0	1	0	0
>4V	0	0	0	0	N/A	N/A

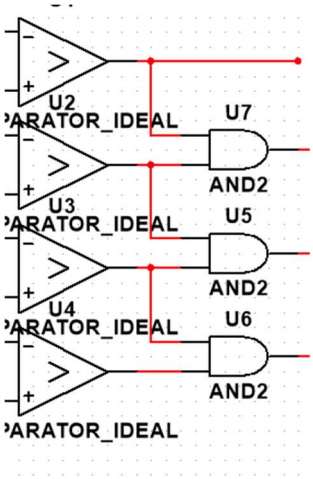
Then we can get logic equations:

$$S_0 = Z_1$$

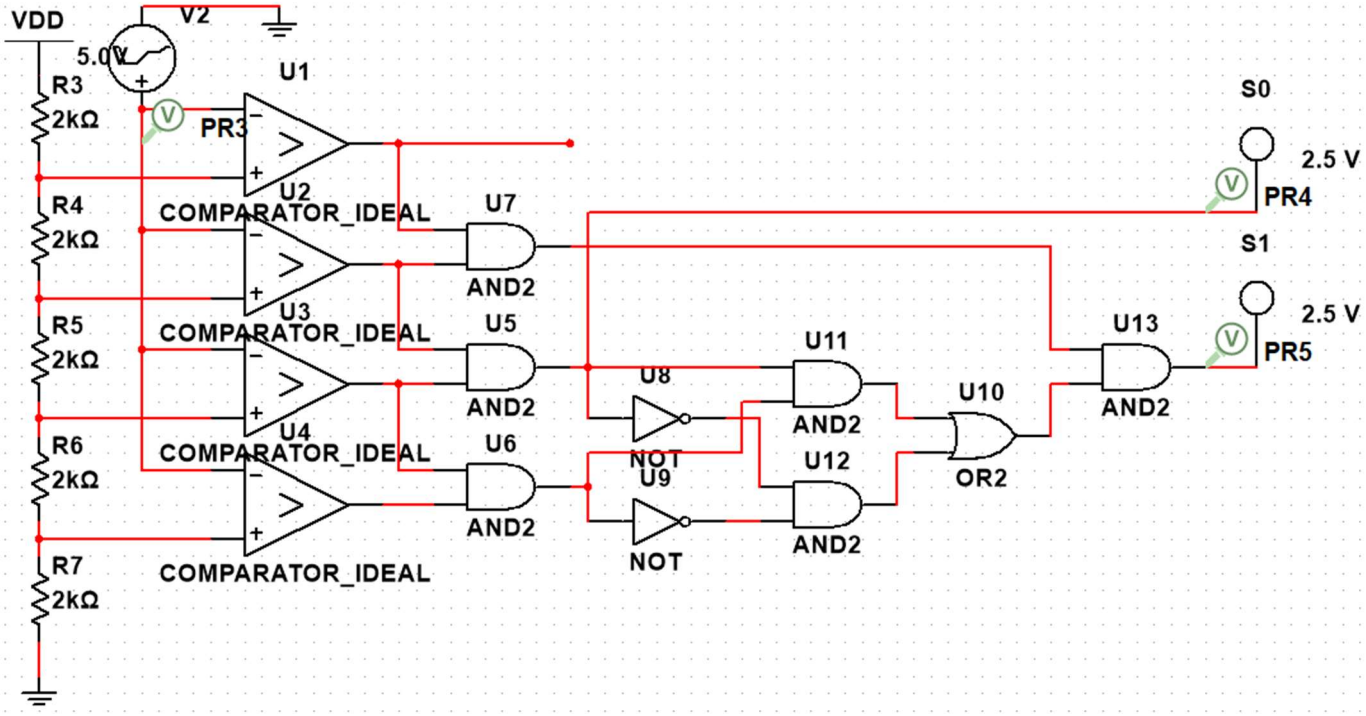
$$S_1 = Z_2 Z_0 Z_1 + Z_2 \overline{Z_1}\,\overline{Z_0}$$

Before building the digital encoding part circuit, we should add bubble error correction part to avoid unexpected errors (For example, a comparator which should output low voltage may wrongly give high output due to voltage fluctuation).

In this case, we add AND gates for Z_n and Z_{n+1} for output Z_n to avoid unexpected 1 output which should be 0 instead.

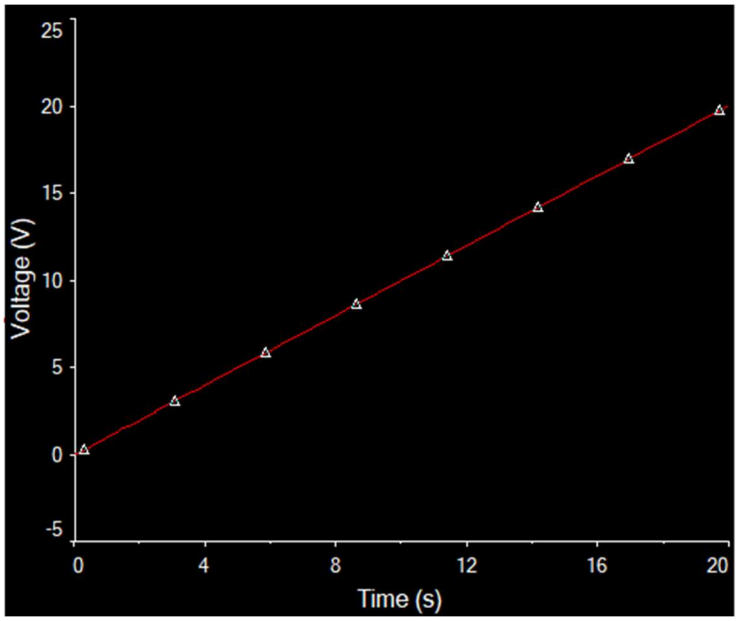


Finally, we can build the digital encoding part according to the logical equations.

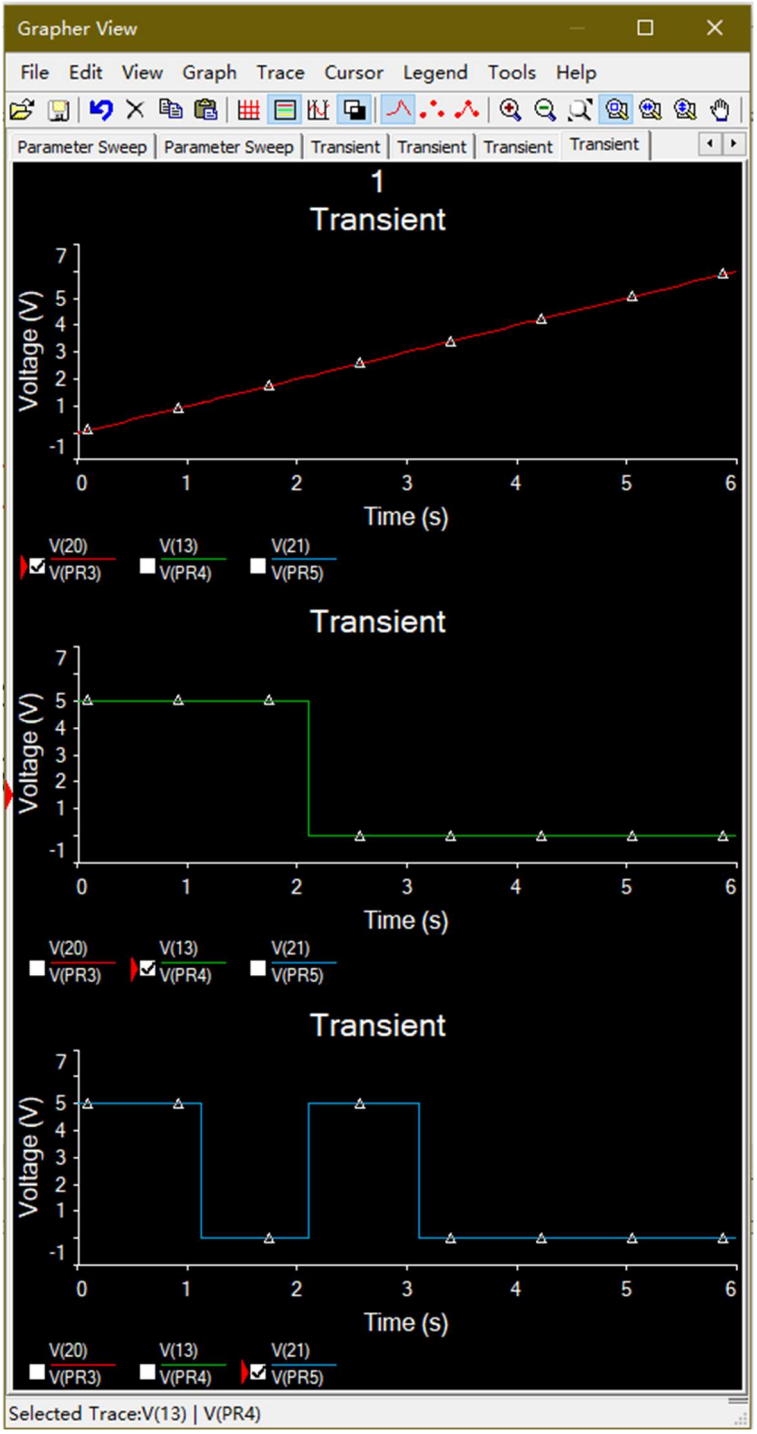


Use a Piecewise Linear Voltage as input whose waveform is as below:

$$V = t$$



Use Transient to simulate and test the circuit.



** Please submit the softcopy of your solutions to the problems on gradescope.*

** All flow charts and codes should be enclosed in your solutions.*

** Discussion on methodology is allowed, yet, the assignment should be done individually. Plagiarism, once found, grades zero for the whole homework assignment!*