Design of a Digital Baseband Processor for UWB Transceiver on RFID Tag

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Abstract— **In this paper we present a novel digital baseband processor designed for UWB transceiver on RFID tag. It is a low power and low voltage (1.8V) full digital ASIC which is implemented in 0.18 μ m CMOS technology. The processor receives serial signals (consist of data and commands) from the RF Receiver, and based on received command carries out various functions such as receive data and write to the memory, compare data, send data, set/reset tag, kill tag and etc. The processor mainly consists of eight sub modules: Receive Buffer, Transmit Buffer, Random Number Generator (RNG), Slot Counter, Memory Controller, Reset Counter, Comparator, Controller.**

I. INTRODUCTION

Nowadays the applications of RFID are increasing rapidly, including supply chain management, access control to buildings, public transportation, open-air events, airport baggage, and so on. To meet the market requirements, the preferred RFID system must exhibit features like low cost, long operation range and high data rate, requiring a small and low-voltage/low-power integrated circuits [1].

Passive tags are more interested than active tags because of their great advantages such as low cost and maintenance free. In passive RFID tags, power supply is taken from incident RF electromagnetic wave transmitted by readers. The power consumption constraint in this kind of RFID requires an extremely low power transceiver. There are many wireless standards such as Bluetooth and Wi-Fi, but they are not suitable for ultra low power consumption applications such as RFID. Ultra wideband (UWB) technique [2] using impulse radio has possibility to achieve high throughput, long operating range, low power consumption, position location, ranging capability and low cost. It is recognized to be a cost-effective way to be integrated in the RFID system.

UWB offers several advantages to the whole RFID system. It offers longer operation range with less power consumption. Due to the short duration pulses used in UWB communication, compared to the narrowband radio, it is very difficult to jam or eavesdrop it. This feature makes it more secure in communication, so unlike the normal RFID, no complicated digital cryptography and coding are needed. It means reduction in baseband complexity, chip area and total power consumption. UWB communication has greater multiple access performance. Therefore no more complex circuit is needed for anti-collision protocol. On the other hand, more tags can be read in a short time with lower probability of collision. Ranging and positioning are other benefits that UWB brings to the system. It can be a powerful candidate for monitoring and positioning applications [3].

In this paper, we present a novel digital baseband processor designed for UWB-RFID system [3]. The processor receives the serial signals including commands and data from the RF receiver. Depending on the received commands, the processor can carry out various functions such as receive data and write to the memory, compare data, send data, set/reset tag, kill tag and etc.. The processor employs Framed Slotted ALOHA algorithm as anti-collision protocol. It is designed as a full digital ASIC, implemented with 1.8V voltage in 0.18 μ m CMOS technology.

II. SYSTEM DESCRIPTION

A. System architecture

The block diagram of the proposed module can be seen in Fig.1. It consists of a power scavenging unit, a power management block, a narrowband receiver, a low power impulse UWB transmitter, a digital baseband, an embedded UWB antenna and a dipole antenna.

As can be seen different standards have been used in uplink and downlink. Same as conventional passive RFIDs, incoming RF signal transmitted by the reader is used to provide power supply and receive the data. However, unlike usual RFIDs which back scatter the data to the reader; our proposed tag uses a low power impulse ultra wideband (IR-UWB) transmitter. The short pulses used in UWB communication, bring several advantages to the system such as more security, less collision probability, ranging and positioning capability and adaptive data rate[3].

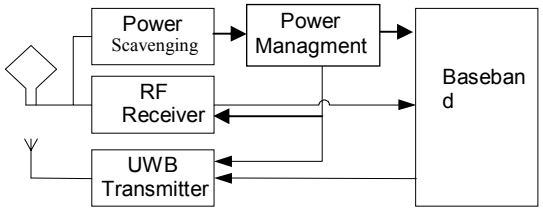

Fig. 1. Block diagram of the module

B. Block Diagram of the Baseband Processor

The processor can receive serial signals from the RF receiver at the rising edge of external clock 1 (which was extracted from

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the signals), the serial signals may be commands or data (64-bit ID,16-bit CRC,8-bit Pass,8-bit Control). Depending on the commands it received, the processor can carry out various functions such as receive data and write to the memory, compare data, send data, set/reset tag, kill tag and etc.. At the end of each function or bad incoming data, the processor enters the HALT mode and does nothing, then the Reset Counter starts to count and when it reaches 96, the processor will be reset. The RNG and slot counter are used to implement Framed Slotted Aloha anti-collision algorithm. The baseband processor mainly consists of eight sub modules: Receive Buffer, Transmit Buffer, Random Number Generator (RNG), Slot Counter, Memory Controller, Reset Counter, Comparator, and Controller.

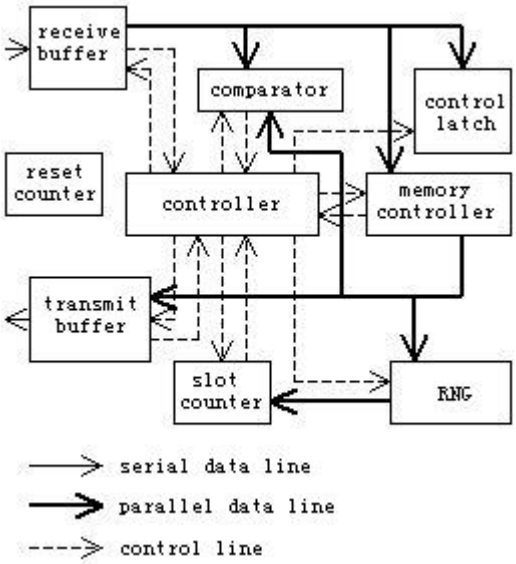


Fig. 2. Block diagram of the baseband processor

Fig. 2 is the block diagram of the baseband processor. The data flow between the sub modules is in parallel form. This can improve the efficiency of the baseband processor significantly. The controller is the control center of the processor. It sends control signals to other sub modules to control their status. It starts the sub module when needed and stops it when the sub module finishes its task. This can reduce the power consumption of the processor to a great level.

Table 1 summarizes the pins of the baseband processor chip.

TABLE 1. PINS OF THE BASEBAND PROCESSOR CHIP

Pins	Descriptions
CLK_1	External clock 1, can vary from 40KHz to 160KHz based on the received data rate.
CLK_2	External clock 2, high frequency (10MHz) clock which defines the transmitting data rate.
CLK_3	External clock 3, the second high frequency (100MHz) clock which defines the chip rate and does OOK modulation in UWB transmitter.
DATAIN	The serial input to receive the serial signals from RF receiver.
DATAOUT	The serial output from the Transmit Buffer to send the data.
RESETO	Reset signal output when Reset Counter reaches 96.

C. *Baseband control flow*

This baseband processor employs Framed Slotted ALOHA algorithm as the anti-collision protocol that each tag transmits its ID to the reader in a slot of a frame. The reader identifies a tag when it receives the ID without any collision and sends an acknowledgement in the next slot. The identified tag goes to the sleep mode after receiving the ACK in order to decrease the collision. Collided tags send the ID in the next frame again until all tags are identified.

Initially, all data (64-bit ID, 16-bit CRC, 8-bit Pass, kill bit, and flag bit) are stored in the memory. The processor firstly read out all the data and the kill and flag bits, from the memory if the power is on. Then it checks the kill bit to see if the tag is killed or active. Then if the tag is active (kill bit = 0), the RNG (Random Number Generator) will start to work to generate a random number. The RNG continues working until the processor receives the first 0 bit. Then, the processor can carry out various functions depending on the received following bits. If the next bit is 0, and the tag has not been identified before (flag bit=0), the processor performs a transmitting command. The ID and CRC are loaded into the Transmit Buffer and prepared for transmitting. Since the baseband processor employs Framed Slotted ALOHA algorithm as the anti-collision protocol, different tag transmits its ID in different time slot. The transmitting slot is chosen based on the generated random number by the RNG. Table 2 summarizes the commands performed by the processor.

TABLE 2. COMMANDS PERFORMED BY THE PROCESSOR

Bit Sequence	Commands and Functions
0	Transmitting (Send ID, CRC)
11	Reset Tag
101	Receiving Data (ID, CRC, Pass)
1001	Verify (Send ID, CRC, Pass)
1000	Check incoming bit sequence with ID
10001	ACK (Set Flag bit)
100001	Receive Control and write to control latch
100000	Check incoming bit sequence with Pass

Fig. 3 shows the state diagram for the baseband controller.

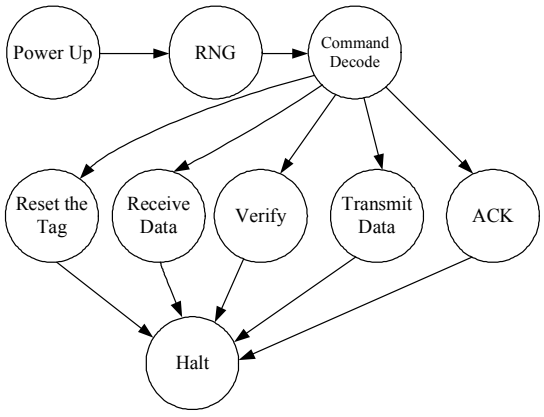


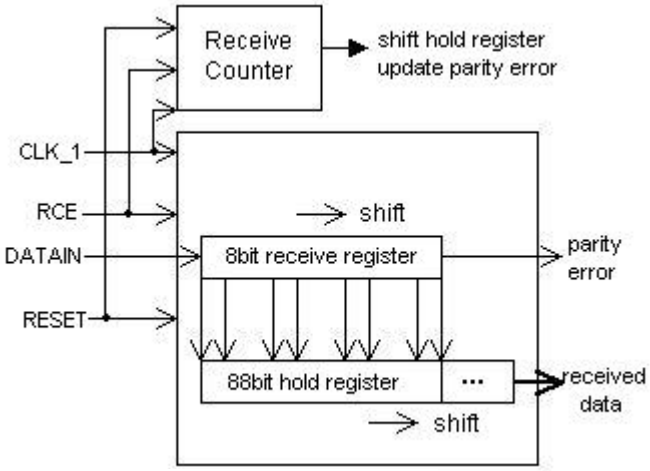
Fig. 3. State diagram of the baseband controller

D. Description of the Sub Modules

1) Receive Buffer

The Receive Buffer is used to receive the serial data (ID, CRC, Pass and Control) and check parity for every 8 data bits.

Fig. 4 shows the architecture of the Receive Buffer. It mainly consists of an 8-bit receive register, an 88-bit hold register and a receive counter.



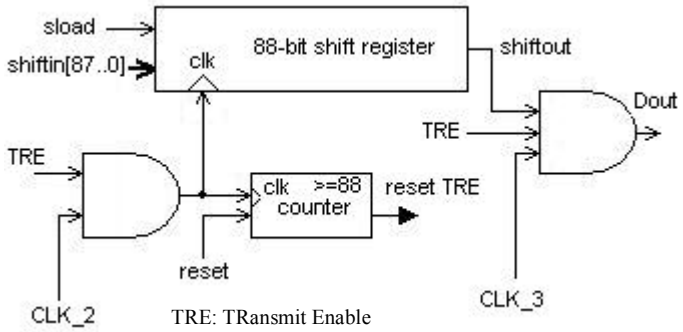
RCE: ReCeive Enable

Fig. 4. Architecture of the Receive Buffer

The 8-bit receive register is an 8-bit shift register, it right shifts 1 bit at the rising edge of CLK_1 in one shift action. The 88-bit hold register is an 88-bit shift register, it right shifts 8 bits at the rising edge of the CLK_1 in one shift action. The receive register performs shift actions when receiving the data from DATAIN, when all 8 bits data have shifted into the receive register, the data are loaded into the hold register and the hold register performs one shift action. This will go on and repeat until all the required data are received by the hold register. When all the required data are received by the hold register, the RCE will be disabled and the Receive Buffer stops working. The receive counter counts the receiving. The Receive Buffer has a mechanism which can check parity for every 8 bits incoming data during the receiving.

2) Transmit Buffer

The Transmit Buffer is used to modulate and send the data (ID, CRC and Pass).



TRE: TRansmit Enable

Fig. 5. Architecture of the Transmit Buffer

Fig.5 shows the architecture of the Transmit Buffer. It mainly consists of an 88-bit shift register and a transmit counter.

The synchronous load-parallel in-serial out shift register is used as the transmitting cache. CLK_2 is used to clock the transmitting and CLK_3 is used to do the On-Off Keying modulation. We choose On-Off Keying as the modulation method because of its simplicity. The data can be loaded into the shift register through the 88-bit parallel input shiftin, and shift out through the serial output shiftout. The transmit counter counts the transmitting, and when all the data were transmitted, the TRE is disabled by the Controller and the Transmit Buffer stops working.

3) Random Number Generator and Slot Counter

The RNG is a 16-bit Linear Feedback Shift Register (LFSR), and the Slot Counter is a 16-bit synchronous load down counter. Architecture of the RNG can be seen in fig. 6.

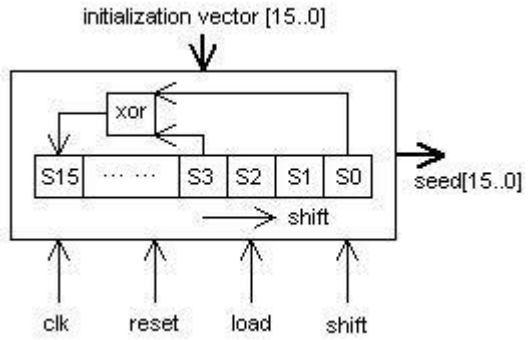


Fig. 6. Architecture of RNG

To increase the randomness of the Random Number, we explored a new method to generate the Random Number. We use the 16-bit CRC data which was fetched from the memory as the initialization vector of the RNG, and the tag's unique ID data determine the working period of the RNG. Because of the different initialization vector and different working period of each tag's RNG, the probabilities of same random number among tags are reduced to very small.

The RNG works after checking the kill bit and before starting to receive comands, in which period most of the modules don't work, this can reduce the peaking power of the baseband processor.

The generated 16-bit random number is loaded into the Slot Counter, and the transmitting will not start until the Slot Counter counts to 0, therefore different tag can transmit in different time slot.

4) Memory Controller

We choose an I^2C bus EEPROM as the memory. So the memory controller is a simple I^2C bus controller. It does not support multimaster mode and slave mode, this can reduce the circuit complexity significantly.

The memory controller is clocked by CLK_2, it can produce a SCL of 100KHz. Although the EEPROM supports 400KHz mode, we only use the 100KHz mode because this can reduce the power consumption significantly.

Tri-state buffers are utilized to connect the I2C bus controller to the I2C bus.

5) Reset Counter and system reset function

At the end of each function or bad incoming data, the processor enters the HALT mode and does nothing. Then the Reset Counter starts to count up to 96, and reset the circuit.

The reset counter is clocked by the internal clock (250KHz) which is generated by CLK_2, and reset by the rising and following edge of CLK_1. When the processor enters the HALT mode and if there is no rising and following edge of CLK_1, the Reset Counter can count up and when it reaches 96 (after about 400ms), a short pulse will be generated at the output RESETO and reset the circuit. The Reset Counter does not work when the processor is in working mode, and starts to work only when the processor enters the HALT mode. This can reduce the peaking power consumption of the processor. Figure 7 shows the architecture of the Reset Counter, Figure 8 shows the method to generate the edge-reset signal from CLK_1.

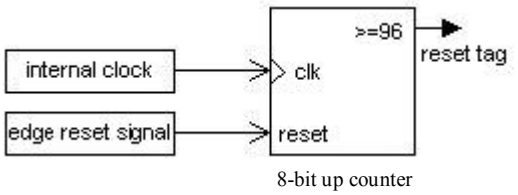


Fig. 7. Architecture of the Reset Counter

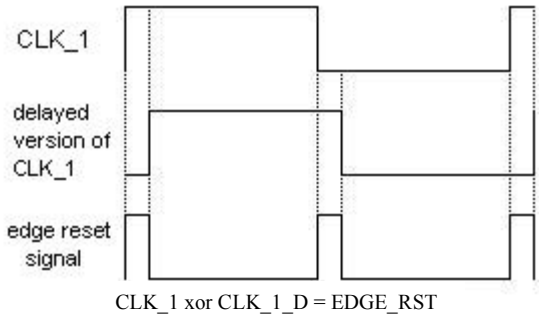


Fig. 8. Method to generate the edge-reset signal

6) Controller

The Controller is the control center of the baseband processor. It is mainly a FSM which is based on the state diagramof Fig.3. It sends control signals to the sub-modules and receives status signals from the sub-modules to control their status. It starts the sub-module when needed and stops it when the sub-module has finished its task, this can reduce the peaking power of the processor significantly.

III. RESULTS AND DISCUSSIONS

The baseband processor is designed as a full digital ASIC, implemented with 1.8V voltage in 0.18 μ m CMOS technology. The final chip is supposed to be integrated into the UWB module designed for the UWB RFID tag. So the circuit should be ultra low power and in small area. During the design, we use several methods to reduce the power consumption of the baseband processor, especially the peaking power.

We use Altera FPGA device Hardcopy Stratix (a structured ASIC in 0.13 μ m technology) and Altera Quartus II 6.0 PowerPlay to do the power analysis, the dynamic power of the logic cells is 0.04 mW, or 40 μ W, this basically fulfills the requirements of the UWB Transceiver for a power consumption of tens of μ W.

We use LeonardoSpectrum from Mentor Graphics as the synthesis tool. We use Gray state machine encoding method and optimize for area, the total number of gates is 9616, in the scale of thousands of gates, this is a very small area.

IV. CONCLUSIONS AND FUTURE WORKS

In this paper, a novel digital baseband processor designed for UWB Transceiver on RFID tag is presented. Due to the security feature and other advantages of UWB, no complicated coding and cryptography is needed. This also reduces the complexity, area and power consumption of the baseband processor. Furthermore, several strategies of reducing the power has explored during the design, so the final power consumption of the baseband processor basically fulfills the ultra low power requirements of the UWB Transceiver.

Future works include integrating the baseband processor into the UWB Transceiver to test the whole system and researching for more strategies to reduce the power consumption of the baseband processor if possible.

V. ACKNOWLEDGEMENT

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