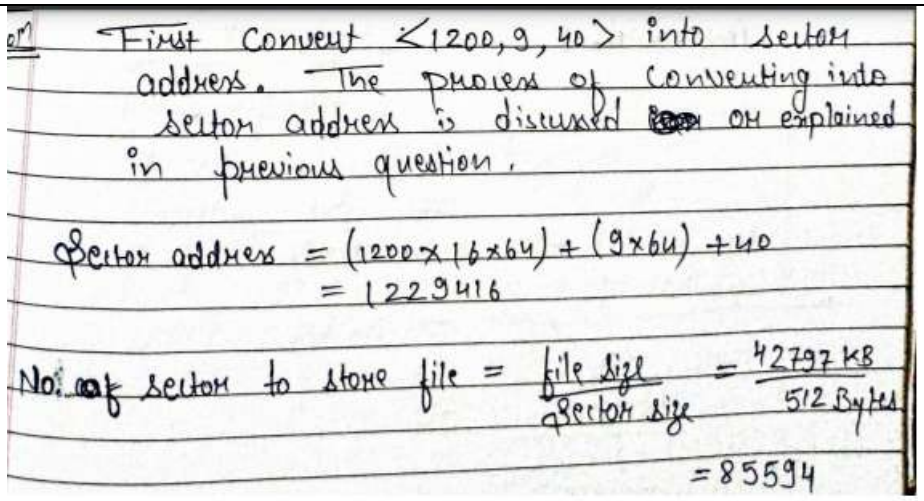
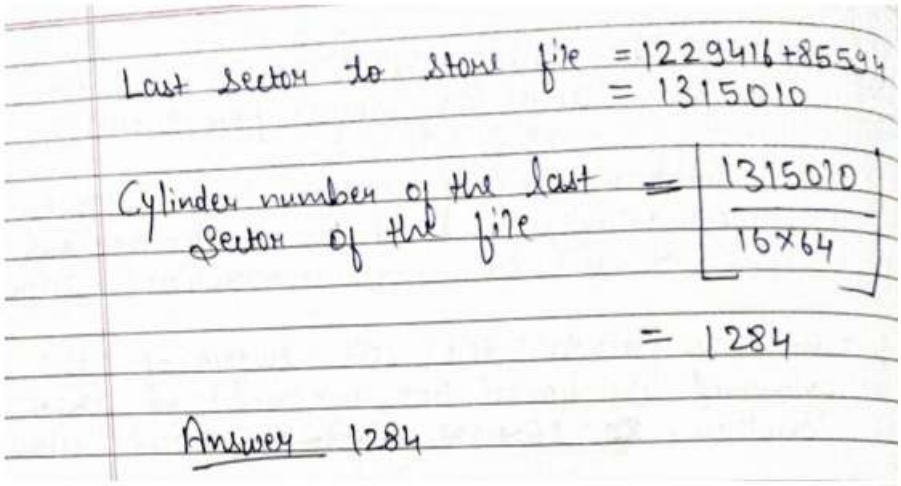
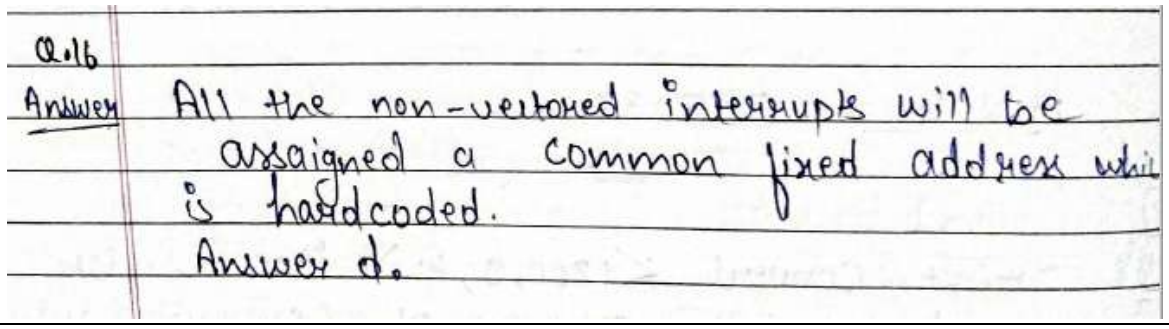


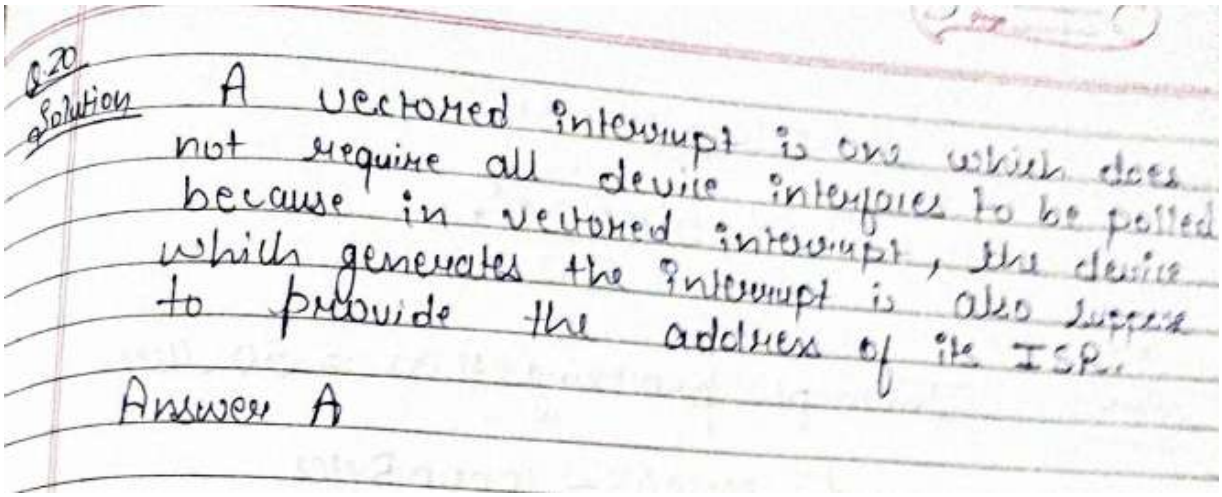


Q10. When the processor constantly checks the status of an I/O device, this is called:
(a) Memory mapped I/O
(b) Asynchronous communication
(c) Interrupt-Driven I/O
(d) Polling
Answer : (d)
Solution :
When processor constantly check the status of an I/O device this is called polling.
Answer: D

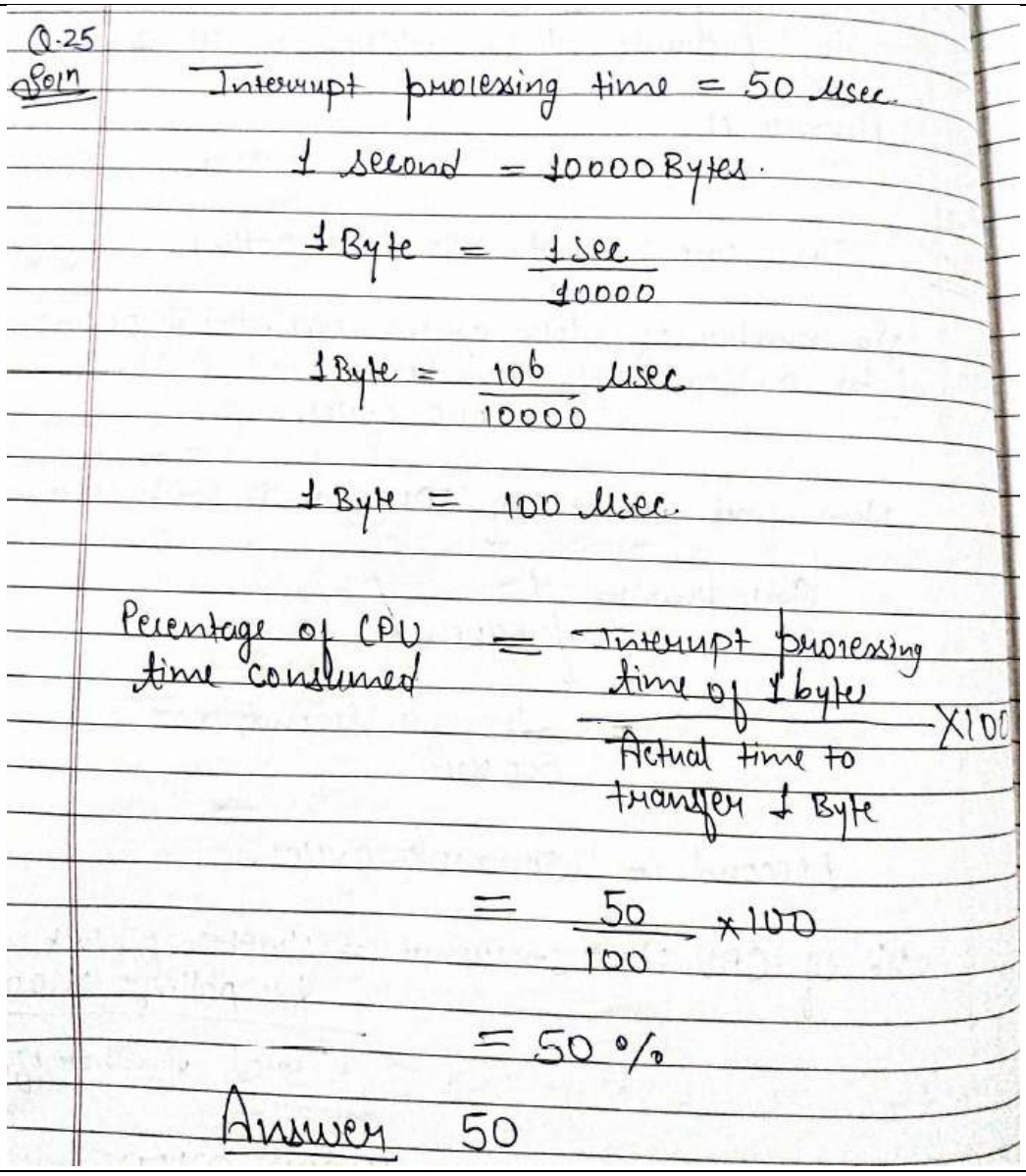
Q11. What advantage(s) does Interrupt-Driven I/O have over polling?
(a) Interrupt-Driven I/O is synchronous while polling is asynchronous
(b) Interrupt-Driven I/O does not require any additional hardware
(c) Interrupt-Driven I/O allows the computer to process other tasks while waiting for I/O
(d) Interrupt-Driven I/O can be memory-mapped while polling cannot
Answer : (c)
Solution :
In interrupt driven I/O allow the computer to process other tasks while waiting
for I/O.

	Answer: C
Q12.	**[MSQ]** Which of the following statements below is/are true? (a) In polling, I/O devices set flags that must be periodically checked by the CPU (b) When using interrupts, the CPU interrupts I/O devices when an I/O event happens (c) The overhead of polling depends on the polling frequency (d) Polling is often a viable option for slow and asynchronous devices Answer :(a)&(c) Solution : (a) True, In polling I/O device set flag that must be periodically check by CPU true. (b) False because CPU does not generate interrupt. Interrupt are generated by I/O device. (c) True (d) False **Answer: (a)&(c)**
Q13.	When the processor treats I/O devices as locations in memory and uses the same instructions to access them, this is called: (a) Memory mapped I/O (b) Asynchronous communication (c) Synchronous communication (d) Interrupt-Driven I/O Answer : (a) Solution : Memory mapped I/O uses the same address space to address both memory and I/O.**Answer: A**
Q14.	**[MSQ]** Which of the following is /are advantages of cycle stealing in DMA. (a) It increases the maximum I/O transfer rate. (b) It reduces the interference by the DMA controller in the CPU's memory access. (c) It is beneficially employed for I/O device with shorter bursts of data transfer. (d) None of the above Answer : (a)(b)&(c) Solution : All are the advantages of cycle stealing mode .
Q15.	The main reason for implementing DMA in a computer system is (a) To free off the CPU from cache coherency problems.

	(b) To simplify the writing of interrupt service routines (c) To remove the need for a buffer on the device interface (d) To speed up the transfer of data between an interface and the main memory Answer : (d) Solution : CPU sole purpose is to execute instruction, not data transfer. Thus CPU transfer data solely dma was introduce to reduce this time .
Q16.	In a non-vectored interrupt, the address of interrupt service routine is (a) Obtained from interrupt address table. (b) Supplied by the interrupting I/O device. (c) Obtained through Vector address generator device. (d) Assigned to a fixed memory location. Answer : (d) Solution : 
Q17.	Which of the following I/O methods requires the CPU to initialize the I/O device? i. Programmed I/O ii. Interrupt driven I/O iii. Direct memory access (a) ii and iii only (b) iii only (c) i and ii only (d) All of the above Answer : (D) Solution :
Q18.	Which of the following I/O methods requires the CPU be able to use interrupts? i. Programmed I/O ii. Interrupt driven I/O iii. Direct memory access (a) ii and iii only (b) iii only (c) i and ii only (d) All of the above **Answer : (a)** **Solution :**
Q19.	Which of the following I/O methods requires the CPU to act as a bridge for moving data between the I/O device and main memory?

	i. Programmed I/O ii. Interrupt driven I/O iii. Direct memory access (a) ii and iii only (b) iii only (c) i and ii only (d) All of the above Answer : (c) Solution :
Q20.	A vectored interrupt is one which (a) Does not require all device interfaces to be polled (b) Does not require the cpu to check the interrupt line at the end of each" Fetch and Execute" cycle (c) Reduces the number of control lines needed on the bus (d) Removes the need to enable interrupts on the interface Answer : (a) Solution : 
Q21.	In order to execute a program, instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory accesses would be needed in this case to transfer a 32 bit instruction from memory to the CPU? (a) 1 (b) 2 (c) 3 (d) 4 **Ans :-d since we have &data lines in data bus at a time or in a cycle & bit data can be transferred so if we want to a accurs 32 bits** **32/8 =4 cycles will be necessary or 4 memory accurs .**
Q22.	Consider a printer which can print 20 pages per minute where a page consists of 4000 characters (1 character = 1 byte). it takes 50 microseconds by CPU to handle a interrupt. How much CPU time per minute is consumed in handling the interrupt if output is sent to the printer one character at a time?_____% Answer : (6.67) Solution : 20 pages and consist of 4000 character per page, and print 20 pages in one minute.

	4000*20→80,000 character print in one minute. and interrupt are generated per single character and so total interrupt generate = 80,000. and for handing single interrupt = 50microseconds are required. for handling 80,000 interrupt number of time= 80,000*50 =40,00000 used ⇒4sec →$\frac{4}{60}$ Minute, consumed by CPU to handle interrupt = 0.06666 = 6.67% **Answer: 6.67**
Q23.	Assume the number of clock cycles for a polling operation, including transferring to the polling routine, accessing the device, and restarting the user program, is 400 cycles, with a 500 MHz clock. The mouse must be polled 30 times a second to ensure that no user movement is missed. Fraction of CPU time (in %) consumed for polling is_____ Answer : (0.002) Solution :
Q24.	Suppose we want to read 5000 bytes in programmed I/O mode of transfer, where the bus width is 16 bits. Each time an interrupt occurs, it takes 10 microseconds to service it (i.e. transfer 16 bits). The CPU time required to read 5000 bytes is _____milliseconds. Answer :(25) Solution : 25 milliseconds. 2 byte transfer requires a minimum of 10 microseconds. So, 5000 bytes transfer will require: 10 / 2 * 5000 = 25,000 microseconds = 25 milliseconds.
Q25.	Consider a system employing interrupt-driven I/O for a particular device that transfers data at an average of 10000 bytes per second on a continuous basis. If interrupt processing takes 50 μs, what fraction(in percent) of CPU time is consumed by this I/O device if it interrupts for every byte?_____ Answer : (50) Solution :



Q26. The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 32 Mbytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____

Answer : (512)

Solution :

Maximum number that can be stored in 16 bits is $2^{16} - 1 = 65535 = 64K$ (approx.)

So, up to 64K bytes of data can be transferred by the DMA controller at a time.

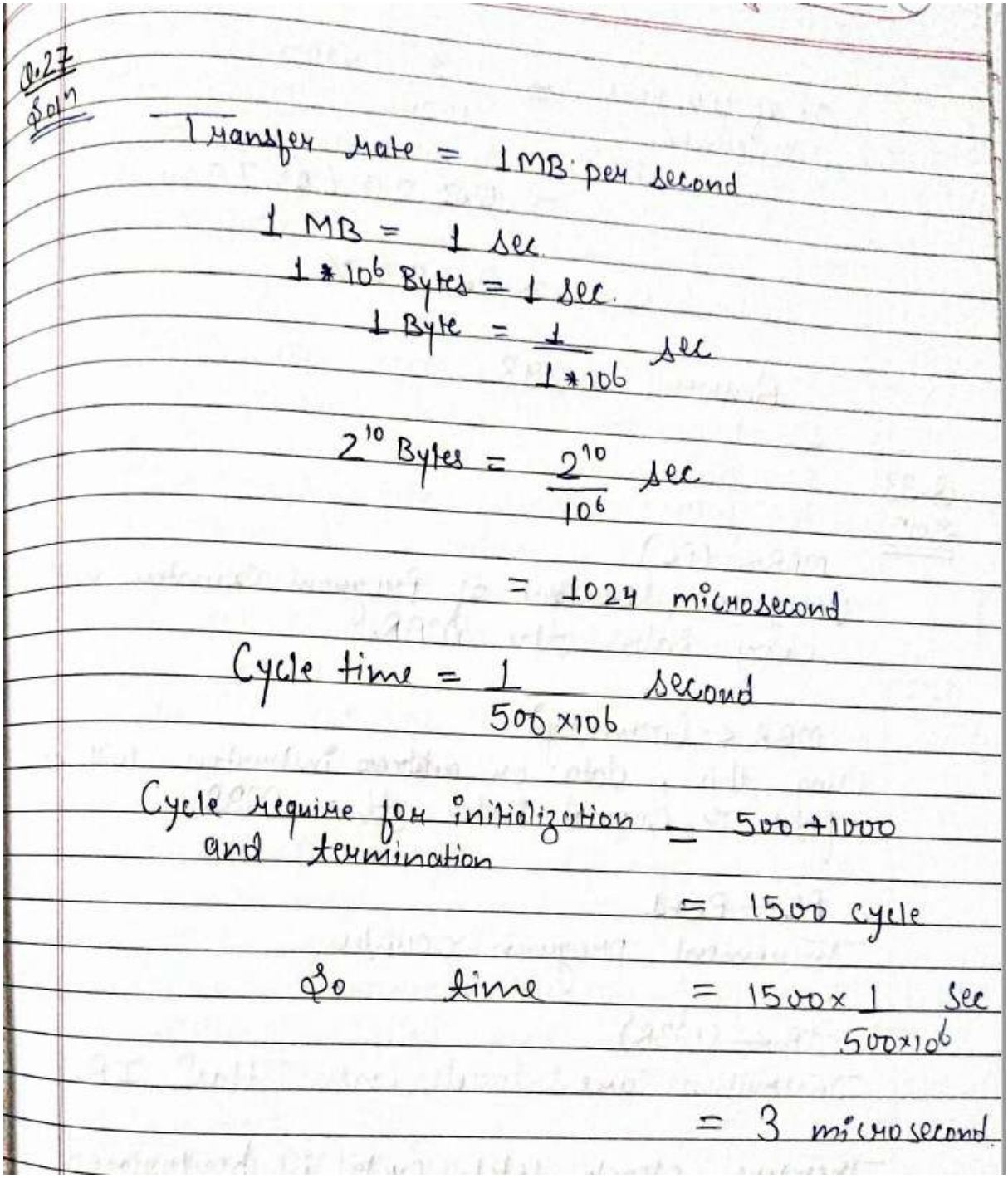
Number of times DMA controller needs to be invoked = 2^{15} K / 64 K= 512

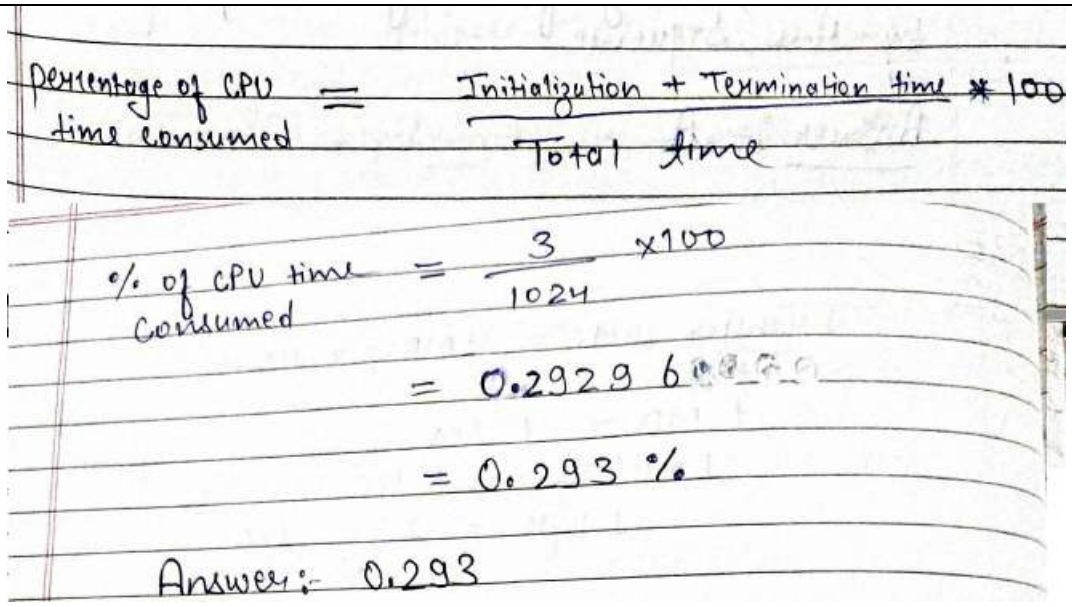
Q27. A hard disk with a transfer rate of 1 Mbytes/ second is constantly transferring data to memory using DMA. The processor runs at 500 MHz, and takes 500 and 1000 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 1 Kbytes, what is the percentage of processor time consumed for the transfer operation?_____(Rounded off to three decimal

places)

Answer : (0.292)

Solution :





Q28.

A DMA controller transfers 4 byte words from an input device to memory in one clock cycle using cycle stealing. The input device transmits data at a rate of 9600 bytes per second. The CPU is fetching and executing instructions at an average rate of 1,000,000 instructions per second. Assume that size of each instruction is4bytes. The CPU will be slowed down because of the DMA transfer by _____ percent.

Answer : (0.24)

Solution :

In 1 second, the input device transfers 9600 bytes of data.

This is equivalent to 9600 / 4 = 2400 DMA cycles, as 4 bytes are transferred every cycle.

Earlier, in 1 second, 1,000,000 instructions were executed.

But now, in 1 second, (1,000,000 – 2400) = 997600 instructions are executed.

So, slowdown = 2400/1000000 = 0.24 %

Q29.

A hard drive with a maximum transfer rate of 1MB/sec is connected to a 32-bit, 10 MIPS CPU operating at a clock frequency of 100 MHz. Assume that the I/O interface is DMA based and it takes 500 clock cycles for the CPU to set-up the DMA controller. Also assume that the interrupt handling process at the end of the DMA transfer takes an additional 300 CPU clock cycles. If the data transfer is done using 2000Bytes blocks, what is the percentage of the CPU time consumed in handling the hard drive?_____

Solution

Since the hard drive transfers at 1MB/sec, and each block size is 2KB, there are

1000/2= 500 blocks transferred/sec

Every DMA transfer uses 500+300=800 CPU cycles. This gives us

800x500 = 400,000 = $400x10^3$ cycles/sec For the 100 MHz CPU, this

	corresponds to $(400x10^3) / (100x10^6) = 4x10^{-3} = 0.4\%$ This would be the case when the hard drive is transferring data all the time. In actual situation, the drive will not be active all the time, and this number will be much smaller than 0.4%.
For the next two questions, consider a system in which bus cycle takes 500 ns. Transfer of bus control in either direction, from processor to device or vice-versa, takes 250 ns. One of the I/O device has data transfer rate of 75 KB/sec and employs DMA. Data are transferred one byte at a time.	
Q30.	Suppose we employ DMA in a burst mode. That is, the DMA interface gains bus master ship prior to the start of block transfer and maintains control of the bus until the whole block is transferred. For how long (in nanoseconds) would the device tie up with the bus when transferring a block of 256 bytes?_____(Rounding to 2 decimal places) Ans. Time to start + end DMA = 250+250= 500 nsec. Since device is slow, the DMA speed is governed by device speed. Time taken by device $= \frac{256}{75 \times 10^3} = 3.4msec$ Total time = 500 nsec + 3.4 msec. ≈ 3.4 msec.
Q31.	Now suppose we employ DMA in a cycle stealing mode. That is, the DMA interface gains bus master ship prior to the start of each byte of data to be transferred and then return control to the CPU after each byte of data transferred. For how long (in nanoseconds) would the device tie up with the bus when transferring a block of 256 bytes?_____ (Rounding to 2 decimal places) Ans. The bus cycle is stolen for 256 times. Time for bus transfers (256 times) = (250+250)*256 = 128,000 nsec. Time for 256 bus cycles = 256 * 500 = 128,000 nsec. Total = 256,000 nsec. = 0.256 msec.
Q32.	Consider the following sequence of microinstructions t1: MAR ← (PC) t2: MBR ← (memory), PC ← (PC) + 1 t3: IR ← (MBR) t4: MAR ← (PC) t5: MBR ← (memory), PC ← (PC) + 1 t6: R1 ← R1 + (MBR) What operations do the following instructions perform? (a) Add the number NUM to register R1. (b) Add contents of memory location NUM to register R1. (c) Add contents of the memory location whose address is at memory location NUM to register R1 (d) None of the above