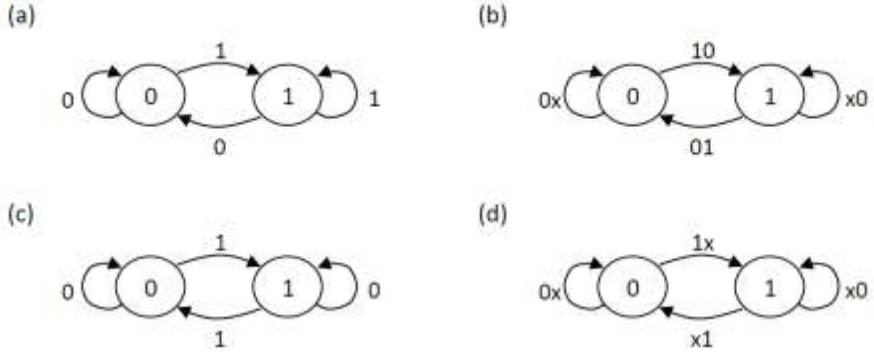
In n – bit carry look ahead adder output (carry propagation) is independent of Cin. Therefore less delay as compared to n – bit ripple carry adder. But look ahead carry adder requires complex circuitry as $\frac{n\,(n+1)}{2}$ AND & n 'OR' gates for n bit addition.

∴ (a) is true.

Sequential Circuit

Q1. Match the following state diagrams to the 4 flip-flops: JK flip-flop, D flip-flop, SR flip-flop, and T flip-flop. Don't-care value is indicated by "x".



(A) (a)- T Flip-Flop, (b) – JK FlipFlop (c)- D FlipFlop (d) – SR FlipFlop
(B) (a)- D Flip-Flop, (b) – JK FlipFlop (c)- T FlipFlop (d) – SR FlipFlop
(C) (a)- D Flip-Flop, (b) – SR FlipFlop (c)- T FlipFlop (d) – JK FlipFlop
(D) (a)- D Flip-Flop, (b) – JK FlipFlop (c)- SR FlipFlop (d) – T FlipFlop

Answer :- C

Solution

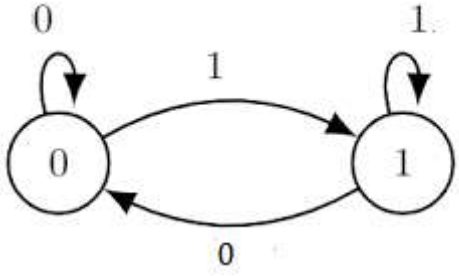
Characteristic table:

D Flip flop

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$Q_{n+1} = D$

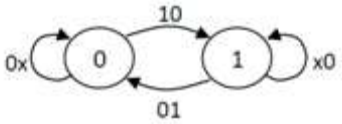
State diagram can be drawn as



R- S flip flop:

Q_n	R	S	Q_{n+1}
0	0	0	0
1	0	0	1
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	0
×	1	1	invalid

State diagram can be drawn as



Excitation table for R S flip flop:

Q_n	Q_{n+1}	R	S
0	0	×	0
0	1	0	1
1	0	1	0
1	1	0	×

By looking excitation table, we can easily draw transition from current state to next state.

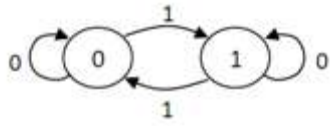
R –S matches with the option (b).

T flip flop:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q_{n+1} = T \oplus Q_n$

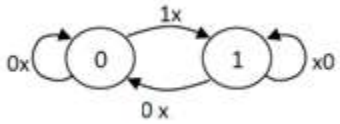
Characteristic equation



Matches with option ©.

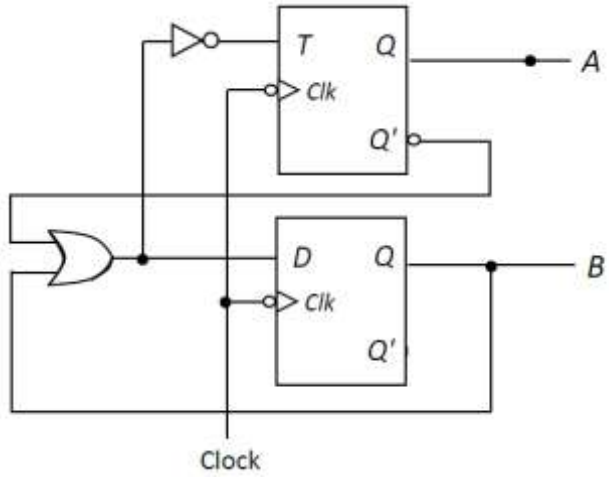
J K flip flop;-

Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	0
1	1	×	0



Matches with (d).

Q2. Consider the following sequential circuit?(Assume initial clock is 00)



What is the output AB of the circuit after two clock cycle?

(a) 00 (b) 01

(c) 10 (d) 11

Answer :- B

Solution

$A^+ = (\overline{A} + B)' \oplus A$

$= A\overline{B} \oplus A$

$= A\overline{B}.\overline{A} + A.\overline{A\overline{B}}$

$= A\,(\overline{A} + B) = AB$

$= A^+ = AB$

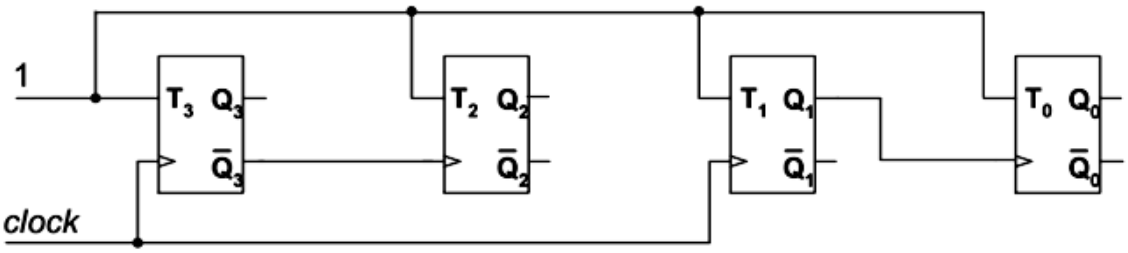
$B^+ = \overline{A} + B$

AB $\xrightarrow{\text{CLOCK}}$ A^+ B^+

00 $\xrightarrow{\text{1ST}}$ 0 1

01 $\xrightarrow{\text{2ND}}$ 0 1

Q3. If the current state is Q3Q2Q1Q0=0101, then after the next positive edge of the clock signal the new state of Q3Q2Q1Q0 will be:



(a) 0110

(b) 1111

(c) 1011

(d) 1110

Answer :- D

Solution

T_3& T_1 are synchronous while (T_2 changes its o/p when T_3 falls from 1 to 0).

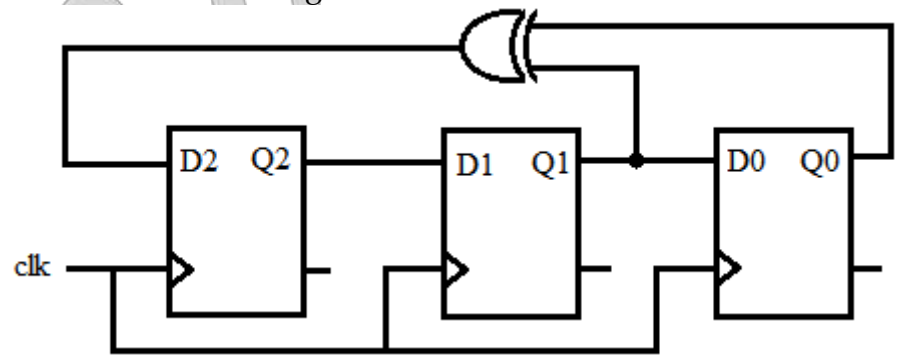
(T_0 changes its o/p when T_1 rises from 0 to 1).

Now Q_3 Q_2 Q_1 Q_0 $Q_3^+ Q_2^+ Q_1^+ Q_0^+$

0 1 0 1 → 1 1 1 0

1 1 1 0 (changes)

Q4. Consider the following MOD-N counter circuit



If the initial state of the circuit is $Q_2Q_1Q_0$ is 100, then the value of N is_____

Answer :- 7

Solution

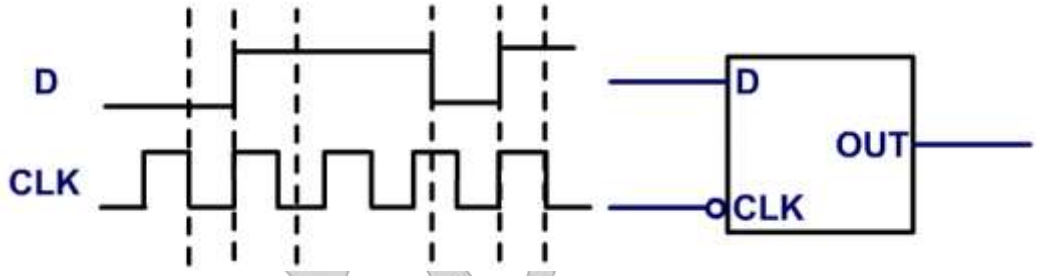
Clearly given counter circuit is synchronous.

$R_2^+ = Q_0 \oplus Q_1$	$Q_1^+ = Q_2$	$Q_0^+ = Q_1$

Q_2	Q_1	Q_0	next state $Q_2^+ Q_1^+ Q_0^+$
1	0	0	0 1 0
0	1	0	1 0 1
1	0	1	1 1 0
1	1	0	1 1 1
1	1	1	0 1 1
0	1	1	0 0 1
0	0	1	1 0 0

Mod 7 counter circuit.

Q5. What is the appropriate output sequence of the following negative level edge triggered circuit assuming that initial state is 0(also assume that setup time is zero and hold time is equal to cycle time)?



(a) 001111

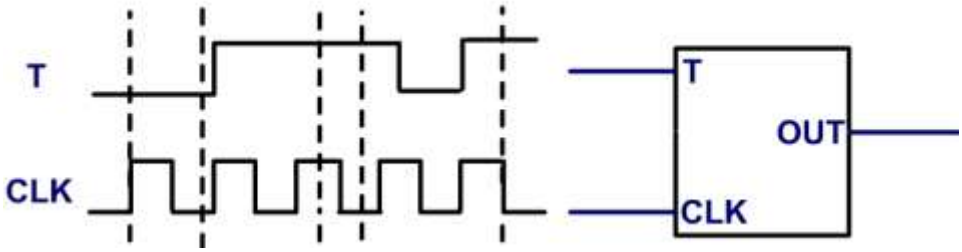
(b)000110

(c)100101

(d) 001101

Answer :- D

Q6. What is the appropriate output sequence of the following positive level edge triggered circuit assuming that initial state is 0 (also assume that setup time is zero and hold time is equal to cycle time)?



(a) 01011 (b) 10011

(c) 000000 (d) None

Answer :- D(01010)

Solution

Ans :-D

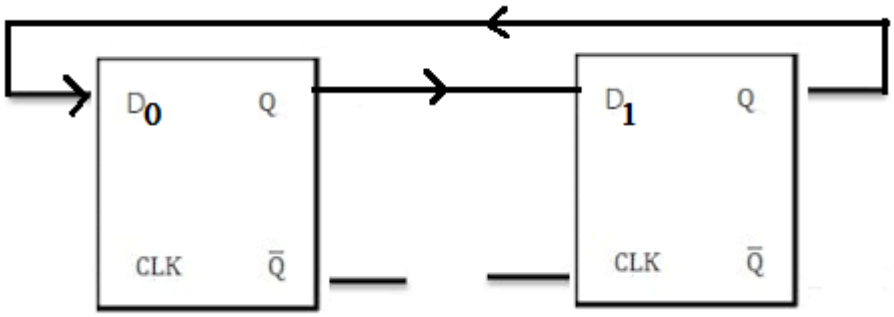
Q7. Consider a counter circuit in which D flip-flops are in series and the output of the last D flip flop is connected to the D input of the first flip flop. The counter is

(a) Ring Counter (b) johnson counter

(c) straight counter (d) None of the above

Answer :- A

Solution



Q_0	Q_1
0	1
1	0

$Q_0^+ Q_1^+$

1 0

0 1

Above circuit is Mod-2 ring counter.

Q8. Consider a counter circuit in which D flip-flops are in series and the complement of the

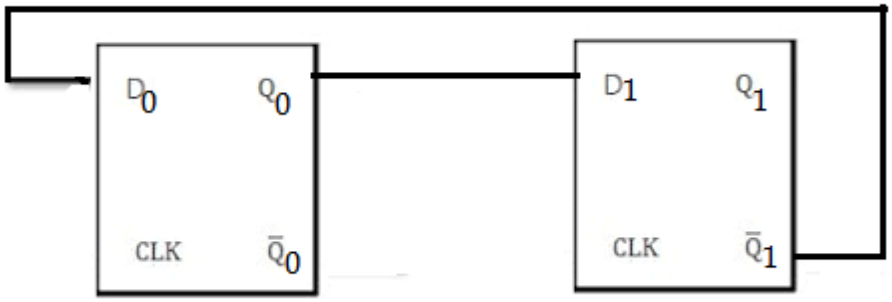
output of the last D flip flop is fed back to the D input of the first flip flop.

(a) Ring Counter (b) Johnson counter

(c) Straight counter (d) None of the above

Answer :- B

Solution



Q_0	$Q_1 Q_0^+ Q_1^+$		
0	0	1	0
1	0	1	1
1	1	0	1
0	1	0	0

Mod 4 Johnson counter

Q9. How many states does a 3-bit ring counter will have?____

Answer :- 3

Solution

In ring counter.

No of states = No of bits in ring counter.

So it is 3 bit ring counter

Than no of states =3

So answers is :-3

Q10. How many states does a 3-bit Johnson counter will have?_____

Answer :- 6

Solution

In Johnson counter no of ratter =2 n

=2x(no of bit)

2x3=3

So answers is :-6

Q11. How many unused states does a 3-bit Johnson counter will have?_____

Answer :- 2

Solution

No. of used states in n bit Johnson Counter = 2n

Total states in n bit counter = 2^n

$\therefore$ No. of unused states = $(2^n - 2n)$

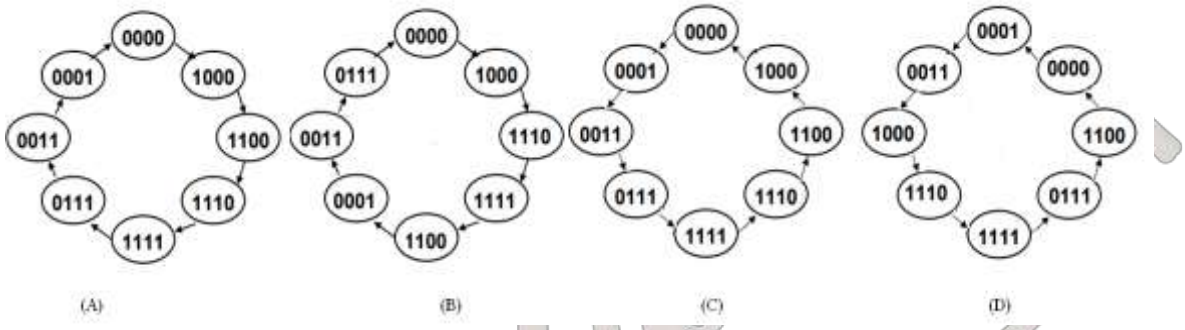
For 3 bit :

Unused states = $2^3 - 2 \times 3$

$= 8 - 6$

$= 2$ unused states.

Q12. Which of the following is correct state diagram for a 4-bit Johnson counter?



Answer :- A

Solution

4 bit Johnson Counter

Q_0	Q_1	Q_2	Q_3	next State Q_0^+	Q_1^+	Q_2^+	Q_3^+
0	0	0	0		1	0	0	0
1	0	0	0		1	1	0	0
1	1	0	0		1	1	1	0
1	1	1	0		1	1	1	1
1	1	1	1		0	1	1	1
0	1	1	1		0	0	1	1
0	0	1	1		0	0	0	1
0	0	0	1		0	0	0	0

Q13. The content of a 4-bit shift register is initially 1101. It is shifted to the left six times with the serial input being 101101. What is the content of the register at the end?

(a) 0110 (b) 1011 (c) 1101 (d) None

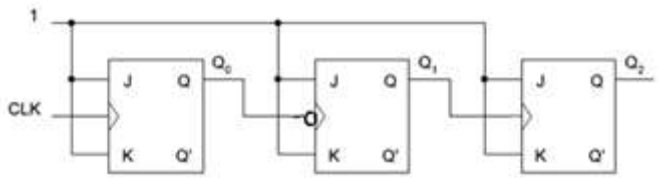
Answer :- C

Solution

Initial	Clock	Next
1101	$1^{st}\rightarrow$	1011
1011	$2^{nd}\rightarrow$	0110
0110	$3^{rd}\rightarrow$	1101
1101	$4^{th}\rightarrow$	1011
1011	$5^{th}\rightarrow$	0110
0110	$6^{th}\rightarrow$	1101

Trick: As after 6^{th} clock all 4 bit got washed and addition 2 bits from input also vanish (leftmost 2 bits), $\therefore$ we left with 1101

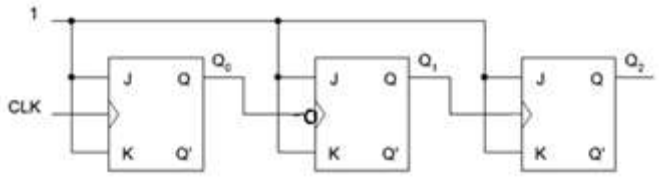
Q14. Consider the following mod-N counter circuit:



The value of N is_____

Answer :- 8

Solution

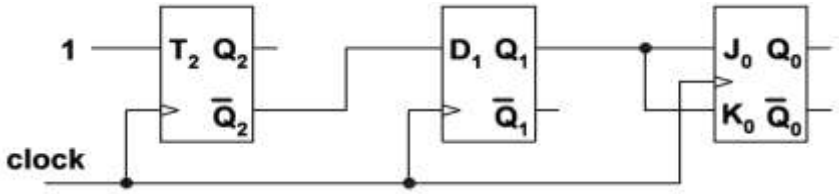


Q_0	Q_1	Q_2
0	0	0
1	0	0
0	1	1
1	1	1
0	0	1
1	0	1
0	1	0

1	1	0
1	1	0
0	0	0

Mod 8 counter

Q15. Consider following counter circuit:



After how many states you will get state 111(Q3Q2Q1) using initial state 000 ?_____

Answer :- 3

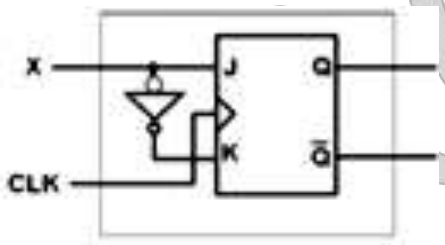
Solution

Q_2	Q_1	Q_0
0	0	0
1	1	0
0	0	1
1	1	1

$T_2 = 1$ $D_1 = Q`_2$ $J_0 = K_0 = Q_1$

After 2 states form initial state we. Will get state 111

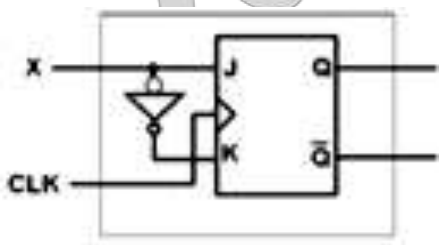
Q16. Consider following figure,



for what value of x you will get complement of previous state to find next state?____

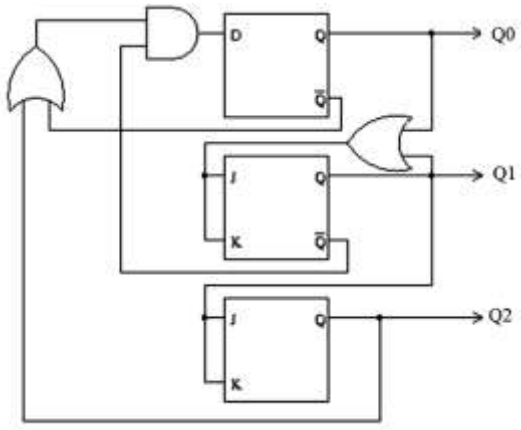
Answer :- 1

Solution



X=1

Q17. For the synchronous circuit shown below which of the following is valid transition sequence for (Q2,Q1,Q0) Sequence?



(a) 0→1→2→4→5→7→0 (b) 0→1→2→3→4→5→0

(c) 0→1→2→4→7→5→0 (d) 0 →4 →2→1→5→7→0

Answer :- A

Solution

D0 = $\overline{Q1}$ (Q2+Q0')

J1=K1=Q0+Q1

J2=K2=Q1

Q2	Q1	Q0
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	1
0	0	0

0 →1→ 2→ 4→5→ 7→ 0

Answer is A

Q18. If the present (ABC) state is 110, and the input X=0 ; what will be the next state if the flip flops input

functions are as follows:

J_A=B'X K_A=1

J_B=A+C'X' K_B=XC'+CX'

J_C=AX+A'B'X' K_C=X

(a) 111 (b) 001 (c) 010 (d) 011

Answer :- C

Solution

$J_A=B'X$ $K_A=1$

$J_B=A+C'X'$ $K_B=XC'+CX'= C\oplus X$

$J_C=AX+A'B'X'$ $K_C=X$

A	B	C
1	1	0
0	1	0

Input X=0

$J_A=B'x =0$

$K_A =1$

J_B $A+\bar{C}\bar{X}=1+1.1=1$

$K_B =C\oplus X= 0+X=X=0$

$J_C = AX+\bar{A}\bar{B}\bar{X}$

=1.0+0.0.1=0

$K_C =X=0$

The next output will be

010.

Answer is C

Q19. A sequential circuit with two D flip-flops A and B, and one input X is specified by the following input equations:

$DA = AX + BX$

$DB = A'X$

What are the next states of the flip-flops A and B if the present state of the flip-flops A, B and the input X equals, 001, 110 respectively:

(a)11, 00 (b) 10, 00

(c) 00, 10 (d) 01, 00

Answer :- D

Solution

$D_A = AX + BX$, $D_B= \bar{A}X$

A	B	X
0	0	1
0	1	

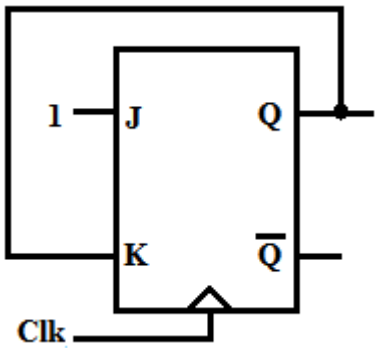
A	B	X
1	1	0
0	0	

If present state is 001 then next state of the flip- flop A & B is 01.

And if present state is 110 then next state of the flip-flop A &B is 00.

Answer is D

Q20. In a J-K flip-flop we have J = 1 and K = Q. Assuming the flip-flop was initially cleared and then clocked for five pulses, the sequence at the Q output will be



(a) 1,0,0,0,0 (b) 1,0,0,1,0

(c) 1,1,0,0,1 (d) 1,0,1,0,1

Answer :- D

Solution

Given J = 1, K = Q

Characteristic equation for J K flip flop

$Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$

$Q_{n+1} = \overline{Q_n} + \overline{Q_n}Q_n = \overline{Q_n}$

$Q_{n+1} = Q_{n+1} = \overline{Q_n}$

0 $1^{st}\rightarrow$ 1

1 $2^{nd}\rightarrow$ 0

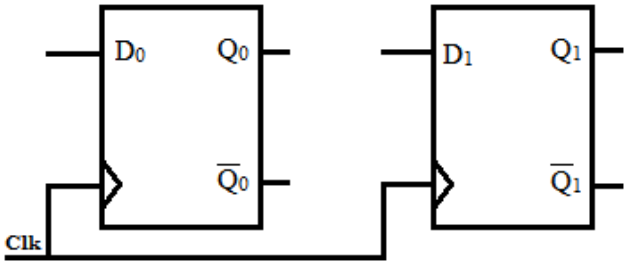
0 $3^{rd}\rightarrow$ 1

1 $4^{th}\rightarrow$ 0

0 $5^{th}\rightarrow$ 1

(d) 1, 0, 1, 0, 1

Q21. Consider the two D – flip-flops as shown below:



Both are to be connected as a synchronous counter that goes through the following Q_0, Q_1 sequence: 00 →10 →11→01→ 00 → …

The inputs D_0, D_1 respectively should be connected as:

(a) $\overline{Q_1}$ and Q_0

(b) Q_0 and $\overline{Q_1}$

(c) $\overline{Q_1}$ Q_0 and $\overline{Q_0}$ Q_1

(d) $\overline{Q_1 Q_0}$ and $Q_1 Q_0$

Answer :- A

Solution

Given

Q_0	Q_1	Q_0^+	Q_1^+
0	0	1	0
1	0	1	1
1	1	0	1
0	1	0	0

Q_0^+ K Map will be

Q_0 \ Q_1	0	1
0	1	0
1	1	0

$Q_0^+ = \overline{Q_1}$

Q_1^+ K map will be

Q_0 \ Q_1	0	1
0	0	0
1	1	1

$Q_1^+ = Q_0$

Q22. Two D flip-flops are connected as a synchronous counter that goes through the following Q_BQ_A sequence 00 →11 →01 →10 →00. The combination to the inputs D_A and D_B are

(a) $D_A = Q_B;\ D_B = Q_A$

(b) $D_A = \overline{Q_A};\ D_B = \overline{Q_B}$

(c) $D_A = Q_A\overline{Q_B} + \overline{Q_A}Q_B\ ;\ D_B = \overline{Q_A}$

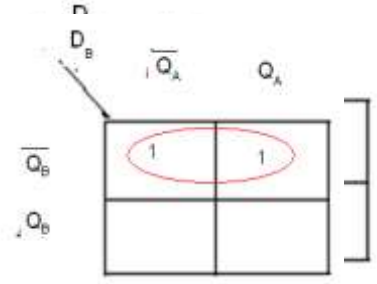
(d) $D_A = Q_AQ_B + \overline{Q_AQ_B}\ ;\ D_B = \overline{Q_B}$

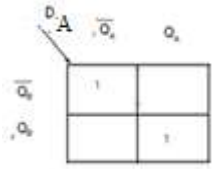
Answer :- D

Solution

Q_B	Q_A	D_B	D_A
0	0	1	1
1	1	0	1
0	1	1	0
1	0	0	0
0	0		

$: D_B = \overline{Q_B}$





$D_A = \overline{Q_BQ_A} + Q_BQ_A$

Answer is D

Q23. The next state table of a 2-bit saturating up counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expression for T1 and T0 respectively are

(a) $T_1 = Q_1Q_0T_0 = \bar{Q}_1\bar{Q}_0$

(b) $T_1 = \overline{Q_1}Q_0T_0 = \bar{Q}_1 + \bar{Q}_0$

(c) $T_1 = Q_1 + Q_0T_0 = Q_1 + \bar{Q}_0$

(d) $T_1 = Q_1Q_0T_0 = \bar{Q}_1 + \bar{Q}_0$

Answer :- B

Solution

Given:

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	0	0

$Q_1^+ = T_1 \oplus Q_1$

$T_1 = Q_1^+ \oplus Q_1$

$Q_0^+ = T_0 \oplus Q_0$

$T_0 = Q_0^+ \oplus Q_0$

K – Map of T_1 & T_0 will be:

$T_1 =$

Q_0 \ Q_1	0	1
0	0	1
1	0	0

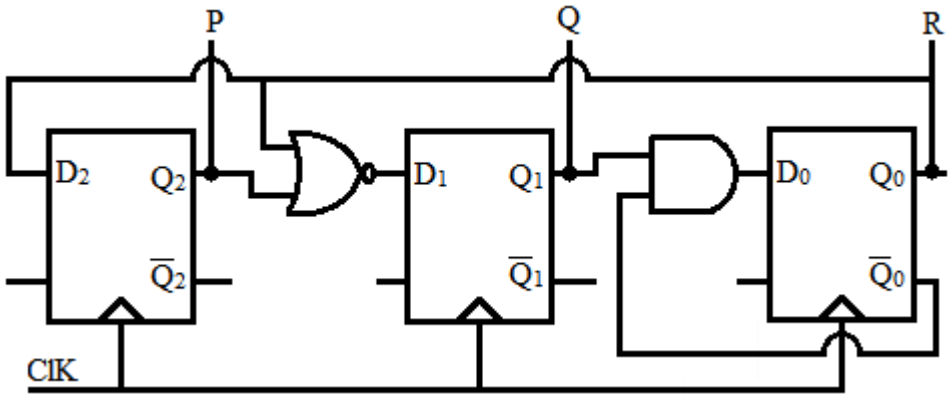
$T_0 =$

Q_0 \ Q_1	0	1
0	1	1
1	1	0

$T_1 = \overline{Q_1}Q_0$ $T_0 = \overline{Q_1} + \overline{Q_0}$

Q24. Consider the following circuit involving three D-type flip-flops used in a certain type of

counter configuration.



If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?_____

Answer :- 4

Solution

Given:

D_2^+ = R

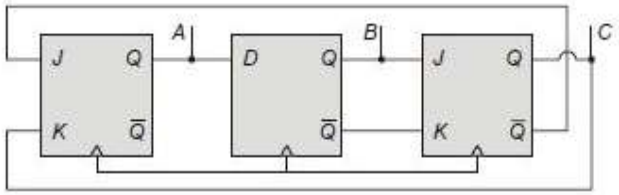
D_1^+ = $\overline{P + R}$

D_0^+ = Q. $\overline{R}$

P	Q	R	D_2^+ = R	D_1^+ = $\overline{P + R}$	D_0^+ = Q. $\overline{R}$
0	0	0	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

PQR has 4 distinct outputs (states).

Q25. Consider the logical circuit shown below:



If initially ABC = 000 then after how many clock pulses the circuit will reach its initial

stage?_____

Answer :- 6

Solution

$J_A = \overline{Qc}$= K_A=Qc

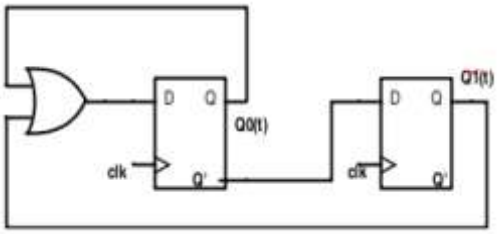
D_B= Q_A , J_C = QB Kc=$\overline{QB}$.

A	B	C
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0

J_A=1	K_A=0	D_B=0	J_C=0	K_C = 1
J_A=1	K_A=0	D_B=1	J_C=0	K_C = 1
J_A=1	K_A=0	D_B=1	J_C=1	K_C = 0
J_A=0	K_A=1	D_B=1	J_C=1	K_C = 0
J_A=0	K_A=1	D_B=0	J_C=1	K_C = 0
J_A=0	K_A=1	D_B=0	J_C=0	K_C = 1

Answer is 6

Q26. For the circuit shown below which of the following is valid transition sequence(Q0Q1)?



(a) 00 →01 →11 →00

(b) 00 →10 →11 →00

(c) 00 →11 →10 →00

(d) 00 →01 →11 →10

Answer :- (d)

Solution

D_0=$Q_0 + Q_1$

D_1 =$\overline{Q_0}$

Q_0	Q_1
0	0
0	1
1	1
0	0

Sequence will be 00→01→11→00

Answer is A

Q27. In a clocked S-R flip flop, R is connected with S through an inverter, the circuit is called

(a) JK flip-flop

(b) T flip-flop

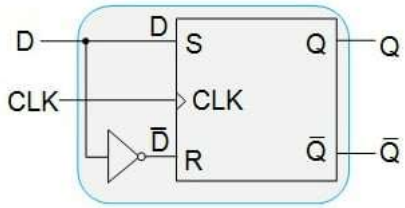
(c) D flip-flop

(d) None of these

Answer :- C

Solution

Solution: In a clocked S-R flip-flop, R is connected with S through an inverter, the circuit is D flip- flop.



SR to D Verification Table

Input	Intermediate Inputs				Outputs	
D	Q	Q̄	S = D	R = D̄	Q	Q̄
0	0	1	0	1	0	1
0	1	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0

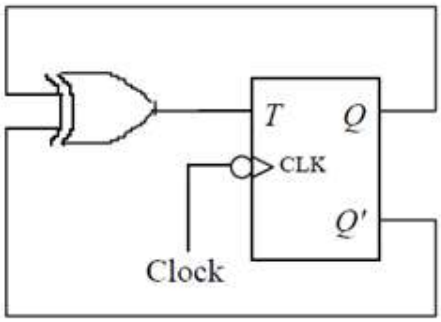
Truth Table of SR Flip-Flop

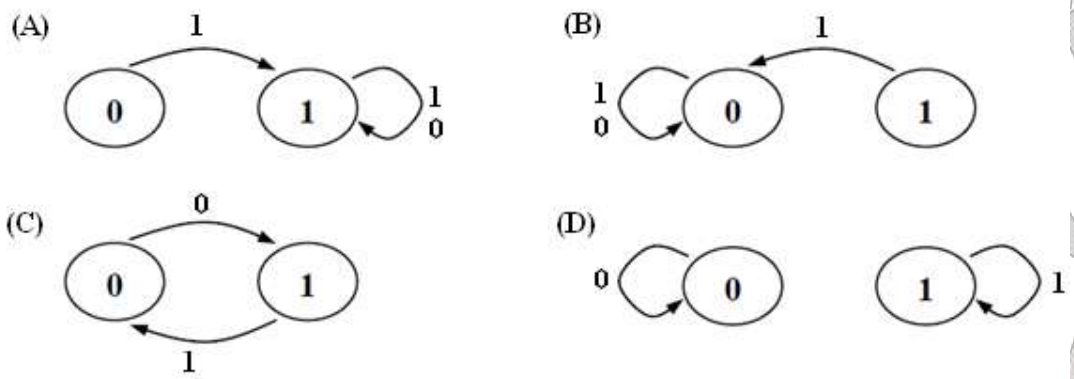
Truth Table of D Flip-Flop

Input	Outputs	
	Present State	Next State
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Answer is C

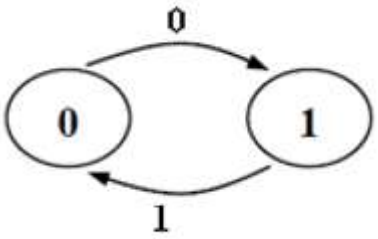
Q28. Given the following sequential circuit consisting of a T flip-flop and an XOR (exclusive-OR) gate,which is its state transition diagram?





Answer :- C

Solution



T (Q⊕ Q`)	Q (t)	Q (t+l)
1	0	1
1	1	0
1	0	1
1	1	0

For the next two questions, consider the following state transition table of a sequential circuit with 2 D flip-flops A and B, and an external input X:

X	Current state A	B	Next state A^+	B^+
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

Q29. Which of the following is the D-input of flip-flop A?

(A) A.B' + A'.B

(B) A.B + A'.B'

(C)A + B

(D)A' + B'

Answer :- A

Solution

A^+

	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{x}$	0	1	0	1
x	0	1	0	1

$\bar{A}B + A\bar{B}$

Q30. [MSQ]

Which of the following is the D-input of flip-flop B?

(A)X

(B)X'

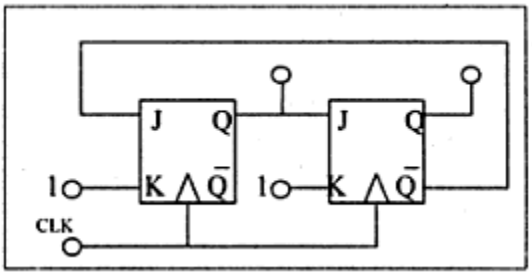
(C) X.A + X'.A'

(D) X.B + X'.B'

Answer :- D

Solution

Q31. Figure shows a mod-K-counter:



The value of K is

(A) 1

(B) 2

(C) 3

(D) 4

Answer :- (c)

Solution

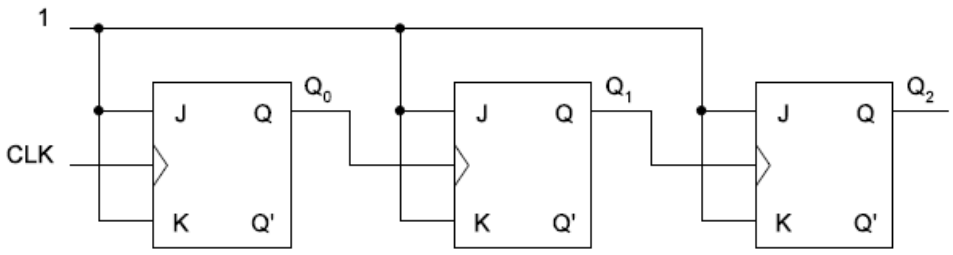
JA = QB′ , KA =1

JB = QA , KB = 1

A	B
0	0
1	0
0	1
0	0

It Is mode 3 counter.

Q32. Consider the following asynchronous counter:



The output sequence of the above counter with initial values of Q0Q1Q2=000 is.

(A) 000, 111, 011, 101, 001, 110, 000

(B) 000, 111, 010, 100, 000

(C) 000, 001, 010, 011, 100, 101, 110, 111, 000

(D) 000, 111, 010, 100, 000

Answer: - None.

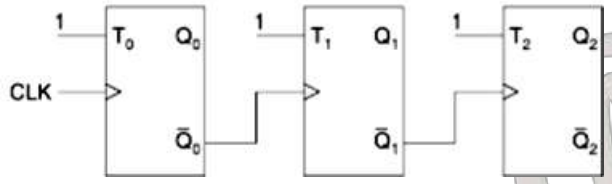
000, 111, 011, 101, 001, 110,010,100, 000

Solution

Given: Counter circuit is Asynchronous.

Q_0	Q_1	Q_2	Q_0^+	Q_1^+	Q_2^+
0	0	0	1	1	1
1	1	1	0	1	1
0	1	1	1	0	1
1	0	1	0	0	1
0	0	1	1	1	0
1	1	0	0	1	0
0	1	0	1	0	0
1	0	0	0	0	0

Q33. The given Figure shows a ripple counter using positive edge triggered flip flops. If the present state of the counter is $Q_2\ Q_1\ Q_0$= 011 then its next state ($Q_2\ Q_1\ Q_0$) will be



(a) 010 (b) 100 (c) 111 (d) 101

Answer :- B

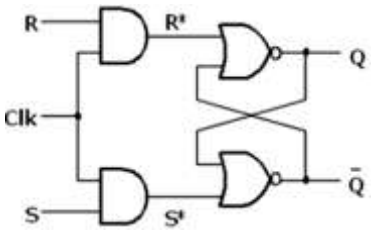
Solution

T_1 changes when T_0 changes from 1 to 0

T_2 changes when T_1 charges from 1 to 0

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1

Q34. Which of the following is the correct truth for the gated SR flip flop circuit shown?



(a)

Clk	S	R	Q(t+1)
0	X	X	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	X

(b)

Clk	S	R	Q(t+1)
0	X	X	Q(t)
1	0	0	0
1	0	1	1
1	1	0	Q(t)
1	1	1	X

(c)

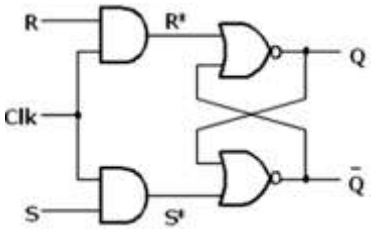
Clk	S	R	Q(t+1)
0	X	X	Q(t)
1	0	0	Q(t)
1	0	1	1
1	1	0	0
1	1	1	X

(d)

Clk	S	R	Q(t+1)
0	X	X	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q(t)}$

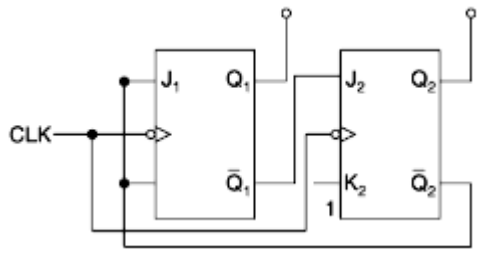
Answer :- A

Solution



clk	S	R	Q_t	Q_{t+1}
0	×	×	0	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	×	×

Q35. The output sequence (Q_1Q_2) produced by the following counter circuit is



(a) $00 \rightarrow 11 \rightarrow 10 \rightarrow 00$

(b) $00 \rightarrow 11 \rightarrow 01 \rightarrow 00$

(c) $00 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00$

(d) $00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00$

Answer :- A

Solution

Given, $J_1 = K_1 = \overline{Q_2}$

$J_2 = \overline{Q_1}$ $K_2 = 1$

$Q_1^+ = J_1\overline{Q_1} + \overline{K_1}Q_1$

$= \overline{Q_2Q_1} + \overline{\overline{Q_2}}\, Q_1 \Rightarrow Q_2 \odot Q_1$

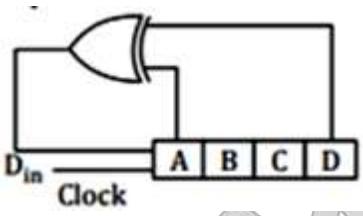
$Q_2^+ = J_2\overline{Q_2} + \overline{K_2}Q_2$

$= \overline{Q_1Q_2} + 0 \Rightarrow \overline{Q_1 + Q_2}$

Q_1	Q_2	Q_1^+	Q_2^+
0	0	1	1
1	1	1	0
1	0	0	0

Sequence $00 \rightarrow 11 \rightarrow 10 \rightarrow 00$

Q36. A 4-bit shift register circuit configured for right-shift operation is $D_{in} \rightarrow A$, $A \rightarrow B$, $B \rightarrow C$, $C \rightarrow D$, is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 is_____



Answer :- 10

Solution

$A^+ = A \oplus D$

$B^+ = A$

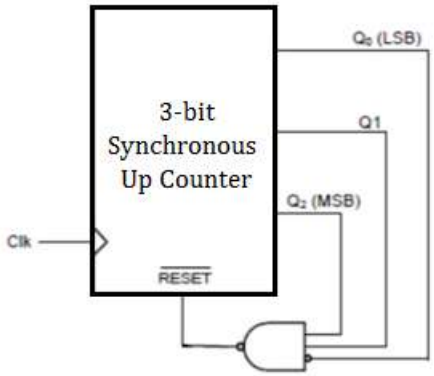
$C^+ = B$

$D^+ = C$

A	B	C	D		A^+	B^+	C^+	D^+
1	1	0	1	1ST →	0	1	1	0
0	1	1	0	2ND →	0	0	1	1
0	0	1	1	3rd →	1	0	0	1
1	0	0	1	4TH →	0	1	0	0

0	1	0	0	5TH →	0	0	1	0
0	0	1	0	6TH →	0	0	0	1
0	0	0	1	7TH →	1	0	0	0
1	0	0	0	8TH →	1	1	0	0
1	1	0	0	9TH →	1	1	1	0
1	1	1	0	10TH →	1	1	1	1

Q37. For the circuit shown in the figure, the delay of the bubbled NAND gate is 2ns and that of the counter is assumed to be zero.



If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

(a) mod-5 counter (b) mod-6 counter

(c) mod-7 counter (d) mod-8 counter

Answer :- D

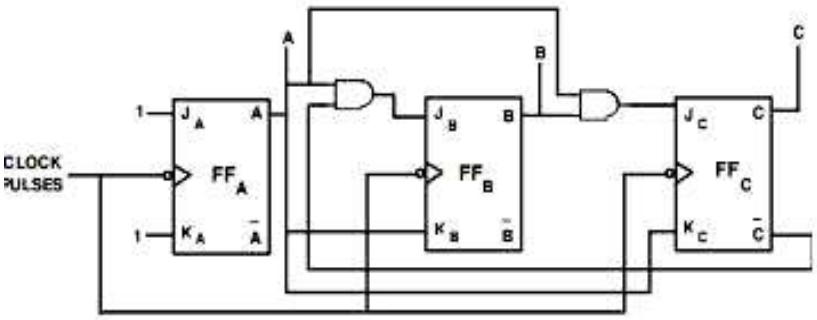
Solution

Clk	Q2	Q1	Q0	o/p of NAND	Q_2^+	Q_1^+	Q_0^+
-	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
2	0	1	0	1	0	1	1
3	0	1	1	1	1	0	0
4	1	0	0	1	1	0	1
5	1	0	1	1	1	1	0
6	1	1	0	0	0	0	0

If delay Of NAND gate is 0 then given circuit acts like mod-6 counter. But Here delay of NAND is 2ns so it will count two more clock before it resets the counter (∴ clock period =1 ns, gate delay =2ns)

∴ so the given counter acts like Mod-8 counter

Q38. Consider the following circuit with A as the MSB



The output after the 4th clock pulse is ____, if initial state is 110.

Answer :- 100

Solution

Given # $J_A = K_A = 1$

$A^+ = J_A\overline{Q_A} + \overline{K_A}Q_A$

$A^+ = \bar{A}$

$J_B = A\bar{C}$, $K_B = A$

$B^+ = J_B\overline{Q_B} + \overline{K_B}Q_B$

$B^+ = A\bar{C}\bar{B} + \bar{A}B$

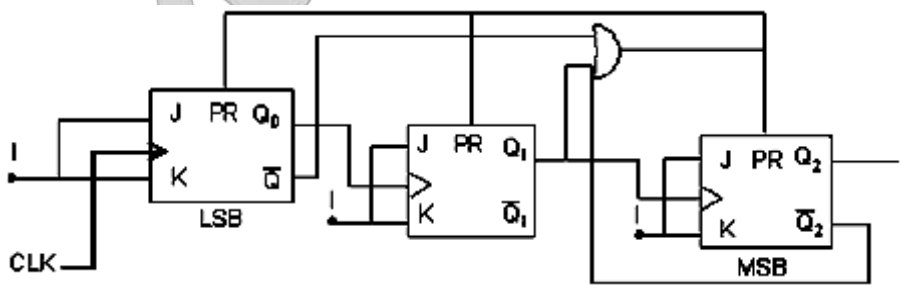
$J_C = AB$, $K_C = A$

$C^+ = J_C\overline{Q_C} + \overline{K_C}Q_C$

$C^+ = AB\bar{C} + \bar{A}C$

A	B	C		A^+	B^+	C^+
1	1	0	1st →	0	0	1
0	0	1	2nd →	1	0	1
1	0	1	3rd →	0	0	0
0	0	0	4th →	1	0	0

Q39. The Ripple counter shown in the figure works as a



(a) Mod 3 up counter

(b) Mod 5 up counter
(c) Mod 3 down counter
(d) Mod 5 down counter

Answer :- (d)

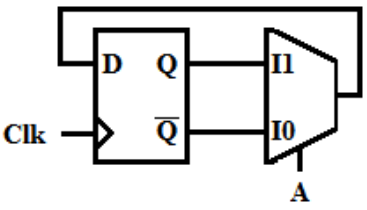
Solution

Given circuit is Asynchronous counter in which
Q_1 Changes when Q_0 changes from 0 to 1.
Q2 changes when Q_1 changes from 0 to 1.

Q0	Q1	Q2
1	1	1
0	1	1
1	0	1
0	0	1
1	1	0
0	1	0

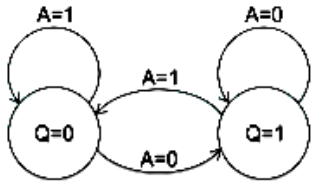
It is mod-5 down counter.

Q40. Consider the following circuit:

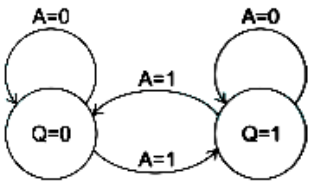


The state transition diagram for the circuit shown is

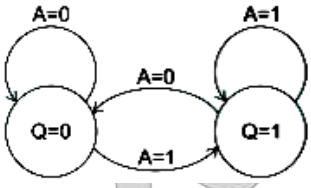
(a)



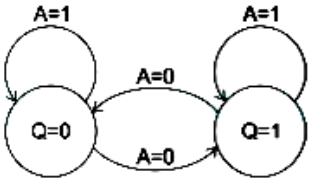
(c)



(b)



(d)



Answer :- D

Solution

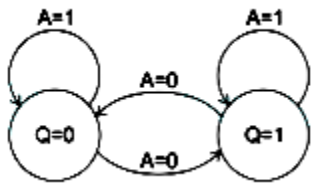
By given circuit diagram

$D = QA + \overline{Q}\overline{A}$

$D = Q \odot A$

$\therefore$ $Q^+ = R \odot A$

Q_n	A	Q_{n+1}
0	0	1
0	1	0
1	0	0
1	1	1



∴Correct answer is (d)

Time :40 min **Digital Test-1** **Marks:50**

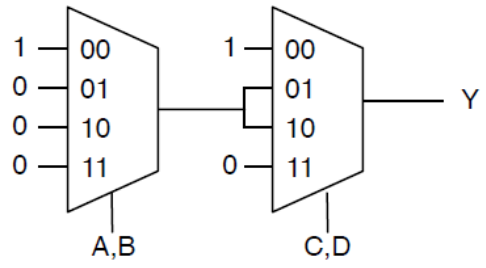
Q1. Given the function $F(A,B,C,D) = \Sigma m(0, 2, 5, 8, 10, 15)$. How many *prime implicants* are there in its K- map?

(A)6 (B) 5 (C)4 (D)3

Q2. Given the function $G(A,B,C) = \Sigma m(1,3) + d(4,5,6,7)$. What is the *minimum number of gate* that can be used to implement this function?

(A)0 (B)1 (C)2 (D)3

Q3. Which of the following Boolean expression represents the function performed by the following circuit?



(A)C`D`+A`B`(C⊕D) (B)A`B`+C`D`+C⊕D(C)A`B`+C`D` (D)A`B`C`D`

Q4. A Boolean expression $f(x\ y,z) = xyz + x\ \bar{y}\ z + \bar{x}y\bar{z} + xy\bar{z}$ will reduce to