Counter

1 FF used for 1 bit counter
n FF " " n bit counter

$2^n \geq M$

n ← no. of FF
2^n → no. of States
M → mod number

#Note: no. bit in highest state of counter = no. of FF used

#Note: any of one output of FF, frequency will be divided by the M number of counter.

#Note: at least 1 FF have output repeating clock Pattern

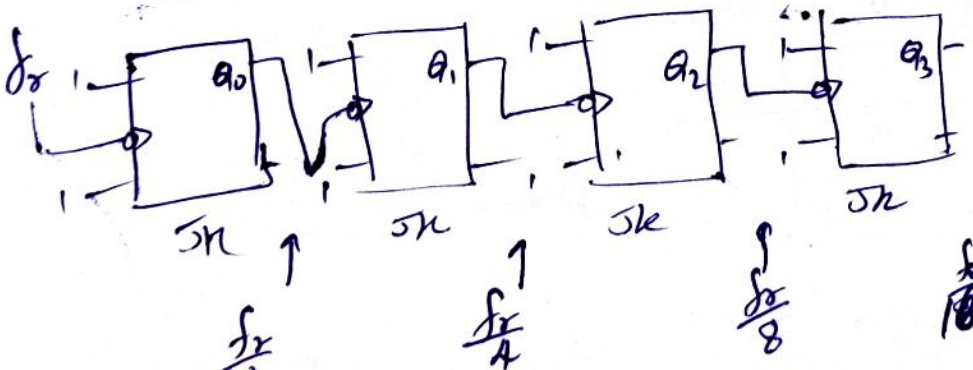
Async.

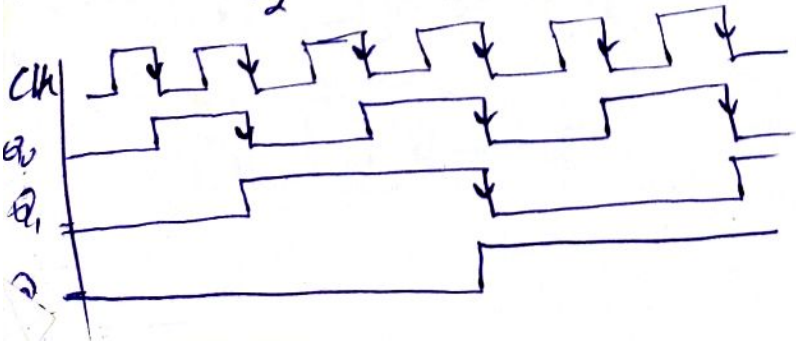
① Every FF have different clock with different freq.
② Delays are more
③ Sequence → up (1→2→3)
→ Down (3→2→1)
④ Decoding Error (can't be removed) (Essential Hazards)

Sync.

① All FF have same clock
② Delays are less
③ any sequence possible
④ no decoding error

4-bit - async counter





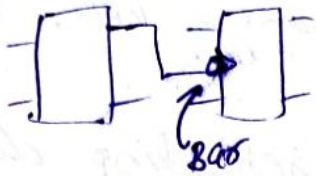
How to identify MSB & LSB Bit in Asyc counter

① Identify that counter is async or Sync.

② for all case FF in which clock is directly, is LSB

③

if there is one Bar in any of input. It is up counter

e.g 

One bar → up counter

0 or 2 bar → down counter

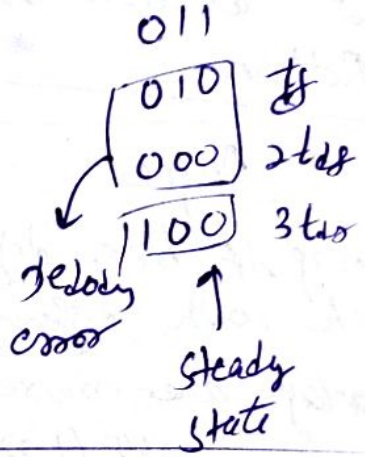
Decoding Error

$T_{clk} \geq n \cdot t_{dff}$ ← delay of FF

$\Rightarrow f_s \leq \frac{1}{n \cdot t_{dff}}$

n = no. of FF

f_s = clock time

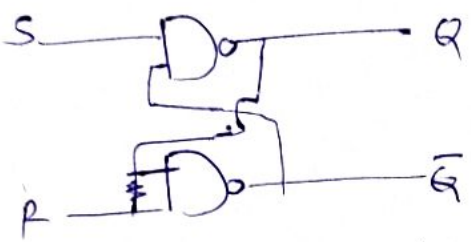


Note:- Don't count state in asyn counter if not exist till complete time period.

Note: frequency got by 2 by T-flip-flop

Subject- DLD
Topic- Sequential Ckt
type- Notes (generic education youtube)

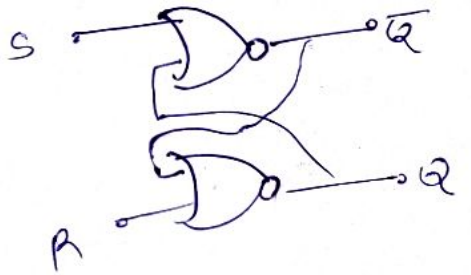
NAND LATCH



S	R	Q(n+1)
0	0	Invalid
0	1	1
1	0	0
1	1	(no-change) (hold) Q_n

Note NAND one any input 0 produces 1
eg $A \uparrow B \Rightarrow \boxed{A \uparrow 0 = 1}$

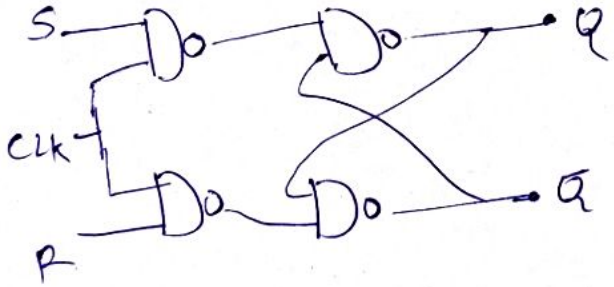
NOR LATCH (S-R LATCH)



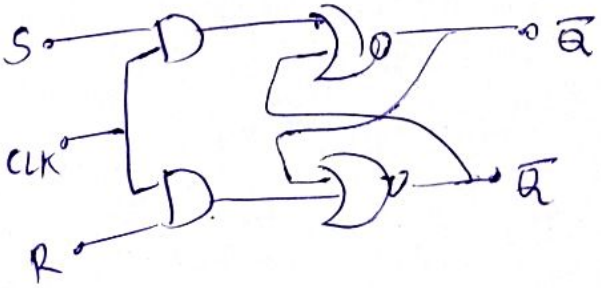
S	R	Q
0	0	~~Invalid~~ (hold) Q_n
0	1	0 (0)
1	0	1 (1)
1	1	~~(halt)~~ Invalid

Proper 2
$A \downarrow 1 = 0$
$\boxed{0 \downarrow 0 = 1}$

SR flip flop



CLK	S	R	Q(n+1)
Not trig.	x	x	Q(n)
trig	0	0	Q(n)
"	0	1	0
"	1	0	1
"	1	1	Invalid



characteristic table

$\boxed{Q(n+1) = S + \bar{R}Q(n)}$