3 Computer Organization & Architecture

Practice Questions

Q.1 Consider a system with byte addressable main memory and size of all instructions are 32 bit.

Consider following instructions:

ADD R_1, A // $R_1 = R_1 + \text{Mem}[A]$

Where R_1 is register and A is a memory address and Mem[A] is reading value of memory address A. This instruction stored at memory location 2460 H and A is a memory location with address 4408 H, both are in hexadecimal notation.

What are the values of Program Counter (PC) and Memory Address Register (MAR) during execution of this instruction but after calculating effective address?

(A) PC = 2464 H, MAR = 4408 H

(B) PC = 2460 H, MAR = 440C H

(C) PC = 2464 H, MAR = 440C H

(D) PC = 2460 H, MAR = 4408 H

Q.2 Consider the following table for two systems A and B :

	Word size	**Main Memory (MM)**	**Addressability**
System A	4 bytes	4 GB	Byte addressability
System B	4 bytes	16 GB	Word addressable

x and y are number of bits used to represent address of a memory location in system A and B respectively. Value of x and y are

(A) $x = 32, y = 32$

(B) $x = 32, y = 34$

(C) $x = 30, y = 32$

(D) $x = 34, y = 34$

Q.3 What is the use of Program Counter (PC) in a system?

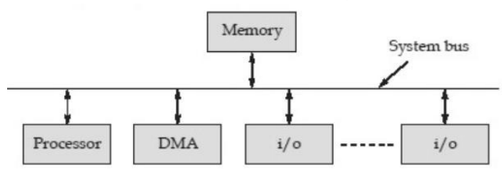
(A) PC contains address of the next instruction to be executed.

(B) PC contains address of current instruction that is being executed.

(C) PC is number of processes running in a system at a particular instance.

(D) PC contains effective address that calculated for operand of current executing instruction.

Q.4 Below diagram shows single bus detached DMA configuration of a system. How many times system bus used for a single data transfer using DMA (consider only data transfer, not command or status transfer).



(A) 1 (B) 2
(C) 3 (D) 0

Q.5 Consider a system with 4 GB main memory with word size of 32 bits. Main memory is half word addressable. Then size of Memory Address Register (MAR) and Memory Data Register (MDR) for this system are respectively.

(A) 32 bits, 30 bits
(B) 31 bits, 32 bits
(C) 32 bits, 31 bits
(D) 30 bits, 32 bits

Q.6 A hard disk has 32 recording surfaces, 256 cylinders, 512 sectors per track and sector size is 1 KB. Find the total size of this hard disk in GB _____.

(Rounded of upto 1 decimal place)

Q.7 Consider a system with 32 bit physical address has data cache of size 16 Kbytes. Cache block size is 256 bytes. Cache is using fully associative mapping. x is tag field length in bits and y is set field length in bits for this cache system. Find value of $x - y$ _____.

Q.8 Which input/output uses interrupts to take attention of CPU/processor?

[MSQ]

(A) Programmed input/output
(B) Interrupt driven input/output
(C) Direct memory access (DMA)
(D) None of the above

Q.9 For a cache memory system, if we change the cache block size then in which of the following cache mapping method the tag field length cannot change.

[MSQ]

Assume, after change in the block size the number of sets in direct mapped and k associative cache must be greater than 1.

(A) Direct mapped cache
(B) k associative cache
(C) Fully associated cache
(D) None of the above

Q.10 A hard disk has 100 cylinders, 16 recording surfaces, 32 sectors per track and 512 bytes per sector. Address of a byte is represented by <c, s, r, b>, where c is cylinder number, s is surface, r is sector number and b is byte number. Thus, 0th byte represented as <0, 0, 0, 0>. 1st byte represented as <0, 0, 0, 1 > and so on. The head of disk starts reading the disk sequentially from <0, 0, 0, 0> and reached at <8, 8, 16, 127>. How many bytes have the head read, including the byte with address <8, 8, 16, 127>.

(A) $2^{21} + 2^{16} + 2^{13} + 128$ bytes
(B) $2^{21} + 2^{17} + 2^{12} + 127$ bytes
(C) $2^{20} + 2^{17} + 2^{12} + 128$ bytes
(D) $2^{21} + 2^{17} + 2^{13} + 128$ bytes

Q.11 A system has 4 GB byte-addressable main-memory and 128 Kbytes data cache memory with block size of 64 bytes. Tag field length is 16 bits in cache. Which of the following cache mapping used in this system?

(A) Direct mapped
(B) 2-way set associative
(C) 4-way set associative
(D) Fully associative

Q.12 Let R_1, R_2 and R_3 are 4 bit registers in a system. $R_1 - 0011$ and $R_2 - 0101$ in 2's complement binary format. System execute following instruction

SLT R_3, R_1, R_2

where SLT is 'set less than' operation in which $R_3 = 0001$ if $R_1 < R_2$ else $R_3 = 0000$, values in 2's complement binary number. What are the values of states bits overflow (V), zero (Z), negative (N) and half carry (H) after executive above instruction? Assume system uses 2's complement addition and subtraction.

(A) $V = 0, Z = 0, N = 1, H = 0$

(B) $V = 0, Z = 1, N = 1, H = 0$

(C) $V = 1, Z = 1, N = 0, H = 1$

(D) $V = 1, Z = 0, N = 1, H = 0$

Q.13 Consider 4 ns CLK cycle processor which consumes 6 cycles for data transfer, 8 cycles for ALU and 4 cycles for branch instructions. Relative frequencies of these instructions are 40%, 30% and 30% respectively. What is the average instruction execution time?

(A) 20 ns (B) 6 ns

(C) 4 ns (D) 24 ns

Q.14 A system has L_1 and L_2 cache with access time of 10 ns and 100 ns respectively. Main memory access time is 1 μs. Miss rates of L_1 and L_2 are $\frac{1}{100}$.

Find average memory access time for this system in ns. (Rounded upto one decimal place)

Q.15 A disk has seek time of 50 ms, 64 sectors per track, 512 bytes per sector and rotate at 600 rounds per minute. A file of size 48 Kbytes sequentially stored in two consecutive adjacent tracks, but starting point of file on both tracks can be anywhere on tracks. Negligible time spend on moving from one track to its adjacent track. Find the average time required to access and read the whole file in ms?

Q.16 Consider two systems A and B, each system contains byte addressable main memory of size 4 GB and "2-way set associative" cache memory of size 128 KBytes. System A has cache block of size 128 bytes and system B has cache block of size 256 bytes. x is difference of tag field lengths of system A and B. y is difference of set field lengths of system A and B. Find value of x and y?

[MSQ]

(A) $x = 0$ (B) $y = 1$

(C) $x = 1$ (D) $y = 0$

Q.17 A system with 8 blocks of cache memory which is 2 way set associative mapped. Cache memory using LRU replacement algorithm. A process referencing following main memory blocks in given order :

[MSQ]

10, 11, 12, 18, 5, 11, 6, 7, 10, 15, 11, 5

Assume cache is initially empty. Which of the following is/are true?

(A) 4 conflict misses

(B) 8 compulsory misses

(C) 0 capacity misses

(D) 2 hits

Q.18 Which of the following is/are correct?

[MSQ]

(A) Little-endian versus big-endian comes into play when the memory is word-addressable and an integer sits completely in one byte.

(B) Little-endian versus big-endian comes into play when the memory is byte-addressable and an integer spans multiple bytes.

(C) The issue of which "endian" type(big or little) the computer uses becomes critical when the memory assigns a separate address to each byte.

(D) The issue of which "endian" type(bog or little) the computer uses becomes critical when the memory assigns a separate address to each word.

Q.19 Consider the following PC-relative addressing mode instruction of RISC instruction set architecture.

I_1 :

$1000 : \text{BEQ } R_1, R_2, \text{label}$

I_2 :

$1004 : \text{ADD } R_1, R_2, R_3$

Where the label is used as an offset and 1000 is the memory location from where instruction I_1 is fetched. $R_1, R_2,$ and R_3 are general purpose registers.

The BEQ instruction branches the PC if the first source register's contents and the second register's contents are equal.

If $R_1 = 0; R_2 = 0$ and label $= 20,$ what is the memory address of the next instruction to be executed?

Q.20 A digital computer has a memory unit with 32 bits per word. The instruction set consists of 110 different operations. All instructions have an operation code part (opcode) and two address fields: one for a memory address and one for a register address. This particular system includes eight general-purpose, user-addressable registers. Registers may be loaded directly from memory, and memory may be updated directly from the registers. Direct memory-to-memory data movement operations are not supported. Each instruction is stored in one word of memory, If X, Y, Z represent the number of bits that are needed for the opcode, for the register field, and bits that are left for the memory address part of the instruction, respectively, then $XY + YZ$ is

_____

Q.21 The unsigned integer 3, 505, 468, 161 can be written in 32-bit binary as 11010000 11110001 00110011 00000001. Putting it into four bytes of memory beginning at address 98370 in little-endian fashion would give which picture?

(A)

98370	98371	98372	98373
11010000	11110001	00110011	00000001

(B)

98370	98371	98372	98373
00000001	11110001	00110011	11010000

(C)

98370	98371	98372	98373
00000001	00110011	11110001	11010000

(D)

98370	98371	98372	98373
00110011	00000001	11010000	11110001

Q.22 When performing hardware integer arithmetic, we say that overflow has occurred when the mathematically correct result of a computation cannot be represented in the number of bits available for the type being used. Obviously, it is important to be able to detect when an overflow error has occurred. **[MSQ]**

For the following options, the bit-sequences are 16-bit 2's complement representations of (signed) integer values. For which of the following an overflow occurs when the given two integers are added?

(A) 0111 1001 1011 1011 + 0011 1011 1110 1110

(B) 1111 0111 0110 1001 + 1000 0001 0110 0100

(C) 0001 1100 0110 1111 + 1111 0111 1110 1101

(D) 1100 1011 1010 1101 + 0111 1111 0010 1111

Q.23 A CPU has an arithmetic unit that adds bytes and then sets its *V*, *C*, and *Z* flag bits as follows. The *V*-bit is set if arithmetic overflow occurs (in two's complement arithmetic). The *C*-bit is set if a carry-out is generated from the most significant bit during an operation.

The *Z*-bit is set if the result is zero.

What are the values of the *V*, *C*, and *Z* flag bits (in that order) after the 8-bit bytes 1100 1100 and 1000 1111 are added?

(A) 000 (B) 110

(C) 111 (D) 001

Q.24 Consider the following :

Consider the instruction Load $R_5, X(R_7)$ which uses the Index addressing mode to load a word of data from memory location $X + [R_7]$ into register R_5.

Execution of this instruction involves the following actions :

- (I_1) Fetch the instruction from the memory.
- (I_2) Decode the instruction to determine the operation to be performed.
- (I_3) Add the immediate value X to the contents of R_7.
- (I_4) Read register R_7.
- (I_5) Use the sum $X + [R_7]$ as the effective address of the source operand, and read the contents of that location in the memory.
- (I_6) Increment the program counter.
- (I_7) Load the data received from the memory into the destination register, R_5.

Which of the following is the most preferred order of execution of the above instruction?

(A) $I_1 \rightarrow I_2 \rightarrow I_3 \rightarrow I_4 \rightarrow I_5 \rightarrow I_6 \rightarrow I_7$

(B) $I_1 \rightarrow I_2 \rightarrow I_6 \rightarrow I_3 \rightarrow I_4 \rightarrow I_5 \rightarrow I_7$

(C) $I_1 \rightarrow I_6 \rightarrow I_2 \rightarrow I_4 \rightarrow I_3 \rightarrow I_5 \rightarrow I_7$

(D) $I_1 \rightarrow I_6 \rightarrow I_2 \rightarrow I_5 \rightarrow I_4 \rightarrow I_3 \rightarrow I_7$

Q.25

	Micro-operations	Active Control Signals
	t_1 : MAR ← (PC)	C_2
Fetch :	t_2 : MBR ← Memory	C_5, C_R
	PC ← (PC) + 1	
	t_3 : IR ← (MBR)	C_4
	t_1 : MAR ← (IR (Address))	C_8
Indirect :	t_2 : MBR ← Memory	C_5, C_R
	t_3 : IR (Address) ← (MBR(Address))	C_4
	t_1 : MBR ← (PC)	C_1
Interrupt :	t_2 : MAR ← Save-address	
	PC ← Routine-address	
	t_3 : Memory ← (MBR)	C_{12}, C_W

$C_R =$ Read control signal to system bus.

$C_W =$ Write control signal to system bus.

Let us define control signals, P and Q, that have the following interpretation

- $PQ = 00$ Fetch cycle
- $PQ = 01$ Indirect cycle
- $PQ = 10$ Execute cycle
- $PQ = 11$ Interrupt cycle

Which of the following expression boolean expression defines C_4 ?

(A) $P't_3$

(B) $Pt_3^{'} + Q't_3$

(C) $P'Q't_3 + PQ't_3$

(D) $P'Q't_3 + PQt_3$

Q.26 The 8-bit registers M, N, O and P initially have the following values.

M = 10001111; N = 01100010; O = 01001001; P = 01110010

The following assembly code is executed :

- $M \leftarrow M \oplus N$
- $M \leftarrow CSL\, M$
- $N \leftarrow M + N$
- $O \leftarrow O \wedge N$
- $O \leftarrow CSR\, O$
- $P \leftarrow P + 1$
- $P \leftarrow P + 0$

Determine the 8-bit values in each register after the execution of the above sequence of micro-operations.

CSL : Circular shift left: CSR : Circular shift right; A : logical AND; + : Arithmetic addition 0 : logical Ex-or.

(A) M = 11101101; N = 00111101; O = 10000100; P = 11110111

(B) M = 11011011; N = 00111101; O = 10000100; P = 11110111

(C) M = 11011011; N = 10111101; O = 10000100; P = 11110111

(D) M = 11011011; N = 00111101; O = 00001001; P = 01110011

Q.27 A particular parallel program computation requires 100 seconds when executed on a single processor. If 40 percent of this computation is "inherently sequential" (i.e., will not benefit from additional processors), then the theoretically best possible elapsed times for this program running with 2 and 4 processors, respectively, are

(A) 20 seconds and 10 seconds

(B) 50 seconds and 25 seconds

(C) 70 seconds and 55 seconds

(D) 80 seconds and 70 seconds

Q.28 A 64-bit processor has 64 registers and uses a 20-bit instruction format. It has two types of instructions: M-type and R-type. Each M-type instruction contains an opcode and a memory address. Each R-type instruction contains an opcode and two register names. Main memory is 8K words, and it is byte addressable. If there are 10 distinct M-type opcodes, then the maximum number of distinct R-type opcodes is _____

Q.29 Amdahl's Law pertains to the speedup achieved when running a program on parallel processors versus using a single serial processor. In this context, the speedup is the ratio of original running time to improved running time. According to Amdahl's Law, approximately how much speedup could we expect for an unlimited number of processors if 10 percent of a program is sequential i.e., will not benefit from additional processors) and the remaining part is ideally parallel?

(A) $10X$ (B) $20X$

(C) $40X$ (D) Infinite

Q.30 Following is a definition of a widget and a declaration of an array A that contains 10 widgets. The sizes of a byte, short, int, and long are 1, 2, 4 and 8 byte, respectively. Alignment is restricted so that an *n*-byte field must be located at an address divisible by *n*.

The fields in a struct are not rearranged; padding is used to ensure alignment. All widgets in A must have the same size.

1. struct widget
2. short *s*
3. byte *b*
4. long *l*
5. int *I*
6. end widget
7. widget *A*[10]

Assuming that *A* is located at a memory address divisible by 8, what is the total size of *A*, in bytes?

(A) 150 (B) 160

(C) 2001 (D) 240

Q.31 Consider two different design enhancements of ALU as follows :

i. A part of a bigger task is improved twenty times than it was before. The other part of the same task constitutes 60% of the overall task time, and it remains unchanged.

ii. The designer can make changes to improve 20% of the task 100% faster, 35% of the task 4 times faster, and 10% of the task 100 times faster, but it causes the remaining part of the task to perform as bad as 50% slower than before.

Which of the following value is the best approximate difference between the two speedups achieved in those two improvements :

(A) 0.3567 (B) 0.2667

(C) 0.4875 (D) 0.4325

Q.32 Big-Endian(BE) and Little-Endian(LE) change the order in which the bytes of a word are stored in RAM. We typically show the contents of a word, especially if it's an integer, as four hexadecimal pairs of characters. For example, the hex string $0\times abcdef12$ contains four bytes: "*ab*" is the first, which have the binary value of 1010 and 1011. So the first 8 bits are 10101011. BE/LE specifies whether this byte goes into RAM as the first of the four bytes in the word or as the last. Suppose Byte 0 in RAM contains the value 0×00. Subsequent bytes contain $0\times01, 0\times40$ and 0×70. On a Big-Endian system with a 32-bit word, what's the decimal value of the word?

Q.33 Consider the control unit that adopts the single address field branch control logic. Assume that the control memory is 24 bits wide. The control portion of the micro-instruction format is divided into two fields. A micro-operation field of 13 bits specifies the micro operations to be performed. An address selection field specifies 8 conditions that will cause a micro-instruction branch.

[MSQ]

Which of the following is true?

(A) 8 bits are in the address field

(B) 8 bytes are in the address field

(C) the size of the control memory is 768 Bytes

(D) the size of the control memory is 4096 bits.

Q.34 Let x and y are represented in singed 2's complement notation with 8 bit. The correct statement in the given below is/are **[MSQ]**

(A) Overflow occurs after adding $x=(94)_{16}$ and $=(79)_{16}$

(B) Overflow does not occurs after adding $x=(94)_{16}$ and $y=(79)_{16}$

(C) Overflow occurs after subtracting $x=(79)_{16}$ from $y=(94)_{16}$

(D) Overflow does not occur after subtracting $x=(79)_{16}$ from $y=(94)_{16}$

Q.35 For adding 2 number of singed data with the available size, let first data size is m bits and second data size in n bits, $(m>n)$ to get the target result

[MSQ]

(A) Size of m and n should be same

(B) The longest result size is $(m+n)$ bits

(C) The longest result is $m+1$ bits

(D) The longest result size is $n+1$ bits

Q.36 Consider a disk pack with a average seek time of 3 millisecond and rotational speed of 12000 RPM. It has 100 sectors/track and 1K Bytes/sector. A file contains 20 sectors stored in the disk. Assume that every sector access requires one average seek time, one average rotational delay and data transfer (RD/WR) time. The total time needed to read entire file is _____ milliseconds.

Q.37 A cache memory access time is 10 ns and main memory access time is 100 ns. The hit rate for read operation is 90%. In total memory references, 70% are used for read operations with write through technique. The average memory access time is _____ns.

Q.38 A system is designed with direct mapped cache wit capacity of 128 KB and each block size is 512 Bytes. The processor generates 24 bit physical address (Note word size = one byte)

[MSQ]

(A) Tag field size in each cache line is 7 bits

(B) Total Tag directory size is 1792 bits

(C) No. of blocks available in cache memory is 256

(D) IN this conflict miss does not occur when the CPU requires the same words repeatedly

Q.39 Let the given data in variable format and it is in signed 2's complement notation; the decimal value of n bit size 'x' value is p $\left(x_{n-1}x_{n-2}.....x_2x_1x_0\right)_2 = P$

The decimal value of 'P' is

(A) $\sum_{i=0}^{n-1} a_i \times 2^i$

(B) $\sum_{i=0}^{n-2} a_i \times 2^i + \left\{(-1)\left[x_{n-1}\right] \times \left(2^{n-1}\right)\right\}$

(C) $\sum_{i=0}^{n-2} a_i \times 2^i + \left\{(-1)\, x_{n-1} \times 2^{n-1}\right\}$

(D) $\sum_{i=0}^{n-2} a_i \times 2^i + \left\{(-1) * \left(x_{n-1}\right) \times \left(2^{n-2}\right)\right\}$

Q.40 A 16 bit resister is used to represent floating data with biasing value of 64, one bit (MSB) in the resister is reserved for representing the sign of the mantissa; next field to MSB in used to represent Biased exponent and last field is used to represent the mantissa in signed magnitude form. The no. of bits needed to represent Biased exponent field and mantissa field respectively are

(A) 7, 8 (B) 8, 7

(C) 6, 9 (D) 9, 6

Q.41 A magnetic hard disk is having 16 surface, 1024 Track/surface; 256 sectors/track and 64 Bytes/sector. It is operated with the RPM of 'x' average latency is 5 milliseconds, the 'x' value is_____.

Q.42 In the given below, the single conflict miss does not occur in

(A) Fully associative mapped cache

(B) Direct mapped cache

(C) 4 way block set associative

(D) 16 way block set associative mapped cache

Q.43 A direct mapped cache size is 64 KB and each cache line size is 256 byte and CPU generates 20 bit memory address. The 2049 addressed work of main memory maps to the cache line of

(A) CL_a (cache line 8)

(B) CL_1 (cache line 1)

(C) CL_{255} (cache line 255)

(D) None of the above

Q.44 One magnetic surface is having 1024 tracks $\left(T_0 \text{ to } T_{1023}\right)$, each track has 64, $\left(S_0 \text{ to } S_{63}\right)$ sectors with 16 bytes $\left(B_0 \text{ to } B_{15}\right)$ in each sector. Let starting word address in the surface is (00000) H and last word address is (FFFFF) h. Find the correct statement in the given below

[MSQ]

(A) $(\text{FFC0F})_{16}$ Address byte is in S_{63} sector

(B) $(\text{FFC0F})_{16}$ Address byte is in S_0 sector

(C) $(003F2)_{16}$ Addressed byte in S_0 sector

(D) $(003F2)_{16}$ Addressed byte is in S_{63} sector

Q.45 The size of the ROM required for storing the truth table for 16 for squarer operation is____ kilo bytes.

Q.46 Let 0 X F F F E 0 0 0 0 is represented in IEEE single precision notation with biasing value of 127. It represents

(A) Decimal value –17.725

(B) Decimal value –29.775

(C) Not a number (special value)

(D) ± Infinitive (special value)

Q.47 Consider the three floating point number P, Q and R stored in Registers R_P, R_Q, R_R respectively as per IEEE – 754 single precision floating point format. The 32 bit contact stored in these registers (in Hexa decimal) are as follows.

$R_P = \text{C1D00000}$, $R_Q = \text{C1600000}$,

$R_R = 41\text{D00000}$

Which one of the following is false?

(A) $R = P + Q$ (B) $R > Q$

(C) $P + R = 0$ (D) $R + Q = 12$

Q.48 To implement a $64\text{ K} \times 8$ bit memory with $16\text{ K} \times 4$ bit chips

[MSQ]

(A) Total no. of 16×4 bit chips needed is '4'

(B) Total no. of $16\text{ K} \times 4$ bit chips needed is '8'

(C) 2×4 size row chip select decoder is needed

(D) 3×8 size row chip select decoder is needed

Q.49 In the given below, the correct statements is/are

[MSQ]

(A) Index register addressing mode instruction is faster than immediate addressing mode instruction

(B) Memory cycle is not needed for operand reading while executing the register addressing mode instruction. Memory indirect addressing mode instruction requires more

(C) No. of memory clock cycle than register indirect addressing mode instruction

(D) Position independent addressing mode instruction is used in the place of short jump instructions.

Q.50 Match the following

P:	Compact Disk driven	1.	Interrupt
Q:	Printer controller	2.	DMA
R:	Non mask able interrupt	3.	A. L. U
S:	Carry flag	4.	Power failure

	P	Q	R	S
(A)	2	1	4	3
(B)	1	2	3	4
(C)	4	3	2	1
(D)	4	1	2	3

Q.51 The main memory is byte addressable and count register fabricated in IO processor is having 16 bits length. IN burst DMA operation, the IO processor requests the CPU for bus services 16 times. The maximum size of the data that can be transferred from secondary memory to main memory is_____.

Kilo bytes (Note: 1 KB = 1024 Bytes)

Q.52 P.C Relative addressing mode instruction is

[MSQ]

(A) Used only for forward jump but not for backward jumping instructions

(B) Used for both forward and backward jump instructions

(C) Generally used in the place of short jump instructions

(D) Used for array implementation

Q.53 The given below program is executed on 2GHZ CPU

Memory Address	Instruction	No. of clock cycles required
1600 (I_1)	MOV C # 06	1
1601 (I_2)	MOV B # 00	1
1602 (I_3)	ADD C	1
1603 (I_4)	DCR C	1
1604 (I_5)	JNZ: 1602	2
1605 (I_6)	(Jump on Non zero) HLT	1

The amount of time required to execute the above program is_____ ns.

Q.54 Consider a one word machine instruction ADD $R_2 @ R_1$ executed on hypothetical CPU, R_1 and R_2 are processing registers. Fetching operation takes 2 clock cycles, operand read takes 2 clock cycles and any ALU operation takes one clock cycles and extra clock is not required for storing the result in destination register.

No. of memory cycles needed to complete the instruction cycle of the above ADD $R_1 @ R_2$ $\{R_2 \leftarrow R_2 + (R_1)\}$ is _____.

Q.55 Certain CPU permits only one address and two address instructions and address field size is 6 bit and CPU word size is 16 bits. Let it used 'X' no. of two address instruction and 448 no. of one address instructions, the value of 'X' is _____

Q.56 Horizontal microprogram control word technique

[MSQ]

(A) Is used to reduce the control memory space

(B) Provide higher degree of parallelism

(C) Requires larger size control word

(D) Does not require signal encoders and decoders

Q.57 Let the processor word size is 16 bit and all processing registers size also 16 bits including program counter, stack pointer and program status word. While executing RET, Let the memory is word addressable and present SP content is $(5926)_{10}$. **[MSQ]**

(A) The SP content becomes 5928 if system used stack grows upward technique

(B) The SP content becomes 5924 if system uses stack grows upward technique.

(C) The SP content becomes 5928 if the system used stack goes down technique

(D) The SP content becomes 5924 if system used stack goes down technique

Q.58 CPU generates 72 control signals and these are divided into three unique groups, $G_1 = 40$, $G_2 = 25$ and $G_3 = 7$

[exclude the bits required for recognizing group number]

The no. of control bits that can be saved when it used vertical microprogram control word over Horizontal micro program control word is_____.

Q.59 A pipelined processor (without branch prediction unit)

[MSQ]

(A) While executing a conditional branch instruction, the CPU comes to know the status of the condition after completing the execute stage only.

(B) Requires longer execution time for arithmetical instruction then conditional branch instruction

(C) CPU finds the target instruction address immediately after fetching the conditional branch instruction

(D) Generally flags are used for writing the conditional branch instructions.

Q.60 A CPU has 6 stage pipeline and runs at 2 GHz frequency. The CPU finds the target address for the conditional branch outcome is known. While executing the largest size program CPU find 25% instructions are conditional branch related. The average instruction time is _____ns

Q.61 A system used memory mapped IO technique for connecting IO devices and CPU address bus size is 16 bits. Let system used 56594 memory register for storing the program and data, the maximum no. of IO devices to be addressed is_____.

(Note: One memory address permits only one IO device connection)

Q.62 While using memory mapped IO technique for connecting IO devices

[MSQ]

(A) Load and store instruction are used for addressing input and output devices respectively

(B) IO Read and IO write control signals are used

(C) Maximum no. of IO devices to be connected is 65536 when memory address size is 16 bits

(D) Memory space is blocked by the IO devices connection

Q.63 Consider a processor with 1 GHz clock frequency. The stack memory addressing instruction POP R_1 requires one clock cycle for memory read operation and 2 clock cycle for instruction fetch and decode (R_1 is the processing register). The amount of time needed for the instruction cycle of POP R_1 is _____micro seconds.

Q.64 Which of the following is incorrect for interrupt driven I/O implementation?

(A) Every word of data that goes from memory to I/O module or vice-versa must pass through the processor.

(B) Need to implement a mechanism such that processor can determine which device issued the interrupt.

(C) In Daisy chain implementation, for interrupt, all I/O modulus share a common interrupt request line.

(D) If interrupt occurred, processor save only current program counter (PC) in control/interrupt stack and then start execution of interrupt handler.

Q.65 Which of the following statements is false for data organized on a hard disk?

(A) Sector is the smallest unit of data that can be transferred.

(B) A collection of sectors is called tracks.

(C) A collection of tracks on various surfaces is called cylinder.

(D) None of the above

Q.66 A program runs separately on system S_1 and S_2 System S_1 execute 30% of program parallely using 6 processors. System S_2 execute 20% of program parallely using 20 processors. Find the ratio of speedup of system S_1 over speedup of system S_2 ? Consider speedup of S_1 and S_2 with respect to sequential execution of program.

Q.67 What is maximum speedup that can be achieved (approximately) by a k-stage pipeline?

(A) 2k

(B) k

(C) k^2

(D) None of the above

Q.68 Consider a system uses DMA transfer with size of word count register of DMA controller is 16 bits. The processor need to transfer 1630 KB size file from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from disk to main memory is _____

Q.69 A system uses programmed I/O mode of transfer. Width of bus is 16 bits. Assume CPU need to read 4000 bytes from a I/O device. Each word I/O transfer (16 bits) takes 2 microseconds. Minimum CPU time required to I/O transfer of required data is _____ milliseconds.

Q.70 Consider a system with following content of memory addresses at this instance:

Memory address	Content in address
2000	20
2030	25
3000	30
3020	40
5000	50

Let system execute following instructions in order:

LOAD	$R_1, 3000$	//immediate mode
ADD	$R_2, R_1, (2000)$	//direct mode
ADD	$R_3, (R_2), 0$	//register indirect mode

Left most registers in above instructions are destination registers and other fields are operands for instruction. The value of R_3 after above execution is

(A) 40 (B) 50

(C) 3020 (D) 25

Q.71 Which of the following is/are correct?

(A) Data forwarding in data path reduces impact of data hazards.

(B) Splitting the memory into separate data memory and instruction memory reduces impact of data hazards.

(C) In delayed branching technique, a pipeline stall created by control/branch hazard can always be filled by an instruction of same program.

(D) Register renaming reduces the impact of control hazard.

Q.72 Which of the following sequence of microinstructions adding an immediate value in instruction with accumulator

register (AC) and storing result in AC? (IR_{imm} is bits is immediate field of instruction).

(A) MAR $\leftarrow IR_{imm}$
MBR $\leftarrow$ Mem[MBR]
$R_1 \leftarrow$ MBR
$Z \leftarrow AC + R_1$
$AC \leftarrow Z$

(B) MAR $\leftarrow IR_{imm}$
MBR $\leftarrow$ Mem[MBR]
$Z \leftarrow AC + MBR$
$AC \leftarrow Z$

(C) $R_1 \leftarrow IR_{imm}$
$Z \leftarrow AC + R_1$
$AC \leftarrow Z$

(D) None of the above

Q.73 Consider a system with 24 bits wide control memory. Every microinstruction is 24 bits long and divided into two parts, control and address. Control part is further divided in to two parts, micro-opcode and flag selection.
Micro-opcode field is 11 bits long and specifies the micro-operation to be performed. Flag selection field used to select a flag for the purpose of finding next address depend on value of one selected flag. There are 16 flags. Consider following statements for above control memory:
S_1 : Maximum size of control memory is 1536 bytes.
S_2 : Flag selection field is 4 bits long.
Which of the following is true?
(A) Only S_1 is correct
(B) Only S_2 is correct
(C) Both S_1 and S_2 are correct
(D) Neither S_1 and S_2 is correct

Q.74 Consider the following pipelines with specified stage delays in nanoseconds. Assume zero latency for inter stage pipeline registers. Which of the following pipeline have the highest clock frequency?
(A) 6 stage pipeline with stage delays 3, 5,4, 3,4, 4.5
(B) 5 stage pipeline with stage delays 4, 3,4.5, 4, 3.5
(C) 4 stage pipeline with stage delays 4,4.5, 5, 5.5
(D) 4 stage pipeline with stage delays 3.5, 5, 6, 4

Q.75 Consider a 4 way set associative cache memory with 32 cache blocks. The main memory consists 128 blocks numbered from 0 to 127. Assume, initially cache is empty. A program request following memory blocks in order:
7,13, 2,18, 5, 87, 45, 53, 50, 98, 87, 53, 34, 33, 69,122,13, 2, 39, 50
Cache uses LRU replacement algorithm. The number of cache block replacements occurred on above sequence of requests is _____.
[Replacement means remove of already filled cache block]

Q.76 Assertion (A): The DMA technique is more efficient than the interrupt-driven technique for high volume I/O data transfer.
Reason (R): The DMA technique does not make use of the interrupt mechanism.
(A) Both A and R are true and R is the correct explanation of A.
(B) Both A and R are true but R is NOT the correct explanation of A.
(C) A is true but R is false.
(D) A is false but R is true.

Q.77 Match List-I (Characteristic) with List II (Processor Architecture) and select the correct answering the code given below the lists:

List-I

A. Write through protocol
B. Write back protocol
C. RISC
D. CISC

List-II

1. Relatively few addressing modes
2. Inclusion
3. Coherence
4. Variable length instruction format

Codes:

	A	B	C	D
A	2	4	1	3
B	1	3	2	4
C	2	3	1	4
D	1	4	2	3

(A) A (B) B
(C) C (D) D

Q.78 Consider the following statements:

(i) In a uniform delay pipeline execution time for a single instruction is less than the execution time in non-pipelined processor.

(ii) Execution time for single instruction on six stage pipelined CPU is less than or equal to identical non-pipelined CPU.

Which of the above statements are correct?

(A) Only (i)
(B) Only (ii)
(C) Both (i) and (ii)
(D) Neither (i) and (ii)

Q.79 Consider following instruction sequence with their meaning given below:

Instruction

I_0 : DIV R_1, R_2, R_1

I_1: MUL R_2, R_3, R_5

I_2 : ADD R_5, R_4, R_2

I_3 : SUB R_1, R_3, R_7

Meaning of instruction

$R_1 \leftarrow R_2 / R_1$

$R_2 \leftarrow R_3 * R_5$

$R_5 \leftarrow R_4 + R_2$

$R_1 \leftarrow R_3 - R_7$

What is the number of Write After Read (WAR) and Write After Write (WAW) hazards for the above instruction sequence?

(A) 0.2 (B) 2.2
(C) 3.1 (D) 1.3

Q.80 Consider the following statement:

S_1 : The main disadvantage of write through technique is that it generates substantial memory traffic and may create a bottleneck.

S_1 : In write back, when an update occurs a dirty bit associated with the line is set, after that if a block is replaced. It is written back to main memory irrespective of dirty bit.

Which of the following is correct?

(A) Neither S_1 nor S_2 is true
(B) Only S_1 true
(C) Only S_2 true
(D) Both S_1 and S_2 true

Q.81 Consider the following booths multiplication:
Multiplicand: 10010011011
Multiplier: 10100101
The number of addition operations required in the multiplication will be_____

(A) 2 (B) 3
(C) 4 (D) 1

Q.82 Match List-I (Instructions) with List II (Addressing modes) and select the correct answer using the codes given below the lists:

List I

A. ADD R_0[[2000]]

B. MOVR_1, 10

C. ADD R_1, R_2

D. ADD R_0, (100)

List II

1. Direct addressing mode
2. Immediate addressing mode
3. Register addressing mode
4. Indirect addressing mode

Codes:

	A	B	C	D
(A)	4	2	3	1
(B)	4	3	1	2
(C)	3	1	2	4
(D)	3	1	4	2

(A) A (B) B
(C) C (D) D

Q.83 Consider the instruction ADD [[2000]] where ADD stands for addition. The number of memory cycles required to execute the instruction is

(A) 1 (B) 2
(C) 3 (D) 4

Q.84 Consider a DRAM that must be given a refresh cycle of 64 times per msec. Each refresh operation requires 100 ns and a memory cycle requires 200nsec. The percentage of the memory's total operating time must be given to refresh is_____. (Up to 2 decimal places)

Q.85 A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4 K blocks of 128 words each. Find the value of X + 5Y where X is number of bits for tag and Y is number of bits for set?

Q.86 Consider a micro-programmed control unit which supports 360 instructions. Each instruction takes 10 micro operations, 15 flags are supported and 62 control signal vertical micro-programmed is used then the size of 4 control word is _____ bytes.

Q.87 5 stage pipeline has the stage delay 100,140,170,180 and 200 ns respectively. Registers that are used between the stages have a delay of 2 ns each. Assuming constant clock rate, the total time taken to process 580 data items on this pipeline will be_____ (in micro seconds).

Q.88 Consider a task that makes extensive use of floating point operations with 40% of the time is consumed by floating point operations with a new hardware design. If the floating point module is speeded by a factor of 4. What is overall speed up_____? (Up to 2 decimal places)

Q.89 The access time of a cache memory is 100 ns and that of main memory is 1 micro-seconds. 80% of the memory requests are for read and others are for write. Hit ratio for read only accesses is 0.9. A write through procedure is used. The average access time of the system for both read and write requests is_____ (in ns).

Q.90 Which of the following is true about horizontal micro-instruction?

[MSQ]

(A) It has high degree of parallelism.
(B) Slower execution than vertical micro-instruction.
(C) Longer control word than vertical micro-instruction.
(D) Control signal is expressed in decoded binary format.

Q.91 Which of the following is/are true?

[MSQ]

(A) I/O mapped I/O is most widely used communication for connecting I/O devices as compared to memory mapped I/O.
(B) Internal Interrupts are given priority over external interrupts for service.
(C) In Interleaving DMA mode, the waiting time of CPU is almost zero.
(D) Arithmetic left shift is exactly same as logical left shift.

Q.92 Consider a hypothetical CPU which supports 16 bit instruction, 62 registers and 1 KB memory space. If there exist 12 two address instructions which uses register reference and 14 one address memory reference instructions. How many 0-address instructions are possible?

(A) 1024 (B) 2448
(C) 4096 (D) 8192

Q.93 Consider a direct mapped cache with 16 blocks with block size of 16 bytes. Initially the cache is empty. The following sequence of access of memory addresses: 0x80000, 0x80008, 0x80010, 0x80018, 0x30010

Is repeated 10 times. Which of the following represents number of compulsory and conflict misses?

(A) Compulsory = 2 and conflict = 18
(B) Compulsory = 3 and conflict = 18
(C) Compulsory = 4 and conflict = 16
(D) Compulsory = 2 and conflict = 20

Q.94 The speed gained by an '*rl* segment pipeline executing 'm' tasks is

(A) $\frac{(n+m-1)}{mn}$ (B) $\frac{mn}{(n+m-1)}$

(C) $\frac{n+m}{(nm-1)}$ (D) $\frac{n+m}{(nm+1)}$

Q.95 A particular parallel program computation require 200 seconds when it is executed on a single processor. If 40% of this computation is "inherently sequential" then what are the theoretically best elapsed time for this program running with 2 and 4 processors respectively?

(A) 80 and 120 seconds
(B) 90 and 60 seconds
(C) 140 and 110 seconds
(D) 100 and 80 seconds

Q.96 Consider the following floating point format:

Sign	Exponent	Mantissa
19	18 11	10 0

What is the representation of 0.625×8^{12} in hexadecimal without normalization?

(A) Ox545D0 (B) OC58700
(C) OX51D00 (D) Ox5AC00

Q.97 Consider the following code:

$I_1 : \text{ADD}\, r_1, r_2$	$r_1 \leftarrow r_1 + r_2$
$I_2 : \text{Load}\, r_1, (r_0)$	$r_1 \leftarrow M[[r_0]]$
$I_3 : \text{SUB}\, r_3, r_4$	$r_3 \leftarrow r_3 - r_4$
$I_4 : \text{Load}\, (r_0), r_3$	$M[[r_0]] \leftarrow r_3$
$I_5 : \text{ADD}\, r_1, r_3$	$r_1 \leftarrow r_1 + r_3$
$I_5 : \text{Halt}$	Halts

The data transfer instruction size is 64 bit, ALU operation instruction size is 32

bit and branch instruction size is 16 bit. Assume program has been loaded in the memory starling from the location 5000 decimal onwards. If an interrupt occurs during the execution of I_6,the return address pushed on to the stack is.

(A) 5030 (B) 2024

(C) 5028 (D) 5016

Q.98 Consider 4 stage instruction pipeline where different instructions are spending different cycles at different stage shown below:

	S_1	S_2	S_3	S_4
I_1	1	3	2	1
I_2	1	1	3	2
I_3	3	1	1	1
I_4	1	2	1	1

The following loop is executed in the pipeline

For (i=1;i<=2;i++)

{

I_1;

I_2;

I_3;

I_4;

}

The number of cycles saved using the loop level parallelism over without loop level parallelism to executed the above program is ____(in cycles).

(A) 1 (B) 2

(C) 3 (D) 4

Q.99 Consider the machine with a byte addressable main memory of 216 byte, block size of 16 byte and a 2 way set associate mapped cache having 210 lines Suppose there are two bytes in main memory i.e. first byte $[E01F]_{16}$ and second byte $[E208]_{16}$ respectively then the difference of the set value (in decimal) between given two bytes i.e. (SET value of second byte - SET value of 1st byte) is

(A) 21 (B) 31

(C) 40 (D) 51

Q.100 Consider a system with two level cache hierarchies with L_1 and L_2 cache. Program refers memory 2000 times, out of which 30 misses are in L_1 cache and 20 misses are in L_2 cache If miss penalty of L_2 is 400 clock cycles, hit time of L_2 is 12 clock cycle and hit time of L_1 is 1 clock cycle, the average memory access time is _____ clock cycles (Upto 2 decimal places).

Q.101 A hypothetical 6 stage pipeline processor is designed in which branch is predicted at 4th stage and each stage takes 1 cycle to compute its task. If f is a the probability of an instruction being a branch instruction then the value of f such that speed up is at least 5 is (Up to 3 decimal places)

Q.102 A 5 stage pipeline has instruction Fetch (IF), Instruction decode (ID), Operand fetch (OF), Process data (PD) and Write back (WB) stages. The IF, ID, OF takes 1 clock cycles each for any instruction. The process data lakes 1 dock cycle for ADD and SUB instruction. 2 clock cycles for MUL instruction and 4 clock cycles for DIV instruction respectively. The number of dock cycles needed to execute the following sequence of

instruction where operand forwarding from WB to PO and PO to of is used

Instruction Meaning of Instruction

$I_0 = \text{SUB } R_2, R_0, R_1$

$R_2 \leftarrow R_0 - R_1$

$I_1 : \text{MUL } R_5, R_3, R_4$

$R_5 \leftarrow R_3 * R_4$

$I_2 : \text{ADD } R_2 \leftarrow R_5, R_2$

$R_2 \leftarrow R_5 + R_2$

$I_3 : \text{DIV } R_5, R_2, R_6$

$R_5 \leftarrow R_2 / R_6$

Q.103 Consider a disk that rotates at 60000 rotations per minute and has a transfer rate of 80 MBps If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 8 times the Ask transfer time, the average time to read or write a 128 byte sector of the disk is___msec.(Upto 4 decimal places)

Q.104 Consider a machine with 8 way set associative data cache of size 64 Kbytes and block size 8 byte. The cache is managed using 32 bit virtual address and page size is 4 Kbytes. What Is the total size of the tags in the cache directory____(K bits)?

Q.105 Consider a two- way set associative cache with total of 8 cache blocks and the following sequence of memory block requests arrived:

20,17,21, 32, 20, 16, 27, 7, 16, 32

If LRU replacement policy is used then the hit ratio will be____(Upto 2 decimal places)

Q.106 A hypothetical DMA is designed to transfer the data from I/O device to main memory under burst transfer mode. The count register size Is 34 bit and gets the control of the system buses 4 times then the maximum size of the data transferred by controller in Giga byte is____.

Q.107 Consider the following addressing modes:

[MSQ]

(a) Indirect addressing mode

(b) Indexed addressing mode

(c) Relative addressing mode

(d) Based addressing mode

In which of the following addressing mode's, effective address is calculated by adding the constant value to some register content.

(A) a (B) b

(C) c (D) d

Q.108 Which of the following is correct regarding data hazard to pipeline?

[MSQ]

(A) Read after read causes no hazards for the processor.

(B) When the output register of an instruction is used to write after read by a previous instruction, hazards occur due to write After read dependency (anti- dependency).

(C) When the value produced by an instruction is required by a subsequent instruction, then hazards occur due to output data dependency.

(D) Code reordering mechanism can be used to handle data hazards.

Q.109 The method of accessing the I/O devise by repeatedly checking the status flags is

(A) Program controlled I/O

(B) Memory mapped I/O

(C) I/O mapped

(D) None of these

Q.110 Which of the following statements about synchronous and asynchronous I/O is False?

(A) An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O

(B) In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O

(C) A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O

(D) In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked alter the completion of I/O

Answers **Computer Organization & Architecture**

1.	A	2.	A	3.	A	4.	B	5.	B
6.	4	7.	24	8.	B,C	9.	A,B	10.	D
11.	B	12.	A	13.	D	14.	11.1	15.	300
16.	A,B	17.	B,C,D	18.	B,C	19.	1024	20.	87
21.	C	22.	A,B	23.	B	24.	C	25.	A
26.	B	27.	C	28.	96	29.	A	30	D
31.	C	32.	82032	33.	A,C	34.	B,C	35.	A,C
36.	111	37.	43.3	38.	A,B,C	39.	B	40	A
41.	6000	42.	A	43.	A	44.	B,D	45.	256
46.	C	47.	A	48.	B,C	49.	B,C,D	50.	A
51.	1024	52.	B,C	53.	13.5	54.	5	55.	9
56.	B,C,D	57.	B,C	58.	58	59.	A,D	60.	0.87
61.	8942	62.	A,C,D	63.	0.003	64.	D	65.	D
66.	1.08	67.	B	68.	26	69.	4	70.	A
71.	A	72.	C	73.	C	74.	B	75.	6
76.	A	77.	C	78.	D	79.	C	80.	B
81.	B	82.	A	83.	C	84.	0.64	85.	28
86.	11	87.	116.8	88.	1.42	89.	253	90.	A,C,D
91.	A,B,C,D	92.	B	93.	B	94.	B	95.	C
96.	C	97.	C	98.	C	99.	B	100.	5.14
101.	0.066	102.	12	103.	1.5128	104.	152	105.	0.18
106.	64	107.	B,C,D	108.	A,B,D	109.	A	110.	B

1. (A)

Just before fetching given instruction $PC = 2460$ H

Just after fetching given instruction $PC = PC + 4 = 2460 + 4 = 2464$ H because instruction size is 4 bytes (32 bits).

Mem [A] is using direct addressing mode.

So, Effective address $= A = 4408$ H

Now to read value of location A system has to make MAR $= A = 4408$ H.

2. (A)

System A :

It is byte addressable and 4 GB in size of memory.

So number of addressable locations in memory

$$= \frac{\text{Memory size}}{\text{Addressable size}}$$

$$= \frac{4\text{ GB}}{1\text{ byte}} = 4\text{ GB} = 2^{32}$$

Number of bits required for 2^{32} locations $= \log_2(2^{32}) = 32$ bits

So, $x = 32$

System B :

It is word addressable, word size is 4 bytes and 16 GB in size of memory, so number of addressable locations in memory

So, number of addressable locations in memory

$$= \frac{16\text{ GB}}{4\text{ bytes}} = 4\text{ GB} = 2^{32}$$

Number of bits required for 2^{32} locations $= \log_2(2^{32}) = 32$ bits

So, $y = 32$

3. (A)

4. (B)

One access of system bus for data transfer from input/output to DMA and other for data transfer from DMA to memory.

5. (B)

Word size is 32 bit, so MDR size is 32 bits.

$$\text{Size of MAR} = \log_2\left(\frac{\text{Main memory size}}{\text{Addressable size}}\right)$$

$$= \log_2\left(\frac{4\text{ GB}}{16\text{ bits}}\right)$$

$\{\because$ Here half word $= 16$ bits$\}$

$$= \log_2\left(\frac{4 \times 2^{30} \times 8}{16}\right) = \log_2(2^{31}) = 31\text{ bits}$$

6. 4

Number of tracks = Number of cylinders

Total size = (Number of surfaces) × (Number of tracks per surface) (Number of sectors per track) × (Size of a sector)

$= 32 \times 256 \times 512 \times 1024$ bytes

$= 2^5 \times 2^8 \times 2^9 \times 2^{10}$ bytes $= 2^{32}$ bytes $=$ 4 GB

7. 24

Block size (BS) $= 256$ bytes $= 2^8$ B

Block offset (BO) $= \log_2(2^8) = 8$ bits

In fully associative mapping physical address divided into tag field and block offset, so set field length $= 0$ bits.

Tag field length = Physical address length – Block offset

$= 32 - 8 = 24$ bits

So, $x = 24, y = 0$

$x - y = 24$

8. B,C

In interrupt driven input/output, device interrupt CPU before data transfer. And DMA interrupt CPU at the end of input/output operation.

9. A,B

Fully associative cache contains only tag field and block offset, so if we change block size then it will effect tag field.

Direct mapped and k associative cache have tag field, set field and block offset. Here block offset will affect only set field, but not tag field.

10. (D)

Current address of head <8, 8, 16, 127>.
Head have read 8 cylinders from 0 to 7, so
Bytes for 8 cylinders = (Number of cylinders) × (Number of surfaces) × (Number of sectors per track) × (Bytes per sector)

$$= 8 \times 16 \times 32 \times 512 \text{ bytes}$$

$$= 2^3 \times 2^4 \times 2^5 \times 2^9 = 2^{21} \text{ bytes} \quad \ldots \text{(i)}$$

On 8th cylinder, head completed 8 surfaces from 0 to 7, so
Bytes for 8 surfaces = (Number of surfaces) × (Number of sectors per track) × (Bytes per sector)

$$= 8 \times 32 \times 512$$

$$= 2^3 \times 2^5 \times 2^9 = 2^{17} \text{ bytes} \quad \ldots \text{(ii)}$$

On 8th surface of 8th cylinder, head completed 16 sectors from 0 to 15, so
Bytes for 16 sectors = (Number of sectors) × (Bytes per sector)

$$= 16 \times 512 = 2^4 \times 2^9 = 2^{13} \text{ bytes} \quad \ldots \text{(iii)}$$

On 16th sector of 8th surface on 8th cylinder, head completed 128 bytes from 0 to 127, so
On this sector bytes read = 128 bytes … (iv)
From (i), (ii), (iii) and (iv) total bytes read by head.

$$= 2^{21} + 2^{17} + 2^{13} + 128 \text{ bytes}$$

11. (B)

$4 \text{ GB} = 2^{32}$ bytes and memory is byte addressable, so address length is 32 bit

Block size (BS) $= 64 \text{ bytes} = 2^6$ B

Block offset (BO) $= \log_2(2^6) = 6$ bit

Number of cache blocks

$$= \left(\frac{\text{Cache size}}{\text{Block size}}\right) = \frac{128 \text{ KB}}{2^6 \text{ B}} = 2^{11} \text{ blocks}$$

Length of set field = Address length – Block offset – Tag length $= 32 - 6 - 16 = 10$ bit

Length of set field

$$= \log_2\left(\frac{\text{Number of cache blocks}}{\text{Associativity}}\right)$$

$$10 = \log_2\left(\frac{2^{11}}{x}\right)$$

$$\frac{2^{11}}{x} = 2^{10}$$

$$x = 2$$

So, cache is 2 way set associative.

12. (A)

SLT operation actually implemented using subtraction, as shown below :
For SLT a, b, c

$$a = \begin{cases} 0, & \text{if } b - c > 0 \\ 1, & \text{if } b - c < 0 \end{cases}$$

So, here use $R_1 - R_2$

$$R_2 = 0101$$

$-R_2 = 2\text{'s}$ complement of $R_2 = 1011$

$$R_1 - R_2 = R_1 + (-R_2)$$

$$= 0011 + 1011 = 1110$$

1110 is negative number in 2's complement.
So, $N = 1$
1110 is non zero
So, $Z = 0$
No overflow in above operation
So, $V = 0$
No half carry
So, $H = 0$

13. (D)

Average instruction execution time $= \sum(\text{IC} \times \text{CPI}) \times \text{Cycle time}$

$$= \big((0.4 \times 6) + (0.3 \times 8) + (0.3 \times 4)\big) \text{ 4 ns}$$

$$= 24 \text{ ns}$$

14. 11.1

Average memory access time (AMAT)

$$= (L_1 \text{ access time}) + \text{Miss rate of } L_1$$

$$\times \begin{bmatrix} L_2 \text{ access time} + \text{Miss rate} \\ L_2 \times \text{Memory access time} \end{bmatrix}$$

$$= 10 \text{ ns} + \frac{1}{100} \times \left[100 \text{ ns} + \frac{1}{100} \times 1000 \text{ ns} \right]$$

$$= 11.1 \text{ ns}$$

15. 300

600 rounds in $= 1$ minute $= 60$ sec

1 round in $= \frac{60}{600} = \frac{1}{10} = 100 \text{ ms} -$ rotation time

Bytes read in 1 round = Bytes in a track

= (Number of sectors per track) × (Bytes per sector)

$$= 64 \times 512 = 2^6 \times 2^9 = 2^{15} \text{ bytes}$$

Time to access 1st track of file = Seek time

$$= 50 \text{ ms} \quad \ldots \text{(i)}$$

Time to access starting point of file on 1st track = Average rotational latency

$$= \frac{\text{Rotation time}}{2} = \frac{100}{2} = 50 \text{ ms} \quad \ldots \text{(ii)}$$

Let x bytes of file stored on 1st track, then

$$\text{Time to record } x \text{ bytes} = x \times \frac{\text{Rotation time}}{\text{Bytes in 1 rotation}}$$

$$= x \cdot \frac{100}{2^{15}} \cdot \text{ms} \quad \ldots \text{(iii)}$$

Negligible time on moving from 1st track to its adjacent track which contain other part of file.

Time to access starting point of file on 2nd track = Average rotational latency

$$= \frac{\text{Rotation time}}{2} = \frac{100}{2} = 50 \text{ ms} \quad \ldots \text{(iv)}$$

1st track has x bytes of file, so 2nd track has $(48 \text{ KB} - x)$ bytes.

Time to read $(48 \text{ KB} - x)$ bytes from 2nd track

$$= (48 \text{ KB} - x \text{ bytes}) \times \frac{\text{Rotation time}}{\text{Bytes in 1 rotation}}$$

$$= (48 \text{ KB} - x \text{ bytes}) \frac{100}{2^{15}} \text{ ms} \quad \ldots \text{(v)}$$

Add (i), (ii), (iii), (iv) and (v) for total time to access and read given file.

Total time

$$= 50 \text{ ms} + 50 \text{ ms} + x \cdot \frac{100}{2^{15}} \text{ ms}$$

$$+ 50 \text{ ms} + (48 \text{ KB} - x) \frac{100}{2^{15}} \text{ ms}$$

$$= 100 \text{ ms} + \frac{100}{2^{15}} (x + 48 \text{ KB} - x) + 50 \text{ ms}$$

$$= 150 \text{ ms} + \frac{100}{2^{15}} \times 48 \times 2^{10}$$

$$= 150 \text{ ms} + \frac{100}{32} \times 48$$

$$= 150 \text{ ms} + 150 \text{ ms} = 300 \text{ ms}$$

16. A,B

Main memory (MM) address length

$$= \log_2 (\text{MM size}) = \log_2 (4 \text{ GB})$$

$$= \log_2 (2^{32}) = 32 \text{ bits}$$

System A :

Number of cache blocks

$$= \frac{\text{Cache size}}{\text{Block size}} = \frac{128 \text{ KB}}{128 \text{ B}} = 1 \text{ K} = 2^{10}$$

$$\text{Set numbers} = \frac{\text{Block}}{\text{Associativity}} = \frac{2^{10}}{2} = 2^9$$

Set field length $= \log_2$ (Set numbers)

$$= \log_2 (2^9) = 9 \text{ bits}$$

Block offset $= \log_2$ (Block size)

$$= \log_2 (2^7) = 7 \text{ bits}$$

Tag field length = Address length – Set length – Block offset

$$= 32 - 9 - 7 = 16 \text{ bits}$$

System B :

$$\text{Number of cache blocks} = \frac{128 \text{ KB}}{256 \text{ B}} = 2^9$$

$$\text{Set numbers} = \frac{2^9}{2} = 2^8$$

Set field length $= \log_2 (2^8) = 8$ bits

Block offset $= \log_2(256) = \log_2(2^8) = 8$ bits

Tag field length $= 32 - 8 - 8 = 16$ bits

$x =$ Tag length of $A -$ Tag length of B

$= 16 - 16 = 0$

$y =$ Set length of $A -$ Set length of B

$= 9 - 8 = 1$

17. B,C,D

$C_1 \rightarrow$ Conflict miss

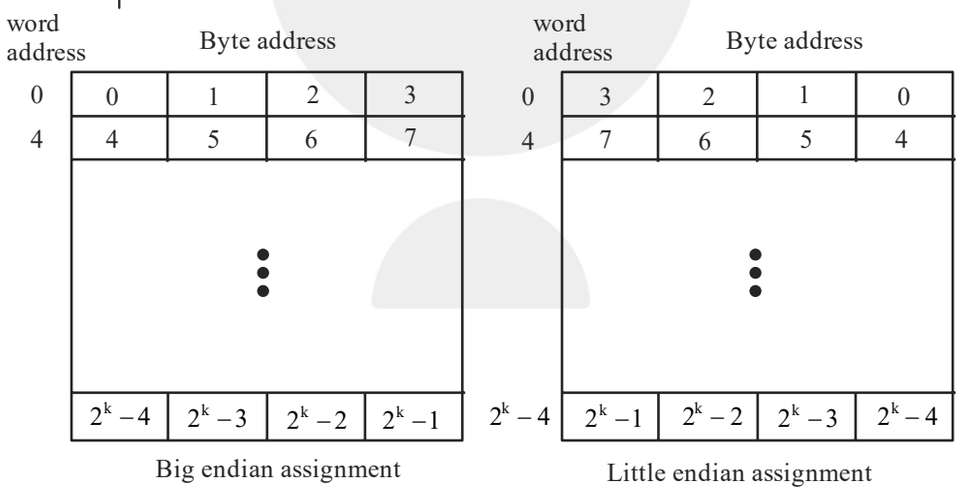
$C_2 \rightarrow$ Compulsory miss

$C_3 \rightarrow$ Capacity miss

$H \rightarrow$ Hit

10	11	12	18	5	11	6	7	10	15	11
C_1	C_2	C_2	C_2	C_2	H	C_2	C_2	C_1	C_2	C_1	H

0	12			
1	5			
2	~~10~~	~~15~~	6	10
3	~~11~~	~~7~~	15	11



Big endian assignment

Little endian assignment

19. 1024

Branch is checking equality R_1 and R_2. PC relative mode is used. Before adding the offset the PC is already incremented by 4.

Therefore mem address of next instruction must be

$1004 + \text{label} = 1004 + 20 = 1024$

20. 87

X (opcode bits) = ceil $(\log_2 110) = 7$ (because the instruction set consists of 110 different)

Number of $C_1 = 2$

Number of $C_2 = 8$

Number of $C_3 = 0$

Number of $H = 2$

18. B,C

Byte addresses can be assigned across words in two ways

Big endian and little endian

Big endian: the most significant byte has the lowest address, and the least significant byte has the highest address $(1-2-3-4)$.

Little endian: the least significant byte has the lowest address, and the most significant byte has the highest address $(4-3-2-1)$

Bits for register address $(Y) = \log 8 = 3$ (because there are registers)

Total size of the instruction = 32 bits

Therefore bits for mem address

$(Z) = 32 - 7 - 3 = 22$

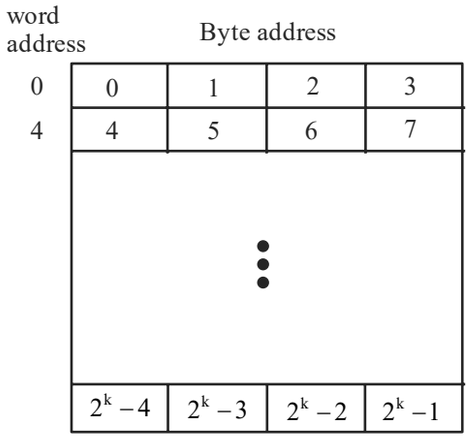
$XY + YZ = 21 + 66 = 87$

21. (C)

Byte addresses can be assigned across words in two ways:

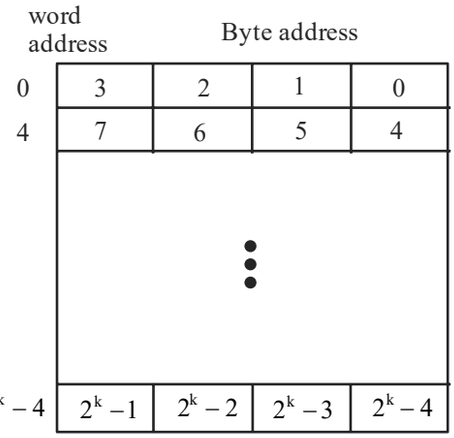
Big Endian and little endian

Big Endian the most significant byte has the lowest address, and the least significant byte has the highest addresses $(1-2-3-4)$



Big endian assignment

Little Endian the least significant byte has the lowest address, add the most significant byte has the highest address $(4-3-2-1)$



Little endian assignment

22. A,B

If 2 Two's Complement numbers are added, and they both have the same sign (both positive and both negative), then overflow occurs if and only if the result has the opposite sign. Overflow never occurs when adding operands with different signs.

i.e. Adding two positive number must give a positive result

Adding two negative number must give a negative result

$$\begin{array}{l} 0111\ \ 1001\ \ 1011\ \ 1011 \\ +\,0011\ \ 1011\ \ 1110\ \ 1110 \\ =1011\ \ 0101\ \ 1010\ \ 1001 \\ 1111\ \ 0111\ \ 0110\ \ 1001 \\ +\,1000\ \ 0001\ \ 0110\ \ 0100 \\ =1011\ \ 1100\ \ 01100\ \ 1101 \end{array}$$

Overflow never occurs when adding operands with different signs, so, in option C, and D, we don't have any overflow.

23. (B)

$$\begin{array}{r} 1100\ \ 1100 \\ 1000\ \ 1111 \\ \hline 1\ \ 0101\ \ 1011 \end{array}$$

There is a carry out is generated from the most significant bit during an operation, so C =1

To check overflow, we can check the MSB bits of the two number being added. Since both are 1 but the result is 0 hence, an overflow has occurred (Or we can check by seeing that there is out carry from MSB, but there is No in carry into MSB). Hence, V = 1.

Result is not zero, hence, Z = 0.

24. (C)

Very first step = fetch the inst^n = I1

After fetching we can increment the PC = I6

Now we have the inst in the IR let's decode it = I2

After decoding read the operand value from R7 = I2

We have the immediate value add it to R7 = I3

Now calculate the EA using I4 and I3 and fetch the source operand = I5

Load the data = I7

Therefore ans should be C.

25. (A)

C_4 CS is there in fetch cycle as well as in indirect cycle section

Boolean Expression for C_4

$$C_4 = P'Q't_3 + P'Qt_3$$

Since No option is matching. Let's simplify

$$C_4 = P't_3(Q'+Q) = P't_3$$

Therefore answer should be A.

26. (B)

Initially

$M = 10001111$
$N = 01100010$
$O = 01001001$
$P = 01110010$

Now, program execution begins:

$1: M \leftarrow M \oplus N :: / / M = 11101101$
$2: M \leftarrow CSLM :: / / M = 11011011$
$3: N \leftarrow M + N :: / / N = 00111101$
$4: O \leftarrow O \wedge N :: / / \mathrm{O} = 00001001$
$5: O \leftarrow CSRO :: / / \mathrm{O} = 10000100$
$6: P \leftarrow P + 1 :: / / P = 01110011$
$7: P \leftarrow P + O :: / / P = 11110111$

Hence, answer is options B.

27. (C)

When the program is executed on a single processor i.e. All instructions are executed sequentially, then the time taken is 100 units. The assumed program has 100 instruction. So, each instruction takes 1 unit of time.

Program running with 2 processors:

40 percent of computation is "inherently sequential" (i.e. will not benefit from additional processors), So, 40 units of time will be required for these 40 instruction. The remaining 60 instruction can be executed parallelly on the two processors, so 30 units of time more required. Hence a total 70 units of time 70 seconds.

Program running with 4 processors:

40 percent of computation is "inherently sequential" (i.e. will not benefit from additional processors), so 40 units of time will be required for these 40 instruction. The remaining 60 instructions can be executed parallelly on the four processors, so 15 units of time more required hence a total 55 units of time 55 seconds.

28. 96

Instruction length is 20, so, maximum possible encodings $= 2^{20}$

It is given that there are 10 M – type instruction. Let's assume the maximum R-Type instructions to be *x*.

$$2^{20} \geq (10 \times 2^{16}) + (x \times 2^6 \times 2^6)$$
$$\Rightarrow x \leq 96$$

So, maximum 96 R type instructions possible.

29. (A)

Say the program takes 100 units time when executed sequentially

Now, on the parallel processors, 10 of the program is executed sequentially, so the time needed for that is 10 units.

The remaining 90 of the program is run parallelly using an unlimited no of processors, then execution time is negligible.

So, speed up = 100 unit/10 unit = 10.

Speed up is approximately 10 times.

30. (D)

As Alignment is mentioned in the question and no rearrangement of fields of a widget can be done memory layout:

1. Short *s*, byte *b* (2+1)+5 (padding to make the sum = 8 bytes)
2. Long *l* (8 bytes, no need of padding)
3. int *I* (4+4(padding) = 8)

Therefore each element in the widget array occupies 3 words $= 3 * 8 = 24$ bytes

The answer is D.

31. (C)

Design 1:

A part of a bigger task is improved twenty times than it was before. The other part of the same task constitutes 60 of the overall task time and it remains unchanged.

Let, this task be T, and let's assume this task takes 100 units of time before enhancement. Let

it have two part: part A (40 units of time) and part B (60 units of time)

After enhancement, part A is improved twenty times than it was before, so now part A will take time : $40/20 = 2$ unit of time

After enhancement, Part B remains unchanged so, Now part B will take time 60 unit of time.

So, after enhancement, the task T will take $2+60 = 62$ unit of time

So, speedup achieved is = (execution time before enhancement)/ (execution time after enhancement)

$= 100/62 = 1.61290323$

Design 2:

The designer can make changes to improve 20 of the task 100 faster, 35 of the task 4 times faster and 10 of the task 100 times faster but it causes faster, but it causes the remaining part of the task to perform as bad as 50 slower than before.

Let this task be S, and let's assume this task takes 100 units of time before enchantment. Let it have four part: Part 1 (20 unit of time), Part 2 (35 unit of time), Part 3 (10 units of time) and part 4 (remaining 35 unit of time)

After enhancement, Part 1 is improved to be made 100 faster than it was before, so, now part 1 will take time: 20/2 = 10 unit of time

After enhancement, part 2 is improved to be made 4 times faster than it was before, so, now part 3 will take time: 10/100 = 0.1 unit of time

After enhancement part 4 becomes 50 slower than it was before, so, now part 4 will take time: 35*2 = 70 units of time.

So, after enchantment, the task S will take 10 + (35/4) + 0.1 + 70 = 88.85 unit of time

So, speedup achieved is = (execution time before enhancement) / (execution time after enhancement) = 100/88.85 = 1.1254924

So, difference in speedup is 1.61290323

– 1.1254924 = 0.4875 (approx.).

32. 82032

Big endian: the most significant byte has the lowest address and the least significant byte has the highest address $(1-2-3-4)$

Little endian: the least significant byte has the lowest address and the most significant byte has the highest address $(4-3-2-1)$

So the given word is 0×00014070 which in decimal is 82032

33. A,C

Here, no of flags = 8

Therefore, no of bits required in the address selection field = 3

No of bits in address field $= 24-13-3 = 8$

Size of control memory

$= 2^8 = 256$ word $= 256*24$ bits

$= 6144$ bits

34. B,C

Since data is 8 bit the OVEL occurs, when the result is between

$(-128)_{10}$ and $(+127)$

94_{16} = 1 0 0 1 0 1 0 0 = $-(108)$

−128 16 4

79_{16} = 0 1 1 1 1 0 0 1 = +121

64 32 16 8 1

Option (A) is False, $-108+121 = -13$ No OVEL

Option (B) is True, $-108+121 = -13$ No OVEL

Option (C) is True, $-108-79 = -187$ OVEL

Option (D) is False, $-108-79 = -187$ OVEL

35. A,C

While adding 2 number of signed data the of both operands is same and longest result size of $m+1$ bits

36. 111

RPM = 12000, RPS = 200,

One rotation time $= \frac{1}{200}\text{sec} = 5$ ms

Avg. latency = 2.5 msec

Access time of ac sector $= T_{\text{seek}} + T_{\text{AvgRot}} + T_{\text{RD/WR}}$

$T_{\text{track}} = 5$ ms, one sector data

RD/WR time $\left(T_{\text{sec tor}}\right) = \frac{5 \text{ ms}}{100} = 0.5$ m.sec

One sector access time $= 3 + 2.5$ ms $== 5.55$ ms

$T_{20\text{sector}} = 20 \times 5.55 \text{ ms} = 111$

37. 43.3

$T_{cm} = 10$ ns, $T_{mm} = 100$ ns

$H_{RD} = 90\% = 0.9$

Read frequency $f_{RD} = 70\%$

Write frequency $f_{WR} = 30\%$

$T_{Avg} = f_{RD} * T_{\text{Read}} + f_{\text{WRAvg}}$

$T_{\text{readAvg}} = \left(T_{em} * H_{RD}\right) + \left(1 - H_{RD}\right) \times T_{MM}$

$= (10 \times 0.9) + 0.1 \times 100 = 19$ ns

$T_{\text{WRAvg}} =$ lostgest delay in $T_{cm}. T_{mm}$

$= 1000$ ns(write through)

$T_{Avg} = \left(0.7 * 19 \text{ ns}\right) + \left(0.3 \times 100 \text{ ns}\right)$

13.3 ns + 30 ns = 43.3 ns

38. A,B,C

$MMW = 2^{24}$ word $= 16$ M word

$CMW = 2^{17}$ word $= 128$ K word

$BW = 9; PA = 24; CA = 17;$

Tag size $= PA - CA$

$= 24 - 17 = 7$ bits

$$CL = \frac{CMW}{BW} = \frac{2^{17}\text{B}}{2^{9}\text{B}} = 2^{8} = 256$$

Tag directory size $=$ Tag $\times CL$

$= 7 \times 256 = 1792$ bits

When CPU requires the same word repeatedly, then there are more no. of chances for occurring conflict miss.

39. (B)

Given data is in singed 2's complement notation, its decimal value is

$$\underset{}{x_{n-1}} \quad \underset{}{x_{n-2}} \quad \underset{}{-x_4} \; \underset{}{x_3} \; \underset{}{x_2} \; \underset{}{x_1} \; \underset{}{x_0}$$

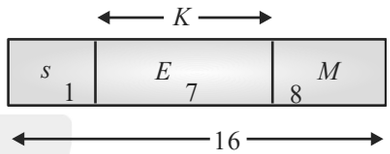
$$\underbrace{-(2^{n-1})}_{-ve\ value} \quad \underbrace{2^{n-2} \quad 2^4 \; 2^3 \; 2^2 \; 2^1 \; 2^0}_{-vev\ alue}$$

$$\left\{(-1)\left(x_{n-1}\right) \times \left(2^{n-1}\right)\right\} + \sum_{i=0}^{n-2} a_i \times 2^i$$

40. (A)

Biasing value $= 64 = 2^6$

Hence $K - 1 = 6, \; K = 7$



E size = 7 bit and

M size = 8 bits

41. 6000

Average latency is equal to the half Rotation time $= \frac{T_{\text{track}}}{2} = 5$ m sec

$T_{track} = 10$ msec (One track reading time)

One rotation time = 10 msec

$$\text{RPS} \frac{1}{T_{\text{track}}} = \frac{1}{10 \times 10^{-3}} = 100$$

Hence RPM $= 60 \times 100 = 6000$

42. (A)

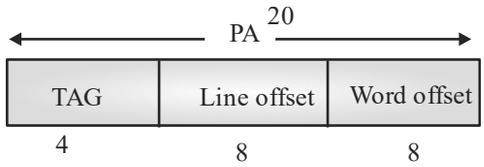
Conflict miss occurred, when a word is accessed 2nd time on words and the word is not available in cache memory address. In fully associative mapped cache only compulsory and capacity misses will occur.

43. (A)

PA = 20 bit, direct map CM size = 64 KB,

CMW $= 2^{16}$, BW $= 2^8$

$$CL = \frac{CMW}{BW} = \frac{2^{16}}{2^8} = 2^8$$
$$= 256(CL\ 0 \text{ to } CL\ 255)$$



$$W_{2049} = 100000000001$$

$$= 0000 \left| \begin{array}{c} 128\ 64\ 32\ 16\ 8\ 4\ 2\ 1 \\ 0\ 0\ \ 0\ 0\ 1\ 0\ 0\ 0 \\ \text{Cache line offset} \\ = \text{CL}_8 \end{array} \right| \begin{array}{c} 00000001 \\ \text{word address} \end{array}$$

44. B,D

$$T = 1024 = 2^{10},\ S = 64 = 2^6,\ B = 16 = 2^4$$

Hence word address format $\langle T\ S\ B \rangle$

$$= 10 + 6 + 4 = 20 \text{ bits}$$

$$\rightarrow FFC.F_{16} = \begin{array}{c} 1111\,111111 \\ \text{Track address} \\ T_{1023} \end{array} \left| \begin{array}{c} 000000 \\ \text{Sector} \\ \text{Address} \\ S_0 \end{array} \right| \begin{array}{c} 1111_2 \\ \text{Byte address} \\ B_{15} \end{array}$$

It is in sector S_0, hence option (A) is false and option (B) is True.

$$(003F2)_{16} = \begin{array}{c} 0000\ 0000\ 00 \\ \text{Track address} \\ T_0 \end{array} \left| \begin{array}{c} 111111 \\ \text{Sector} \\ \text{Address} \\ S_{63} \end{array} \right| \begin{array}{c} 0010 \\ \text{Byte address} \\ B_2 \end{array}$$

It is in sector S_{63}, hence (C) is wrong and (D) is True.

45. 256

Operand size = 16 bit
Operation is squarer
Address size = 16 bit
Longest result size = 32 bit (data size)

$$\text{ROM size} = 2^{16} \times 32 \text{ bits}$$
$$= 64\text{K} \times 4 \text{ bytes} = 256 \text{ KB}$$

46. (C)

$$(FFFE0000)_{16}$$

$$\begin{array}{c|c|c} 1 & 111\ \ 11111 & 111\,1110\ 0000\ 0000\ 0000\ 0000_2 \\ S & E = \ \ 255 & M \end{array}$$

Let, E = 255, $M \neq 0$, it is reserved for special value (NAN)

Note: Let E = 255, M = 0; it is used to represent $\pm$ infinitive

47. (A)

$$R_P = \text{C1D00000} =$$

$$\begin{array}{c|c|c} 1 & 100\ 0011 & 1010000000....0(32 \text{ bits}) \\ S & E = 131 & M \end{array}$$

$$\text{Value} = (-1)^S * 1.M \times 2^{E-127} = (-1) * 1.1010 \times 2^4$$
$$= (-1)11010 \times 2^0 = (-)11010_2 = -26$$

$$R_R = 41\text{D}00000 = 0 \left| \begin{array}{c} 10000011 \\ S \\ E = 131 \end{array} \right| \begin{array}{c} 10100000....0 \\ M \end{array}$$

$$= (-1)11010 \times 2^4 = +11010 = +26$$

Hence P + R = 0 True

R = P +Q = False

26 = –26 – 14 False

$$R_Q = C1600000 = 1 \left| \begin{array}{c} 10000010 \\ S \\ E = 130 \end{array} \right| \begin{array}{c} 1100000....0(32 \text{ bits}) \\ M \end{array}$$

$$\text{Value} = (-1)^s * 1.M \times 2^{E-127}$$
$$= (-1)^1 * 1.1100 \times 2^{130-127}$$
$$= (-)1110 \times 2^0 = -14 = Q$$

$R > Q$ = True; $R + Q = 26 - 14 = +12$ True

48. B,C

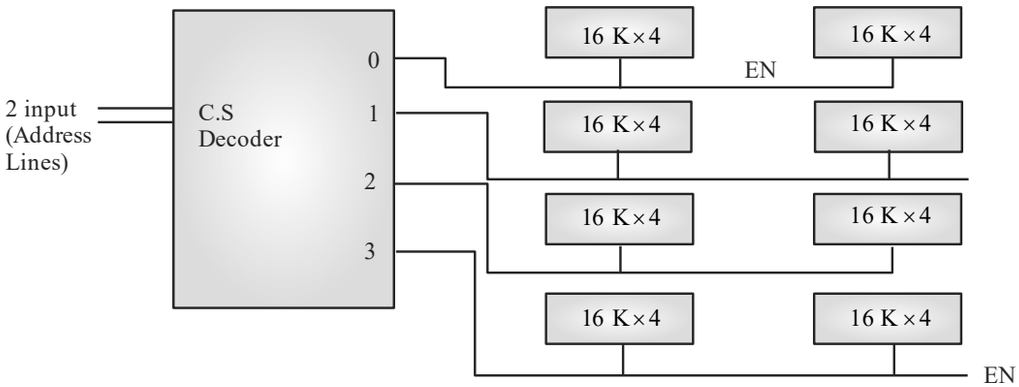
$$\text{Target size} = 64\text{ K} \times 8 = 2^{16} \times 8$$

$$\text{Basic size} = 16\text{ K} \times 4 = 2^{14} \times 4$$

$$\text{Total no. of chips needed} = \frac{64\text{ K} \times 8}{16\text{ K} \times 4} = 4 \times 2 = 8$$

These '8' chips are arranged in 4 rows and 2 columns.

No. of free address lines $= 16 - 14 = 2$



49. B,C,D

Option (A) is false because Index register addressing mode instruction requires one operand read from memory but it is not needed for immediate addressing mode instruction.

Option (B) and (C) are True. Option (D) is true because PC Relative addressing mode is also known as position independent addressing mode.

50. (A)

P = 2 because generally DMAC is used to transfer the data from secondary memories

Q = 1 because interrupt driven IO used for connecting printer and monitor.

R = 4 CPU used NMI for checking the power failure case

S = 3 Flag register is connected to the output of the ALU.

51. 1024

Since count register size is 16 bits one bus request is used to transfer 2^{16} Bytes $= 64$ KB

Maximum size of the data to be transferred for 16 request

$$= 16 \times 64 \text{ KB} = 1024 \text{ KB}$$

52. B,C

Option (A) is false because PC Relative addressing mode is used for both forward and backward jump that is specified by the MSB of the displacement.

Option (D) is false because indexed addressing mode is used for array implementation

53. 13.5

I_1, I_2 and I_6 are executed for only one time but I_3, I_4 I_5 are executed for 6 times.

(Count = 6).

Total no. of clock cycles required

$$I_1 = 1,\ I_2 = 1,\ I_3 = 6,\ I_4 = 6$$

$$I_5 = 12,\ I_6 = 1 = 27$$

$$f_{clk} = 2 \text{ GHz},\ T = 0.5 \text{ ns}$$

$$\text{Total time} = 27 \times 0.5 \text{ ns} = 13.5 \text{ ns}$$

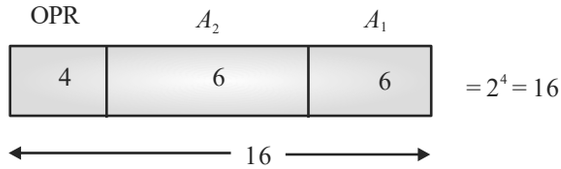
54. 5

Instruction cycle is the combination of both Fetch cycle and execute cycle.

Fetching requires 2 clocks. @ R_1 is register indirect addressing mode i.e. CPU reads the operand from memory that address is given by R_1 hence it requires 2 clocks and for adding operation one more clock is needed. Hence total no. of clocks needed is $2 + 2 + 1 = 5$

55. 9

Maximum no. of two address instruction is



But it used 'X' only, the no. of free combinations $= (16 - X)$, each one free

combination produces 2^6 one address instructions.

i.e. $(16-X)\times 2^6 = 448$

$$16-X = \frac{448}{64} = 7$$

$$X = 9$$

56. B,C,D

Horizontal microprogram control word required longer size control word hence it requires larger size control space. Option (A) is false it is used to generate more no. of control signals in parallel hence degree of parallelism is high.

It does not require signal encoders and decoders option (B), (C) & (D) are true.

57. B,C

SP = 5926

Memory is word addressable i.e. CPU access one memory location for reading PC and 2nd memory location content.

Hence RET requires POP operations; the SP content is incremented for stack going downward method and decremented fir stack going upward method.

Stack	Stack
Goes upward	Goes down ward
5926 –2	5926 + 2
= 5924	= 5928

58. 58

Total number of control signals = 72

Hence 72 bits are needed for horizontal microprogram control word but for vertical microprogram control word Log_2n bits are sufficient for 'N' signals, Hence vertical system needs $6+5+3=14$

Hence, it saves 58 bits.

59. A,D

Option (A) is true and option (C) is false because when there is no branch prediction, CPU stops the fetching of new instruction until completion of branch instruction execute stage option (B) is false arithmetical instruction takes shorter time than conditional branch instruction option (D) is True because conditional code resister is also known as flag register.

60. 0.87

$$f_{clk} = 2 \text{ GHz}; T_{CLK} = 0.5 \text{ ns} = T_{\text{seg}}$$

Hence for executing the non branch instruction, only 0.5 ns time is sufficient, non branch instructions = 75% and branch instructions = 25% CPU finds the target address for the branch instruction means, it requires 3 stalls (3 segment delays)

Average time

$$= \left(0.75(1+0)\times T_{\text{seg}}\right) + \left(0.25\times(1+3)*T_{\text{seg}}\right)$$

$$= (0..75\times 0.5)\text{ns} + \left(1\times 0.5 \text{ ns}\right) = 0.875 \text{ ns}$$

61. 8942

Address bus size = 16 bit, hence maximum no. of memory registers to be addressed

$= 2^{16} = 64 \text{ K} = 65536$; but 56594 memory locations are used for programs and data storage, the no. of IO devices permitted.

$= 65536 - 56594 = 8942$

62. A,C,D

Option (A) is true, input and output have load and store instructions respectively.

Options (B) is false because IO RD and IO WR control signals are used in IO mapped IO only

Options (C) is true because since memory address size is 16 bit maximum no. of IO devices to be addressed

$$= 2^{16} = 64 \text{ K} = 64\times 1024 = 65536$$

Option (D) is True because, it is not possible to use the memory register after connecting IO device.

63. 0.003

$$f_{clk} = 1 \text{ GHz}; T = 1 \text{ ns}$$

POP R_1 instruction cycle requires instruction fetch (fetch + decode) and operand read form

stack to R_1 in execute cycle. Hence it requires 3 clock. Total instruction cycle time

$$= 3 \times 1 \text{ ns} = 3 \text{ ns} = 0.003 \ \mu\text{sec}.$$

64. (D)

On interrupt, processor save PC, processor status word (PSW) and other required thing, PC is not only thing which saved.

65. (D)

A sector is the smallest physical storage unit on a disk and is almost always 512 bytes (0.5 kB) in size.

Collection of sectors are called tracks and collection of tracks are called cylinder.

Hence, all the option are true.

Therefore option (D) is incorrect.

66. 1.08

Using Amdahl's law

$$\text{Speedup}(S_1) = \frac{1}{0.7 + \frac{0.3}{6}} = \frac{1}{0.7 + 0.05}$$

$$= \frac{1}{0.75} = \frac{4}{3}$$

$$\text{Speedup}(S_2) = \frac{1}{0.8 + \frac{0.2}{20}} = \frac{1}{0.8 + 01}$$

$$= \frac{1}{0.81} = \frac{100}{81}$$

$$\frac{\text{Speedup}(S_1)}{\text{Speedup}(S_2)} = \frac{\frac{4}{3}}{\frac{100}{81}} = \frac{4 \times 81}{3 \times 100} = 1.08$$

67. (B)

Speedup of K stage pipeline is K **.**

68. 26

Maximum value of word count register

$$= 2^{16} - 1 = 65535$$

DMA can transfer 65535 bytes maximum at a time.

Number of tunes DMA controller needs to be invoked

$$= \left\lceil \frac{1630 \times 1024}{65535} \right\rceil = [25.469] = 26$$

69. 4

2 bytes (16 bits) require time to transfer $= 2\mu s$

4000 bytes will take minimum time $4000\,\mu s = 4$ ms

70. (A)

LOAD	$R_1, 3000$	$// R_1 = 3000$
ADD	$R_2, R_1, (2000)$	$// R_2 = R_1 + M[2000]$
ADD	$R_3, (R_2), 0$	$// R_3 = M[R_2] + 0$ $= 40 + 0 = 40$

71. (A)

(b) Splitting reduces structural hazards.

(c) Stall filling possible, but not always.

(d) Register renaming reduces data hazards.

72. (C)

(A) and (B) adding AC using direct addressing, not immediate

73. (C)

16 flags, and one flag need to select, so $\lceil \log_2(16) \rceil = 4$ bits required

Address field length = 24 – (opcode) – (flag)

$$= 24 - 11 - 4 = 9 \text{ bits}$$

Instruction length = 24 bits

Memory size = Number of addresses × Instruction length $= 2^6 \times 24$ bits

$$= \frac{512 \times 24}{8} \text{ Bytes} = 1536 \text{ Bytes}$$

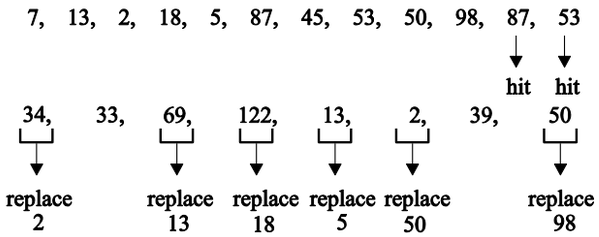
μ – opcode	Flag	Address
11	4	9

74. (B)

Maximum clock frequency is limited by the slowest pipeline stage. In (b), slowest pipeline delay is 4.5 ns and it is smallest among given options.

75. 6

$$\text{Number of sets} = \frac{\text{Number of blocks}}{\text{Associativity}} = \frac{32}{4} = 8$$



Set	
0	
1	33
2	~~2~~, ~~15~~, ~~50~~, ~~98~~, 34, 122, 2, 50
3	
4	
5	~~13~~, ~~5~~, 45, 53, 69, 13
6	
7	7, 87, 39

76. (A)

The DMA technique does not make use of the interrupt mechanism, that's why it is more efficient than the interrupt-driven technique for high volume I/O data transfer.

77. (C)

Write through protocol – Inclusion
Write back protocol – Coherence
RISC – Relatively few addressing modes
CISC –Variable length instruction format

78. (D)

When all stages of pipeline having same delay and buffer latency is zero then, for a single instruction execution time of pipeline CPU is equal to the execution time of non-pipelined CPU.

For a single instruction time taken on pipelined CPU is greater than or equal to the identical non-pipeline.

79. C)

WAR

$$I_1(R_2) - I_0(R_2)$$
$$I_2(R_5) - I_1(R_5)$$
$$I_3(R_3) - I_0(R_1)$$

WAW

$$I_3(R_1) - I_0(R_1)$$

WAR = 3 and WAW = 1

80. (B)

S_1 is correct, in write through all write operations are made to main memory as well as to the cache ensuring the main memory is always valid, thus it generates substantial memory traffic.

S_2 is false, in write back updates are made to main memory on the basis of dirty bit.

81. (B)

Multiplier	Pair with (q - 1)	Operation
1	0	SUB
0	1	ADD
1	0	SUB
0	1	ADD
0	0	Shift only
1	0	SUB
0	1	ADD
1	0	SUB

Total 3 ADD required

82. (A)

MOV R_1, 10 is immediate addressing mode.

83. (C)

For execution of the instruction, we have to consider the instruction fetch and operand fetch.
Instruction fetch = 1 cycle
Operand fetch = 2 cycles (due to indirect addressing mode)
So total 3 cycle required.

84. 0.64

0.64 [0.63 – 0.65]
Refreshments done in 1msec = 64
Refreshments done in

$$10^6 n\sec = 64 (\because 1n\sec = 10^6 n\sec)$$

Now refreshments done in

$$200n\sec = \frac{64\times 200}{10^6} = \frac{128}{10^4}$$

In 1 memory cycle, $\frac{128}{10^4}$ refreshes could be done

Time spent in doing $\frac{128}{10^4}$ refreshes

$$= 100n\sec \times \frac{128}{10^4} = 1.28n\sec$$

Out of 200nsec is spent in doing refreshments
Percentage of CPU time spent in refreshments

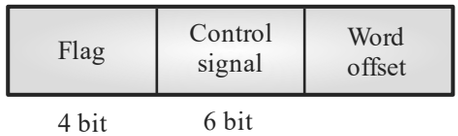
$$= \frac{1.28n\sec}{200n\sec}\times 100 = 0.64\%$$

85. 28

Cache is divided into 16 sets of 4 lines each, therefore 4 bits are needed to identify the set number.
Main memory consist of 2^{12} blocks. Therefore set + Tag length must be 12 bits.
So, Tag = 12 – 4 =8

Block size = 128 words = 7 bit
Thus, X = 8 bit, Y = 4
So, $X + 5Y = 8 + 4\times 5 = 8 + 20 = 28$

86. 11



Number of bits for flag $= \lceil \log_2 15 \rceil = 4$ bit
Number of bits for control signal $= \lceil \log_2 62 \rceil = 6$ bit
Length of control word = Flag + Control signals + Address
Also, number of the operations for 360 instructions $= 360\times 10 = 3600$
So, Address field $= \lceil \log_2 3600 \rceil = 12$ bits
So, Size of 1 control word = 12 + 4 + 6 = 22 bit
For 4 control words $= 4\times 22$ bits $= 88$ bits
i.e. $\frac{88}{8} = 11$ bits

87. 116.8

116.8 [116.8 – 119.9]
$t_p = 200$ ns $\quad n = 580$
$k = 5$
$\Rightarrow \quad (k+n-1)t_p$
$\Rightarrow \quad (5+580-1)\times 200$ ns
$\Rightarrow \quad 1165800$ ns $= 116.8$ ns

88. 1.42

By using Amdhal's law
$s = 4; f = 40\%$

$$s_{\text{overall}} = \left[(1-f) + \frac{f}{s}\right]^{-1}$$

Here f is most frequency used operation frequency and s is speed up factor.

$$s_{\text{overall}} = \left[(1-f) + \frac{0.4}{4}\right]^{-1}$$
$$= [0.6 + 0.1]^{-1} = 1.42$$

89. 352

Read access time $= HT + (1-H)(T_w)$

$= 0.9\times100 + 0.1\times(1000)\,n\text{sec}$

$= 190n\,\text{sec}$

Total Access time

$= (0.8\times190 + 0.2\times1000)\,n\text{sec}$

$= 352n\,\text{sec}$

90. A,C,D

High degree of parallelism (more than 1 control signal enabled at a time).

Little encoding (faster).

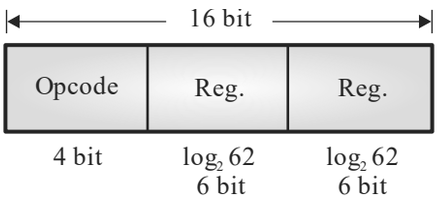
1 bit/control signal (longer control word).

91. A,B,C,D

In I/O mapped I/O mapping, the I/O devise are given a separate addressing region separate from the memory. These separate address spaces are known as 'Ports'

Interleaved DMA is a more complex type of DMA operation using this technique, the DMA controller takes over the system bus when the microprocessor is not using it.

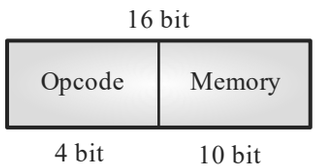
92. (B)



Number of 2 address instructions $= 2^4 = 16$

Number of free opcodes $= 16 - 12 = 4$

Number of 1 address memory reference instructions $= 4\times2^2 = 16$



Number of free opcodes $= 16 - 14 = 2$

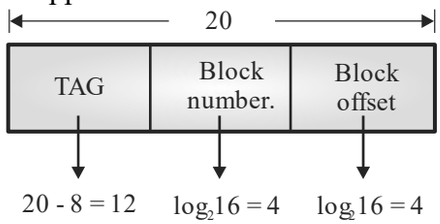
Number of 0 address instruction

$= 2\times2^{10} = 2^{11} = 2048$

93. (B)

Main memory address size $= 5\times4 = 20$ bits

Direct mapped cache:



1st pass

1. $O\times80000 =$ Compulsory misses
2. $O\times80008 =$ Hit
3. $O\times80010 =$ Compulsory misses
4. $O\times80018 =$ Hit
5. $O\times30010 =$ Compulsory

2nd pass

1. $O\times80000 =$ Hit
2. $O\times80008 =$ Hit
3. $O\times80018 =$ conflict misses
4. $O\times80018 =$ Hit
5. $O\times30010 =$ Conflict misses

So, for 10 passes

Compulsory misses = 3

Conflict misses $= 2\times9 = 18$

94. (B)

Tasks $\rightarrow m$

Stages in pipeline = n

Without pipelining number of cycles required to execute m tasks = n m.

(Each task required n cycle)

When we pipeline the tasks for I s t task it requires n cycles and for next (m - 1) 1 cycle for each

(m – 1) tasks

So total cycles required with pipelining

$= n + (m-1) \times 1$

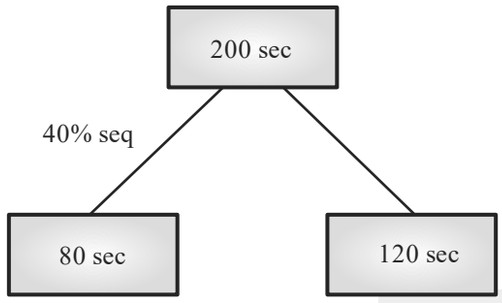
$= (n + m - 1)$

Speed gained by pipeline

$$= \frac{\text{Number of cycles without pipelining}}{\text{Number of cycles with pipeline}}$$

$$= \frac{mn}{(n+m-1)}$$

95. (C)

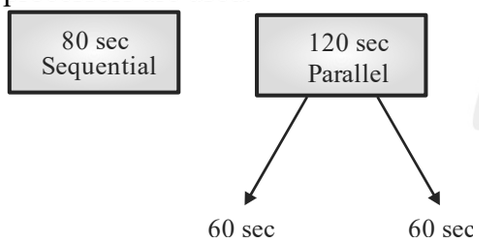


A single processor which requires 200 ns for computation.

It's 40 % computation is serial i.e. 80 s.

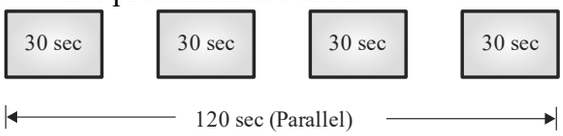
Then 60% will be parallel i.e. 120 s.

If 2 processors are used.



Here maximum elapsed time = (80 + 60) sec = 140 sec

If 4 processors are used.



Here maximum elapsed time = (80 + 30) = 110 sec

96. (C)

Bias $= 2^{8-1} = 127$

Biased exponent (B.E.)= Actual exponent +Bias

Also 8^{12} can be written as $= (2^3)^{12} = 2^{36}$

Now, B.E. $= 36 + 127 = 163$

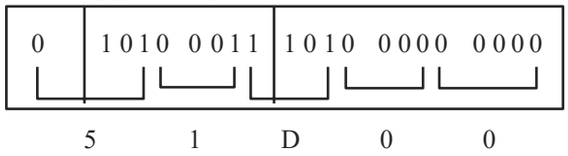
Representing exponent in binary

$$(163)_2 = (10100011)_2$$

Representing mantissa in binary

$$(0.625)_2 = (0.10100000000)_2$$

Floating point representation will be



= Ox51D00

97. (C)

$I_1 : 5000 - 5003$

$I_2 : 5004 - 5011$

$I_3 : 5012 - 5015$

$I_4 : 5016 - 5023$

$I_5 : 5024 - 5027$

$I_6 : 5028 - 5029 \rightarrow$ Interrupt

$I_7 : 5030 - 5033$

Return address 5028 is pushed on to stack due to halt.

98. (C)

With loop level // ^{sm}:23 cycles

Without loop level// ^{sm}:26 cycles

Number of cycle saved = (26–23) = 3

99. (B)

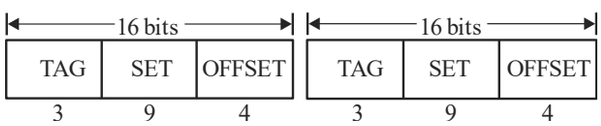
Block size = 16 byte = 2^4 byte =4 bits

Blocks in main memory = 2^{10}

So number of sets $= \frac{2^{10}}{2^1} = 2^9 \Rightarrow 9$ bits

Number of bits in physical address

$= 2^{16}$ byte $\Rightarrow 16$ bits



$$\underbrace{111}_{[E\ 0\ 1\ F]}\underbrace{0000000001}_{\text{SET}}\underbrace{1111}_{}$$

$$\underbrace{111}_{[E\ 2\ 0\ 8]}\underbrace{0001000001}_{\text{SET}}\underbrace{1000}_{}$$

SET value$_1$= 000000001

= Decimal value $= (1)_{10}$

SET value$_2$= 000100001

= Decimal value $= (32)_{10}$

Difference $= \text{SET}_2 - \text{SET}_1$

$= 32 - 1 = (31)_{10}$

100. 5.14

L_1 miss rate $= \dfrac{30}{2000} = 0.015$

L_2 miss rate (we need to take local miss rate)

$= \dfrac{20}{30} = 0.66$

Average memory access time= Hit time (L_1) + miss rate (L_1) [Hit time (L_2) + Miss rate $L_2 \times$ Miss penalty]

$= 1 + 0.015[12 + 0.66 \times 400]$

$= 1 + 4.14 \Rightarrow 5.14$ clock cycles

101. 0.066

$$\text{Sepeedup} = \frac{\text{Pipe line depth}}{1 + \text{Branch freqency} \times \text{Branch penalty}} \geq 5$$

$$\Rightarrow \quad \frac{6}{1 + f \times 3} \geq 5$$

[$\because$ Branch penalty = Branch predicted stage –1]

$5 + 15f \leq 6$

$15f \leq 6 - 5$

$15f \leq 1$

$f \leq \dfrac{1}{15}$

$f \leq 0.066$

102. 12

Since operand forwarding is not maintained, so wait till instruction finish.

	IF	ID	OF	PD	WB
SUB	1	1	1	1	1
MUL	1	1	1	2	1
ADD	1	1	1	1	1
DIV	1	1	1	4	1

	1	2	3	4	5	6	7	8	9	10	11	12	13
I_0	IF	ID	OF	PD	WB								
I_1		IF	ID	OF	PD	PD	WB						
I_2			IF	ID	OF	OF	PD	WB					
I_3			IF	ID	-	-	OF	PD	PD	PD	PD	WB	

So, total 12 cycles required.

103. 1.5128

Average time to read/ write = Seek time + Rotational delay + Effective transfer time

Rotational delay $= \dfrac{1}{2}\left(\dfrac{60}{60000}\right) = 0.5$ msec

Seek time $= 2 \times 0.5$ msec $= 1$ msec

Disk transfer time $= \dfrac{128}{80 \times 10^6} = 0.0016$ msec

Effective transfer time =

8×0.0016 msec $= 0.0128$ msec

So, average time to read/write = 1 msec + 0.5 msec+ 0.0128 =1.5128

104. 152

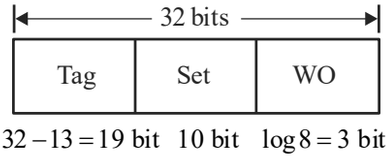
8 – way set associative cache

Cache memory size = 64 KB

Block size = 8 bytes

$$\text{Number of lines} = \frac{64\ \text{KB}}{8\,\text{B}} = 8\text{K} = 2^{13}$$

32 bit virtual address



Tag memory size = Number of lines of cache × Number of tag bits

$$= 2^{13} \times 19 = 152\,\text{K bits}$$

105. 0.18

$$\text{Number of sets} = \frac{8}{2} = 4$$

20 mod 4 = 0 → miss
17 mod 4 = 1 → miss
21 mod 4 = 1 → miss
32 mod 4 = 0 → miss
20 mod 4 = 0 → miss
16 mod 4 = 0 → miss
27 mod 4 = 3 → miss
22 mod 4 = 2 → miss
7 mod 4 = 3 → miss
16 mod 4 = 0 → hit
32 mod 4 = 0 → miss

$$\text{Hit ratio} = \frac{\text{Total hit}}{\text{Total reference}} = \frac{2}{11} = 0.18$$

0	~~20~~ 32	~~32~~ 16
1	17	21
2	22	7
3	27	7

106. 64

Count register size =34 bit

So, it can transfer 2^{34} bytes of data in 1 time.

∴ Total data transferred in 4 times.

$$= 4 \times 2^{34}$$

$$= 16 \times 4 \times 2^{30} = 64\ \text{GB}$$

107. B,C,D

- In indexed addressing mode, effective address is calculated by adding index value to the register content.
- In relative addressing mode effective address is calculated by adding relative value to the register content.
- In based addressing mode effective address is calculated by adding constant value to the base register content.

108. A,B,D

There is no conflict between two read so there is no hazard.

- Option (b) is case of anti data dependency.
- Option (c) is true data dependency because of subsequent write and read
- Code reordering, forwarding, stall insertion are the methods used to handle data hazards.

109. (A)

In Program controlled I/O method, the processor constantly checks the status flags, and when it finds that the flag is set it performs the appropriate operation.

Hence, the correct option is (A).

110. (B)

In synchronous I/O process performing I/O operation will be placed in blocked state till the I/O operation is completed. An ISR will be invoked after the completion of I/O operation and it will place process from block state to ready state

In asynchronous I/O, a process need not stay in the blocked state until the I/O is complete. It can place a request for I/O to the kernel, and resume with the execution. After the I/O operation is

completed, a signal is directed to the process notifying the completion
Hence, the correct option is (B).

❖❖❖❖