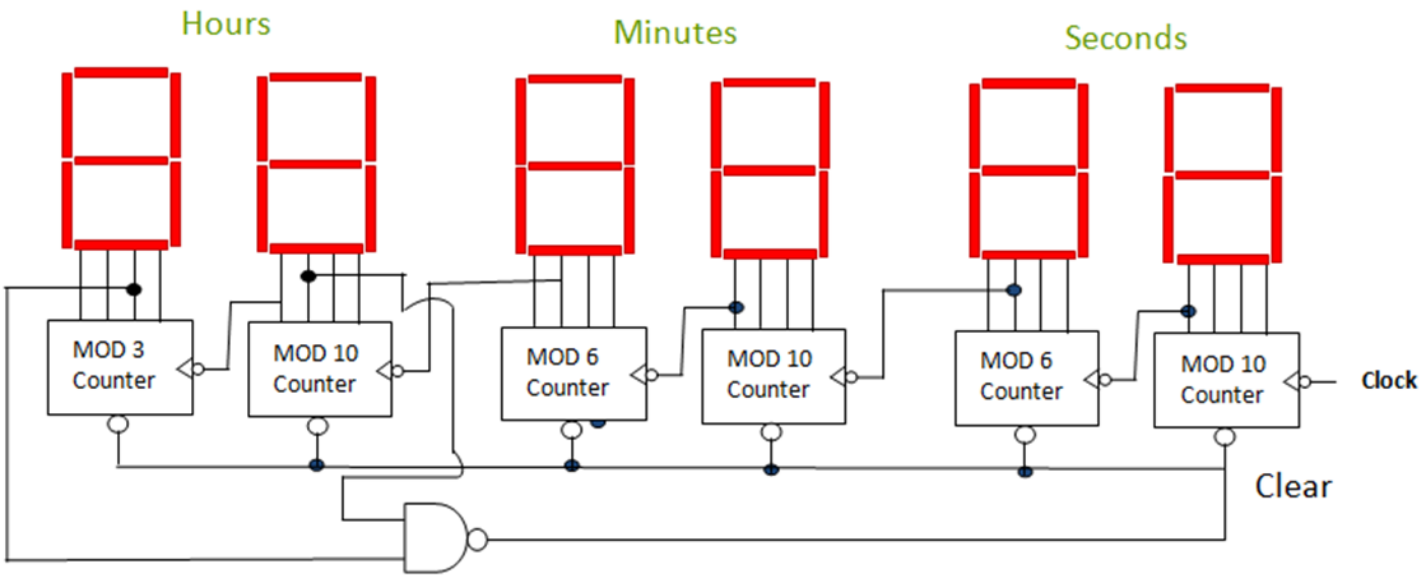
LABORATORY REPORT

ECE279

Basic Electrical and Electronics Engineering



DIGITAL WATCH

Name of the Student :……
Registration Number/Roll No:……
Section and Group……

LOVELY PROFESSIONAL UNIVERSITY
Transforming Education Transforming India

	Course Outcome Statements	Applicable to
CO1	Learn to use basic electrical & electronics measuring instruments and component specific ratings.	All practical
CO2	Use basic electrical laws and theorems to analyse DC circuits	P1 and P2
CO3	Build virtual applications with at least one sensor module by programming microcontroller board.	P6
CO4	Make use of various digital & analogue ICs and conduct their functionality test.	P3, P4, P5, P7, P8
CO5	Assemble various electrical & electronics components on the breadboard and create circuit connections.	P1 to P5, P7, P8
CO6	Design and analyse combinational and sequential circuits.	P5, P7, P8

Table of Contents

General Safety guidelines for the students

- Use only tools and equipment with non-conducting handles when working with electrical devices.
- When checking an operating circuit, keep one hand either in a pocket or behind your back to avoid making a closed circuit through the body.
- Never plug leads into power source unless they are connected to an established circuit.
- Avoid contacting circuits with body parts or wet materials.
- Use wires of appropriate length. Do not allow them to drape over your equipment. Avoid splices, which create live surfaces. When running a pair of wires to adjacent terminals, twist the wires together so they don't dangle. This also neatens your work and will save time.
- All current transmitting parts of any electrical devices must be enclosed.
- Maintain a work space clear of extraneous material such as books, papers, and clothes.
- Never change wiring with circuit plugged into power source.
- Don't depend on switches to de-energize a circuit. Pull the plug out from the socket/outlet.
- If an individual comes in contact with a live electrical conductor, do not touch the equipment, cord or person. Disconnect the power source from the circuit breaker or pull out the plug using a leather belt.
- Place the IC's Properly in the bread board, don't break the IC pins by forcefully inserting in bread board.
- Switch off the power supply when not in use.
- Always cut wire leads so the clipped wire falls on table top and not towards others.
- Shoes must be worn at all times.
- Remove all loose conductive Jewelry and trinkets, including rings, which may come in contact with exposed circuits. (Do not wear long loose ties, scarves, orother loose clothing around machines.
- Don't switch ON the power supply without confirming the connections from the lab instructor.
- When making measurements, form the habit of using only one hand at a time. No part of a live circuit should be touched by the bare hand.
- Keep the body, or any part of it, out of the circuit. Where interconnecting wires and cables are involved, they should be arranged so people will not trip over them.
- Be as neat as possible. Keep the work area and workbench clear of items not used in the experiment.

Evaluation Mechanism and Sequence of events for the course

1. **Continuous assessment Practical (CAP):** There will be 4 Continuous Assessment for Practical (CAP). Each evaluation will be for 30 marks. and in CAP: 3 best out of 4 will be considered. All the CAP(except CAP-1: subjective questions to evaluate circuit connection ability on breadboard) will be MCQ based with 15 questions of two marks each. CAP evaluates the student ability to conduct the practical, knowledge of equipment's/components involved and related theory. A printed question paper will be shared with the students to conduct CAP.

2. **Evaluation mechanism in Written Test Practical (WTP)**: Both WTP-1, WTP-2 Examinations are compulsory. Here faculty assigns one practical to each student and student uses answer book to demonstrate practical related theory, components, Circuit diagram, breadboard diagram, procedure, observation table (including %age error), precautions and sources of error for 20 minutes and later individually perform the same practical for about 15-20 minutes to complete observations and calculations. Both write up and Practical performance gets the same weightage of 15 marks out of total 30.

3. **Mid Term Practical (MTP):** No Mid-term exam is applicable for this course

4. **End Term Practical (ETP):** This may be conducted in next teaching week after WTP-2. Student will get any one practical to perform in the ETP out of 8 practical for being evaluated on Viva, Written and Performance. Weightage of evaluation of answer book is 20%, viva is 30% and Performance of the students on the components/simulations to get results amounts to 50%.

   Note: *In case students missed some Lab classes due to holidays, then faculty will plan same number of CAPs in extra classes (not to be conducted in lab), which will be announced to the students on LPU Live, 7 days in advance.*

Sequence of Lab Activities

Activity	Week Number	Remarks
Practical 1	Week 1	*Content for CAP-1*
Practical 2	Week2	
CAP-1	Week 3	
Practical 3	Week 4	*Content for CAP-2*
Practical 4	Week 5	
CAP-2	Week 6	
WTP-1	Week7	*Lab Performance for P1- P4*
MTE	Week 8	*Not Applicable*
Practical 5	Week 9	*Content for CAP-3*
Practical 6	Week 10	
CAP-3	Week 11	
Practical 7	Week 12	*Content for CAP-4*
Practical 8	Week 13	
CAP-2	Week 14	
WTP-2	Week 15	*Lab Performance for P5- P8*
ETP	Week 16	*Lab Performance for P1-P8 and write up*

EXPERIMENT No.1

Aim: Implement Kirchhoff's Voltage Law and Current Law.

Learning Objective: 1. To identify values of resistances using color coding scheme.

2. To use ammeter and voltmeter
3. To verify KVL and KCL theorems.
4. To use breadboard and make connections

Apparatus required:

S. No.	Items	Specifications	Quantity
1	DC Voltage source	0-20V	01
2	Resistors	330 ohms	05
3	Ammeter	Digital/Analog	01
4	Voltmeter	Digital/Analog	01
5	Connecting wires	As per requirements	

1. **Kirchhoff's Voltage Law** states that the algebraic sum of all the voltages around any closed path (loop or mesh) is zero.

Applying Kirchhoff's voltage law to the first (loop with voltage source) and the second loops (without voltage source) in the circuit of **Figure 1**

Loop 1: $-Vs + V_1 + V_2 + V_5 = 0$ (1),

Loop 2: $V_2 + V_3 + V_4 = 0$ (2)

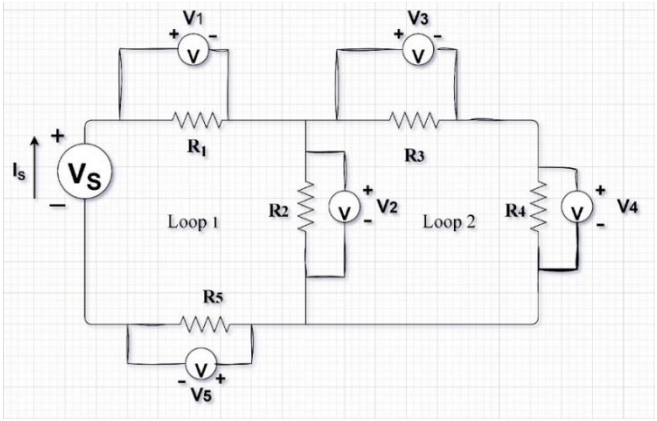


Figure 1 Voltage measurement across circuit elements

2. **Kirchhoff's Current Law** states that the algebraic sum of all the currents at any node is zero.

Applying Kirchhoff's current law to the first four nodes in the circuit shown in **Figure 2** yields the following equations; In Figure 2 Clockwise Current: through voltage source is I_V, through R1 is I_1, through R2 is I_2 , through R3 is I_3 , Current through R4 is I_4 , and Current through R5 is I_5 ,

Let's consider that node **e** is a reference node and is chosen as GND. V_a, V_b, V_c, V_d are node voltages at points **a, b, c** and **d** respectively.

Node a: $-I_s + I_1 = 0$,Node b: $I_1 = I_2 + I_3$, Node c: $I_3 = I_4$, Node d: $I_2 + I_4 = I_5$

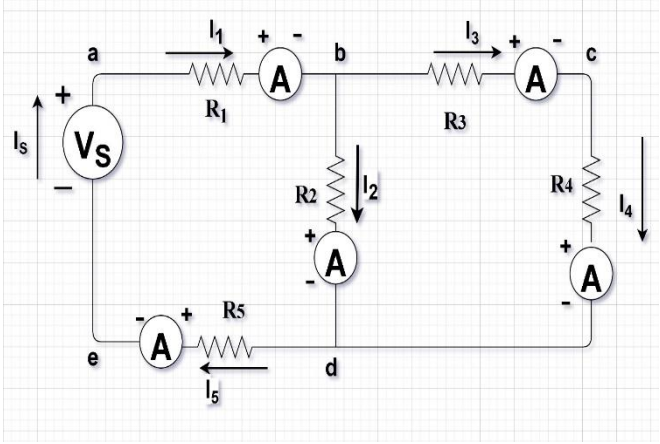
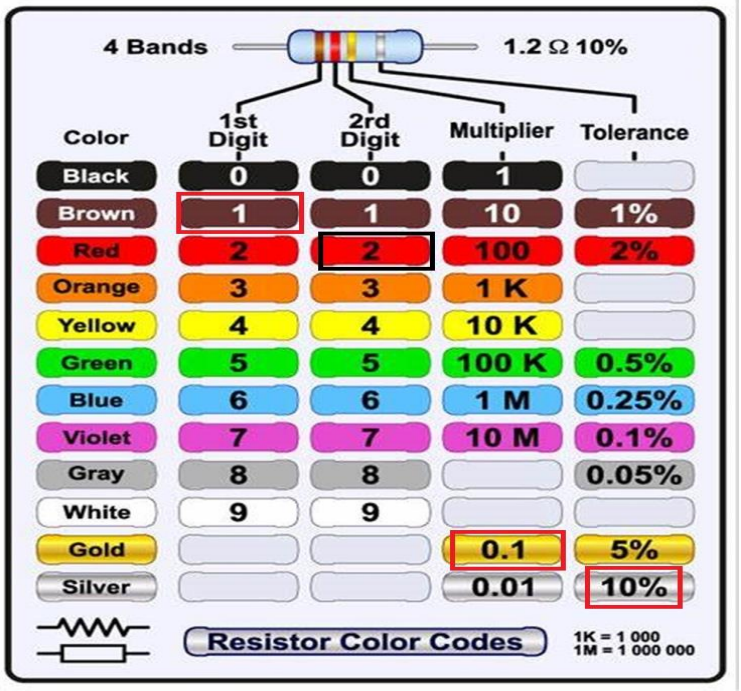


Figure 2 Current measurement through circuit elements

3. Reading Resistor with color code:

The color code is used to specify the resistance value, the tolerance value, and sometimes the reliability or failure rate. The number of bands varies from three to six. At a minimum, two bands indicate the resistance value and one band serves as multiplier.



The four-band color code is the most common variation. These resistors have two bands for the resistance value, one multiplier and one tolerance band. In the example shown here, the 4 bands are green, blue, red and gold. By using the color code chart, one finds that green stands for 5 and blue for 6. The third band is the multiplier, with red representing a multiplier value of 2 (10^2). Therefore, the value of this resistor is $56 \times 10^2 = 56 \times 100 = 5600\ \Omega$. The gold band means that the resistor has a tolerance of 5%. The resistance value lies therefore between 5320 and 5880 Ω (5560 ± 5%). If the tolerance band is left blank, the result is a 3-band resistor. This means that the resistance value remains the same, but the tolerance is 20%. **For 5 band resistors**, the first three bands indicate the significant digits, the fourth band is the multiplication factor, and the fifth band represents the tolerance. Let us consider another example (say); brown (1), yellow (4), violet (7), black ($x10^0 = x1$), green (0.5%) represents a resistor of 147 Ω with a tolerance of 0.5%. The tolerance represents deviation from the normal value. It is measured at 25 ^{0}C with no load applied and is generally expressed as ±%.

Resistance Value of 330ohm as Band1: Orange, Band2: Orange, Band3: Brown=> 33x10=330∓ tolerance (5% Gold, 10% Silver)

4. **Least count of Voltmeter and Ammeter**

In the given **figure 3** below, total range is up to 3V for voltmeter and 1000 mA for ammeter.

Least count = $\frac{Total\ \boldsymbol{range}\ of\ meter}{Total\ \boldsymbol{number}\ of\ division}$

Least count of voltmeter = 3/30 = 0.1 V

Least count of ammeter = 1000/50 = 20mA

Reading of Voltmeter = Number of divisions scaled by the pointer * Least count of voltmeter = 21*0.1=2.1V

Reading of Ammeter = Number of divisions scaled by the pointer * Least count of Ammeter= 15 *20mA= 0.3A=300mA

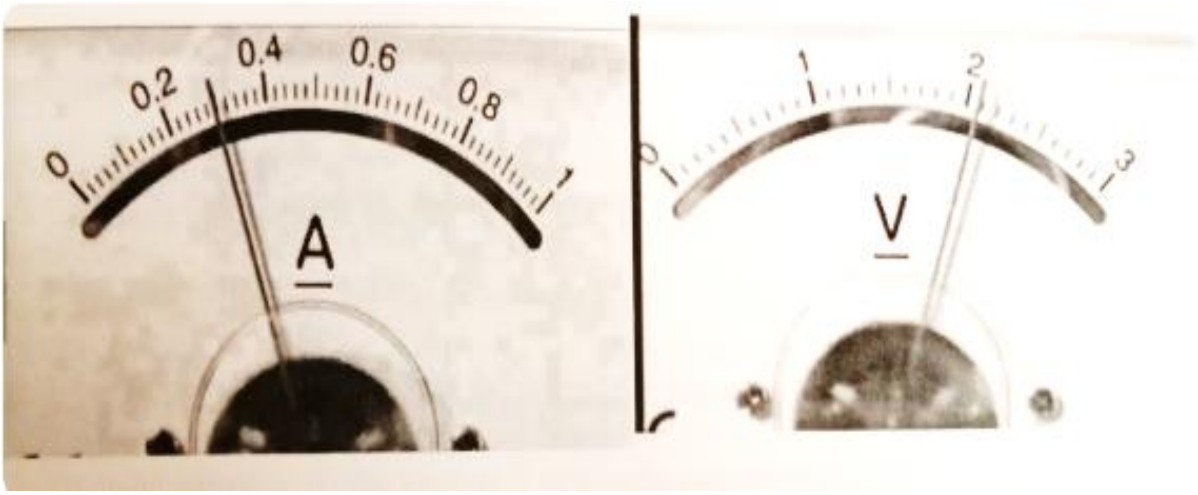


Figure 3: Measurement of Current and Voltage using Ammeter and Voltmeter

5. **Half-Breadboard for circuit implementation:**

Table 1: Internal connections of holes through metal strip

	Internally connected
W column	Hole 1 to 25, vertically
X Column	Hole 1 to 25, vertically
Y Column	Hole 1 to 25, vertically
Z Column	Hole 1 to 25, vertically
	Internally connected
Row-1	Holes A B C D & E, horizontally
Row -1	Holes F G H I & J, horizontally
Row-2	Holes A B C D & E, horizontally
Row -2	Holes F G H I & J, horizontally
And so on till 30th row	

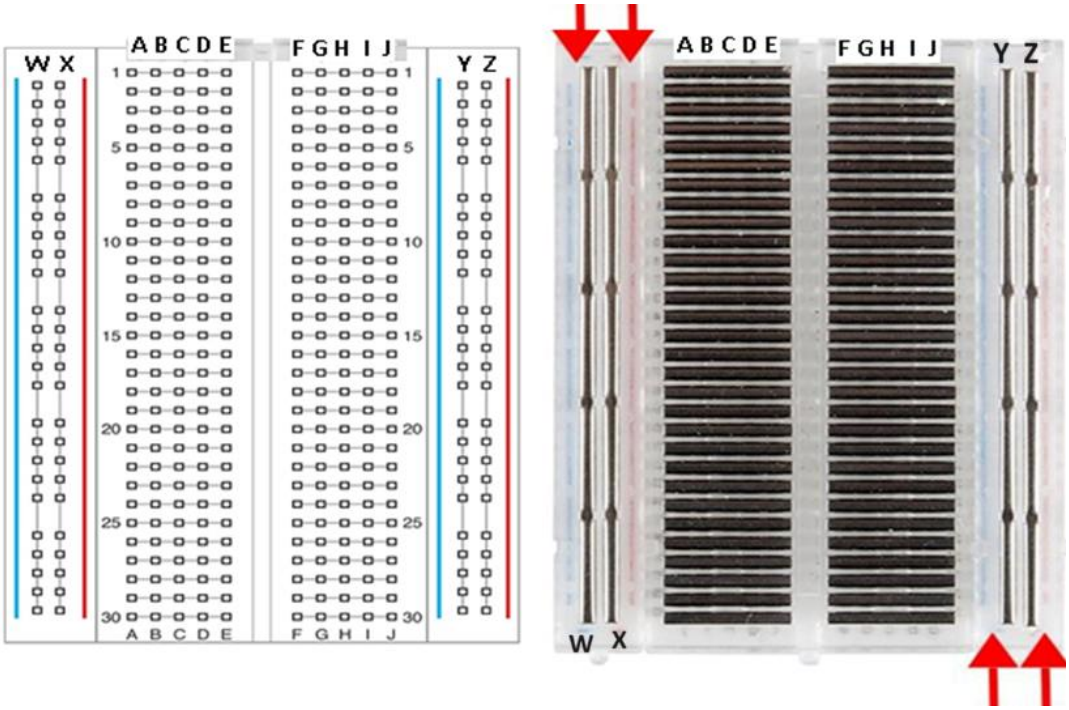


Figure 4: Front view and backside view of Half Breadboard

6. Digital Multimeter

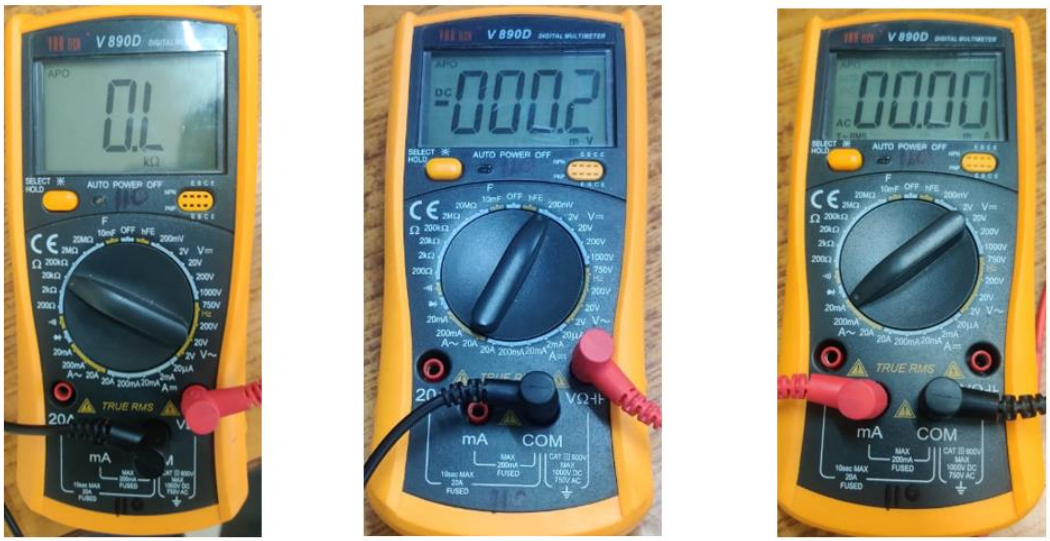
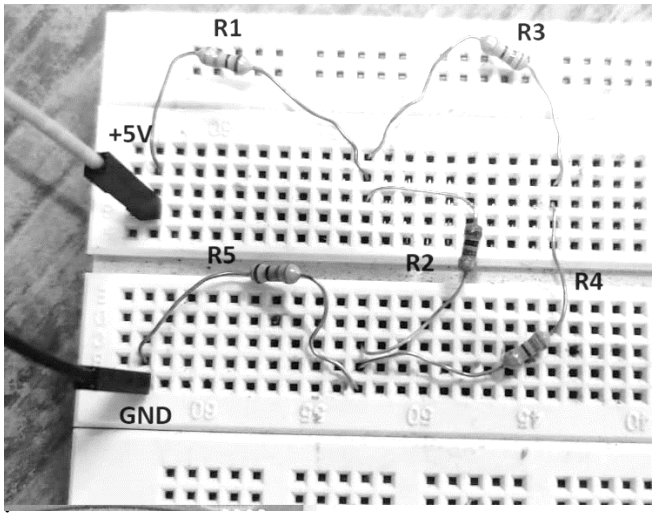


Figure 5: R, V and I Measurement Settings of Multi-meter

Procedure:

1. Construct the circuit as shown in *Figure below* using the values below: R_1 = 330 Ω R_2 = 330Ω, R_3 = 330Ω, R_4 = 330Ω, R_5 = 330 Ω.
2. Set the Variable Power Supply (Vs) to 5 Volts.
3. Accurately measure all voltages and currents in the circuit using the Digital/Analog (as shown in Figure 5/3) Meter



4. Record the measurements in the observation and calculation table.
5. Find $\%age\ Error = ([V\_Calculated - V\_Measured)/V\_Calculated]x100$
6. Verify KVL for the loops in the circuit using equations of Results and Discussion section.
7. Verify KCL for the loops in the circuit using equations of Results and Discussion section.

WORKSHEET FOR STUDENT

Observation and Calculations: Vs=5V, R=330ohm

Resistance	*Theoretical Value using KVL and KCL Equations*		*Practical value using Ammeter and Voltmeter*			
	Voltage across R	Current in R	Voltage across R	%age error	Current in R	%age error
R_1						
R_2						
R_3						
R_4						
R_5						

Results and Discussion:

1. Verify the KVL principle using measured values for the equations below:

LOOP-1: $-Vs + V_1 + V_2 + V_5 = 0$,

LOOP-2: $V_2 + V_3 + V_4 = 0$

2. Verify the KCL principle using measured values for the equations below:

Node b: $I_1 = I_2 + I_3$

Node c: $I_3 = I_4$

Node d: $I_2 + I_4 = I_5$

Precautions:

1. All the connections should be perfectly tight.
2. Always connect ammeter in series and voltmeter in parallel

3. Use safety guards while working on live parts
4. Don't touch the bare conductor when supply is ON.
5. Supply should not be switched ON until and unless the connections are checked by the Faculty/Lab Instructor
6. Use proper wire for connections

Learning Outcome (expected):

1. Able to connect circuit on the breadboard.
2. Use voltmeter and ammeter on the breadboard and finding least count.
3. Read resistance values using formula "BB ROY of Great Britain Having Very Good Wife".
4. Calculate I and V across any circuit element.

Learning Outcome (what I have learnt):

1. How will you apply BB ROY formula on Resistances to find their values?

Ans:

2. How measuring current is different from measuring voltage?

Ans:

3. Draw Breadboard Circuit Diagram for Figure 1?

Ans:

4. Draw Breadboard Circuit Diagram for Figure 2?

Ans:

EXPERIMENT No.2

Aim: Apply Thevenin's theorem on DC circuits.

Learning Objective:

1. To implement the circuit on the breadboard and verify Thevenin's theorem.
2. To use voltmeter and ammeter.
3. To identify the values of the resistances using color coding scheme
4. To identify different sources of error.

Apparatus/Components required:

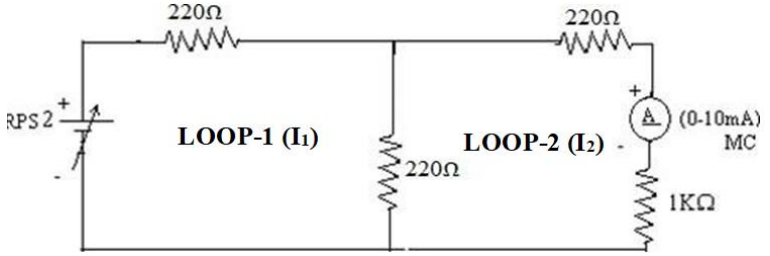
S No	Apparatus	Range	Quantity
1	Regulated Power Supply	(0-30V)	1
2	Ammeter/Digital multimeter	(0-10mA)	1
3	Voltmeter/ Digital multimeter	(0-30V)	1
4	Resistor	1Kohm, 220ohm, 330ohm	1,3,1
5	Bread Board	--	1

Statement: If we wish to find I or V across any element (load resistance) in the linear bilateral circuit, then we go for Thevenin's theorem. Any complex circuit can be broken down to only three elements such as V_{TH}, R_{TH}, and load resistance (R_L) using Thevenin's theorem. In this practical we will find I across 1Kohm Load resistance of **Circuit-1** using Thevenin's equivalent **Circuit-4.** We will prove that I_L of Circuit-1 and Circuit-4 are same.

Procedure:

1. Connections are given as per the circuit diagram.
2. Set 5Vvalue of voltage using RPS and note down the correspondingammeter readings as per **Circuit-1.**
3. **To find V_{TH}** : Remove the load resistance and measure the open circuit voltage using multimeter (VTH) as per **Circuit-2**.
4. **To find R_{TH}** : Remove the RPS and short circuit it and find the RTH using **multimeter in Circuit -3.**
5. Give the connections for equivalent circuit and set VTH and RTH and note the corresponding Ammeter reading in **Circuit -4**.
6. Verify Thevenin's theorem for theoretical and practical values using observation table and identify sources of error (if any).
7. Also find percentage error.

Circuit Diagrams: Circuit - 1: To find load current

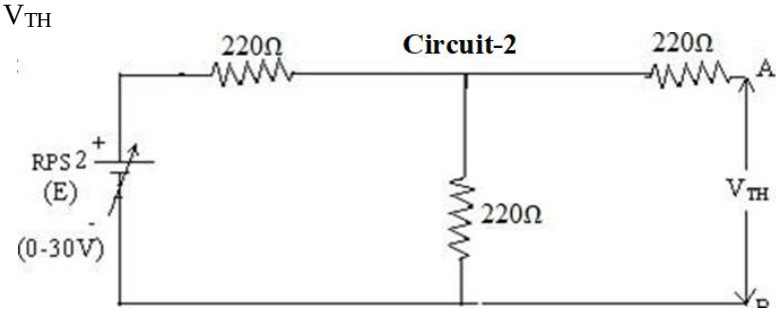


Supply Voltage =5V**,** I_1 and I_2 are in clockwise direction, $I_2 = I_L$

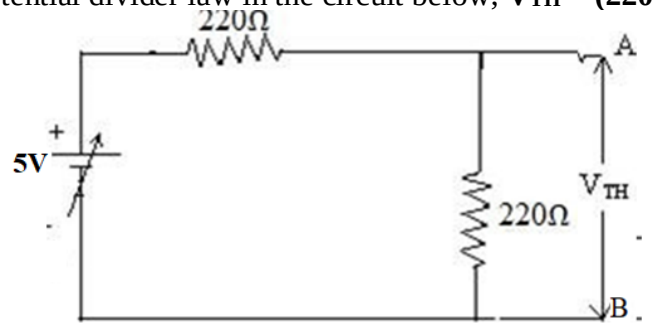
$5 = 220\ I_1 + 220\ (I_1 - I_2) \Rightarrow 440\ I_1 - 220\ I_2$ ----------(1)

0=220 I_2 +1000 I_2 + 220 (I_2- I_1); => -220 I_1 + 1440 I_2 ----------(2) => **I_2= 1.879mA= I_L**

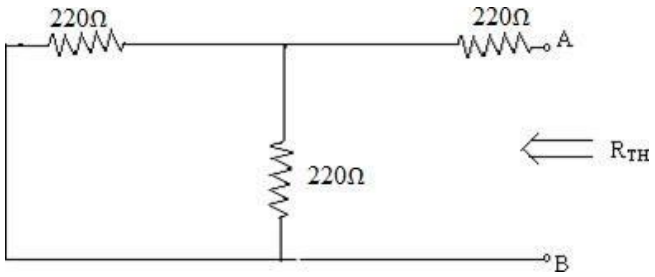
Circuit 2: To find V_{TH}



Since no current is passed through the resistance connected to point A, so it will not contribute to V_{TH} value, so using potential divider law in the circuit below, **V_{TH} = (220*5V)/440 =2.5V**

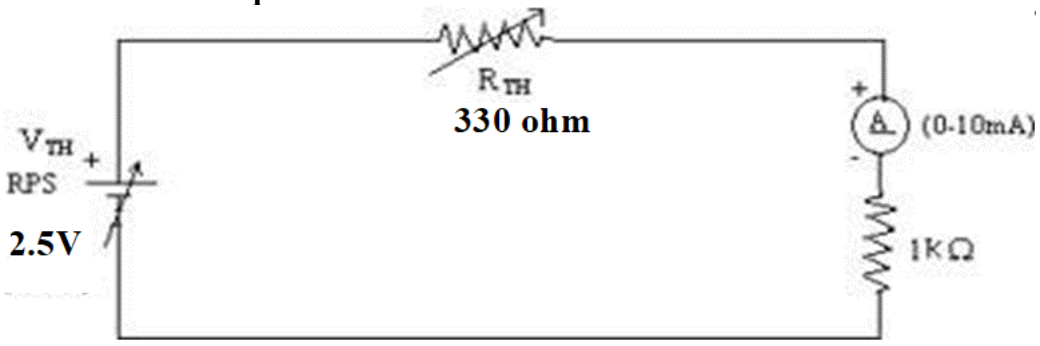


Circuit 3: To find R_{TH}



R_{TH} = 220 ohm connected to point A + Parallel combination of other two resistances
Parallel combination of other two resistances = (220*220)/(220+220)=220*220/440=110ohm
⇨ **R_{TH} =220+110=330ohm**

Circuit-4: Thevenin's Equivalent Circuit:



Current flowing through 1Kohm**, I_L= 2.5/(330+1000)= 1.879mA**

Precautions:

1. All the connections should be perfectly tight.
2. Always connect ammeter in series and voltmeter in parallel
3. Use safety guards while working on live parts
4. Don't touch the bare conductor when supply is ON.
5. Supply should not be switched ON until and unless the connections are checked by theFaculty/Lab Instructor
6. Use proper wire for connections

Worksheet of the student

Observation table: for Input Voltage =5V

	Power supply Voltage	**Thevenin's Voltage V_{TH} Circuit-2**	**Thevenin's Resistance R_{TH} Circuit-3**	**Load Current I_L (mA)**	
				Circuit -1	**Thevenin's equivalent Circuit-4**
Calculated value	5V				
Measured value					

$$\%age\ Error\ for\ V = ([V\_Calculated - V\_Measured)/V\_Calculated]X100$$

Results and Discussion: Calculation of %age Error

1. %age Error for V_{TH} =

2. %age Error for R_{TH} =

3. %age Error for I_L =

Learning Outcomes (expected):

1. Measure the values of Thevenin's voltage and resistance and create Thevenin equivalent circuit.
2. Able to use ammeter and voltmeter and breadboard
3. Identify different sources of error in this practical.
4. Prove that current flowing in load resistance (R_L) of Circuit-1 and Circuit-4 are same.

Learning Outcomes (what I have learnt):

1. What is advantage of creating Thevenin equivalent Circuit?
   Ans:

2. How to find Vth and Rth in Circuit-1?
   Ans:

3. Draw Bread Board Circuit Diagram/ Connection Diagram for Circuit-1, Circuit 2, Circuit-3 and Circuit-4
   Ans:

EXPERIMENT No. 3

Aim: Analysis of V-I characteristics of PN Junction diode.

Learning Objective(s):

1. To measure diode current and voltage in forward biased condition.
2. To test the diode for functioning.
3. To identify different sources of error.

Instruments/Components: A p-n junction diode, 30V DC power supply, 1Kohm, 0-30V voltmeter, 0−100mA ammeter and connecting wires.

Sr. No.	Components/Instruments	Range	Quantity
1.	IN 4007 for Si or DR-25 for Ge		1
2.	Regulated DC Variable Power Supply	0-30V	1
3.	Analog DC Voltmeter or Digital multimeter	0-1V/0-20V	1
4.	DC Ammeter (Digital Multimeter only)	0-30mA	1
5.	Resistance	1Kohm	1
6.	One Bread Board and Connecting Wires Single Strand 8-10 number		

Theory: A semiconductor PN junction diode is a two terminal electronic device (Di-electrode → Diode). The metal contacts taken out from p-region and n-region are called anode and cathode respectively. There are three possible biasing conditions and two operating regions for the typical PN-Junction Diode, they are: zero bias, forward bias and reverse bias.Figure 1 shows the symbol diagram of diode with its real appearance.

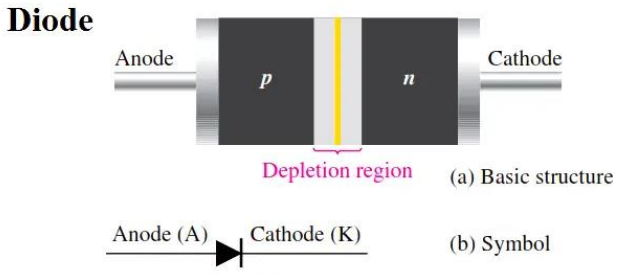


Fig. 1: Symbol of PN Diode

Forward Bias Condition: On forward biasing, initially no current flows due to barrier potential. As the applied potential exceeds the barrier potential the charge carriers gain sufficient energy to cross the potential barrier and hence enter the other region. The holes, which are majority carriers in the P-region, become minority carriers on entering the N-regions, and electrons, which are the majority carriers in the N-region, become minority carriers on entering the P-region. This injection of minority carriers results in the current flow, opposite to the direction of electron movement.

Calculation of Current limiting resistance, R = max power supply voltage/ current rating of the diode (50mA) = 20 / 50 mA or 30 /50 mA (supply 30 V)
Thus R = 400 to 600 ohm

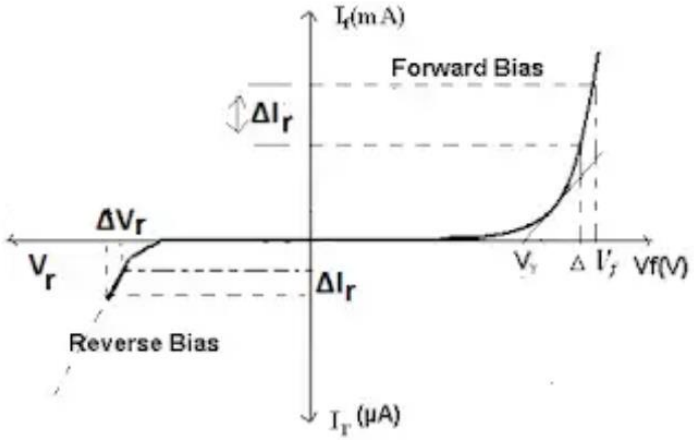


Fig. 3: VI characteristic of Forward Bias diode.

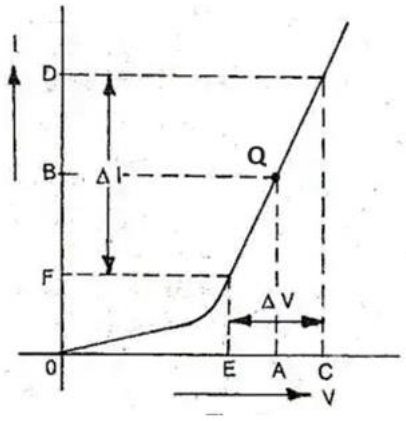


Fig 3.1 Dynamic resistance

Calculations from Graph: (*https://physicswave.com/dynamic-resistance-of-diode/)*

1. Cut in voltage (Vγ) (It is observed that Ge diode has smaller (0.3V) cut in voltage when compared to Si diode (0.7V). The reverse saturation current in Ge diode is larger in magnitude when compared to Si diode.

2. Static forward Resistance $R_{DC} = V_f / I_f$ Ω (at any quotient point Q (DC operating point) after diode gets on, where V/I is almost constant)
3. Dynamic Forward Resistance $r_{ac} = \Delta V / \Delta I$ Ω (Figure 3.1)

Procedure:

1. Before connection of the diode in the circuit test that diode is working or not, for that connect the diode the anode terminal with +ve probe of multimeter and cathode with –Ve probe and adjust the multimeter knob at Diode symbol as sown in figure 3. If value on multimeter is zero then diode is working fine and if lower voltage present in the diode it is due to charged capacitor.

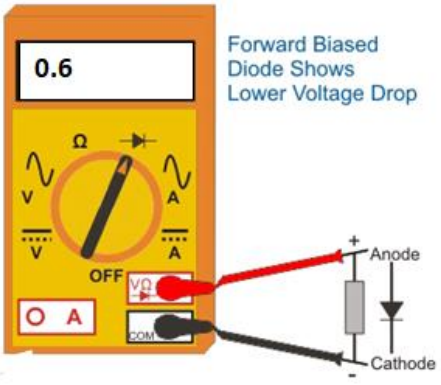


Fig: 4 Diode testing with multimeter.

1. Connect the circuit as shown in figure 6 using PN Junction diode
2. Before switch 'On' the supply, rotate power supply potentiometer fully in CCW (counter clockwise direction) to start experiment from Zero voltage otherwise excessive voltage can damage the diode and multimeter.
3. Connect Ammeter in series of Power supply positive terminal and anode of Diode to measure diode current ID (mA)

4. Connect Voltmeter across diode to measure forward voltage (V_F).
5. Vary the Regulated Power Supply voltage, Vs from 0 to 5 volt in steps as shown in observation table.
6. Note down ammeter (I_D) readings in the observation table.
7. Draw the VI characteristics of forward bias on the ***graph paper as shown in Figure 5***
8. ***Find Q point (V_D, I_D)*** *using maximum Power supply voltage (Vs), Current limiting resistance R.*

Precautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit. Avoid the heating of IC. Provide proper clock pulse.

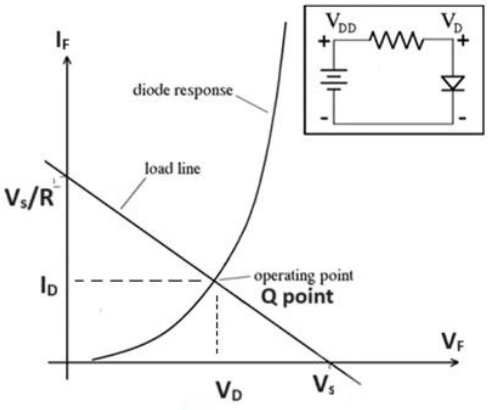


Figure 5: *Calculation of Q point in graph*

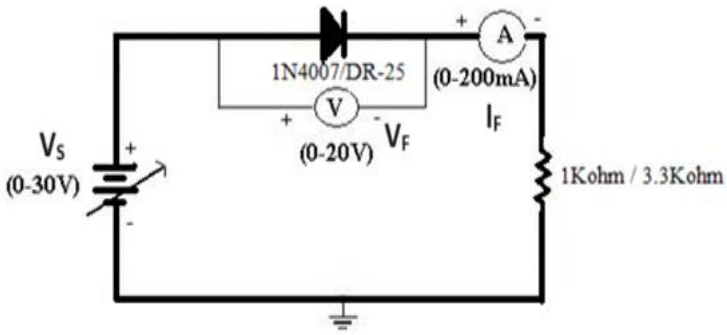


Fig. 6: Circuit diagram of Forward Bias

WORKSHEET FOR STUDENT

Observation Table:

Sr. No.	V_s (V)	Diode Voltage (V_F)	Diode Current (I_F)
1.	0		
2.	0.1		
3.	0.2		
4.	0.3		
5.	0.4		
6.	0.5		
7.	0.6		
8.	0.7		
9.	0.8		
10.	0.9		
11	1		
12	2		
13	3		
14	4		
15	5		

Calculations from Graph:

1. Cut in voltage ($V\gamma$) =

2. Static forward Resistance $R_{DC} = V_D / I_D$ Ω (at quotient point Q after diode gets on, where V/I is almost constant) as shown in figure 5 =

3. Dynamic Forward Resistance w. r. t. point Q, r_{ac} = $\Delta V / \Delta I$ Ω =

Learning Outcomes (expected):

1. Leant to forward bias a diode
2. Know the type of diode; Si or Ge diode?
3. Identify sources of error
4. The forward resistance of the diode decreases with an increase in the forward biasing voltage.

Learning Outcomes (what I have learnt):

1. How will you identify, whether practical diode is made up of Si or Ge using graph and multimeter?

Ans:

2. Why to bias a diode?

Ans:

3. Why forward resistance of the diode decreases with an increase in the forward biasing voltage?

Ans:

4. Draw Breadboard Connection Diagram for Figure 1?

Ans:

EXPERIMENT No.4

Aim: Understanding the truth table of Logic Gates and implement these gates using Universal gates.

Learning Objectives: 1. To verify the functionality of Logic Gates

2. To implement Basic Logic gates using Universal gates and verify their function.

Instruments/Components required: IC-7404,7408,7432, 7400,7402, 7486, Digital Trainer module,

Theory and verification:

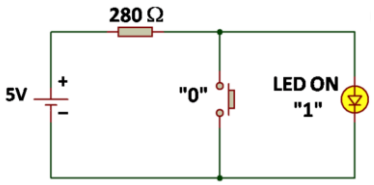
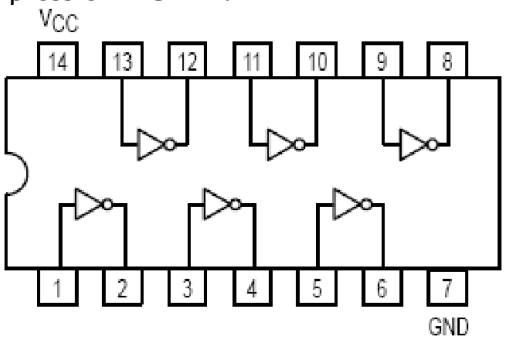


Figure1: NOT gate using a SWITCH

1. **NOT GATE 7404**

The NOT gate, also known as **an inverter**, produces the complement of its input. If **the input** is high, the output is low, and vice versa. It can be represented by the Boolean expression **NOT A.**



Input	Output
0	1(LED GLOW)
1	0 (LED OFF)

Figure 2: IC diagram of 7404 and Truth Table

Table 1: Observation table for NOT gate (7404)

Input	Outputs taken at					
	PIN2(Y1)	PIN4(Y2)	PIN6(Y3)	PIN8(Y4)	PIN10(Y5)	PIN12(Y6)
0						
1						

2. **AND GATE 7408**

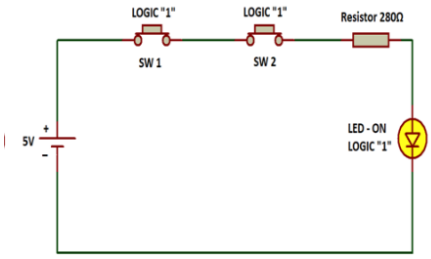
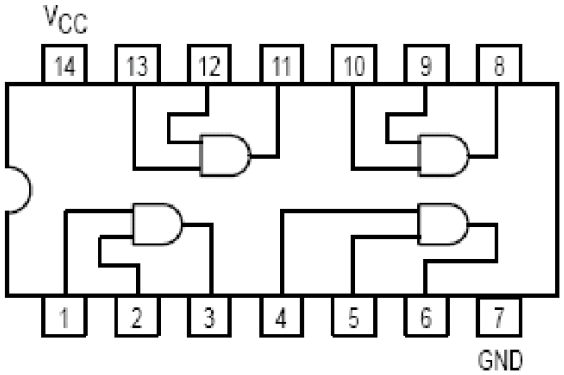


Figure 3: AND Gate using switches

The AND gate produces a high output only when all of its inputs are high. It can be represented by **the Boolean expression** A AND B, where A and B are **the input**s.



Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4: IC diagram of 7408 and Truth Table

Table 2: Observation table for AND gate (7408)

Input A	Input B	PIN3, Y1	PIN6, Y2	PIN8, Y3	PIN11, Y4
0	0				
0	1				
1	0				
1	1				

3. **OR GATE 7432**

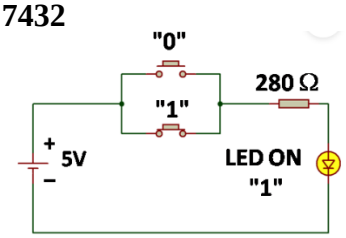
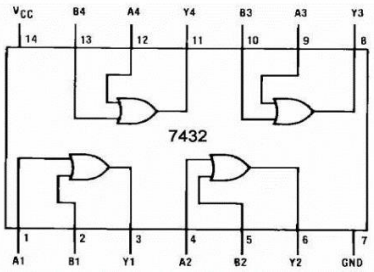


Figure 5: OR gate using a SWITCH

The OR gate produces a high output if any of its inputs are high. It can be represented by **the Boolean expression A** OR B.



Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure 6: IC diagram of 7432 and Truth Table

Table 3: Observation table for OR gate (7432)

Input A	Input B	PIN3, Y1	PIN6, Y2	PIN8, Y3	PIN11, Y4
0	0				
0	1				
1	0				
1	1				

4. **NOR Gate 7402**

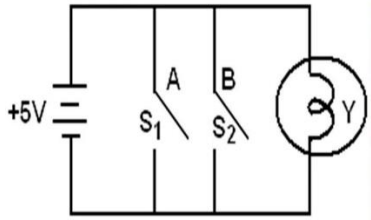
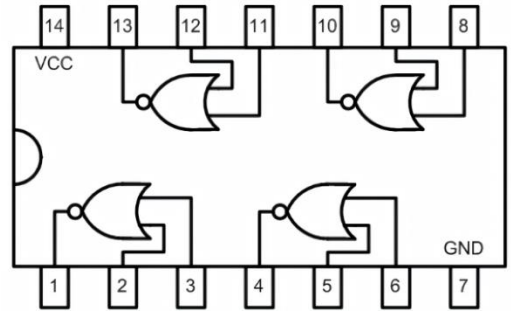


Figure 7: NOR gate using a SWITCH

NOR gate: **The NOR gate** is a combination of an OR gate followed by a **NOT gate**. It produces the complement of **the OR gate output**. It can be represented by the Boolean expression NOT **(A OR B**).



Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Figure 8: IC diagram of 7402 and Truth Table

Table 4: Observation table for NOR gate (7402)

Input A	**Input B**	**PIN1, Y1**	**PIN4, Y2**	**PIN10, Y3**	**PIN13, Y4**
0	0				
0	1				
1	0				
1	1				

5. **NAND Gate 7400**

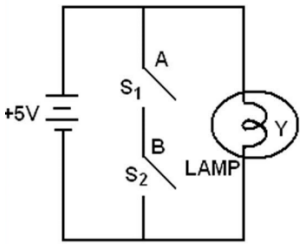
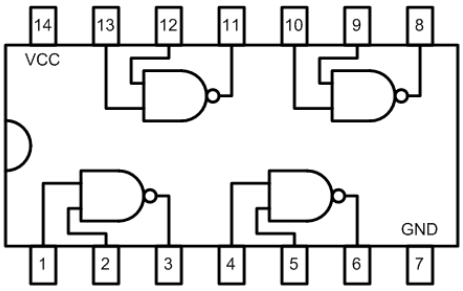


Figure 9: NAND gate using a SWITCH

The N**AND gate** is a combination of an **AND gate** followed by a **NOT gate**. It produces the complement of the **AND gate** output. It can be represented by the Boolean expression NOT (A AND B).



Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 10: IC diagram of 7400 and Truth Table

Table 5: Observation table for NAND gate (7400)

Input A	**Input B**	**PIN3, Y1**	**PIN6, Y2**	**PIN8, Y3**	**PIN11, Y4**
0	0				
0	1				
1	0				
1	1				

6. **XOR Gate 7486**

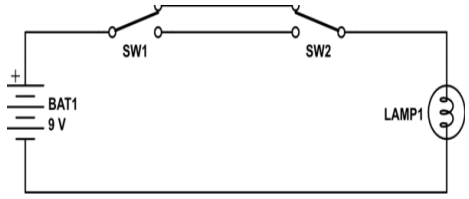
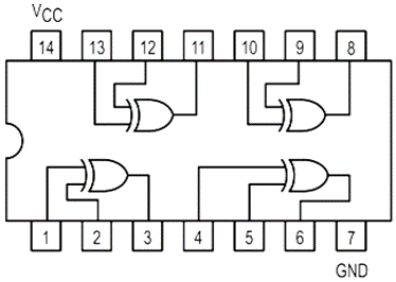


Figure 11: XOR gate using a SWITCH

The XOR gate, also known as **an exclusive OR gate**, produces a high output if the number of high inputs is odd. It can be represented by **the Boolean expression A xor B.**



Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Figure 12: IC diagram of 7486 and Truth Table

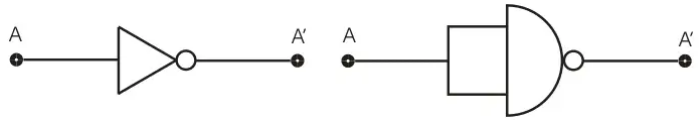
Table 6: Observation table for XOR gate (7486)

Input A	**Input B**	**PIN3, Y1**	**PIN6, Y2**	**PIN8, Y3**	**PIN11, Y4**
0	0				
0	1				
1	0				
1	1				

7. **Implementation using Universal gates**

7.1 Using NAND Gate:

NAND Gate as NOT Gate:



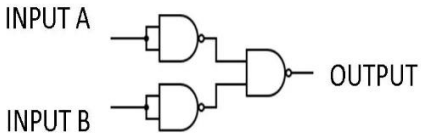
Input	Output
0	1
1	0

Figure 13: NOT gate using NAND Gate and Truth table

Table 7: Observation table for NOT gate using NAND Gate

Input	Outputs taken at			
	PIN3, Y1	PIN6, Y2	PIN8, Y3	PIN11, Y4
0				
1				

NAND Gate as OR Gate:



Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure 14: OR gate using NAND Gate and Truth table

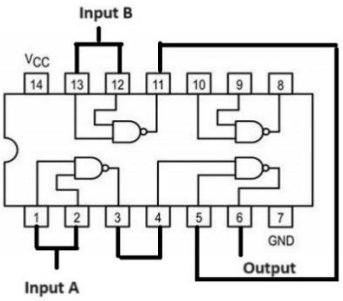
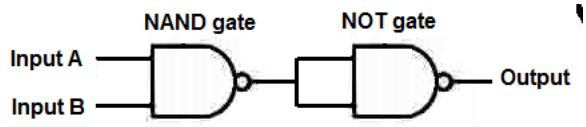


Figure 14.1: IC Diagram of OR gate using NAND Gate

Table 8: Observation table for OR Gate using NAND Universal gate

Input-A	Input-B	Output taken at PIN6, Y
0	0	
0	1	
1	0	
1	1	

NAND Gate as AND Gate:



Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

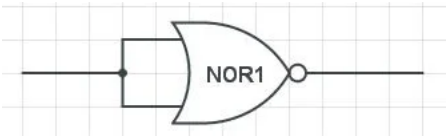
Figure 15: AND gate using NAND Gate and Truth table

Table 9: Observation table for AND Gate using NAND Universal gate

Input-A	Input-B	Output taken at PIN6, Y1
0	0	
0	1	
1	0	
1	1	

7.2 Using NOR Gate:

NOR Gate as NOT Gate:



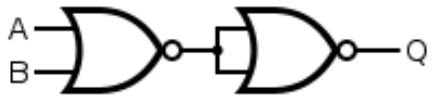
Input	Output
0	1
1	0

Figure 16: NOT gate using NOR Gate and Truth table

Table 10: Observation table for NOT gate using NOR Gate

Input	Outputs taken at			
	PIN1, Y1	PIN4, Y2	PIN10, Y3	PIN13, Y4
0				
1				

NOR Gate as OR Gate:



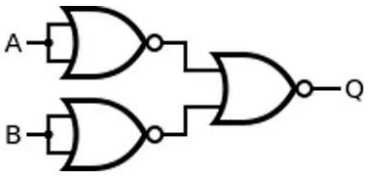
Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure 17: OR gate using NOR Gate and Truth table

Table 11: Observation table for OR Gate using NOR Universal gate

Input-A	Input-B	Output taken at PIN4, Y1
0	0	
0	1	
1	0	
1	1	

NOR Gate as AND Gate:



Input1	Input2	Output
0	0	0
0	1	0
1	0	0
1	1	1

Figure18:AND gate using NOR Gate and Truth table

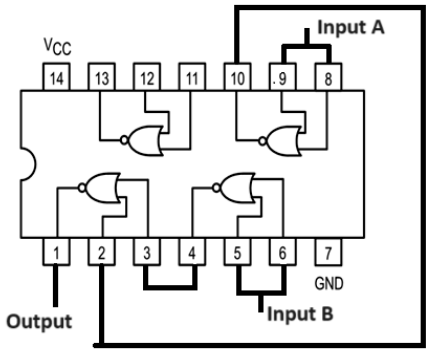


Figure18.1: IC Diagram of AND gate using NOR Gate and Truth table

Table 12: Observation table for AND Gate using NOR Universal gate

Input-1	Input-2	Output taken at PIN1, Y
0	0	
0	1	
1	0	
1	1	

Procedure:

1. Place the IC on the breadboard of digital trainer module as indicated in Figure 1.
2. **Power on the IC**: Identify VCC and GND terminals of the trainer module and connect them to VCC and GND pins of the IC.
3. **Input Sources**: Identify toggle switches on the trainer module and connect them as inputs to the IC.
4. **Output LED**: Identify output LEDs on the trainer module. Connect output pins of the IC to those LEDs.
5. **Verify truth Table**: Apply various combinations of inputs according to the truth table and observe behavior of the logic gates of the IC.

6. Disconnect the inputs and outputs of the IC and replace this IC with a new one and go to step 1.
7. Got to step 1, till all ICs are tested/verified.
8. Now implement NOT, OR, AND using NOR, NAND respectively and verify the functionality of NOT, OR, AND Gates.

Precautions:

1. All the connections should be perfectly tight.
2. Always connect ammeter in series and voltmeter in parallel.
3. Use safety guards while working on live parts.
4. Don't touch the bare conductor when supply is ON.
5. Supply should not be switched ON until and unless the connections are checked by the Faculty/Lab Instructor.
6. Use good shape wires for connections.

Learning Outcome (expected):

1. Understanding the breadboard and its usage for Digital IC connections.
2. Able to understand logic gates and universal gates.
3. Understand pin diagrams of Logic Gate IC's.
4. Able to implement AND, OR, NOT, XOR gates using Universal gates.

Learning Outcome (what I have learnt):

1. How to check whether all gates of IC7400 are working or not? Explain?
   Ans:

2. What is the difference between Logical operations and arithmetic operations?
   Ans:

3. Draw the IC Connection Diagram for Figure 15, 17:
   Ans:

Practical No: 05

Aim: Understanding the combinational logic by implementing the Boolean function using a multiplexer.

Learning Objective: 1. To implement Full Adder (FA) and Full Subtractor (FS) using 4:1 MUX.
2. To verify the working of FA and FS using MUX.
3. To verify the functioning of IC-74153

Instruments/Components: 74153 IC, 7404 IC, Digital Trainer module, connecting probes

Theory: Multiplexer (MUX) is a device that connects one of the input lines to the output line depending upon control signal as shown in **Figure 1**. Same is explained through a control switch and internal circuit of 4:1 MUX.

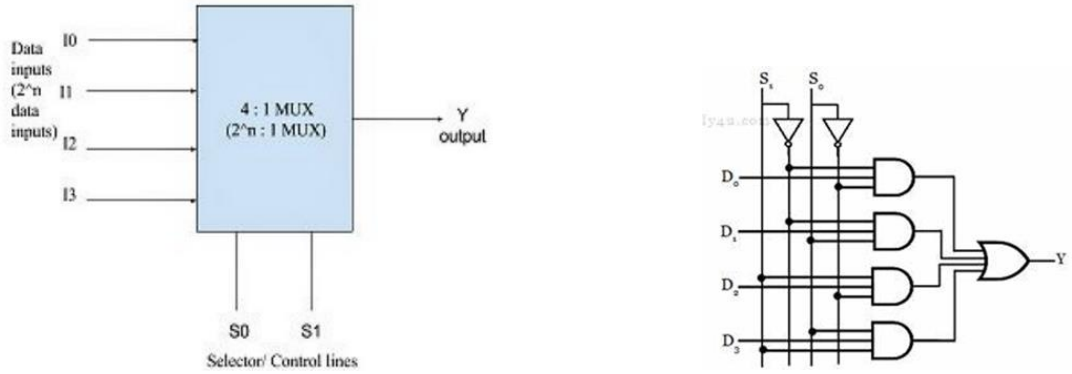


Figure 1: Block diagram of 4:1Mux, 4:1 Mux implementation using Select lines, Internal circuit of 4:1 MUX

There are four input lines, I0, I1, I2 and I3, which are to be multiplexed on a single line output line (Y). The four input lines are also known as the Data Inputs. Since there are four inputs, there is need of two additional inputs to the multiplexer, known as the Select Inputs. The purpose of select inputs is to select, which of the input line can be connected to the output line. Call these select lines S1(A) (MSB) and S0(B). The pin diagram of IC74153, which is dual 4:1 Multiplexer IC is shown below in **Figure 2**.

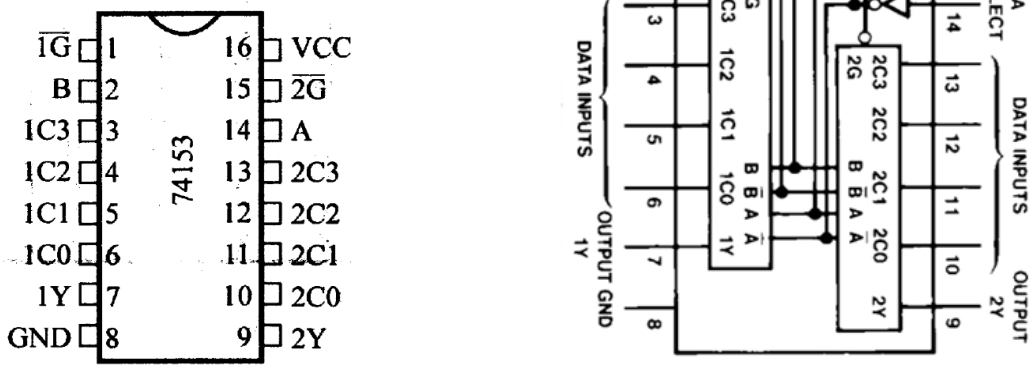


Figure 2: Pin diagram of IC 74153 and internal connection diagram

Implementation of a Full Adder using 4:1 mux:

The full adder has three inputs and 2 outputs i.e. Sum and Carry. In order to realize full adder 2 multiplexers are required, one for implementation of Sum and another of realization of Carry. The Sum (S_n) and Carry (C_n) are expressed following Boolean functions:

Decimal value	A	B	C_{n-1}	Carry (Cn)	Sum (Sn)
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

$Sum(A, B, C_{in}) = \sum m(1,2,4,7)$---------1

$Carry(A, B, C_{in}) = \sum m(3,5,6,7)$-------2

Select Lines: *A=> pin 14, B=>Pin 2.* $\boldsymbol{C_{n-1}}$=> to input data lines,

The value of C_{n-1} connected to input data line will be calculated using Mux Map for Sum and Carry

Table "Mux Map for SUM" and "Mux Map for Carry" helps to identify input data line connections using equations 1 and 2, wherein bracketed values in the table below indicate values of equation 1 and 2 respectively.

Mux map for Sum (Using Tabular Approach)

Inputs	**I0**	**I1**	**I2**	**I3**
$\boldsymbol{\overline{C}_{n-1}}$	0	**(2)**	**(4)**	**6**
$\boldsymbol{C_{n-1}}$	**(1)**	3	5	**(7)**
	$\boldsymbol{C_{n-1}}$	$\boldsymbol{\overline{C}_{n-1}}$	$\boldsymbol{\overline{C}_{n-1}}$	$\boldsymbol{C_{n-1}}$

Mux map for Carry (Using Tabular Approach)

Inputs	**I0**	**I1**	**I2**	**I3**
$\boldsymbol{\overline{C}_{n-1}}$	0	2	4	**(6)**
$\boldsymbol{C_{n-1}}$	1	**(3)**	**(5)**	**(7)**
	0→ GND	$\boldsymbol{C_{n-1}}$	$\boldsymbol{C_{n-1}}$	**1→ Vcc**

MUX map for SUM is implemented in A part of MUX IC & MUX map for Carry is implemented in B part of MUX IC, A & B are select lines as indicated in **Figure** 3:

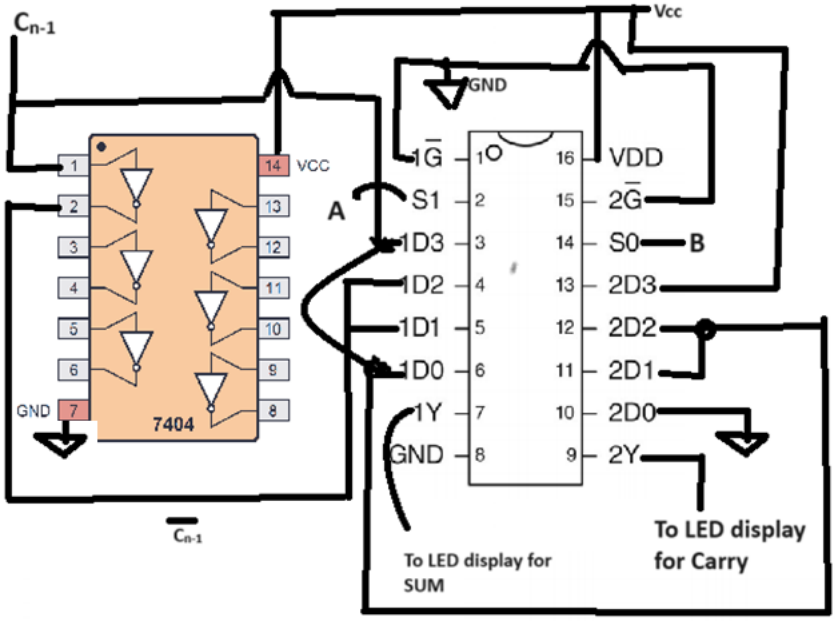


Figure 3: Connection diagram of Full Adder using 74153

Implementation of a Full Subtractor using 4:1 mux:

The full subtractor has three inputs and 2 outputs i.e. Difference and Borrow. In order to realize full subtractor, 2 multiplexers are required, one for implementation of Difference and another of realization of Borrow. The Difference (D_n) and Borrow (B_n) are expressed following Boolean functions:

Decimal value	A	B	B_{n-1}	Borrow (Bo)	Difference (Dn)
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

$Difference\ (A, B, B_{n-1}) = \sum m(1,2,4,7)$--------3

$Borrow(A, B, B_{n-1}) = \sum m(1,2,3,7)$----------4

Select Lines: A=> Pin 14, B=>Pin 2. $\boldsymbol{B_{n-1}}$=> to input data lines,

The value of B_{n-1} connected to input data line will be calculated using Mux Map for Difference and Borrow

Table "Mux Map for Difference" and "Mux Map for Borrow" helps to identify input data line connections using equations 1 and 2, wherein bracketed values in the table below indicate values of equation 3 and 4 respectively.

Mux map for Difference(Using Tabular Approach)

Inputs	I0	I1	I2	I3
$\boldsymbol{\bar{B}_{n-1}}$	0	**(2)**	**(4)**	6
$\boldsymbol{B_{n-1}}$	**(1)**	3	5	**(7)**

	B_{n-1}	$\overline{B}_{n-1}$	$\overline{B}_{n-1}$	B_{n-1}

MUX map for Borrow (Using Tabular Approach)

Inputs	I0	I1	I2	I3
$\overline{B}_{n-1}$	0	(2)	4	6
B_{n-1}	(1)	(3)	5	(7)
	B_{n-1}	1→ Vcc	0→ GND	B_{n-1}

MUX map for Difference is implemented in A part of MUX IC & MUX map for Borrow is implemented in B part of MUX IC, A & B are select lines as indicated in **Figure** 4:

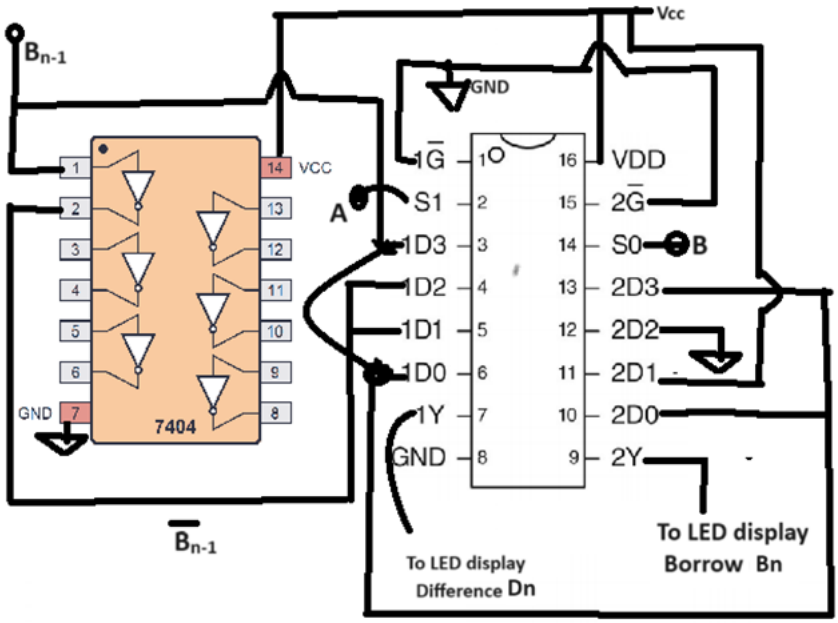


Figure 4: Connection diagram of Full Subtractor using 74153

Procedure:

1. **Power ON the IC**: Connect Vcc *to* Pin [16] and GND to Pin [8].
2. **Enable the IC-74153**: Initialize MUX 'A' and MUX 'B' by connecting *EA(pin1), EB(pin 15)* to GND.
3. **Select Lines:** The inputs 'A' and 'B' are applied to Pin [2] and input Pin [14] as select lines, respectively.
4. **Verification of IC-74153**: Connect pin 2, 14 to GND, Connect Pin 6, 10 to Logic High. Observe, High at Pin 7 and 9 indicates that IC is functional.
5. **Data line inputs for FA**: Make use of 7404 and create input connections to MUX-A and MUX-B part of IC-74153 as shown in Figure 3. Connect toggle switches (input switches) to A, B, Cin.
6. In full adder the outputs S_n and C_n are taken from pins [7] and [9], respectively. Now, complete the observation Table.
7. **Data line inputs for FS**: Make use of 7404 and create input connections to

MUX-A and MUX-B part of IC-74153 as shown in Figure 4. Connect toggle switches (input switches) to A, B, B_{n-1}.

8. In full subtractor the outputs D_n and B_n are taken from pins [7] and [9], respectively, Now, complete the observation Table.

Precautions:

1. Do press the IC on breadboard until pins are aligned with pours.
2. Do not make loose connections.
3. There should not any short circuit to avoid the heating of IC.

Observation Table:

Full Adder

Inputs			**Outputs**	
A	B	C_{n-1}	S_n	C_n
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Full Subtractor

Inputs			**Outputs**	
A	B	B_{n-1}	D_n	B_n
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Draw IC Connection Diagram for Figure 3 and Figure 4:

Learning Outcomes (Expected):

1. Could differentiate between adder is HA and FA?
2. Able to connect digital ICs and make connections as per circuit diagram of Fig 3 and 4.
3. Understand provision of input carry and Borrow in FA, FS respectively, in multibit addition or subtraction.
4. Verify the functioning of IC-74153

Learning Outcomes (What I have learnt):

1. How to check if IC-74153 is functional or not?
   Ans:

2. Write steps to create mux map for Full adder?
   Ans:

Viva Questions:

1. How many select lines are there in 4:1 mux?
2. How can you implement a function with multiplexer?
3. IC 74153 is which type of the IC?
4. In 74153 what is the purpose of Strobe pin?
5. In 74153 how many multiplexers are present?
6. Which pin is active low pin in 74153 IC.

EXPERIMENT No. 6

Aim: Virtual Integration of IR sensor using Arduino.

Learning Objective (s):

1. To write a program code on Arduino for integration of IR sensor
2. To verify the working of the experiment using a circuit simulator.

Instruments/Components Required:

S.No.	Items	Quantity
1	Arduino Uno	1
2	LED-GREEN (or any color)	1
3	Analog Primitive Resistor (220-ohm)	1
4	Virtual Terminal	1
5	Logic Toggle	1
6	IR Obstacle Sensor	1
7	Battery (Cell)	1

Theory:

An object can be detected with an infrared system consisting of an infrared transmitter and a receiver. More in detail an IR transmitter, also known as IR LED, sends an infrared signal with a certain frequency compatible with an IR receiver which has the task to detect it. There are different kind of IR sensors for different type of application. In this practical, IR technology is used as a proximity sensor to detect a near object.

IR sensor principle of operation with/without object: The IR transmitter sends an infrared signal that, in case of a reflecting surface (e.g., white color), bounces off in some directions including that of the IR receiver that captures the signal detecting the object. When the surface is absorbent (e.g., black color) the IR signal isn't reflected and the object cannot be detected by the sensor. Same result would occur with object absent.

IR transmitter and IR receiver:

The IR transmitter is a particular LED that emits radiation in the frequency range of infrared, invisible to the naked eye as shown in **Figure 1**. An infrared LED just works as a simple LED with a voltage of 3V DC and a current consumption of about 20mA. The IR receiver, such as a photodiode or a phototransistor, is capable of detect infrared radiation emitted from the IR

transmitter. Aesthetically it is similar to a LED but the external capsule can be wrapped by a dark color film.

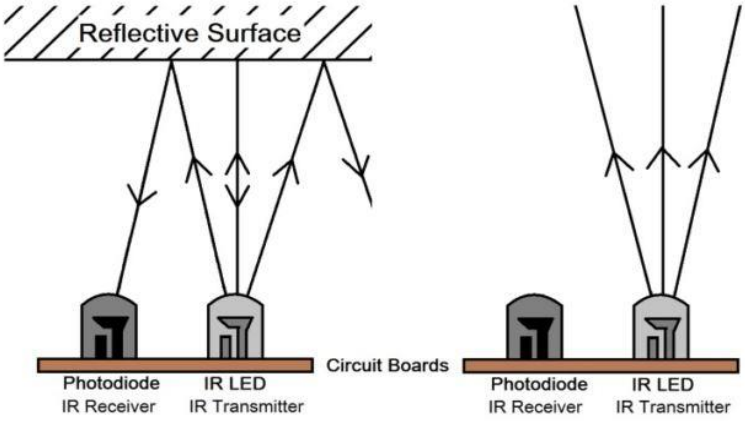


Figure 1: working of IR transmitter Receive module

Circuit Diagram for IR sensor connected at pin no 2 and output led connected at pin no 13:

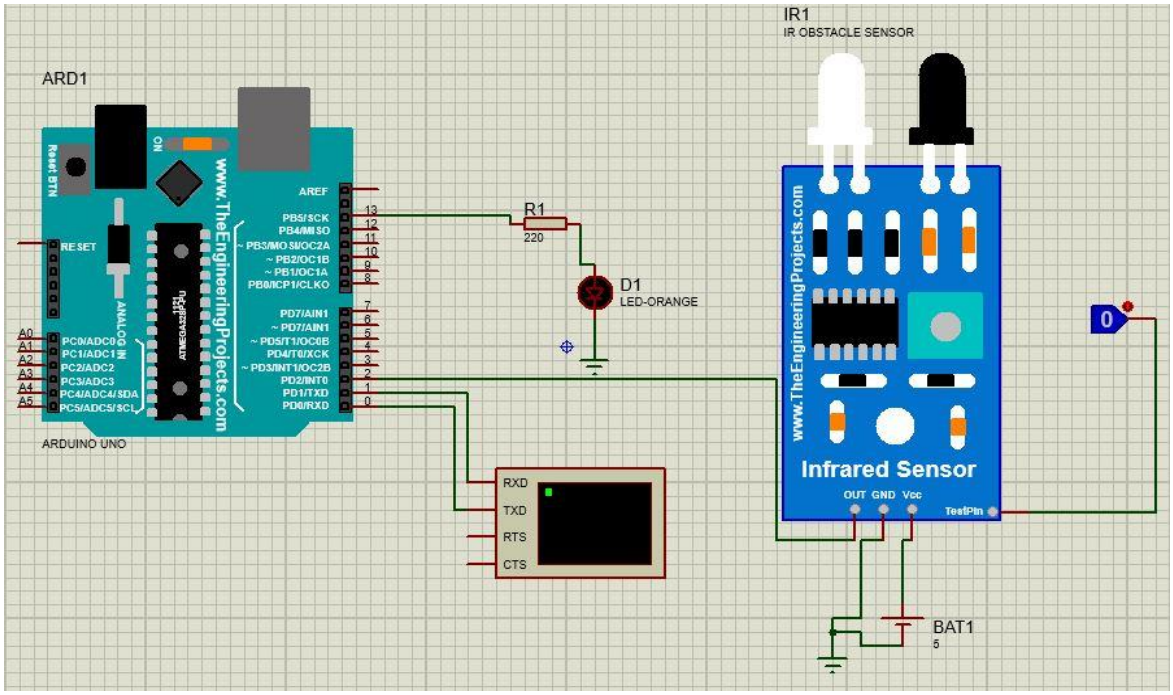


Figure 2: Connection Diagram of the Practical

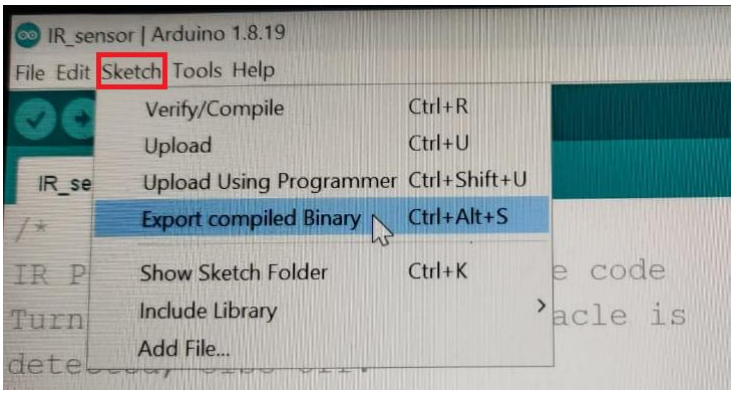
Program File for IR sensor connected at pin no 2 and output led connected at pin no 13:

```
void setup() {
  pinMode(13, OUTPUT);
  pinMode(2, INPUT);
  //Serial.begin(9600);
```

```
}
void loop() {
  int SensorValue = digitalRead(2);
 //Serial.print("SensorPin Value: ");
  //Serial.println(SensorValue);
  delay(100);
   if (SensorValue==LOW){ // LOW MEANS Object Detected
    digitalWrite(13, HIGH);
  }
  else
  {
    digitalWrite(13, LOW);
  }
}
```

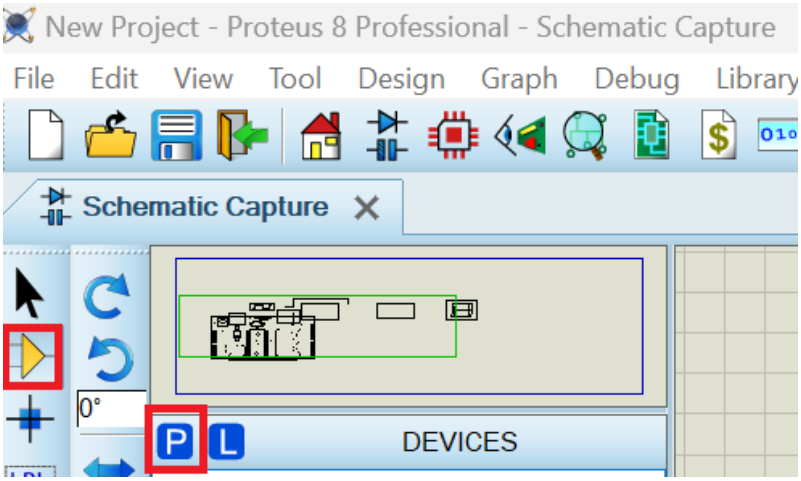
Procedure:

1. At first, write the program (code) as given above on Arduino Uno 1.8.19. Verify the code and save it. Secondly, Go to Sketch → export compiled binary, and click on it to get IR_sensor.ino.standard.hex, and IR_sensor.ino.with_bootloader.standard.hex in your folder where Arduino program is saved.

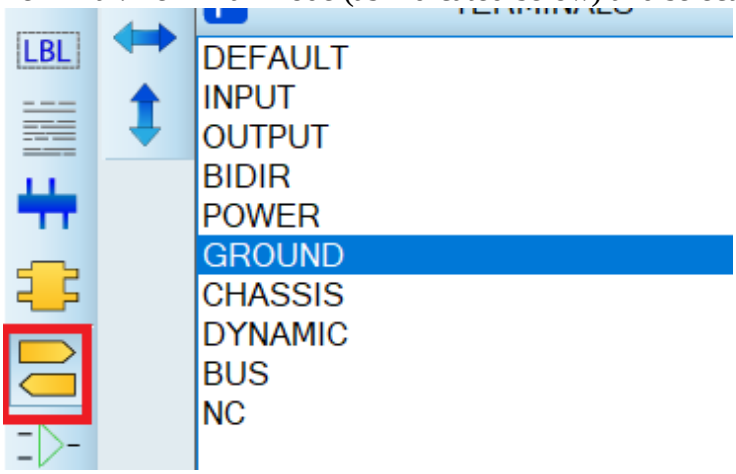


2. For circuit simulation, Open simulation window and follow the path: File → Project Name→ Create a schematic from Templates (Select Default) → Do not create a PCB layout → No Firmware Project→ Schematic→ Press "finish".
3. Double click on Arduino board (at simulation window) and place compiled binary files IR_sensor.ino.standard.hex, and IR_sensor.ino.with_bootloader.standard.hex file at the location of circuit simulator file.
4. Ensure that following library file are available at a place where circuit simulator file is saved: "InfraredSensorsTEP.HEX"
5. If files not available as per step 4, then follow path follow path; C::://→ Program files (*86) → lab Centre electronics→ professional→ Data→ library → Copy "InfraredSensorsTEP .HEX" and past at location of circuit simulator file.

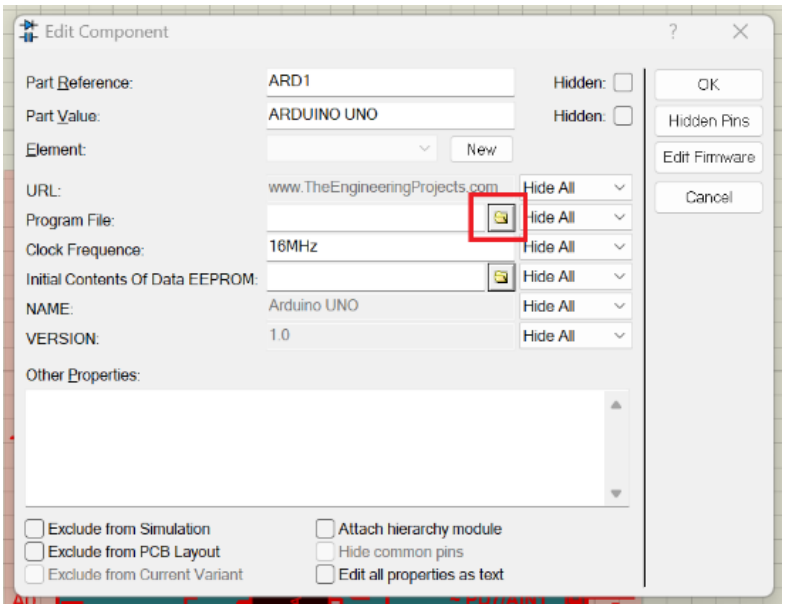
6. Click on component mode (highlighted in red above) → **P** icon (highlighted in red) → search component names as mentioned in "apparatus required" and place components as per given above diagram with double click on the simulation window.



6.1 Get Arduino Board: Component mode→ P→ Search "Arduino UNO R3 V1.0"
6.2 Get Infrared Sensor: Component mode→ P→ Search "IR Obstacle Sensor"
6.3 Get Toggle Switch: Component mode→ P→ Search "LOGICTOGGLE"
6.4 Get Battery: Component mode→ P→ Search "CELL"→ Battery (single cell). Now edit the value of battery (right click on the icon) and make it 5V.
6.5 Get Resistance: Component mode→ P→ Search "RESISTORS"→ 1K---10Watt. Now edit the value of resistance (right click on the icon) and make it 220 ohm.
6.6 Get LED: Component mode→ P→ Search "LED"→ LED-GREEN
6.7 Get Virtual Terminal: Right click on the circuit creation space→ Place→ Virtual Instrument→ Virtual Terminal.
6.8 Get Ground Terminal: Terminal Mode (as indicated below) and select Ground



7. Now Double click on Arduino board -→ open the folder highlighted in RED→ select the IR_sensor.ino.standard.hex from circuit simulator file folder → Press "OK".



8. Repeat the same exercise IR sensor, Double click on IR Sensor → Open program file folder → select "InfraredSensorsTEP.HEX" from circuit simulator file folder→ press "OK"
9. Once the circuit diagram is completed as indicated in **Figure 2**, press the play button available at bottom left corner of simulation window as shown below (highlighted in red).

Verification of circuit connections

The sensor input is at pin 2 and the output is taken from pin no 13 as per given code. The "glowing LED" will detect the presence of object in the IR radiation path. On changing logic toggle to 0 & 1, the virtual terminal displays the presence or absence of object indicating communication through serial port. The virtual terminal is used to display the content of print statements.

Precautions:

1. Carefully write the program to avoid syntax errors.
2. In the circuit simulator, bin files must be called before running the circuit.

Observation Table:

Proteus circuit		Arduino Program code		Observation
Sensor I/P	Arduino O/P	Sensor I/P	Arduino O/P	
2	13	2	12	
2	13	2	13	
2	13	3	13	

Viva Questions:

1. The function which repeatedly executes in the main program is?
2. How many buttons exist for reset and erase in Arduino Due?
3. What is the Importance Virtual terminal and logic toggle switch?

Learning outcomes (Expected)

1. Write a program on Arduino and simulate it
2. Use the Arduino binary file in circuit simulator
3. Learn to use TEP.HEX file in IR sensor module and its significance.
4. Connect other sensors and repeat the practical (home exercise)

Learning outcomes (what I have learnt)

1. What is Void setup for?
   Ans:

2. What is void loop for?
   Ans:

3. Where constants can be declared in an Arduino program?
   Ans:

4. How to get binary file of the Arduino program and where to use it?
   Ans:

Experiment No.- 7

AIM: Understand JK Flip-Flop and implement T-Flip Flop using NAND circuit of JK Flip Flop.

Learning Objectives:

1. To implement JK flip flop using NAND gates and verify of its functionality.
2. To implement T flip flop using NAND gates and verify its functionality.

Components & Instruments required: IC 7410, 7400, Power supply and LEDs.

Theory:

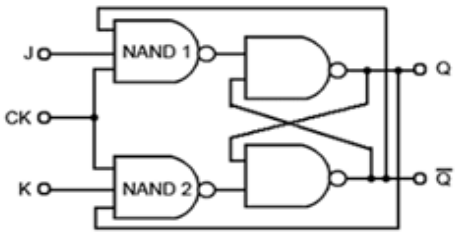
The logic circuits whose outputs at any instant of time depend not only on the present input but also on the past outputs are called sequential circuits. The simplest kind of sequential circuit which is capable of storing one bit of information is called latch. The operation of basic latch can be modified, by providing an additional control input that determines, when the state of the circuit is to be changed. The latch with additional control input is called the Flip-Flop. The additional control input is either the clock or enable input. Flip flop is formed using logic gates. Flip flop are fundamental building blocks in the memory of electronic devices. Each flip flop can store one bit of data. Based on their operations, flip flops are basically 4 types. They are

1. S-R flip flop
2. D flip flop
3. J-K flip flop
4. T flip flop

J-K flip-flop: JK flip flop operates on sequential logic principle, where the output is dependent not only on the current inputs but also on the previous state. There are two inputs in JK Flip Flop Set and Reset denoted by J and K. It also has two outputs: Output and complement of Output denoted by Q and $\overline{Q}$. The internal circuitry of a JK Flip Flop consists of a combination of logic gates, usually NAND gates as shown in **Figure 1**.

JK flip flop comprises four possible combinations of inputs:

- **J=0, K=0:** In this state, flip flop retains its preceding state. It neither sets nor resets itself, making it stable.
- **J=0, K=1:** This input combination forces flip flop to reset, resulting in Q=0 and $\overline{Q}$=1. It is often referred to as the "reset" state.
- **J=1, K=0:** Here, flip flop resides in the set mode, causing Q=1 and $\overline{Q}$=0. It is known as the "set" state.
- **J=1, K=1:** This combination toggles flip flop. If the previous state is Q=0, it switches to Q=1 and vice versa. This makes it valuable for frequency division and data storage applications.



Inputs			Output Q_{n+1}	Operation
CLK	J	K		
0	X	X	Q_n	No change
↓	0	0	Q_n	No change
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	Q_n'	Toggles

Figure 1: J-K Flip flop using NAND gate, Truth Table (here Q_n=Q)

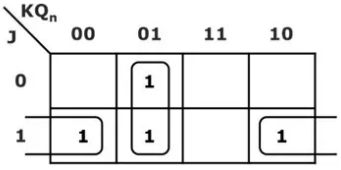
Characteristic Table:

J	K	Q_n	Q_{n+1}	State
0	0	0	0	Q_n (Hold)
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggel
1	1	1	0	

Excitation table:

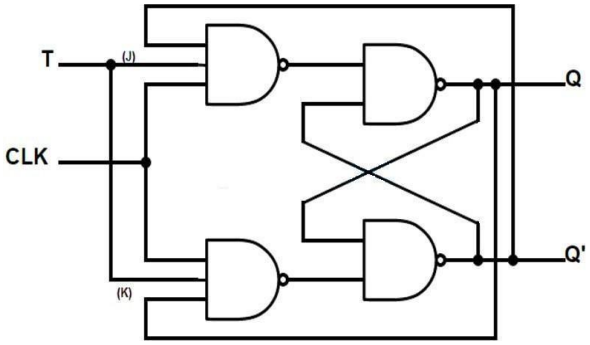
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Characteristic Equation:



$$\Rightarrow Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

T flip-flop: T flip flop or to be precise is known as Toggle Flip Flop because it can able to toggle its output depending upon on the input. T, here stands for Toggle. Toggle basically indicates that the bit will be flipped i.e., either from 1 to 0 or from 0 to 1. The toggle or T-type flip-flop gets its name from the fact that its two outputs Q and Q invert from their previous state as it toggles back and forth every time it is triggered (T = 1). That is, the Q and Q outputs change to a "1" if it was "0", and "0" if it was previously a "1" but only when the "T" input changes HIGH, otherwise they do not change. Same is shown in Figure 2



Clk	T	Q_{n+1}	Operation
0	×	Q_n	Memory
1	0	Q_n	Memory
1	1	Q_n'	Toggle

Figure 2: NAND implementation of T-FF and Truth Table

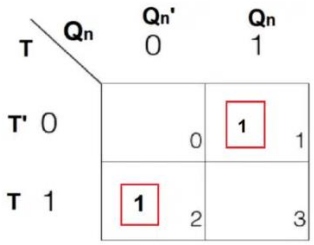
Characteristic Table:

Clk	T	Q_n	Q_{n+1}
0	×	×	×
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

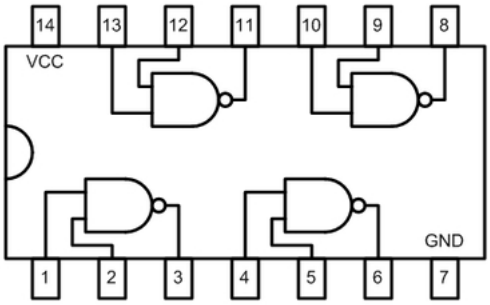
Characteristic equation:



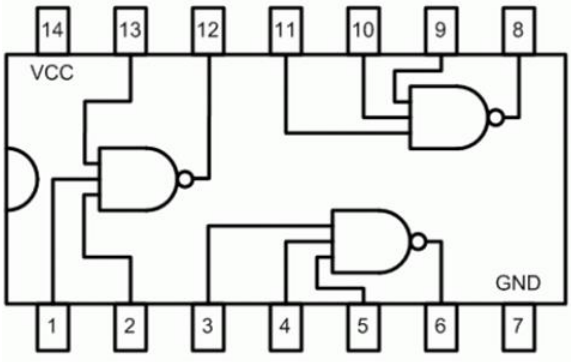
$Q_{n+1} = T\overline{Q_n} + \bar{T}Q_n$ = T xor Q_n

Procedure:

1. Make the connections using IC 7400 and 7410 as per Figure 1



7400 Quad-Two input NAND



7410 Tripple three input NAND

2. **Power on the IC**-7410 and 7400 by connecting V_{CC} at pin 14 and GND at PIN 7.
3. Connect the "Clock 1Hz" button or pulse button as a CLK.
4. Apply the inputs as per characteristic table of JK FF and note the outputs in **Figure 1**, Update the observation table of JK FF.
5. Verify the practical and theoretical values of JK-FF as per entries in observation table of JK FF.
6. Similarly repeat step 4 and 5 for T FF of **Figure 2**.
7. Identify different sources of error in the practical.

IC Diagram of JK-FF using NAND Gates:

IC Diagram of T-FF using NAND Gates

Precautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit. Avoid the heating of IC. Provide proper clock pulse.

Learning Outcomes:

1. Explain the working of flip flops.
2. Test the IC of logic gates 7400, 7410.
3. Verify the effect of previous output and current input on the next state output.

Viva Questions:

1. What is the function of clock pulse?
2. What do you mean by race around condition?
3. How the race around condition can be removed?
4. How to convert JK to T-FF.

Learning Outcomes (expected):

1. Implement JK and T-FF on the breadboard
2. Verify JK and T FF.
3. Identify different sources of error in the practical.

Learning Outcomes (what I have learnt?):

1. How to test functioning of 7400 and 7410?
   Ans:

2. What steps are required to convert JK-FF to T-FF?
   Ans:

Worksheet of the student

Observation Table for J-K Flip Flop

J	K	Q_n	Q_{n+1} (Calculated using Characteristic equation) $J\overline{Q_n} + \overline{K}Q_n =$	$Q_{(n+1)}$ (Observed using LED display of Digital trainer kit)
0	0	0	$0.\overline{0} + \overline{0}.0$=0.1+1.0=0+0 = 0	
0	0	1	$0.\overline{1} + \overline{0}.1$=0.0+1.1=0+1 = 1	
0	1	0	$0.\overline{0} + \overline{0}.0$=0.1+1.0=0+0 = 0	
0	1	1	$0.\overline{1} + \overline{1}.1$=0.0+0.1=0+0 = 0	
1	0	0	$1.\overline{0} + \overline{0}.0$=1.1+1.0=1+0 = 1	
1	0	1	$1.\overline{1} + \overline{0}.1$=1.0+1.1=0+1 = 1	
1	1	0	$1.\overline{0} + \overline{1}.0$=1.1+0.0=1+0 = 1	
1	1	1	$1.\overline{1} + \overline{1}.1$=1.0+0.1=0+0 = 0	

Observation Table for T Flip Flop

T	Q_n	Q_{n+1} (Calculated using Characteristic equation) $T\overline{Q_n} + \overline{T}Q_n$=	$Q_{(n+1)}$ (Observed using LED display of Digital trainer kit)
0	0	$0.\overline{0} + \overline{0}.0$=0.1+1.0=0+0 =0	
0	1	$0.\overline{1} + \overline{0}.1$=0.0+1.1=0+1 =1	
1	0	$1.\overline{0} + \overline{1}.0$=1.1+0.0=1+0 =1	
1	1	$1.\overline{1} + \overline{1}.1$=1.0+0.1=0+0 =0	

Practical No 8

Aim: Implement Decade counter using IC-7490 and seven segment display.

Learning Objective: To use IC-7490 as MOD-2, MOD-5 and MOD-10 counter, and display IC-7490 output value on 7 segment display through decoder circuit.
Instruments/Components required: IC 7490, IC 7447 Decoder, Seven Segment Common Anode Display, Resistance 1Kohm, Digital Trainer module with 1Hz clock terminal.

Theory:
The design of the experiment requires three ICs i.e. 7490, 7447 and seven segment display. The outputs of 7490 acts as input to 7447 (BCD to seven segment decoder). There are 7 output PIN from 7447 which acts as inputs to seven segment display IC as shown in Figure 1.

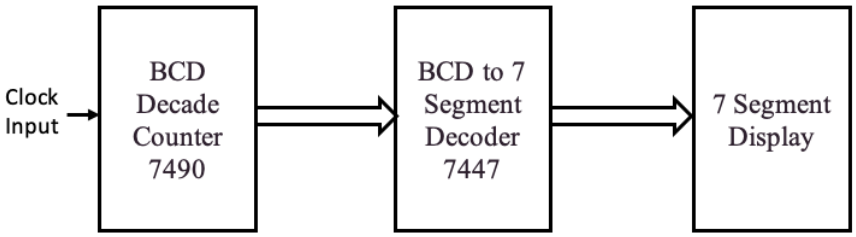


Figure 1: Block Diagram of the Experiment

1. **IC 7490 BCD Decade Counter**: It is a 14 pin IC, which can output the binary numbers from 0000 to 1001. After 1001 it gets resets and again starts counting from zero, as shown in **Figure 3 & 4**. Since, IC 7490 gets reset after counting ten numbers, it is called MOD-10 or Decade Counter. This IC takes 10 clock pulses to generates BCD code corresponding to each clock pulse. The outputs QA, QB, QC and QD are four bits of the BCD code.

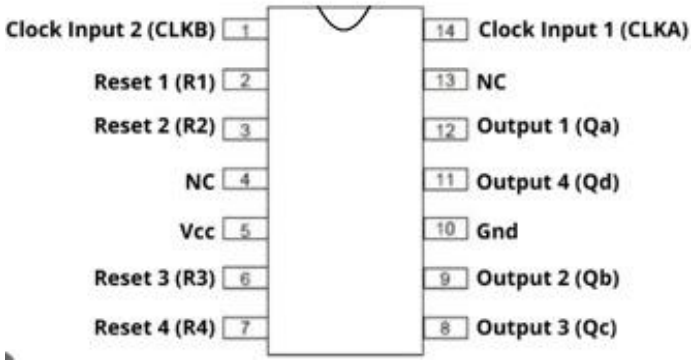


Figure 2: PIN diagram of IC-7490

The IC 7490 consists of MOD-2 and MOD-5 counters.

MoD-2 counter has output QA, Count sequence of MOD-2 counter is 0→1→0 and so on.

MOD-5 counter has output Q_D, Q_C and Q_B (Q_D is MSB and Q_B is LSB). Count sequence of MOD-5 counter is 0→1→2→3→4→0 and so on.

It should be noted that external CLK signal is applied at MOD-2 counter and its output Q_A acts as clock for MOD-5 counter. This is shown in Figure 7. The state diagram for decade counter is as:

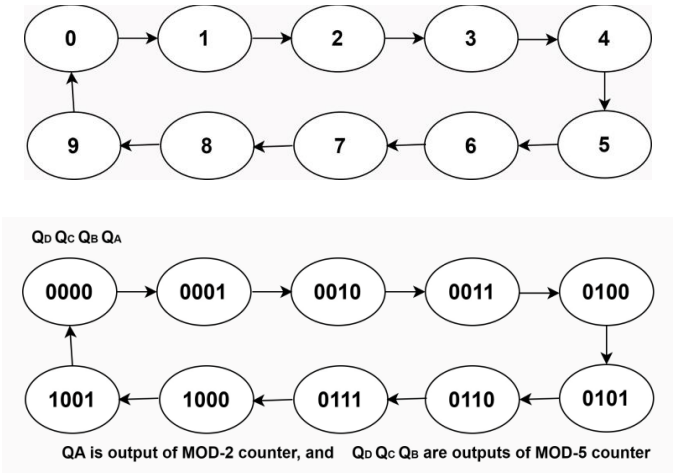


Figure 3: State diagram of MoD-10 Counter

Truth table of Decade Counter IC -7490					
Clock Count	**Output Bit Pattern**				**Output in decimal value**
	QD	Qc	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9

Figure 4: Truth table of Decade Counter

2. **IC 7447 BCD to seven segment decoder/driver IC**: It is a 16 pin IC, which accepts a binary coded decimal as input and converts it into a pattern to drive a seven-segment for displaying digits 0 to 9. BCD is an encoding method in which each digit of a number is represented by its own binary sequence (usually of four bits). It accepts four lines of BCD (8421) input data and generates their complements internally. The outputs correspond to common anode (CA) configuration of seven segment as shown in **Figure 5**.

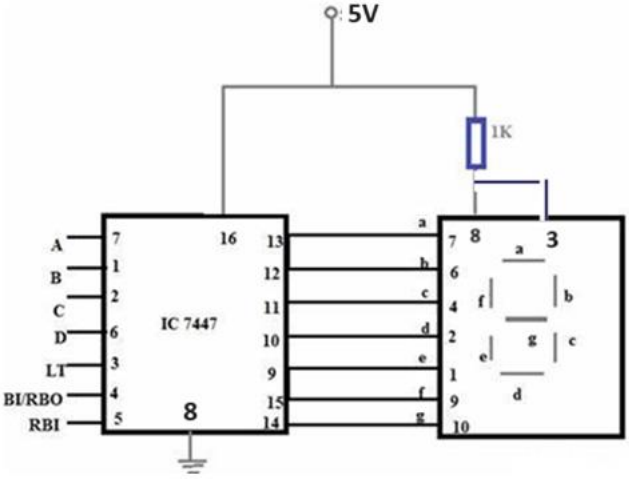
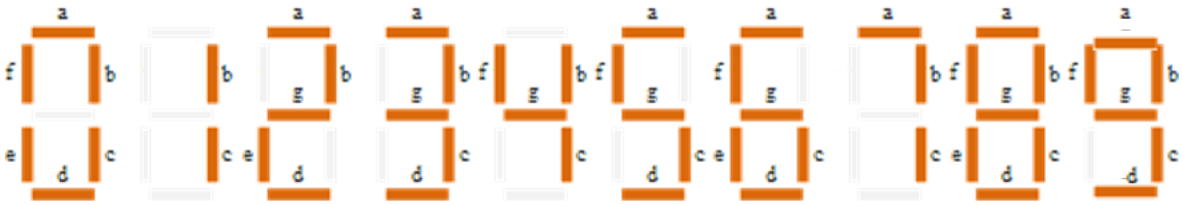


Figure 5: PIN diagram of IC-7447 and 7 segment Common Anode display

Truth table of IC-7447 (for common Anode Seven segment display): (Digits 10 to 15 are not displayed in single digit display)



Digit	Is Digit, output of decade counter?	Input Terminals of IC - 7447				Output Terminals of IC-7447 or inputs of Seven segment display						
		A	B	C	D	a	b	c	d	e	f	g
0	Yes	0	0	0	0	0	0	0	0	0	0	1
1	Yes	0	0	0	1	1	0	0	1	1	1	1
2	Yes	0	0	1	0	0	0	1	0	0	1	0
3	Yes	0	0	1	1	0	0	0	0	1	1	0
4	Yes	0	1	0	0	1	0	0	1	1	0	0
5	Yes	0	1	0	1	0	1	0	0	1	0	0
6	Yes	0	1	1	0	0	1	0	0	0	0	0
7	Yes	0	1	1	1	0	0	0	1	1	1	1
8	Yes	1	0	0	0	0	0	0	0	0	0	0
9	Yes	1	0	0	1	0	0	0	0	1	0	0
10	No	1	0	1	0	x	X	x	x	X	x	x
11	No	1	0	1	1	x	X	x	x	X	x	x
12	No	1	1	0	0	x	X	x	x	X	x	x
13	No	1	1	0	1	x	x	x	x	x	x	x
14	No	1	1	1	0	x	x	x	x	x	x	x
15	No	1	1	1	1	x	x	x	x	x	x	x

3. **Seven Segment Display**: Seven segment displays are 10 pin output display device that provides a way to display information in the form of images or text or decimal numbers, which is an alternative to the more complex dot matrix displays. It is widely used in digital clocks, basic calculators, electronic meters, and other electronic devices that displays numerical information. It consists of seven segments of light-emitting diodes (LEDs), which are assembled like numerical 8. According to the type of application, there are two types of configurations of seven-segment displays: **common anode display and common cathode display** as shown in **Figure 6.**

   In common cathode seven segment displays, all the cathode connections of LED segments are connected together to logic 0 or ground. We use logic 1 through a current limiting resistor to forward bias the individual anode terminals a to g (we may also connect without using a resistance). Whereas all the anode connections of the LED segments are connected together to logic 1 in a common anode seven segment display. We use logic 0 through a current limiting resistor to the cathode of a particular segment a to g (we may also connect without using a resistance).

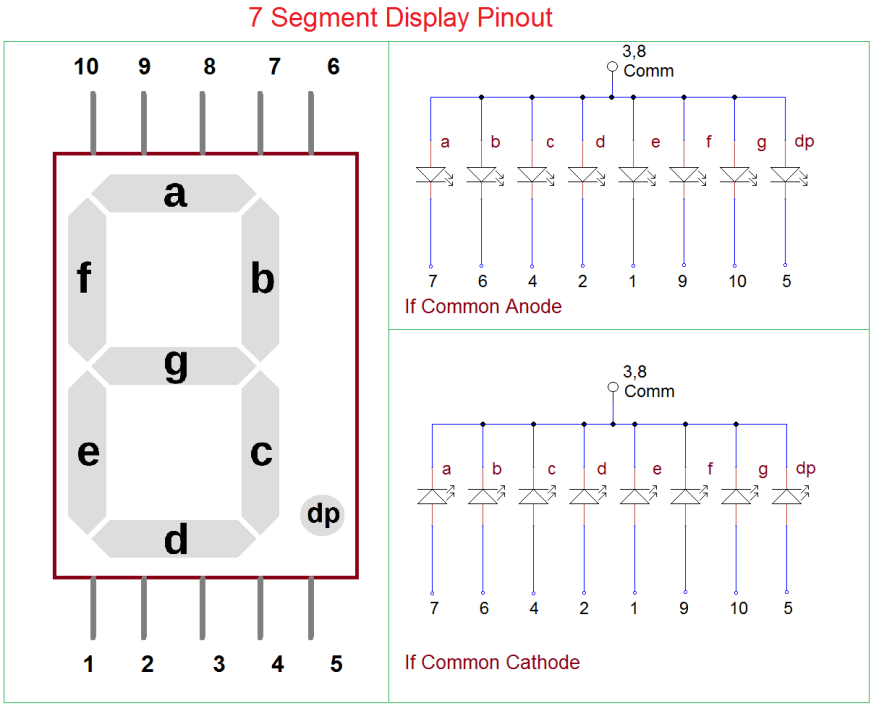


Figure 6: Common Cathode, Common Anode Display

For Common anode seven segment display: LED will glow with input LOW

For Common cathode seven segment display: LED will glow with input HIGH

7 Procedure:

7.1 **Power On the ICs**: **IC-7490**: PIN 5 to Vcc and PIN 10 to GND,
IC-7447: PIN 16 to Vcc and PIN 8 to GND,
7-Segment display: PIN 8 and or 3 to Vcc through a resistance to provide less than 5V to power on display IC (for Common Anode Display).

7.2 **Connection diagram**: - The output of IC-7490 is connected to IC7447 decoder and decoder output to 7-segment display unit. Make the connections as shown in **Figure 7**, as per case-2 of observation table.

7.3 **Case-1 of Observation table**:

7.3.1 Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490.

7.3.2 PIN-12 is not connected to PIN-1 of IC-7490

7.4 **Case-2 of Observation table**:

7.4.1 Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490.

7.4.2 PIN-12 is connected to PIN-1 of IC-7490.

7.5 **Case-3 of Observation table**:

7.5.1 Master CLK of 1Hz taken from Trainer module is not connected at PIN -14 of IC-7490.

7.5.2 PIN-12 is not connected to PIN-1 of IC-7490

7.5.3 Master CLK of 1Hz taken from Trainer module is connected at PIN -1 of IC-7490

WORKSHEET FOR STUDENT

Observation Table

Sr No	Changes in connection diagram of Figure 7	Expected sequence	Observed Sequence
Case: 1	1) Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490 and 2) PIN-12 is not connected to PIN-1 of IC-7490	0→ 1→0	
Case: 2	1) Master CLK of 1Hz taken from Trainer module is connected at PIN -14 of IC-7490 and 2) PIN-12 is connected to PIN-1 of IC-7490	0→1→2→3→4 →5→6→7→8 →9→0	
Case: 3	1) Master CLK of 1Hz taken from Trainer module is not connected at PIN -14 of IC-7490 and 2) PIN-12 is not connected to PIN-1 of IC-7490 3) Master CLK of 1Hz taken from Trainer module is connected at PIN -1 of IC-7490	0→1→2→3→4 →0	

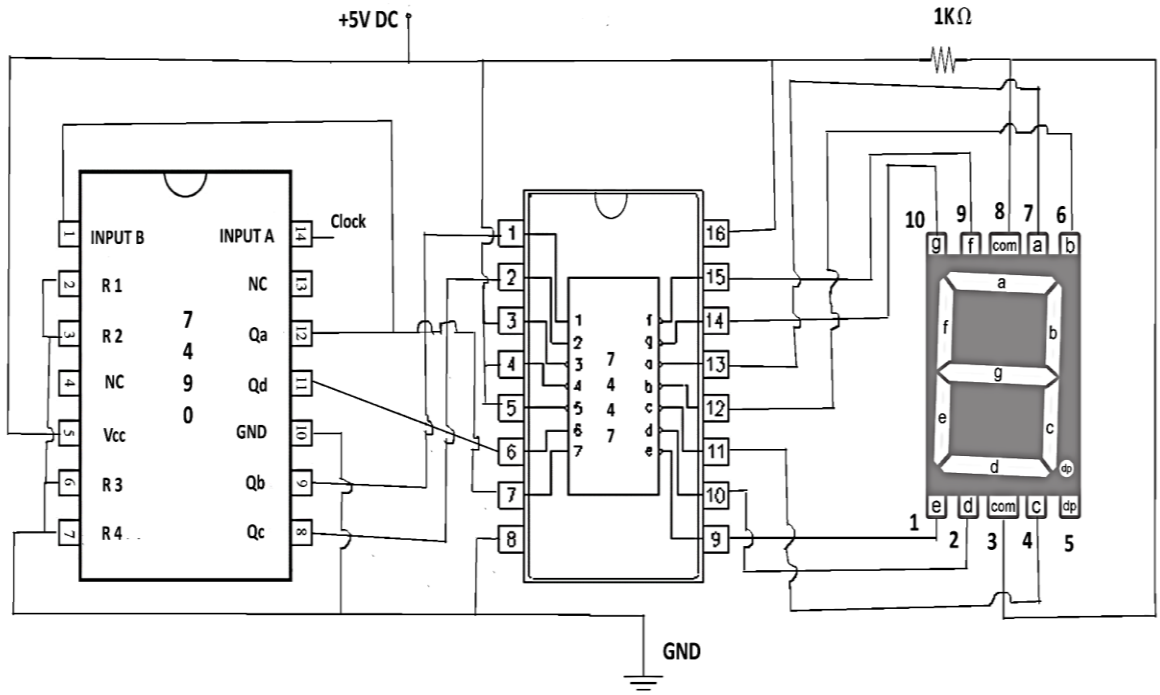


Figure 7: Connection diagram as per CASE-2

8 **Precautions**:

8.1 Do not press the IC on breadboard until pins are aligned with pours.
8.2 Make connection properly.
8.3 There should not any short circuit in the circuit.
8.4 Avoid the heating of IC.
8.5 Provide proper clock pulse.

9. **Learning Outcomes (expected):**

10.1 Connect the circuit diagram using breadboard, and Digital Trainer module.
10.2 Use IC7490 as MoD-2. MoD-5 and MoD-10 Counter.
10.3 Identify Common anode and common cathode display.
10.4 Identify faults in the connection diagram.

10. **Learning Outcomes (What I have learnt):**

1. Which type of seven segment display IC is used in this experiment?
   Ans:

2. What should be the value of a, b, c, d, e, f and g, if we have to display 6?
   Ans:

3. What happens if CLK is directly connected to PIN 1 of IC 7490 and Pin 14 is left open?
   Ans:

4. How to check if Seven segment display is functional or not?
   Ans: