

$$V = IR$$

$$P = VI$$
 watt

$$G = \frac{1}{R}$$
 Conductance

$$V = \frac{W}{Q}$$
 (volt) work done / charge

$$P = I^2 R = \frac{V^2}{R}$$

$$I = C \frac{dV}{dt}$$
 A C = conductance

$$P = C V \frac{dV}{dt}$$

$$X_C = \frac{1}{\omega C}$$
 (N)

$$E = \frac{1}{2} CV^2$$
 J → Energy in capacitor

$$V = L \frac{dI}{dt}$$
 L = Inductance Energy

$$E = \frac{1}{2} LI^2$$

Star to Delta,  $Z_1 = Z_A + Z_B + \frac{Z_A Z_B}{Z_C}$ ,  $\frac{1}{C_1} = \frac{1}{C_A} + \frac{1}{C_B} + \frac{C_A C_B}{C_A C_B}$

Delta to star,  $Z_A = \frac{Z_1 Z_3}{Z_1 + Z_2 + Z_3}$ ,  $\frac{1}{C_A} = \frac{1}{C_1} + \frac{1}{C_3}$

Current division,  $I_2 = \frac{I R_1}{R_1 + R_2}$ ,  $I_1 = \frac{I R_2}{R_1 + R_2}$

Voltage division,  $V_1 = \frac{V R_1}{R_1 + R_2}$ ,  $V_2 = \frac{V R_2}{R_1 + R_2}$

Mess = Branch - (Node-1) Node eq = N-1 CN = Principal node

$$I_L = \frac{V_{TH}}{R_{TH} + R_L}$$

$$I_N = \frac{V_{TH}}{R_{TH}}$$

$$P_{max} = \frac{V_{TH}^2}{4R_{TH}}$$

$$P_{max} = I_L^2 R_L$$

$$I = I_m \sin(\omega t + \theta)$$

$$I_{avg} = \frac{2 I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$K_f = \frac{r_{ms}}{r_{avg}} = 1.011$$
 (load factor)

$$\text{Gest/Peak/Ampitude factor} = \frac{\text{max}}{\text{rms}} = \sqrt{2}$$

$$P = V_{rms} I_{rms}$$

$$V = \sqrt{V_R^2 + V_C^2}$$

$$V = \sqrt{V_R^2 + (V_L - V_C)^2}$$

$$V = IR$$

$$|Z| = \frac{V_m}{I_m}$$

$$|Z| = \sqrt{R^2 + X_L^2}$$

$$\theta = \tan^{-1} \left( \frac{X_L}{R} \right)$$

$$f = \frac{1}{2\pi\sqrt{LC}}$$

UNIT-1 DC CIRCUITSVoltage / Potential

The amount of workdone to bring a unit positive charge from  $\infty$  to a point is voltage.

$$V = \frac{W}{Q} \quad \text{Volt (V)}$$

Ohm's Law

$$V \propto I$$

$$V = IR$$

$$G = \frac{1}{R} \quad (G = \text{conductance})$$

$$P = VI$$

$$P = I^2 R = \frac{V^2}{R} \quad \text{Watt}$$

Capacitor - The property of material which stores energy in a EF is known as Capacitance (C) Unit  $\Rightarrow$  Farad (F)

$$i = C \frac{dv}{dt}$$

$$P = VI$$

$$P = C V \frac{dv}{dt}$$

$$E = \int pdt$$

$$E = \frac{1}{2} CV^2$$

Inductance - The property of material which stores energy in MF is inductance. (Henry)

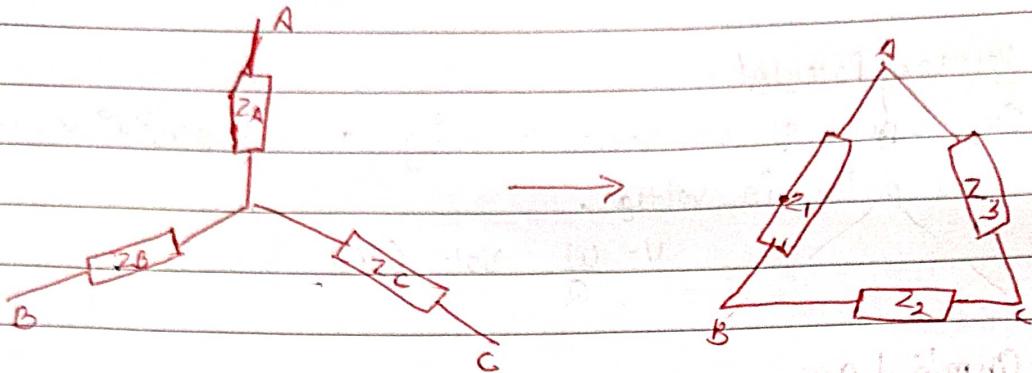
$$V = L \frac{di}{dt}$$

$$E = \frac{1}{2} L i^2$$

$$P = LI \frac{di}{dt}$$

$$P = LI \frac{di}{dt}$$

## Star to Delta conversion



$$Z_1 = Z_A + Z_B + \frac{Z_A Z_B}{Z_C}$$

In case of capacitor

$$Z_2 = Z_B + Z_C + \frac{Z_B Z_C}{Z_A}$$

$$Z_3 = Z_A + Z_C + \frac{Z_A Z_C}{Z_B}$$

$$C_1 = \frac{1}{C_A} + \frac{1}{C_B} + \frac{1}{C_A C_B}$$

## Delta to Star conversion

$$Z_A = \frac{Z_1 Z_3}{Z_1 + Z_2 + Z_3}$$

In case of capacitor

$$Z_B = \frac{Z_1 Z_2}{Z_1 + Z_2 + Z_3}$$

$$\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

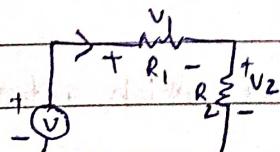
$$Z_C = \frac{Z_1 Z_2}{Z_1 + Z_2 + Z_3}$$

## Kirchoff's Laws -

### KVL (Kirchoff Voltage Law)

$$\sum V = 0$$

$$\sum V_{\text{drop}} = \sum V_{\text{rise}}$$

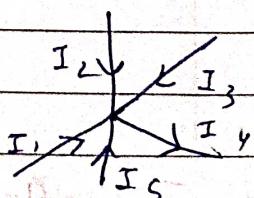


$$-V_1 + I_1 R_1 + I_2 R_2 = 0$$

$$V = I_1 R_1 + I_2 R_2$$

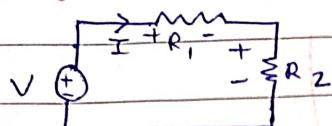
$$V = V_1 + V_2$$

### KCL (Kirchoff Current Law)



$$I_1 + I_2 + I_3 - I_4 + I_S = 0$$

$$I_1 + I_2 + I_3 + I_S = I_4$$

Voltage Division Rule

$$-V + IR_1 + IR_2 = 0$$

$$V = I(R_1 + R_2)$$

$$I = \frac{V}{R_1 + R_2}$$

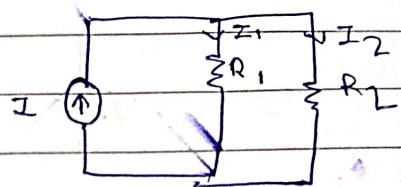
$$V_{R_1} = IR_1$$

$$V = \frac{IR_1}{R_1 + R_2}$$

$$V_1 = IR_1$$

$$V_1 = \frac{VR_1}{R_1 + R_2}$$

$$V_2 = \frac{VR_2}{R_1 + R_2}$$

Current Division

$$V = I_1 R_1 = I_2 R_2 \quad [I_1 = I_2]$$

$$I = I_1 + I_2$$

$$I = \frac{R_2 I_2 + I_2}{R_1}$$

$$I_2 = \frac{IR_1}{R_1 + R_2}$$

$$I_1 = \frac{IR_2}{R_1 + R_2}$$

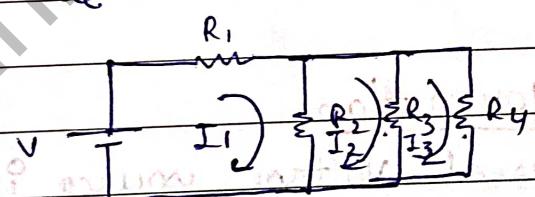
Mesh Analysis

$$M = B - (N - 1)$$

$\downarrow$   
node

(KVL + Ohm's law)

[No. of mesh = M, B = Branches]



$$B = 4$$

$$n = 2$$

$$M = 4 - (2 - 1)$$

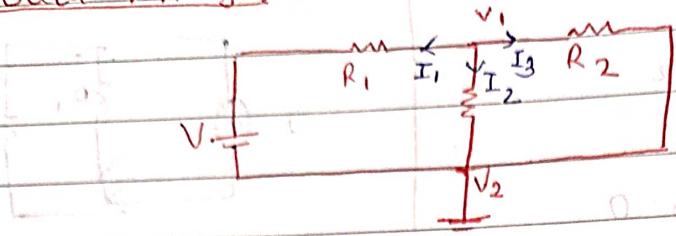
$$\boxed{M = 3}$$

→ Calculate the mesh

→ Write mesh eq. using KVL

→ Find current

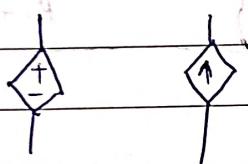
## Nodal Analysis (KCL + Ohm's law)



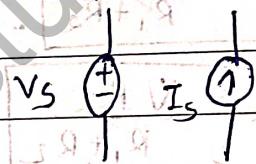
- Identify principal node and selected reference node and treat it as ground voltage.
- Write nodal eqns for all nodes except reference node using KCL [nodal eqn =  $(n-1) \times$  Principal node]

## Source Conversion

Dependent source (indicated by diamond)



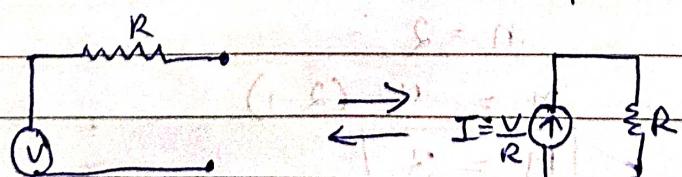
Independent source (indicated by circle)



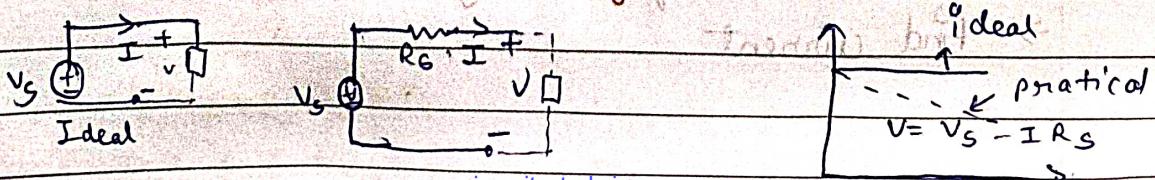
- 1) Voltage Controlled Voltage Source
- 2) Current Controlled Voltage Source
- 3) Voltage Controlled Current Source
- 4) Current controlled Current Source

## Source Transformation

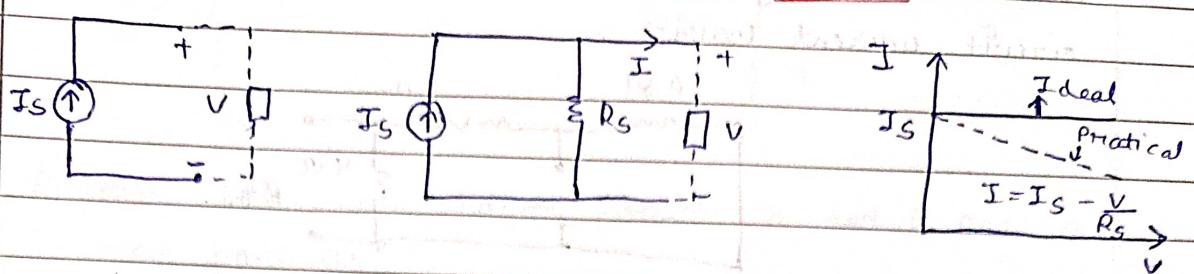
We can represent voltage source in series with resistance as current source with parallel resistance.



## Ideal voltage / Practical voltage source



## Ideal Current / Practical current source

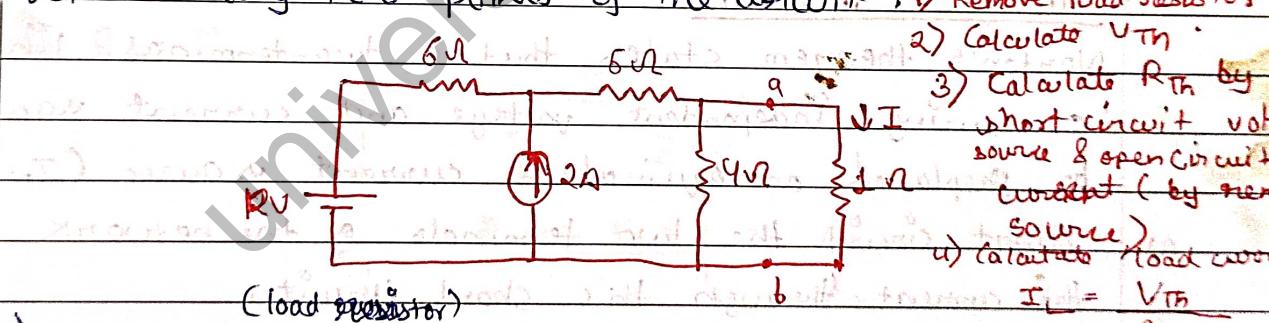


## Network Theorems

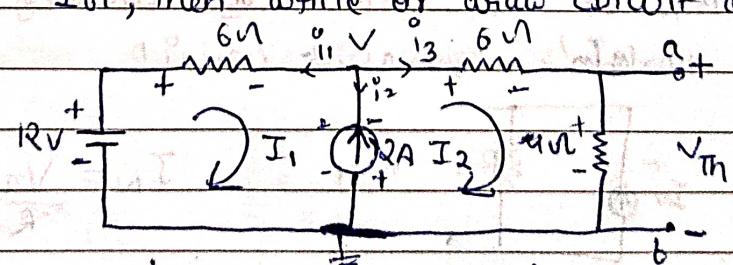
1. Superposition Theorem
2. Thévenin's Theorem
3. Norton's Theorem
4. Maximum Power transfer Theorem

## Thévenin's Theorem

It states that it is possible to simplify any linear circuit containing independent and dependent voltage and current sources, no matter how complex, to an equivalent circuit with just a single voltage source and series resistance between any two points of the circuit.



1) Remove  $R_L$ , then write or draw circuit again



$$\text{At loop 1, } -12 + 6I_1 = 0$$

$$I_1 + I_2 + I_3 = 0$$

$$\frac{V - 12}{6} + (-I_2) + \frac{V}{10} = 0$$

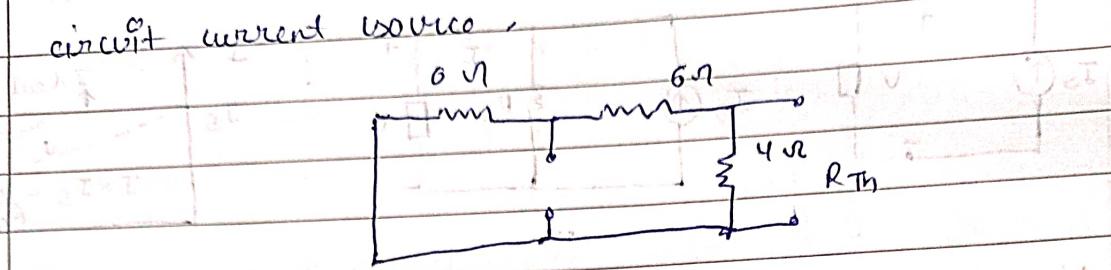
$$V = 15$$

$$I_3 = \frac{15}{10} = 1.5 \text{ A}$$

$$V_{TH} = 1.5 \times 4$$

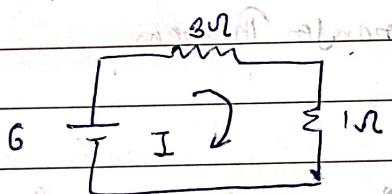
$$V_{TH} = 6 \text{ V}$$

(1) Calculate  $R_{TH}$  by short circuit of voltage source and open circuit current source.



$$R_{TH} = \frac{12 \times 4}{12 + 4} = \frac{48}{16} = 3\Omega$$

(2) Thevenin's equivalent circuit



$$\text{Using Kirchhoff's Law, } I_2 = \frac{V_{TH}}{R_{TH} + R_L} = \frac{6}{3 + 1} = 1.5 \text{ A}$$

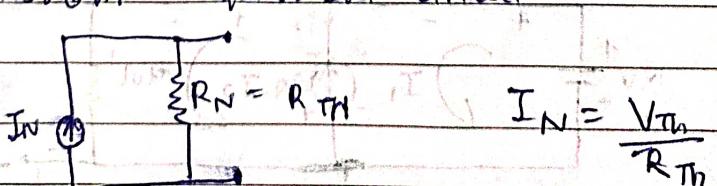
### Norton's Theorem

Norton's theorem states that a two-terminal linear network containing independent voltage and current sources may be replaced by an equivalent current source ( $I_N$ )

(1) Short circuit the two terminals of the network and determine the current through this short circuit.

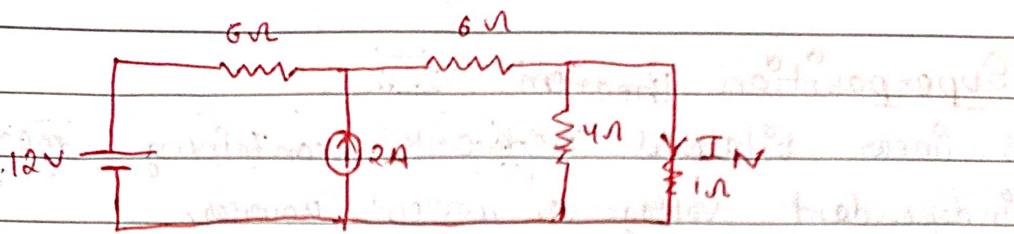
(2) Calculate  $R_N$  or  $R_{TH}$ . (Same by removing source)

(3) Draw Norton's equivalent circuit



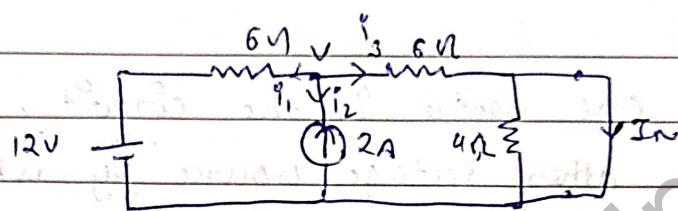
$$I_N = \frac{V_{TH}}{R_{TH}}$$

(Q)



1)

Remove  $6\Omega$ , and short circuit a and b and calculate current in that path as  $I_N$ .



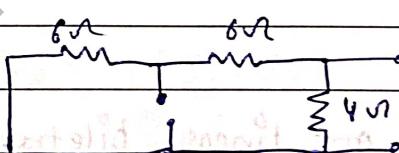
By Applying KCL,  $i_1 + i_2 + i_3 = 0$

$$\frac{V-12}{6} - 2 + \frac{V}{4} = 0$$

$$V - 12 - 12 + V = 0$$

$$V = 12 \text{ Volts}$$

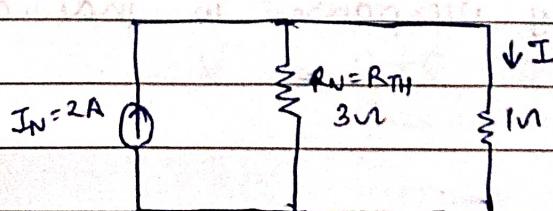
$$I_N = i_3 = \frac{V}{4} = \frac{12}{4} = 3 \text{ A}$$

(Q)  $R_N = R_{TH}$ 

$$R_N = \frac{12 \times 4}{12 + 4} = 3.7 \Omega$$

(3)

Norton equivalent circuit



$$I = \frac{2 \times 3}{3+1} = \frac{6}{4} = 1.5 \text{ A}$$

## Superposition Theorem

A linear bilateral network containing more than one independent voltage or current sources.

This theorem is applicable only to a linear network containing independent or dependent source.

Replace

### Steps

- 1) Select any one source in the circuit,
- 2) Replace all other voltage source by short circuit and current source by open circuit.
- 3) If the dependent sources are there then remain undisturbed,
- 4) Determine the magnitude and direction of current through a desire branch as result of single source selected in step ①,
- 5) Repeat step 1-4 for each source.
- 6) Algebraically add all the components current to obtain the desire branch current.

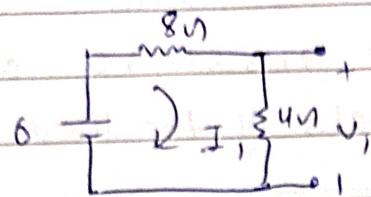
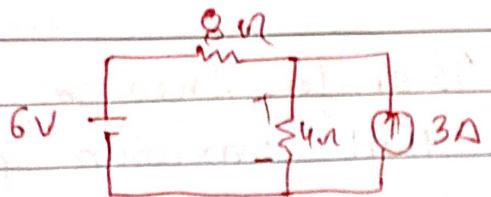
### Limitation

- Only applicable on linear bilateral.
- There should be more than one energy sources.
- We cannot measure or drawn power.

### Advantage

- We can identify response in individual element.

(Q5)

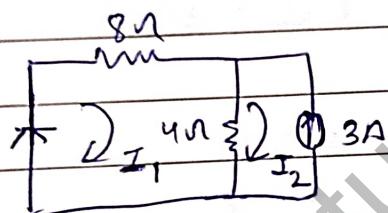


$$-6 + 8I_1 + 4J_1 = 0$$

$$I_1 = 0.5A$$

$$V_1 = 4 \times 0.5$$

$$V_1 = 2V$$



$$8J_1 + 4(J_1 - I_2) = 0$$

$$[I_2 = -3A]$$

$$[J_1 = -1A]$$

$$\begin{aligned} V_2 &= 4(I_2 - I_3) \\ &= 8V \end{aligned}$$



$$V_1 = V_1 + V_2$$

$$V_2 = 4(-1 + 3)$$

$$[V_2 = 8V]$$

$$V = V_1 + V_2$$

$$V = 2 + 8 = 10V$$

111

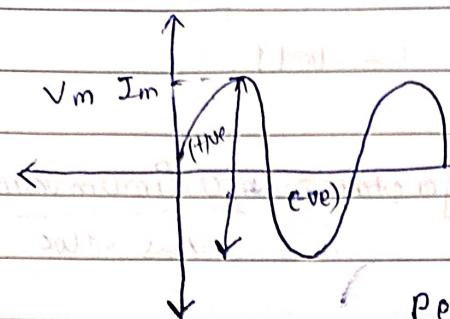
## Maximum Power Transfer Theorem

This theorem states that maximum power is absorbed from a network when the load resistance is equal to the output resistance of the network as seen from the terminals of the load.

$$P_{\max} = \frac{V_{TH}^2}{4R_{TH}}$$

$$V_L = \frac{V_{TH}}{R_{TH} + R_L}$$

$$P_{\max} = I_L^2 R_L$$

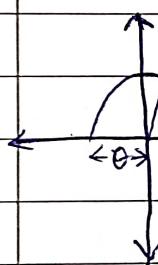
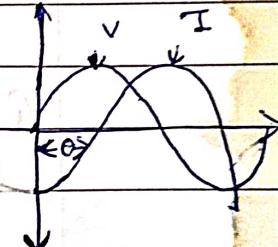
UNIT-2Fundamental of AC CircuitPEAK to PEAK value =  $2V_m$ 

$$I = I_m \sin(\omega t + \phi), (\phi = 0) \text{; then } I = I_m \sin \omega t$$

$$V = V_m \sin \omega t$$

if

$$I = I_m \sin(\omega t - \theta) \text{ (lagging)}$$



$$I = I_m \sin(\omega t + \theta) \text{ (leading)}$$

$$i_{avg} = \frac{i_0 + i_1 + i_2 + \dots}{\pi} = \frac{\text{Area under the curve}}{\text{Total length}}$$

$$i_{avg} = \int i_m \sin \omega t \, d\omega t$$

$$\frac{i_{avg}}{i_m} = \frac{2}{\pi}$$

$$i_{avg} = 0.637 I_m$$

Root mean square value -

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

Form factor (K<sub>f</sub>)

$$K_f = \frac{\text{rms value}}{\text{avg value}} = \sqrt{\frac{\text{Im}^2}{\frac{2 \text{Im}}{\pi}}} = 1.1$$

Greatest or peak or Amplitude factor =  $\frac{\text{maximum value}}{\text{rms value}} = \sqrt{2}$

Rms value and Average value for non-sinusoidal waveforms.

$$V_{\text{rms}} = \left[ \frac{1}{T} \int_0^T V^2(t) dt \right]^{1/2}$$

$$V_{\text{avg}} = \frac{1}{T} \int_0^T V(t) dt$$

In AC circuit,  $R \rightarrow R \Omega$

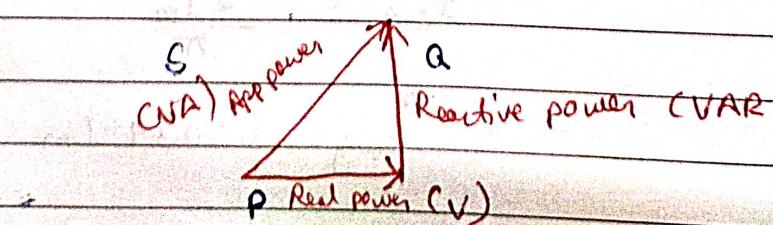
$$\omega L = X_L \Omega$$

$$\frac{1}{\omega C} = X_C \Omega$$

$$Z = \frac{V_m}{I_m} \angle \phi$$

Power concept

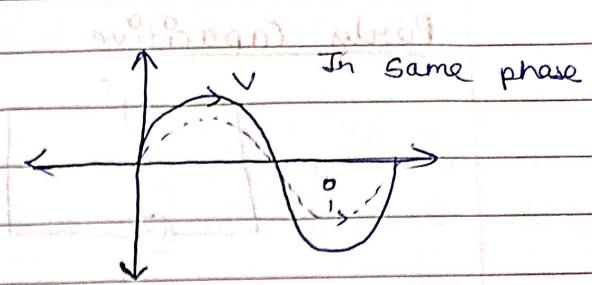
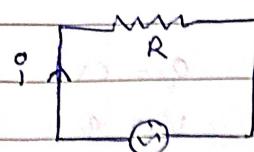
$$\text{Power factor} = \frac{P}{S} = \cos \phi \quad (\phi \text{ is phase diff.}) = \frac{\text{True power}}{\text{Apparent power}}$$



$$P = V_{\text{rm}} I_{\text{rm}} \cos \phi$$

$$Q = V_{\text{rm}} I_{\text{rm}} \sin \phi$$

$$S = V_{\text{rm}} I_{\text{rm}}$$

Purely Resistive Circuit

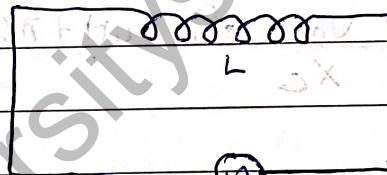
$$V = V_m \sin \omega t$$

$$V = IR$$

$$i = \frac{V_m}{R} \sin \omega t$$

$$i = I_m \sin \omega t$$

$$P = V_{rms} I_{rms} = \frac{V_m I_m}{\sqrt{2}}$$

Purely Inductive Circuit

$$V = L \frac{di}{dt}$$

$$V_m \sin \theta$$

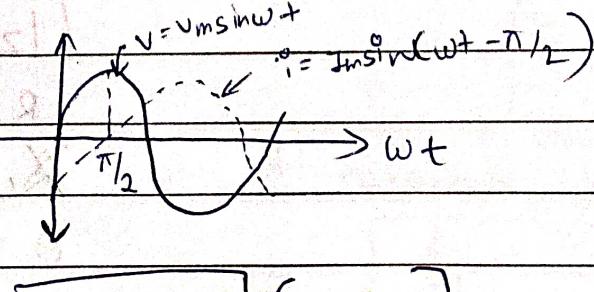
$$V = V_m \sin \omega t$$

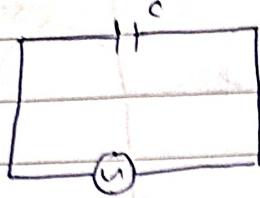
$$i = \frac{V_m}{WL} \sin(\omega t - \pi/2)$$

$$i = I_m \sin(\omega t - \pi/2)$$

$$I_m = \frac{V_m}{WL} = \frac{V_m}{X_L}$$

In inductive current will lag by  $\pi/2$



Purely Capacitive

$$q = CV$$

$$V = \frac{q}{C}$$

$$X_C = \frac{1}{\omega C}$$

$$V = V_m \sin(\omega t + \phi)$$

$$\frac{q}{C} = V_m \sin(\omega t + \phi)$$

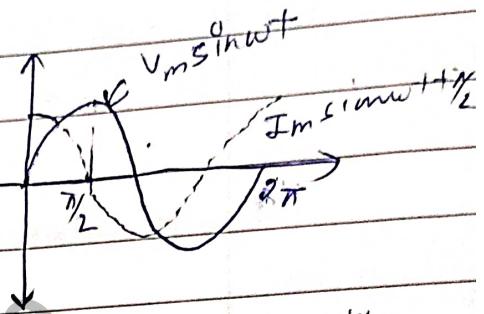
$$i = \frac{dq}{dt}$$

$$\frac{d}{dt} = d(CV_m \sin(\omega t + \phi))$$

$$i = \omega C V_m \sin(\omega t + \phi)$$

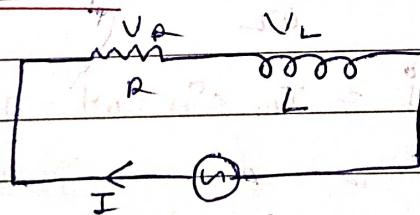
$$i = \frac{V_m \sin(\omega t + \phi)}{\frac{1}{\omega C}}$$

$$i = \frac{V_m \sin(\omega t + \pi/2)}{X_C}$$



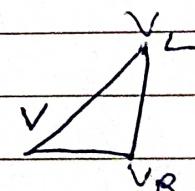
\* Current will lead by  $\pi/2$

$$|P| = 0 \text{ (always)}$$

Series RL circuit

$$V_R = IR$$

$$V_L = IX_L$$



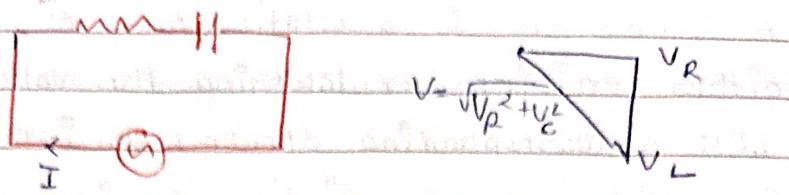
$$V = \sqrt{V_L^2 + V_R^2}$$

$$|Z| = \sqrt{R^2 + X_L^2}$$

$$R_L = Z \cos \theta$$

$$X_L = Z \sin \theta$$

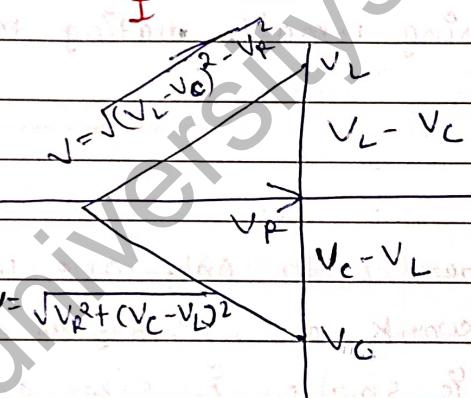
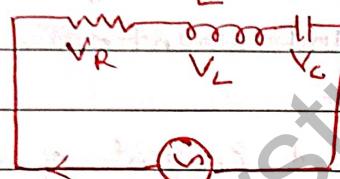
$$\theta = \tan^{-1} \left( \frac{X_L}{R} \right)$$

Series RC circuit

$$V = \sqrt{V_R^2 + V_C^2}$$

$$V_L = -I X_L$$

$$Z = \sqrt{R^2 + X_C^2}$$

Series RLC circuit

$$V = \sqrt{V_R^2 + (V_C - V_L)^2}$$

If  $X_L > X_C$  Inductive

$X_C > X_L$  Capacitive

$$\text{If } X_L = X_C$$

$$V = IR$$

$$Z = \frac{V}{I}$$

At resonant  $X_L = X_C$

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

## Transformer

A transformer is a static piece of equipment used for either raising or lowering the voltage of an ac supply with a corresponding decrease or increase in current.

- It consists of two windings i.e primary and secondary.
- These windings are wound on a common laminated magnetic core.

## Instrumental Transformer

- They are used in AC system for measurement of electrical quantity i.e voltage, current, power.
- Basic fxn of Instrumental Transformer is to step down the AC system Voltage and current.

## Advantages

- The large voltage and current of AC Power system can be measured by using small rating measuring instrument i.e 5A, 110-120V.

## AutoTransformer

It is transformer with only one winding. In this one winding work as primary as well as secondary

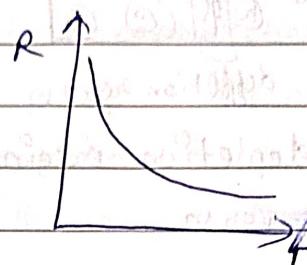
- Auto transformer is smaller in size and cheaper.
- Auto transformer has higher efficiency than two winding transformer because of less ohmic loss and core loss due to reduction of transformer material.

## Unit - 3

### Semiconductor

A semi-conductor is a substance which has resistivity ( $10^{-4}$  to  $0.5 \Omega \text{ m}$ ) in btw insulator and conductor eg) Germanium, silicon, carbon etc.

- Resistivity of semiconductor is less than insulator and more than conductor.
- Resistance increases with rising temp.



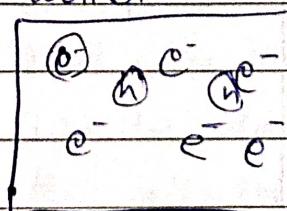
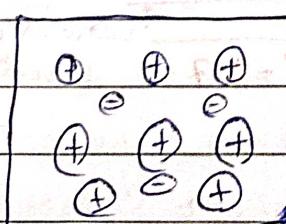
- Chromat → Semiconductors without impurity are intrinsic and with small amount of impurity are extrinsic.
- The process of adding impurity is called doping.

### Extrinsic Semiconductor

P-type (+) (Hole)

N-type (-) (e-)

- When 13<sup>th</sup> group element (B, Al, Ga, In, T) are doped it makes p-type semiconductor.
- When 15<sup>th</sup> group element (P, As, Sb, Bi) are doped it makes n-type semiconductor.
- Holes are majority carriers.
- Electrons are majority carriers.



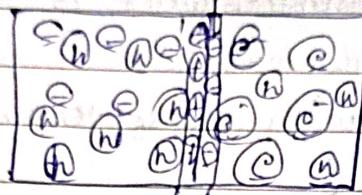
$$S_i = 0.7V$$

$$G_o = 0.3V$$

Saturation current

## PN Junction diode -

- When P-type semiconductor and n-type semiconductor joined by using ion implantation it forms p-n junction.

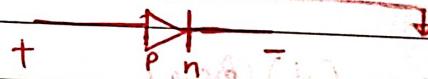


depletion region

- After formation of depletion region, holes in p-type can't move into n-side vice-versa.

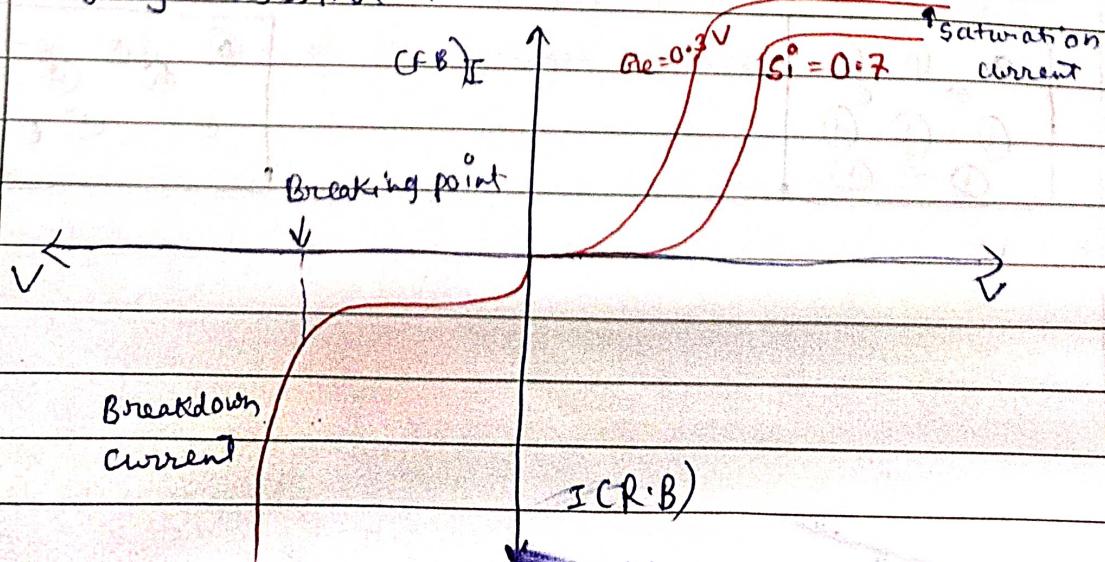
### On applying forward bias (p with + & n with - terminal)

- Depletion region decreases.
- Result in forward current ( $I_F$  Diffusion current).
- Small amount of minority current will also generate but can be neglected.
- Low resistive



### On applying reverse bias (p with - & n with + terminal)

- Depletion region increases.
- Small amount of minority current flows from n to p side known as reverse saturation current ( $I_S$ ).
- Highly resistive.



**Static Resistance**

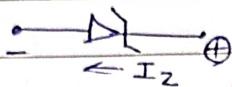
$$\frac{V_D}{I_D}$$

**Dynamic Resistance**

$$\frac{\Delta V_D}{\Delta I_D}$$

1 / 1

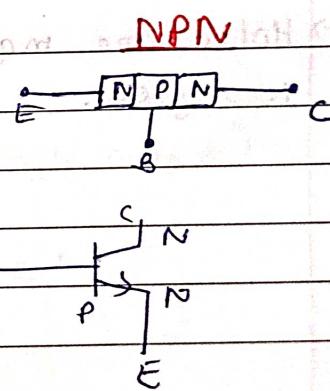
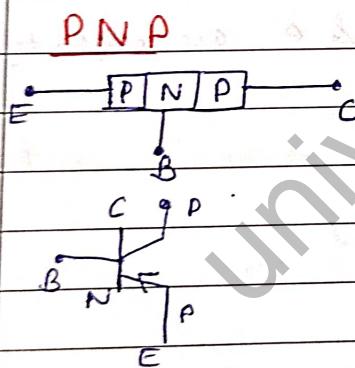
- \* The forward potential at which sharp rise of current occurs is commonly known as offset voltage or threshold voltage or firing or knee voltage.

Zener diode

- Zener diodes are special diodes manufactured with adequate power dissipation capabilities to operate in the breakdown region. It can handle more power dissipation.
- Doping concentration is more for zener diode when compared with normal diode.

Bipolar Junction Transistors

- Transistor has 3 regions. They are emitter, base and collector regions.



- Emitter supply majority charge carriers. It is heavily doped & moderately in size.
- Collector is also reverse biased.

- It is moderately doped, high resistance.
- Base (centre section). Emitter-base is F.B and offers low resistance.

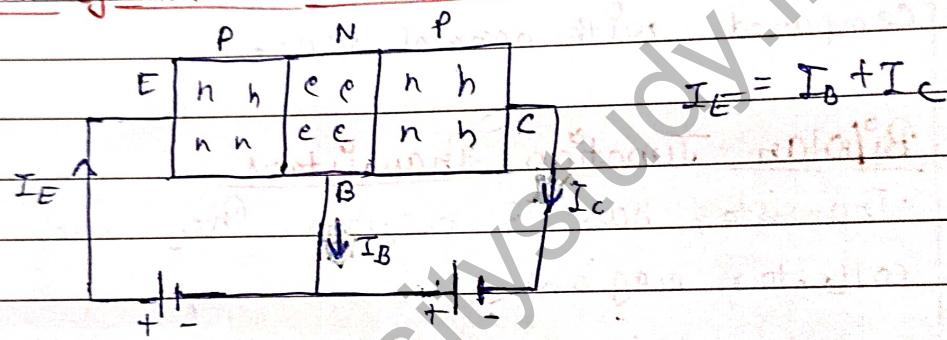
- Emitter is moderately doped, the base is lightly doped and the collector is comparatively more doped.

- Collector size is largest.
- Base is thinnest.

## Transistor Modes of Operation

Type	J <sub>CB</sub>	J <sub>CB</sub>
Active	F <sub>B</sub>	R <sub>B</sub> (Amplifier)
Saturation	F <sub>B</sub>	F <sub>B</sub> ] Switching App
Cut off	R <sub>B</sub>	R <sub>B</sub>
Inversion	R <sub>B</sub>	f <sub>B</sub> (Not in use)

## Operation of Transistor in Active mode

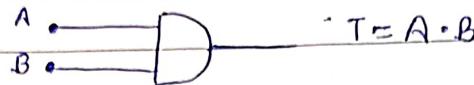


→ Holes are majority charge carriers & e<sup>-</sup> are minority carriers in N-region.

UNIT 4

Logic Gate (Basic Gate) - Basic Building block which can perform basic logical operations.

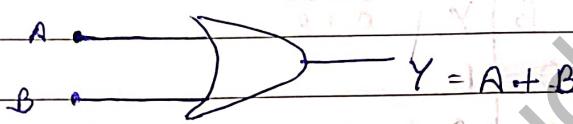
1) AND (Two input or none) (-)



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

multiple input gives single output

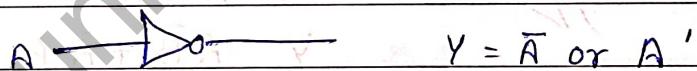
2) OR (+)



Y = A + B --- N  
↑  
single output

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

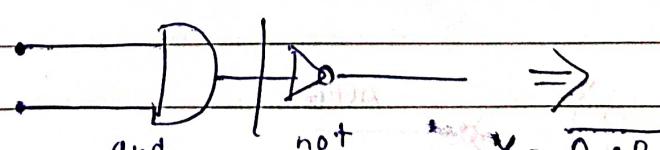
3) Not (Inverter) (Single input  $\rightarrow$  single output)



A	Y
0	1
1	0

Universal Gates

c) NAND

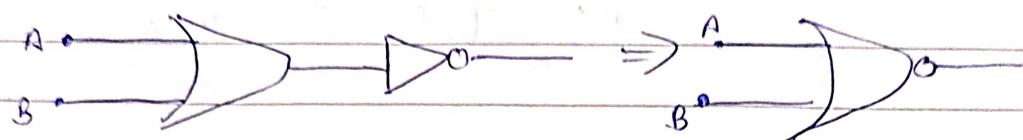


A B | Y ( $\overline{A \cdot B}$ )

0 0	1
0 1	0
1 0	0
1 1	1

Step function

### (iii) NOR

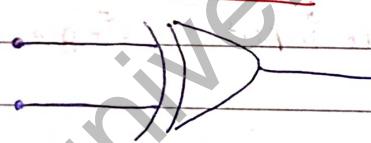


$$Y = \overline{A + B}$$

$$Y = \overline{A} \cdot \overline{B}$$

A	B	Y	$\overline{A + B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

### (iv) Exclusive OR (Ex-OR)



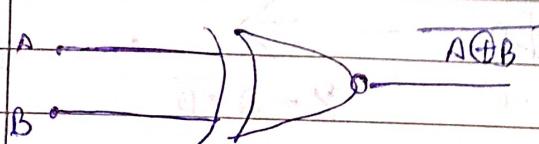
$$Y = A \oplus B$$

$$Y = A \cdot \overline{B} + \overline{A} \cdot B$$

A	B	Y	$(A \oplus B)$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

### (v) Ex-NOR Gate



$$Y = \overline{A \oplus B}$$

$$Y = \overline{A \cdot B} + \overline{\overline{A} \cdot \overline{B}}$$

$$Y = \overline{A \cdot B} + \overline{A} \cdot \overline{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

## Combination (m-tatal combination)

$$m = 2^n$$

$n$  = no. of points

If  $n = 1$

$$M = 2^1 = 2 \text{ (0-1)}$$

If  $n = 2$

$$M = 2^2 = 4 \text{ (0-3)}$$

If  $n = 3$

$$M = 2^3 = 8 \text{ (0-7)}$$

## Boolean fxn

### Boolean law -

- Commutative law -  $A + B = B + A$

$$A \cdot B = B \cdot A$$

- Associative law -  $(A + B) + C = A + (B + C)$

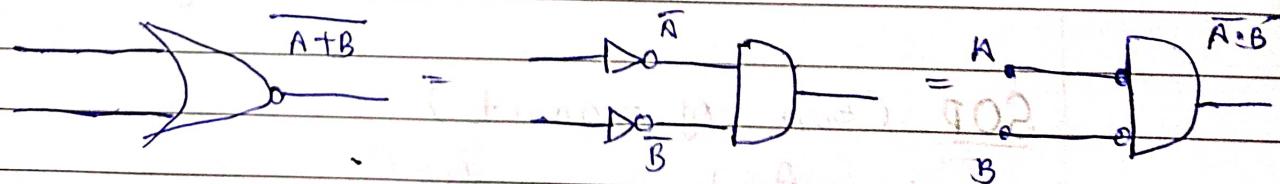
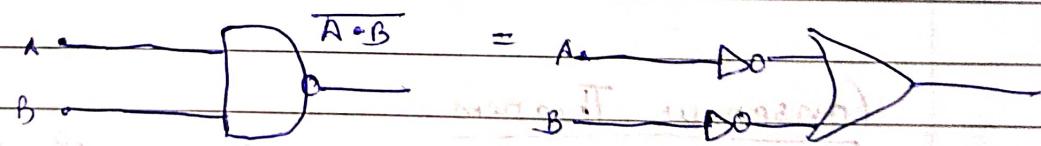
$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$

- Distributive law -  $A \cdot (B + C) = A \cdot B + A \cdot C$

$$A + (B \cdot C) = (A + B) \cdot (A + C)$$

- DeMorgan -  $\overline{A \oplus B} = \overline{A} + \overline{B}$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$



## Boolean Algebra

AND

$$A \cdot 0 = 0 \quad 0 \cdot 0 = 0$$

$$A \circ I = A \quad O \circ I = O$$

$$A^*A = A \quad 1 \cdot 0 = 0$$

$$A \cdot \bar{A} = 0 \quad | \cdot | = 1$$

strains OR

$$A+0 = A \quad 0+0 = 0$$

$$A+1=1 \quad 0+1=1$$

$$n+n=n \quad 1+0=1$$

$$A \cdot \tilde{A} = I \quad \text{and} \quad I + I = I$$

$$\begin{array}{r}
 & 0 & 0 & 1 & * & 1 & & 0 & 1 & 1 & \rightarrow & 0 \\
 + 0 & + 1 & + 0 & + 1 & \text{carry} & - 0 & - 0 & - 1 & - 1 & & \\
 \hline
 0 & 1 & 1 & 10 & & 0 & 0 & 1 & 0 & \xrightarrow{\text{Ans}}
 \end{array}$$

## Transposition Theorem

$$A \circ B + \bar{A} \circ C = (A+C) \circ (\bar{A} + \bar{B})$$

$$R.H.S = (A+C) \cdot (\bar{A}+B)$$

$$A \cdot \bar{A} + A \cdot B + C \cdot \bar{A} + C \cdot B$$

$$A \cdot B + \bar{A} \cdot C + B \cdot C$$

$$A \cdot B + \bar{A} \cdot C + B \cdot C \cdot (A + \bar{A}) \quad ( \text{Multiply missing variable to form you want to remove} )$$

$$A \cdot B + \bar{A} \cdot C + A \cdot B \cdot C + \bar{A} \cdot B \cdot C$$

$$A \cdot B (1+C) + \bar{A} \cdot C (1+B)$$

$$A \circ B + \bar{A} = C$$

## Consensus Theorem

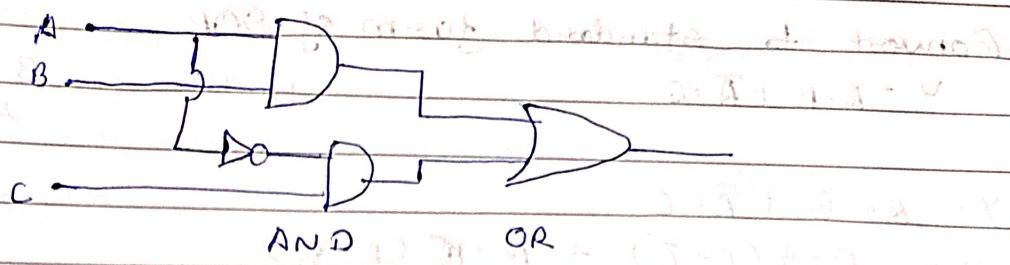
$$A \cdot B + \bar{A} \cdot (C + B) = A \cdot B + \bar{A} \cdot C \quad (\text{if } B \cdot C \text{ is multiply by } A + \bar{A})$$

$$= \bar{A} \cdot (A + B \cdot C) \quad (\text{if } AB \text{ ps multiply by } (+\bar{c}))$$

SOP (Sum of products)

$$A = 1 \quad \bar{A} = 0$$

$$SOP = (A \cdot B \cdot \bar{C}) + (\bar{B} \cdot D) + (\bar{A} \cdot \bar{D})$$



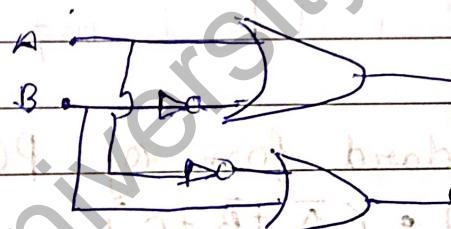
M<sup>o</sup>d term represented by 1

A	B	Minterm
0	0	$\bar{A}\bar{B}$ m <sub>0</sub>
0	1	$\bar{A}B$ m <sub>1</sub>
1	0	$A\bar{B}$ m <sub>2</sub>
1	1	$AB$ m <sub>3</sub>

POS (Product of sum)

$$A = 0 \quad \bar{A} = 1$$

$$\text{POS} = (A + \bar{B}) \cdot (\bar{A} + C + B) \cdot (A + \bar{B} + \bar{C})$$



Max terms represented by 0

A	B	Maxterm
0	0	$A + B$ M <sub>0</sub>
0	1	$A + \bar{B}$ M <sub>1</sub>
1	0	$\bar{A} + B$ M <sub>2</sub>
1	1	$\bar{A} + \bar{B}$ M <sub>3</sub>

1) Convert to standard form of SOP.

$$Y = A \cdot B + \bar{A} \cdot C$$

If there is 3 variable then  
should in 3 digit sum

$$Y = A \cdot B + \bar{A} \cdot C$$

$$Y = A \cdot B (C + \bar{C}) + \bar{A} \cdot C (\bar{B} + B)$$

$$Y = A \cdot B \cdot C + A \cdot B \cdot \bar{C} + \bar{A} \cdot B \cdot C + \bar{A} \cdot B \cdot \bar{C}$$

$$Y = m_7 + m_6 + m_3 + m_1$$

A	B	C	Y
0	0	0	0
0	0	1	1 $m_1$
0	1	0	0
0	1	1	1 $m_3$
1	0	0	0
1	0	1	0
1	1	0	1 $m_6$
1	1	1	1 $m_7$

2) Convert to standard form of POS

$$Y = (A + \bar{B}) \cdot (\bar{B} + C) \cdot (\bar{A} + \bar{B} + C)$$

$$Y = (A + \bar{B}) \cdot (\bar{C} \cdot \bar{C}) \cdot (\bar{B} + C) + (A \cdot \bar{A}) \cdot (\bar{A} + \bar{B} + C)$$

$$Y = (A + \bar{B} + C) \cdot (A + \bar{B} + \bar{C}) \cdot (\bar{B} + C + \bar{A}) \cdot (\bar{B} + C \cdot \bar{A}) \cdot (\bar{A} + \bar{B} + C)$$

$$Y = (A + \bar{B} + C) \cdot (A + \bar{B} + \bar{C}) \cdot (\bar{A} + \bar{B} + C)$$

$$Y = (0 + 1 + 0) \cdot (0 + 1 + 1) \cdot (1 + 1 + 0)$$

$$M_5 \quad M_4 \quad M_1$$

A	B	C	Y
0	0	0	1 $\bar{A} + B + C$
0	0	1	0 $M_1 \quad \bar{A} + B + \bar{C}$
0	1	0	1 $\bar{A} + \bar{B} + C$
0	1	1	1 $\bar{A} + \bar{B} + \bar{C}$
1	0	0	0 $M_4 \quad \bar{A} + B + C$
1	0	1	0 $M_5 \quad \bar{A} + B + \bar{C}$
1	1	0	1 $\bar{A} + \bar{B} + C$
1	1	1	1 $\bar{A} + \bar{B} + \bar{C}$

# Grey code provide 1 bit change

1/1

### K Map Representation (Karnaugh)

$$2 \text{ variable} = 2^2 = 4 \text{ cells}$$

$$3 \text{ variable} = 2^3 = 8 \text{ cells}$$

$$4 \text{ variable} = 2^4 = 16 \text{ cells}$$

	$\bar{B}\bar{B}$	$\bar{B}B$	$B\bar{B}$	$BB$
A	00	01	11	10
$\bar{A}$	10	11	01	00
	2	3	1	0
3 variable	110	111	101	100

A	$\bar{B}\bar{B}$	$\bar{B}B$	$B\bar{B}$	$BB$
$\bar{A}$	00	01	11	10
A	10	11	01	00
$\bar{A}$	2	3	1	0

$A\bar{B}$	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	$BC$	$B\bar{B}$
$\bar{A}\bar{B}$	00	01	11	10	00
$\bar{A}B$	01	11	10	00	11
$A\bar{B}$	11	01	00	11	00

### KMap Simplification Rule

- 1) Construct Kmap and place 1's in the squares according to the truth table.
- 2) Grouping can contain Only 1's
- 3) Grouping can be formed only at right angles, diagonal grp's are not allowed.
- 4) The number of 1's in a grp must be a power of 2.
- 5) The grp must be made as large as possible.
- 6) Groups can overlap and wrap around the sides of the Kmap.
- 7) Every grp puts a term in the solution.

Q)  $F(x, y, z) = \sum(1, 2, 3, 4, 7)$

	$\bar{B}C$	$\bar{B}\bar{C}$	$BC$	$B\bar{C}$	$\bar{B}\bar{C}$
A	0	1	1	1	1
$\bar{A}$	1	0	1	0	1

$$Y = \bar{A}C + BC + \bar{A}B + A\bar{B}\bar{C}$$

Q)  $F(A, B, C) = \prod M(0, 3, 6, 7)$  (Max term)

	$\bar{B}C$	$BC$	$\bar{B}\bar{C}$	$B\bar{C}$
A	0	0	1	1
$\bar{A}$	1	0	0	0

$$Y = ABC + \bar{B}\bar{C} + \bar{A}\bar{B}$$

## UNIT-5 COMBINATION CIRCUIT

### Combinational Circuit

Adder - Adder is a digital circuit which performs addition operations.

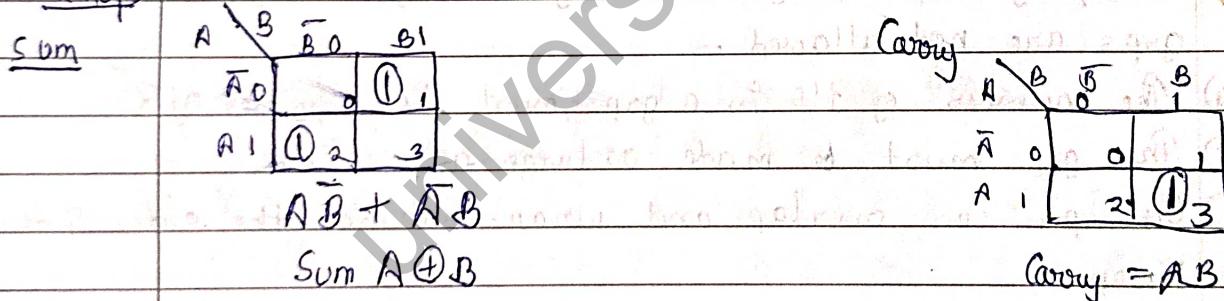
(1) Half Adder - Logic circuits which performs addition of 2 bits is called half adder.

Contains 2 binary input & 2 binary output (sum & carry)

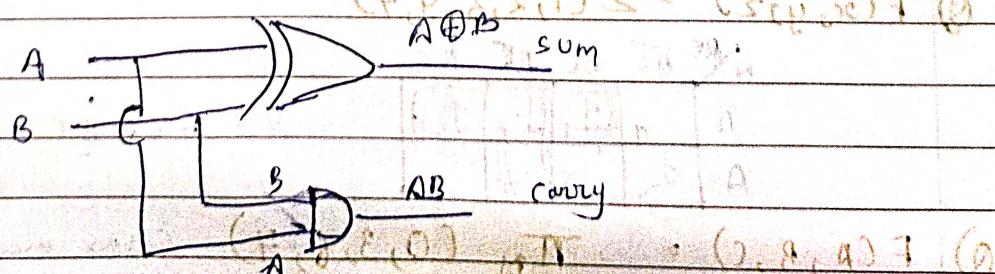


A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

K Map

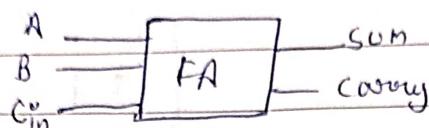


### Logic Circuit



11

Full Adder: Full adder is combinational circuit that performs arithmetic sum of 3 inputs & 2 outputs.  
 $C_{in}$  → represent carry from previous significant terms



A	B	C	Sum	$C_{out}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A	B	C	00	01	11	10
0	0	0	0	1	1	1
0	0	1	1	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	1	1
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	1	1	0
1	1	1	1	1	1	1

$$\text{Sum} = (1, 3, 4, 7)$$

$$\begin{aligned}\text{Sum.} &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\ &\Rightarrow (\bar{A}\bar{B} + AB)C + (\bar{A}B + A\bar{B})\bar{C} \\ &= (\bar{A} \oplus B)C + (A \oplus B)\bar{C}\end{aligned}$$

$$\text{Let } W = A \oplus B$$

$$\bar{W}C + W\bar{C}$$

$$W \oplus C$$

$$\boxed{\text{Sum} = A \oplus B \oplus C}$$

K-Map (Carry)

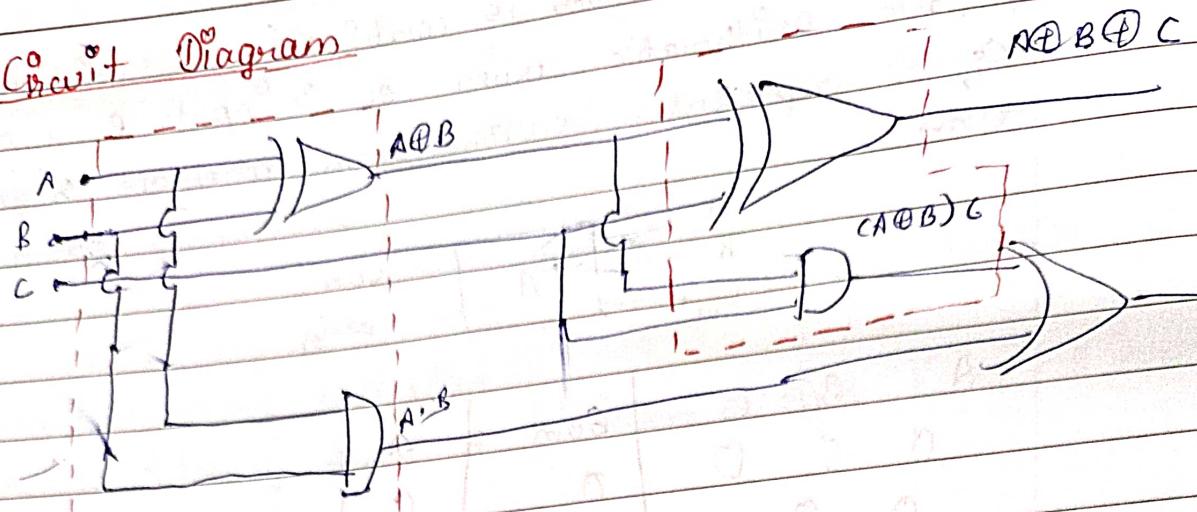
$$(C_{out} = \Sigma(3, 5, 6, 7))$$

A	B	00	01	11	10
0	0	0	1	(1) 3	2
1	0	4	(1) 5	(1) 7	(1) 6

$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

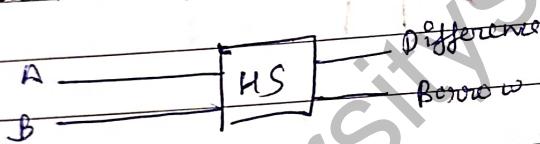
$$= (\bar{A}B + A\bar{B})C + AB(\bar{C} + C)$$

$$= (A \oplus B)C + AB$$

Circuit Diagram

Subtractor: digital circuit which is used to perform subtraction operation.

Half Subtractor - Combination circuit used to perform subtraction of 2 bits



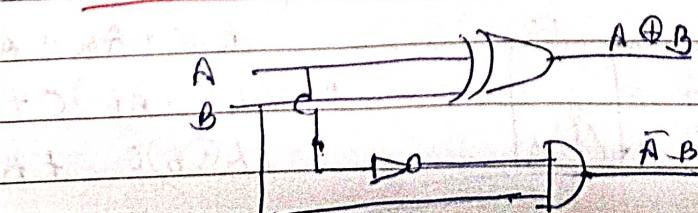
A	B	Diff	Bout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	0

$Diff = A \oplus B$

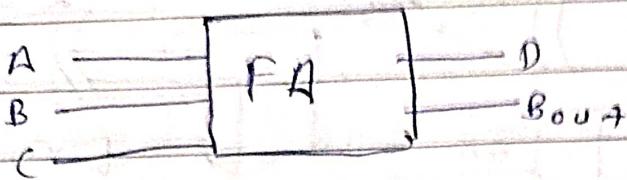
$Bout = \bar{A}B + \bar{A}\bar{B}$

A	B	0	1
0	0	0	1
1	1	2	3

$B_{out} = \bar{A}B$

Circuit Diagram

Full Subtractor - Combinational circuit performs subtraction of 2 binary bits by considering borrow of previous stage. 3 input & output.



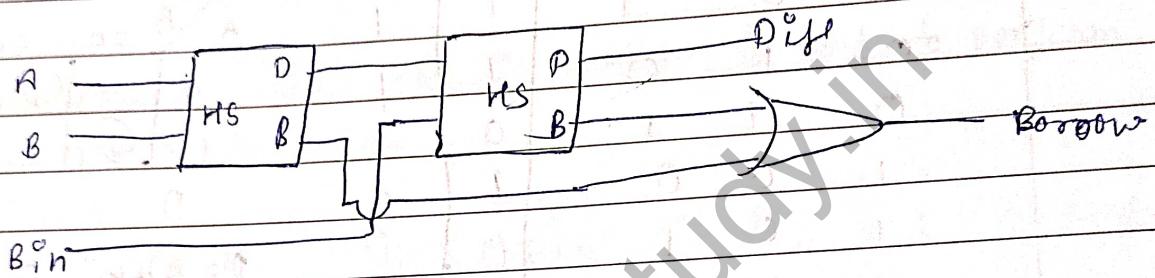
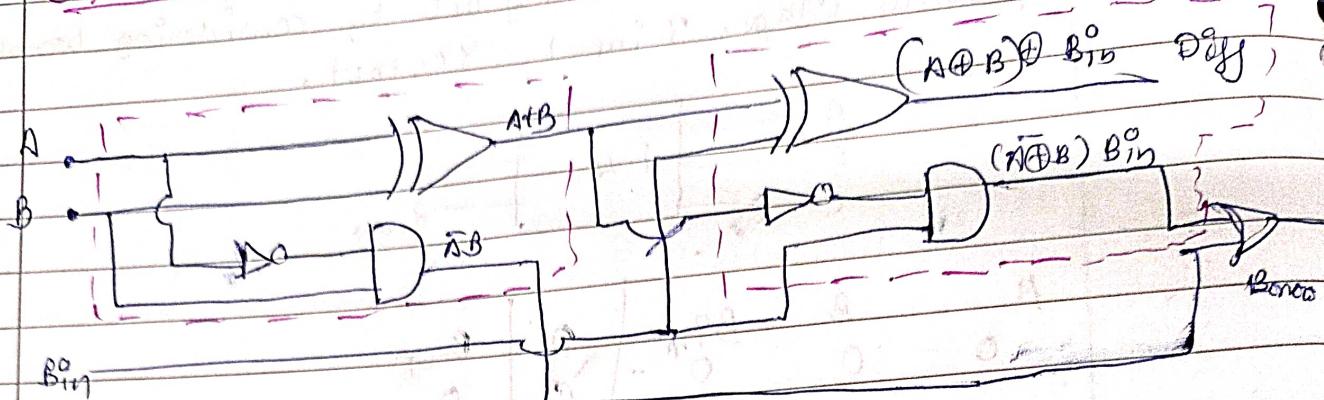
A	B	$B_{in}$	D	$B_{out}$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

A	B	00	01	11	10
0	0	0	1	3	2
0	1	1	0	4	5
1	0	1	0	7	6
1	1	0	0	6	1

$$\begin{aligned}
 D &= \Sigma m(1, 2, 4, 7) \\
 D &= \bar{A}B\bar{B}_{in} + \bar{A}\bar{B}\bar{B}_{in} + A\bar{B}\bar{B}_{in} \\
 &\quad + AB\bar{B}_{in} \\
 D &= (A \oplus B) B_{in}
 \end{aligned}$$

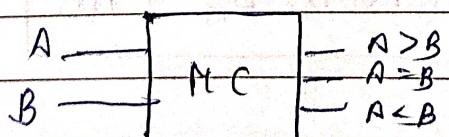
A	B	00	01	11	10
0	0	0	1	3	2
1	0	4	5	7	6

$$\begin{aligned}
 B_{out} &= \bar{A}B\bar{B}_{in} + \bar{A}\bar{B}\bar{B}_{in} + A\bar{B}\bar{B}_{in} + AB\bar{B}_{in} \\
 B_{out} &= (\bar{A} \oplus B) B_{in} + \bar{A}\bar{B}
 \end{aligned}$$

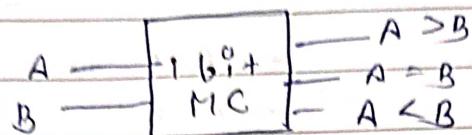
Circuit diagramMagnitude Comparator:

Special combinational circuit designed primarily to compare the relative magnitude of 2 binary numbers

If we have n bit number A & B input and produces 3 outputs  $A > B$ ,  $A < B$ ,  $A = B$



## 1 bit Magnitude Comparator

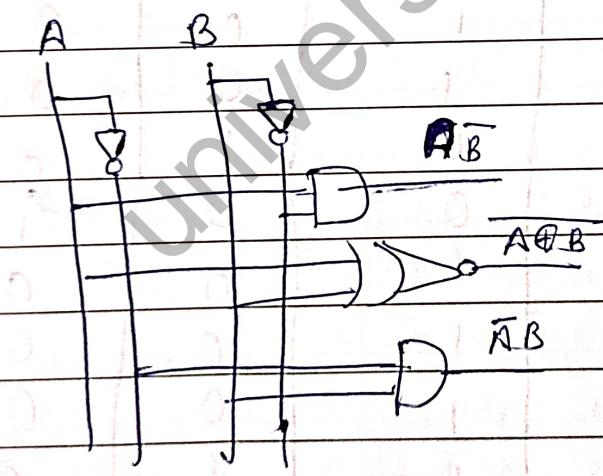


A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$$A > B \rightarrow \Sigma_m(2) \Rightarrow A\bar{B}$$

$$A = B \rightarrow \Sigma_m(0,3) \Rightarrow \overline{A}\bar{B} + A\bar{B}$$

$$A < B \rightarrow \Sigma_m(1) \Rightarrow A\bar{B}$$



## 2-bit Magnitude Operations

A		B		A > B	A = B	A < B
A <sub>1</sub>	A <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>			
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	0
0	0	1	1	0	0	0
0	1	0	0	1	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	0
1	0	0	0	1	0	0
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	0	1	1	0	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

$$A > B \rightarrow \Sigma_m (4, 8, 9, 12, 13, 14)$$

$$A = B \rightarrow \Sigma_m (0, 5, 10, 15)$$

$$A < B \rightarrow \Sigma_m (1, 2, 3, 6, 7, 11)$$

1 /

K Map

(1)  $A > B \Rightarrow \Sigma_m(4, 8, 9, 12, 13, 14)$

$A_1 A_0 \backslash B_1 B_0$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	1	13	15
10	8	9	11	10

$$\Rightarrow A_1 \bar{B}_1 + A_1 A_0 \bar{B}_0 + A_0 \bar{B}_1 \bar{B}_0$$

(2)  $A = B, \Sigma_m(0, 5, 10, 15)$

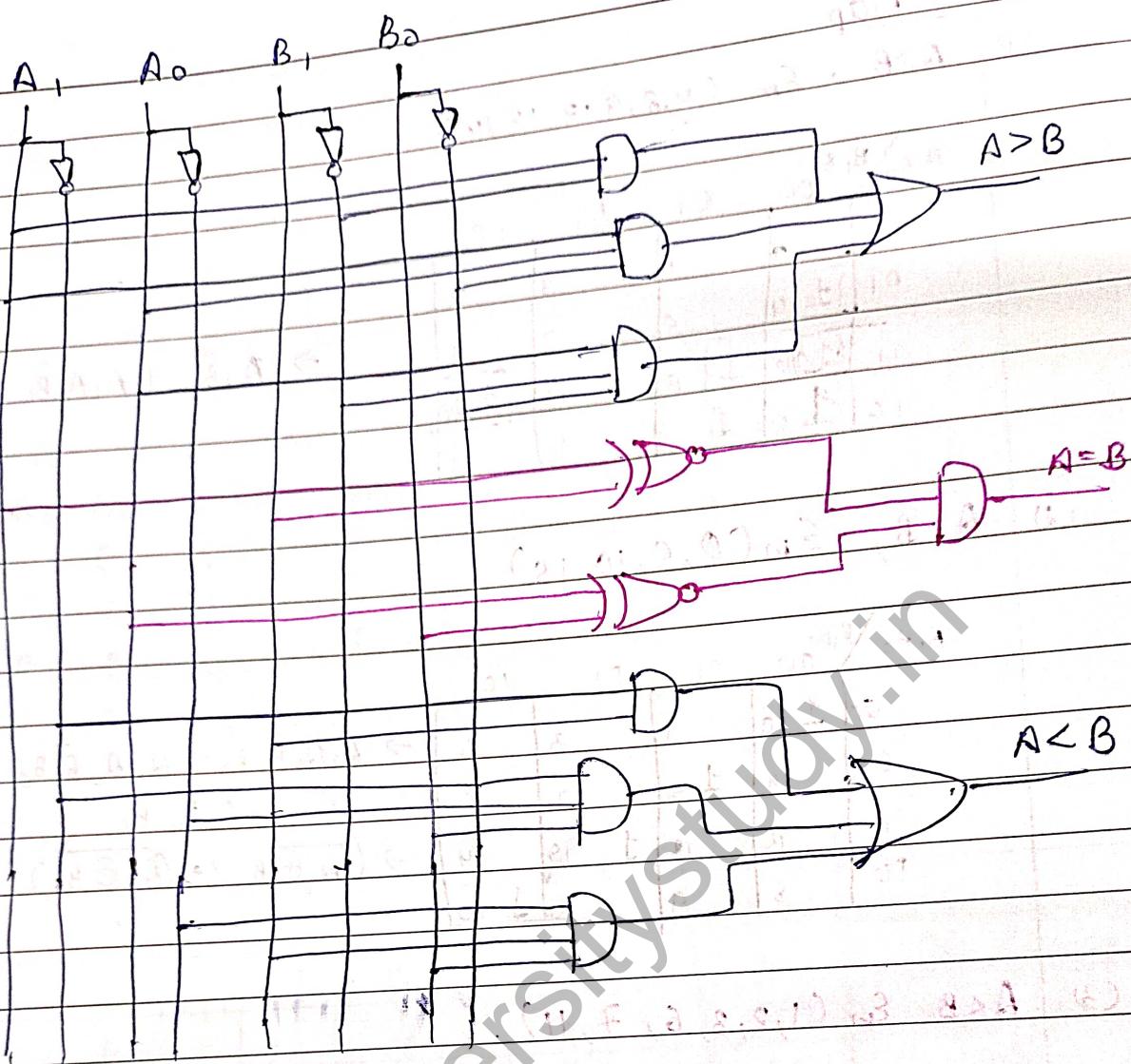
$A_1 A_0 \backslash B_1 B_0$	00	01	11	10	
00	1	0	1	3	2
01	4	5	7	6	
11	12	13	5	15	14
10	8	9	11	10	

$$\Rightarrow \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{A}_0 B_1 B_0 + A_1 A_0 B_1 B_0$$

(3)  $A < B \Sigma_m(1, 2, 3, 6, 7, 11)$

$A_1 A_0 \backslash B_1 B_0$	00	01	11	10	
00	0	1	1	3	2
01	4	5	1	7	16
11	12	13	1	15	14
10	8	9	1	14	10

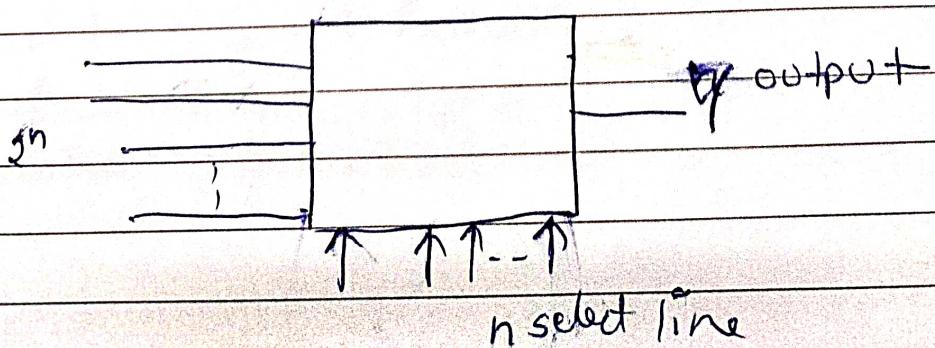
$$\Rightarrow \bar{A}_1 B_1 + A_1 A_0 B_0 + \bar{A}_0 B_1 B_0$$

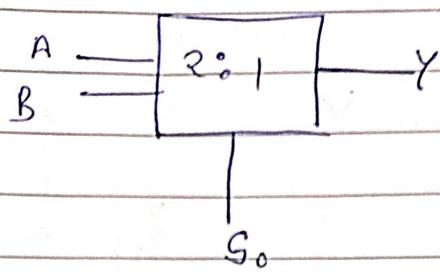


### Multiplexer / Data Selector

Combinational logic circuit that select binary information from one of many input lines and directs it into single output line.

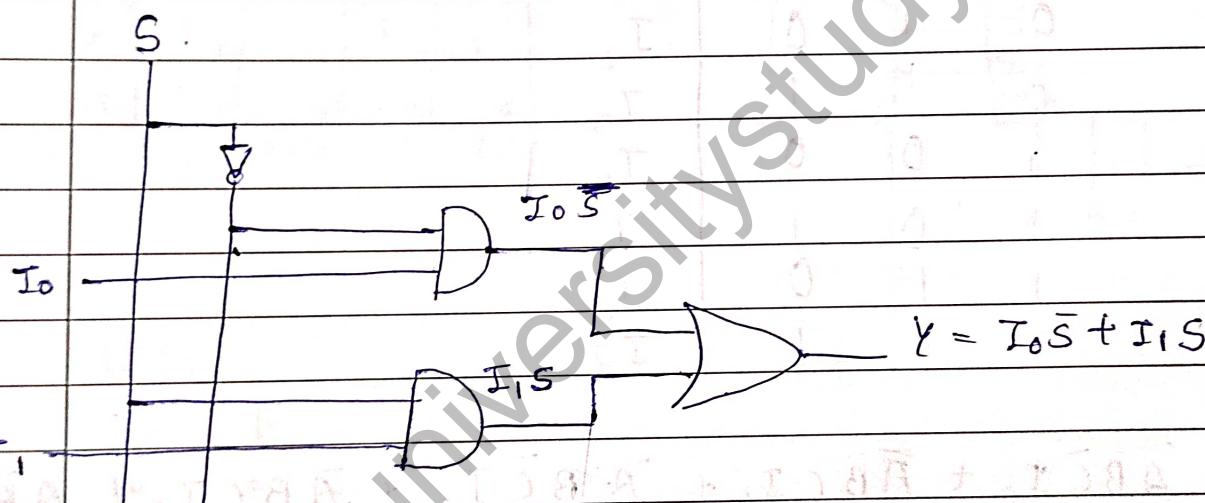
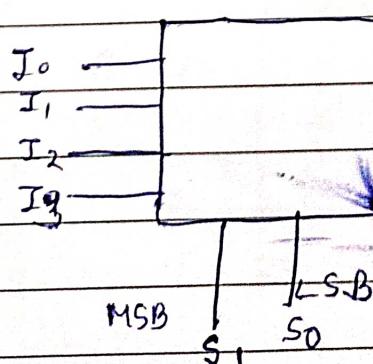
$2^n$  inputs : and  $n$  select lines (parallel to series)



2:1 MUX

S	$I_0$	$I_1$	Y
0	1	0	$0 - Y_1 = I_0$
1	0	1	$1 - Y_2 = I_1$

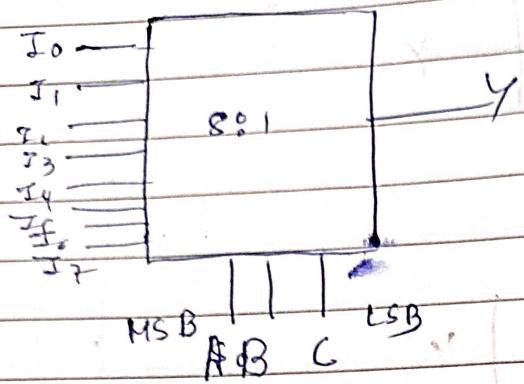
$$Y = I_0 \bar{S} + I_1 S$$

4:1 MUX  $n=2$ 

E	$S_1$	$S_0$	$I_0$	$I_1$	$I_2$	$I_3$
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

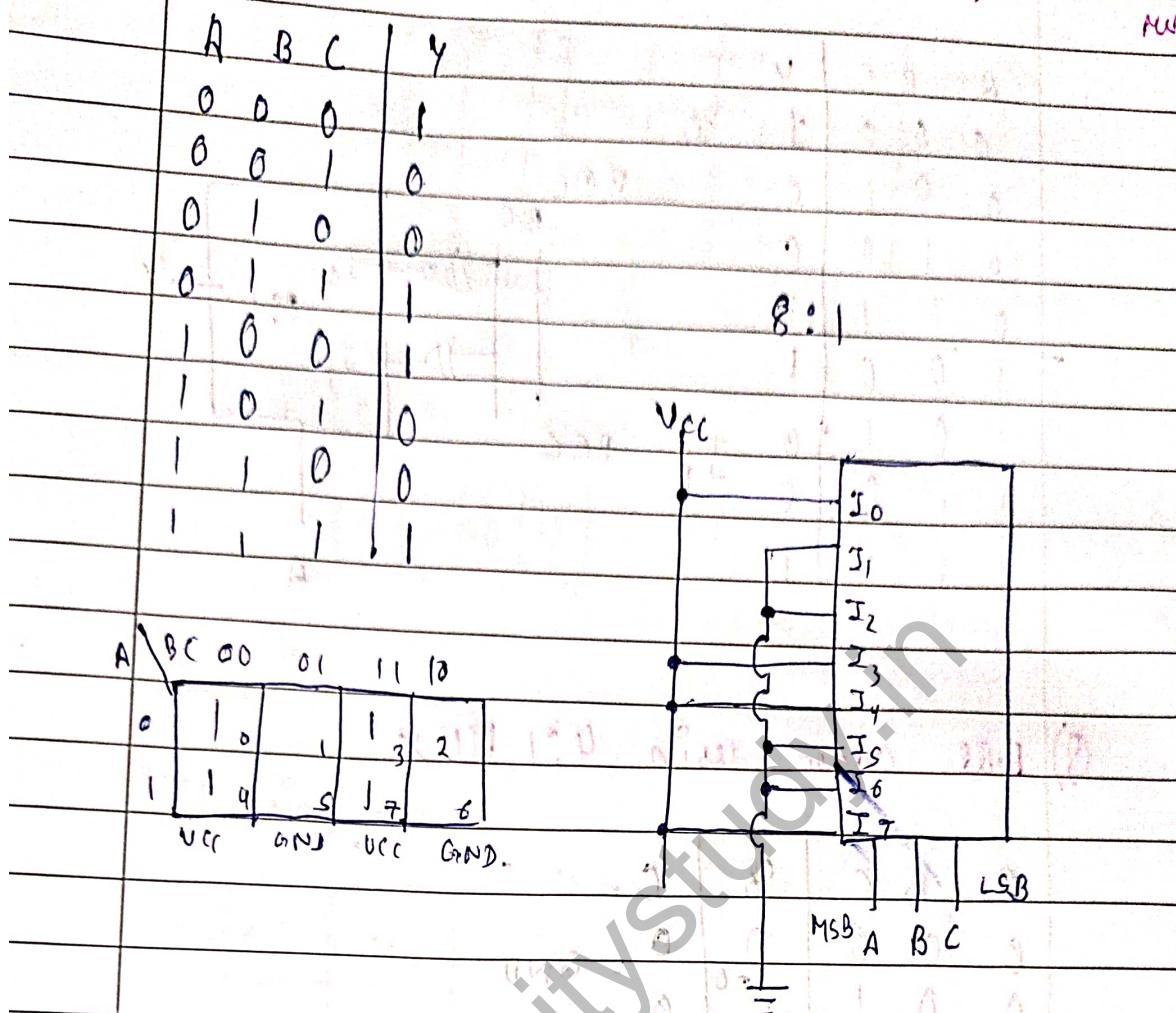
## 8:1 MUX



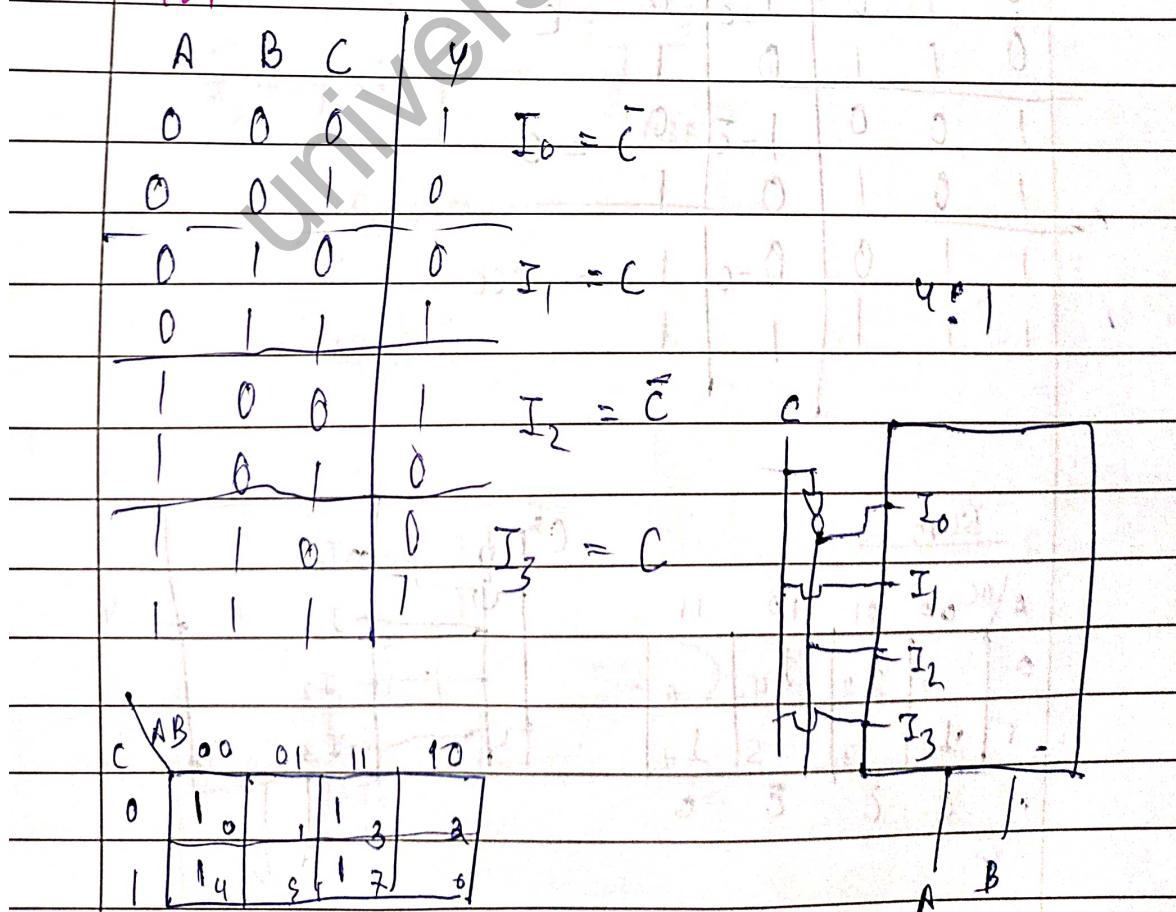
A	B	C	Y
0	0	0	$I_0$
0	0	1	$I_1$
0	1	0	$I_2$
0	1	1	$I_3$
1	0	0	$I_4$
1	0	1	$I_5$
1	1	0	$I_6$
1	1	1	$I_7$

$$Y = \overline{ABC} I_0 + \overline{AB}\overline{C} I_1 + \overline{A}\overline{B}\overline{C} I_2 + \overline{ABC} I_3 + A\overline{B}\overline{C} I_4 + \\ A\overline{B}C I_5 + AB\overline{C} I_6 + ABC I_7$$

Q)  $f(A, B, C) = E_M(0, 3, 4, 7)$  using 8:1 MUX, 4:1 MUX & NMOS



4:1

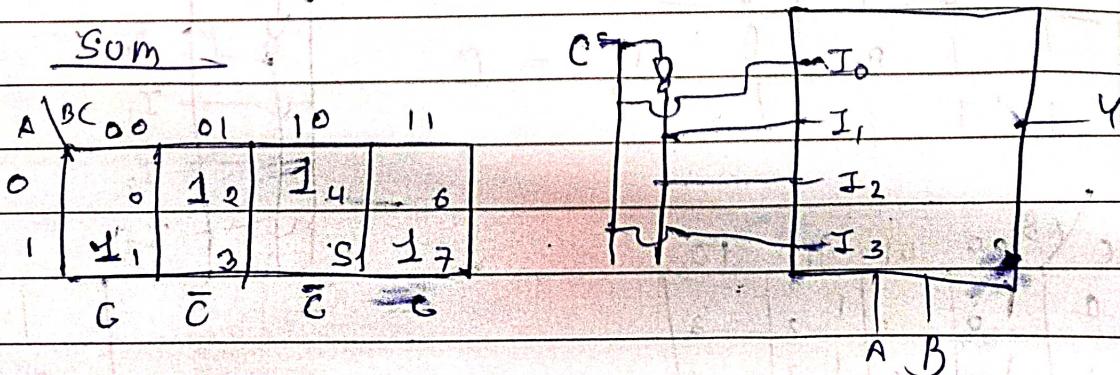


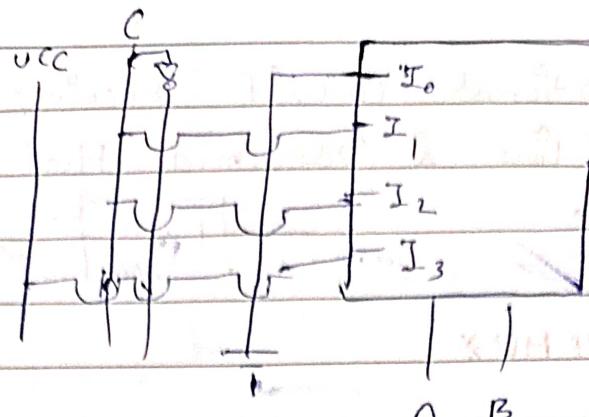
Q1

A	B	C	Y	
0	0	0	1	$I_0$
0	0	1	0	$B \oplus C$
0	1	0	0	$B \oplus C$
0	1	1	1	
1	0	0	1	
1	0	1	0	$I_1$
1	1	0	0	$B \oplus C$
1	1	1	1	

(Q) Full adder using 4:1 MUX

A	B	C	S	C
0	0	0	0	0 = GND
0	0	1	1	0
0	1	0	1	0 = E
0	1	1	0	1
1	0	0	1	0 = C
1	0	1	0	1
1	1	0	0 = C	1 = VCC
1	1	1	1	1

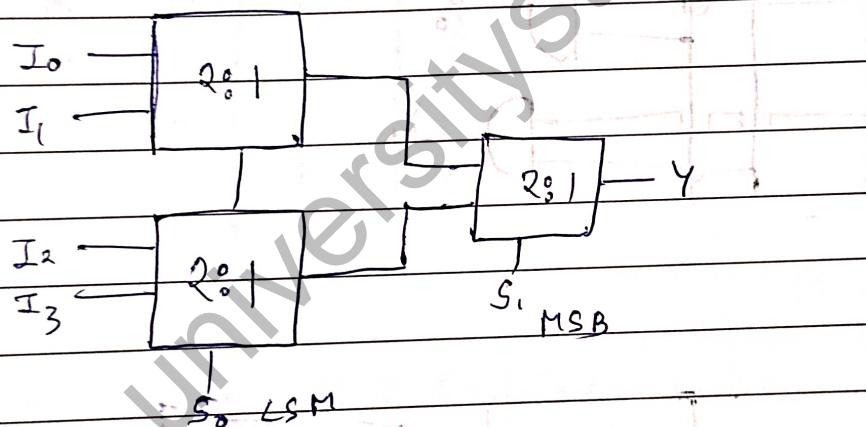


Carry

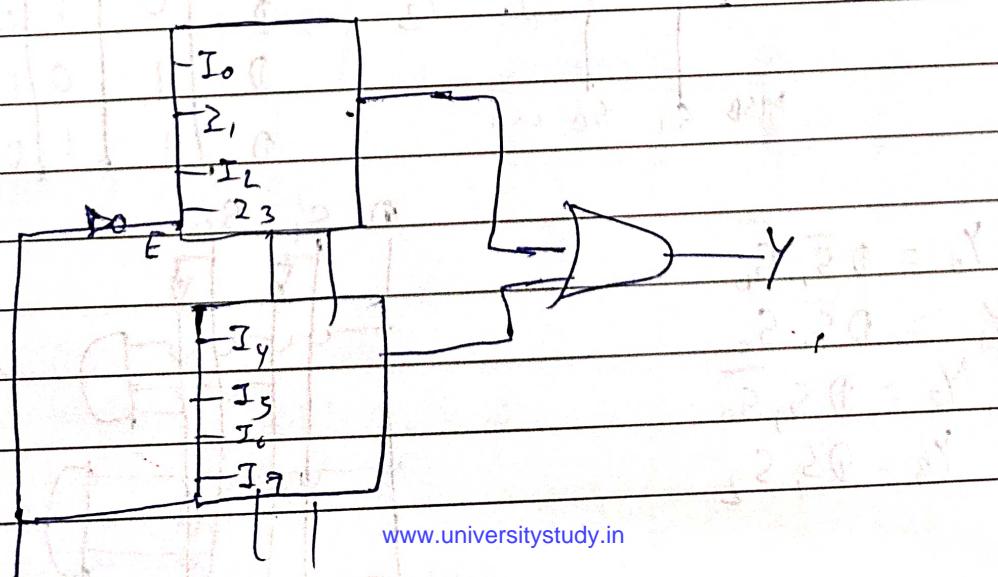
	A	B	00	01	10	11
0	0	0				
1	1	1	0	0	0	0
C	C	C	Vcc			

### MUX Tree

4:1 using 2:1



8:1 using 4:1



## Multiplexer / Data Distributor

(series to parallel)

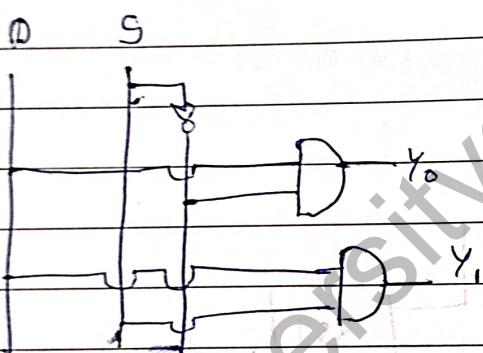
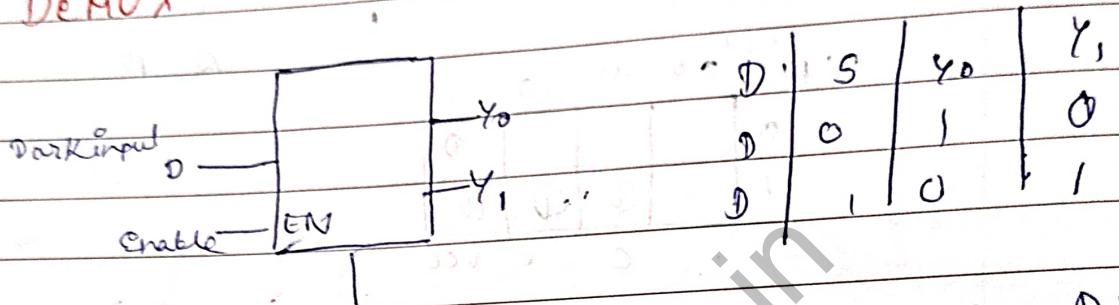
Combinational circuit receives information on a single input line & transmit that info. on one of  $2^n$  possible outputs.

$$1 \times 2^n \text{ series} = 2^n \text{ o/p line}$$

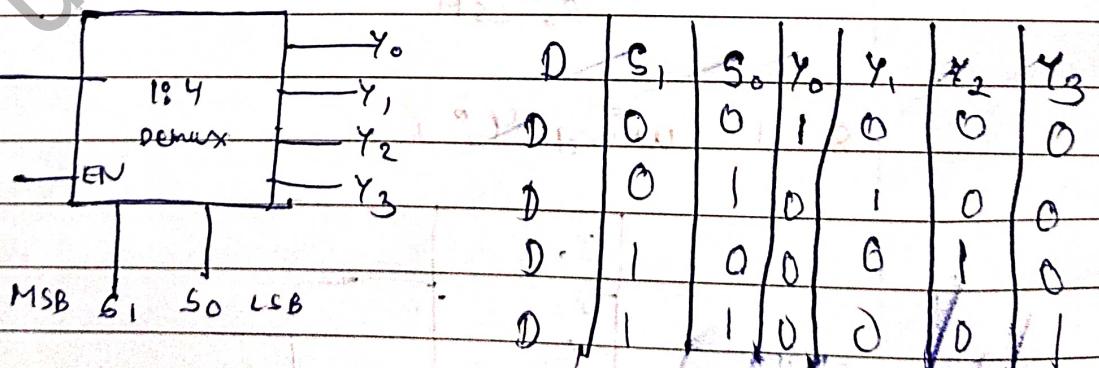
$E=0$  non-operation

$E=1$  operation

### (1) 1:2 DEMUX



### (2) 1:4

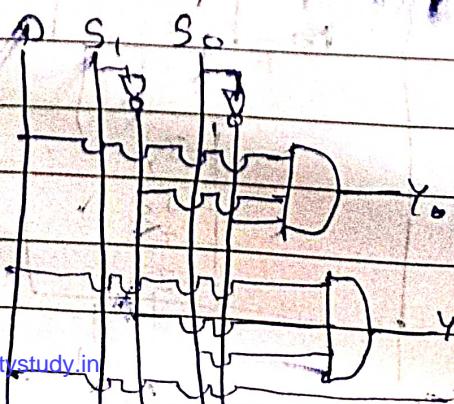


$$Y_0 = D \bar{S}_1 \bar{S}_0$$

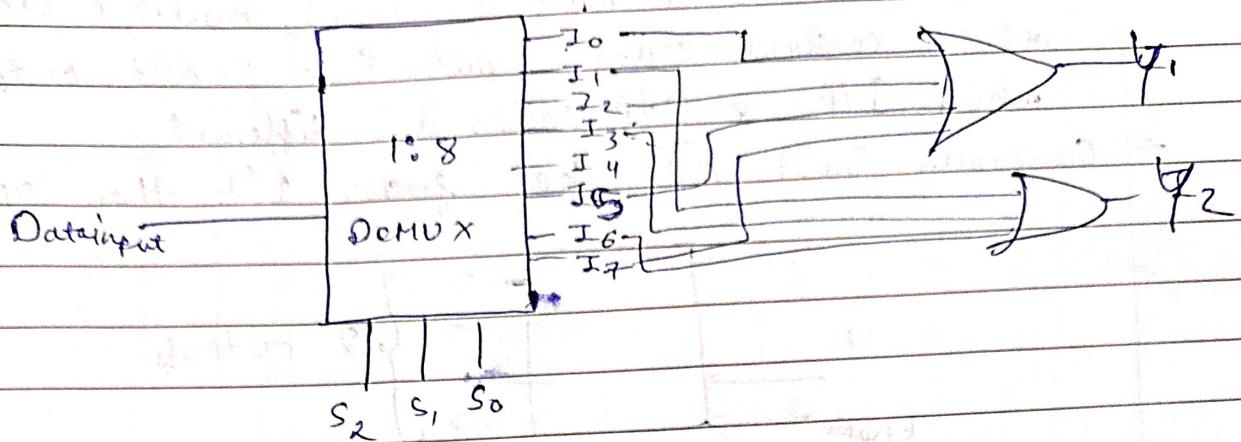
$$Y_1 = D \bar{S}_1 S_0$$

$$Y_2 = D S_1 \bar{S}_0$$

$$Y_3 = D S_1 S_0$$

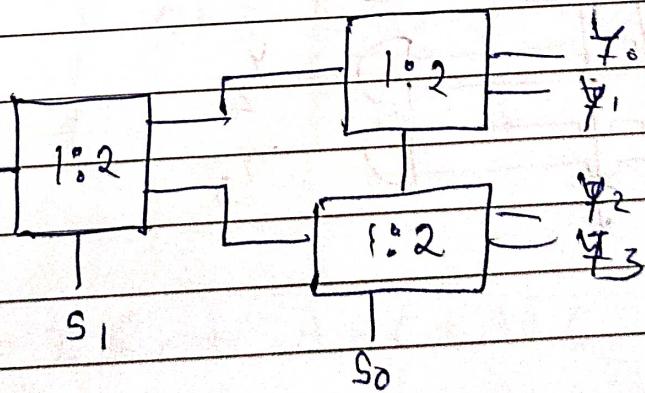


$$\text{Q) } f(A, B, C) = \sum m(0, 2, 5, 7) \quad f(ABC) = \sum m[1, 3, 6]$$



A	B	C	$\bar{Y}_1$	$\bar{Y}_2$
0	0	0	1	0
0	0	1	0	1
0	1	0	0.1	0
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

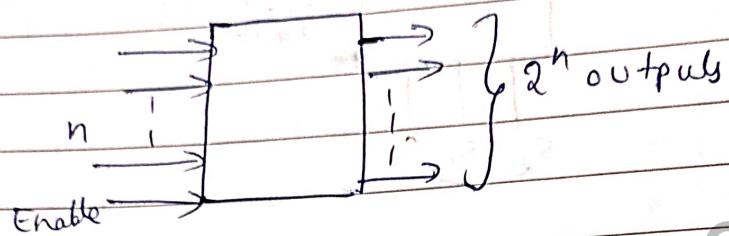
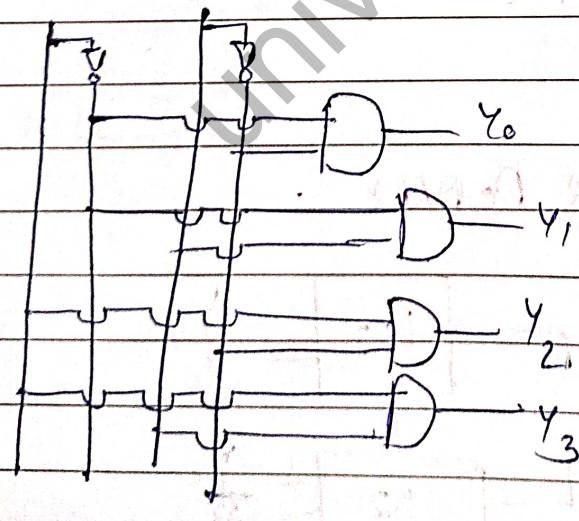
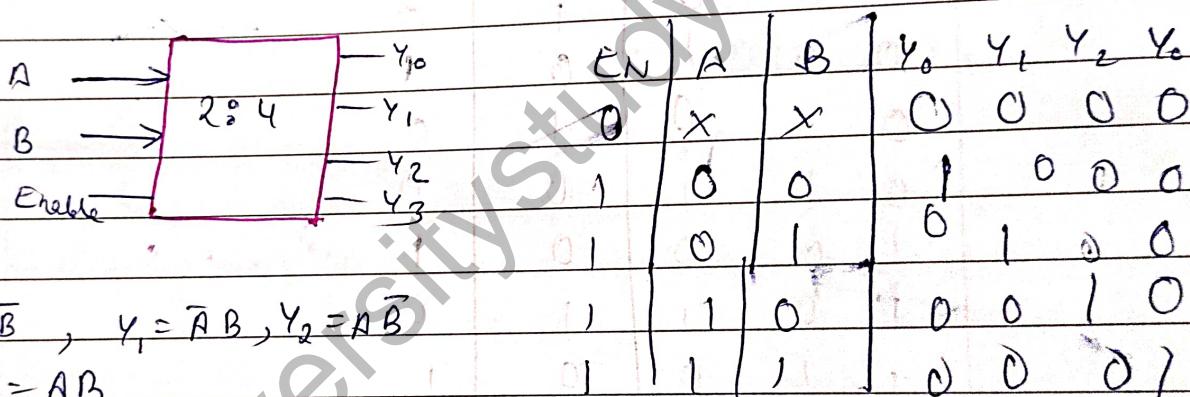
Q) 1:4 using 1:2 Demux



Decoder

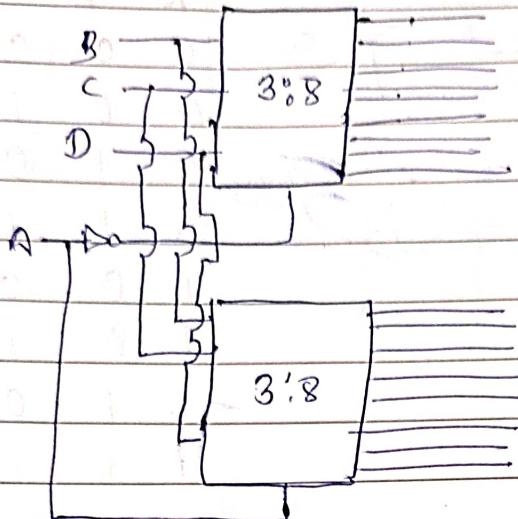
A decoder is a multiple input, multiple O/P circuit, which converts coded input into coded output where I/p & O/P codes are different.

→ Generally input code has fewer bits than output bits

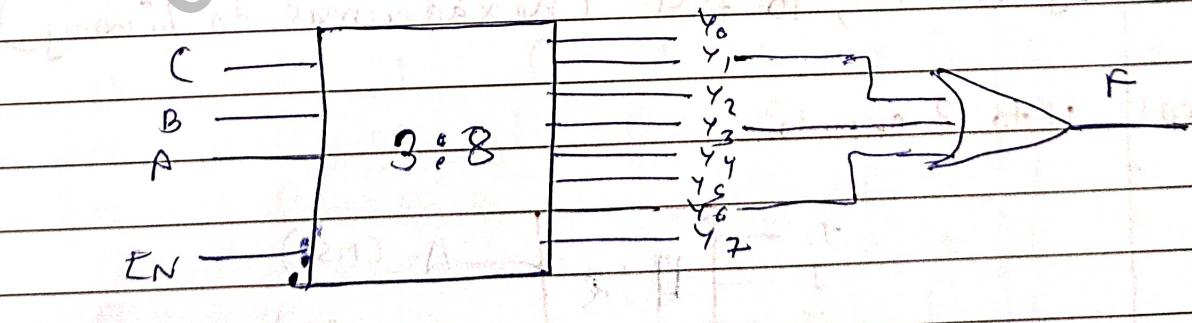
i) 2 to 4 ( $2:4$ ) Binary Decoder

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Q) 4 to 16 decoder using 3:8

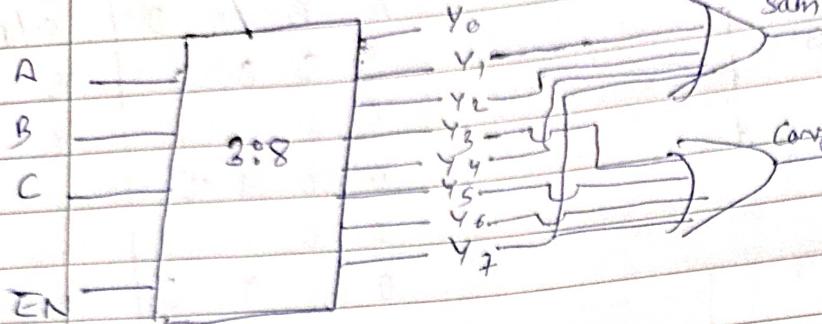


A	B	C	D	O/P
0	0	0	0	$y_0$
0	0	0	1	$y_1$
0	0	1	0	$y_2$
0	0	1	1	$y_3$
0	1	0	0	$y_4$
0	1	0	1	$y_5$
0	1	1	0	$y_6$
0	1	1	1	$y_7$
1	0	0	0	$y_8$
1	0	0	1	$y_9$
1	0	1	0	$y_{10}$
1	0	1	1	$y_{11}$
1	1	0	0	$y_{12}$
1	1	0	1	$y_{13}$
1	1	1	0	$y_{14}$
1	1	1	1	$y_{15}$

Q)  $F(A, B, C) = \sum m(1, 3, 6)$  using decoders

$$Y = \bar{A} \bar{B} C + \bar{A} B C + A \bar{B} C$$

## Q) Full adder using decoder



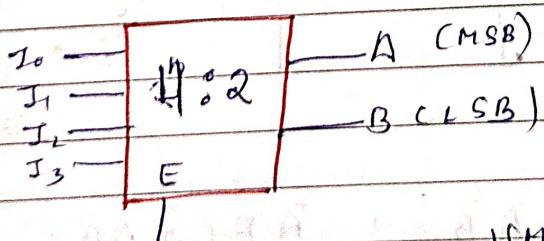
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

## Encoder

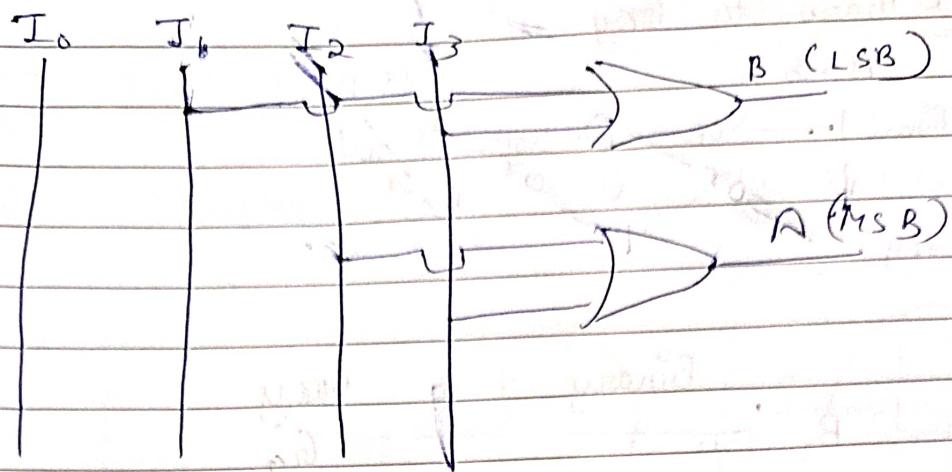
Digital circuit perform inverse operation of decoder.  
It has  $2^n$  input lines and n output lines  
O/P line generate binary code corresponding to I/P value.

- (1) If  $n=2$ , 4 to 2 encoder (Decimal to binary)
- (2) If  $n=3$ , 8 to 3 encoder (Octal to binary)
- (3) If  $n=4$ , 16 to 4 (Hexadecimal to binary)

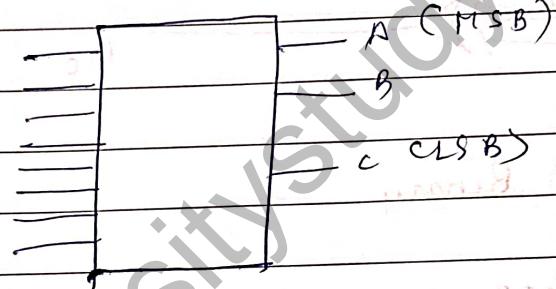
### ① 4 to 2 encoder



E	J <sub>0</sub>	J <sub>1</sub>	J <sub>2</sub>	J <sub>3</sub>	A (MSB)	B (LSB)
0	x	x	x	x	0	0
1	1	0	0	0	0	1
1	0	1	0	0	1	0
1	0	0	1	0	1	1
1	0	0	0	1	1	1

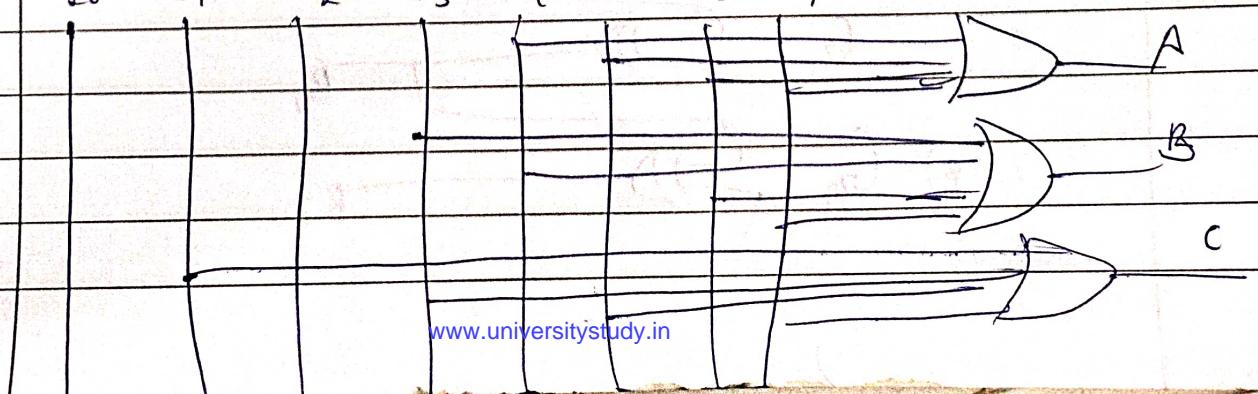


8 to 3 (1 bit)



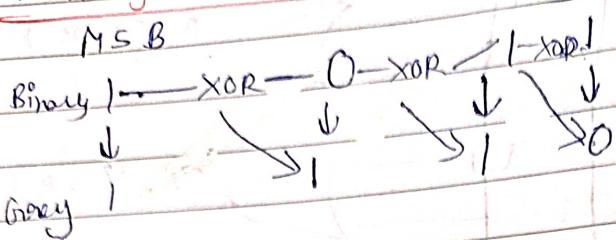
$J_0$	$J_1$	$J_2$	$J_3$	$J_4$	$J_5$	$J_6$	$J_7$	$A$	$B$	$C$
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
0	1	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$J_0 \quad J_1 \quad J_2 \quad J_3 \quad J_4 \quad J_5 \quad J_6 \quad J_7$



Binary to Gray

MSB



Gray

LSB

Binary

Gray

 $B_3$  $G_3$  $B_2$  $G_2$  $B_1$  $G_1$  $B_0$  $G_0$ Gray to Binary

MSB

LSB

Gray

Binary

Binary

Gray

Binary

MSB

Gray

 $B_3$ 

Gray

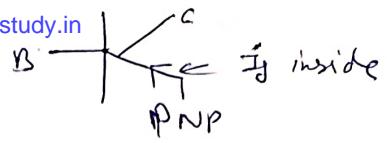
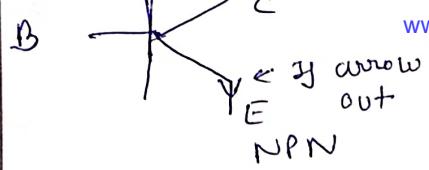
 $B_2$ 

Gray

 $B_1$ 

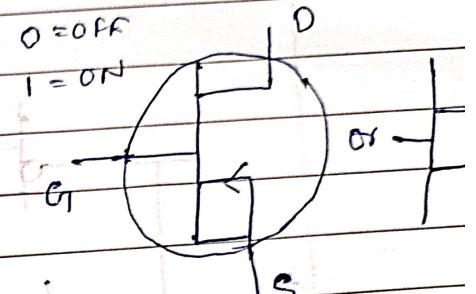
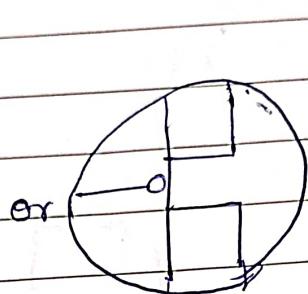
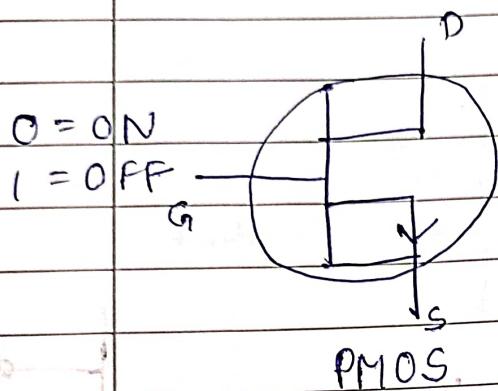
(LSB) Gray

 $B_0$

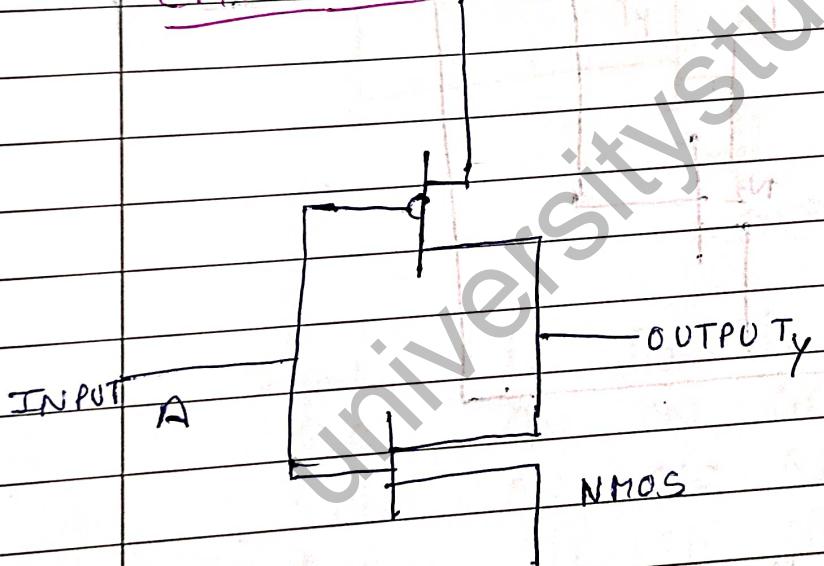


## CMOS LOGIC GATES

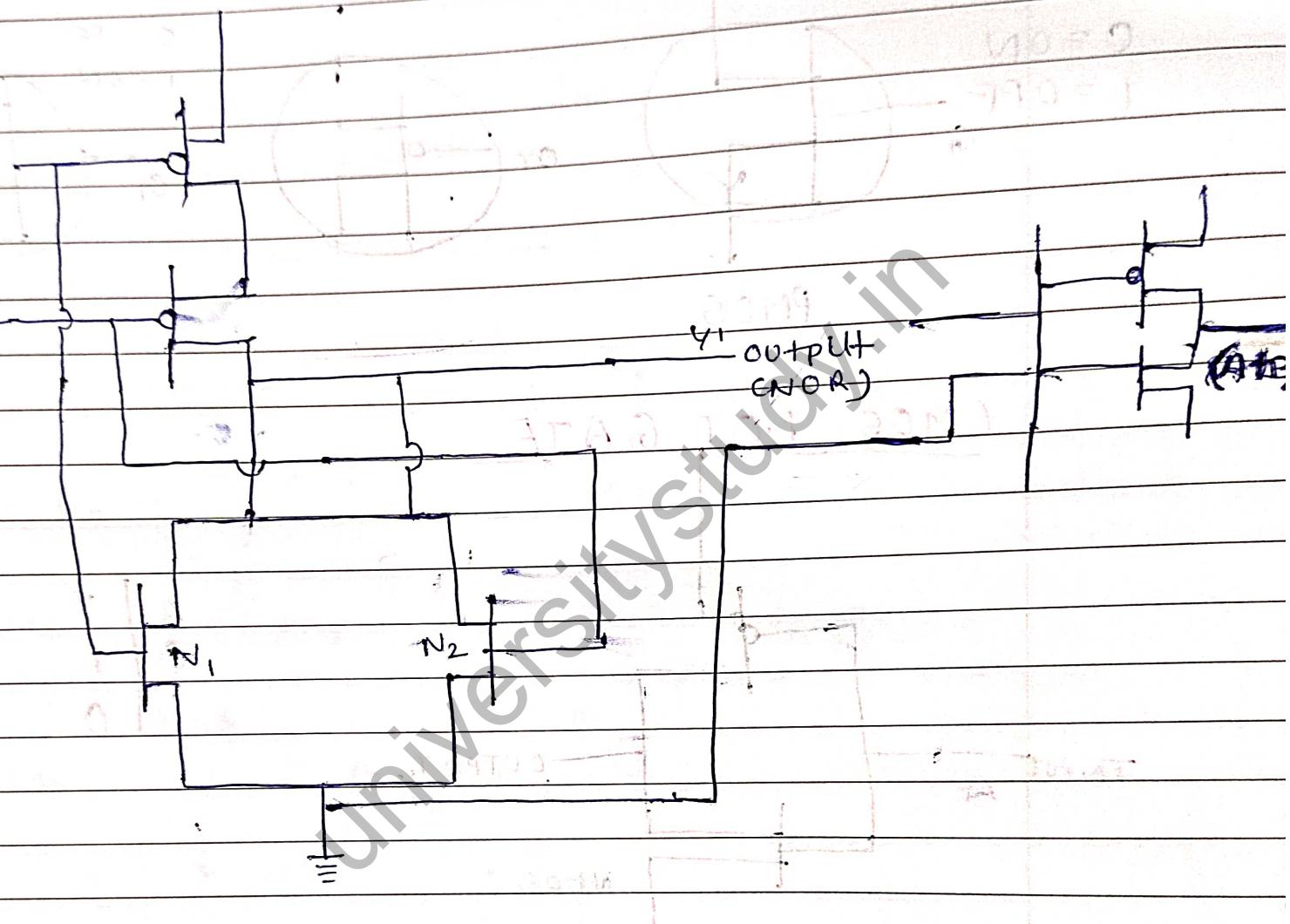
CMOS = Complementary Metal Oxide Semiconductor



## CMOS NOT GATE



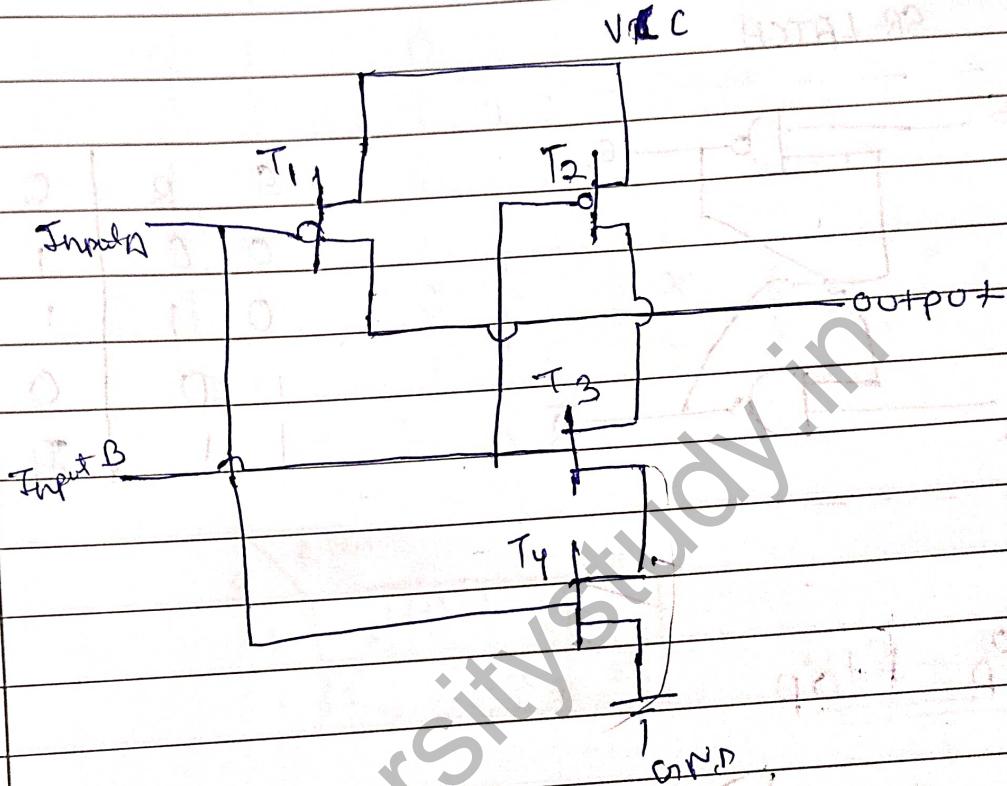
A	Y
0	1
1	0

OR GateP<sub>1</sub> & P<sub>2</sub> PMOS gate

A	B	$\gamma_1(A+B)$	$\gamma_2(A+B)$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

## CMOS NAND GATE

$T_1$  &  $T_2$  are p-channel MOSFET  
 $T_3$  &  $T_4$  are n-channel MOSFET



Input	$T_1$	$T_2$	$T_3$	$T_4$	OUTPUT
0, 0	ON	ON	OFF	OFF	1
0, 1	ON	OFF	ON	OFF	1
1, 0	OFF	ON	OFF	ON	1
1, 1	OFF	OFF	ON	ON	0

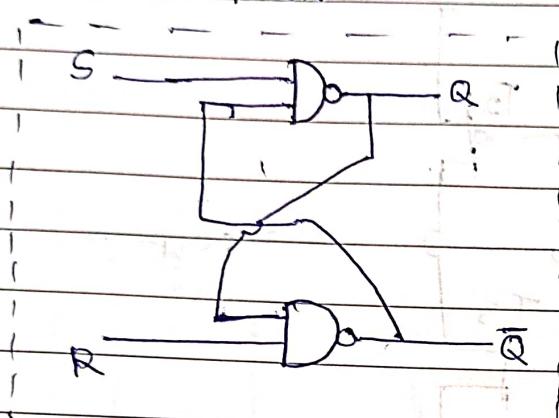
Combination circuit made up by logic gate  
on present input rather than previous output.

## Sequential Logic

If we add memory in combinational circuit it become sequential circuit.

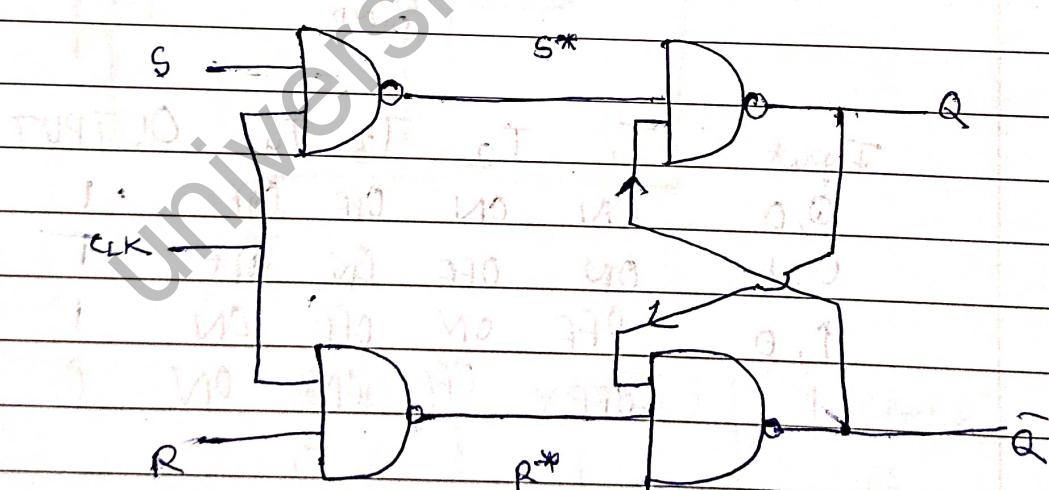
Depends on present and past input to generate any output.

SR LATCH



S	R	Q	$\bar{Q}$
0	0	1	0 (invalid)
0	1	0	1 (set)
1	0	0	1 (Reset)
1	1	0, then 1 (Memory)	1, then 0

## SR Flip Flop



Truth Table

CLK	S	R	Q	$\bar{Q}$
0	X	X	Memory	
1	0	0	Memory	
1	0	1	Reset	
1	1	0	Set	
1	1	1	Invalid	

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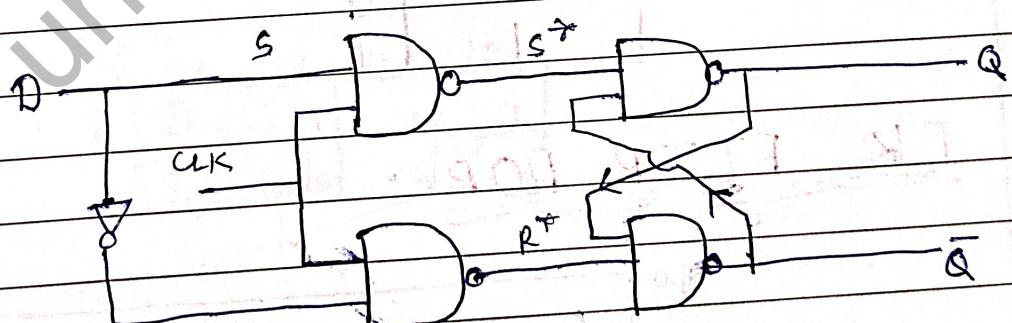
## Characteristic Table ( $CLK=1$ )

S	R	$Q_n$	$Q_{n+1}$	D
0	0	0	0	Memory
0	0	1	1	
0	1	0	0	Reset
0	1	1	1	
1	0	0	1	Set
1	0	1	1	
1	1	0	X	Invalid
1	1	1	X	

S	R	$Q_n$	00	01	11	10
0	0	0	1	1	0	0
1	1	1	1	1	X	X

$$Y = S + \bar{R} Q_n$$

## D-Flip-Flop



CLK	D	Q	$\bar{Q}$
0	X	Memory	
1	0	Reset	
1	1	Set	

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## Characteristic Table

D	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0
0	1	0
1	0	1
1	1	1

$Q_n$

0	0	1
1	1	1

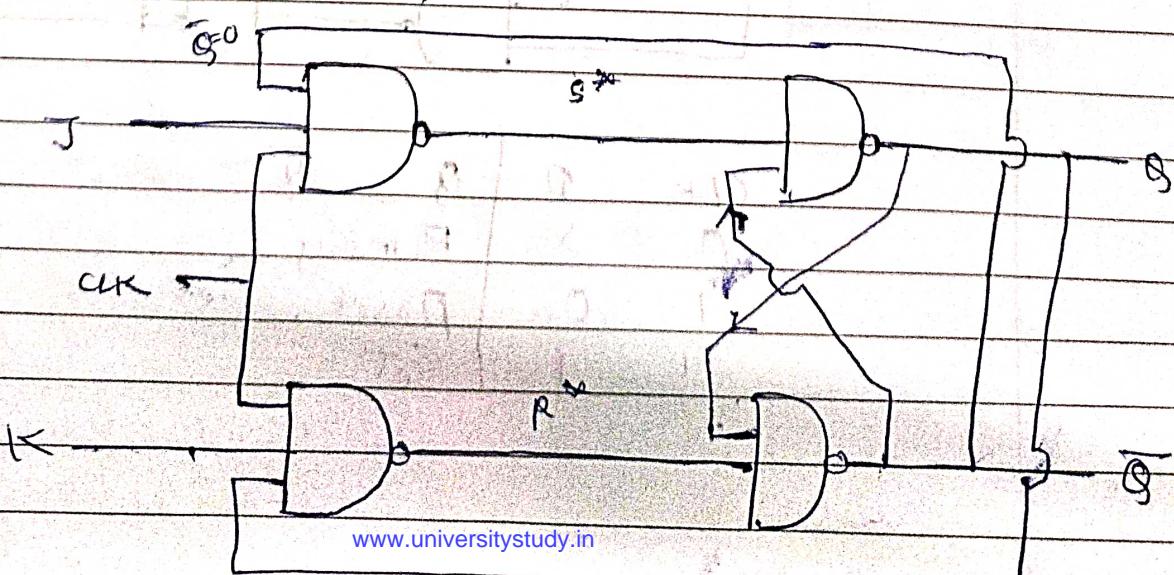
$\rightarrow D$

$$Q_{n+1} = D$$

## Excitation Table

$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0

## JK FLIP-FLOP



CLK	J	K		$\bar{Q}$	$\bar{Q}$
0	x	x		Memory	
1	0	0		Memory	
1	0	1		Reset	
1	1	0		Set	
1	1	1		Toggle	

### Characteristic Table

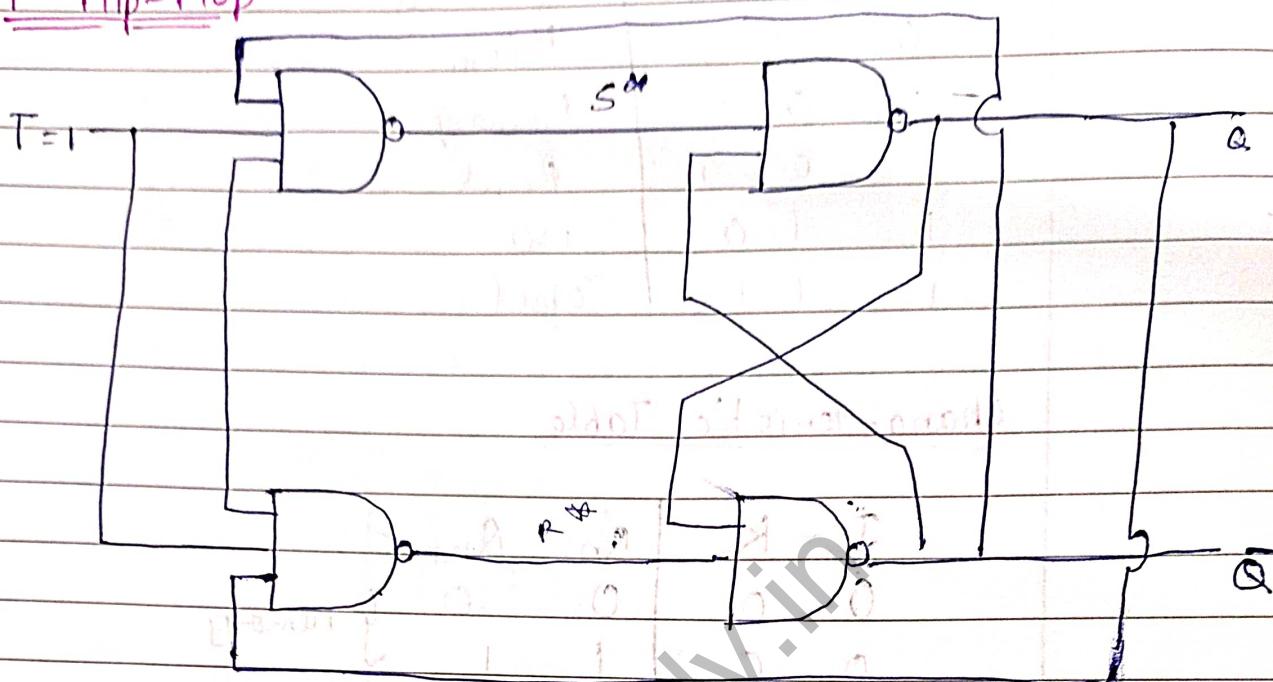
J	K	$Q_n$	$Q_{n+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J	K	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0	1
1	1	1	0

$$Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$

### Excitation table

	$Q_n$	$Q_{n+1}$	D	J	K
x	0	0	0	0	x
1	0	1	1	1	x
0	1	0	0	x	1
x	0	1	1	x	0

T Flip-Flop

CLK	T	Q	$\bar{Q}$
0	X	Memory	0
1	0	Memory	1
1	1	Toggled	1

Characteristic Table

T	Q <sub>n</sub>	Q <sub>n+1</sub>	Q <sub>n+2</sub>	Q <sub>n+3</sub>	Q <sub>n+4</sub>
0	0	0	1	1	0
0	1	1	0	0	1
1	0	1	0	1	0
1	1	0	1	0	1

Excitation Table

$Q_{in}$	$Q_{n+1}$	0	T	J	K	S	R
?	0	0	0	0	x	0	x
0	1	1	1	1	x	1	0
1	0	0	1	x	1	0	1
1	1	1	0	x	0	1	0

## Conversion of Flip-Flops

Write characteristic table of required table

Write excitation table of given table

K Map, K Map equation

Circuit diagram

### JK Flip-Flop to SR Flip-Flop

Characteristic table of SR

SR	Q <sub>n</sub>	Q <sub>n+1</sub>	② Excitation table J      K
00	0	0	0 X
01	0	1	0 X 0
10	1	0	0 0 X
11	1	1	0 X 1
00	0	0	0 0 1 X
01	0	1	X 0
10	1	0	X X
11	1	1	X X

### ③ K Map

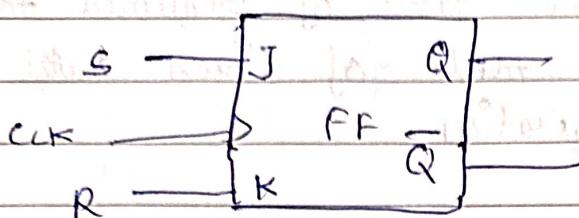
S	R <sub>n</sub>	00	01	11	10
0	0	X <sub>1</sub>	X <sub>3</sub>	X <sub>2</sub>	1
1	1	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$J = S$

S	R <sub>n</sub>	00	01	11	10
0	0	X <sub>0</sub>	1	X <sub>2</sub>	X <sub>3</sub>
1	1	X <sub>4</sub>	X <sub>5</sub>	X <sub>7</sub>	X <sub>6</sub>

$\Rightarrow K = R$

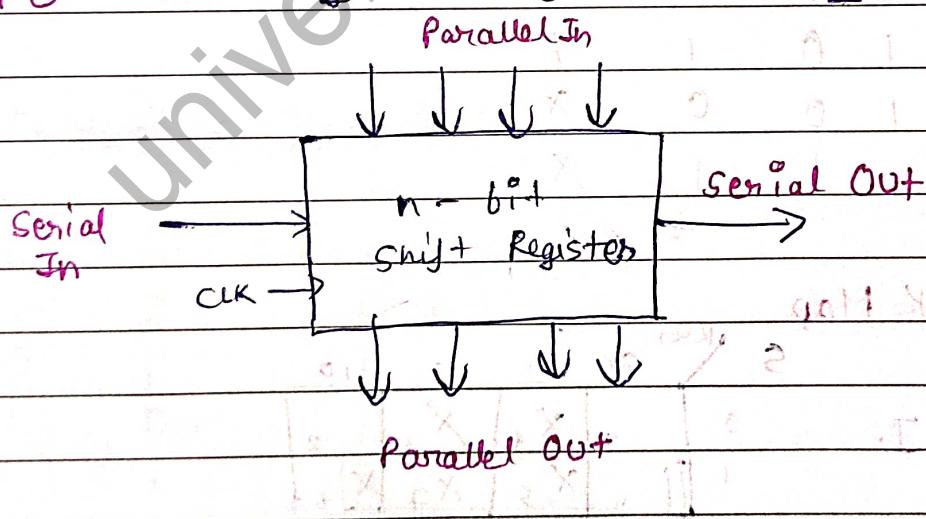
#### ④ Flip Flop diagram



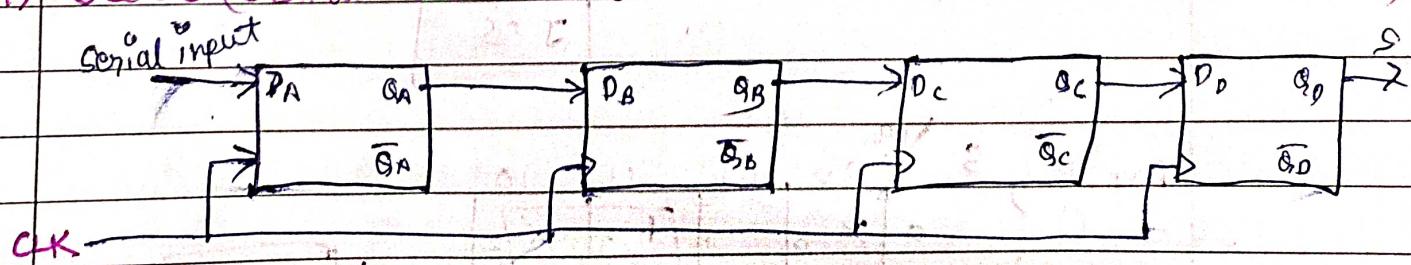
#### Registers

Register is grp of flip flops. N-bit Register consist of n number of flip-flops and it stores n-bit binary information.

	I/P	O/P	Total CLK
1) SISO	A	n-1	$2^n - 1$
2) SJPO	n	0	$2^n$
3) PJSB	1	n-1	$2^n$
4) PIPO	1	0	$2^n - 1$

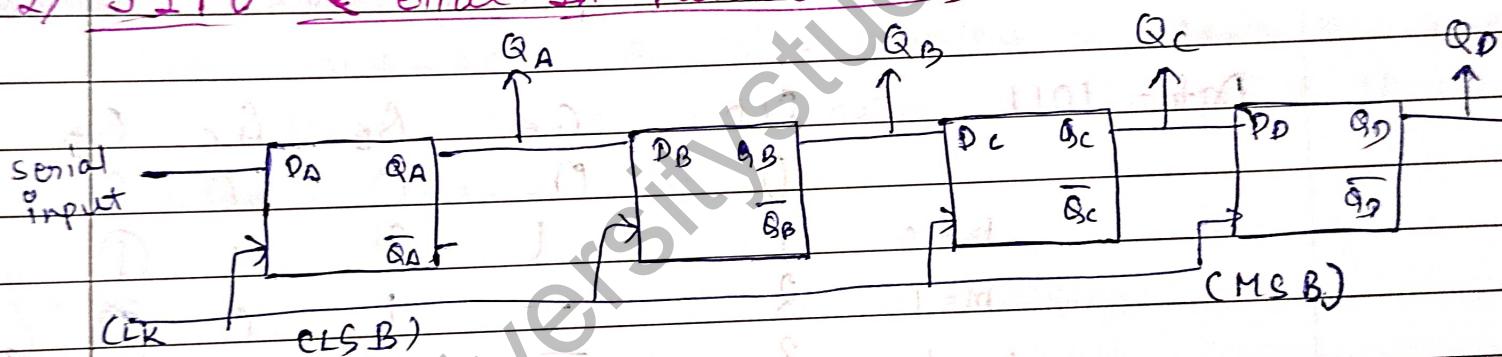


#### 1) SISO (Serial In Serial OUT) (First In First Out FIFO)



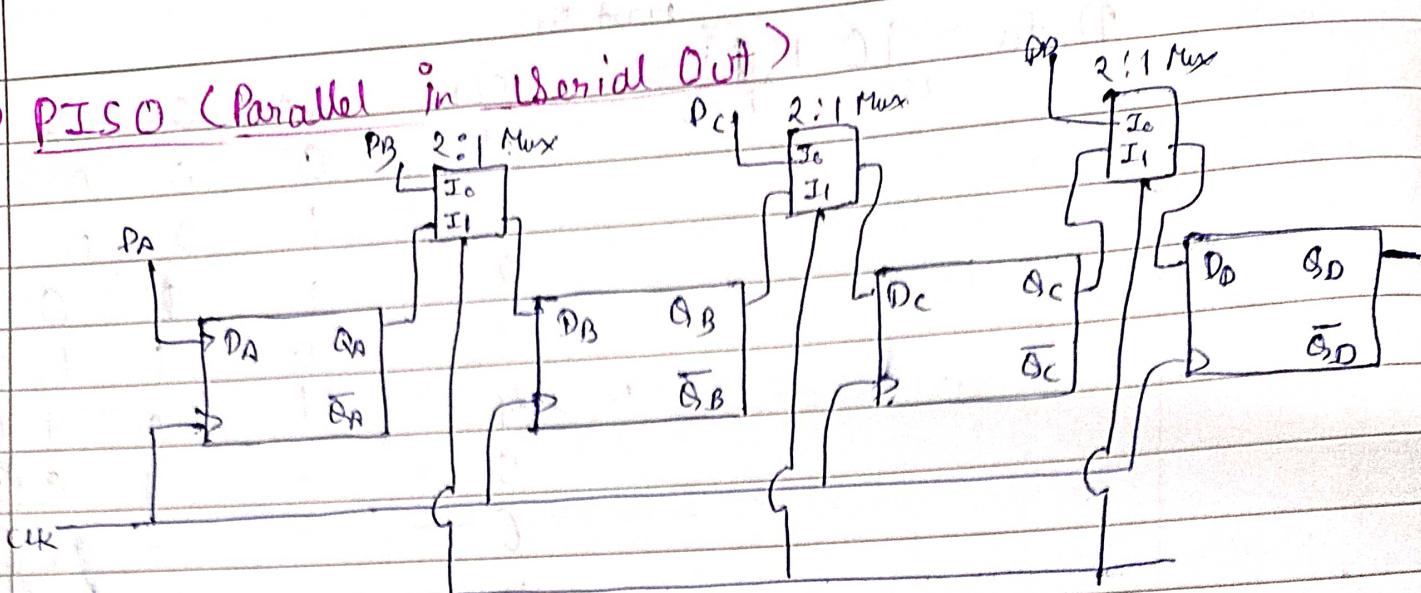
Data = 1010	LSB	MSB	First In	CLK	QA	QB	QC	QD
				0 <sup>th</sup>	0	0	0	0
				1	1	0	0	0
				2	1	0	0	0
				3	0	1	1	0
				4	1	0	1	0
				5	-	1	0	1
				6	-	-	1	0
				7	-	-	-	1

## 2) SIPO (Serial In Parallel Out)



Data = 1010	First in	CLK	QA	QB	QC	QD
		0	0	0	0	0
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
		0	0	1	0	0
		1	1	0	1	0
		0	0	0	0	1
		1	1	1	0	1
		0	0	1	1	0
		1	1	0	1	1
		0	0	0	0	1
		1	1	1	0	0
	</td					

### 3) PIPO (Parallel in Serial Out)



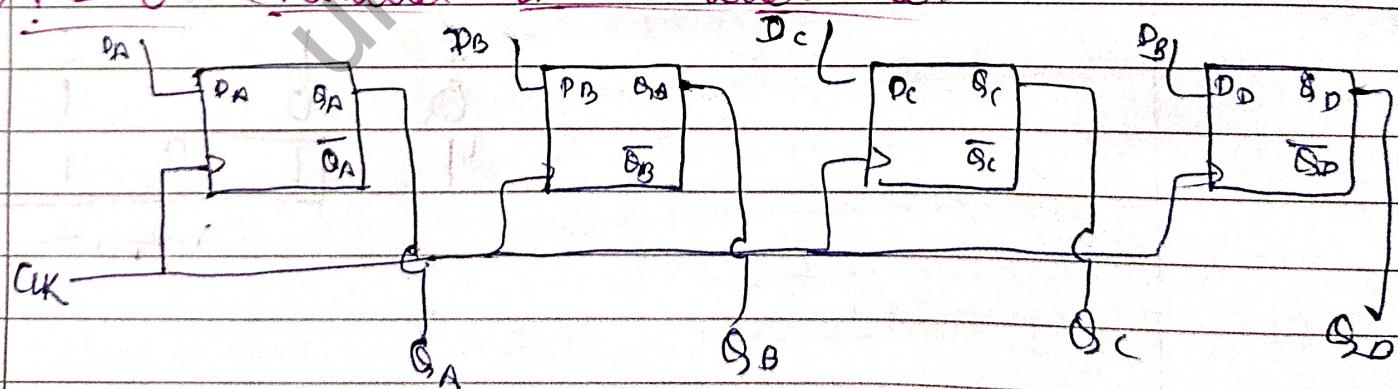
Mode control(m)

When  $m=0$  it perform parallel operation

When  $m=1$  it perform serial operation

	CLK	QA	QB	QC	QD
	0	0	0	0	0
$m=0$	1	1	0	1	1
$m=1$	2	-	-	1	0
$m=1$	3	-	-	-	1
$m=1$	4	-	-	-	1

### 4) PIPO (Parallel in Parallel Out)



CLK	QA	QB	QC	QD
0 <sup>th</sup>	0	0	0	0
1	1	0	1	1

## Counter

- 1) Asynchronous
- 2) Synchronous

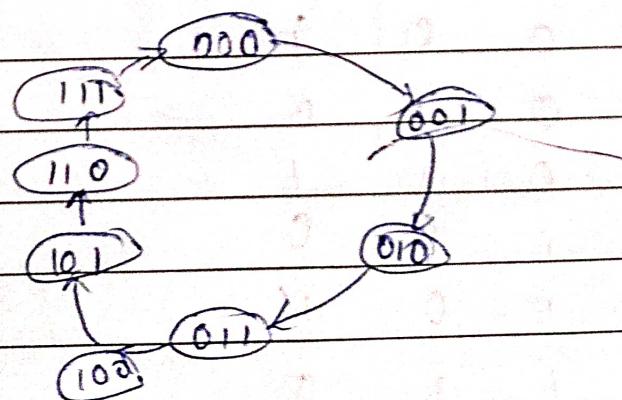
### Asynchronous (Ripple) Counter

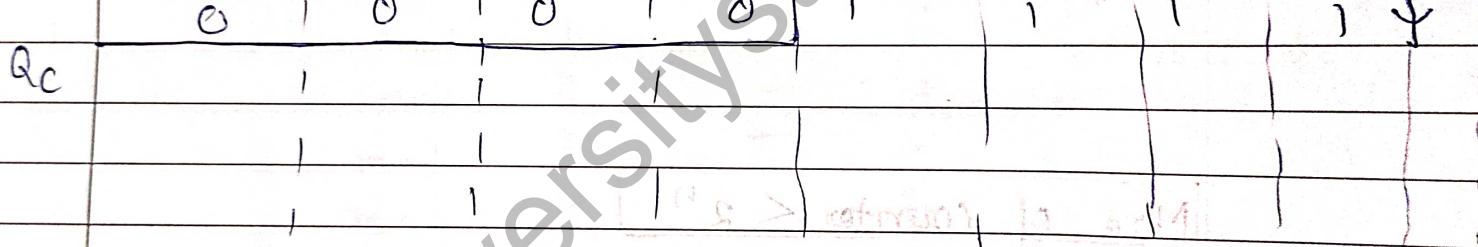
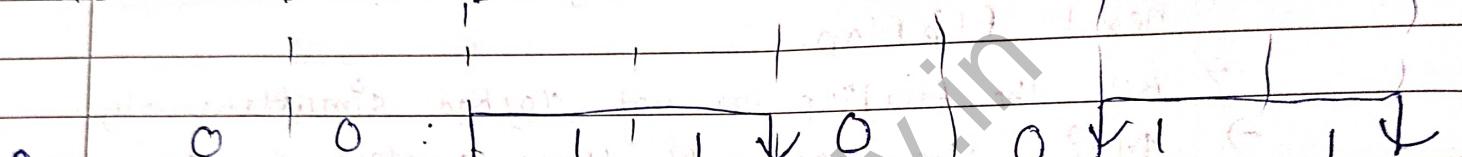
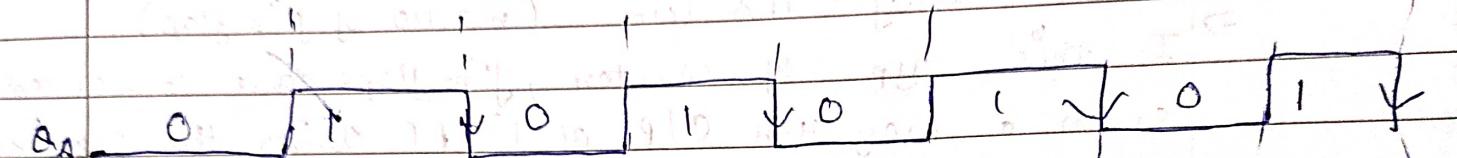
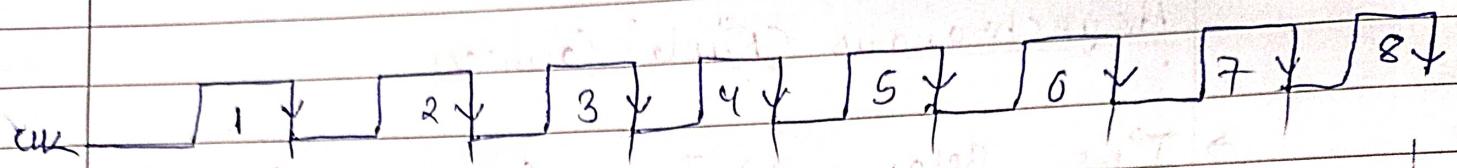
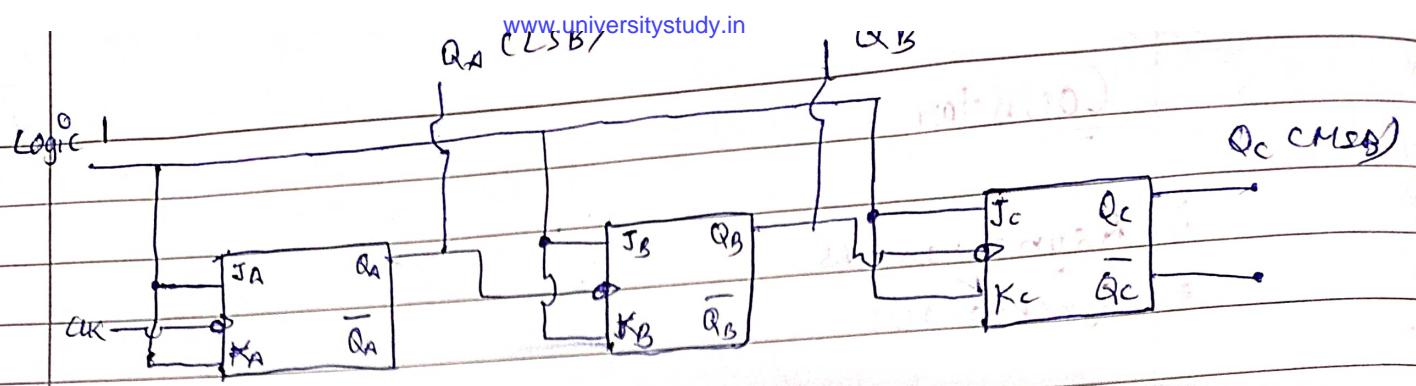
- Time delay =  $n \times T_{clk}$  ( $n = \text{no. of flip flop}$ )
- In this type of counter, flip-flops are connected in such a way that Q<sup>0</sup> of 1<sup>st</sup> FF drives the CLK for the next flip flop.
- All the flip flop are not clocked simultaneously.
- Main drawback of these counters is their low speed as the CLK is propagated through no. of FF before it reaches last FF.

Mod of Counter  $< 2^n$

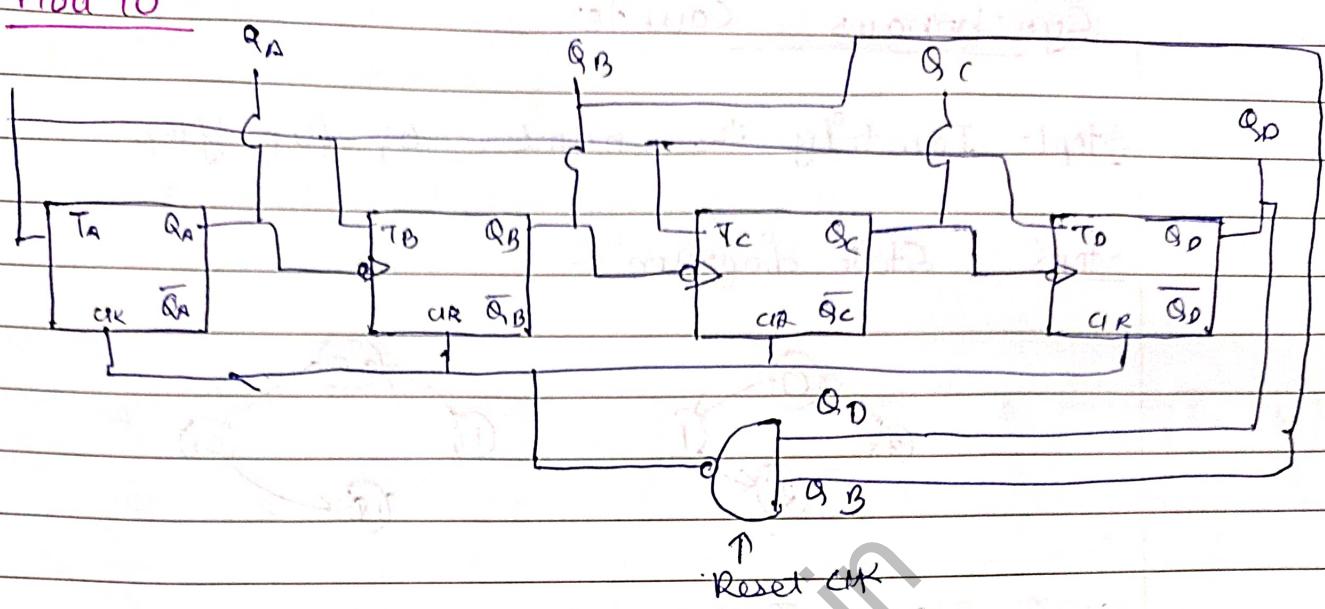
- 1) 3-bit Asynchronous up counter

State diagram





CK	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	0	0	0	1	1	1
1	0	0	0	1	1	1
2	0	0	1	1	1	0
3	0	1	0	1	0	1
4	0	1	1	0	0	0
5	1	0	0	0	1	1
6	1	0	1	0	1	0
7	1	1	0	0	0	1
8	1	1	1	0	0	0
9	1	1	1	0	0	0

Mod 10

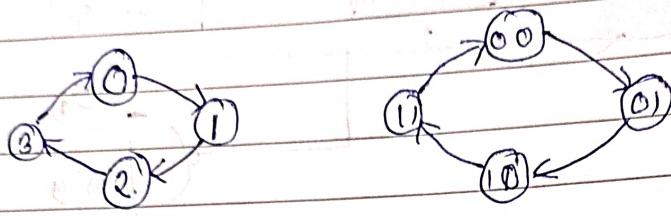
CK	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0 <sup>th</sup>	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

had to be zero

## Synchronous Counter

Step 1 - Identify the number of flip flop

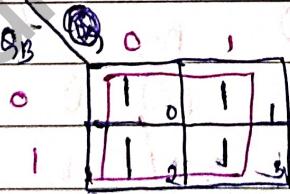
Step 2 - State diagram



Step 3 - State Table

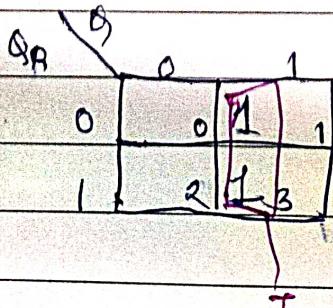
Present State (MSB) (LSB)	$Q_B$	$Q_A$	$Q_B+1$	$Q_A+1$	$T_B$	$T_A$
0 0	0	0	0	0	0	1
0 1	0	1	0	1	1	1
1 0	1	0	1	1	0	1
1 1	1	1	0	0	1	0

Kmap  $T_A$



$$T_A = 1$$

Kmap  $T_B$



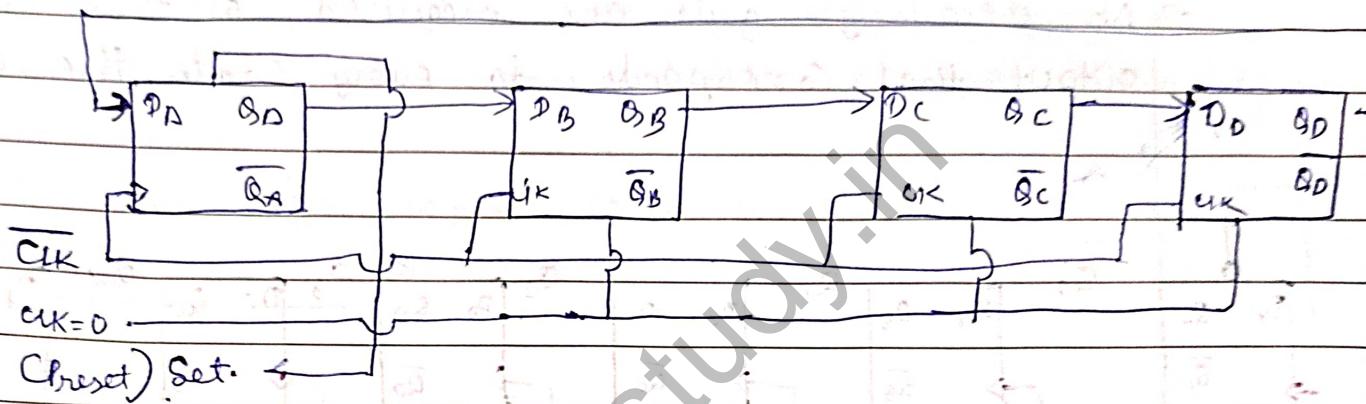
$$T_B = Q_A$$

11

Johnson Counter (made up by shift register)  
 Used in different pattern generation

No. of bits = no. of FF =  $n$

Total n states =  $2^n$



CLK       $Q_0 \quad Q_1 \quad Q_2 \quad Q_3$

0            0 0 0 0

1            1 0 0 0

2            1 1 0 0

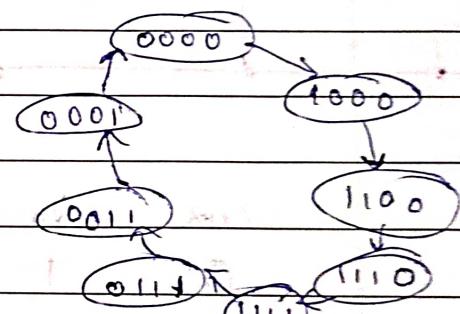
3            1 1 1 0

4            1 1 1 1

5            0 1 0 1

6            0 0 1 1

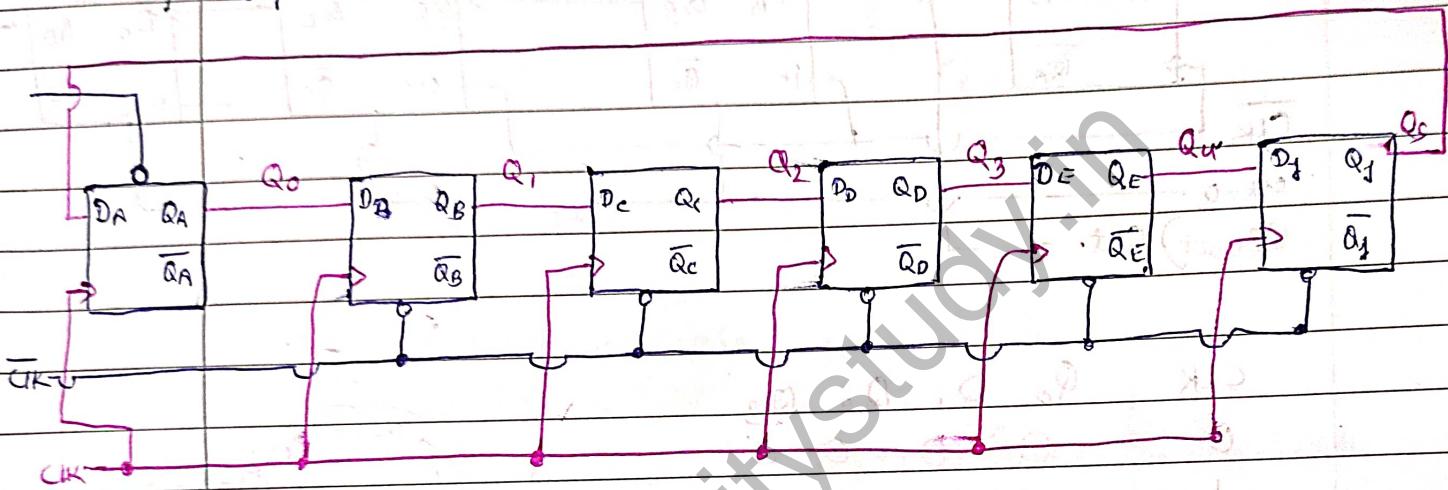
7            0 0 0 1



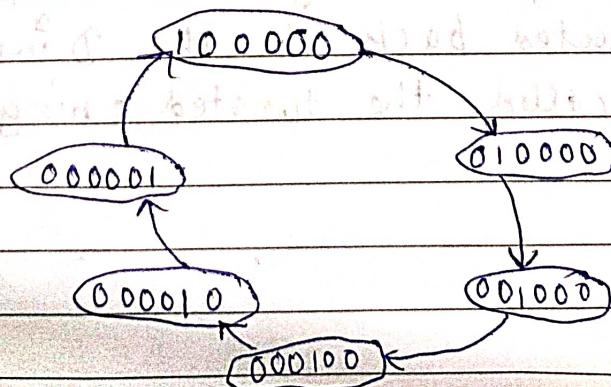
The complement of the output of the last stage is connected back to the  $D$  input of the first stage. It is called the twisted-ring counter.

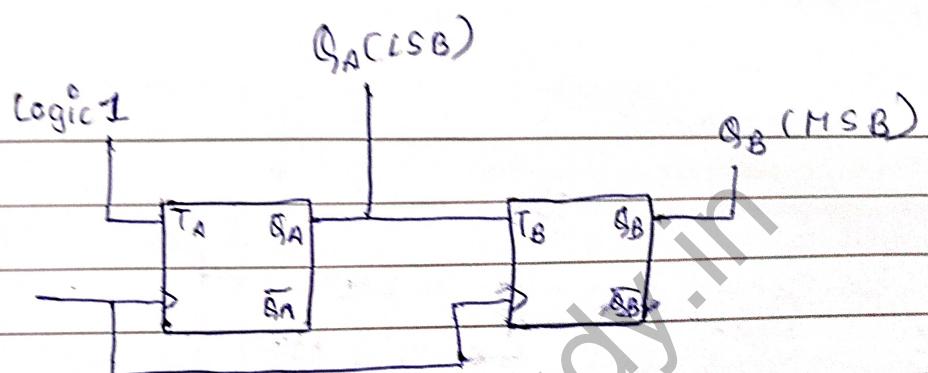
## Ring Counter

- The output of the last stage is connected to the D input of the first stage.
- An n-bit ring counter cycles through  $n$  states.
- No decoding gates are required, as there is an output that corresponds to every state the counter is in.



Clock	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>out</sub>	Q <sub>s</sub>
0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	1
2	0	0	1	0	1	0	0
3	0	0	0	1	0	0	1
4	0	0	0	0	1	0	0
5	0	0	0	0	0	1	1





- All the Flip Flop are clocked simultaneously.
- Design involves complex logic circuits as no of states increases.
- They are high speed counter.