Q1: Set and Reset, both are disabled in case of SR flip-flop then output is...

Options:
(a) Reset
(b) Set
(c) Previous output
(d) Pre-input

Answer: **(c) Previous output**
Explanation:
In an SR flip-flop, if both Set and Reset inputs are disabled (i.e., both are 0), the flip-flop maintains its previous state. T

Q2: Each stage of a Shift register is capable of storing...

Options:
(a) 1 bit
(b) 1 byte
(c) 2 bits
(d) 1 nibble

Answer: **(a) 1 bit**
Explanation:
A shift register is a sequential circuit where each flip-flop stores a single bit of data. Multiple stages are combined for s

Q3: Synchronous counter is also called...

Options:
(a) Asynchronous counter
(b) Parallel counter
(c) Trip counter
(d) Ripple counter

Answer: **(b) Parallel counter**
Explanation:
In a synchronous counter, all flip-flops are triggered simultaneously using the same clock signal. This is why it is also r

Q4: Identify the basic building block of shift registers.

Options:
(a) T flip-flop
(b) SR flip-flop
(c) JK flip-flop
(d) D flip-flop

Answer: **(d) D flip-flop**
Explanation:
D flip-flops are used in shift registers as they are ideal for data storage and transfer. The "D" stands for "Data," and the

Q5: Shift counter is also known as...

Options:
(a) Johnson counter
(b) Ripple counter
(c) Synchronous counter
(d) Asynchronous counter

Answer: **(a) Johnson counter**
Explanation:
A shift counter can be implemented as a **Johnson counter**, where the output of the last flip-flop is inverted and fed ba

Q6: The arrow direction in the diode symbol indicates...

Options:
(a) Direction of electron flow
(b) Direction of hole flow (conventional current)
(c) Opposite to the direction of hole flow
(d) None of the above

Answer: **(b) Direction of hole flow (conventional current)**
Explanation:
The arrow in the diode symbol indicates the **direction of conventional current flow** (from the anode to the cathode) a

Q7: A semiconductor is formed by... bonds.

Options:
(a) Covalent

(b) Electrovalent
(c) Co-ordinate
(d) None of the above

Answer: **(a) Covalent**
Explanation:
In a semiconductor, atoms are held together by **covalent bonds**. These bonds are formed by sharing electrons betwee

Q8: A semiconductor has... temperature coefficient of resistance.

Options:
(a) Positive
(b) Zero
(c) Negative
(d) None of the above

Answer: **(c) Negative**
Explanation:
In semiconductors, as temperature increases, resistance decreases. This is because more charge carriers are genera

Q9: Which region is heavily doped in case of BJT?

Options:
(a) Collector
(b) Base
(c) Emitter
(d) Gate

Answer: **(c) Emitter**
Explanation:
In a Bipolar Junction Transistor (BJT), the **emitter** is heavily doped to supply a large number of charge carriers, enablin

Q10: A ideal diode under reverse biased condition operates as .....

Options:
(a) Either open switch or closed switch
(b) Closed switch
(c) Open switch
(d) None of these

Answer: **(c) Open switch**
Explanation:
In reverse bias, a diode blocks current flow, behaving like an **open switch**, except for a small leakage current.

Q11: A ideal diode under forward bias condition operates as

Options:
(a) Either open switch or closed switch
(b) Closed switch
(c) Open switch
(d) None of these

Answer: **(b) Closed switch**
Explanation:
Under forward bias, a diode allows current to flow, functioning like a **closed switch** after surpassing the forward voltag

Q12: Enhancement mode is present in...

Options:
(a) MOSFET
(b) JFET
(c) Tunnel diode
(d) Pn junction diode

Answer: **(a) MOSFET**
Explanation:
Enhancement mode is a characteristic of **MOSFETs** where the device is initially off, and a positive gate voltage is need

Q13: The concept of virtual ground is applicable in...

Options:
(a) BJT
(b) MOSFET
(c) Diode
(d) Operational amplifier

Answer: **(d) Operational amplifier**

Explanation:
The concept of **virtual ground** is used in operational amplifiers, especially in inverting configurations, where the invert

Q14: MOSFET acts as an amplifier in...

Options:
(a) Cutoff region
(b) Active region
(c) Saturation region
(d) None of these

Answer: **(b) Active region**
Explanation:
A MOSFET amplifies signals when operating in the **active region**, where the drain current depends on the gate-source

Q15: BJT acts as an amplifier in...

Options:
(a) Cutoff region
(b) Active region
(c) Saturation region
(d) None of these

Answer: **(b) Active region**
Explanation:
A **BJT** operates as an amplifier in the active region, where the collector current is proportional to the base current.

Q16: A XOR B is equivalent to...

Options:
(a) A NOR B
(b) A XNOR B
(c) A OR B
(d) None of these

Answer: **(d) None of these**
Explanation:
The XOR operation is **A XOR B = (A'B + AB')**, which is not equivalent to NOR, XNOR, or OR.

Q17: A XOR B, XOR C is equivalent to...

Options:
(a) Complement of (A XOR B)
(b) A OR C
(c) A NOR C
(d) None of these

Answer: **(a) Complement of (A XOR B)**
Explanation:
The XNOR operation is the complement of XOR. Hence, **A XOR B, XNOR C** is equivalent to the complement of A⊕BA \(

Q18: The BJT acts as a closed switch in....

Options:
(a) Linear region
(b) Saturation region
(c) Cutoff region
(d) None of these

Answer: **(a) Linear region**
Explanation:
In forward bias (closed switch), the diode operates in the **linear region**, allowing current to flow with a relatively const

Q11: XOR gate is also called...

Options:
(a) Inverter
(b) Amplifier
(c) Comparator
(d) BCD

Answer: **(c) Comparator**
Explanation:
The XOR gate compares two binary inputs and outputs a 1 if the inputs are different. This behavior is similar to that of a

Q12: The number of inputs in case of Half adder are...

Options:
(a) 1
(b) 2
(c) 3
(d) 4

Answer: **(b) 2**
Explanation:
A **half adder** takes two inputs (A and B) and produces two outputs: the sum and the carry.

Q13: Carry is obtained in case of...

Options:
(a) Subtraction
(b) Addition
(c) Multiplication
(d) Both addition and subtraction

Answer: **(b) Addition**
Explanation:
A carry is generated in **addition** when the sum of two binary digits exceeds 1.

Q14: The binary addition of 1 + 1 = ?

Options:
(a) Sum = 1, Carry = 1
(b) Sum = 0, Carry = 0
(c) Sum = 1, Carry = 0
(d) Sum = 0, Carry = 1

Answer: **(d) Sum = 0, Carry = 1**
Explanation:
In binary addition, 1+11 + 1 results in a sum of **0** and a carry of **1**.

Q15: Number of AND gates required for a 1 to 8 Mux

Options:
(a) 2
(b) 6
(c) 8
(d) 10

Answer: **(c) 8**
Explanation:
A 1-to-8 multiplexer requires **8 AND gates** for 8 input combinations.

Q16: 1 to 8 Demux requires ___ select lines.

Options:
(a) 2
(b) 3
(c) 4
(d) 5

Answer: **(b) 3**
Explanation:
For a 1-to-8 demultiplexer, 2n=82^n = 8, so n=3n = 3. Hence, 3 select lines are required.

Q17: ___ NOT gates will be required for 4 to 1 MUX.

Options:
(a) 3
(b) 1
(c) 2
(d) 4

Answer: **(c) 2**
Explanation:
A **4-to-1 multiplexer** requires 2 NOT gates to complement the select inputs for decoding.

Q18: Identify the building blocks for Encoder.

Options:
(a) OR gate
(b) AND gate
(c) XOR gate
(d) NOR gate

Answer: **(a) OR gate**
Explanation:
An **encoder** uses **OR gates** to encode multiple input signals into a smaller number of outputs.

Q19: Identify the type of circuit for Decoder.

Options:
(a) Logical circuit
(b) Sequential circuit
(c) Combinational circuit
(d) None of the mentioned

Answer: **(c) Combinational circuit**
Explanation:
A **decoder** is a combinational circuit that converts binary data into a specific output pattern.

Q20: TTL stands for...

Options:
(a) Transistor-complementary transistor logic
(b) Transistor-complemented transistor logic
(c) Transistor-capacitor transistor logic
(d) Transistor-coupled transistor logic

Answer: **(d) Transistor-coupled transistor logic**
Explanation:
TTL stands for **Transistor-Transistor Logic**, where bipolar junction transistors (BJTs) perform both logic and amplificat

Q21: D flip-flop is also known as ___ flip-flop.

Options:
(a) Transparent

(b) TTL
(c) Non-transparent
(d) None of these

Answer: **(a) Transparent**
Explanation:
A **D flip-flop** is sometimes called a **transparent flip-flop** because the output directly follows the input when the clock

Q22: T flip-flop is known as ___ flip-flop.

Options:
(a) Toggle
(b) Transparent
(c) Set-Reset flip-flop
(d) None of these

Answer: **(a) Toggle**
Explanation:
A **T flip-flop** toggles its state on each clock pulse when the T input is high.

Q23: The output of JK flip-flop when J=1, K=1, and present state output=1 is...

Options:
(a) Reset to 0
(b) Both 1 and 0
(c) Toggle
(d) None of these

Answer: **(c) Toggle**
Explanation:
When J=1 and K=1, the **JK flip-flop toggles**, meaning it inverts the present state.

Q24: The output of SR flip-flop when S=1, R=1, and present state output=1 is...

Options:
(a) Invalid State
(b) Memory State
(c) Toggle State

(d) Race Around Condition

Answer: **(a) Invalid State**
Explanation:
In an **SR flip-flop**, when both S=1 and R=1, the state is **invalid** because it creates ambiguity.

Q25: The race around condition is related with...

Options:
(a) SR flip-flop
(b) JK flip-flop
(c) D flip-flop
(d) T flip-flop

Answer: **(b) JK flip-flop**
Explanation:
Race around condition occurs in JK flip-flops when both J=1 and K=1, and the clock pulse width is greater than the pr

Q19: A decoder converts inputs to...

Answer: **Outputs**
Explanation:
A **decoder** takes an nn-bit input and produces 2n2^n unique outputs, where each input corresponds to one active out

Q20: Latch output will stay set or reset until...

Options:
(a) Any pulse is given to go into a previous state
(b) They don't get any pulse anymore
(c) The trigger pulse is given to change the state
(d) The pulse is edge-triggered

Answer: **(c) The trigger pulse is given to change the state**
Explanation:
A latch remains in its current state (set or reset) until a **trigger pulse** changes its state. This makes it different from a fl

Q21: Which of the following conditions is true for an active region of BJT?

Options:
(a) Base-Emitter junction is reverse biased, and Collector-Base junction is forward biased.
(b) Base-Emitter junction is forward biased, and Collector-Base junction is forward biased.
(c) Base-Emitter junction is reverse biased, and Collector-Base junction is reverse biased.
(d) Base-Emitter junction is forward biased, and Collector-Base junction is reverse biased.

Answer: **(d) Base-Emitter junction is forward biased, and Collector-Base junction is reverse biased**
Explanation:
In the **active region**, the **Base-Emitter junction** is forward biased (allows current flow), while the **Collector-Base junc**

Q22: The Arduino UNO board has...

Options:
(a) 5 output analog pins
(b) 5 input analog pins
(c) 10 output digital pins
(d) 6 input analog pins

Answer: **(d) 6 input analog pins**
Explanation:
The Arduino UNO board has **6 analog input pins (A0 to A5)** and **14 digital input/output pins (D0 to D13)**.

Q23: The minimum number of 2-to-1 multiplexers required to realize a 4-to-1 multiplexer is...

Options:
(a) 1
(b) 2
(c) 3
(d) 4

Answer: **(c) 3**
Explanation:
A **4-to-1 multiplexer** can be implemented using **3 two-to-one multiplexers**. Two multiplexers are used to handle the 4

Q24: Binary representation of the decimal digit 42 is...

Options:
(a) 110110
(b) 101010
(c) 100100
(d) 111100

Answer: **(b) 101010**
Explanation:
Decimal 42 in binary is **101010**.

Q25: The octal equivalent of the decimal number 41710417_{10} is...

Options:
(a) 6418641_8
(b) 6198619_8
(c) 6408640_8
(d) 5968596_8

Answer: **(a) 6418641_8**
Explanation:
Convert 41710417_{10} to octal: 417÷8=52417 \div 8 = 52 remainder 11, then 52÷8=652 \div 8 = 6 remainder 44. Hen

Q26: The output of latches will remain set/reset until...

Options:
(a) Any pulse is given to go into a previous state.
(b) They don't get any pulse anymore.
(c) The trigger pulse is given to change the state.
(d) The pulse is edge-triggered.

Answer: **(c) The trigger pulse is given to change the state**
Explanation:
Similar to Q20, latches retain their output until a trigger pulse modifies the state.

Q27: The addition of a pentavalent impurity to a semiconductor creates...

Options:

(a) Valence electrons
(b) Free electrons
(c) Bound electrons
(d) Holes

Answer: **(b) Free electrons**
Explanation:
Adding a **pentavalent impurity** (e.g., phosphorus) to a semiconductor introduces **free electrons**, making it an nn-type

Q28: In a D-Flip Flop, if the clock input is high and D=1, the output (Q) will be...

Options:
(a) 0
(b) 1
(c) Toggle
(d) None of these

Answer: **(b) 1**
Explanation:
The output QQ of a **D flip-flop** directly follows the input DD when the clock is high. Hence, D=1D=1 results in Q=1Q=1.

Q29: The D flip-flop is useful as...

Options:
(a) Delay switch
(b) Divider
(c) Differentiator
(d) All the options

Answer: **(a) Delay switch**
Explanation:
A **D flip-flop** is commonly used as a **delay switch** to store and delay the input signal by one clock cycle.

Q1: Gray code for binary number 0101 is:

(a) 1100
(b) 0101
(c) 0111

(d) 0011

Answer: (d) **0011**
Explanation:
Gray code is a binary numeral system where two successive values differ in only one bit. To convert binary to Gray cod

1. The first bit remains the same.
2. Each subsequent bit is obtained by XORing the current binary bit with the previous binary bit.

For 0101:

First bit = 0.
Second bit = 0 XOR 1 = 1.
Third bit = 1 XOR 0 = 1.
Fourth bit = 0 XOR 1 = 1.

So, Gray code = **0011**.

Q2: The minimum distance of ASCII code is:

(a) 1
(b) 2
(c) 3
(d) 4

Answer: (b) **2**
Explanation:
The minimum Hamming distance between characters in the ASCII table is **2**. ASCII code ensures there is a minimum b

Q3: 8421 code is:

(a) Weighted code
(b) Non-weighted code
(c) Alphanumeric code
(d) None

Answer: (a) **Weighted code**
Explanation:
The 8421 code is a **BCD (Binary Coded Decimal)** code, and it is a weighted code because each bit position has a spec

Q4: A + B'A'AB is same as:

(a) C
(b) 0
(c) 1
(d) C'

Answer: (c) **1**
Explanation:
Using Boolean algebra simplifications:

B'A'ABB'A'AB = 0 (as A·A'A \cdot A' = 0).
A+0=AA + 0 = A.
Thus, the expression simplifies to A+A=1A + A = 1.

Q5: Gate formed by inverting the output of AND gate is:

(a) NAND
(b) OR
(c) NOR
(d) NOT

Answer: (a) **NAND**
Explanation:
A **NAND gate** is an AND gate with an inverted output. Its output is high unless all inputs are high.

Q6: For realizing Boolean expression AC' + AB + BC + BD, the number of inputs are:

(a) 6
(b) 4
(c) 5
(d) 16

Answer: (b) **4**
Explanation:
The given Boolean expression involves variables A,B,C,DA, B, C, D. Hence, the number of inputs required is **4**.

Q7: The two-input logic gate that gives high output when both or any one of the inputs is high:

(a) OR gate
(b) NOT gate
(c) AND gate
(d) All of them

Answer: (a) **OR gate**
Explanation:
An **OR gate** gives a high output (1) if **any one or both** inputs are high. For example:

Input (0, 1) → Output = 1.
Input (1, 1) → Output = 1.

Q8: The XOR gate is a combination of:

(a) AND, OR, and NOT gates
(b) OR and AND gates
(c) NOT and OR gates
(d) NOT and AND gates

Answer: (a) **AND, OR, and NOT gates**
Explanation:
An XOR gate produces a high output (1) when the number of high inputs is odd. It is constructed using a combination c

Q9: For a D flip-flop, the output is:

(a) Always 0
(b) Same as the input
(c) Complement of the input
(d) Always 1

Answer: (b) **Same as the input**
Explanation:
A D flip-flop transfers the input (D) to the output (Q) at the triggering edge of the clock. Hence, the output matches the

Q10: Thermal backing diode:

(a) A
(b) B
(c) C
(d) D

Answer: The exact context of the question isn't clear. Could you clarify or provide additional details?

Q11: What is a universal logic gate?

(a) AND
(b) OR
(c) NAND
(d) NOR

Answer: (c) **NAND** and (d) **NOR** (both are correct, based on interpretation)
Explanation:
NAND and NOR gates are universal gates because any other logic gate can be constructed using only NAND or NOR ga

Q12: How many outputs are there in a full adder?

(a) 2
(b) 4
(c) 8
(d) 1

Answer: (a) **2**
Explanation:
A full adder has two outputs:

Sum (S)
Carry-out (Cout)

Q13: In a combinational circuit, the output depends on:

(a) Past inputs
(b) Present inputs

(c) Both past and present inputs
(d) None

Answer: (b) **Present inputs**
Explanation:
In a combinational circuit, the output is a function of the present inputs only, unlike sequential circuits where past inp

Q14: Dynamic RAM stores data in:

(a) Capacitor
(b) Inductor
(c) Resistor
(d) Transformer

Answer: (a) **Capacitor**
Explanation:
Dynamic RAM (DRAM) stores data as charges in capacitors. These capacitors need to be refreshed periodically to reta

Q15: The three types of basic Boolean operations are:

(a) AND, OR, XOR
(b) AND, NOT, XOR
(c) AND, OR, NOT
(d) AND, NOR, NOT

Answer: (c) **AND, OR, NOT**
Explanation:
The basic Boolean operations are AND, OR, and NOT. XOR and NOR are derived operations.

Q16: Which IC is used for a 4-bit binary adder?

(a) 7483
(b) 7408
(c) 7474
(d) 7490

Answer: (a) **7483**
Explanation:

The **7483** IC is a standard 4-bit binary full adder IC.

Q17: The propagation delay of a flip-flop refers to:

(a) Time from input to clock
(b) Time from clock to input
(c) Time from clock to output
(d) Time from clock to feedback

Answer: (c) **Time from clock to output**
Explanation:
The propagation delay of a flip-flop is the time taken for the output to change after the clock pulse is applied.

Q18: To convert an SR flip-flop to D flip-flop, connect:

(a) S = R
(b) S = R'
(c) S = D, R = D'
(d) None of these

Answer: (c) **S = D, R = D'**
Explanation:
To convert an SR flip-flop to a D flip-flop, connect the **Set input (S)** to **D** and the **Reset input (R)** to **D' (complement of**