2-2-23

Lab - 03

Aim : Analysis and design of Cmos Inverter

Apparatus : ngspice - Software.

Theory:

Cmos - Complementary mos.

1) For any Cmos network we use two Combinational networks. Pull up network, Pull down network.
2) Pull up network is connected with Pmos and VDD.
3) Pull down network is connected with Ground and consists of nmos devices.

Why pull-up - pmos ; Pull-down-nmos?

We know that

For n-mos Drain voltage is higher [VD > Vs]

For P-mos work

$V_{SG} > |V_{th}|$

For n-mos work

$V_{GS} > V_{th}$

} otherwise it goes to Cut-off region

For Inverter. For both Pull-up network & Pull-down network is Given with Same Input

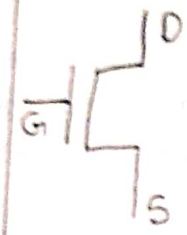
If Pull-up is P-mos, Pull-down is n-mos

I/p	Device-on	Y
0	Pmos	1
1	nmos	0.

It acts as Inverter

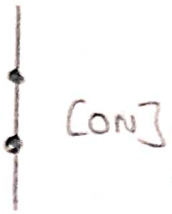
capacity charges upto VDD & goes to Zero

N-MOS

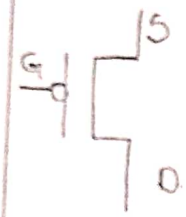


G = 0

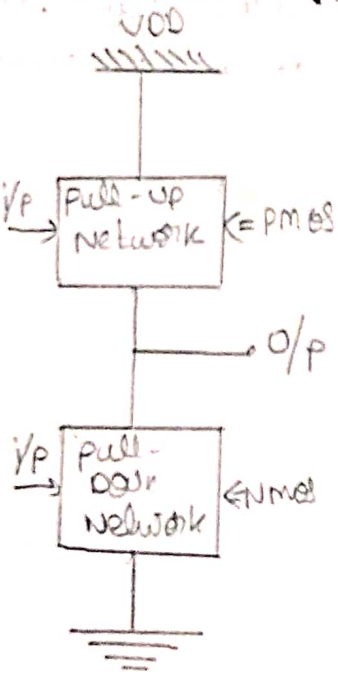
G = 1



P-MOS



C-MOS [Network]:



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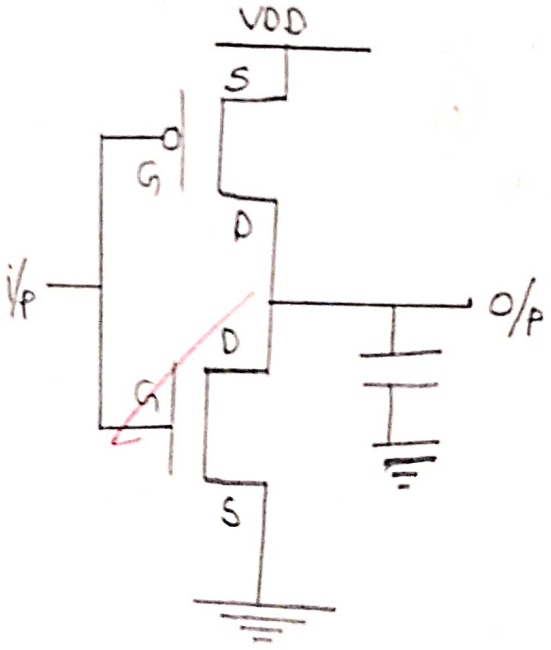


If we change pull-up to n-mos & pull-down to p-mos circuit.

Let us assume $V_{DD} = 5V$. & $V_{th} = 0.7V$.

If i/p = 1 [pull-up network is on / n-mos is on]

capacitor charge upto 4.3V only

$V_{GS} > V_{th}$ [for n-mos to on]

$V_G - V_S > 0.7$

$V_S < V_G - 0.7$; $\boxed{V_S < 4.3V}$ & $V_G = V_{DD}$

After $V_S > 4.3V$ it goes to cut-off.

If i/p = 0. [pull-down network is on / p-mos is on]

capacitor discharge upto 0.7V. only

$V_{SG} > |V_{th}|$ [for p-mos to on]

$V_S - V_G > V_{th}$

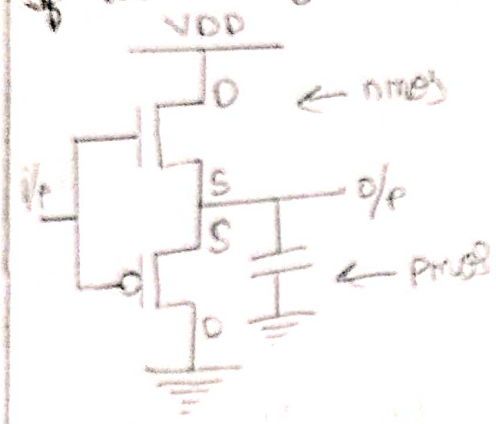
$V_S > V_{th}$

$V_S > 0.7V$.

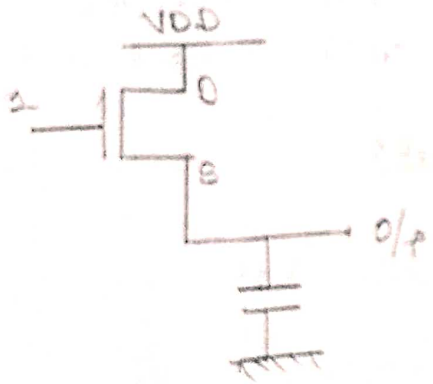
After V_S is less than 0.7V. it goes to cut-off

From this we can conclude that the pmos device can pass 1 but will not pass 0 ; similarly n-mos device can pass 0 but will not pass 1.

If we change:

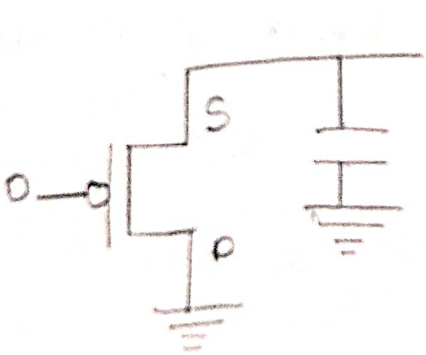


If i/p = 1:



only pull UP - Network is on.

If i/p = 0:



only pull DOWN - Network is ON

Procedure:

1. Name the nodes of the circuits by numbers and Give 0 as ground always.
2. make netlist by nodes ; ie the components between which nodes.
3. Now Give the input of pulse train for 0 & 1's and also do the dc analysis too.
4. And also done the analysis by changing (W/L) of n-mos & p-mos devices
5. Plot the Graphs between vout & time ; vout & Vin.

Code:

(1) Transient analysis:

```
*** CMOS Inverter
Vd  2  0  dc 5 V
vg  1  0  pulse (0 5 0 0 0 10m 20m)
.model nmod nmos level=54 version 4.7
.model pmod pmos level=54 version 4.7
M1  3  1  2  2  pmod  w=100u  l=10u
M2  3  1  0  0  nmod  w=100u  l=10u.
.tran 0.1m 100m
.Control
run
plot v(3) v(1)
.endc
.end
```

DC - analysis :

*** cmos Inverter.

Vd 2 0 dc 5V

Vg 1 0. dc 0V.

• model nmod nmos level = 54 version 4.7

• model pmod pmos level = 54 version 4.7

M1 3 1 2 2 pmod w = 100u l = 10u

M2 3 1 0 0. nmod w = 100u l = 10u

• dc vg 0 5 0.1

• Control

run

Plot v(3) v(1)

• end c

• end

Changing W/L :-

If n-mos device W/L is Increased (or) (W/L)nmos > (W/L)pmos Graph shift towards left.

If p-mos device W/L is Increased (or) (W/L)pmos > (W/L)nmos Graph shift towards Right.

Result/Conclusion :-

We have successfully analysed and designed the cmos Inverter on ngspice software and plotted the graphs.

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