17/02/2023

Lab - 04

Aim :- Implementation of various functions using cmos technology

(i) 3 i/p NAND

(ii) $Y = \overline{ABC + D}$

(iii) $Y = \overline{AB + C(D+E)}$

(iv) 3 i/p NOR

Apparatus Required :- mospice software

Theory :

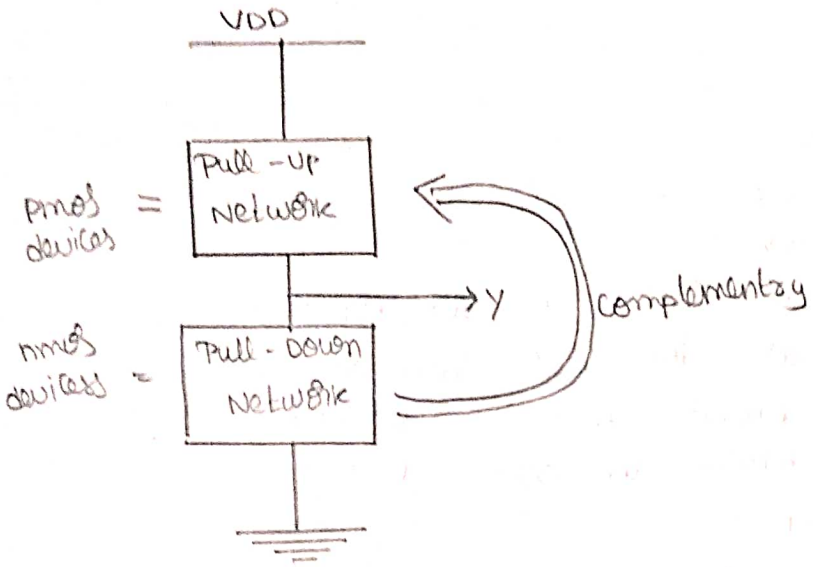
Cmos - Complementary mos

1) For any cmos network, we use two combinational networks
   a) pull-up Network
   b) Pull-down Network
2) Pull-up network is connected with PMOS devices with VDD
3) Pull down Network is connected with ground and consists of n-mos device
4) pull Down - Network is complementary of Pull-up
5) We want to design pull down-network and complement it for Pull-up Network.
6) For AB → Series → Complementary = Parallel
   A+B → Parallel → Complementary = Series

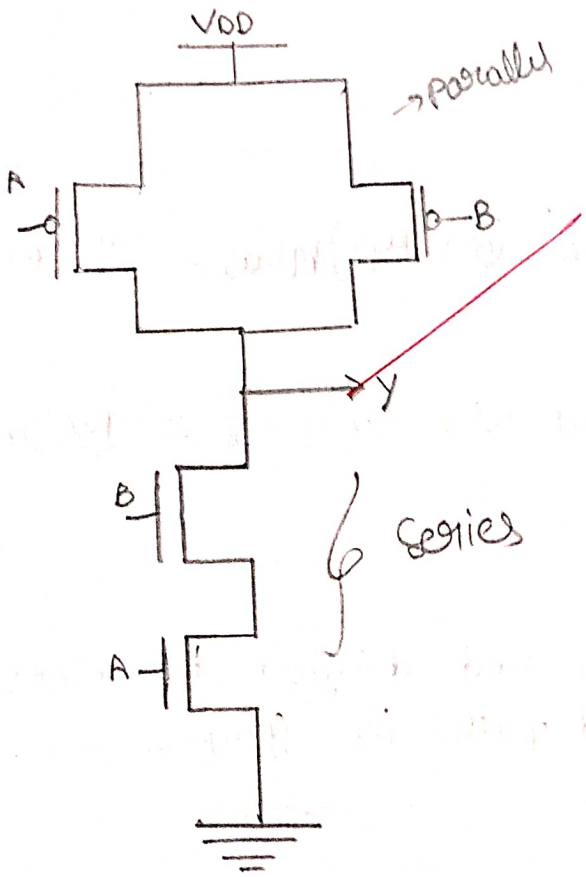
Procedure :

① make the cmos circuit using Pull-up, Pull-down logics by Series Parallel combinations.
② Name the nodes of the circuits by numbers and give 0 as ground always.
③ make netlist by nodes
④ plot the graphs b/w vout & Vin [by changing Vin (A, B, C)]

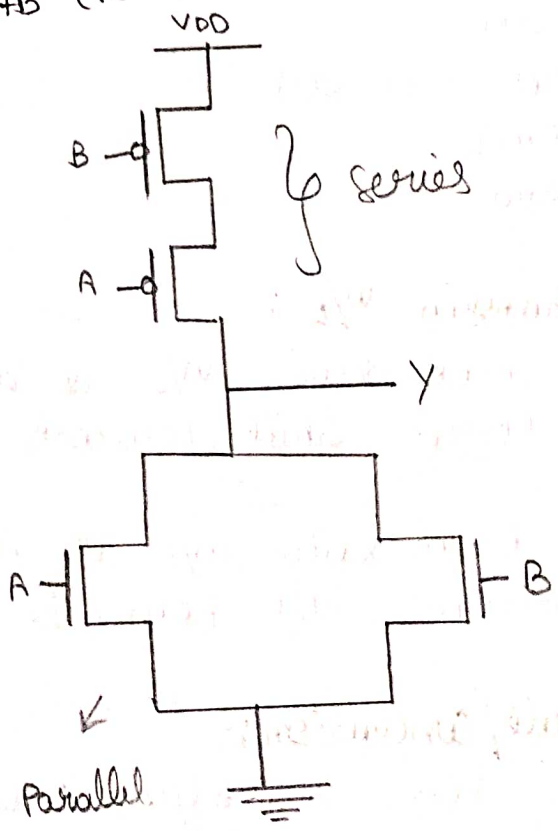
CMOS (Complementary MOS) :-



$Y = \overline{A \cdot B}$ (series)



$Y = \overline{A+B}$ (Parallel)



(1) NAND:-

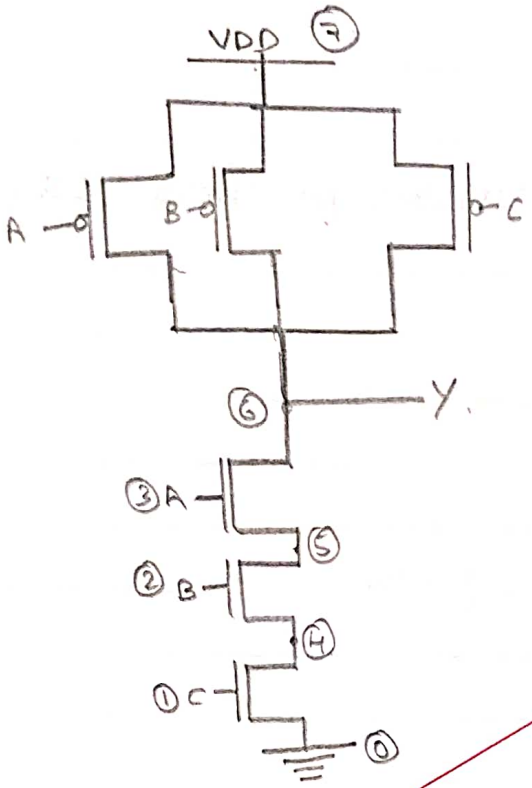
Logic for NAND gate is $Y = \overline{A \cdot B \cdot C}$

* Let us consider B = C = 1 [as 5V] and now vary the A by Pulses.
* If A = 1 Y = 0 } work as Inverter type (complementary)
  A = 0 Y = 1

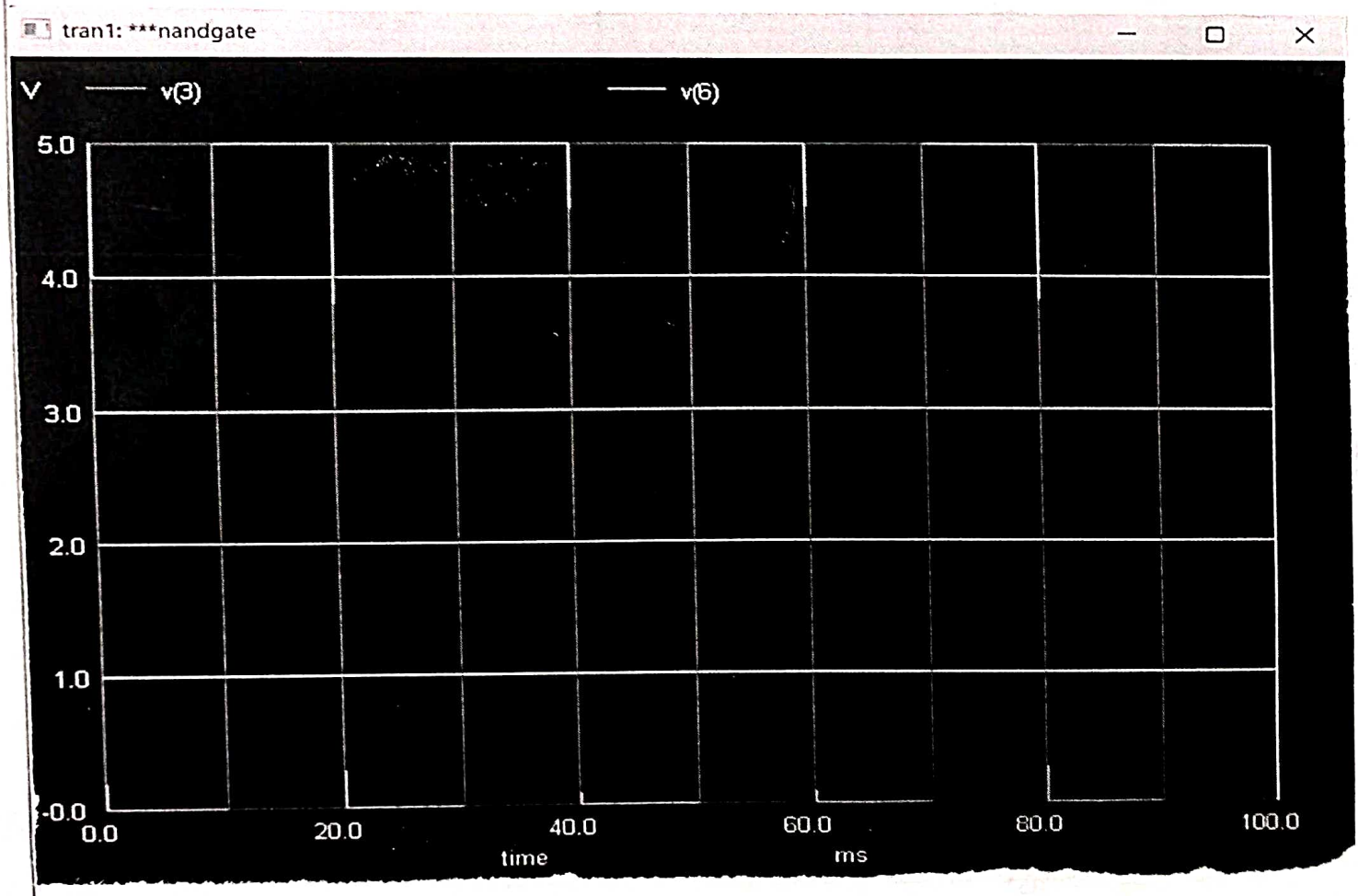
Code:-

```
***Nandgate
V1  3  0  Pulse (0 5 0 0 0 10m 20m)
V2  2  0  dc 5V
V3  1  0  dc 5V
Vd  7  0  dc 5V
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
m1n  4  1  0 0  nmod  w=100u  l=10u
m2n  5  2  4 4  nmod  w=100u  l=10u
m3n  6  3  5 5  nmod  w=100u  l=10u
m1p  6  1  7 7  pmod  w=100u  l=10u
m2p  6  2  7 7  pmod  w=100u  l=10u
m3p  6  3  7 7  pmod  w=100u  l=10u
.tran 0.1m 100m
.control
run
plot v(6) v(3)
.endc
.end
```

NAND:- $Y = \overline{ABC}$



output :-



(ii) Logic 1 { $Y = \overline{ABC + D}$ }

Let us consider $B = 0$, $A = C = 1$, so then output only depends on D. So give input D as transient

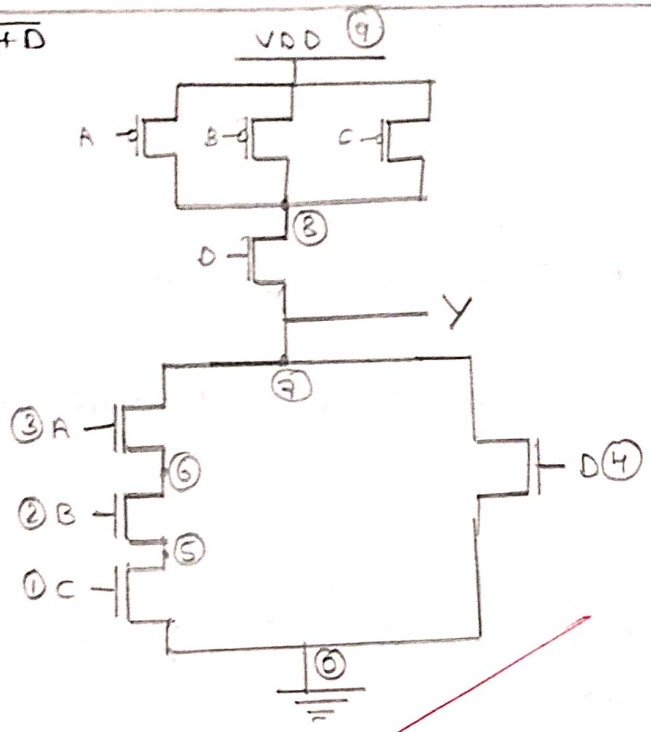
If $D = 0$ $Y = 1$ } complementary

$D = 1$ $Y = 0$.

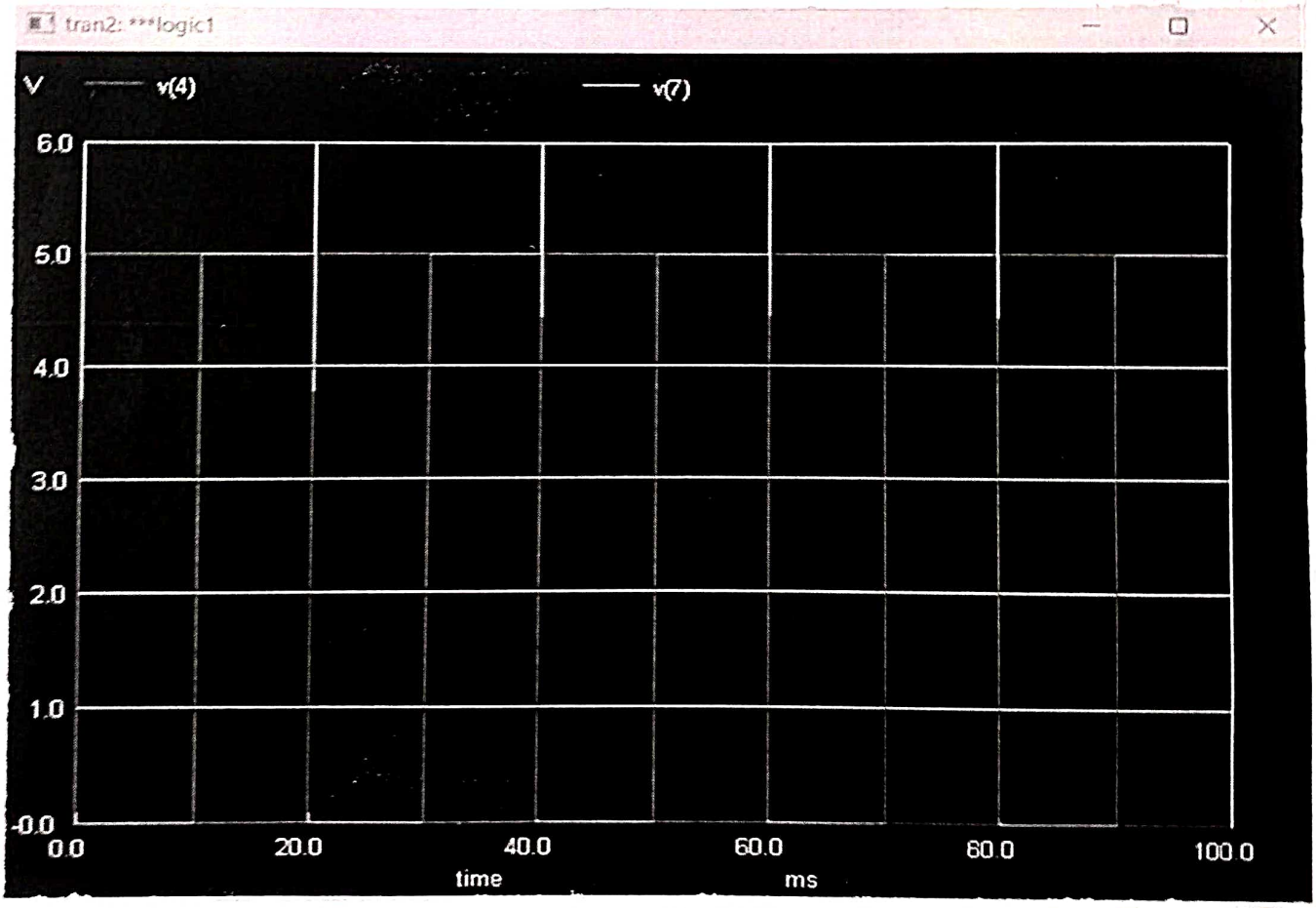
Code:-

```
***Logic 1.
V4  4  0  Pulse (0 5 0 0 0  10m  20m)
V2  2  0  dc 0V
V3  3  0  dc 5V
V1  1  0  dc 5V
Vd  9  0  dc 5V
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
m1n  5 1 00 nmod w=100u l=10u
m2n  6 2 55 nmod. w=100u l=10u
m3n  7 3 66 nmod w=100u l=10u
m4n  7 4 00. nmod w=100u l=10u
m1p  7 4 88 pmod w=100u l=10u
m2p  8 3 9 9. pmod w=100u l=10u
m3p  8 2 9 9 Pmod w=100u l=10u
m4p  8 1 9 9 pmod w=100u l=10u
.tran 0.1m 100m
.control
run
plot v(7) v(4)
.end c
.end
```

Logic (1) $Y = \overline{ABC + D}$



output :



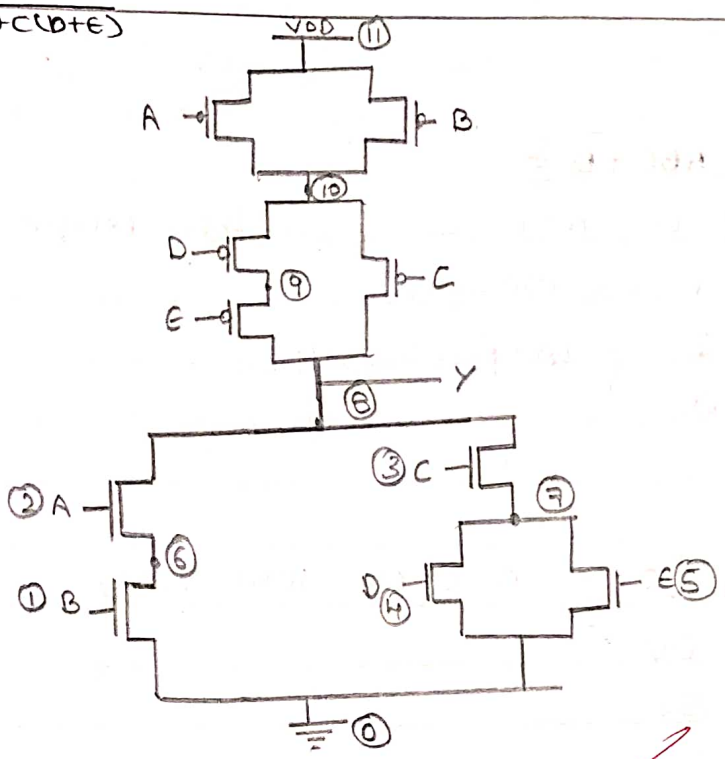
(iii) Logic 2 {$Y = (AB + C(D+E))'$}.

Set up condition $B=1$ and $C=0$, $D=E=1$ then output only depends on A so give input for A as pulse. If $A=0$ $Y=1$ } Complementary
$A=1$ $Y=0$ }

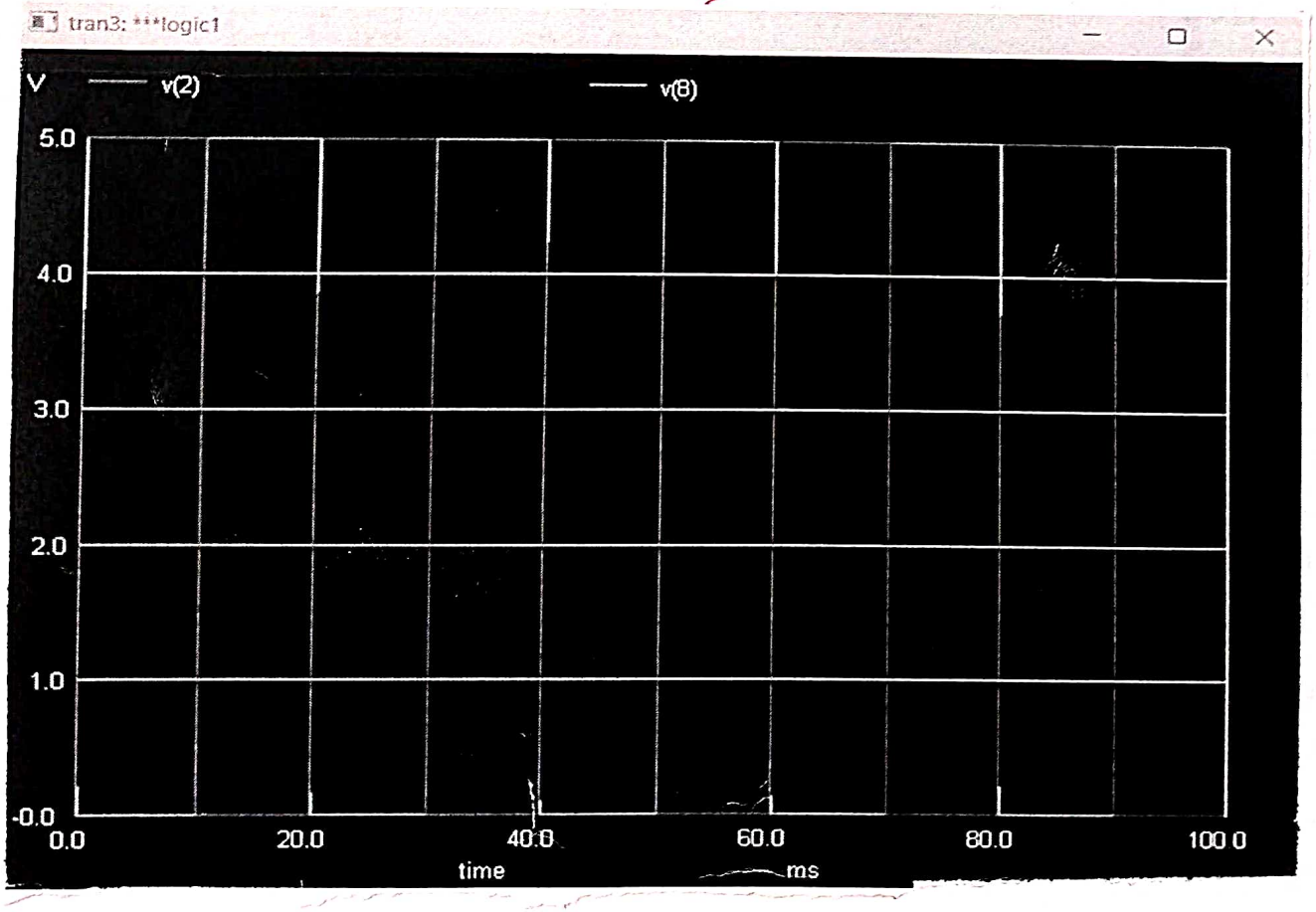
Code:-

```
*** Logic 2 {Y=(AB + C(D+E))'}
V1 1 0 pulse (0 5 0 0 0 0 0ms 20ms)
V2 2 0 dc 5V
V3 3 0 dc 0V
V4 4 0 dc 5V
V5 5 0 dc 5V.
Vd 11 0 dc 5V
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
m1n 8 2 6 6 nmod w=100u l=10u
m2n 6 1 0 0 nmod w=100u l=10u
m3n 8 3 7 7 nmod w=100u l=10u
m4n 7 4 0 0 nmod w=100u l=10u
m5n 7 5 0 0 nmod w=100u l=10u
m1p 8 3 10 10 Pmod w=100u l=10u
m2p 8 5 9 9 Pmod w=100u l=10u
m3p 9 4 10 10 Pmod w=100u l=10u
m4p 10 2 11 11 Pmod w=100u l=10u
m5p 10 1 11 11 Pmod w=100u l=10u
.tran 0.1m 100m.
.control
run
plot v(8) v(2)
.endc
.end.
```

Logic 2 $Y = \overline{AB + C(D+E)}$



Output:



NOR gate :-

Logic expression for NOR gate is $Y = \overline{A+B+C}$

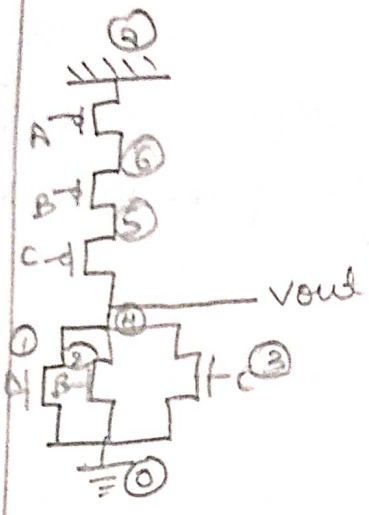
So, let us consider B = 5V (1) ; C = 0 ; A = Pulse. Then the output Y = 1 [A = 0] & constant.

Y = 1 [A = 1].

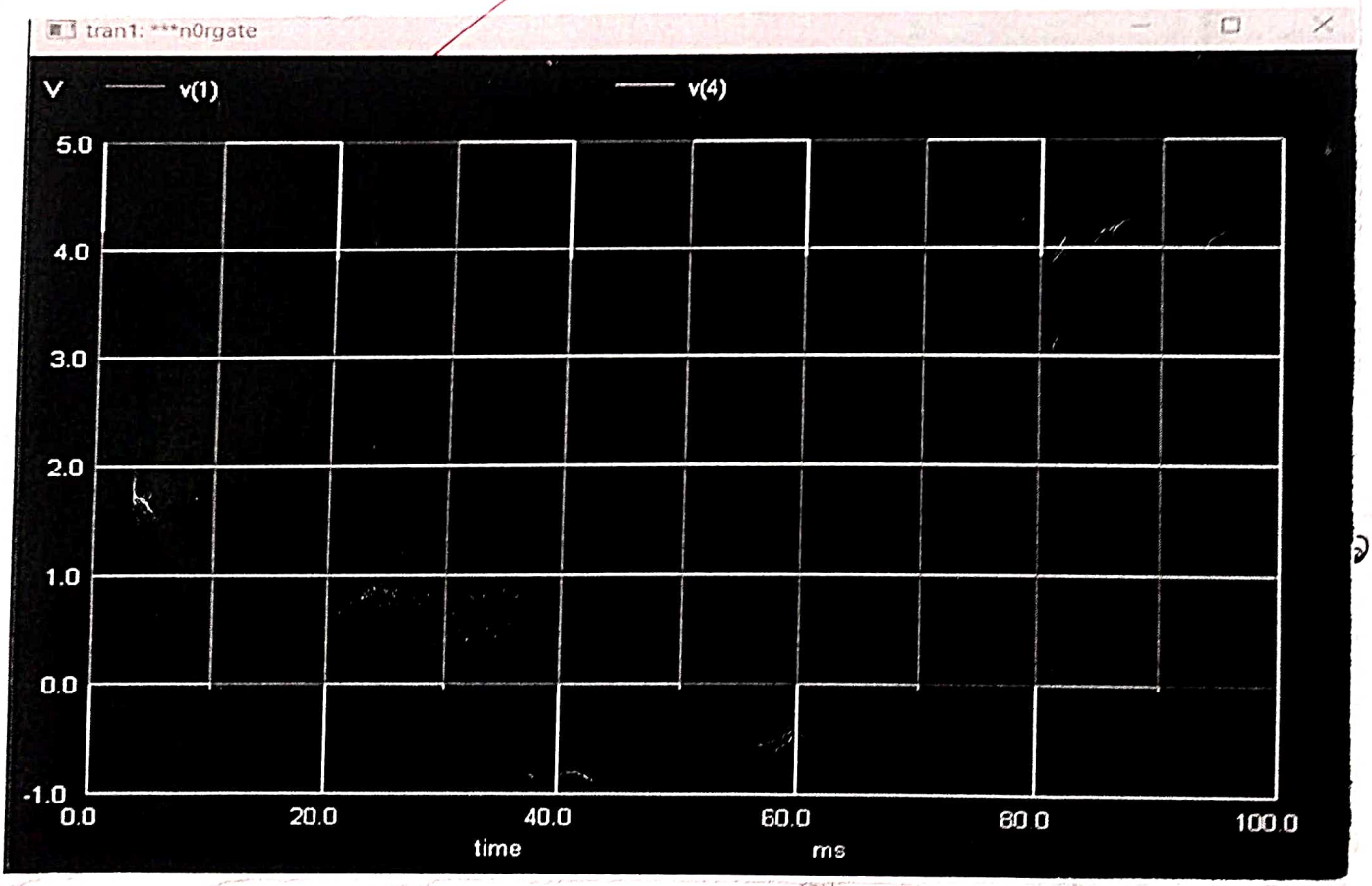
Code :-

```
***NOR Gate
V1  1  0  Pulse (0 5 0 0 0 10m 20m)
V2  2  0  dc 5V
V3  3  0  dc 0V
Vd  7  0  dc 5V
.model nmod nmos level = 54 version = 4.7
.model pmod pmos level = 54 version = 4.7
m1n  4  1  0 0  nmod  w = 100u  l = 10u
m2n  4  2  0 0  nmod  w = 100u  l = 10u
m3n  4  3  0 0  nmod  w = 100u  l = 10u
m1p  4  3  5 5  Pmod  w = 100u  l = 10u
m2p  5  2  6 6  Pmod  w = 100u  l = 10u
m3p  6  1  7 7  pmod  w = 100u  l = 10u
.tran 0.1m 100m.
.Control.
run
plot V(4) V(1).
.end
.end.
```

Logic - 3:- 3 i/p NOR gate



output :-



NOR ($Y = \overline{A+B+C}$).

Conclusion:

From this we conclude that the capacitor charging & discharging depends upon w/L and output V is depend on all the inputs

(i) NAND $Y = \overline{ABC}$ ⇒ complementary

(ii) NOR $Y = \overline{A+B+C}$ ⇒ confused

(iii) $Y = \overline{A+C(B+D)}$ ⇒ complementary

(iv) $Y = \overline{AB+C(D+E)}$

Result:

we have successfully designed the Nand, NOR and given two logics by using cmos on ngspice software and also plotted the output graphs on ngspice using different inputs