

# Guneev Dhillon

(236)332-5804 | guneevd@student.ubc.ca | www.linkedin.com/in/guneev-dhillon | guneevdhillon.com (Portfolio + GitHub)

## EDUCATION

### University of British Columbia

*Bachelor of Applied Science in Computer Engineering*

Vancouver, BC

- Dean's List (2024–25)
- Relevant Coursework: Computing Systems (RISC-V, FPGA), Signals and Systems, Digital Logic, Embedded Systems, Software Construction

## PROJECTS

### RISC-V Labs | C, RISC-V Assembly, SystemVerilog, FPGA, Quartus

2024–2025

- Designed and implemented embedded programs in **C** and **RISC-V assembly** targeting a soft-core processor on an FPGA, interacting directly with **memory-mapped I/O** peripherals
- Built and debugged a **single-cycle RISC-V processor** using SystemVerilog, validating datapath components including ALU, control logic, and register file
- Implemented **interrupt-driven input handling** using hardware timers and edge-capture registers to respond to button presses without polling
- Developed low-level drivers for **LEDs, seven-segment displays, VGA output, and JTAG UART**, reasoning about timing, registers, and bit-level control
- Used **Quartus Prime** and FPGA simulation tools to test, synthesize, and debug hardware-software interactions under constrained execution environments

### NotiFlow | Python, Flask, React, REST APIs, Docker, DigitalOcean, Git

2025

- Designed and debugged a multi-component system with strict interface contracts between services, emphasizing correctness and fault handling
- Owned end-to-end debugging across components, reinforcing disciplined reasoning about system state and data flow

## EXPERIENCE

### Signal Processing Engineer

Oct 2024 - Present

*MindTap, UBC Biomedical Engineering Student Team*

Vancouver, BC

- Owned the processing of **raw EEG sensor signals**, analyzing sampling rates, noise sources, and signal drift to determine viable preprocessing strategies
- Implemented real-time EEG filtering by tuning window sizes and thresholds to reduce noise while maintaining responsive system behavior
- Developed and validated **feature extraction logic** to reliably convert continuous biosignals into discrete control events usable by downstream systems
- Standardized the format and timing of processed EEG outputs so downstream components could reliably consume real-time control signals
- Debugged end-to-end signal flow from sensor input to application response, tracing failures across acquisition, processing, and interface boundaries
- Iterated on signal-processing logic based on empirical testing and failure cases rather than idealized assumptions

### Lead Code Instructor

Sept 2022 - Sept 2024

*Code Ninjas*

Surrey, BC

- Mentored over **150 students** in designing and building games and robots using C#, JavaScript, and Python
- Guided students through the full development cycle, from ideation to deployment, emphasizing modular design
- Tailored coding curricula to support diverse learning levels and foster creativity and technical confidence

## TECHNICAL SKILLS

**Languages:** C, RISC-V Assembly, SystemVerilog, Python, Java

**Embedded & Hardware:** FPGA (DE10-Lite), digital logic, interrupts, timers, memory-mapped I/O, VGA, UART

**Tools:** Quartus Prime, Git, Linux, VS Code, ModelSim, JTAG debugging

**Software:** Flask, React, REST APIs, Docker