IIT Guwahati - Department of Computer Science & Engineering

CS 223- Computer Architecture & Organization – Problem Sheet

1. Consider an instruction pipeline of an issue width of 1 that uses Tomasulo's algorithm with two reservation station per functional unit. There is one instance of each functional unit type and a single CDB. There is an arbitration mechanism for resolving CDB entry collision. Preference is given in round robin fashion. The functional units are not pipelined. An instruction waiting for data on CDB can move to its EX stage in the cycle after the CDB broadcast.

   Assume the following information about functional units.

Functional unit type	Cycles in Execution stage
Integer Mul	4
Integer Div	8
Integer Add	1

   Complete the following table using Tomasulo's algorithm with the above specifications. Fill in the cycle numbers in each pipeline stage for each instruction, and indicate where its source operand's are read from (use RF for register file, ROB for reorder buffer and CDB for common data bus). Some entries are filled in for you. Fill the rest.

#	Instruction	Issue	Src Operand1	Src Operand2	EX	WB	Commit
1	DIVI R4, R4, #12	1	RF	Imm	2	10	11
2	MUL R2, R6, R12	2	RF	RF	3	7	12
3	DIV R1, R1, R2	3	RF	CDB	8		
4	ADD R5, R1, R3						
5	ADDI R7, R2, #4						
6	ADD R5, R6, R7						
7	ADDI R8,R8, #24						
8	ADD R9, R6, R8						
9	MUL R5, R5, R10						
10	ADD R6, R8, R5						

2. Consider the following instruction sequence executed on a MIPS floating point pipeline. Operand forwarding is implemented. [R indicates integer registers and F indicates floating point registers]. Find the clock cycle in which STOR instruction reaches MEM stage. If 8(R2) contains value ‘X’ and F2 contains value ‘A’, then what is stored in 16(R3)

   LOAD F4, 8(R2);
   FMUL F0, F4, F2;
   FADD F3, F0, F2;
   STOR F3, 16(R3);

1. In a dynamically issued speculative superscalar processor the reservation station entries of two functional units (Mul and Add) at clock cycle T is as shown below. At T, none of the instructions waiting in the reservation station have started execution.

Name	Busy	Op	Vj	Vk	Qj	Qk	Dest	A
Mul	Yes	FMUL	8	5	0	#4	#5	40
Mul	Yes	FDIV	2	8	#6	0	#7	20

Name	Busy	Op	Vj	Vk	Qj	Qk	Dest	A
Add	Yes	FADD	8	5	#4	#5	#6	10

(A) Write any possible sequence of three instructions (in the order of issue) along with their corresponding register operands that could result in the reservation station entries shown above. Only F1, F2 and F3 can be used as the operands for the instructions.
Instruction syntax should be of the form: *Opcode DestReg, SrcReg1, SrcReg2*.

(B) State other mandatory conditions (if any) that should hold at the time of issue of these instructions to ensure the correctness of the above entries.

2. Consider a dynamically scheduled single issue instruction pipeline with speculation using a branch predictor that always predicts the branch as taken. The pipeline has one FP-multiplier that takes 4 cycles for execution, one FP-adder that takes 2 cycles for execution, one integer unit that takes 1 cycle for execution and one memory address unit that takes 1 cycle to compute effective address for load and store operations. All the integer and FP units are fully pipelined and support operand forwarding. Memory access for a load operation takes place in the next cycle after the address computation. Store operation access memory only upon commit. This speculative pipeline is implemented with a 4-entry ROB. Assume that instruction issue will not be stalled due to availability of reservation stations. Consider the following code with 9 instructions (I1-I9).

Initial values of registers are as follows: F1← a, F2← b, F3← c, R2← 200, R3← 240

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I1-lxx: L.D F4, 0(R2)          ; load X
I2-     MUL.D F5, F4, F4
I3-     MUL.D F5, F5, F1
I4-     MUL.D F4, F4, F2
I5-     ADD.D F6, F5, F4
I6-     ADD.D F6, F6, F3
I7-     S.D F6, 48(R2)         ; store Y
I8-     ADDI R2, R2, #8
I9-     BNE R2,R3, lxx         ; branch to lxx if R2!=R3
```

Fill up the time of issue, execution, memory access, CDB write and commit for one iteration of the loop in the table given below. Answer the questions given below the table.

	Instruction	Issue	Execute	Memory Access	CDB Write	Commit
I1	L.D F4, 0(R2)	1	2	3	4	5
I2	MUL.D F5, F4, F4	2				
I3	MUL.D F5, F5, F1					
I4	MUL.D F4, F4, F2					
I5	ADD.D F6, F5, F4					
I6	ADD.D F6, F6, F3					
I7	S.D F6, 48(R2)					
I8	ADDI R2, R2, #8					
I9	BNE R2,R3, lxx					

From the duly filled table answer the following questions.

(A) In which clock cycle I4 write result to CDB?

(B) In which clock cycle I6 is issued?

(C) In which clock cycle I7 access memory?

(D) In which clock cycle I8 starts execution?

(E) What is the relation between X and Y in terms of a, b and c?

(F) How many times the loop will be iterated?