CS223 : Computer Architecture & Organization

Lecture 24 [04.04.2022]

Introduction to RISC instruction pipeline

Dr. John Jose

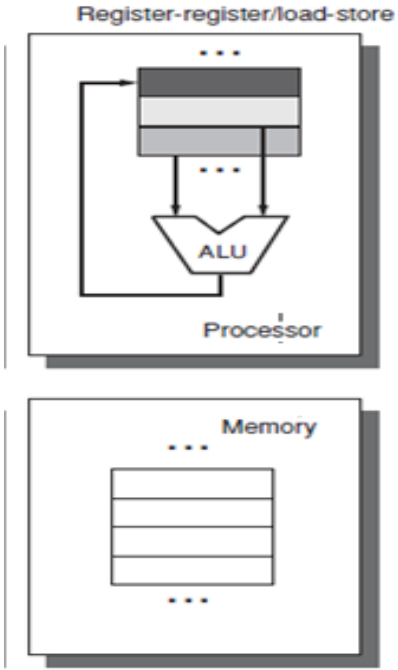
Associate Professor

Department of Computer Science & Engineering

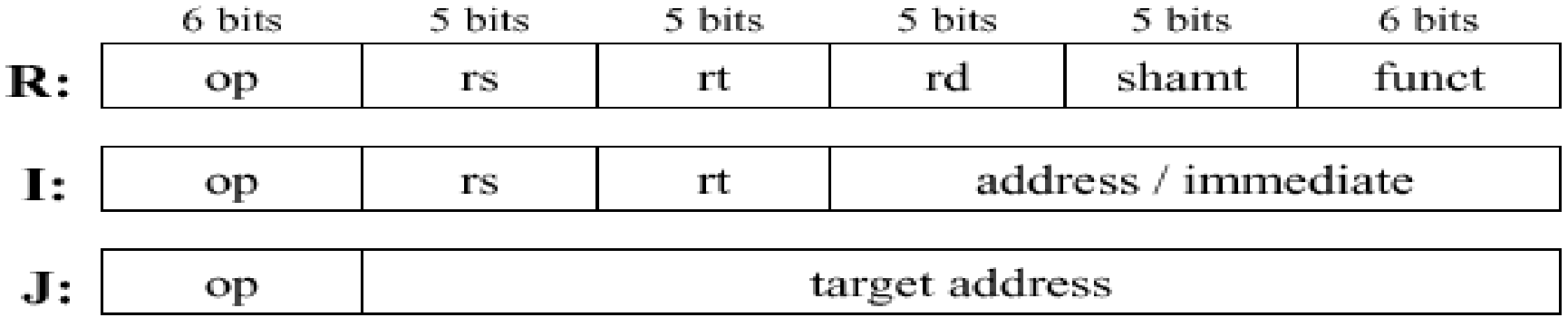
Indian Institute of Technology Guwahati, Assam.

Introduction to MIPS

- Microprocessor without Interlocked Pipelined Stages
- 32 registers (32 bit each)
- Uniform length instructions
- RISC- Load store architecture



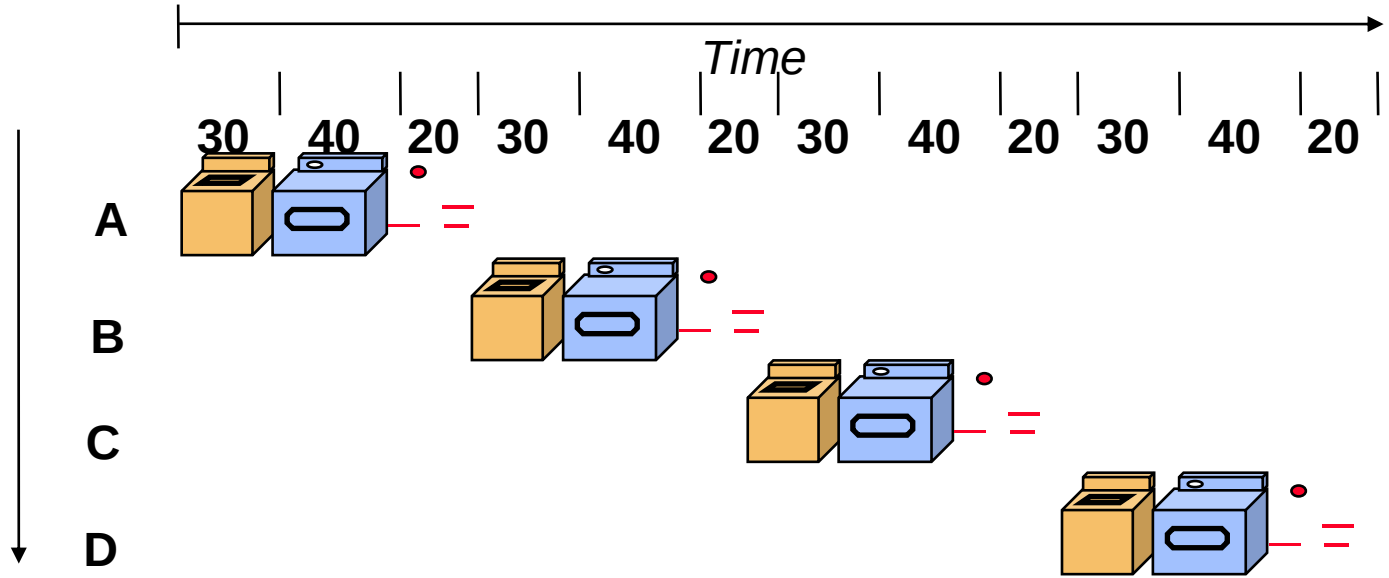
Introduction to MIPS



op: basic operation of the instruction (opcode)
rs: first source operand register
rt: second source operand register
rd: destination operand register
shamt: shift amount
funct: selects the specific variant of the opcode (function code)
address: offset for load/store instructions (+/-2^{15})
immediate: constants for immediate instructions

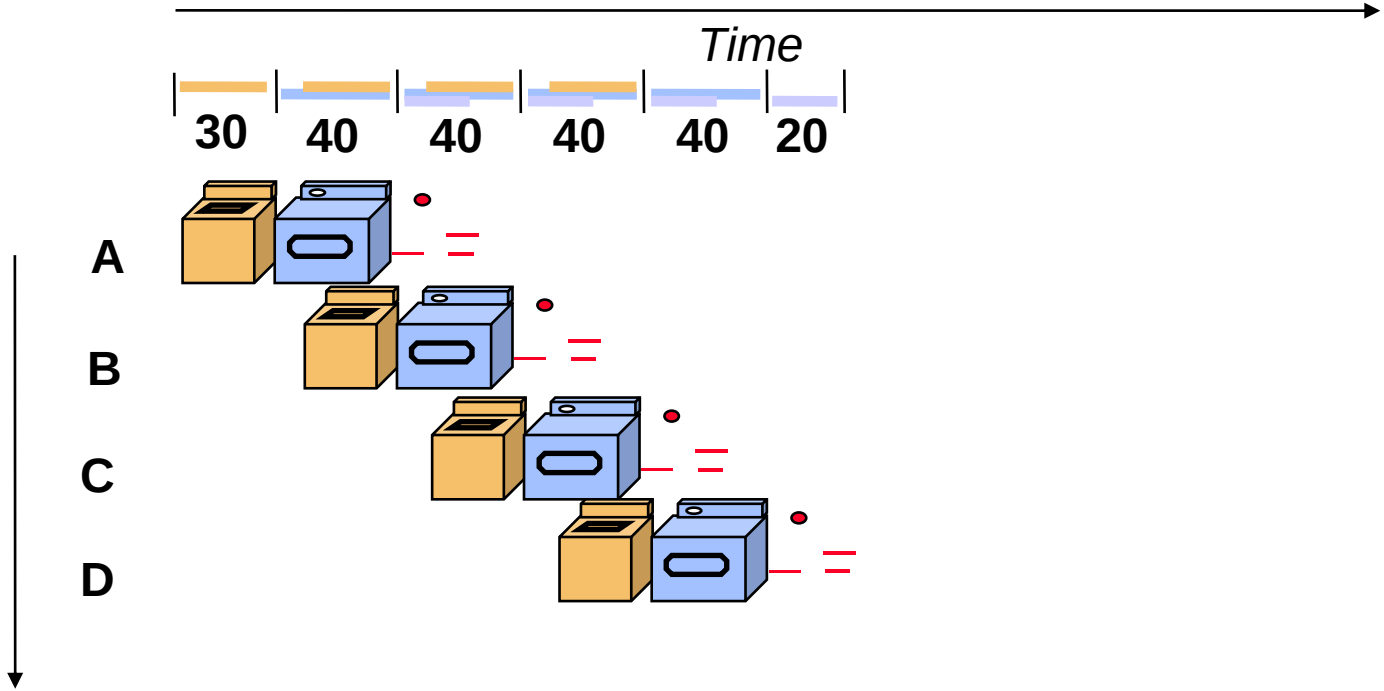
Unpipelined Work flow

- Start work when previous one is fully over
- Sequential laundry takes 6 hours for 4 loads



Pipelined Work flow

- Start work as soon as possible
- Pipelined laundry takes 3.5 hours for 4 loads

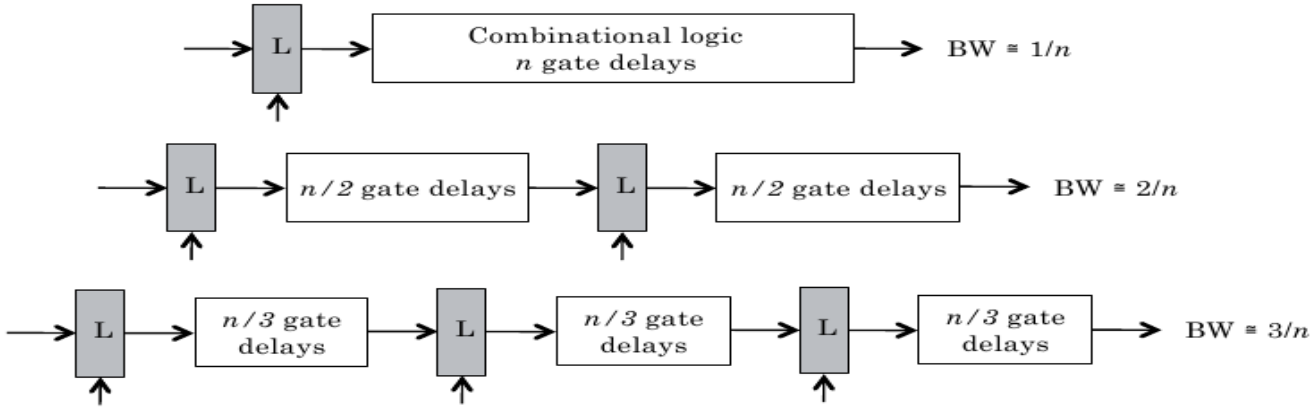


Pipelining Characteristics

- Pipelining doesn't reduce latency of single task, it improves throughput of entire workload
- Pipeline rate limited by slowest pipeline stage
- Potential speedup = Number of pipe stages
- Unbalanced lengths of pipe stages reduces speedup
- Time to fill pipeline and time to drain it reduces speedup

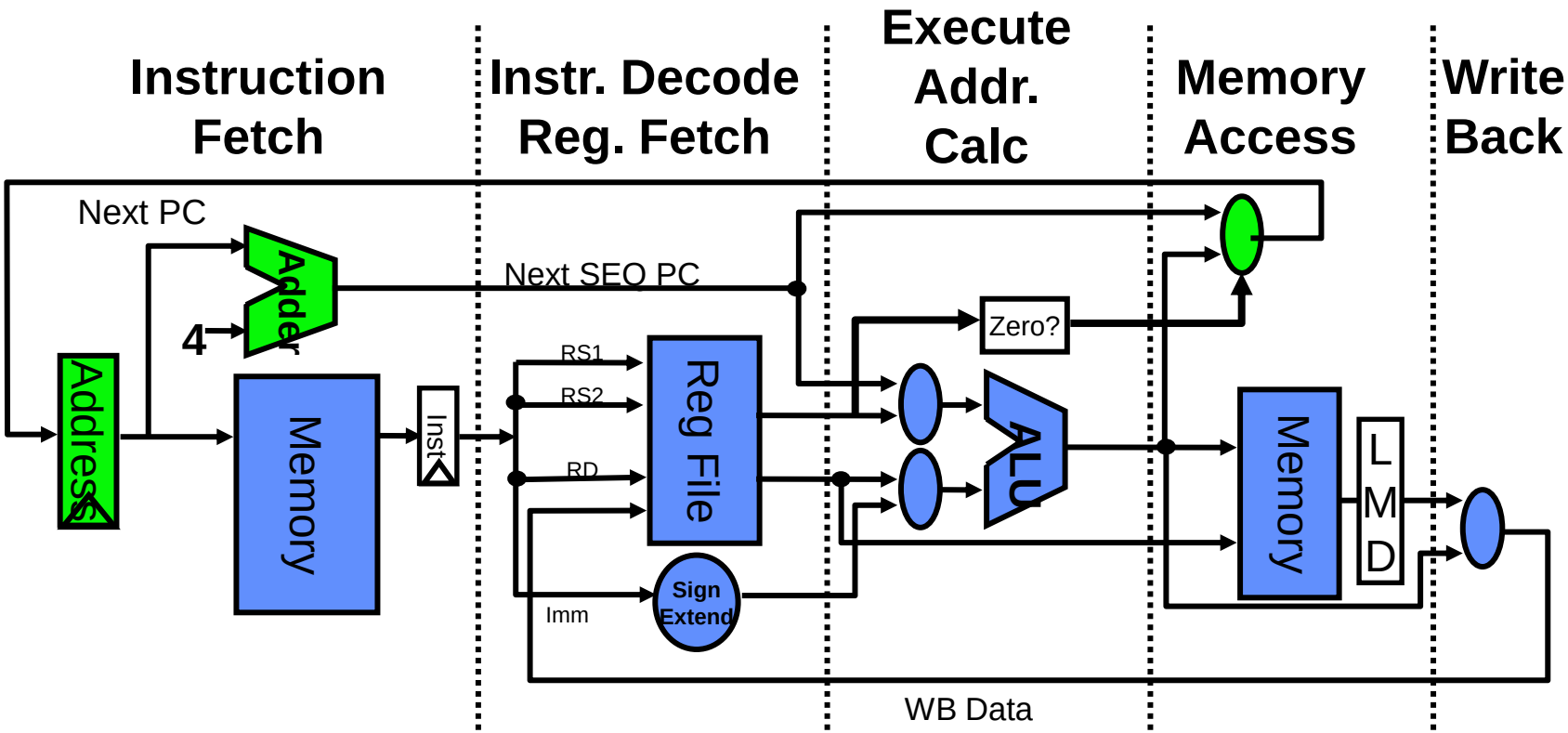
Pipelining in Circuits

- Pipelining partitions the system into multiple independent stages with added buffers between the stages.
- Pipelining can increase the throughout of a system.



Potential k-fold increase of throughput in a k-stage pipelined system

Unpipelined RISC Data path



Reference

- **Computer Architecture-A Quantitative Approach** (5th edition), John L. Hennessy, David A. Patterson, Morgan Kaufman.
- Appendix C: **Pipelining: Basic and Intermediate Concepts**
  - Section C1: **Introduction**

- **NPTEL Video Link: https://tinyurl.com/ybcx9sae**

johnjose@iitg.ac.in
http://www.iitg.ac.in/johnjose/