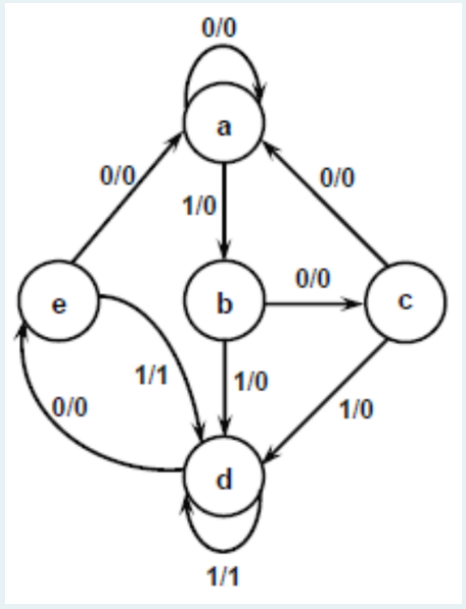
CS224_2021_quiz3_A

Points: 15/20

1



For the FSM given in the figure, write the Verilog code. Put your answers from Q-2 onward as this question is not graded.
Use 'x' as input variable and 'y' as output variable.
The other inputs are 'clk' and 'reset'

declarations in q2

2

Write the Verilog code statements to change the current state. Use 'x' as input variable and 'y' as output variable.
(2/2 Points)

```
//Includes declarations
module q1(
        input x,
        input reset,
        input clk,
        output reg y
        );
reg[2:0] curr, nex;
parameter a = 3'b000;
parameter b = 3'b001;
parameter c = 3'b010;
parameter d= 3'b011;
parameter e = 3'b100;

always@(posedge clk or posedge reset)
begin
        if(reset) curr = 0;
        else curr = nex;
end
```

3

Write Verilog code statements for next state and output logic
(10/10 Points)

```
//  See q2 for declarations
always@(x or curr)
begin
	case(curr)
	a :
	begin
	if(x == 0) begin nex = a; #2 y = 0; end
	else  begin nex = b; #2 y = 0; end
	end
	b :
	begin
	if(x == 0)  begin nex = c; #2 y = 0; end
	else  begin nex = d; #2 y = 0; end
	end
	c :
	begin
	if(x == 0) begin  nex = a; #2  y = 0; end
	else  begin nex = d; #2 y = 0; end
	end
	d :
		begin
	if(x == 0)  begin nex = e; #2 y = 0; end
	else  begin nex = d; #2 y = 1; end
	end
	e :
		begin
	if(x == 0)  begin nex = a; #2 y = 0; end
	else  begin nex = d; #2 y = 1; end
	end
	default : nex = a;
	endcase
end
```

4

For the testbench code given below, paste that in your testbench file and generate the output. Paste the output of the monitor after running the testbench in the space below.

```
initial begin
clk = 0;   forever clk = #5 ~clk;
end

initial begin
$monitor($time, " x=%b, y=%b ", x, y);
reset = 1; x=0;
#10; reset = 0;
#10; x = 0;
#12; x = 1; #5; x=0;
#17; x = 1; #3; x=0;
#17; x = 1; #18; x = 0;
#12; x = 1; #5; x=0;
end
```

(3/8 Points)

```
0 x=0, y=x
                2 x=0, y=0
               32 x=1, y=0
               37 x=0, y=0
               54 x=1, y=0
               57 x=0, y=0
               74 x=1, y=0
               76 x=1, y=1
               92 x=0, y=1
               94 x=0, y=0
              104 x=1, y=0
              106 x=1, y=1
              109 x=0, y=1
              111 x=0, y=0
```