CS223 : Computer Architecture & Organization

Lecture 32 [25.04.2022]

Tiled Chip Multicore Processors & Network on Chip

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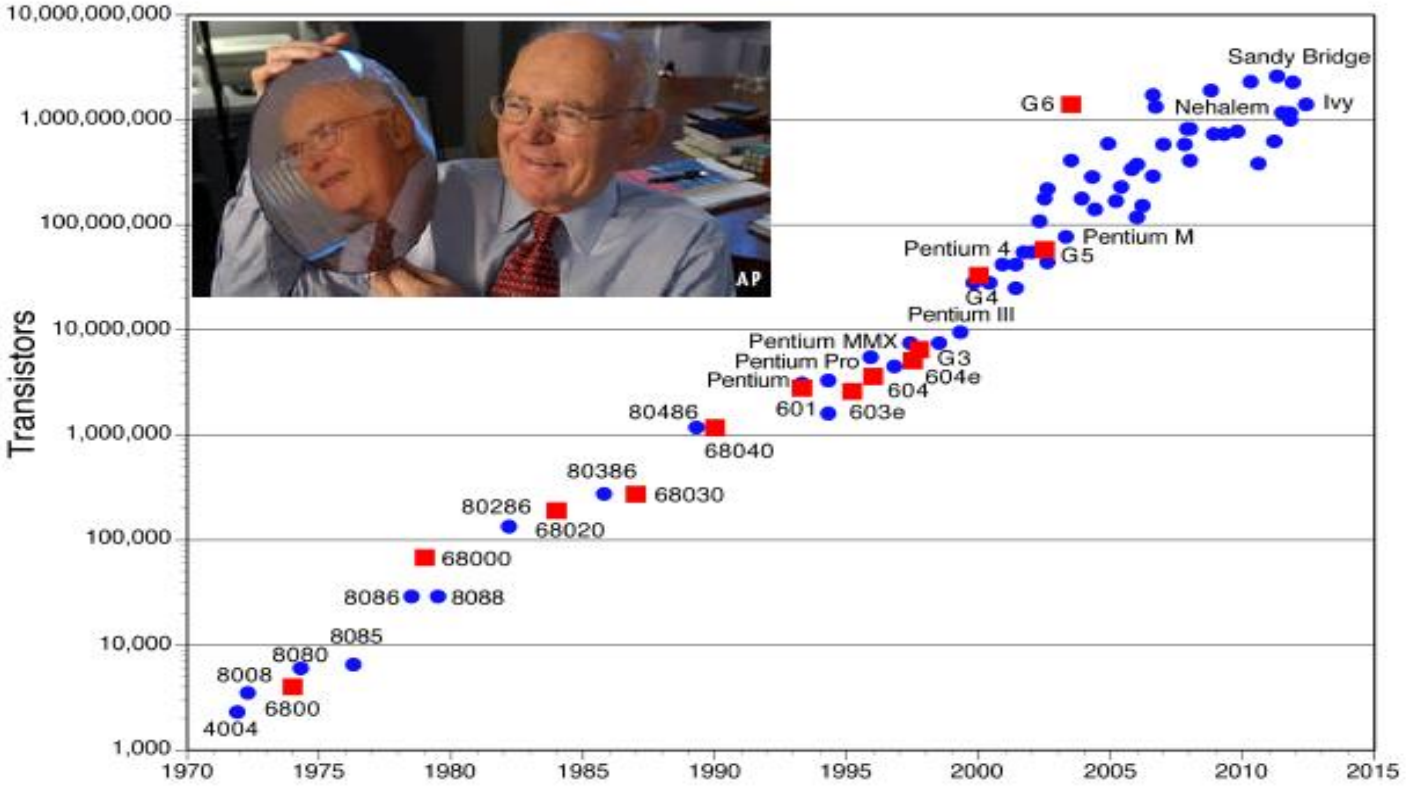
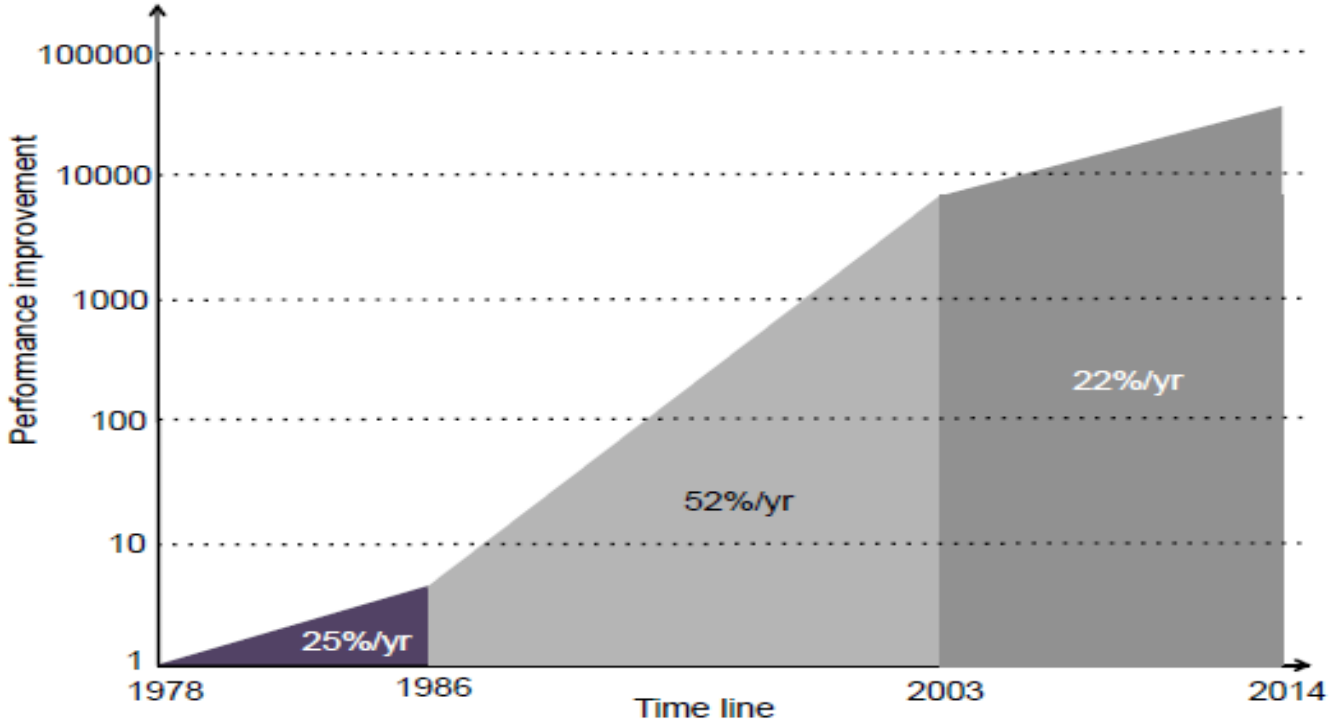
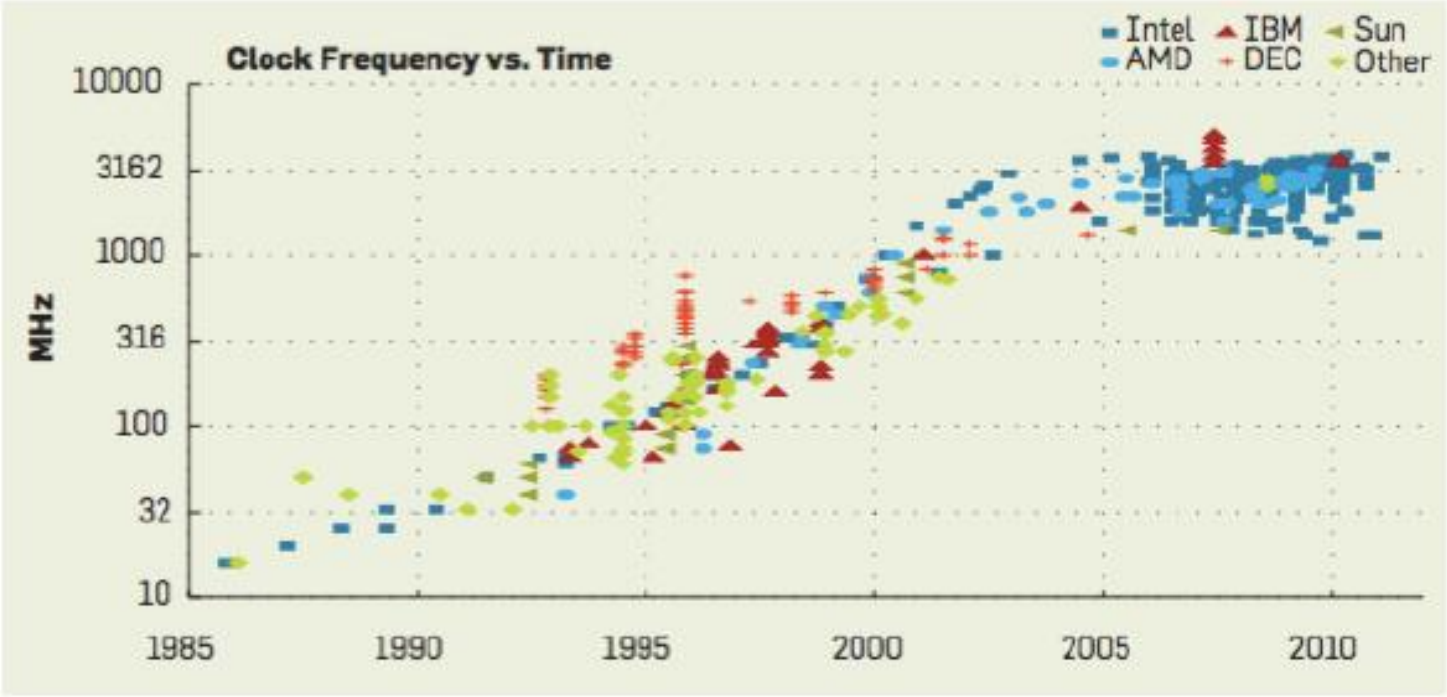
Impact of VLSI in processor trends



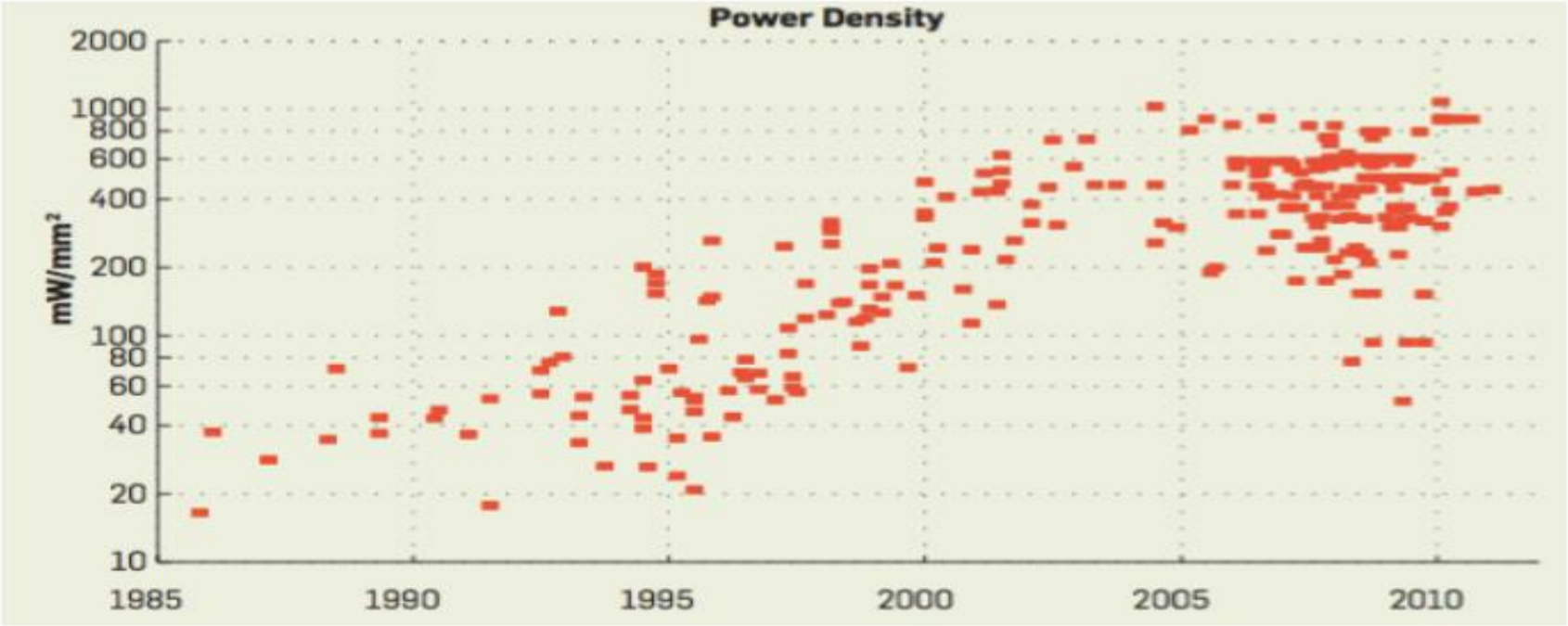
Processors Performance



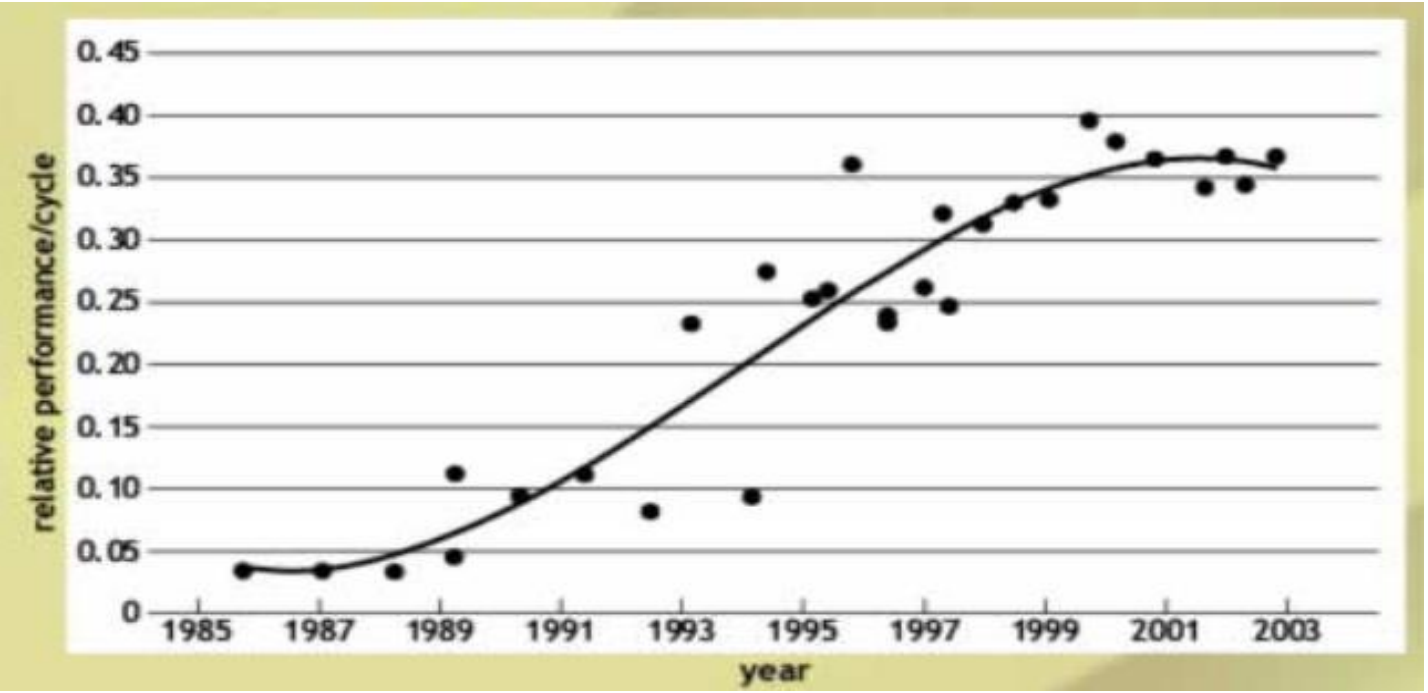
Frequency Wall



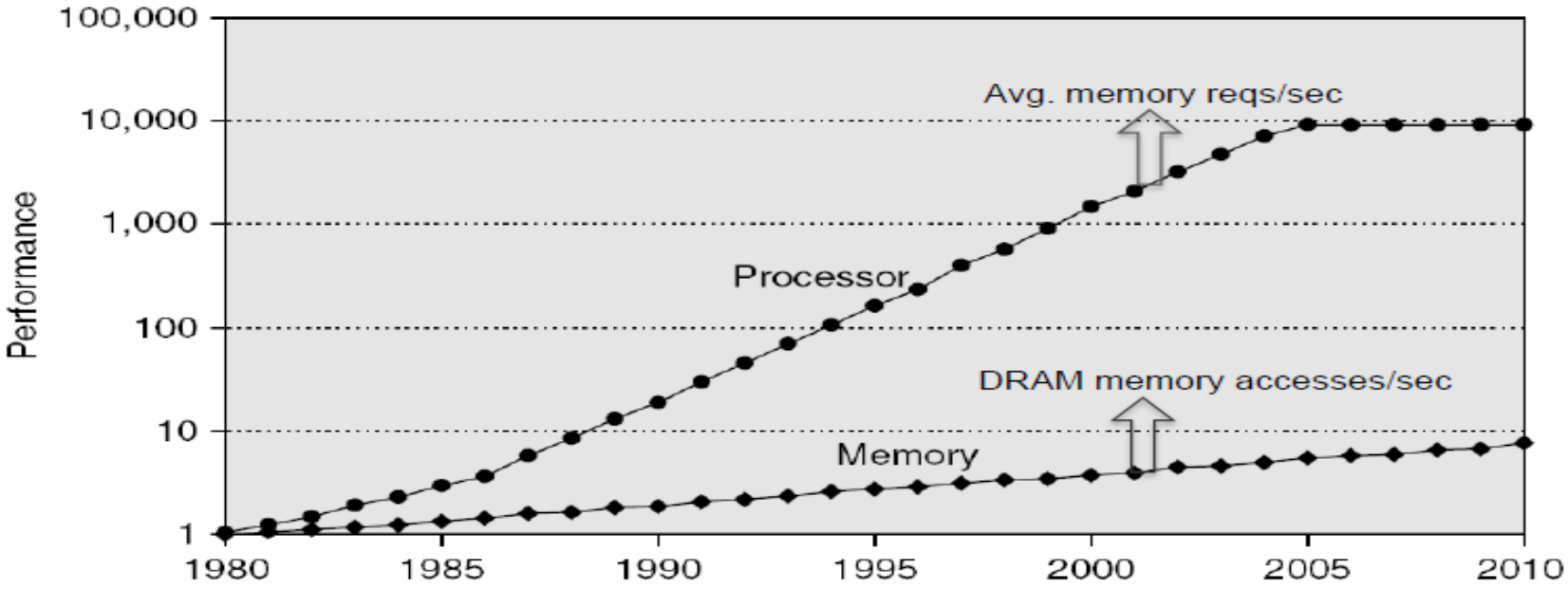
Power Wall


Power Density
mW/mm²
2000
1000
800
600
400
200
100
80
60
40
20
10
1985
1990
1995
2000
2005
2010

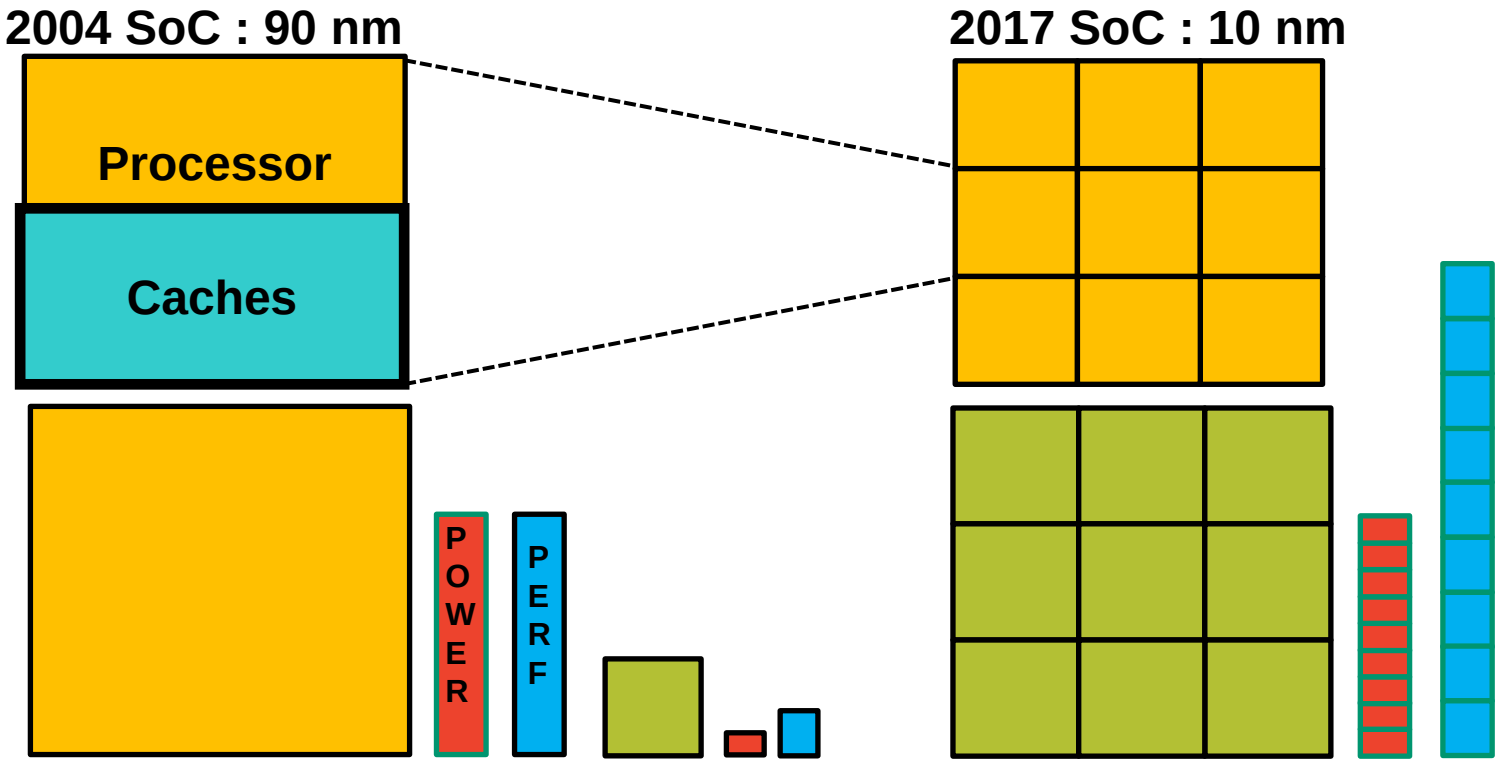
ILP Wall


relative performance/cycle
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0
1985
1987
1989
1991
1993
1995
1997
1999
2001
2003
year

Memory Wall


Performance
100,000
10,000
1,000
100
10
1
1980
1985
1990
1995
2000
2005
2010
Avg. memory reqs/sec
Processor
DRAM memory accesses/sec
Memory

Paradigm Shift to Multicore

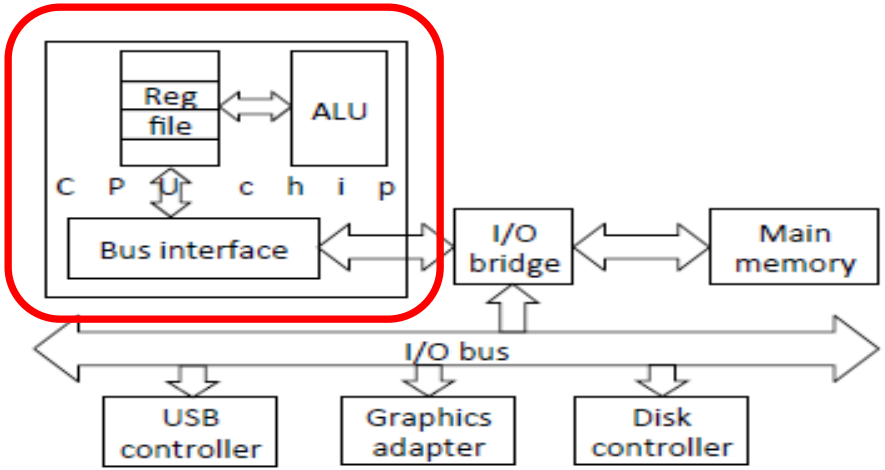


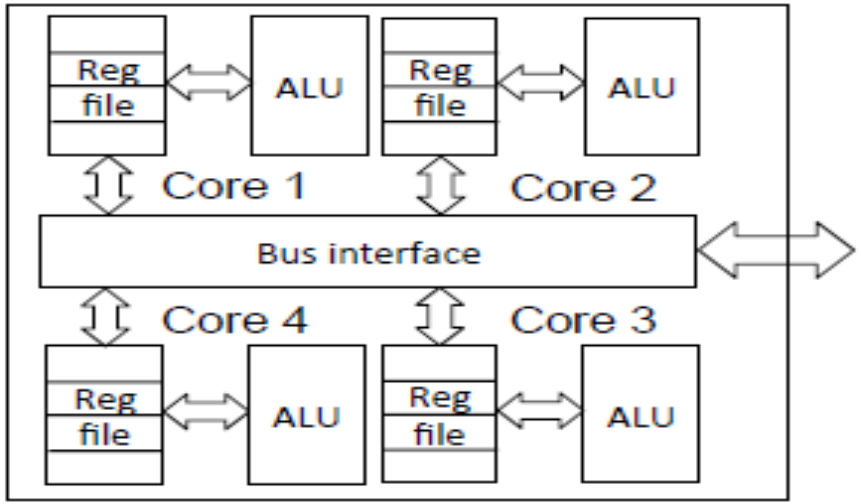
Multiple slower processors vs single fast powerful processor

Paradigm Shift to Multicore

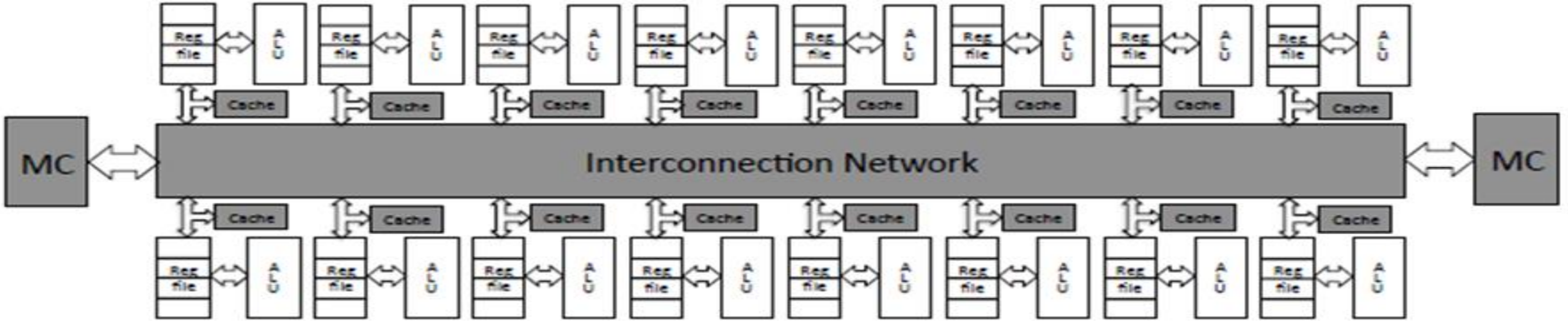
Multiple slower processors is better that single fast powerful processor

What is Multicore ?



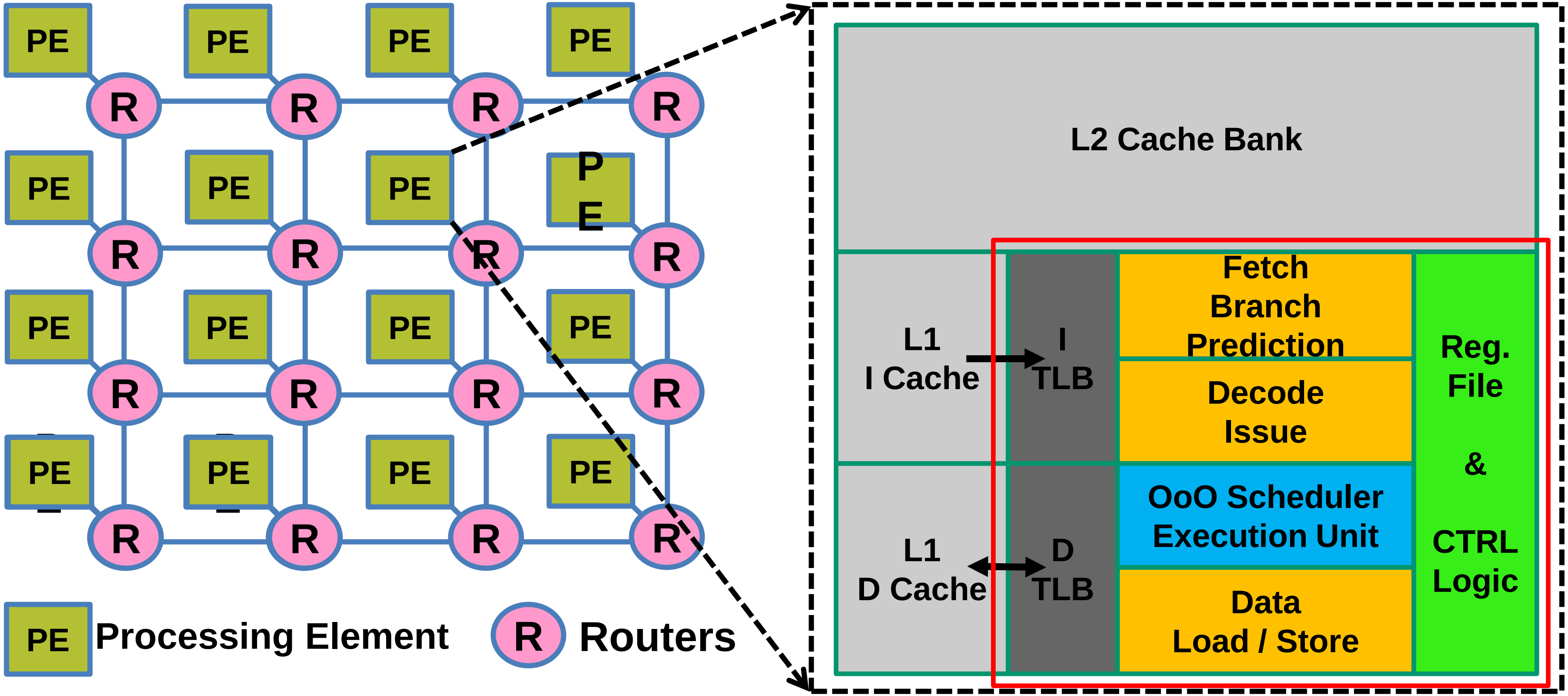


What is Multicore ?

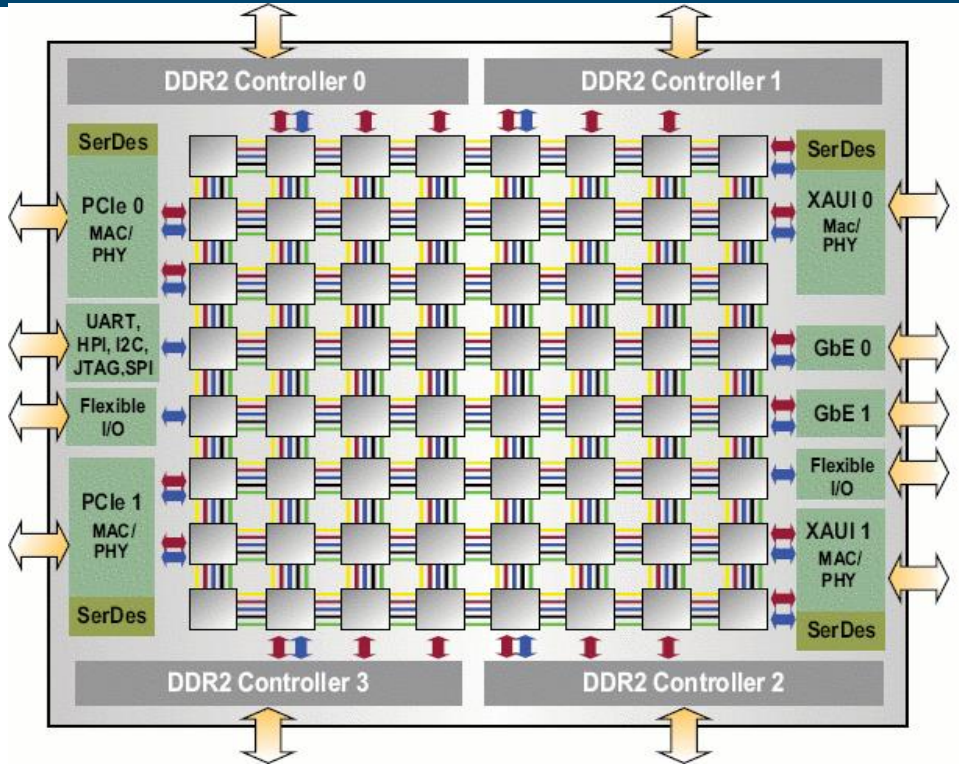


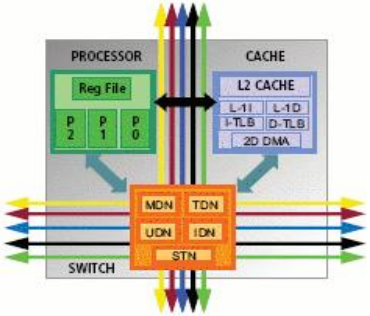
- How these cores communicate ?
- What is the best interconnection mechanism ?

Tiled Chip Many-Core Processor (TCMP)



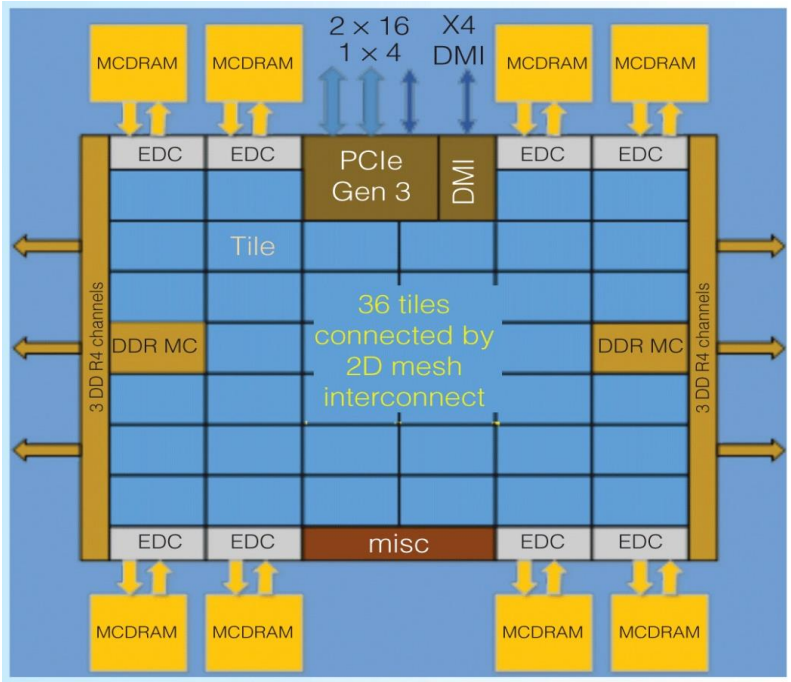
State-of-the-Art Architectures

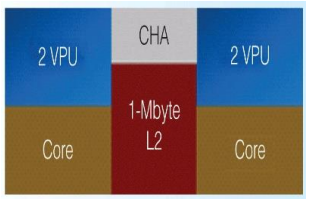




Tilera 64

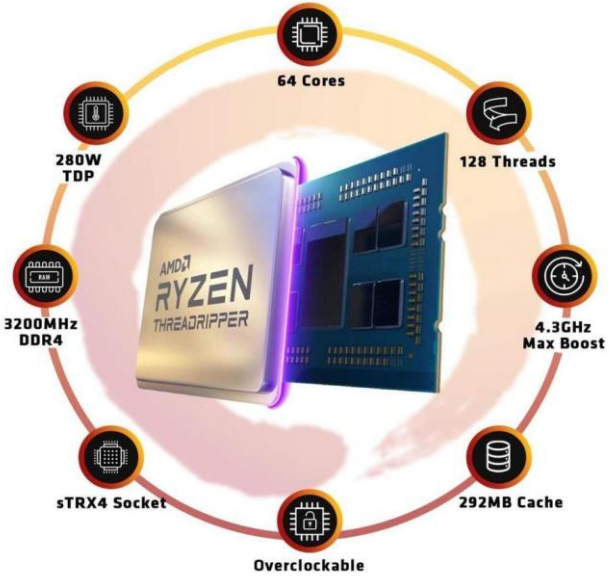
State-of-the-Art Architectures





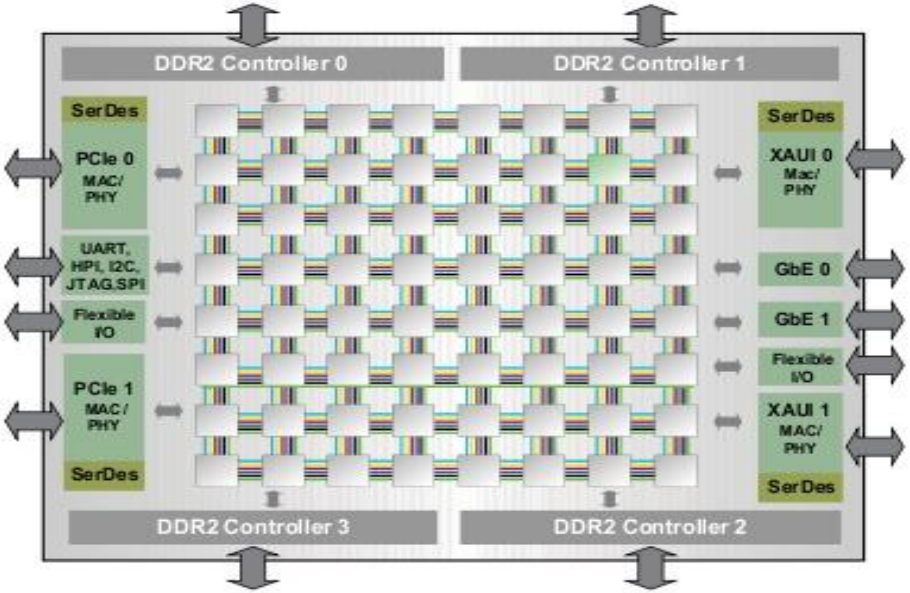
Intel KNL (Xeon PHI)

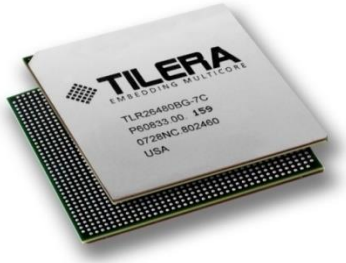
State-of-the-Art Architectures

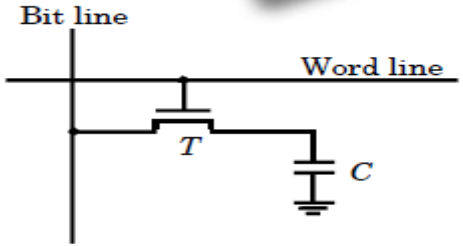


AMD RYZEN ThreadRipper

What is the role of memory controllers?

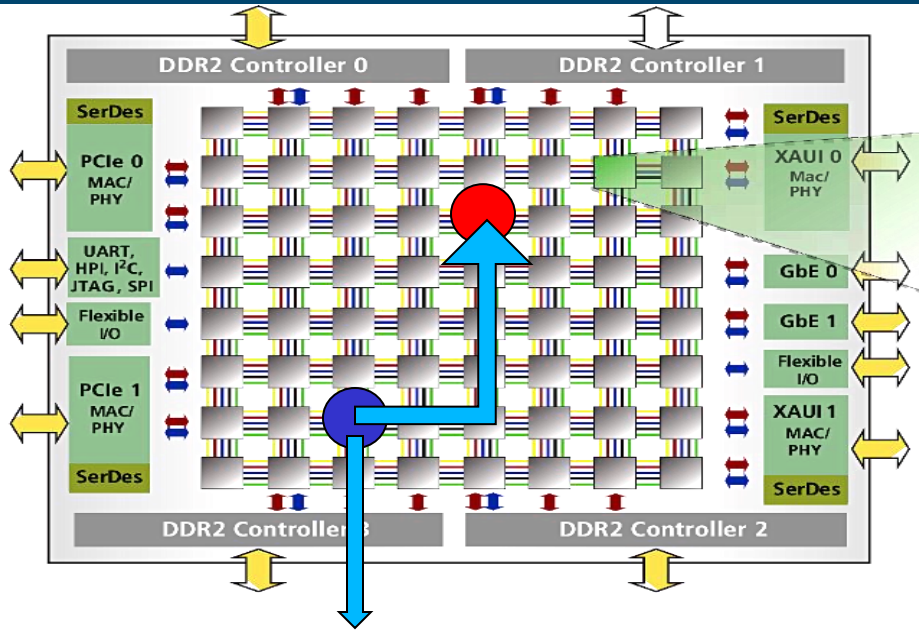


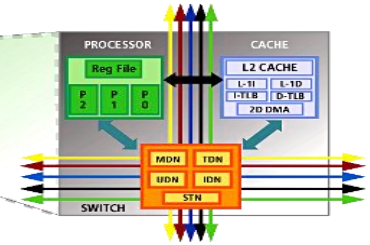




A single-transistor dynamic memory cell

On-Chip Cache Address Mapping





Per core: 512 KB

16-way set associative mapping

64 Bytes/block

Consider a 4GB RAM (2^{32}bits)

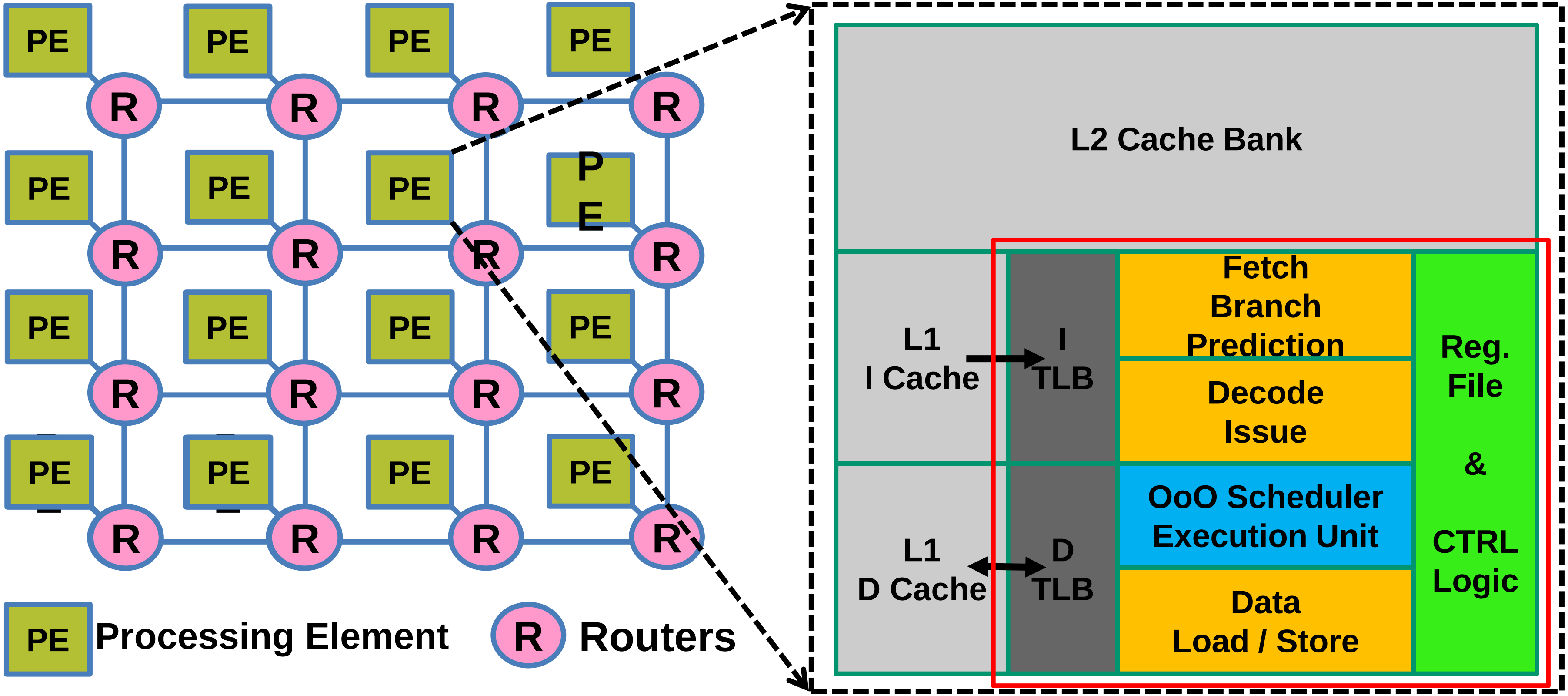
Hex Address : 0x764254

11 bits	15 bits	6 bits
Tag	Index	Block offset

00000000011	101100 100001001	010100
Tag	Index	Block offset

Core No. 44

Tiled Chip Many-Core Processor (TCMP)



Reference

- **Route Packets not wires, William J. Dally, Brian Towles**

  https://dl.acm.org/doi/10.1145/378239.379048.

- **NPTEL Video Links:**
  - https://tinyurl.com/yhclb2xd
  - https://tinyurl.com/ybwpo99z

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