CS223 : Computer Architecture & Organization

Lecture 34 [29.04.2022]

Network on Chip – Routing & Flow Control

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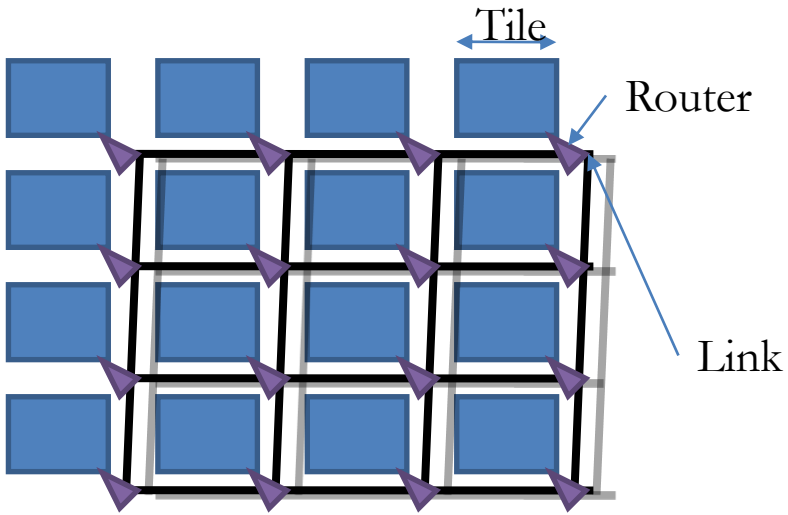
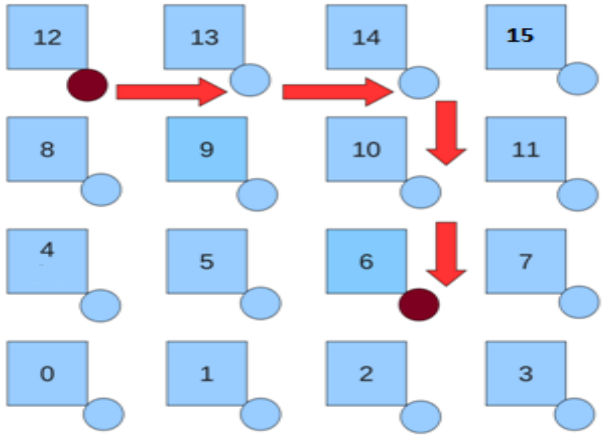
Building Blocks of NoC



- Topology
- Routing
- Flow control
- Router micro-architecture

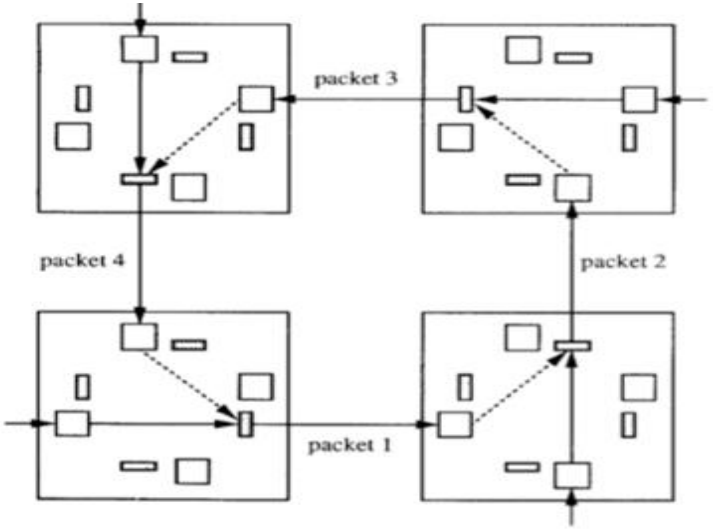
Deterministic Routing

- All packets between the same (source, dest) pair take the same path
- Dimension-order routing – Eg. XY routing
  - First traverse dimension X, then traverse dimension Y
  - Simple
  - Deadlock freedom
  - Could lead to high contention
  - Does not exploit path diversity



Deadlock

- No forward progress
- Caused by circular dependencies on resources
- Each packet waits for a buffer occupied by another packet downstream

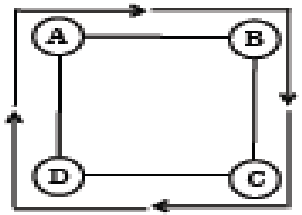


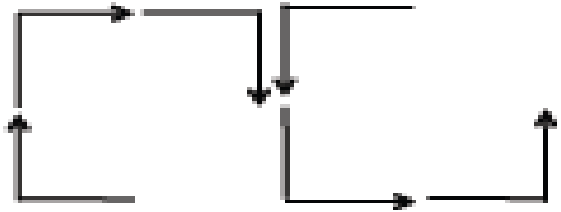
Handling Deadlock

- Avoid cycles in routing - Dimension order routing cannot build a circular dependency
- Restrict the turns each packet can take
- Avoid deadlock by adding more buffering (escape paths)
- Detect and break deadlock by preemption of buffers

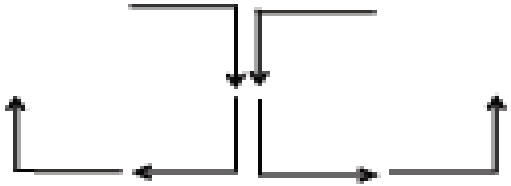
Turn Model to Avoid Deadlock

- Analyze directions in which packets can turn in the network
- Determine turns the can form cycles
- Prohibit just enough turns to break possible cycles

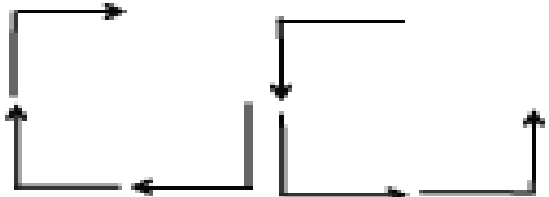




West First Turns

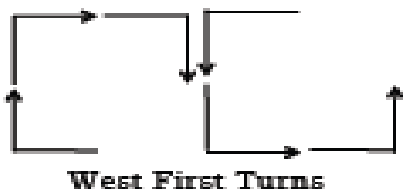


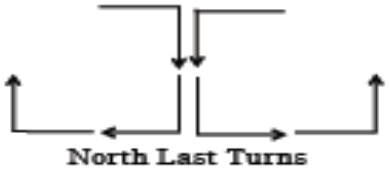
North Last Turns

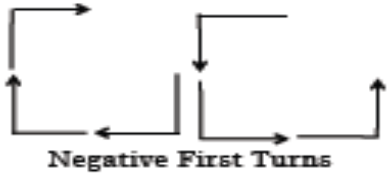


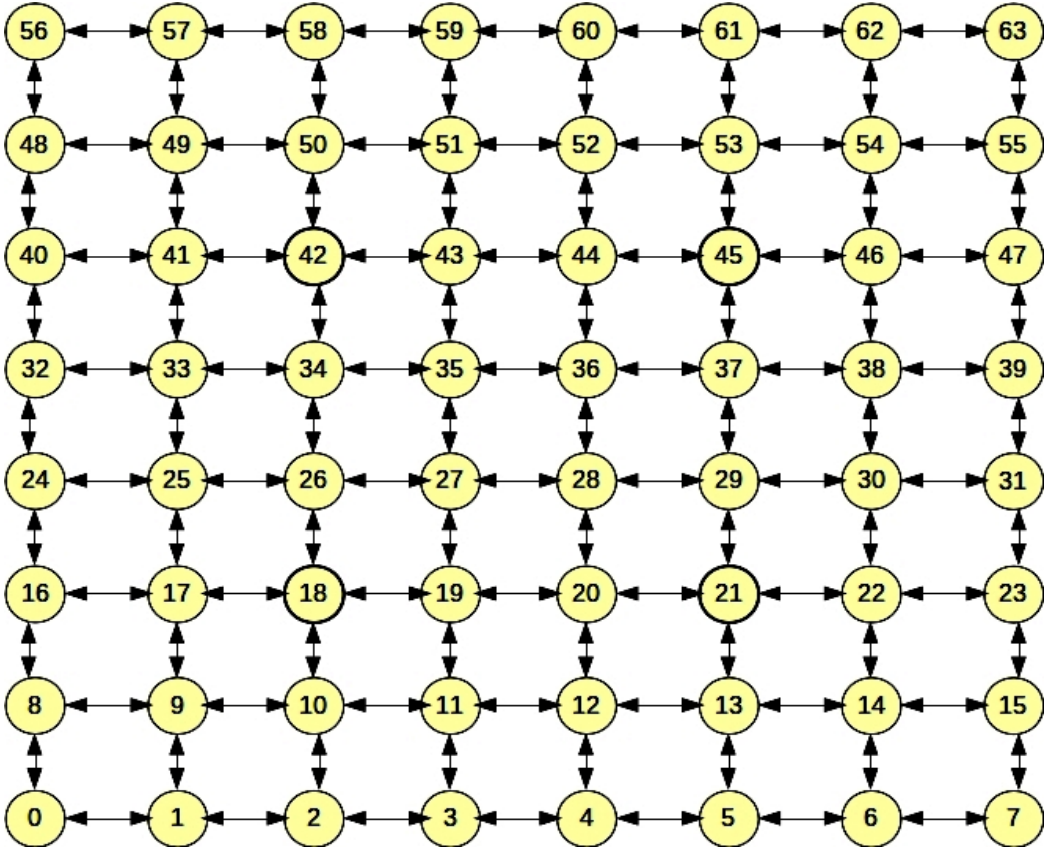
Negative First Turns

Turn Model to Avoid Deadlock

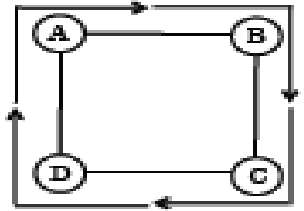






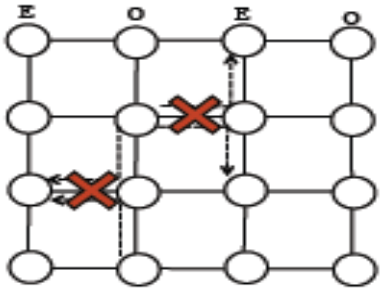


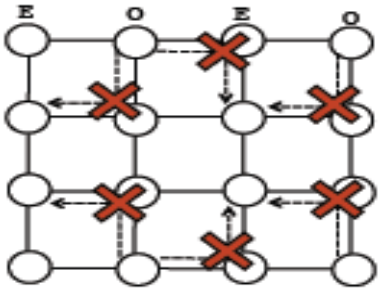
Adaptive Odd-Even Turn Routing

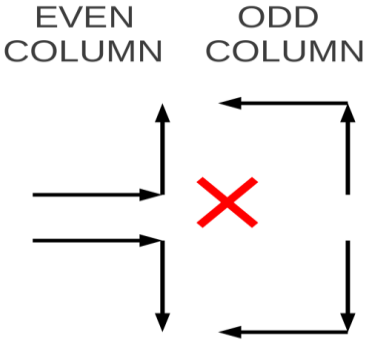


Non restrictive turns leads to deadlocks

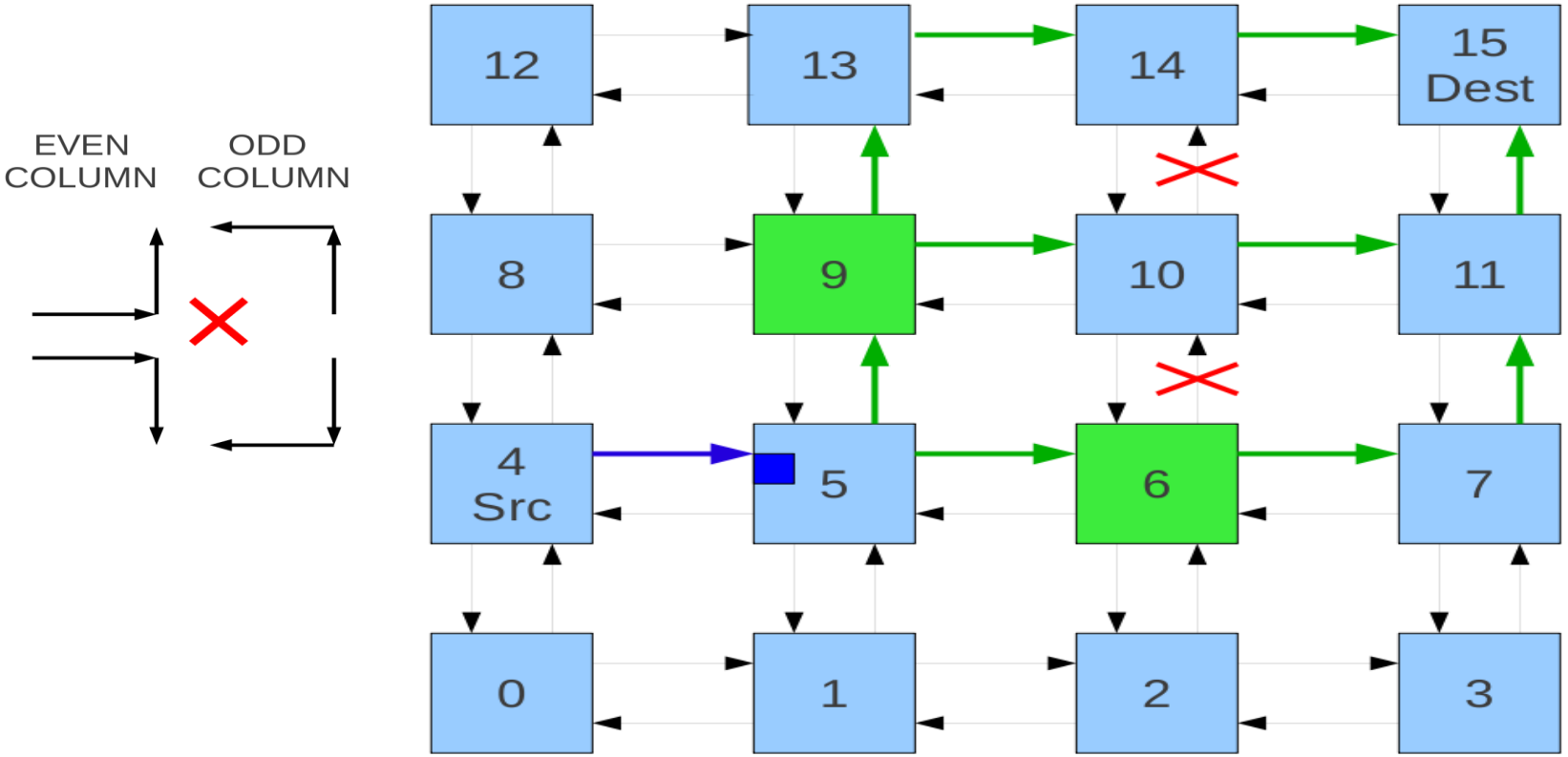
- Prohibited Turns at certain junctions
- For nodes in even column EN and ES.
- For nodes in odd column NW and SW.



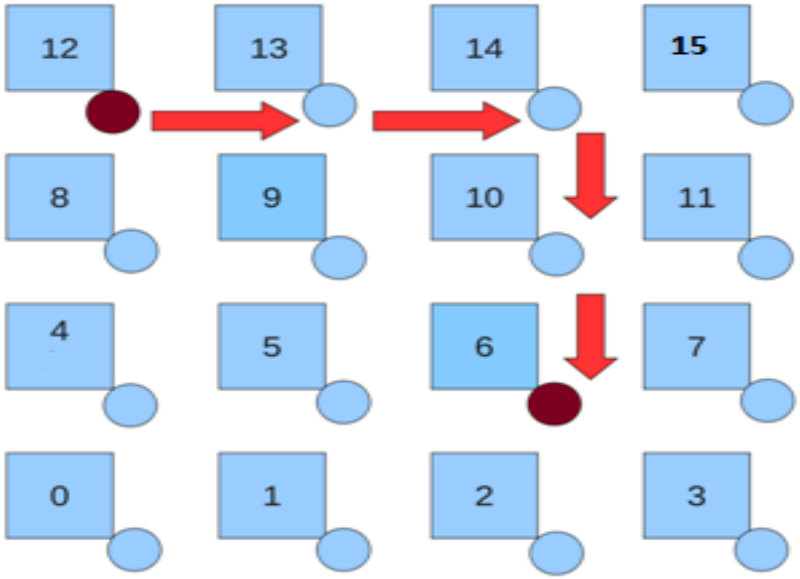




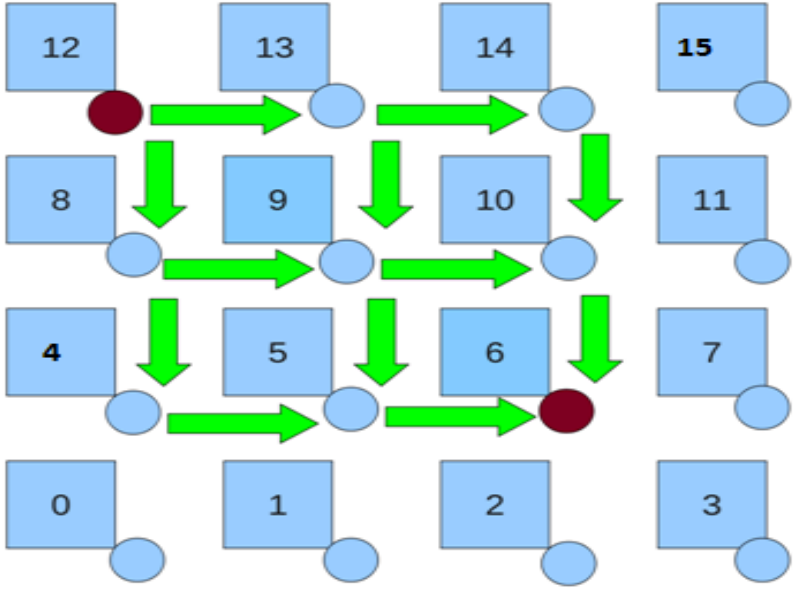
The Minimal Odd-Even Routing



Static vs Adaptive Routing

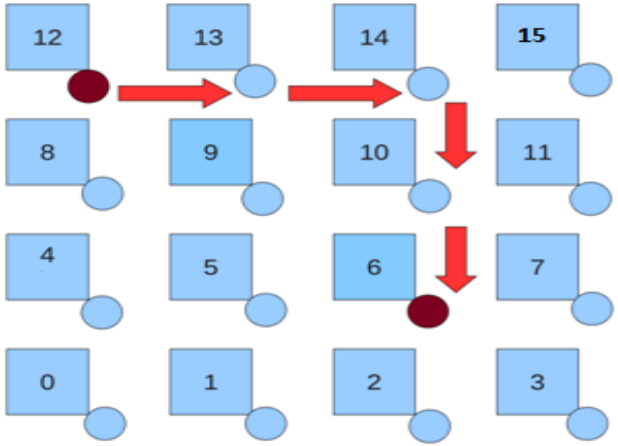


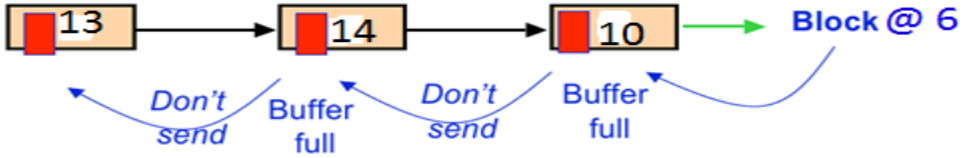
Static routing – XY routing



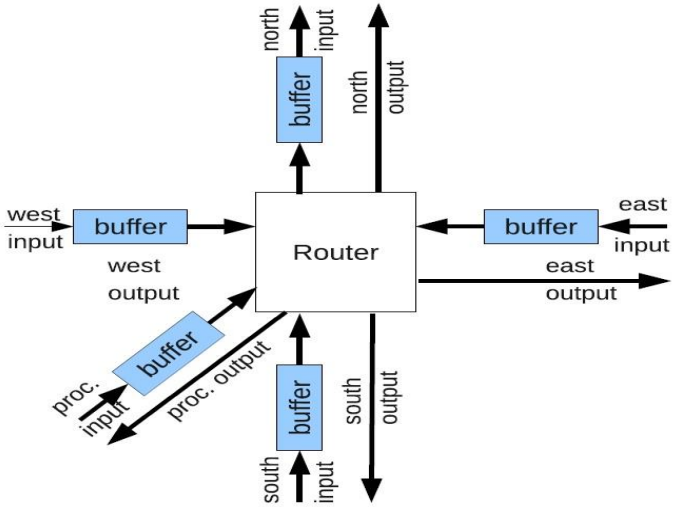
Adaptive Routing

Flow Control



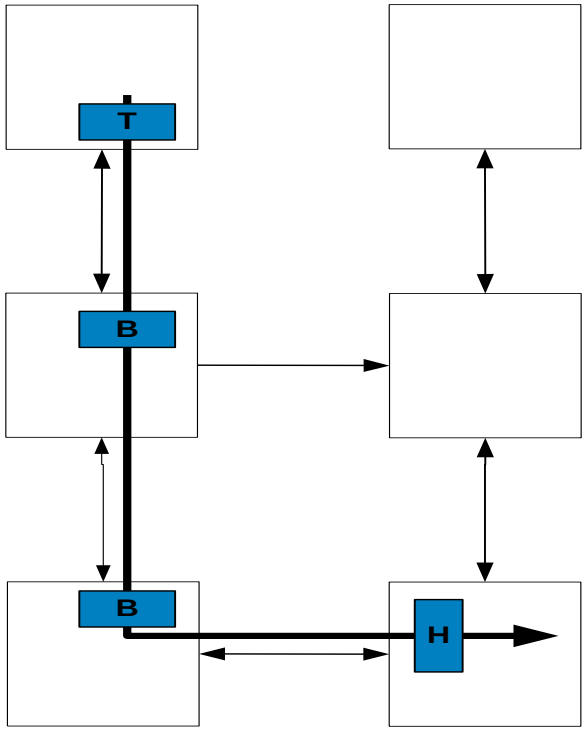


"Backpressure"



- Upstream router should know the buffer availability of downstream router.
- Credit should be exchanged between routers by handshake signals

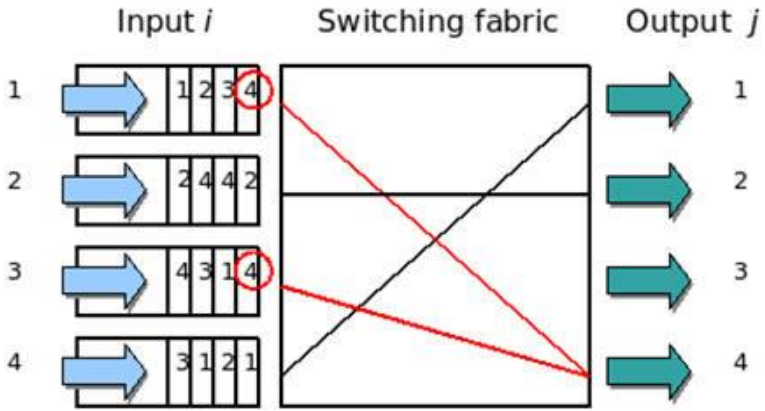
Wormhole Flow Control



- Packets broken into smaller flits
- Flits are sent across the fabric in a *wormhole fashion*
  - Body follows head, tail follows body
  - Pipelined
  - If head blocked, rest of packet stops
  - Routing (src/dest) information only in head
- Lower latency, efficient buffer utilization
- Occupies resources across multiple routers

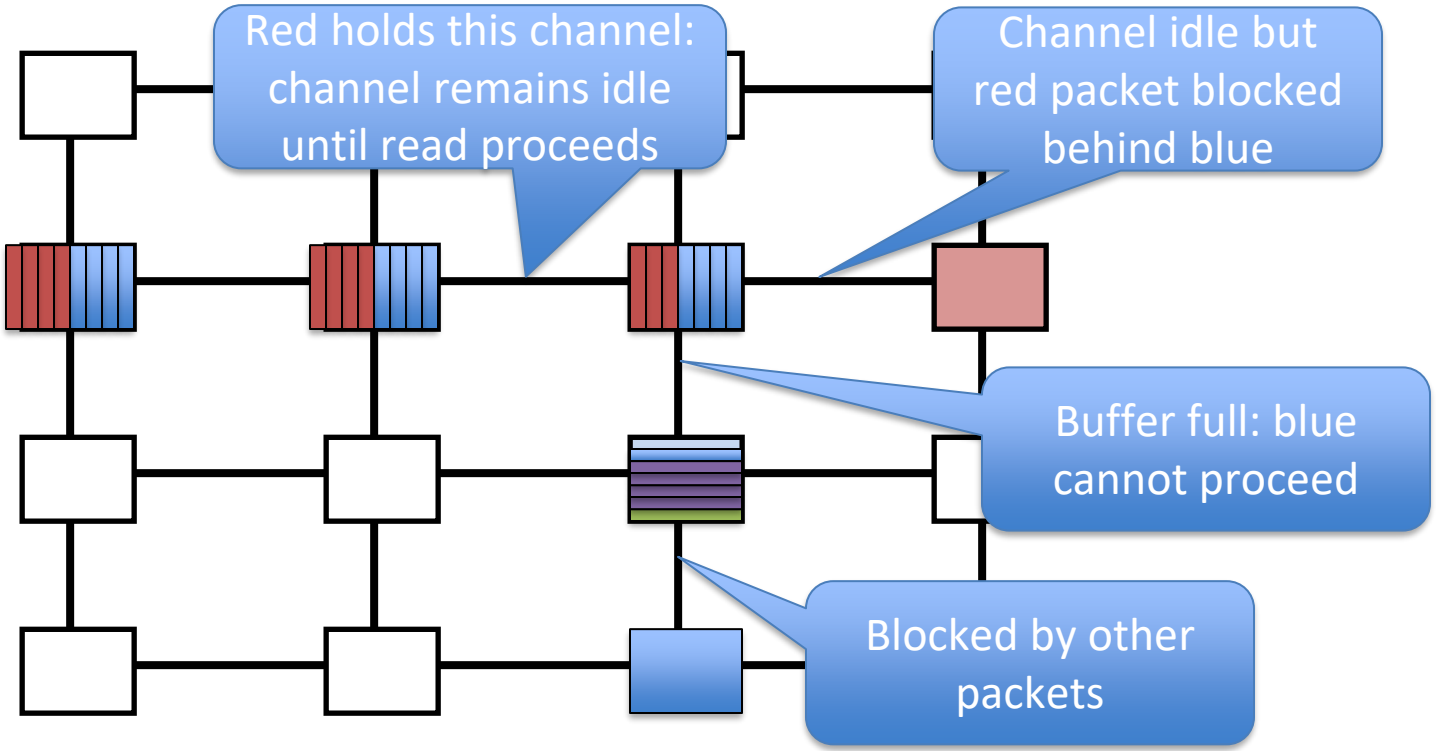
Head of Line Blocking

- Suffers from **head of line blocking**
  - If head flit cannot move due to contention, another worm cannot proceed even though links may be idle



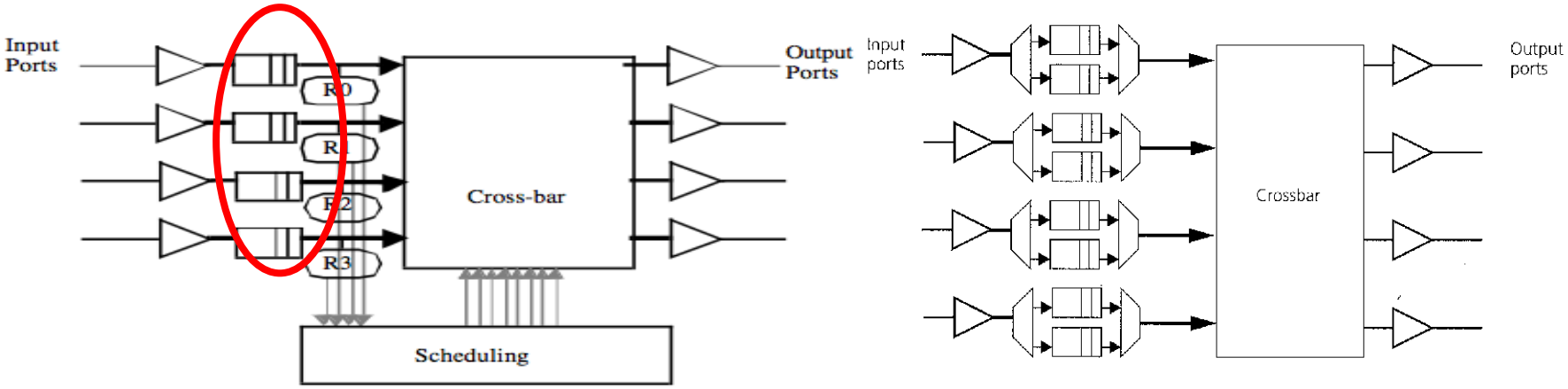
HOL Blocking

Head of Line Blocking

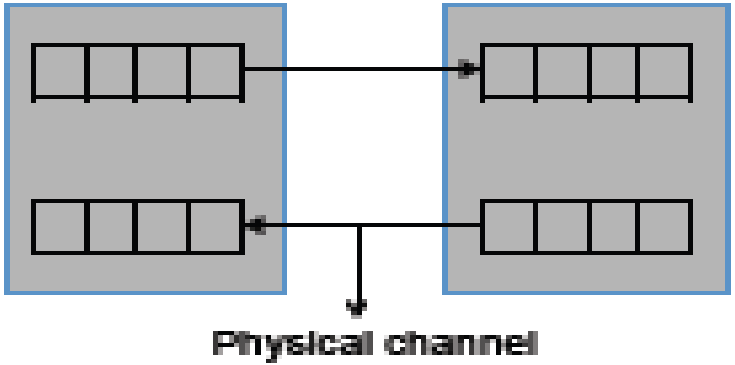


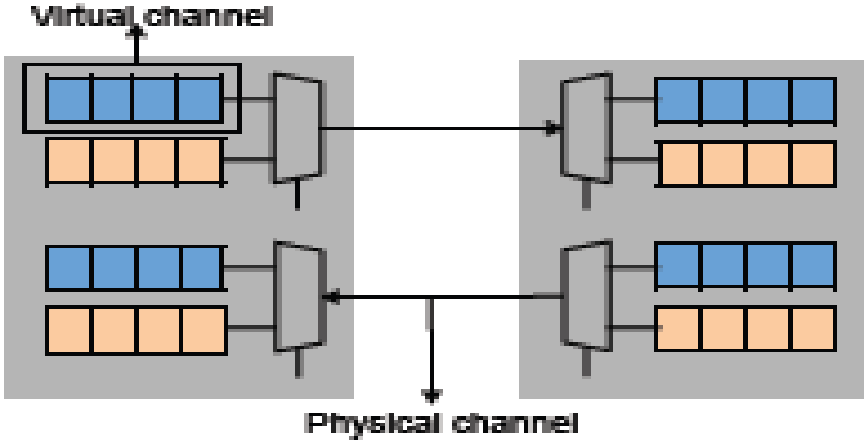
Virtual Channel Flow Control

- Multiplex multiple channels over one physical channel
- FIFO buffers replaced with multilane buffers
- Divide up the input buffer into multiple buffers sharing a single physical channel



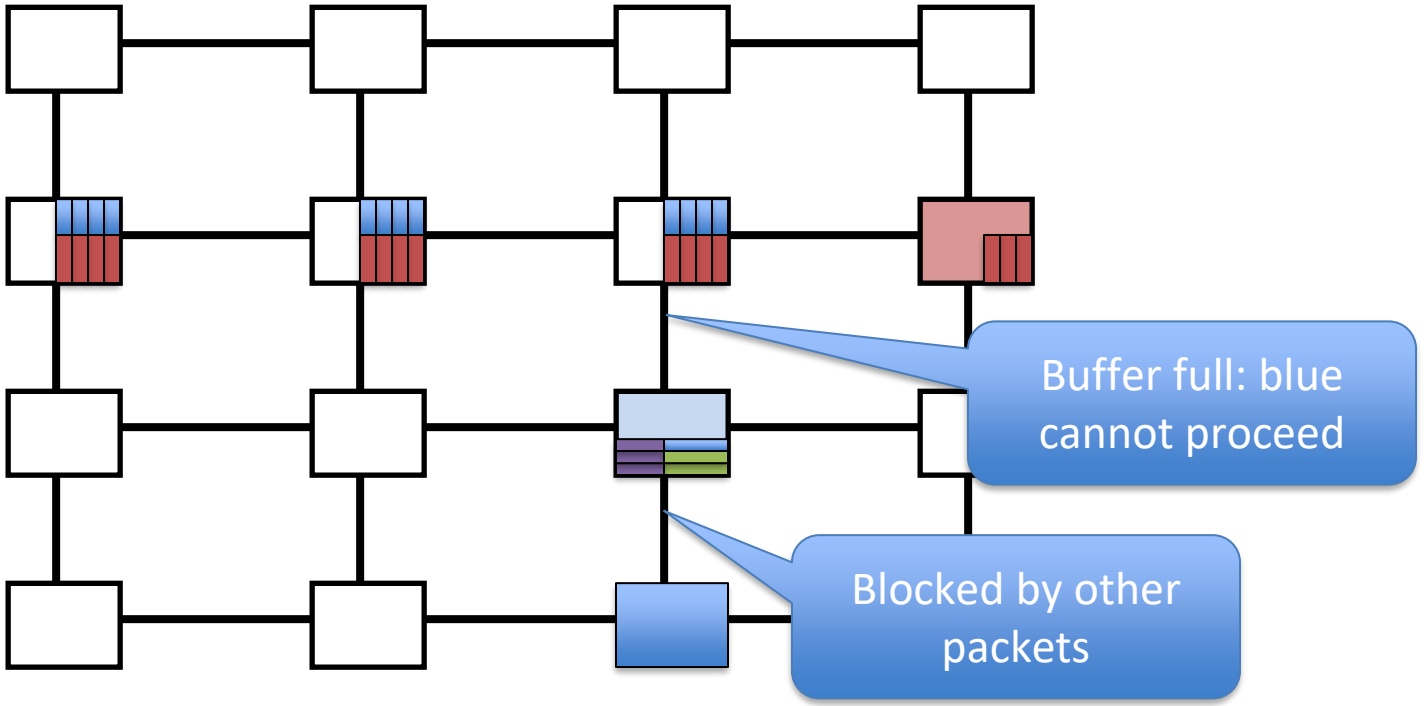
Virtual Channel Flow Control



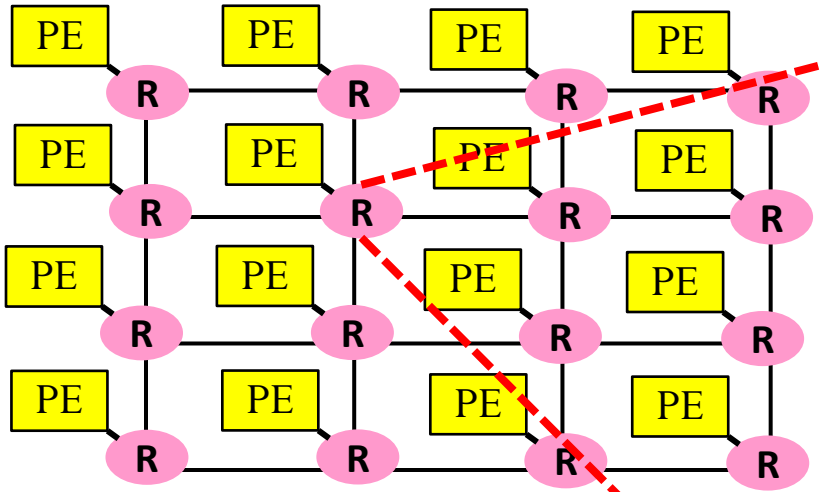


- VCs are allocated once at each router to the head flit and remaining flits of the packet inherit the same VC
- Flits of different packets can be interleaved on the same physical channel
- VCs avoid deadlocks

Virtual Channel Flow Control



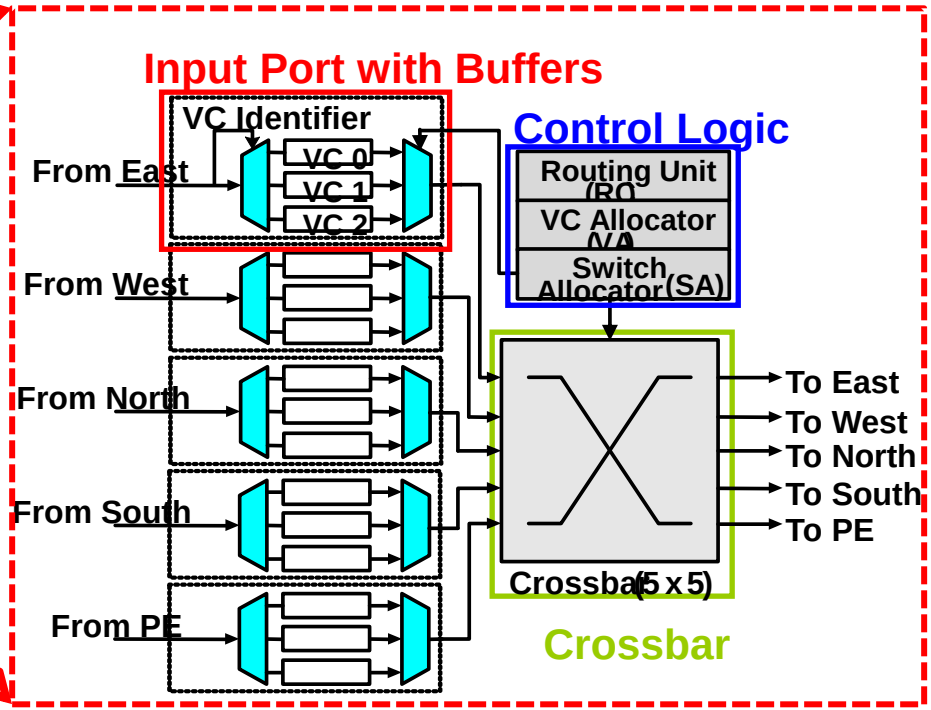
Input Buffered NoC Router



R Router

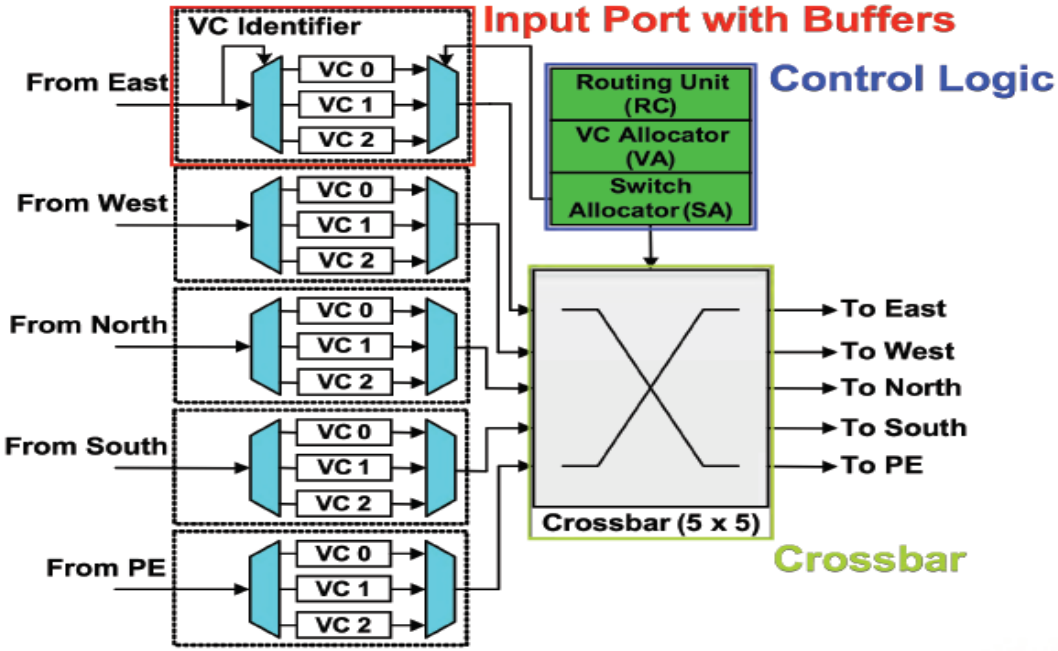
PE Processing Element

(Cores, L2 Banks, Memory Controllers etc)

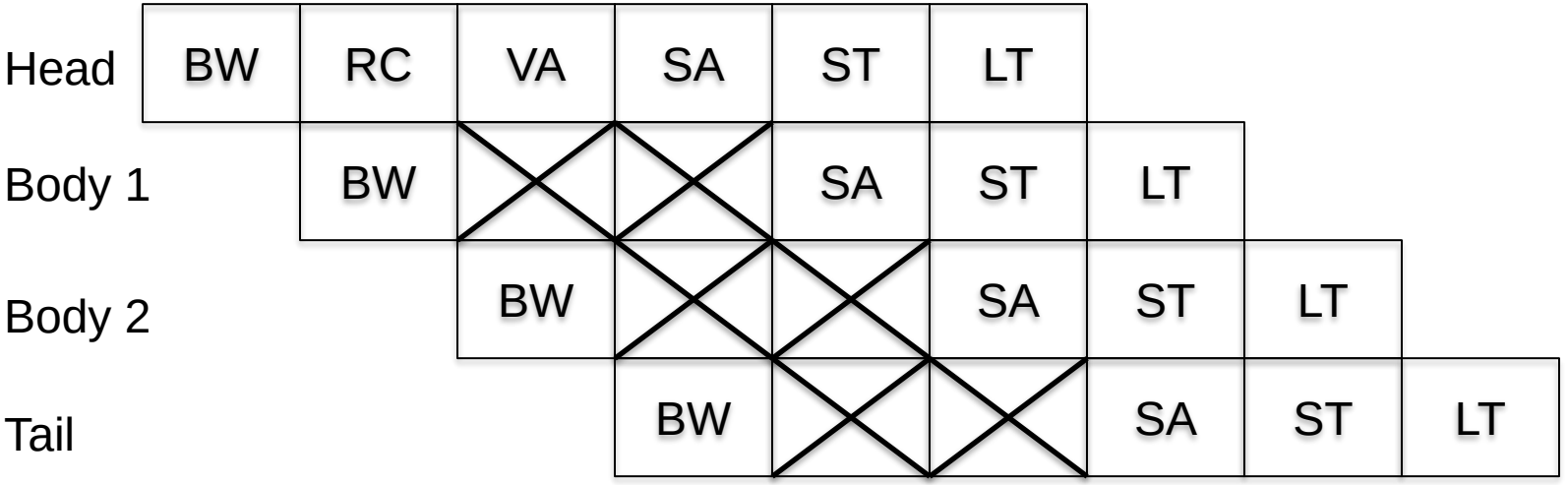


Functions of a Router

- Buffering of flits
- Route computation
- VC allocation
- Switch Allocation
- Switch Traversal
- Link Traversal



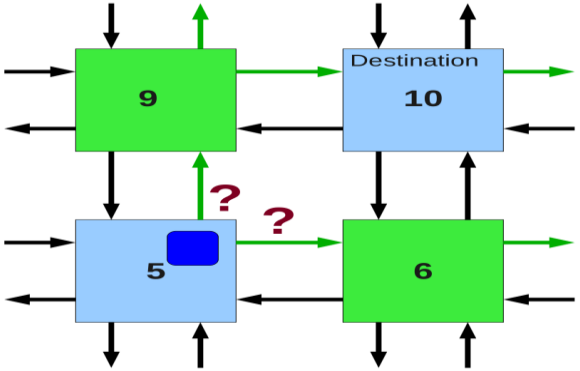
Wormhole Router Timeline

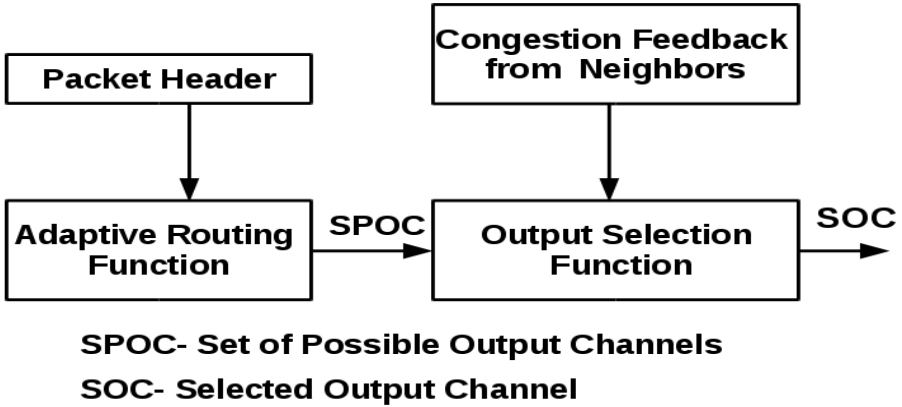


- Route computation performed once per packet
- Virtual channel allocated once per packet
- Body and tail flits inherit this information from head flit

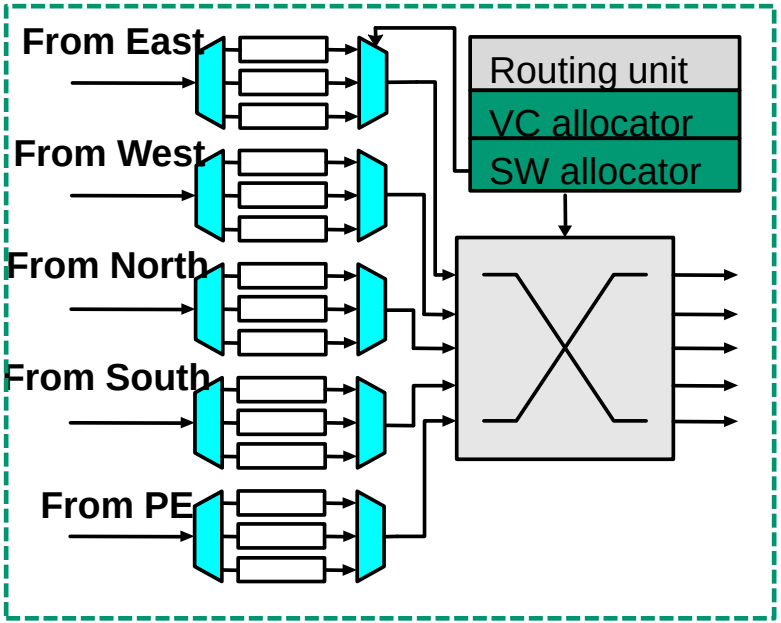
Selection Strategy

When there are multiple possible paths for a packet at a router, which one to choose ?

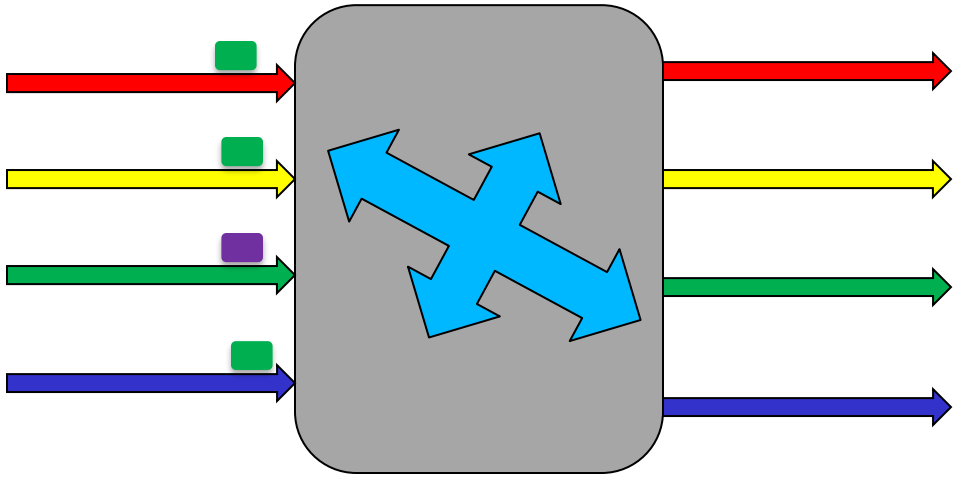




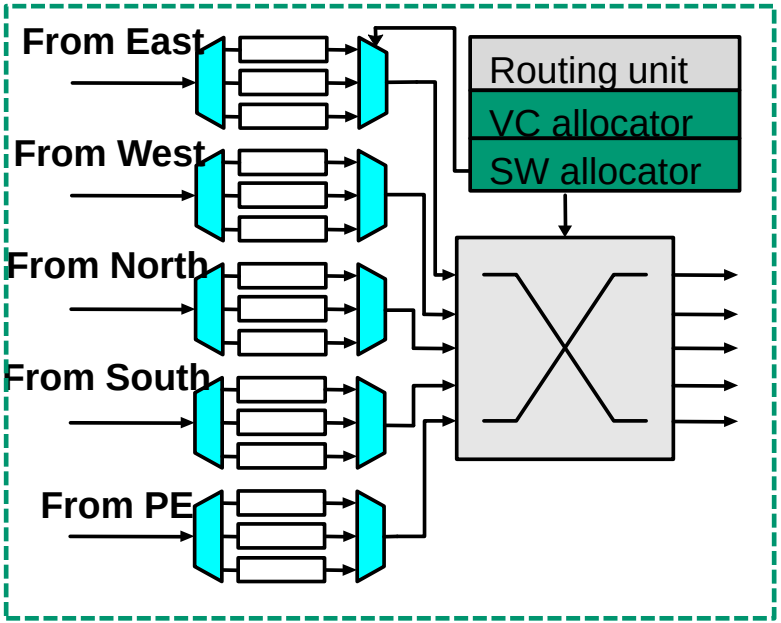
Input / Output Channel Selection



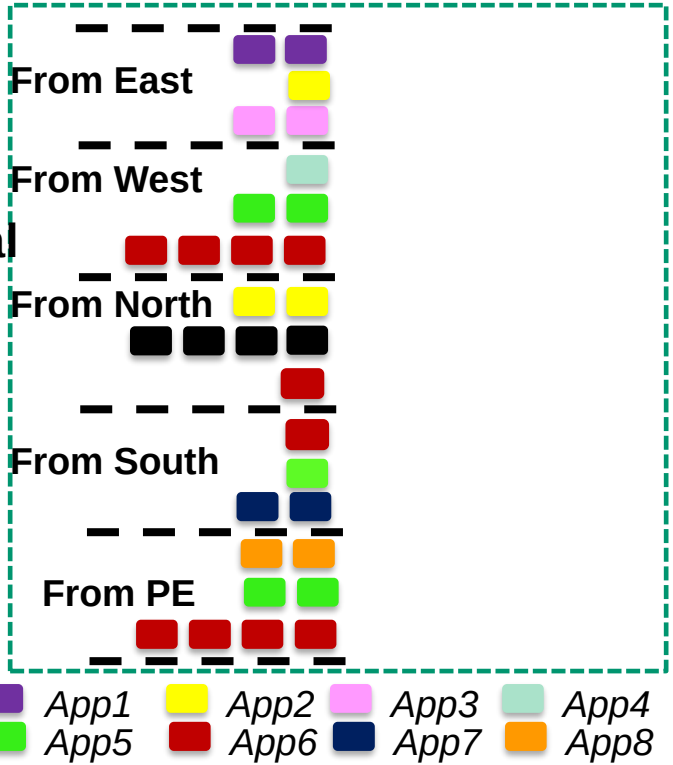
Output Channel Selection
Input Channel Selection



Switch Level Packet Scheduling in NoC



Conceptual View



Reference

- **Route Packets not wires, William J. Dally, Brian Towles**

  https://dl.acm.org/doi/10.1145/378239.379048.

- **NPTEL Video Links:**
  - **https://tinyurl.com/ybwpo99z**
  - **https://tinyurl.com/yjq85rym**
  - **https://tinyurl.com/yhclb2xd**

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