CS 223 Computer Architecture and Organization

CPU Registers

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Components of Computer

- The Control Unit and the Arithmetic and Logic Unit constitute the Central Processing Unit (CPU)

- CPU has temporary storage space - Registers

- Data and instructions need to get into the system and results out

  – Input/output

- Temporary storage of code and results is needed

  – Main memory

Connecting

- All the units must be connected
- Different type of connection for different type of unit
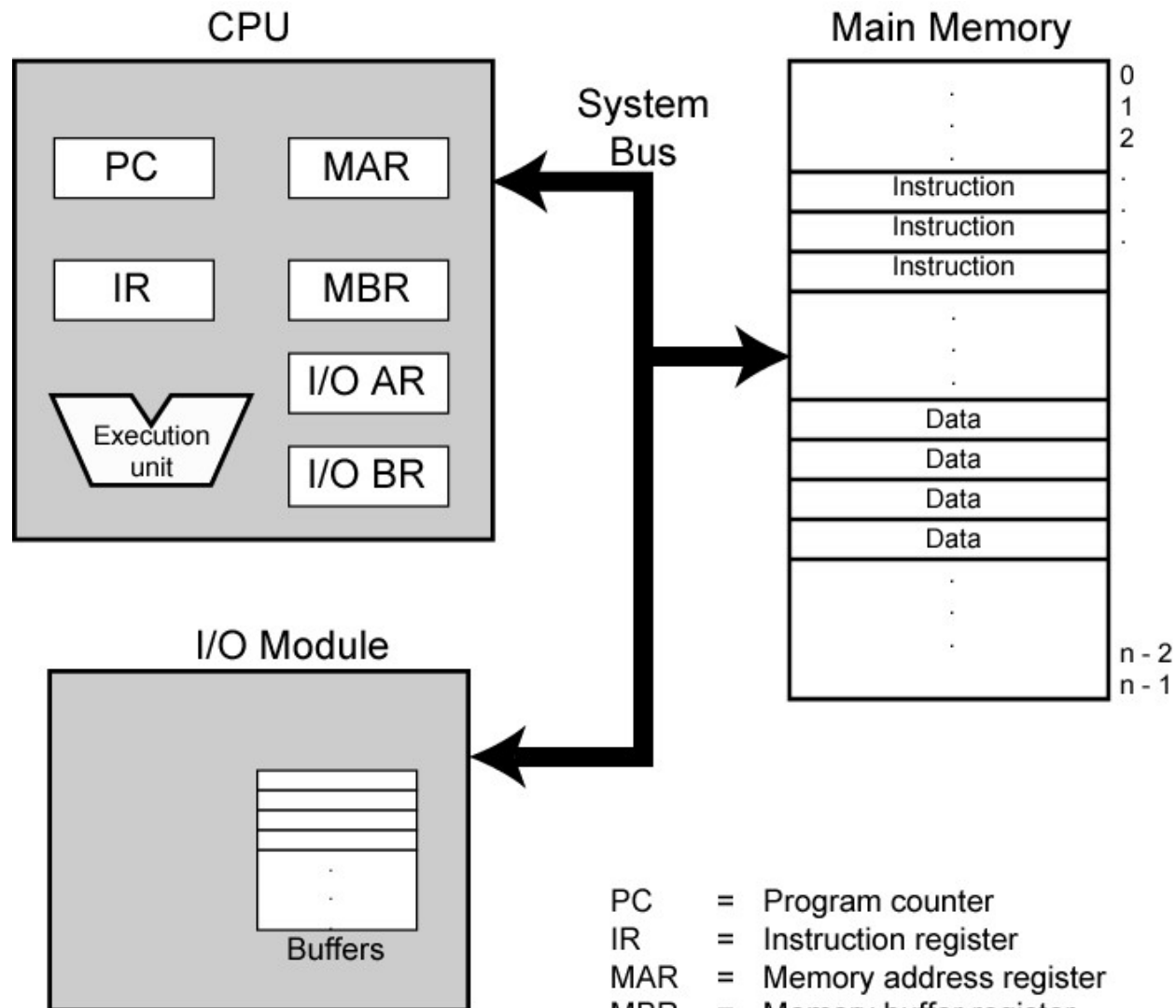 - Memory
  - Input/Output
  - CPU

Memory Connection

- Receives and sends data

- Receives addresses (of locations)

- Receives control signals
  - Read
  - Write
 - Timing

Input/Output Connection

- Similar to memory from computer's viewpoint

- Output

  – Receive data from computer

  – Send data to peripheral

- Input

  – Receive data from peripheral

  – Send data to computer

Computer Components: Top Level View

CPU

| PC | MAR |

| IR | MBR |

| | I/O AR |

Execution unit

| | I/O BR |

System Bus

Main Memory

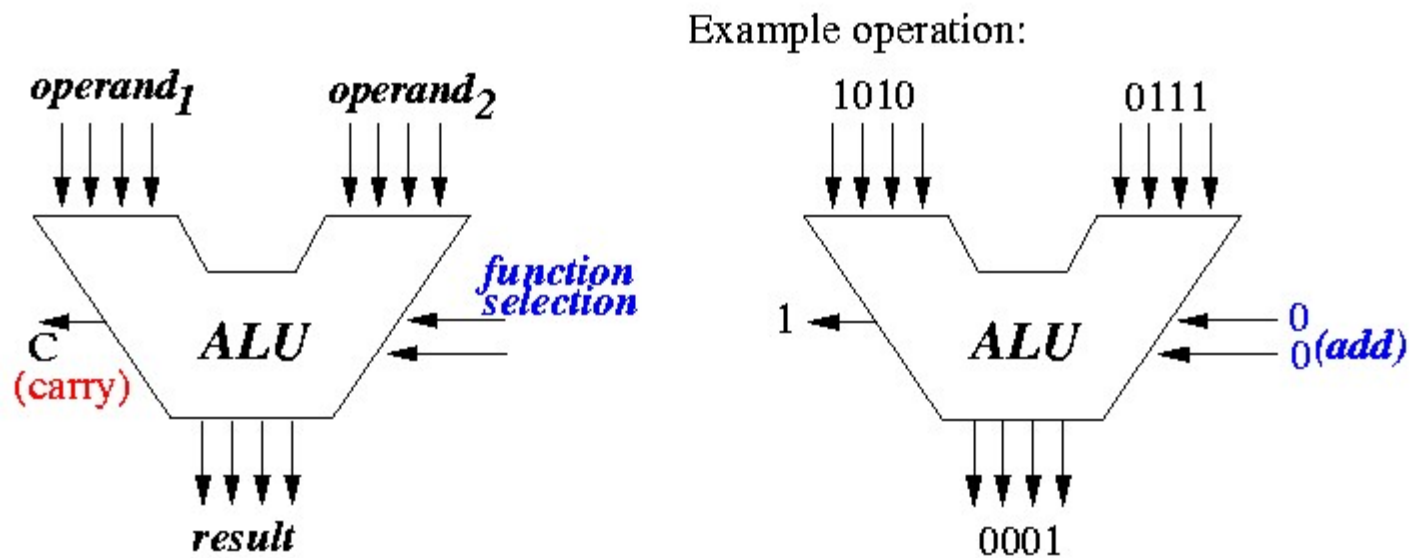| | 0 |
	1
	2
Instruction	
Instruction	
Instruction	
Data	
Data	
Data	
Data	
	n - 2
	n - 1

I/O Module

Buffers

PC = Program counter
IR = Instruction register
MAR = Memory address register
MBR = Memory buffer register
I/O AR = Input/output address register
I/O BR = Input/output buffer register

CPU Internal Structure
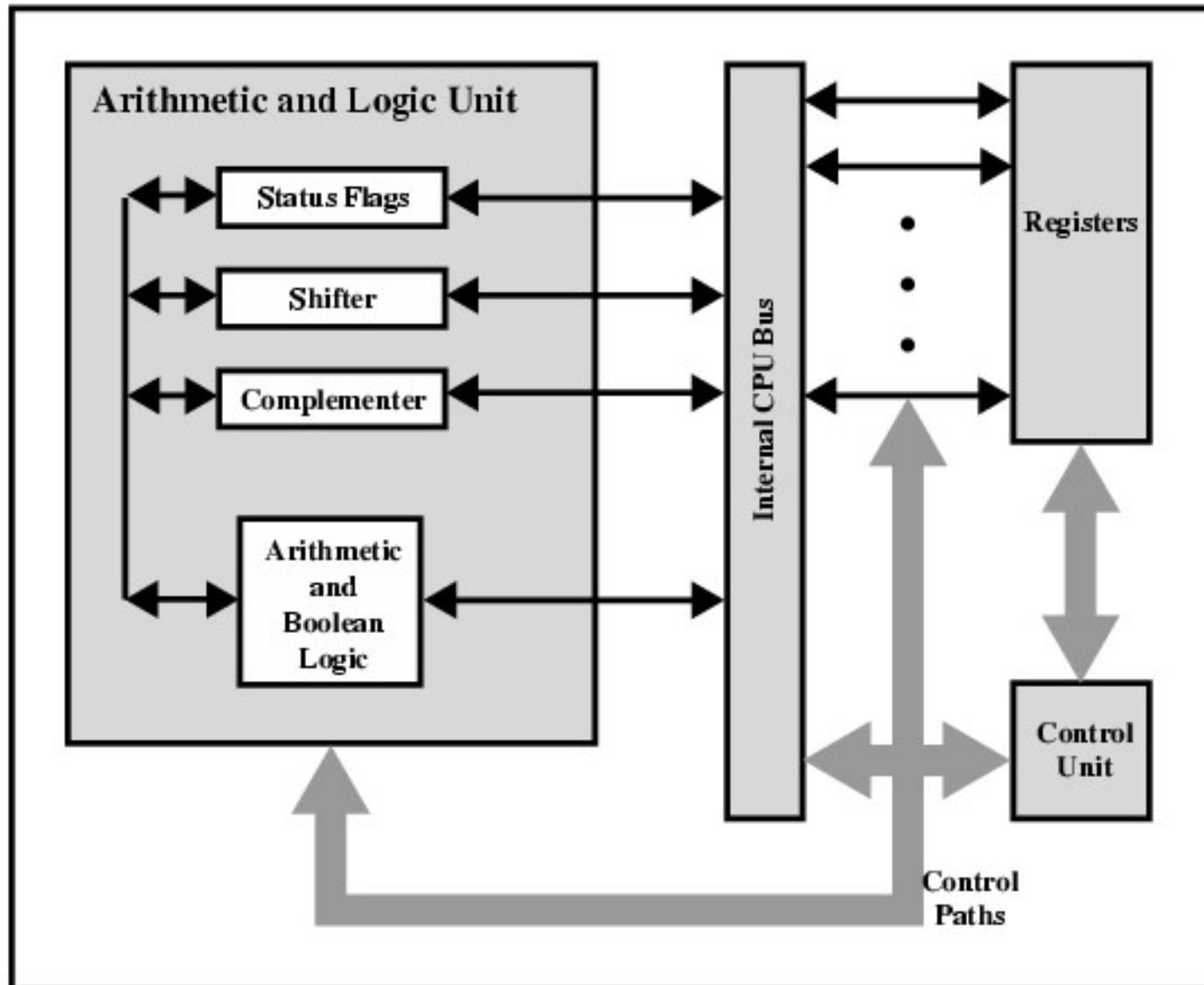
ALU

- ALU: Arithmetic and Logic Unit

Registers

- CPU must have some working space (temporary storage)

- Called registers

- Number and function vary between processor designs

- One of the major design decisions

- Top level of memory hierarchy

User Visible Registers

- General Purpose

- Data

- Address

- Condition Codes

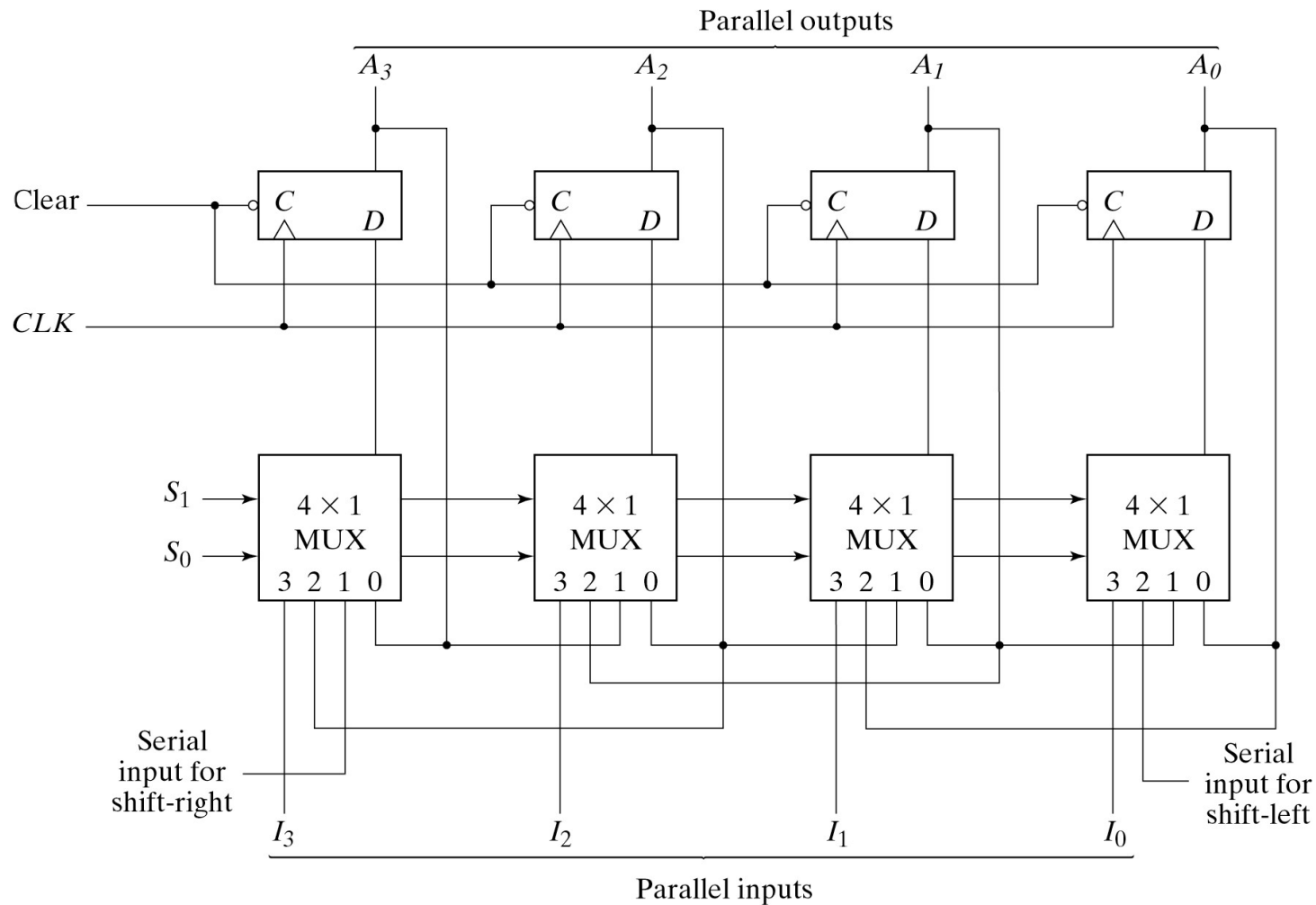# Universal Shift Register

Fig. 6-7 4-Bit Universal Shift Register

How Many GP Registers?

- Between 8 - 32
- Fewer = more memory references
- More does not reduce memory references and takes up processor space
- Large enough to hold full address
- Large enough to hold full word
- Often possible to combine two data registers
  - C programming
  - double int a;
  - long int a;

Control & Status Registers

- Program Counter

- Instruction Decoding Register

- Memory Address Register

- Memory Buffer Register

Condition Code Registers

- Sets of individual bits
  - e.g. result of last operation was zero
- Can be read (implicitly) by programs
  - e.g. Jump if zero
- Can not (usually) be set by programs
- Needs for conditional instructions

Condition Code Registers

- Sets of individual bits
  - e.g. result of last operation was zero

For example:

```
for (i=10; i > 0; i--)
        a[i] = a[i]+10;
```

next instruction

Program Status Word

- A set of bits (Flag bits)

- Includes Condition Codes

- Sign of last result

- Zero

- Carry

- Equal

- Overflow

- Interrupt enable/disable

- Supervisor

Program Status Word

- Condition Flag Bits (Depends on ALU Operation)

  – Sign, Zero, Carry, Equal, Overflow

- Flag bits set by programmer

  – Interrupt enable/disable

  – Supervisor

X	Sup	IE	OV	E	C	Z	S

Reference

Computer Organization and Architecture –
                Designing for Performance
        William Stallings

Chapter 12: Page no. 418 – 423 (Seventh Edition)
                Page No.: 435 – 440 (Eighth Edition)

Discussion

Discussion