CS 223 Computer Architecture and Organization

Main Memory

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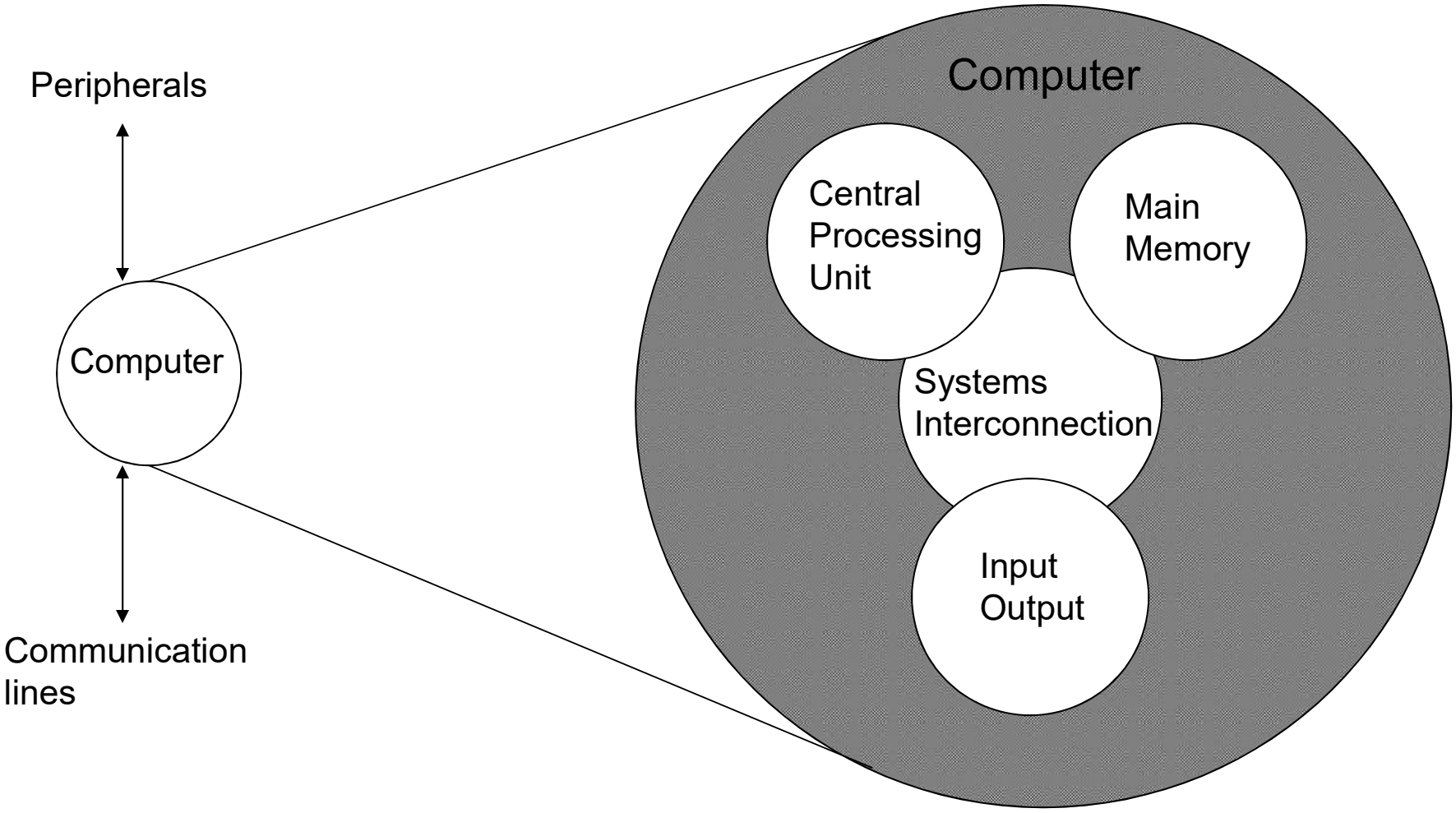
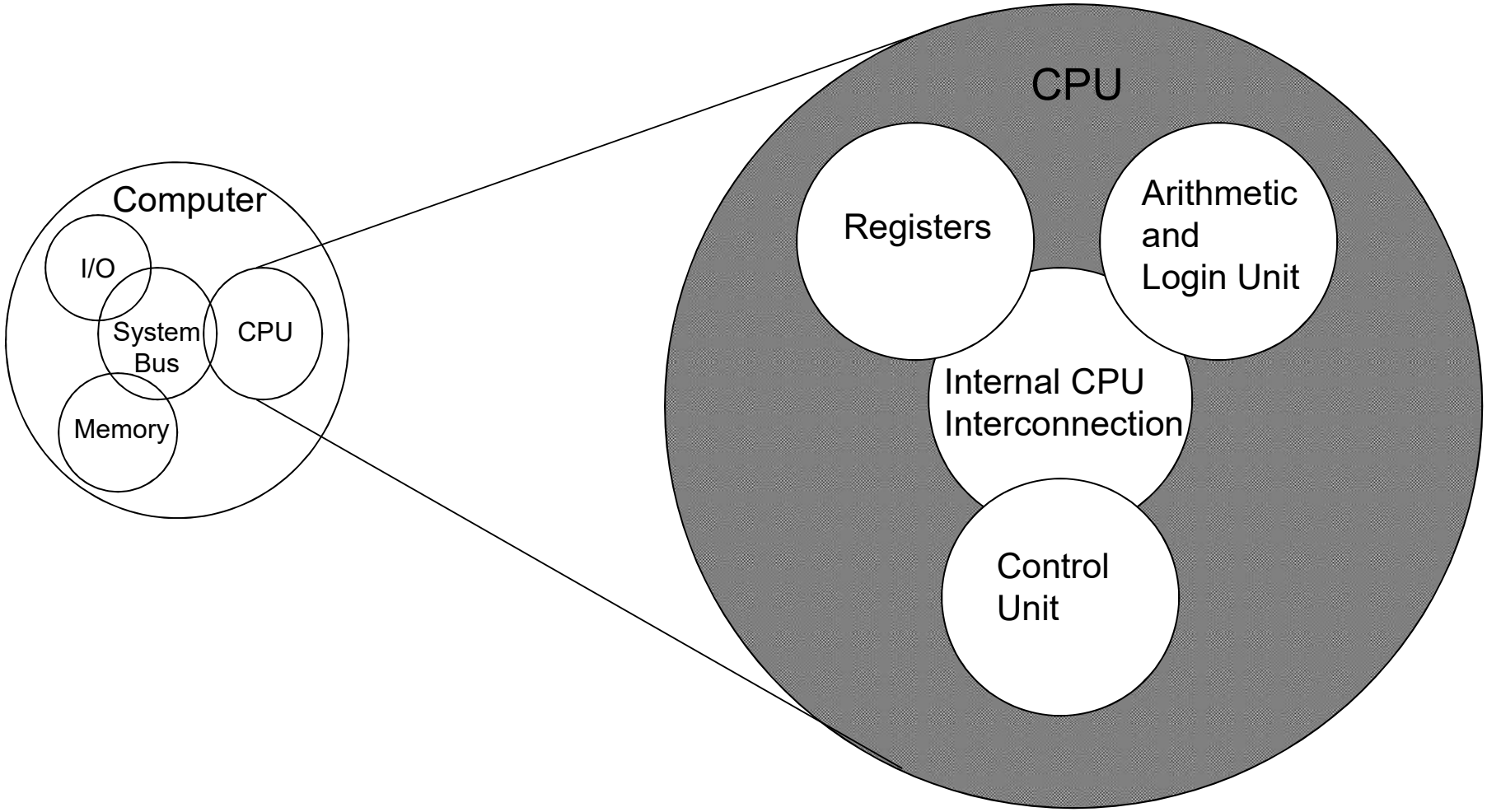
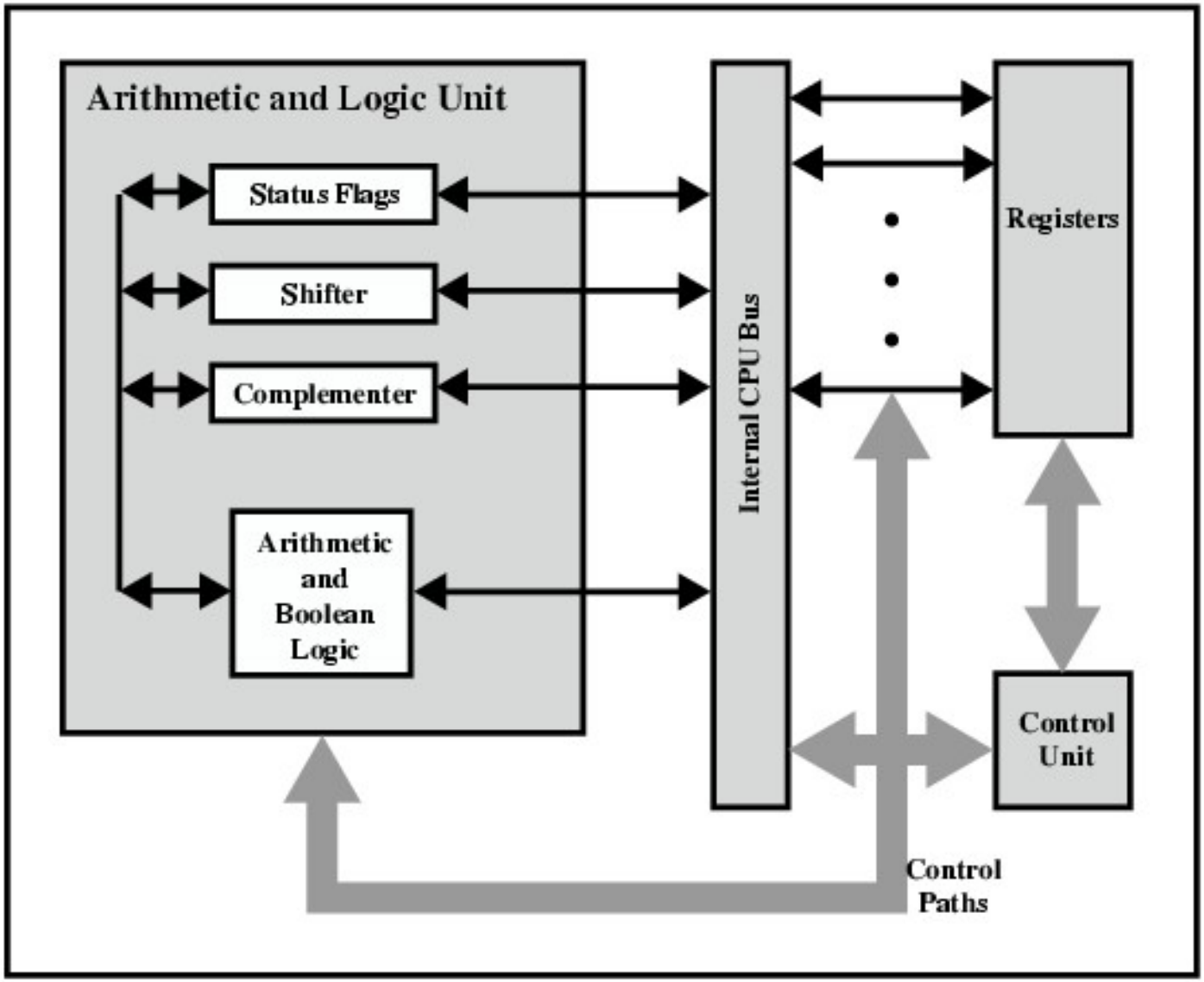
Structure - Top Level



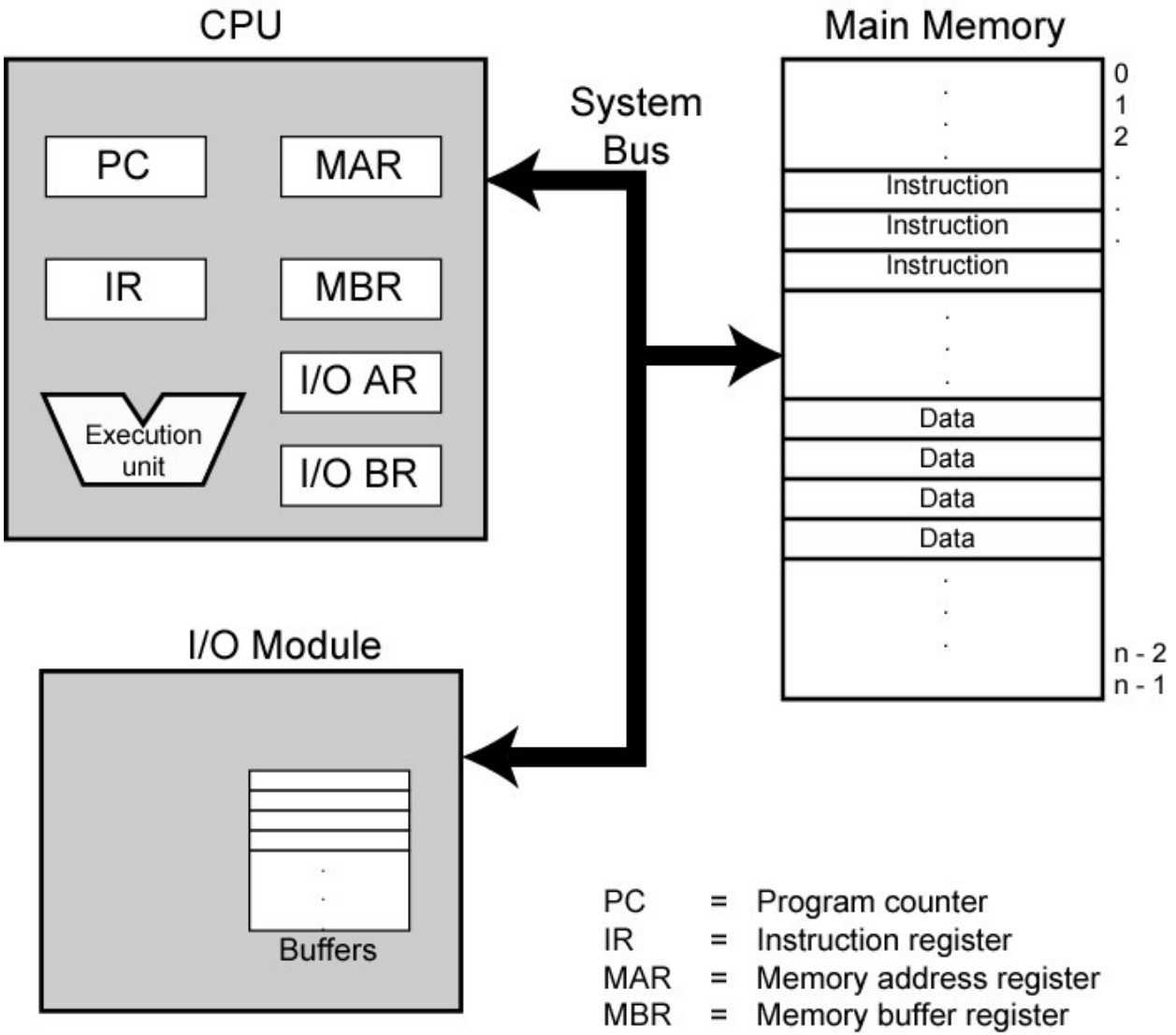
Structure - The CPU



CPU Internal Structure



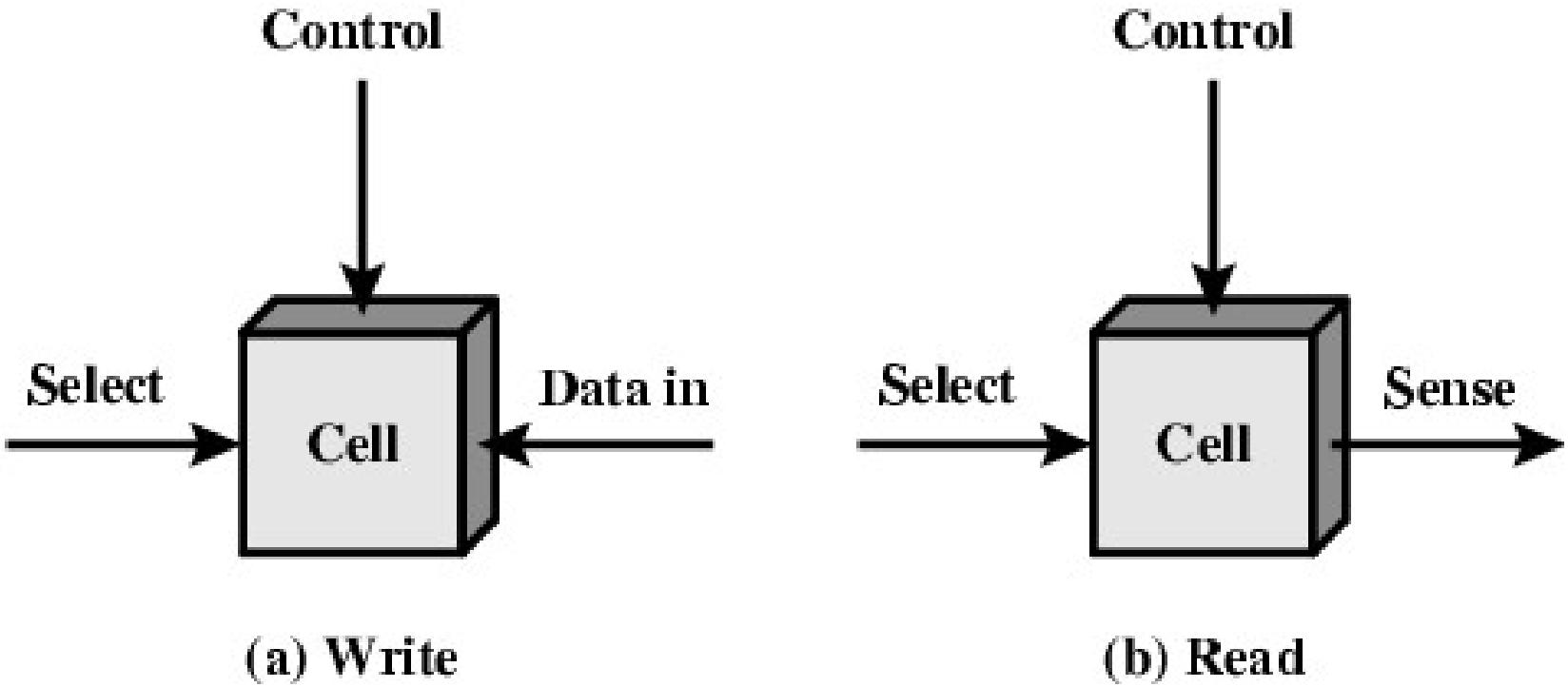
Computer Components



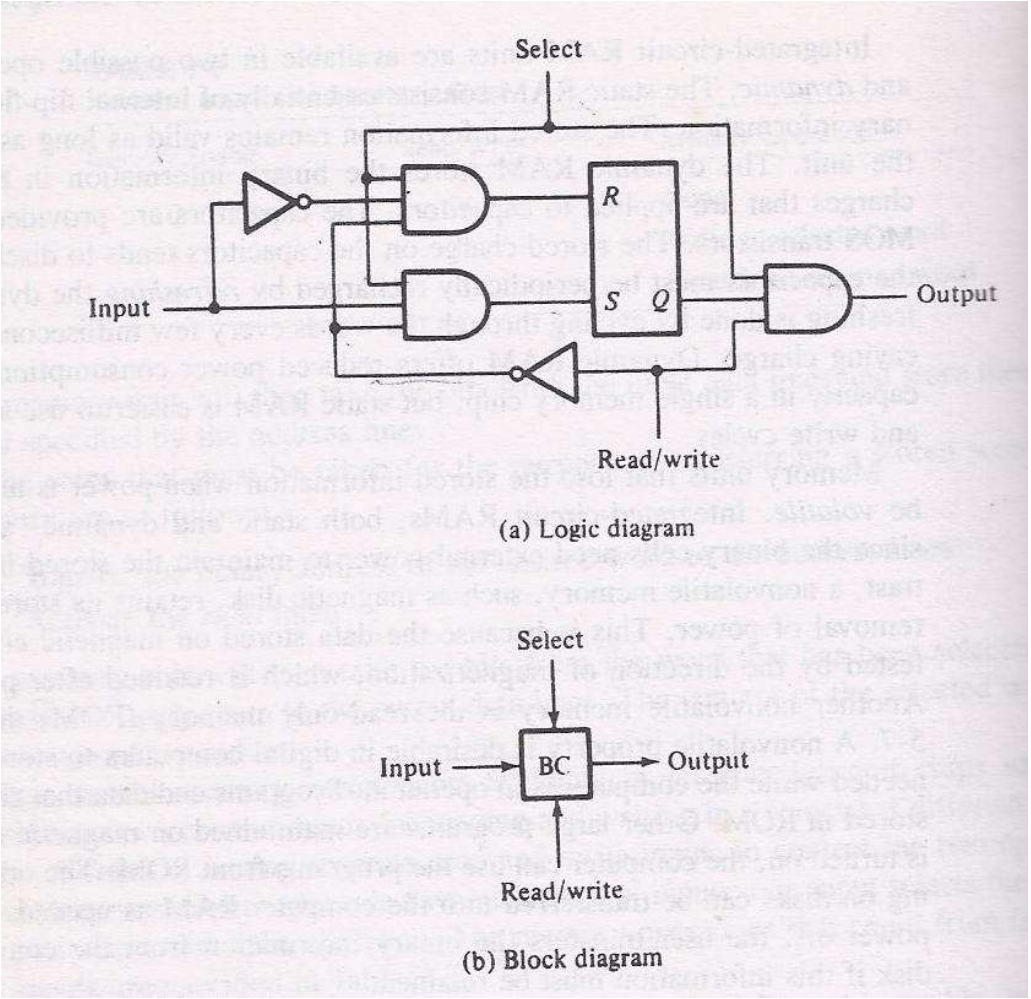
Semiconductor Memory

- RAM (Random Access Memory)
  - Misnamed as all semiconductor memory is random access
  - Read/Write
  - Volatile
  - Temporary storage
  - Static or dynamic

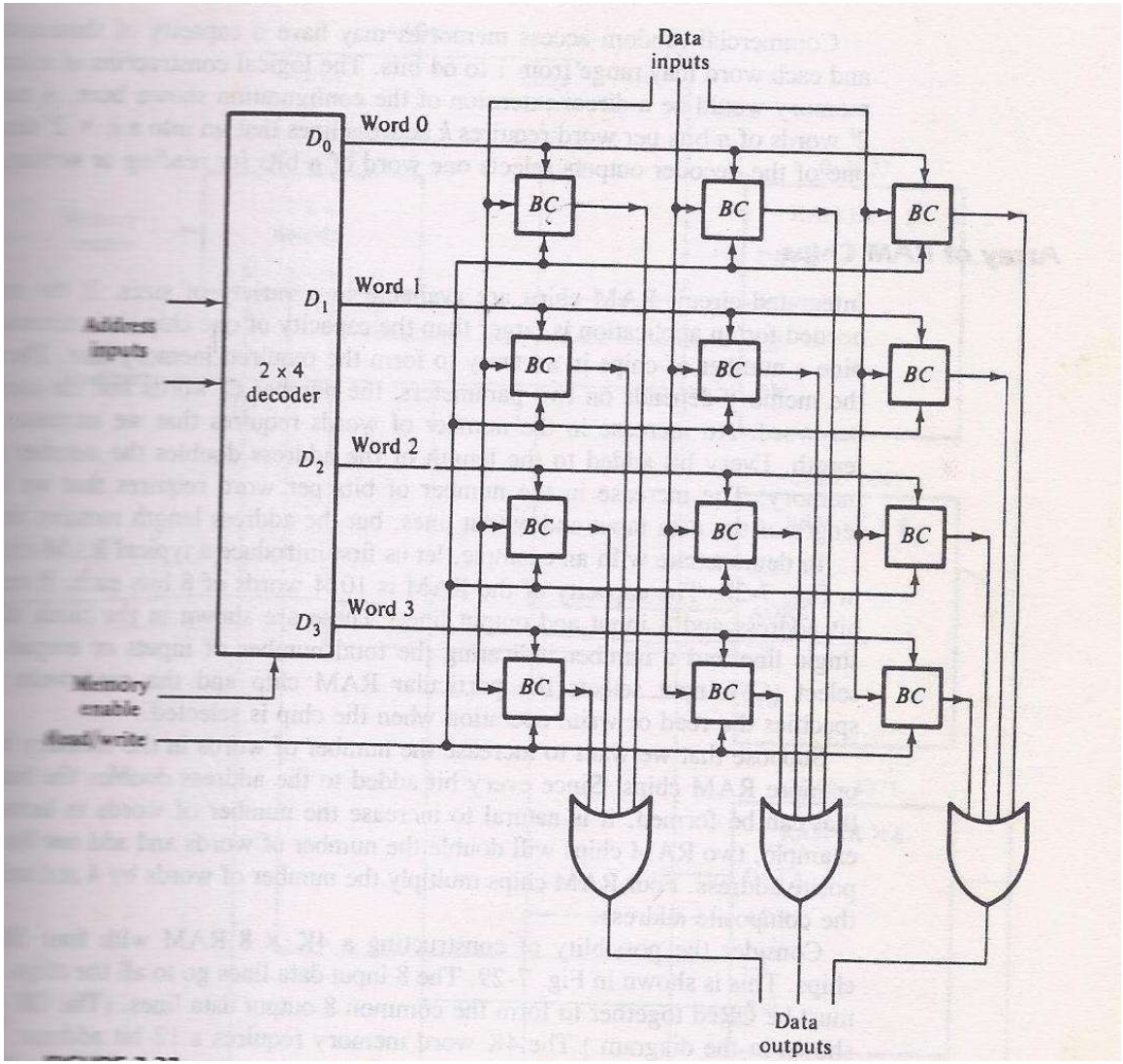
Memory Cell Operation



Memory Cell


Select
R
S
Q
Input
Output
Read/write
(a) Logic diagram
Select
Input
BC
Output
Read/write
(b) Block diagram

Memory Module



Memory Module

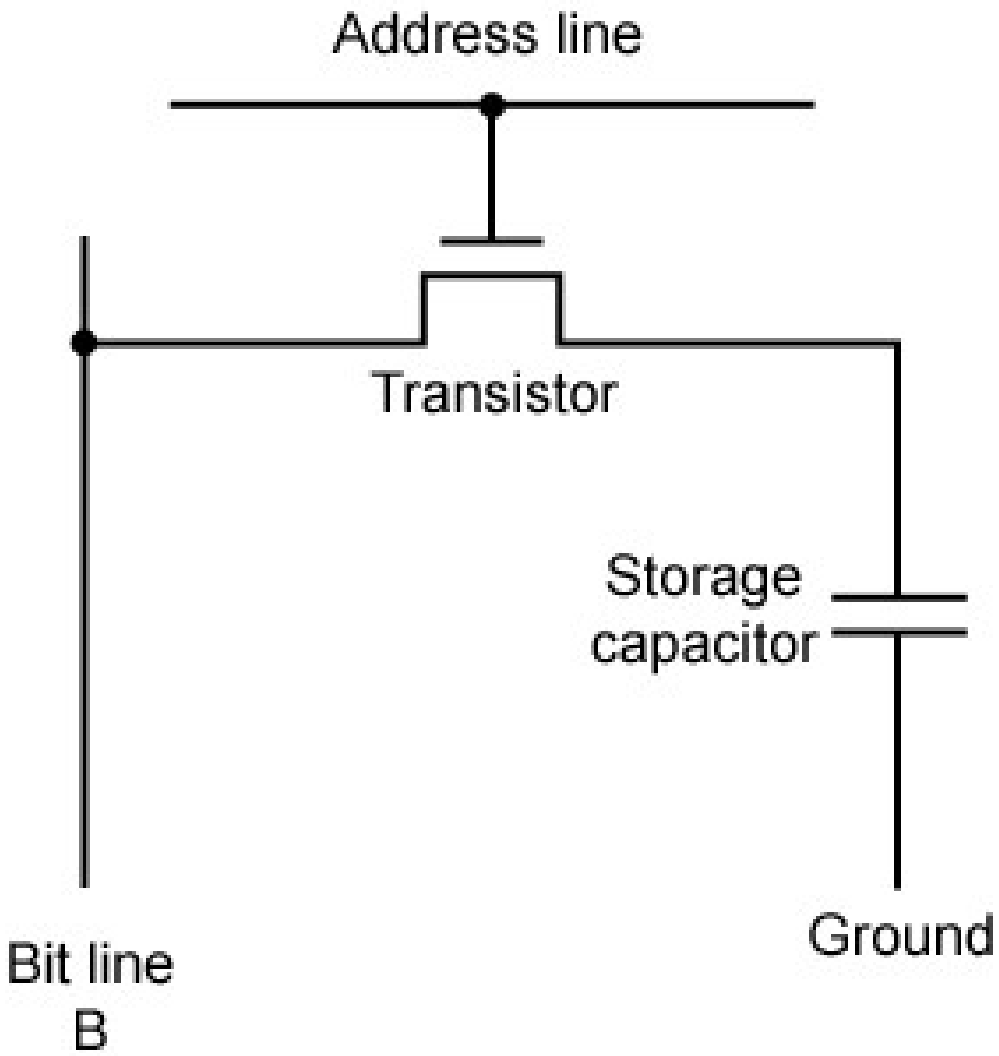
Parameters of Memory Module:

- Addressable Memory Space
  - Size of Address Bus
- Size of Memory Location
  - Size of Data Bus
- Memory Capacity
- Memory Organization
  - Byte organized

Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory
- Essentially analogue
  - Level of charge determines value

Dynamic RAM Structure



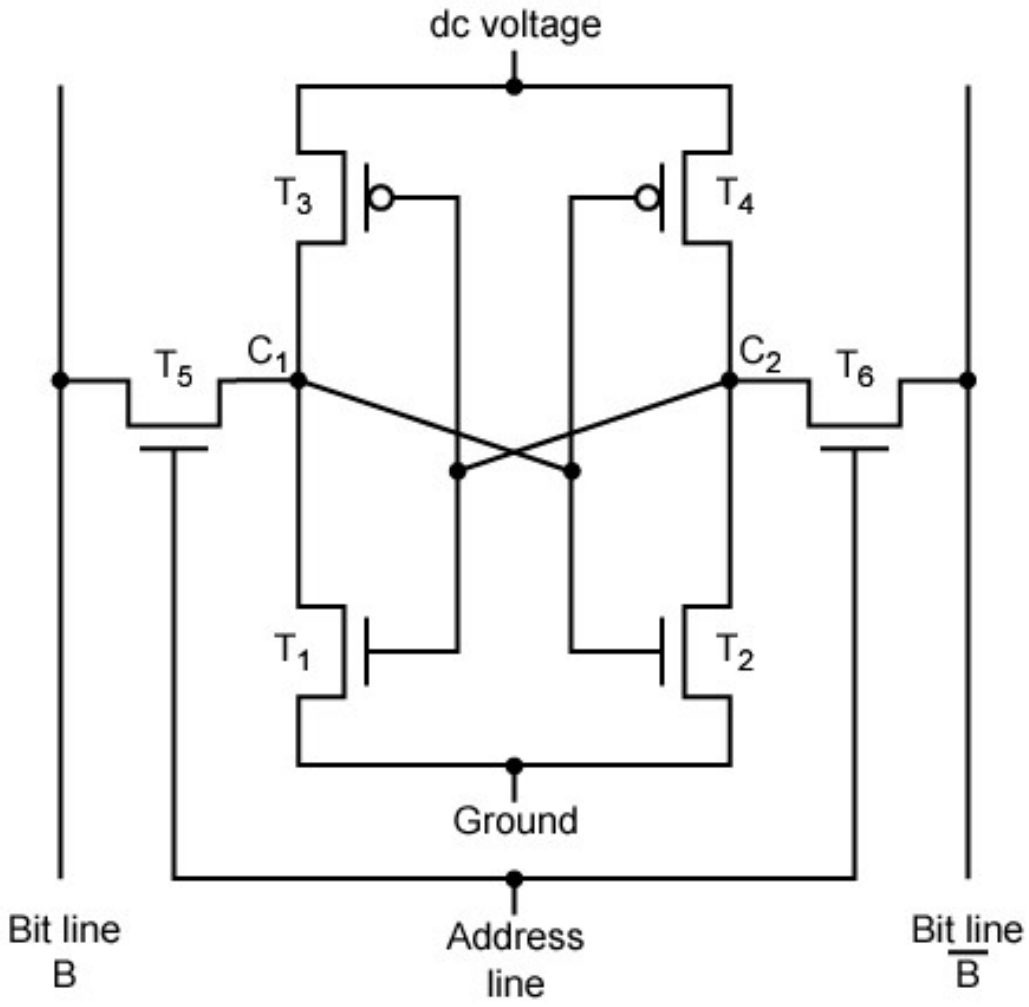
DRAM Operation

- Address line active when bit read or written
  - Transistor switch closed (current flows)
- Write
  - Voltage to bit line
    - High for 1 low for 0
  - Then signal address line
    - Transfers charge to capacitor
- Read
  - Address line selected
    - transistor turns on
  - Charge from capacitor fed via bit line to sense amplifier
    - Compares with reference value to determine 0 or 1
  - Capacitor charge must be restored

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache
- Digital
  - Uses flip-flops

Stating RAM Structure



State 1

C_1 high, C_2 low

T_1 T_4 off, T_2 T_3 on

State 0

C_1 low, C_2 high

T_1 T_4 on, T_2 T_3 off

Static RAM Operation

- Transistor arrangement gives stable logic state
- State 1
  - C_1 high, C_2 low
  - T_1 T_4 off, T_2 T_3 on
- State 0
  - C_2 high, C_1 low
  - T_2 T_3 off, T_1 T_4 on
- Address line transistors T_5 T_6
- Write – apply value to B & compliment to B
- Read – value is on line B

SRAM v DRAM

- Both volatile
  - Power needed to preserve data
- Dynamic cell
  - Simpler to build, smaller
  - More dense
  - Less expensive
  - Needs refresh
  - Larger memory units
- Static
  - Faster
  - Less dense
  - Cache

Reference

Computer Organization and Architecture –
Designing for Performance
William Stallings, Seventh Edition

Chapter 05: Internal Memory

Computer Organization
Hamacher, Vranesic and Zaky, Fifth Edition

Chapter05: Page No.: 291 - 314