CS 223 Computer Architecture and Organization

Main Memory

J. K. Deka

Professor

Department of Computer Science & Engineering

Indian Institute of Technology Guwahati, Assam.

SRAM v DRAM

- Both volatile
  - Power needed to preserve data
- Dynamic cell
  - Simpler to build, smaller
  - More dense
  - Less expensive
  - Needs refresh
  - Larger memory units
- Static
  - Faster
  - Less dense
  - Cache

Read Only Memory (ROM)

- ROM
  - Semiconductor memory
  - Random Access
- Permanent storage
  - Nonvolatile
- Microprogramming
- Library subroutines
- Systems programs (BIOS)
- Function tables

Types of ROM

- Written during manufacture
  - ROM
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Programmable (Read “mostly”)
  - Erasable Programmable (EPROM)
    - Erased by UV
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read

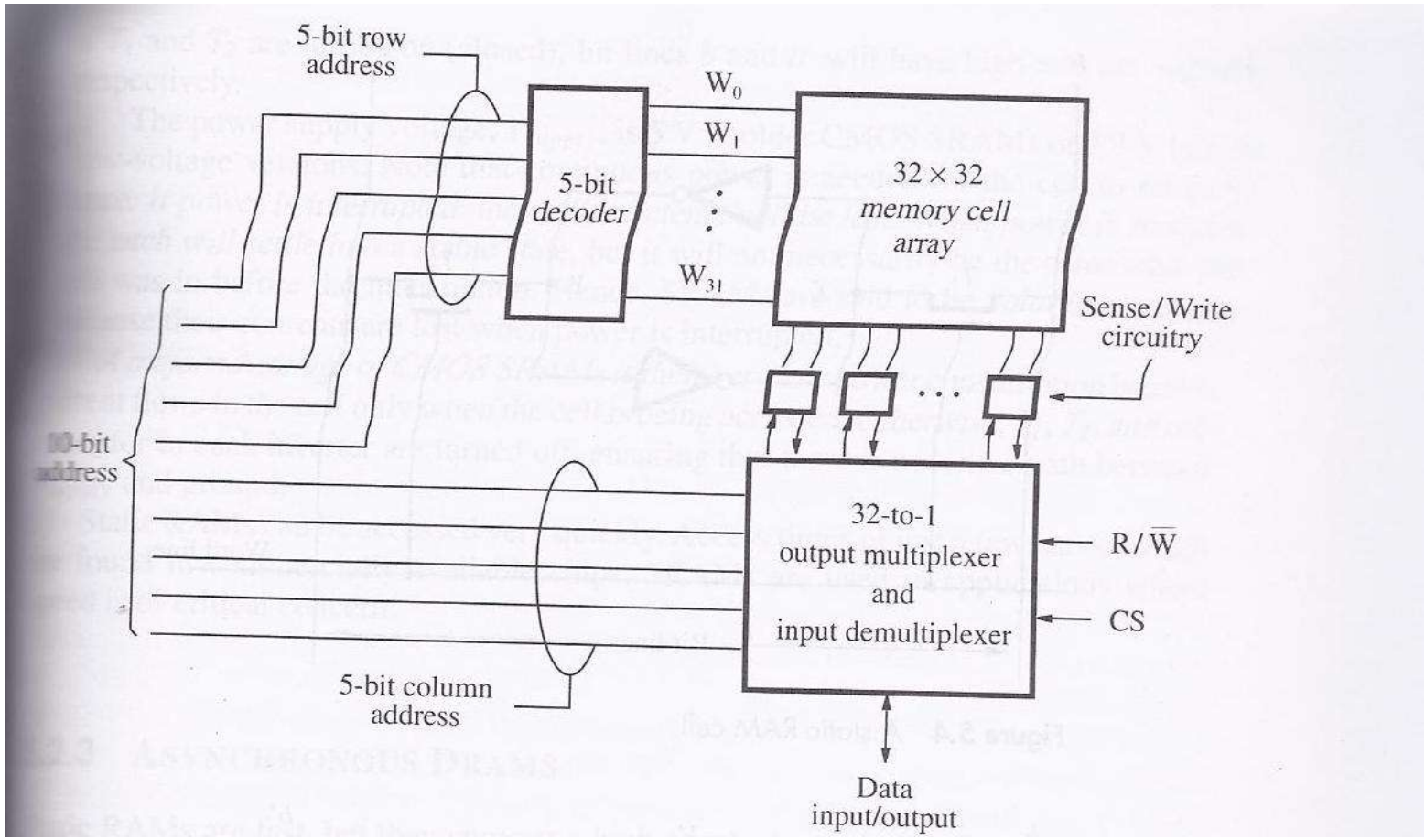
Organisation in detail

- Memory chip of 16Mbit = 16Mx1
- A 16Mbit chip can be organised as 1M of 16 bit words
- A bit per chip system has 16 lots of 1Mbit chip with bit 1 of each word in chip 1 and so on

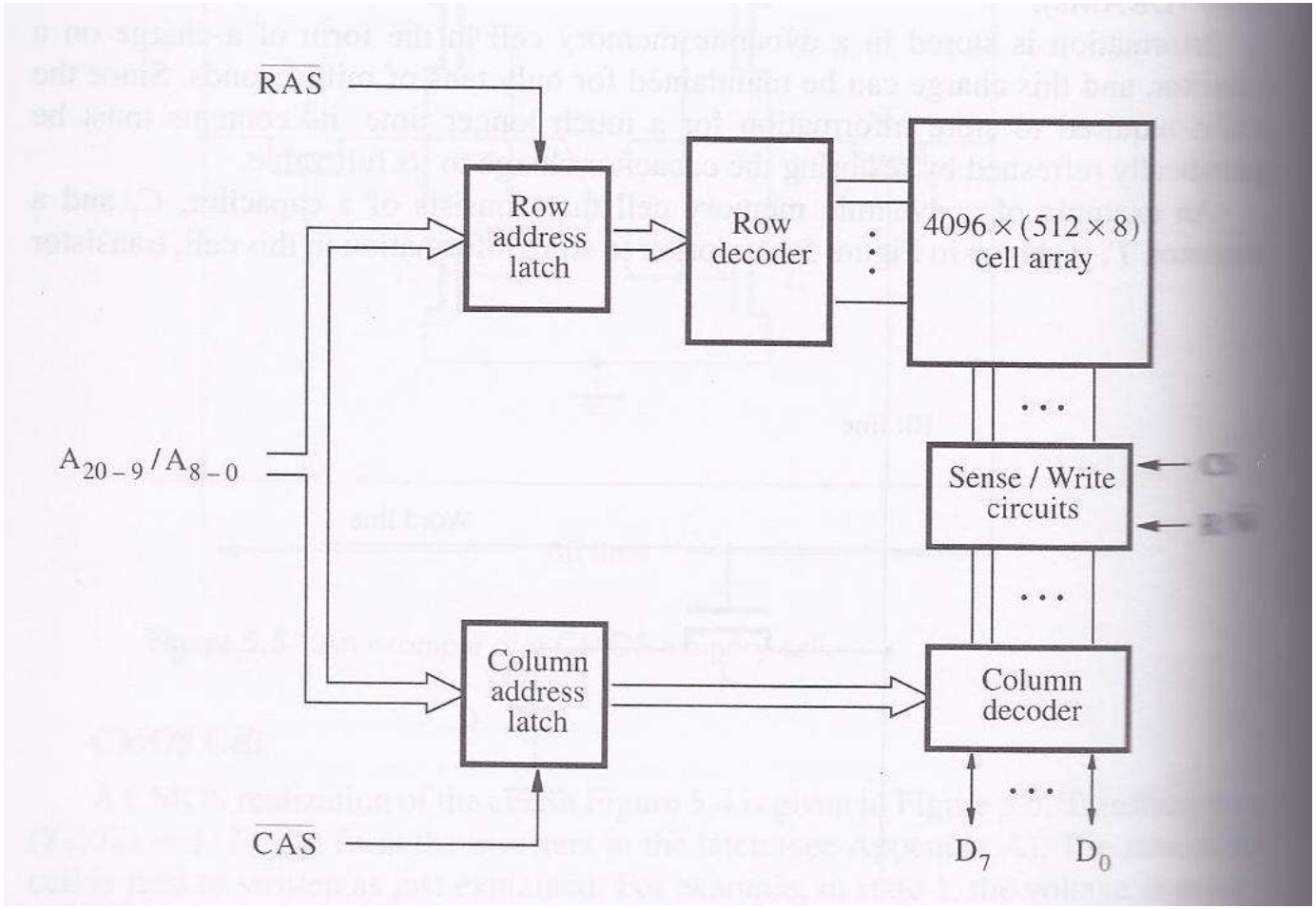
Organisation in detail

- A 16Mbit chip can be organised as a 4096 x 4096 array
  - Reduces number of address pins
    - Multiplex row address and column address
    - 12 pins to address (2^{12}=4096)
    - Adding one more pin doubles range of values so x4 capacity

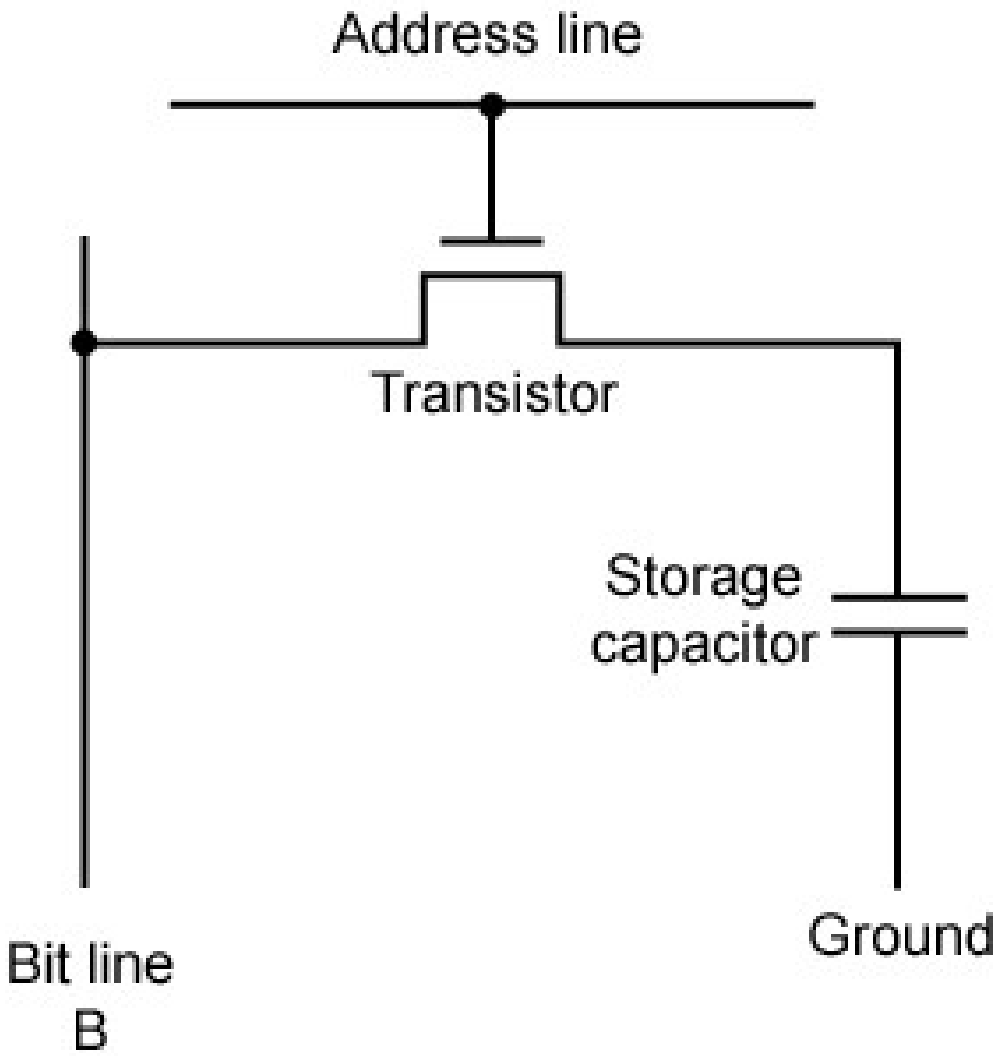
Organisation in detail



Organisation in detail



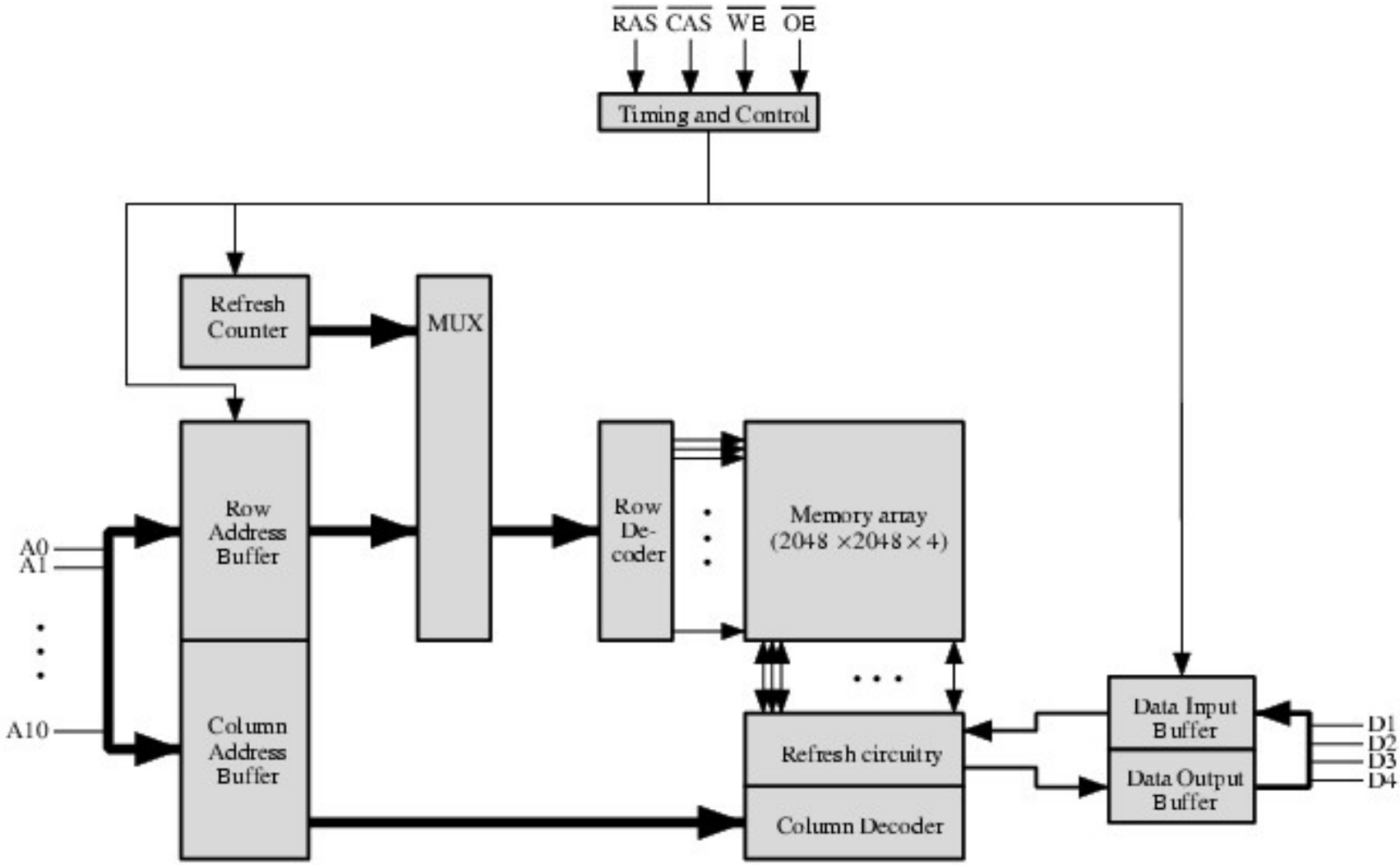
Dynamic RAM Structure



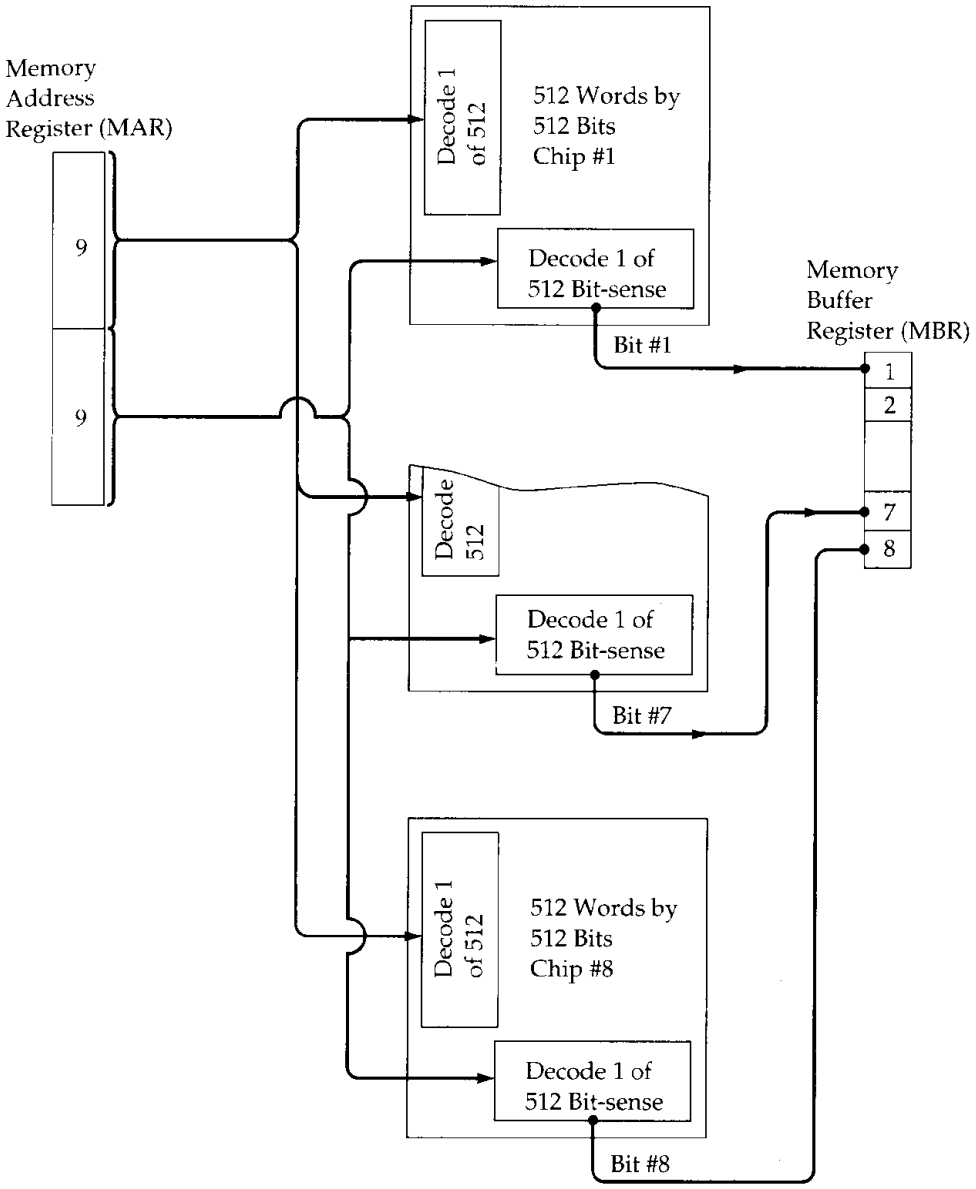
Refreshing

- Refresh circuit included on chip
- Disable chip
- Count through rows
- Read & Write back
- Takes time
- Slows down apparent performance

Typical 16 Mb DRAM (4M x 4)

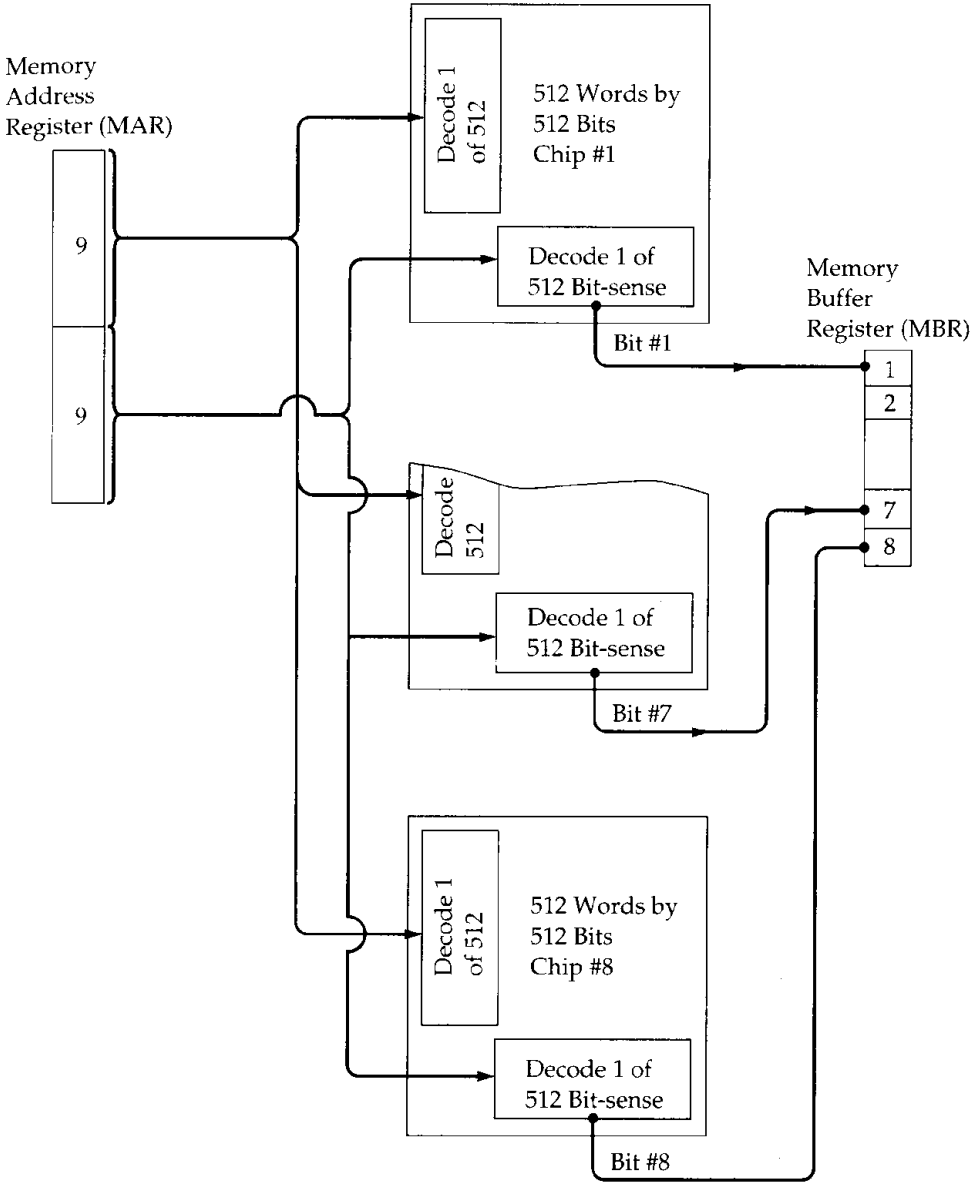


Memory Module Organisation



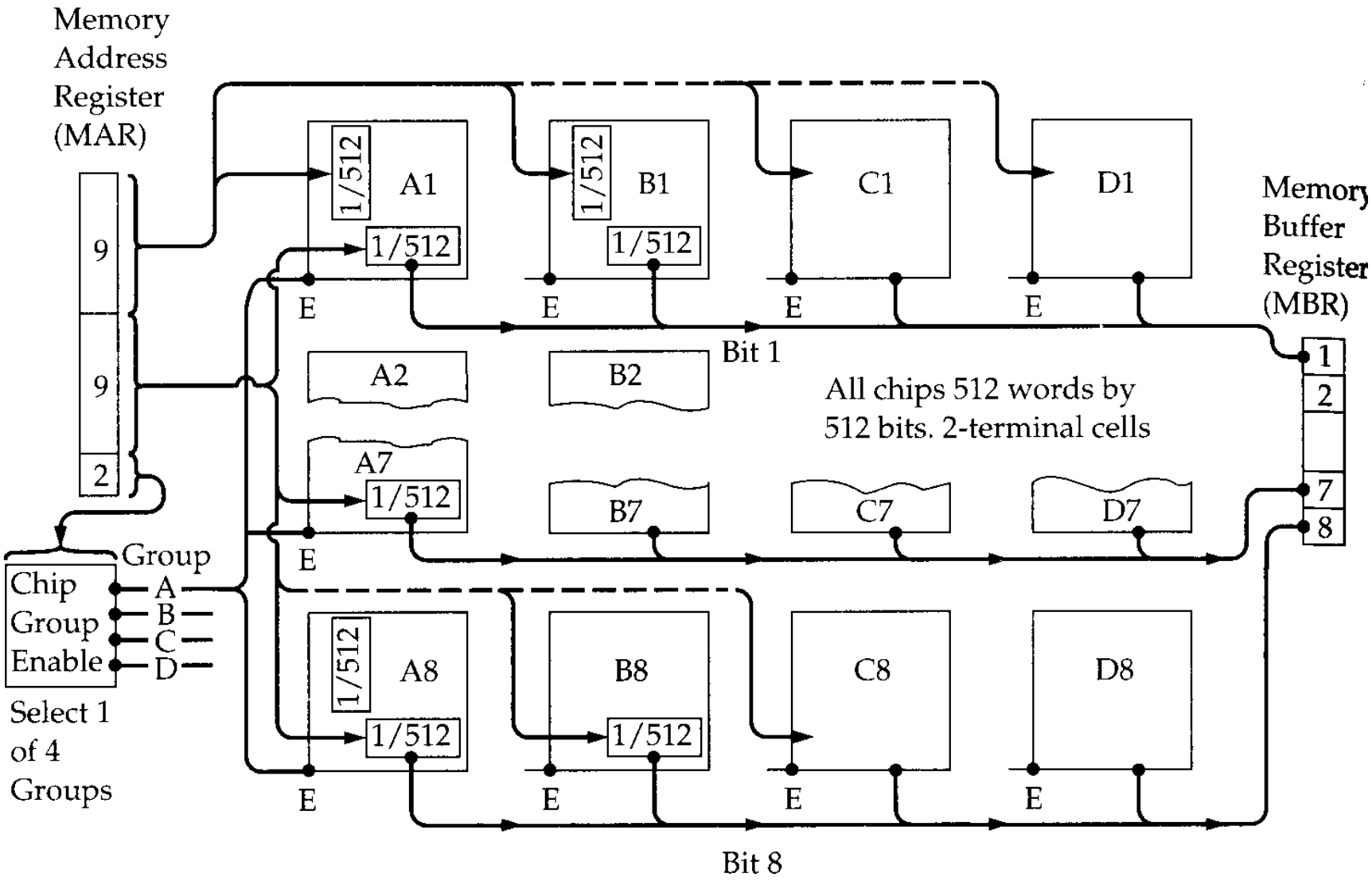
256K bit Memory chip

Memory Module Organisation

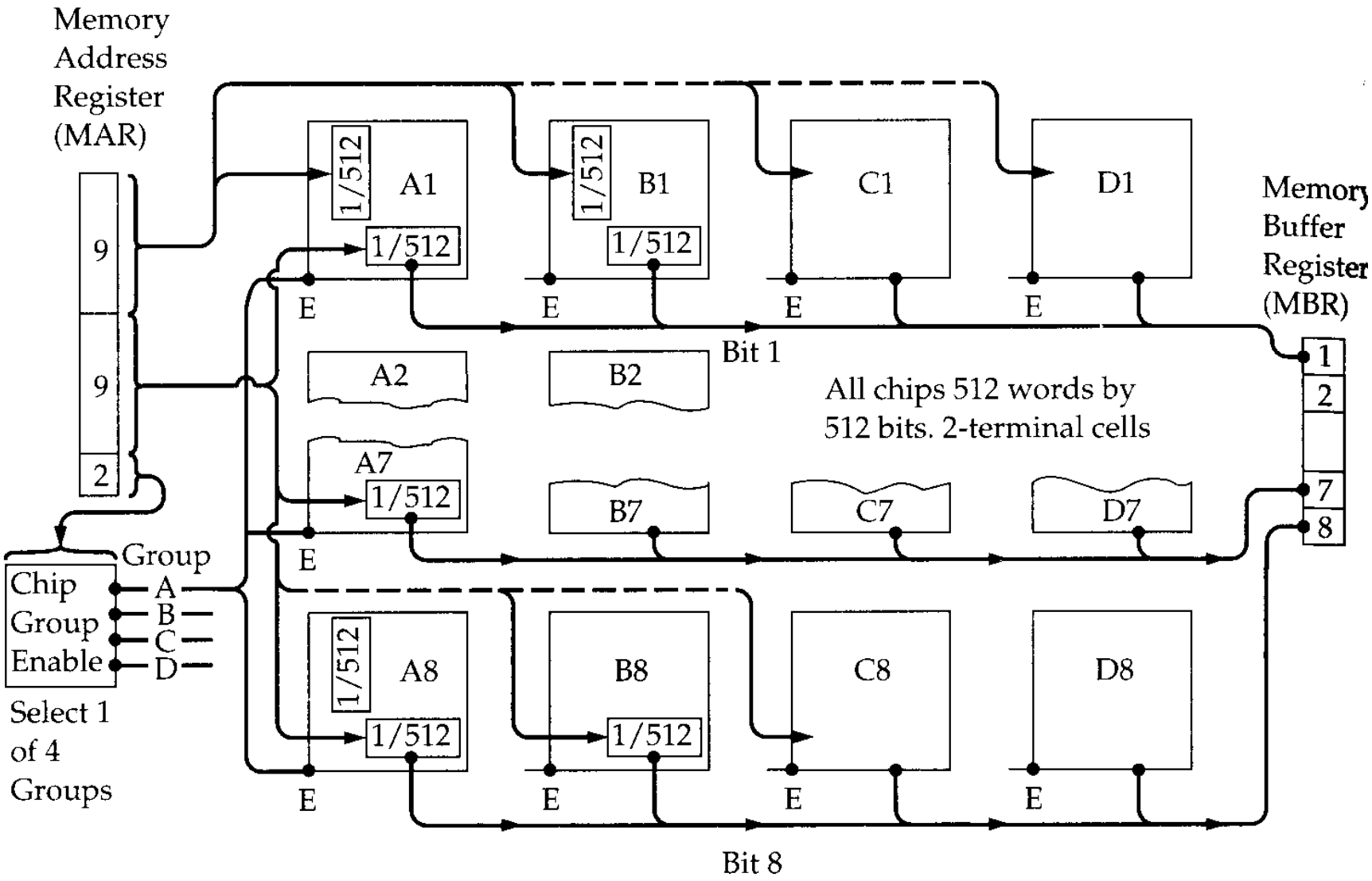


256KByte Module Organisation

Memory Module Organisation



1MByte Module Organisation



Memory Module Organization

Consider memory chip of capacity 1 MB (1Mx8)

- Construct a memory module of capacity 4MB (2Mx16)
  (Size of Address bus and size of data bus)

- Construct a memory module of capacity 16 MB (8Mx16)
  (Size of Address bus and size of data bus)

- Construct a memory module of capacity 32 MB (8Mx32)
  (Size of Address bus and size of data bus)

- Construct a memory module of capacity 128 MB (32Mx32)
  (Size of Address bus and size of data bus)

Memory Module Organization

Consider memory chip of capacity 1 MB (1Mx8)

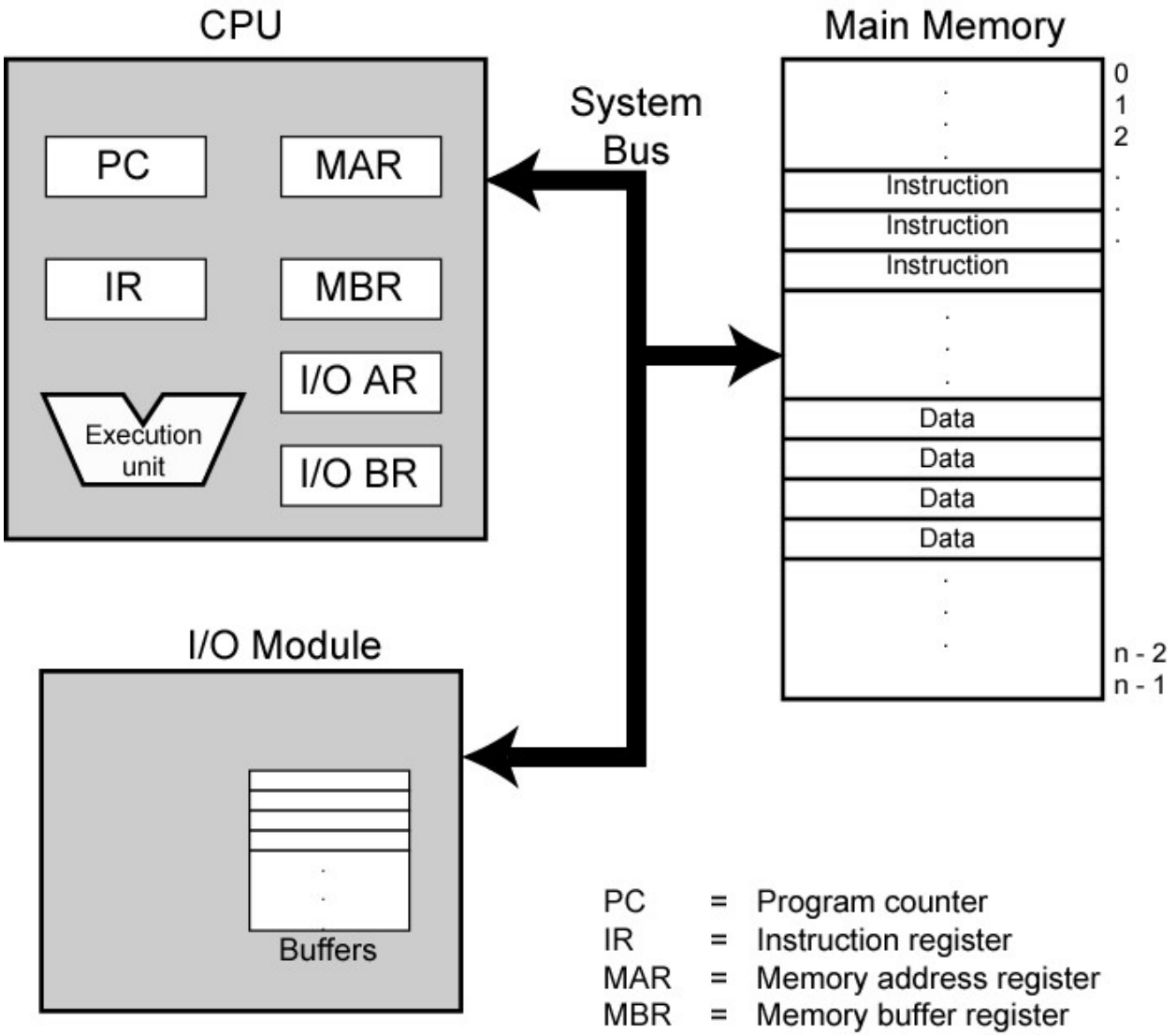
- Construct a memory module of capacity 8 MB (4Mx2)
  (Size of Address bus and size of data bus)

Memory Module Organization

Consider memory chip of capacity 1 MB (1Mx8)

- Construct a memory module of capacity 8 MB (4Mx2)
  - Byte organized
    (Size of Address bus and size of data bus)

Computer Components: Top Level View



Fetch Sequence (symbolic)

- t1: MAR <- PC
- t2: MBR <- (memory)
- PC <- PC +1
- t3: IR <- MBR

  - (tx = time unit/clock cycle)
  - (Speed of CPU and Memory)

Memory Read(symbolic)

- t1: MAR <- R1
- t2: MBR <- (memory)
- t3: R2 <- MBR

  – (tx = time unit/clock cycle)

Address of the memory location is in register R1 and data to be stored in register R2

Memory Write(symbolic)

- t1: MAR <- R1
- t2: MBR <- R2
- t3: (memory) <- MBR

  – (tx = time unit/clock cycle)

Address of the memory location is in register R1 and data is in register R2

Reference

Computer Organization and Architecture –
Designing for Performance
William Stallings, Seventh Edition

Chapter 05: Internal Memory

Computer Organization
Hamacher, Vranesic and Zaky, Fifth Edition

Chapter05: Page No.: 291 - 314