IIT Guwahati - Department of Computer Science & Engineering
CS 223 – Computer Architecture & Organization
Quiz#1 - (08.02.2022): Platform: CodeTantra, 45 minutes, 25 marks

Section 1: [2 questions, 4 marks, Student will get randomly one question each from Q1 and Q2.]

Instruction: Show the calculations and write the answer in a single sheet and upload.

Q1: File Upload: 4 marks

Full marks with proper calculation and correct answer. 1 mark for only correct answer without calculation.

A. The content of a floating-point register is C1000000. The format of the floating point is IEEE-754 (single precision) and it uses excess-127 for biased exponent. What is the equivalent decimal value?

C1000000 = 1100 0001 0000 0000 …….. 1 10000010 000000…….

Sign bit = 1 (-ve) Biased Exponent = 130, Exponent = 130 -127 = 3

$-1.00000 \times 2^3 = -8$

B. The content of a floating-point register is C1200000. The format of the floating point is IEEE-754 (single precision) and it uses excess-127 for biased exponent. What is the equivalent decimal value?

C1200000 = 1100 0001 0010 0000 …….. 1 10000010 010000…….

Sign bit = 1 (-ve) Biased Exponent = 130, Exponent = 130 -127 = 3

$-1.010000 \times 2^3 = -1010.00000 = -10$

C. The content of a floating-point register is C1600000. The format of the floating point is IEEE-754 (single precision) and it uses excess-127 for biased exponent. What is the equivalent decimal value?

C1600000 = 1100 0001 0110 0000 …….. 1 10000010 110000…….

Sign bit = 1 (-ve) Biased Exponent = 130, Exponent = 130 -127 = 3

$-1.110000 \times 2^3 = -1110.00000 = -14$

D. Consider the real number 25.375 and this number is stored in a 32-bit register using IEEE-754 (Single Precision) format and it uses excess-128 for biased exponent. Write the contents of the register in Hexadecimal format.

$25.375 = 11001.011 = 1.1001011 \times 2^4$ Exponent = 4 Biased Exponent = 4+128 = 132

0 10000100 100101100000…… = 424B0000

E. Consider the real number 29.625 and this number is stored in a 32-bit register using IEEE-754 (Single Precision) format and it uses excess-128 for biased exponent. Write the contents of the register in Hexadecimal format.

29.625 = 11101.101 = 1.1101101 x 2^4 Exponent = 4 Biased Exponent = 4+128 = 132

0 10000100 110110100000…… = 426D0000

F. Consider the real number 27.75 and this number is stored in a 32-bit register using IEEE-754 (Single Precision) format and it uses excess-128 for biased exponent. Write the contents of the register in Hexadecimal format.

27.75 = 11011.11 = 1.101111 x 2^4 Exponent = 4 Biased Exponent = 4+128 = 132

0 10000100 1011110000000…… = 425E0000

Q2: File Upload: 4 marks

3 marks for part (a) and 1 marks for part (b)

A. The RTL description of the fetch phase of single bus CPU organization is as follows:

T1: MAR <- PC, Read

T2: MBR <- Memory

PC <- PC+1

T3: IR <- MBR

(a) Give the RTL description of the execution phase of the instruction: BRZ *address* [Branch on Zero]. It is a two-word instruction – first word is the op-code and the second word is the target address of the branch instruction. [Flags bits: Z: Zero, S: Sign, C: Carry, O: Overflow, AC: Auxiliary Carry]

T4: MAR <- PC, Read
T5: MBR <- Memory
PC <- PC +1
T6: IF (Z == 1) PC <- MBR

(b) If the operating clock frequency of the processor is 1 GHz, what is the required time to complete the instruction BRZ (both fetch and execute cycle). Assume that the memory also operates in the same clock frequency.

Clock Frequency = 1 GHz Clock Time = 1/1 GHz = 1 x 10^{-9} second = 1 Nano Second
Time required = 6 x 1 nano second = 6 nano second

B. The RTL description of the fetch phase of single bus CPU organization is as follows:

T1: MAR <- PC, Read

T2: MBR <- Memory

PC <- PC+1

T3: IR <- MBR

(a) Give the RTL description of the execution phase of the instruction: BRN *address* [Branch on Negative]. It is a two-word instruction – first word is the op-code and the second word is the target address of the branch instruction. [Flags bits: Z: Zero, S: Sign, C: Carry, O: Overflow, AC: Auxiliary Carry]

T4: MAR <- PC, Read
T5: MBR <- Memory
PC <- PC +1
T6: IF (S == 1) PC <- MBR

(b) If the operating clock frequency of the processor is 2 GHz, what is the required time to complete the instruction BRN (both fetch and execute cycle). Assume that the memory also operates in the same clock frequency.

Clock Frequency = 2 GHz Clock Time = 1/2 GHz = 0.5 x 10^{-9} second = 0.5 Nano Second
Time required = 6 x 0.5 nano second = 3 nano second

C. The RTL description of the fetch phase of single bus CPU organization is as follows:

T1: MAR <- PC, Read

T2: MBR <- Memory

PC <- PC+1

T3: IR <- MBR

(a) Give the RTL description of the execution phase of the instruction: BRP *address* [Branch on positive]. It is a two-word instruction – first word is the op-code and the second word is the target address of the branch instruction. [Flags bits: Z: Zero, S: Sign, C: Carry, O: Overflow, AC: Auxiliary Carry]

T4: MAR <- PC, Read
T5: MBR <- Memory
PC <- PC +1
T6: IF (S == 0) PC <- MBR

(b) If the operating clock frequency of the processor is 2.5 GHz, what is the required time to complete the instruction BRP (both fetch and execute cycle). Assume that the memory also operates in the same clock frequency.

Clock Frequency = 2.5 GHz Clock Time = 1/2.5 GHz = 0.4 x 10^{-9} second = 0.4 Nano Second
Time required = 6 x 0.4 nano second = 2.4 nano second

Section 2: [1 question, 6 marks, Student will get randomly one question from Q1.]

Instruction: With the help of necessary explanations, write the answers of all sub-sections in a single sheet and upload.

Q1: File Upload: 6 marks

2 marks for each part.

A. Consider the following assembly level code segment of 8085 microprocessor

```
LDA B001
MVI L, 10
MVI H, B0
ADD M
HLT
```

(a) If the machine level code segment of this program is stored from memory location 100B, then what is the content of PC after execution of this code segment?

Starting address of the code segment: 100B
Length of the program: 3 + 2 + 2+ 1 +1 = 9
Content of the PC after execution of the code segment: 1014

(b) What are the locations of the operands of ADD instruction before execution of this code segment?

Location of operands before execution: B001 and B010

(c) What is the final effect of this code segment.

It loads an operand from memory location B001 to the accumulator. Then it adds the content of memory location B010 to accumulator and store the result in accumulator.

B. Consider the following assembly level code segment of 8085 microprocessor

```
MVI L, 20
MVI H, B0
MVI A, 70
ADD M
HLT
```

(a) If the machine level code segment of this program is stored from memory location 200C, then what is the content of PC after execution of this code segment?

Starting address of the code segment: 200C
Length of the program: 2 + 2 + 2+ 1 +1 = 8
Content of the PC after execution of the code segment: 2014

(b) What are the locations of the operands of ADD instruction before execution of this code segment?

Location of operands before execution: B020 and 2011

(c) What is the final effect of this code segment.

It loads an operand from memory location 2011 to the accumulator. Then it adds the content of memory location B020 to accumulator and store the result in accumulator.

C. Consider the following assembly level code segment of 8085 microprocessor

MVI B, 3F

LDA A001

ADD B

STA AF00

HLT

(a) If the machine level code segment of this program is stored from memory location B00A, then what is the content of PC after execution of this code segment?

Starting address of the code segment: B00A
Length of the program: 2 + 3 + 1+ 3 +1 = 10
Content of the PC after execution of the code segment: B014

(b) What are the locations of the operands of ADD instruction before execution of this code segment?

Location of operands before execution: B00B and A001

(c) What is the final effect of this code segment.

It loads an operand from memory location B00B to register B and loads another operand from memory location A001 to the accumulator. Then it adds the content of register B to accumulator and store the result in accumulator. Finally, the result is transferred from accumulator to the memory location AF00.

Section 3: [1 question, 2 marks, Student will get randomly one question from Q1.]

Instruction: With the help of necessary steps used for solving, answer the following in the given space.

Q1: Essay type. 2 marks

Full credit for correct answer with calculation, 1 marks for only answer.

A. For a memory module, the size of data bus (size of memory location) is 16 bits and size of address bus is 36 bits. What is the capacity of the memory module in Giga Byte (GB)? **[2]**

Capacity of memory module = 16 bits x 2^{36} = 2 bytes x 2^{36} = 2^7x2^{30} bytes = 128 GB

B. For a memory module, the size of data bus (size of memory location) is 32 bits and size of address bus is 30 bits. What is the capacity of the memory module in Giga Byte (GB)? **[2]**

Capacity of memory module = 32 bits x 2^{30} = 4 bytes x 2^{30} = 2^2x2^{30} bytes = 4 GB

C. For a memory module, the size of data bus (size of memory location) is 32 bits and size of address bus is 28 bits. What is the capacity of the memory module in Giga Byte (GB)? **[2]**

Capacity of memory module = 32 bits x 2^{28} = 4 bytes x 2^{28} = 2^0x2^{30} bytes = 1 GB

D. The capacity of a memory module is 32 GB. What are the sizes of address bus and data bus if the size of each memory location is 32 bits? **[1+1]**

Size of data bus = 32 bits
Number of memory location = 32 GB/4 bytes = 8 Giga
Size of address bus = 33 bits

E. The capacity of a memory module is 64 GB. What are the sizes of address bus and data bus if the size of each memory location is 32 bits? **[1+1]**

Size of data bus = 32 bits
Number of memory location = 64 GB/4 bytes = 16 Giga
Size of address bus = 34 bits

F. The capacity of a memory module is 8 GB. What are the sizes of address bus and data bus if the size of each memory location is 32 bits? **[1+1]**

Size of data bus = 32 bits
Number of memory location = 8 GB/4 bytes = 2 Giga
Size of address bus = 31 bits

Section 4: [3 questions, 3 marks each, Student will get randomly one question each from Q1, Q2 and Q3.]

Instruction: With the help of necessary steps used for solving, answer the following in the given space.

Q1: Essay type. 3 marks

0.5 marks for each flag provided they show the calculation.

A. If the last operation performed on a computer with an 8-bit word was an addition (A+B) in which the two operands were A = -82 and B = -95; the numbers are represented in 2's complement form. What would be the value of Carry, Zero, Overflow, Sign, Even Parity, and Half Carry flags? (Show the calculations)

A = -82 = 10101110
B = -95 = 10100001
A + B = 101001111
Carry = 1, Zero = 0, Overflow = 1, Sign = 0, Even Parity = 0, Half Carry = 0

B. If the last operation performed on a computer with an 8-bit word was an addition (A+B) in which the two operands were A = -37 and B = -105; the numbers are represented in 2's complement form. What would be the value of Carry, Zero, Overflow, Sign, Even Parity, and Half Carry flags? (Show the calculations)

A = -37 = 11011011
B = -105 = 10010111
A + B = 101110010
Carry = 1, Zero = 0, Overflow = 1, Sign = 0, Even Parity = 1, Half Carry = 1

C. If the last operation performed on a computer with an 8-bit word was an addition (A+B) in which the two operands were A = -77 and B = -66; the numbers are represented in 2's complement form. What would be the value of Carry, Zero, Overflow, Sign, Even Parity, and Half Carry flags? (Show the calculations)

A = -77 = 10110011
B = -66 = 10111110
A + B = 101110001
Carry = 1, Zero = 0, Overflow = 1, Sign = 0, Even Parity = 1, Half Carry = 1

Q2: Essay type. 3 marks

1 mark for displacement and 2 marks for 2's complement representation

A. Consider a branch instruction in PC-relative mode with 12 bits long address field and the size of the instruction is 2 words. First word is the op-code and the second word is the displacement. Assume the instruction is stored in memory address 610_{10}. If the branch is made to location 540_{10}, specify the value of the displacement field of the instruction in 2's complement form.

After fetching the complete instruction, the content of PC is 612
Displacement = 540 – 612 = -72
-72 in 2's complement for 12-bit address field = 111110111000

B. Consider a branch instruction in PC -relative mode with 12 bits long address field and the size of the instruction is 2 words. First word is the op-code and the second word is the displacement. Assume the instruction is stored in memory address 720_{10}. If the branch is made to location 430_{10}, specify the value of the displacement field of the instruction in 2's complement form.

After fetching the complete instruction, the content of PC is 722
Displacement = 430 – 722 = -292
-292 in 2's complement for 12-bit address field = 111011011100

C. Consider a branch instruction in pc-relative mode with 12 bits long address field and the size of the instruction is 2 words. First word is the op-code and the second word is the displacement. Assume the instruction is stored in memory address 950_{10}. If the branch is made to location 670_{10}, specify the value of the displacement field of the instruction in 2's complement form.

After fetching the complete instruction, the content of PC is 952
Displacement = 670 – 952 = -282
-282 in 2's complement for 12-bit address field = 111011100110

Q3: Essay type. 3 marks **1 mark for each representation**

A. The content of an 8-bit register is 11001010. What is the decimal value of the content of the register if the format is **[1+1+1]**

(i) unsigned integer 202
(ii) integer in sign-magnitude form -74
(iii) integer in 2's complement form -54

B. The content of an 8-bit register is 10011011. What is the decimal value of the content of the register if the format is **[1+1+1]**

(i) unsigned integer 155
(ii) integer in sign-magnitude form -27
(iii) integer in 2's complement form -101

C. The content of an 8-bit register is 11010110. What is the decimal value of the content of the register if the format is **[1+1+1]**

(i) unsigned integer 214
(ii) integer in sign-magnitude form -86
(iii) integer in 2's complement form -42