CS 223 Computer Architecture and Organization

Instruction Sets: Characteristics and Functions

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Instructions

- Instruction Set
- Format of Instructions

How many Addresses

- More addresses
  - More complex (powerful?) instructions
  - More registers
    - Inter-register operations are quicker
  - Fewer instructions per program
- Fewer addresses
  - Less complex (powerful?) instructions
  - More instructions per program
  - Faster fetch/execution of instructions

Design Decisions

- Operation repertoire
  - How many ops?
  - What can they do?
  - How complex are they?
- Data types
- Instruction formats
  - Length of op code field
  - Number of addresses

Design Decisions

- Registers
  - Number of CPU registers available
  - Which operations can be performed on which registers?
- Addressing modes

Types of Operand

- Addresses
- Numbers
  - Integer/floating point
- Characters
  - ASCII etc.
- Logical Data
  - Bits or flags

Specific Data Types

- General - arbitrary binary contents
- Integer - single binary value
- Ordinal - unsigned integer
- Unpacked BCD - One digit per byte
- Packed BCD - 2 BCD digits per byte
- Near Pointer - offset within segment
- Bit field
- Byte String
- Floating Point

Integer Representation

- Only have 0 & 1 to represent everything
- Positive numbers stored in binary
  - e.g. 41=00101001
- Sign-Magnitude
- Two's compliment

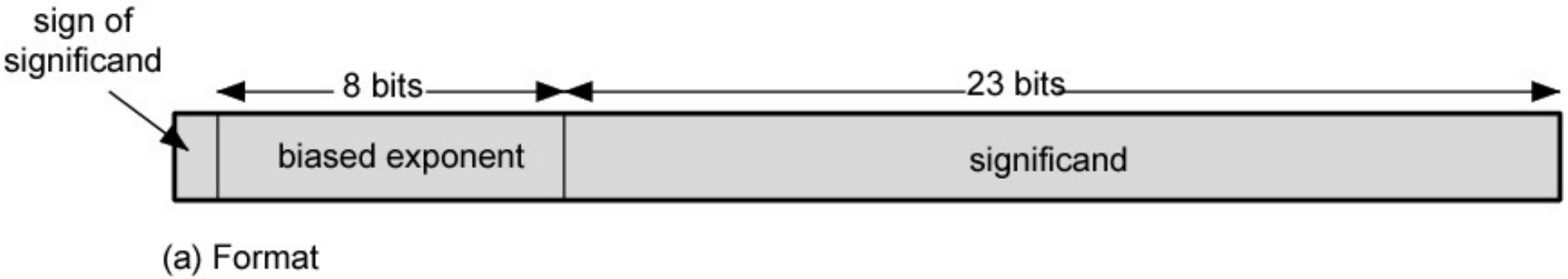
BCD Representation

- Unpacked BCD - One digit per byte
- Packed BCD - 2 BCD digits per byte

Real Numbers

- Numbers with fractions
- Could be done in pure binary
  - $1001.1010 = 2^4 + 2^0 + 2^{-1} + 2^{-3} = 9.625$
- Where is the binary point?
- Fixed?
  - Very limited
- Moving?
  - How do you show where it is?

Floating Point



(a) Format

- +/- .significand x $2^{exponent}$
- Misnomer
- Point is actually fixed between sign bit and body of mantissa
- Exponent indicates place value (point position)
- IEEE 754 single format
- IEEE 754 double format (64bits = 1+11+52)

Types of Operation

- Data Transfer
- Arithmetic
- Logical
- Conversion
- I/O
- System Control
- Transfer of Control

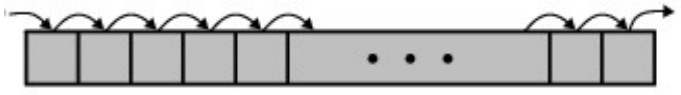
Data Transfer

- Specify
  - Source
  - Destination
  - Amount of data
- May be different instructions for different movements
  - e.g. IBM 370
- Or one instruction and different addresses
  - e.g. VAX

Arithmetic

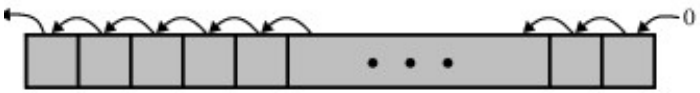
- Add, Subtract, Multiply, Divide
- Signed Integer
- Floating point
- May include
  - Increment (a++)
  - Decrement (a--)
  - Negate (-a)

Shift and Rotate Operations



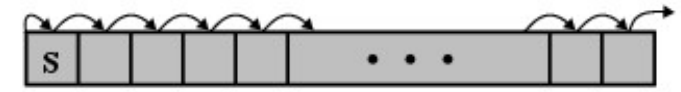
(a) Logical right shift

SHR



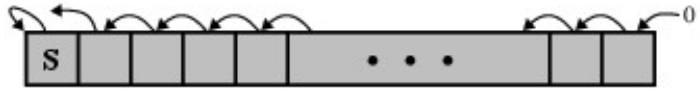
(b) Logical left shift

SHL



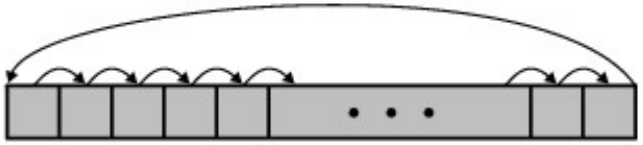
(c) Arithmetic right shift

ASR



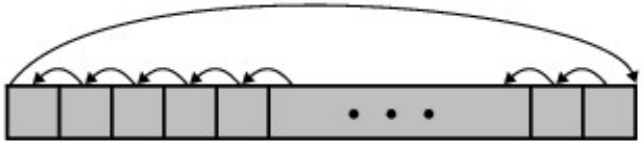
(d) Arithmetic left shift

ASL



(e) Right rotate

ROR



(f) Left rotate

ROL

Logical

- Bitwise operations
- AND, OR, NOT

Input/Output

- May be specific instructions
- May be done using data movement instructions (memory mapped)
- May be done by a separate controller (DMA)

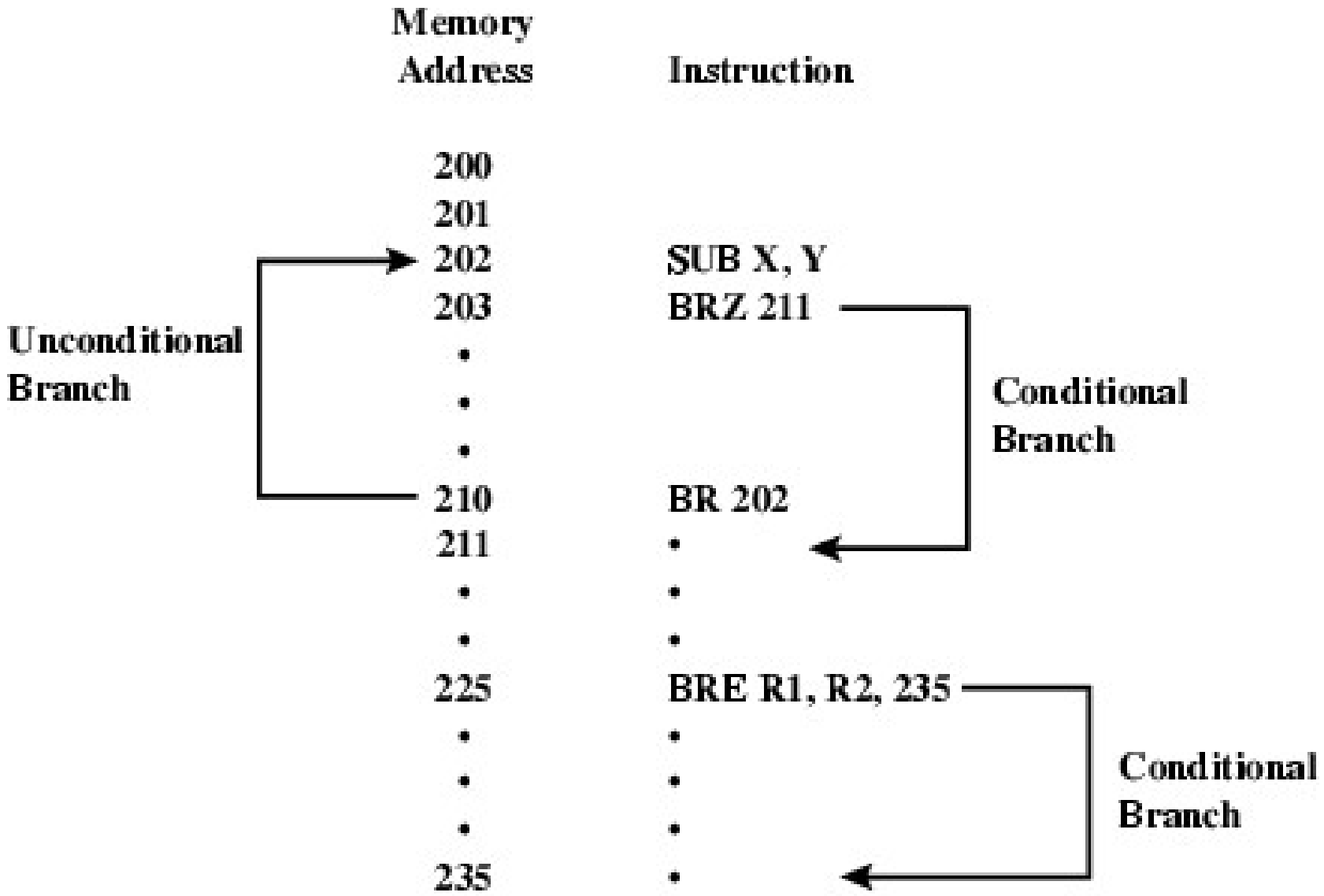
Systems Control

- Privileged instructions
- CPU needs to be in specific state
  - Kernel mode
- For operating systems use

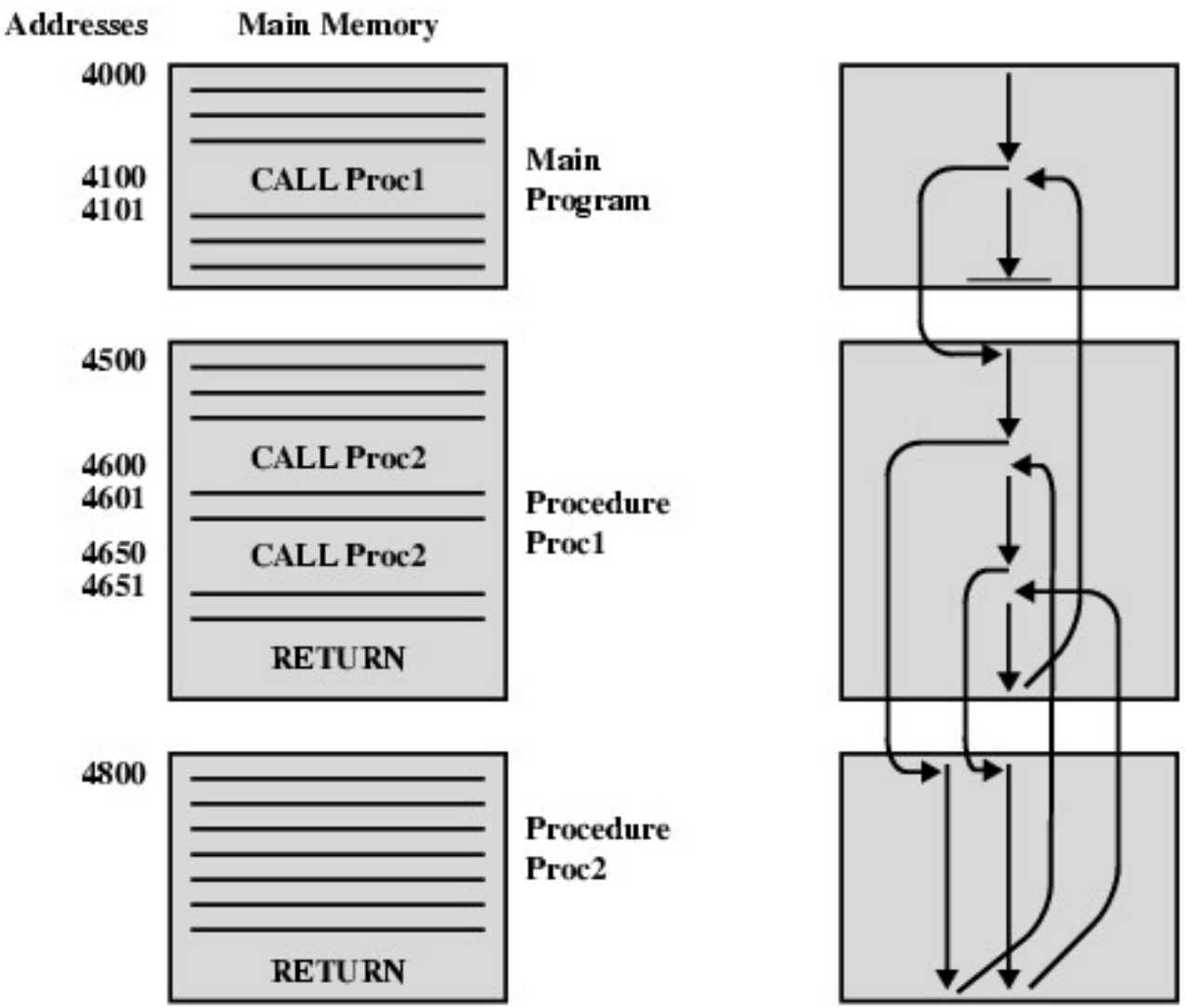
Transfer of Control

- Branch
  - e.g. branch to x if result is zero
- Skip
  - e.g. increment and skip if zero
- Conditional Instruction
  - ISZ Register1
  - Branch xxxx
  - BNZ xxxx
  - BP xxxx
- Subroutine call
  - interrupt call

Branch Instruction



Nested Procedure Calls



Computer System

Hardware: Implement the Instruction Set

Software: Program consists of instructions
- To solve a particular problem

Computer System

How to start a computer?

- Is it possible to provide all required instruction?
- We write software for some function

Firmware:

- BIOS (Basic Input/Output System)

OS (Operating System)

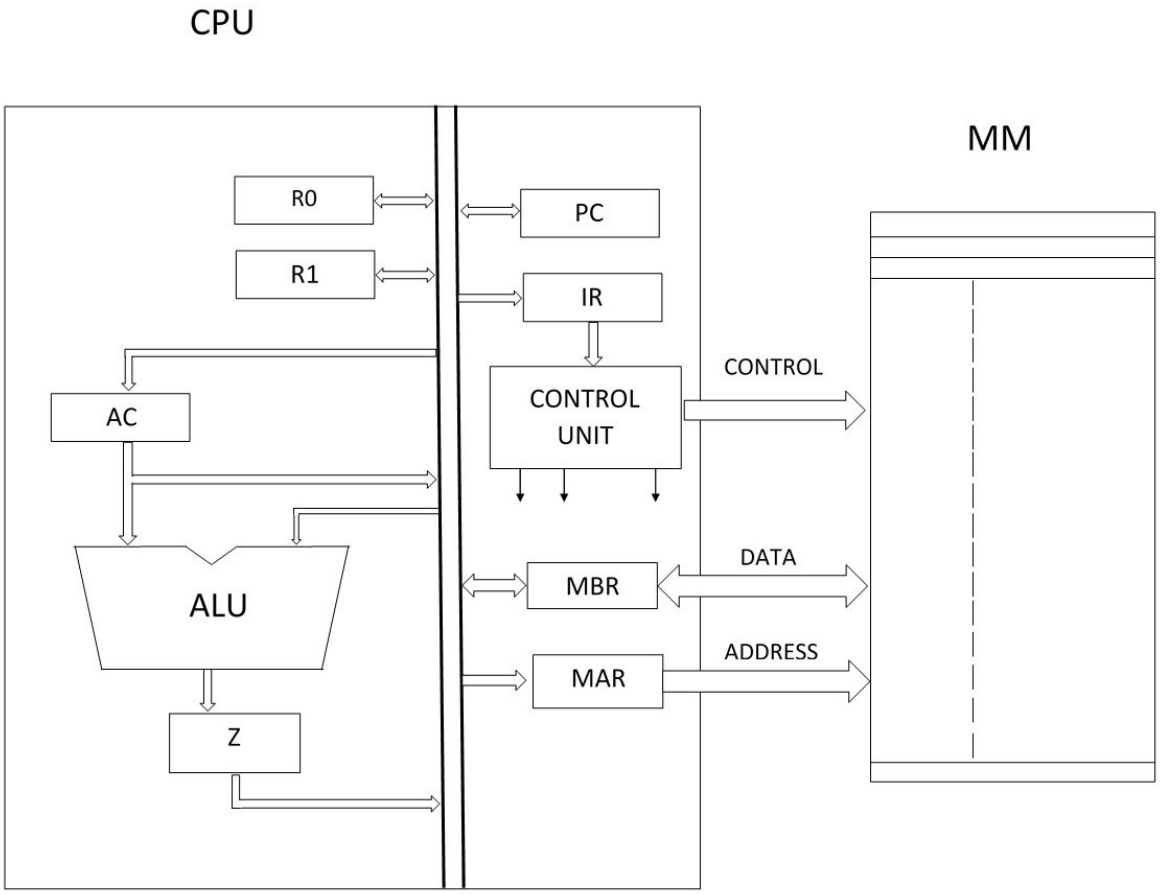
- May be considered as extended machine instructions

Computer Paradigm

CISC: Complex Instruction Set Computer

RISC: Reduced Instruction Set Computer

CPU Organization



Fetch Cycle:

MAR <- PC
Read
PC <- PC+1
IR <- MBR

Discussion

- Instruction: MOV R1, R2

Fetch phase:

T1: MAR <- PC, Read

T2: MBR <- Memory

PC <- PC + 1

T3: IR <- MBR

Execution Phase

T4: R1 <- R2

Operating frequency of the processor: 2 GHz

Discussion

Reference

Computer Organization and Architecture –
Designing for Performance
William Stallings

Chapter 10: Page no. 347 – 359 (Seventh Edition)
Page No:. 356 – 374 (Eighth Edition)