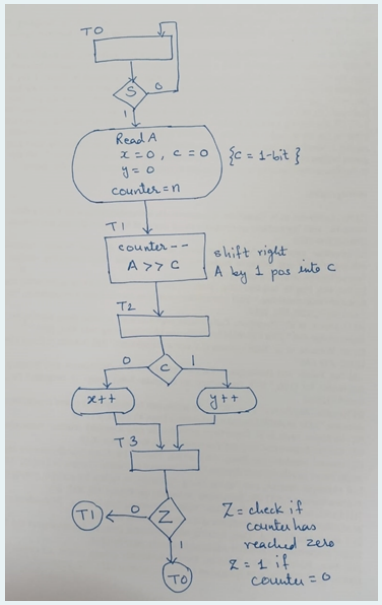
CS224_2021_quiz3_B

Points: 24/24

1



For the ASM chart given in the figure write the Verilog code and answer the question from Q-2 onward.
Inputs = clk, reset, S, A
Outputs = x, y
The other variables in the chart can be used as temporary internal variables in your code.

See q2 for declarations

2

Write the Verilog code statements to change the current state. Use the variable names as mentioned above.
(2/2 Points)

```
// DECLARATIONS :
module partb(
clk,
reset,
S,
A,x, y
);
input clk;
input reset;
input S;
input [3:0] A;
output reg [2:0]x;
output reg [2:0]y;

reg c;
reg [1:0] curr, next;
reg [2:0] counter = 4;
reg [3:0] tmpA;
parameter T0 = 2'b00;
parameter T1 = 2'b01;
parameter T2 = 2'b10;
parameter T3 = 2'b11;



// Q2 ANS:
always @(posedge clk or posedge reset)
begin
	if(reset) curr = T0;
	else curr = next;
end
```

3

Write Verilog code statements for the control path.
(8/8 Points)

```
always @(curr or S)
begin
	case(curr)
		T0: next = (S==1'b1) ? T1 : T0;
		T1: next = T2;
		T2: next = T3;
		T3: next = (counter==2'b00) ? T0 : T1;
	endcase
end
```

4

Write the Verilog statements for the data path
(8/8 Points)

```
always @(*)
begin
	case(curr)
		T0:
			begin
			x = 0;
			c = 0;
			y = 0;
			counter = 4;
			tmpA= A;
			end
		T1:
			begin
			counter = counter - 1;
			c = tmpA[0];
			tmpA[0] = tmpA[1];
			tmpA[1] = tmpA[2];
			tmpA[2] = tmpA[3];
			tmpA[3] = 0;

			end
		T2:
			begin
				if(c == 0) x = x + 1;
				else y = y + 1;
			end
		T3: begin
			end
	endcase
end
```

5

For the testbench code given below, paste that in your testbench file and generate the output. Paste the output of the monitor after running the testbench in the space below.

```
initial begin
 clk = 0; forever clk = #5 ~clk;
end

initial begin
$monitor($time, " A=%b, x=%d, y=%d ", A, x, y);

S = 0; reset = 1; A = 4'b1001;
#10; reset = 0;
#10; S = 1;
#20; S=0;
end
```

(6/6 Points)

```
  0 A=1001, x=0, y=0
 35 A=1001, x=0, y=1
 65 A=1001, x=1, y=1
 95 A=1001, x=2, y=1
125 A=1001, x=2, y=2
145 A=1001, x=0, y=0
```

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