Write the answer in a paper and upload the scan copy of it. [Max 1 page allowed]

File Upload: 1 question from Q1. [4 marks]

Q1. A processor has 8 registers (R0, R1, .. , R7) and it uses 1-byte instruction format. There are three categories of instructions: Type-1, Type-2 and Type-3. Type-1 category consists of two instructions, each with 2 register operands. Type-2 category consists of eight instructions, each with 1 register operand. Type-3 category does not involve any operand.

(a) [1] How many instructions for Type-3 category can be incorporated in this processor?

(b) [3] The op-code of Type-1 starts from 00H, then Type-2 and so on. According to the design of instructions, assign the range of op-code in Hexadecimal for Type-1, Type-2 and Type-3 instructions respectively.

Solution

Since there are eight registers, so three bits are required for register encoding

Type-1 instructions: Two instructions: 00 rrr rrr and 01 rrr rrr

Type-2 instructions: eight instructions: 10 xxx rrr

Type-3 instructions: 11 xxx xxx

(a) Number of instructions of type-3 category: 26 = 64

(b) Range of op-code:

Type-1: 00 000 000 to 01 111 111 -> 00 H to 7F H

Type-2: 10 000 000 to 10 111 111 -> 80 H to BF H

Type-3: 11 000 000 to 11 111 111 -> C0 H to FF H

Q1. [4] A processor uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. How many bits are there in the operation code, the register code part, and the address part of the instruction code? How many op-code we may have in this processor?

Solution

Instruction format: Indirect Bit (1), Operation code (x), register code part (y), address part (z)

Since there are 64 registers, so 6 bite are needed for register encoding; y=6

Memory unit consists of 256K word, so size of address bus is 18 bits; z= 18

Number of bits in operation code: x = 32 – (1+6+18) = 32 – 25 = 7

Number of op-code for this processor: $2^7 = 128$

File Upload: 1 question from Q2. [4 marks]

Q2. [4] An instruction *ADD R1, D* (R1 = R1+D) is stored at memory location 200EH. D is the immediate data which is available in next memory word and R1 is a processor register. Each instruction is 32-bit long. Word size of memory is 32 bits and it is byte addressable. What are the values of PC and MAR after execution of the instruction?

Solution

Instruction is stored in memory location 200E.

Since the memory is byte addressable and word length is 4 bytes, so immediate data D is stored from memory location 2012.

After execution, the value of PC is 2016 and value of MAR is 2012.

Q2. [4] Consider the instruction *ADD R1, M* (R1 = R1 + [M]). M is the memory address of the operand. It is a two-word instruction – first word is the op-code and the second word is the address of the operand. Give the RTL description for the complete execution (including fetch phase) of the instruction.

Solution

T1: MAR <- PC, Read

T2: MBR <- Memory

PC <- PC+1

T3: IR <- MBR

T4 MAR <- PC, Read

T5: MBR <- Memory

PC <- PC + 1

T6: MAR <- MBR, Read

T7: MBR <- Memory

T8: R1 <- R1 + MBR

File Upload: compulsory question for all. [4 marks]

Q3. [4] The size of the word of a memory module is 4 bytes and the memory is byte addressable. The provision is provided for accessing one byte and two bytes also. Give the give the scheme to access one byte, two bytes and whole word with appropriate control signals.

Solution

To identify byte, two-bytes word (S_2B) and whole word (S_4B), we need two additional control signals (S_2B and S_4B). Consider n bit address bus. The scheme to access one byte, two bytes and whole word is as follows:

S_4B	S_2B	A_{n-1} ..... A_2	A_1	A_0	
0	0	xxx x	0	0	single byte (0^{th} byte of the word)
0	0	xxx x	0	1	single byte (1^{st} byte of the word)
0	0	xxx x	1	0	single byte (2^{nd} byte of the word)
0	0	xxx x	1	1	single byte (3^{rd} byte of the word)
0	1	xxx x	0	0	lower two bytes of the word
0	1	xxx x	1	0	higher two bytes of the word
1	X	xxxx x	0	0	whole word

File Upload: 1 question from Q4. [4 marks]

Q4. Consider a DRAM chip of capacity 256 KB and each memory location contains 8 bits. The memory chip is organized in matrix form with equal number of rows and column for each memory location of 8 bits. This DRAM chip has a refresh interval of 64 ms, memory bus runs at 200 MHz, and the refresh cycle takes 4 clock cycle.

a) [3] Time required to refresh the DRAM chip.
b) [1] What is the minimum size of the refresh counter?

Solution

256 KB = 2^18 x 8 = 2^9 x 2^9 x 8 = 512 x 512 x 8

DRAM chip has 512 rows and 512 columns

(a) Length of refresh cycle = 4/200 MHz = 0.02 * 10^-6 s = 20 ns

Time required to refresh = length of refresh cycle * no. of rows = 20 ns * 512 = 10240 ns = 10.240 micro second

(b) Minimum size of refresh counter is 9 bits (2^9 = 512 rows)

Q4. Consider a DRAM chip of capacity 1 MB and each memory location contains 8 bits. The memory chip is organized in matrix form with equal number of rows and column for each memory location of 8 bits. This DRAM chip has a refresh interval of 64 ms, memory bus runs at 400 MHz, and the refresh cycle takes 4 clock cycle.

a) [3] Time required to refresh the DRAM chip.
b) [1] What is the minimum size of the refresh counter?

Solution

1 MB = 2^20 x 8 = 2^10 x 2^10 x 8 = 1024 x 1024 x 8

DRAM chip has 1024 rows and 1024 columns

(a) Length of refresh cycle = 4/400 MHz = 0.01 * 10^-6 s = 10 ns

Time required to refresh = length of refresh cycle * no. of rows = 10 ns * 1024 = 10240 ns = 10.240 micro second

(b) Minimum size of refresh counter is 10 bits (2^10 = 1024 rows)

File Upload: 1 question from Q5. [10 marks] Write the answer in a paper and upload the scan copy of it. [Max 2 pages allowed]

Q5. 2M x 32 memory module is constructed using 256K x 8 memory chips with enable line. The lower address bits A0, A1, etc. are directly connected to the address lines of all the memory chips.

a) [2] How many memory chips are needed to construct the given memory module?
b) [4] Show the schematics diagram of the arrangement with all address and data lines.
c) [4] What are the range of addresses of the memory words of last row of memory chips of your arrangements?

Solution

a) For one word we need 4 memory chips of 256K x 8. For 2M location we need 8 memory chips of 256K location. So, total memory chips requirement is 4 x 8 = 32

b) For 2M memory location, size of address bus is 21. 18 address lines are needed for 256K location and 3 lines are needed to select a row out of 8 rows of memory chips.

A20, A19 and A18 address lines are used to select a row of memory chips and address lines A17, A16, ... A1, A0 are directly connected to the address lines of memory chips.

N.B. Draw the schematic diagram properly

c) Range of addresses for the last row of the memory module: 1C0000 H - 1FFFFF H

Q5. 2M x 32 memory module is constructed using 512K x 8 memory chips with enable line. The lower address bits A0, A1, etc. are directly connected to the address lines of all the memory chips.

a) [2] How many memory chips are needed to construct the given memory module?
b) [4] Show the schematics diagram of the arrangement with all address and data lines.
c) [4] What are the range of addresses of the memory words of second row of memory chips of your arrangements?

Solution

a) For one word we need 4 memory chips of 512K x 8. For 2M location we need 4 memory chips of 512K location. So, total memory chips requirement is 4 x 4 = 16

b) For 2M memory location, size of address bus is 21. 19 address lines are needed for 512K location and 2 lines are needed to select a row out of 4 rows of memory chips.

A20 and A19 address lines are used to select a row of memory chips and address lines A18, A17, A16, ... A1, A0 are directly connected to the address lines of memory chips.

N.B. Draw the schematic diagram properly

c) Range of addresses for the last row of the memory module: 080000 H – 0FFFFF H

File Upload: 1 question from Q6. [10 marks]

Q6. Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The block size is 128 bytes and size of one memory location is 2 bytes. The main memory consists of 1K blocks.

a) What is the total capacity of the main memory and cache memory?
b) Give the format of the memory address showing TAG field, etc.
c) The request for memory blocks is in the following order:
0, 255, 1, 4, 3, 8, 133, 159, 92, 129, 63, 8, 48, 32, 73, 216, 155, 159, 255
Which of the above memory blocks will NOT be in cache if LRU replacement policy is use?

Solution

Number of cache block = 16

Number of main memory block = 1K = 1024

Block size is 128 bytes and size of one memory location is 2 bytes

(a) Total capacity of main memory = 1 K * 128 = 128 KB

Total memory location = 128K/2 = 64 K (since size of one memory location is 2 bytes) = 2^16

Total capacity of cache memory = 16 * 128 = 2^4*2^7 = 2^11 = 2 KB

(b) Block size is 128 bytes, so number of words in a block is 64 = 2^6

Number of set = 16/4 = 4 = 2^2

Format of memory address : TAG: 8 SET: 2 WORD: 6

(c) Mapping function: cache set = block MOD 4

Set0: 0 4 8 92 48 32 216

Set1: 1 133 129 73

Set2:

Set3: 255 3 159 63 155 255

Memory blocks 0, 4, 92 and 3 will not be in cache if LRU replacement policy is used.

Q6. Consider a 4-way set associative cache (initially empty) with total 32 cache blocks. The block size is 256 bytes and size of one memory location is 2 bytes. The main memory consists of 1K blocks.

a) [4] What is the total capacity of the main memory and cache memory?
b) [3] Give the format of the memory address showing tag, index and offset fields.
c) [3] The request for memory blocks is in the following order:
0, 255, 1, 4, 3, 8, 133, 159, 92, 129, 63, 8, 48, 32, 73, 216, 155.
Which of the above memory blocks will NOT be in cache if LRU replacement policy is use?

Solution

Number of cache block = 32

Number of main memory block = 1K = 1024

Block size is 256 bytes and size of one memory location is 2 bytes

(a) Total capacity of main memory = 1 K * 256 = 256 KB

Total memory location = 256K/2 = 128 K (since size of one memory location is 2 bytes) = 2^17

Total capacity of cache memory = 32 * 256 = 2^5*2^5 = 2^13 = 8 KB

(b) Block size is 256 bytes, so number of words in a block is 128 = 2^7

Number of set = 32/4 = 8 = 2^3

Format of memory address : TAG: 7 SET: 3 WORD: 7

(c) Mapping function: cache set = block MOD 8

Set0: 0 8 48 32 216

Set1: 1 129 73

Set2:

Set3: 3 155

Set4: 4 92

Set5: 133

Set6:

Set7: 255 159 63

Memory block 0 will not be in cache if LRU replacement policy is used.

File Upload: 1 question from Q7. [6 marks]

Write the answer in a paper and upload the scan copy of it. [Max 1 page allowed]

Q7. [6] A microprocessor is clocked at a rate of 2.5 GHz. This microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching an initial decoding of the instruction takes 12 clock cycles. Thereafter, it takes 8 clock cycles to transfer each byte.

a) How long is a clock cycle for this microprocessor?
b) Determine the length of the instruction cycle for the case of a string of 50 bytes.
c) What is the worst case delay for acknowledging an interrupt if the instruction is non interruptible?
d) What are the worst-case and average case delay for acknowledging an interrupt if the instruction can be interrupted at the beginning of each byte transfer?

Solution

Clock cycle time = 1/(2.5 GHz) = 0.4 ns
Length of instruction cycle = 12 + 50*8 = 412 clock cycle = 412 * 0.4 ns = 164.8 ns

If the interrupt may arrive at any point of time and it is not interruptible, then the worst case delay in acknowledging the interrupt is as follows.

Assume that the interrupt arrives immediately after the fetch has started, if the interrupt is non interruptible, it will be acknowledged only after the current instruction cycle.

Hence, delay in acknowledging = Length of the instruction cycle time = 164.8 ns

If the interrupt may arrive at any point of time and can be acknowledged at the start of each byte transfer, then the worst case and average case delay in acknowledging the interrupt is as follows.

Let us analyse the worst case delay first. In this case, the interrupt will arrive immediately after the fetch has started. Hence, the interrupt has to wait till the fetch is completed. That gives us the worst case delay as 12 cycles = 12 × 0.4 = 4.8 ns.

The average case analysis is as follows:

Case 1: The interrupt arrives during the fetch cycle. Average delay: 12/2 = 6 clock cycles

Case 2: The interrupt arrives during the transfer of a byte. Average delay: 8/2 = 4 clock cycles

Hence, the average delay is (6 + 50 *4)/51 = 206/51 = 4.039 cycles = 4.039 * 0.4 ns = 1.616 ns

Q7. [6] A microprocessor is clocked at a rate of 2 GHz. This microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching an initial decoding of the instruction takes 15 clock cycles. Thereafter, it takes 10 clock cycles to transfer each byte.

a) How long is a clock cycle for this microprocessor?
b) Determine the length of the instruction cycle for the case of a string of 60 bytes.
c) What is the worst case delay for acknowledging an interrupt if the instruction is non interruptible?
d) What are the worst-case and average case delay for acknowledging an interrupt if the instruction can be interrupted at the beginning of each byte transfer?

Solution

lock cycle time = 1/(2 GHz) = 0.5 ns

Length of instruction cycle = 15 + 60*10 = 615 clock cycle = 615 * 0.5 ns = 307.5 ns

If the interrupt may arrive at any point of time and it is not interruptible, then the worst case delay in acknowledging the interrupt is as follows.

Assume that the interrupt arrives immediately after the fetch has started, if the interrupt is non interruptible, it will be acknowledged only after the current instruction cycle.

Hence, delay in acknowledging = Length of the instruction cycle time = 307.5 ns

If the interrupt may arrive at any point of time and can be acknowledged at the start of each byte transfer, then the worst case and average case delay in acknowledging the interrupt is as follows.

Let us analyse the worst case delay first. In this case, the interrupt will arrive immediately after

the fetch has started. Hence, the interrupt has to wait till the fetch is completed. That gives us the worst case delay as 15 cycles = 15 × 0.5 = 7.5 ns.

The average case analysis is as follows:

Case 1: The interrupt arrives during the fetch cycle. Average delay: 15/2 = 7.5 clock cycles

Case 2: The interrupt arrives during the transfer of a byte. Average delay: 10/2 = 5 clock cycles

Hence, the average delay is (7.5 + 60 *5)/61 = 307.5/61 = 5.041 cycles = 5.041 * 0.5 ns = 2.52 ns

File Upload: 1 question from Q8. [3 marks]

Q8. [1+2] A manufacturer wishes to design a hard disk with a capacity of 30 GB (using the standard definition of 1GB =2^30 bytes). If the technology used to manufacture the disks allows 1024-byte sectors, 512 sectors/track, and 4096 tracks/platter, what is the minimum number of platters required to design this hard disk? (Assume a fixed number of sectors per track.). If the rotational speed of the disk is 15000 rpm, what is the transfer time to transfer a sequential file of size 1.2 MB.

Solution

Size of sector = 1024 bytes number of sector per track = 512 number of tracks per platter = 4096

Total capacity of a platter 1024 * 512 * 4096 = 2^10 * 2^9 * 2*12 = 2^31 = 2GB

Minimum Number of platters needed for 30GB is 15

R = Rotational speed = 15000 rpm = 15000/60 = 250 revolution per second

N = Capacity of a track = 1024 * 512 bytes = 2^19 Bytes

B = Size of sequential file is 1.2 MB = 1.2 * 2^20 Bytes

Transfer time T = B/RN = 1.2*2^20/(250*2^19)=1.2*2/250=2.4/250= 0.0096 seconds = 9.6 millisecond

Q8. [1+2] A manufacturer wishes to design a hard disk with a capacity of 30 GB (using the standard definition of 1GB =2^30 bytes). If the technology used to manufacture the disks allows 512-byte sectors, 1024 sectors/track, and 2048 tracks/platter, what is the minimum number of platters required to design this hard disk? (Assume a fixed number of sectors per track.). If the rotational speed of the disk is 20000 rpm, what is the transfer time to transfer a sequential file of size 1.8 MB.

Solution

Size of sector = 512 bytes number of sector per track = 1024 number of tracks per platter = 2048

Total capacity of a platter 512 * 1024 * 2048 = 2^9 * 2^10 * 2*11 = 2^30 = 1GB

Minimum Number of platters needed for 30GB is 30

R = Rotational speed = 20000 rpm = 20000/60 = 333.33 revolution per second

N = Capacity of a track = 1024 * 512 bytes = 2^19 Bytes
B = Size of sequential file is 1.8 MB = 1.8 * 2^20 Bytes
Transfer time T = B/RN = 1.8*2^20/(333.33*2^19)=1.8*2/333.33=3.6/333.33= 0.0108 seconds = 10.8 millisecond