COL215P: ASSIGNMENT 8

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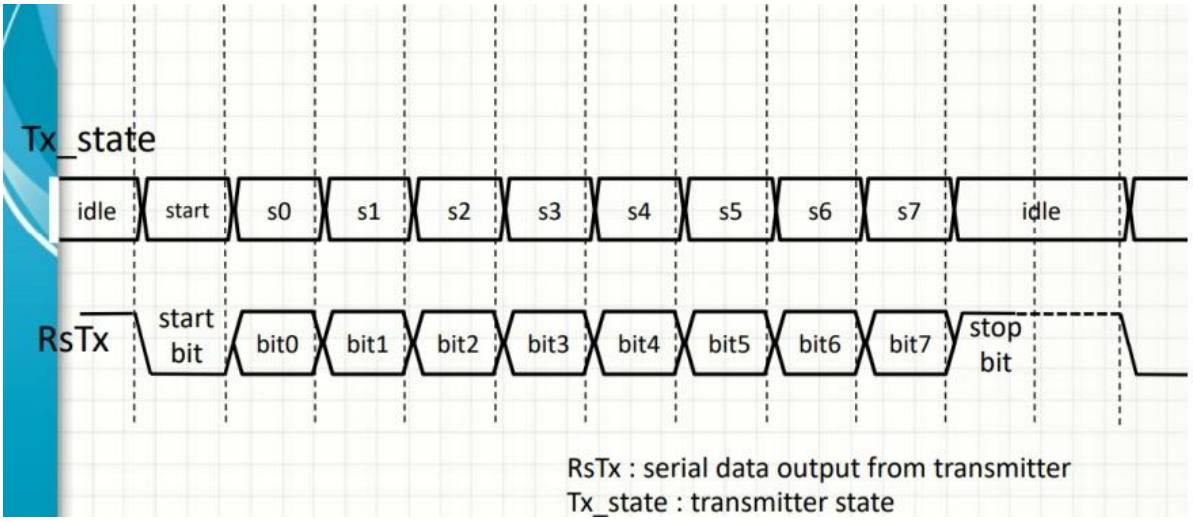
Objective:

- Design and implementation of a serial asynchronous transmitter and connecting the parallel output of the receiver to the parallel input of the transmitter to form a loop. This will be used to demonstrate that the data sent from the PC is echoed back to it through the receiver/transmitter pair.

Implementation Overview:

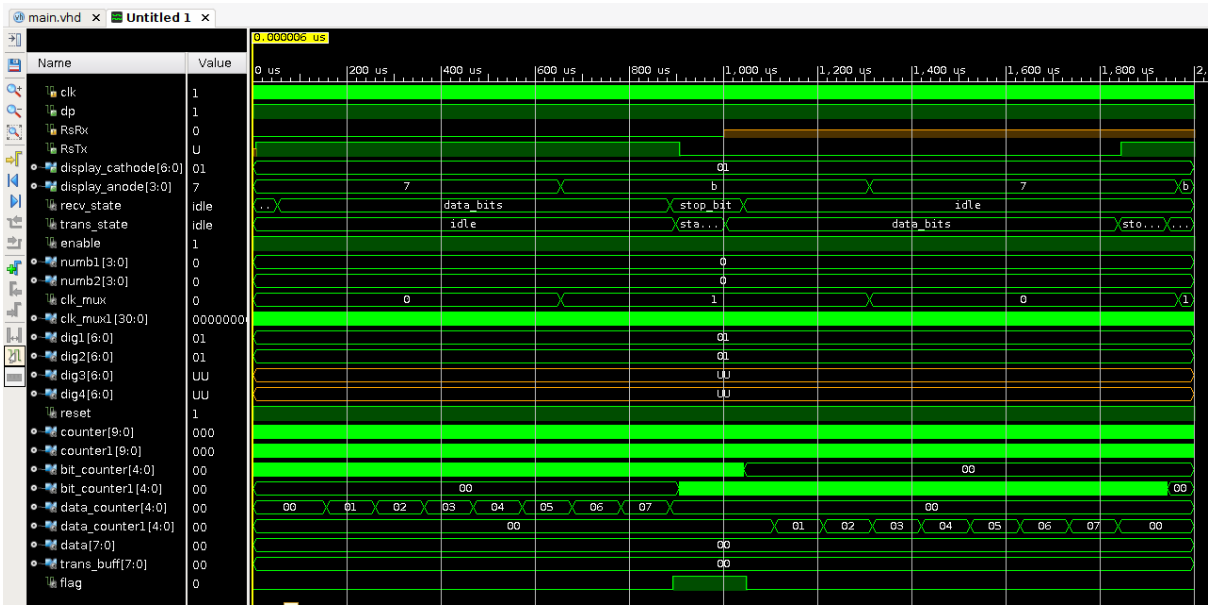
- We use the code of asynchronous serial receiver from the previous assignment.

- There are four states of the transmitter - idle, start, data and stop state. The states of the transmitter are shown below:



- The transmitter is in the idle state when it is not transmitting any data. As soon as the receiver receives the data, the transmitter enters the start state. Then, it sends the 8 data bits and the stop bit. Finally, the transmitter returns back to the idle state.

Simulation:

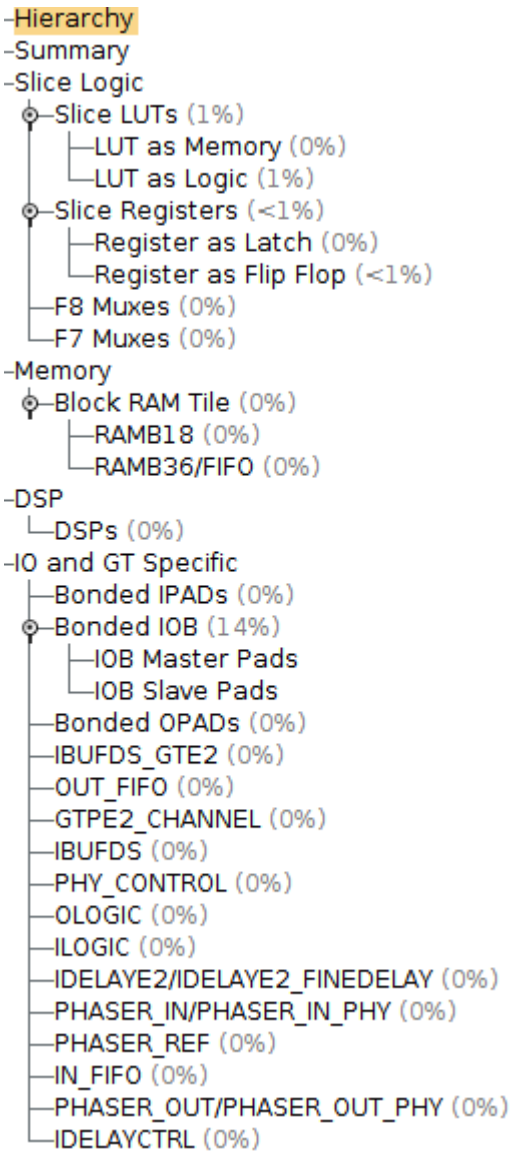

main.vhd
Untitled 1
Name
Value
clk
dp
RsRx
RsTx
display_cathode[6:0]
display_anode[3:0]
recv_state
trans_state
enable
numb1[3:0]
numb2[3:0]
clk_mux
clk_mux1[30:0]
dig1[6:0]
dig2[6:0]
dig3[6:0]
dig4[6:0]
reset
counter[9:0]
counter1[9:0]
bit_counter[4:0]
bit_counter1[4:0]
data_counter[4:0]
data_counter1[4:0]
data[7:0]
trans_buff[7:0]
flag
0.000006 us
0 us
200 us
400 us
600 us
800 us
1,000 us
1,200 us
1,400 us
1,600 us
1,800 us
data_bits
stop_bit
idle
sta...
sto...

Resource utilisation:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
main	97	83	15	1
create_mux_clock (ti...	26	17	0	0

Resource	Utilisation No.	Utilisation %
Slice LUTS	97	1
Slice Registers	83	< 1
F7 Muxes	0	0
BUFGCTRL	1	3
Bonded IOBs	15	14
DSP	0	0



FPGA Observation: