COL215P: ASSIGNMENT 4

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Objective:

- Controlling brightness of the LED of the 7-segment displays using pulse width modulation.

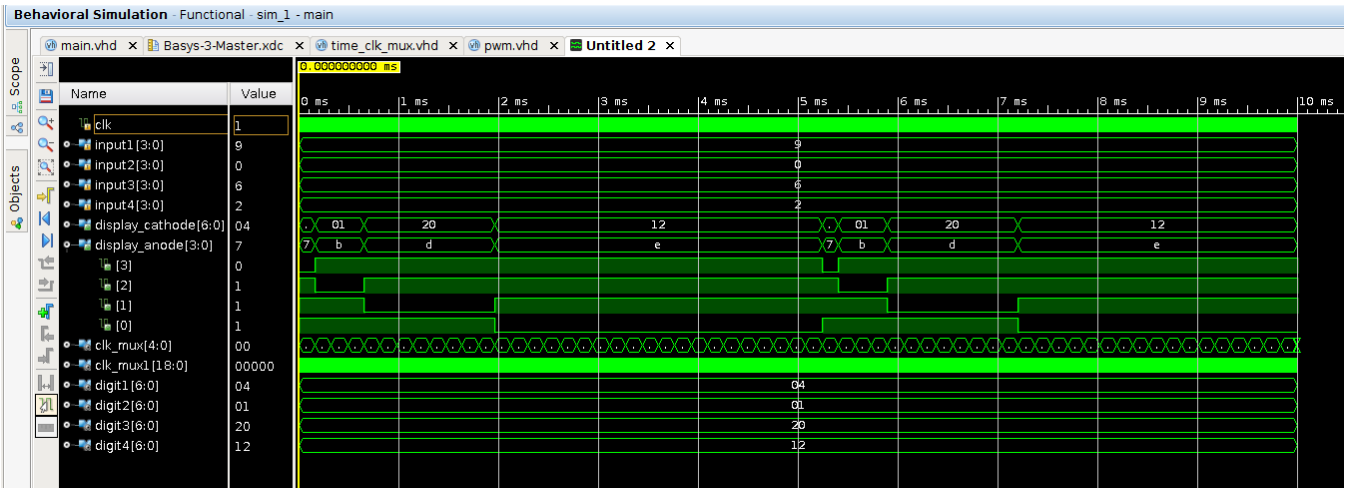
- This is extension of Assignment 3 where we want the leftmost digit to of the highest brightness and lowest on the rightmost display.

Implementation Overview:

- We are using a five bit clk_mux variable for controlling the brightness of the the LEDS.

- If the value of variable is 0, the rightmost display is lit. If the value of the variable is 1-3, then the 2nd display is lit. If the value of the variable is 4-11, then the 3rd display is lit. For the remaining 21 values leftmost display is lit. Thus, the birghtness decreases from left to right.

Simulation:



Resource utilisation:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
main	33	19	16	33	1	28	1
create_mux_clock (ti...	23	19	13	23	1	0	0

Resource	Utilisation Count	Utilisation %
Slice LUTS	33	< 1
Slice Registers	19	< 1
LUT as Logic	33	< 1
LUT as Flip-flop	1	< 1
Bonded IOBs	28	26
BUFGCTRL	1	< 1

Utilization - utilization_1

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (<1%)
    - F8 Muxes (0%)
    - F7 Muxes (0%)
  - Slice Registers (<1%)
- Slice Logic Distribution
  - Slice (<1%)
  - LUT as Memory (0%)
  - LUT Flip Flop Pairs (<1%)
  - LUT as Logic (<1%)
    - using O5 and O6
    - using O5 output only
    - using O6 output only
- Memory
- DSP
- IO and GT Specific
  - Bonded IPADs (0%)
  - OUT_FIFO (0%)
  - IBUFDS (0%)
  - PHY_CONTROL (0%)
  - IDELAYE2/IDELAYE2_FINEDELAY (0%)
  - PHASER_IN/PHASER_IN_PHY (0%)
  - IN_FIFO (0%)
  - PHASER_OUT/PHASER_OUT_PHY (0%)
  - IDELAYCTRL (0%)
  - Bonded IOB (26%)

FPGA Observation: