COL215P: ASSIGNMENT 3

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Objective:

- We have designed a combination circuit that takes a decimal/hexadecimal digit encoded using 4 bits and produces 7-bit output for seven-segment displays of the BASYS3 FPGA board.

- This is extension of Assignment 2 from a single digit display to a multi-digit display by introducing proper timing and refreshing signals by using on-board clock.

Implementation Overview:

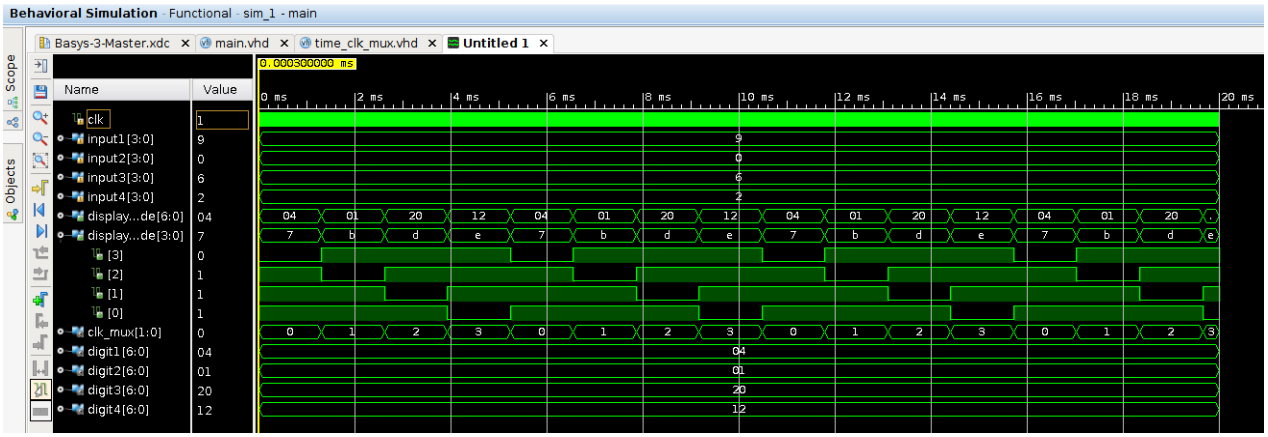
- We have used 7 segment display code of assignment 2 to generate output of one digit corresponding to the respective 4-bit input.

- We have used a 4:1 multiplexer for selecting the one of the 4 7-segment display.

- The 2 bit select input of the multiplexer is the last two bit of 19 bit counter which is incremented on every rising edge of the clock.

- Thus, the refresh rate of the display is 10^8/2^17, which is 6.8 * 10^2 Hz which is greater than the persistence of vision.

Simulation:



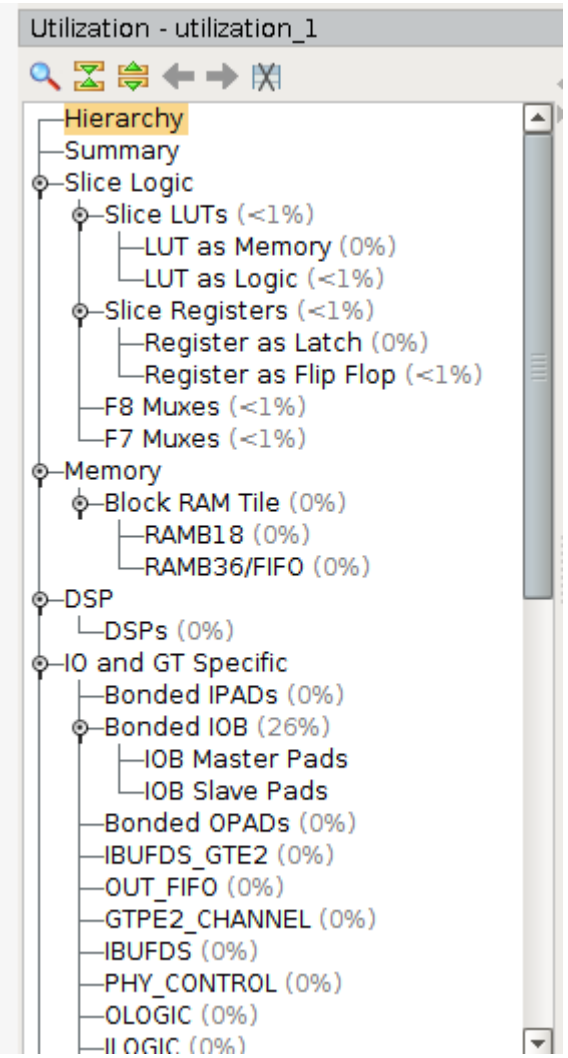
- Here, we can see that the clk_mux variable varies from 0 to 3 which is the select variable for the mux. The display_anode variable changes according to the clk_mux and display_cathode changes according to the input given from the switches corresponding to different digits.

Resource Utilisation:

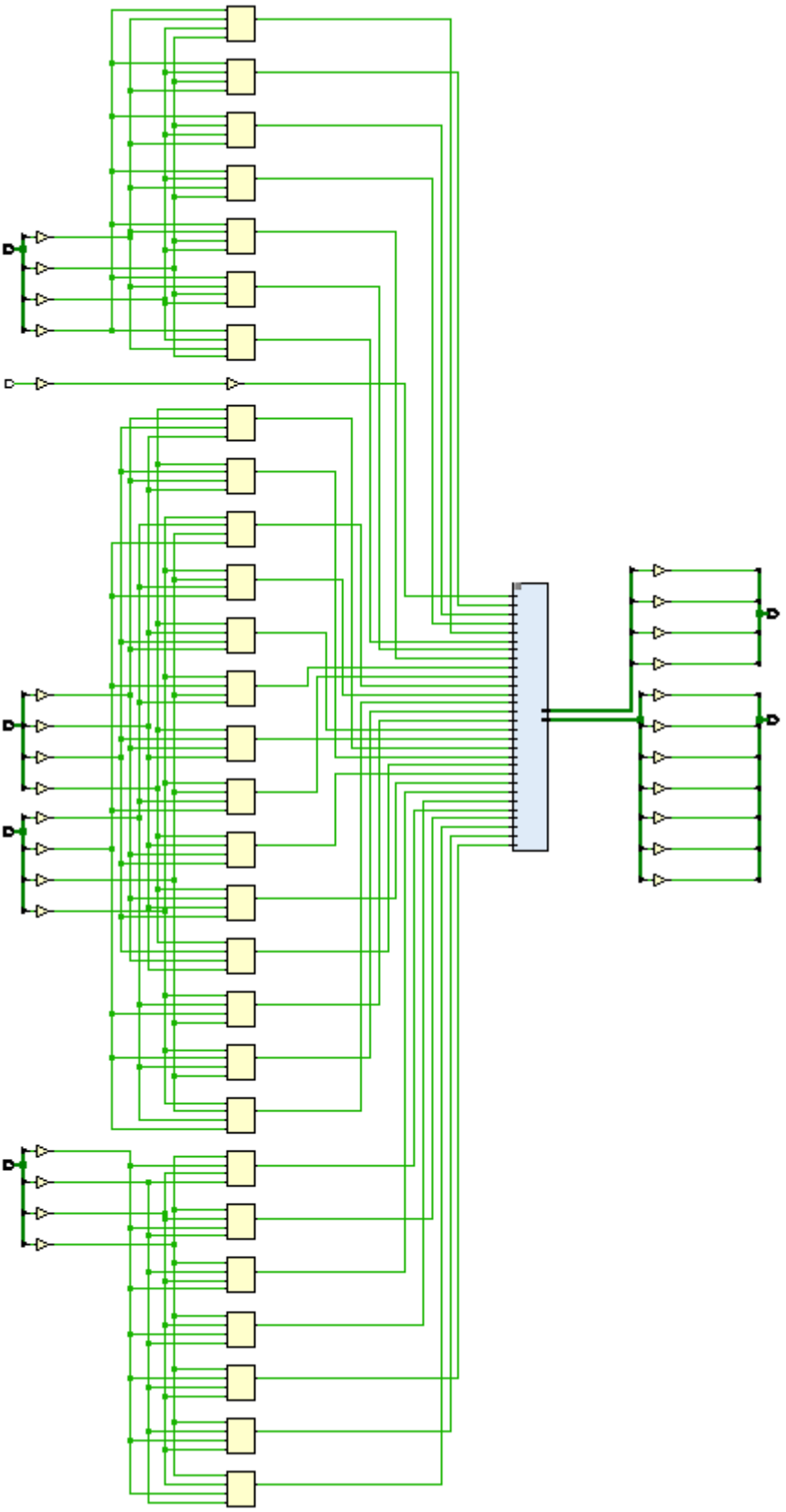
Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
main	49	19	14	7	28	1
create_mux_clock (ti...	21	19	14	7	0	0

Resource	Utilisation(Count)	Utilisation (%)
Slice LUTS	49	< 1
Slice Registers	19	< 1
F7 Muxes	14	< 1
F8 Muxes	7	< 1
Bonded IOBS	28	26
BUFGCTRL	1	< 1



Schematic:



FPGA Observation: