COL215P: ASSIGNMENT 7

Gunjan Kumar - 2019CS10353 **T Abishek - 2019CS10407**

Objective:

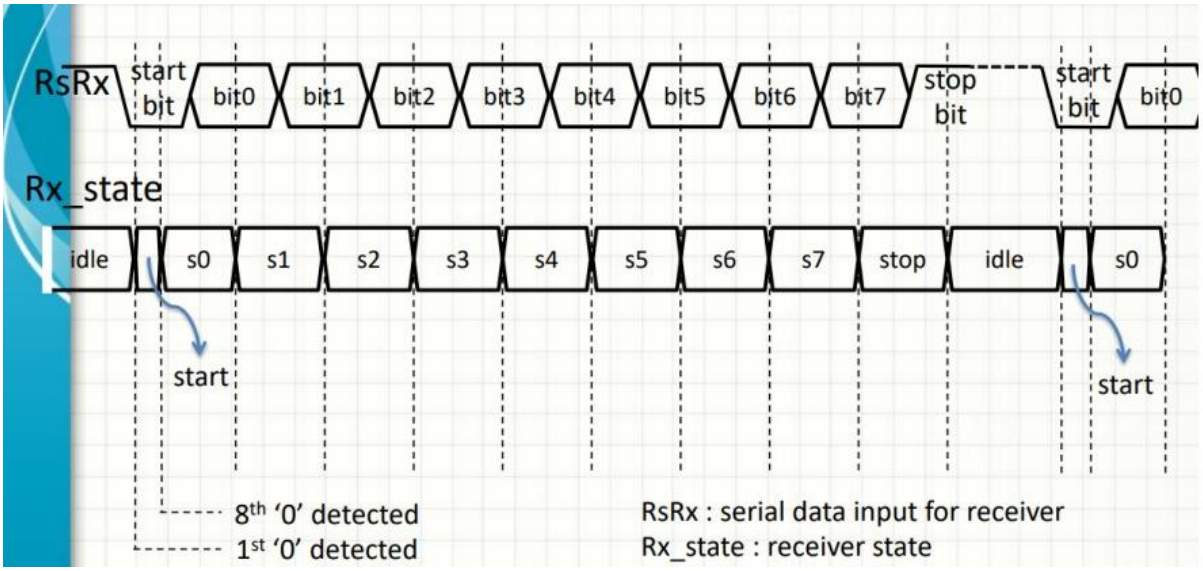
- Design asynchronous serial receiver with baud rate = 9600, 8 data bits, no parity bits and 1 stop bit.

- Display the received data bits on the 7-segmet display using the components designed in previous assignments.

Implementation Overview:

- For display the received data on the seven-segment display, we use the code of assignment 4.

- The states of the asynchronous serial receiver is shown below:

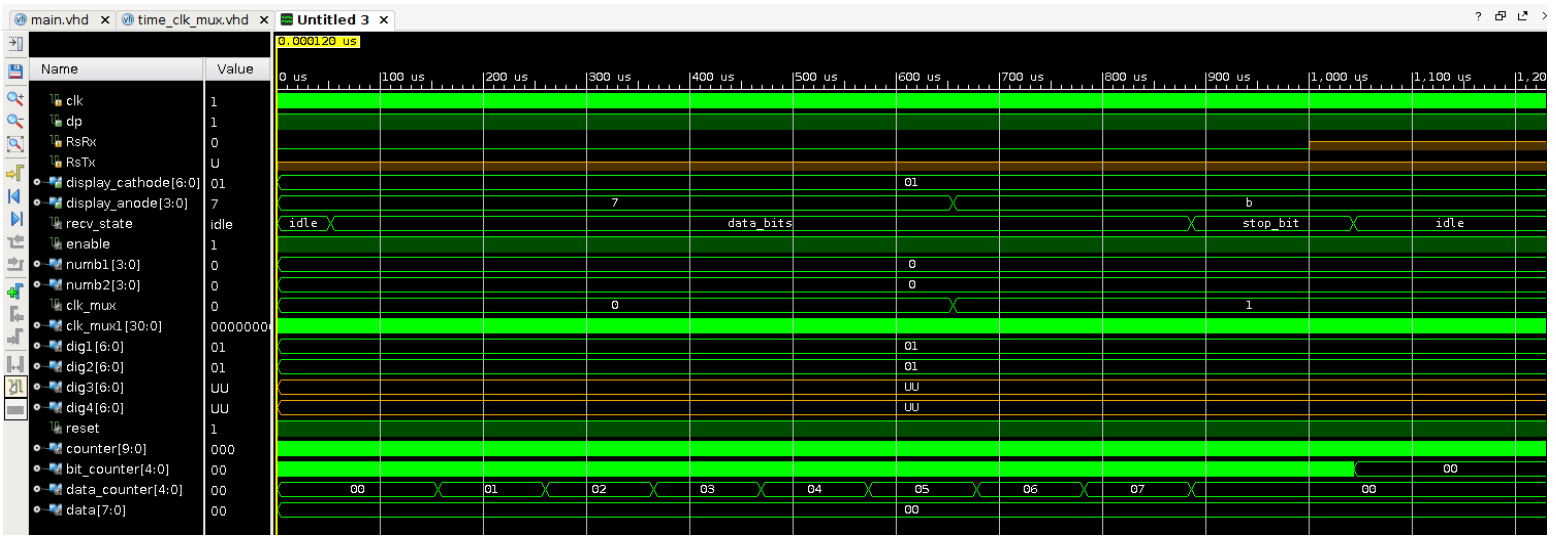


- A three-state FSM is created - idle, data and stop state. When the receiver detects a 0 in the idle state, it switches to the data state after continuously receiving 0 in eight consecutive cycles. Eight data bits are read in the data state. Then it switches to the stop state to receive the stop bit. After that, the status returns to the idle state.

- We count up to 16 before reading the current input bit to ensure that the data is read in the midcle of the cycle. This ensures correctness.

Simulation:

As seen in the simulation below, we can see the transitions of state as explained in the implementation of the receiver.

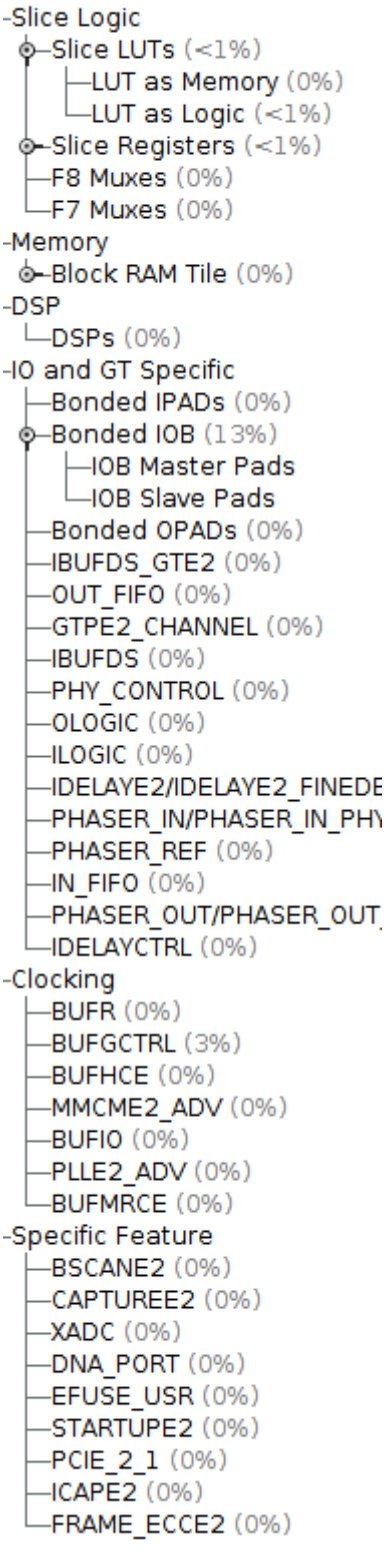


Resource utilisation:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
main	61	55	14	1
create_mux_clock (ti...	25	17	0	0

Resource	Utilisation No.	Utilisation %
Slice LUTS	61	< 1
Slice Registers	55	< 1
F7 Muxes	0	0
BUFGCTRL	1	3
Bonded IOBs	14	13
DSP	0	0



FPGA Observation: