

## COL215P: ASSIGNMENT 6

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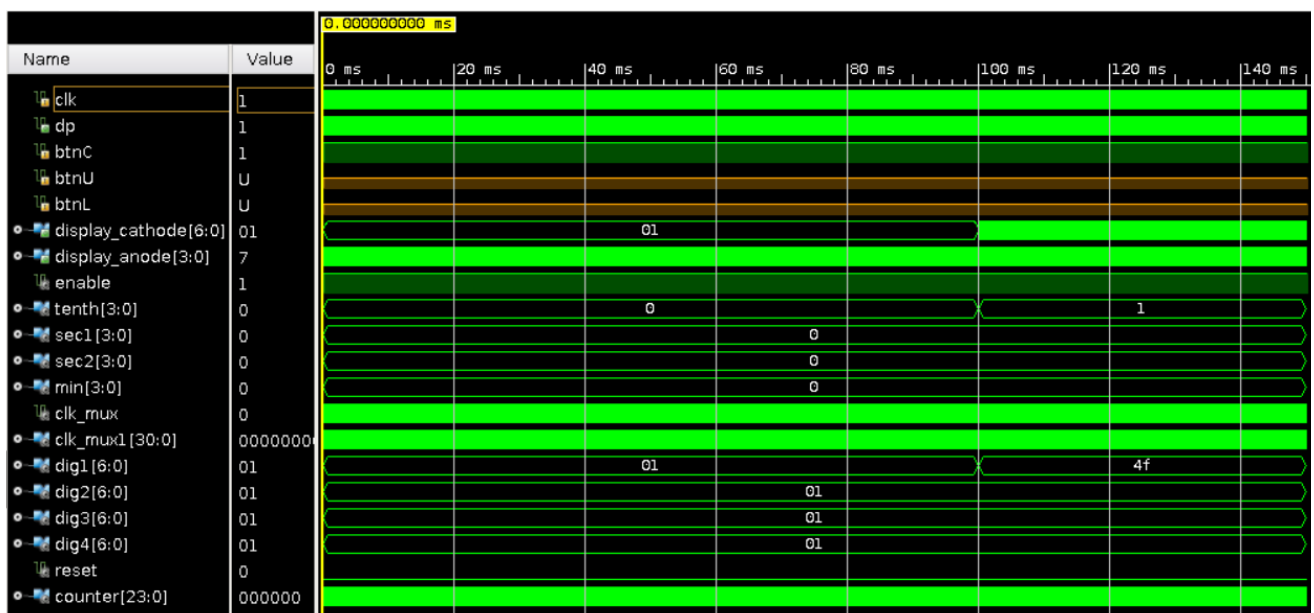
### Objective:

- Using pre-designed circuit of Assignment 3 as a building block and creation of time reference.
- Design a stopwatch and implement it on BASYS 3 board, using its 7-segment display and push buttons.

### Implementation Overview:

- We use the four-digit seven-segment display from Assignment 3.
- Tenth, sec1, sec2, and min are the four variables. For one tenth of a second, tenth stores the digit. Sec1 holds the value of the second's unit digit. The value of the tenth digit of a second is stored in Sec2, and the value of minutes is stored in min.
- We use a 24 bit counter to measure time. When the counter becomes equal to  $10^7$  and then set the counter back to 0. Since the clock is  $10^8$  Hz, thus every 0.1 sec counter gets back to zero.
- The 0.1 second digit grows by one every 0.1 second. When the 0.1 second digit goes from 9 to 10, the unit digit of second increases. When the unit digit of second shifts from 9 to 0, the tens digit of second count increases. When the second count's tens digit changes from 5 to 6, the minute counting digit changes.

### Simulation:



## Resource utilisation:

Hierarchy					
	Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Bonded IOB (106)
	main	91	60	7	16
	create_mux_clock (ti...	35	17	7	0

Resource	Utilisation No.	Utilisation %
Slice LUTs	91	1
Slice Registers	60	< 1
F7 Muxes	7	< 1
BUFGCTRL	16	
Bonded IOBs	2	
DSP	0	

-Slice Logic
○ Slice LUTs (1%)
├── LUT as Memory (0%)
└── LUT as Logic (1%)
○ Slice Registers (<1%)
├── Register as Latch (<1%)
└── Register as Flip Flop (<1%)
├── F8 Muxes (0%)
└── F7 Muxes (<1%)
-Memory
○ Block RAM Tile (0%)
├── RAMB18 (0%)
└── RAMB36/FIFO (0%)
-DSP
└── DSPs (0%)
-IO and GT Specific
├── Bonded IPADs (0%)
○ Bonded IOB (15%)
├── Bonded OPADs (0%)
├── IBUFDS_GTE2 (0%)
├── OUT_FIFO (0%)
├── GTPE2_CHANNEL (0%)
├── IBUFDS (0%)
├── PHY_CONTROL (0%)
├── OLOGIC (0%)
├── ILOGIC (0%)
├── IDELAYE2/IDELAYE2_FINEDELAY (0%)
├── PHASER_IN/PHASER_IN_PHY (0%)
├── PHASER_REF (0%)
└── IN_FIFO (0%)

## FPGA Observation:

