

## COL215P: ASSIGNMENT 9

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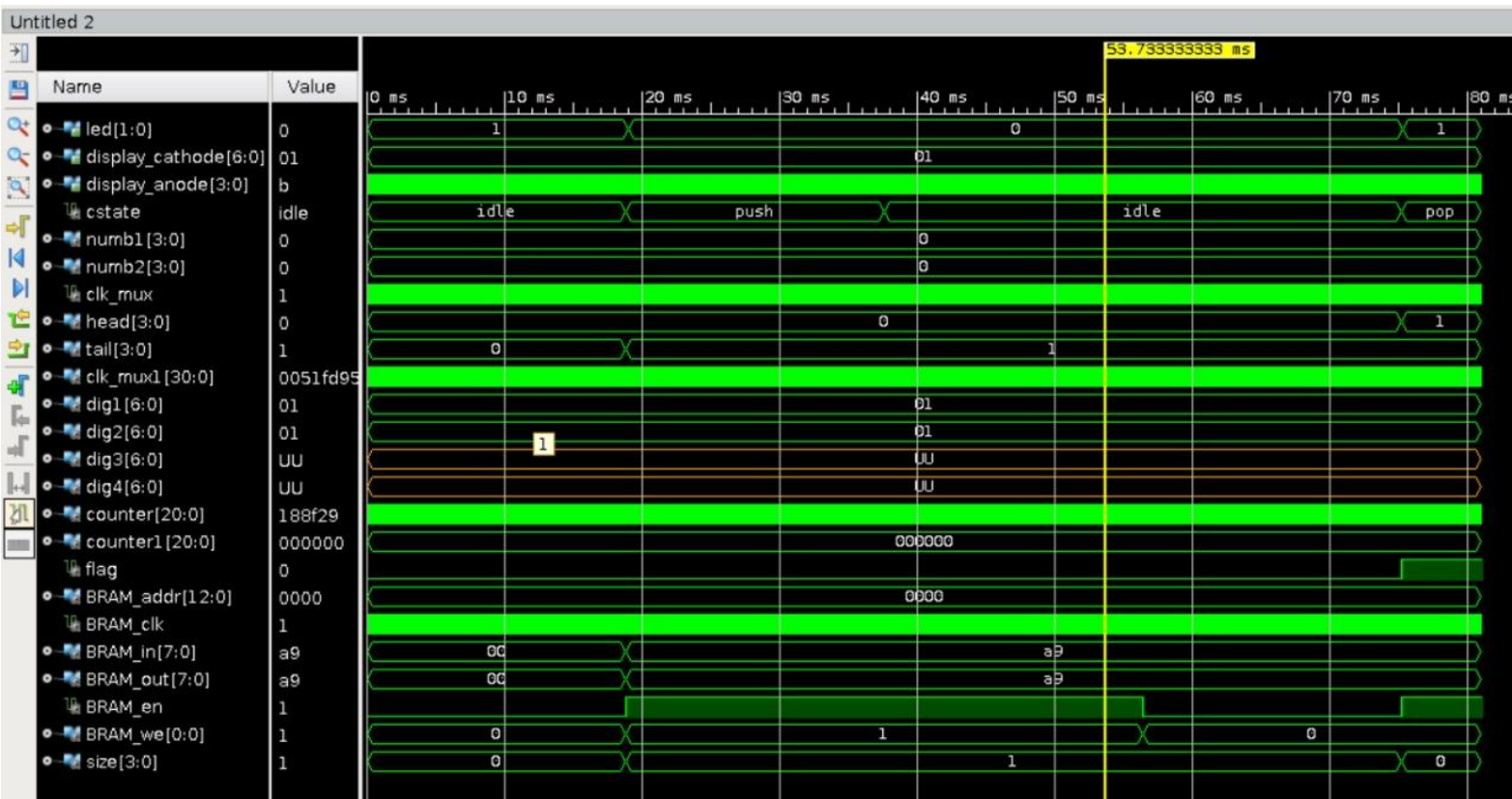
### Objective:

- Implementing memory using BRAM and then designing a FIFO with push button switches for WRITE and READ. WRITE pushes an input from the switches to the FIFO buffer whereas READ pops the head of the FIFO buffer onto a register that is displayed on the 7-segment displays.

### Implementation Overview:

- The four-digit seven-segment display from assignment 4 is used here to display the popped value.
- We create a three-state FSM - idle, pop and push. The BRAM is set to push the four-digit number received from the switch into the queue memory if the push button is pressed when the current state is idle. It is ensured that in the push state, the device does not return to idle and does not press the same four-digit number again until the push button is disengaged (set to 0).

### Simulation:



## Resource utilisation:

Hierarchy						
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
main	86	76	2	25	1	
BRAM (BRAM_wrapper)	7	2	2	0	0	
create_mux_clock (tl...	25	17	0	0	0	

Resource	Utilisation No.	Utilisation %
Slice LUTs	86	1
Slice Registers	76	< 1
BRAM	2	4
BUFGCTRL	1	3
Bonded IOBs	25	24
DSP	0	0

-Slice Logic	
Slice LUTs (1%)	
LUT as Memory (0%)	
LUT as Logic (1%)	
F8 Muxes (0%)	
F7 Muxes (0%)	
Slice Registers (<1%)	
Register as Latch (0%)	
Register as Flip Flop (<1%)	
-Memory	
Block RAM Tile (4%)	
RAMB18 (0%)	
RAMB36/FIFO (4%)	
RAMB36E1 only	
-DSP	
DSPs (0%)	
-IO and GT Specific	
Bonded IPADs (0%)	
OUT_FIFO (0%)	
IBUFDS (0%)	
PHY_CONTROL (0%)	
IDELAYE2/IDELAYE2_FINEDELAY (0%)	
PHASER_IN/PHASER_IN_PHY (0%)	
IN_FIFO (0%)	
PHASER_OUT/PHASER_OUT_PHY (0%)	
IDELAYCTRL (0%)	
Bonded IOB (24%)	
IOB Slave Pads	
IOB Master Pads	
Bonded OPADs (0%)	
IBUFDS_GTE2 (0%)	
GTPE2_CHANNEL (0%)	
OLOGIC (0%)	
ILOGIC (0%)	
PHASER_REF (0%)	

## FPGA Observation:

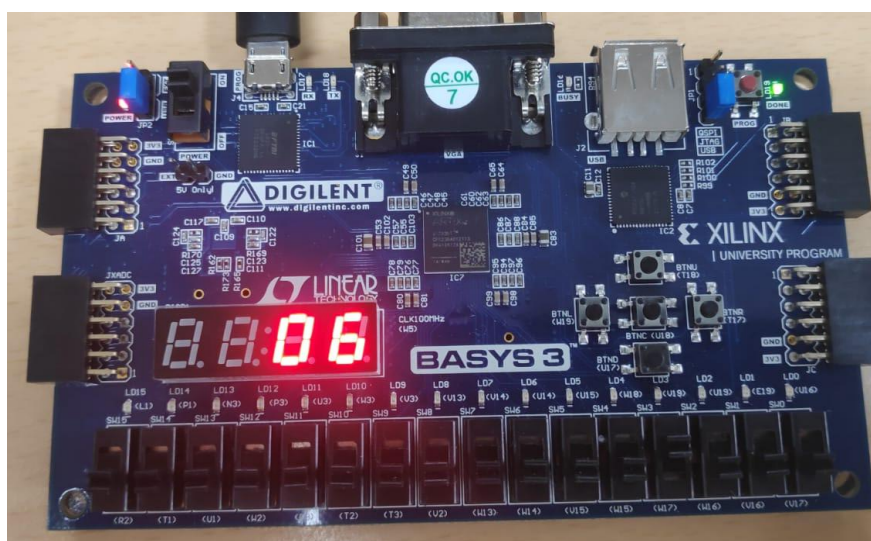


Fig 1: popped value from the queue after inserting it