COL215P: ASSIGNMENT 10

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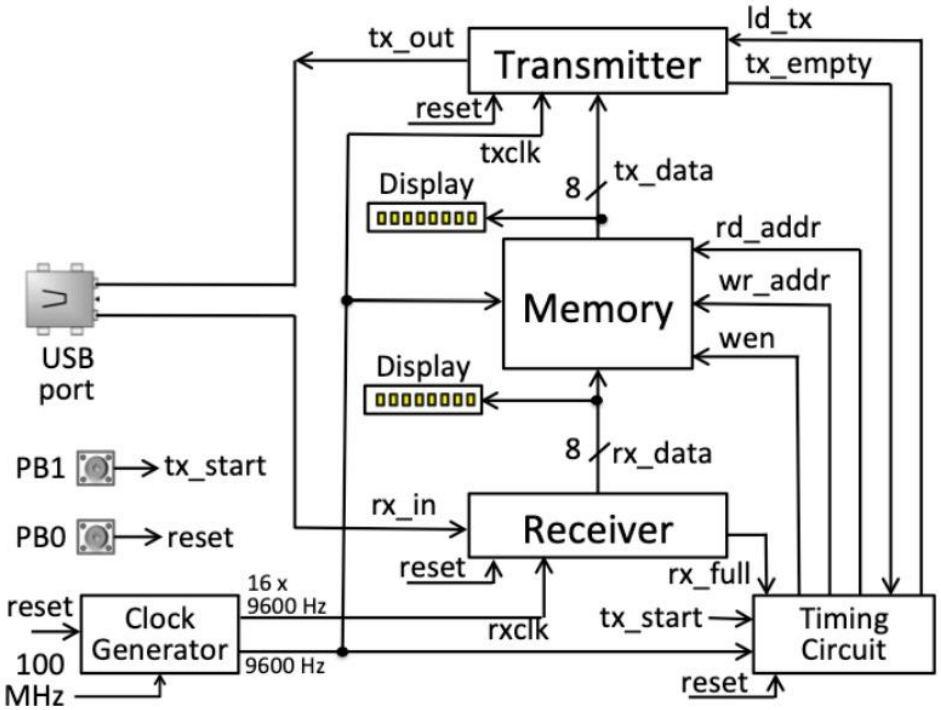
Objective:

- This assignment implements the block diagram depicted below. This device accepts a file as input via an asynchronous receiver. The received values are kept in the memory. Before initiating transmission, it waits for the button to be pressed. The memory sends the read values to the transmitter, which transmits them bit by bit.

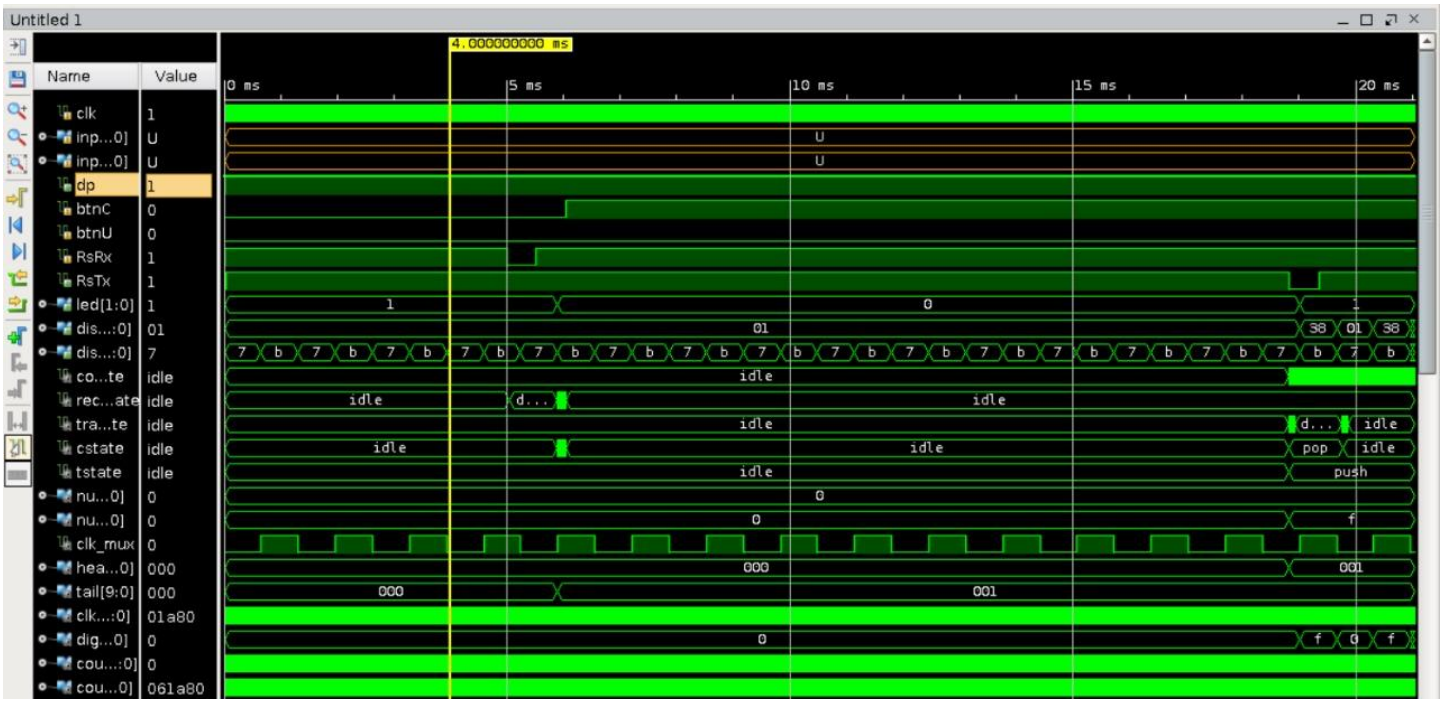


Implementation Overview:

- The transmitter and receiver constructed in A8, as well as the FIFO buffer implemented in A9, are used in this assignment.
- Initially, the fpga board waits for receiving data from the USB. When 8 bits are received, it is stored in a buffer and then uses a flag to indicate that the buffer has to be written into the BRAM. It continues doing this for all data to be received.
- Then, when the transmission button is pressed, one of the states keeps sending a flag to indicate that transmission should occur. This flag stays active until the BRAM is empty. When the flag is active, it pops the data from BRAM, and sends it to the transmitter. The BRAM popper waits until the transmitter sends the data, and when the transmitter indicates that the data

has been transferred, it pops the next one and sends it to the transmitter. This continues until everything has been transferred.

Simulation:



Resource utilisation:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
main	189	183	2	19	1
BRAM (BRAM_wrapper)	11	2	2	0	0
create_mux_clock (ti...	26	17	0	0	0

Resource	Utilisation No.	Utilisation %
Slice LUTS	189	1
Slice Registers	183	1
BRAM	2	4
BUFGCTRL	1	3
Bonded IOBs	19	18
DSP	0	0

- Slice Logic
  - Slice LUTs (1%)
    - LUT as Memory (0%)
    - LUT as Logic (1%)
  - F8 Muxes (0%)
  - F7 Muxes (0%)
  - Slice Registers (1%)
    - Register as Latch (0%)
    - Register as Flip Flop (1%)
- Memory
  - Block RAM Tile (4%)
    - RAMB18 (0%)
    - RAMB36/FIFO (4%)
      - RAMB36E1 only
- DSP
  - DSPs (0%)
- IO and GT Specific
  - Bonded IPADs (0%)
  - OUT_FIFO (0%)
  - IBUFDS (0%)
  - PHY_CONTROL (0%)
  - IDELAYE2/IDELAYE2_FINEDELAY (0%)
  - PHASER_IN/PHASER_IN_PHY (0%)
  - IN_FIFO (0%)
  - PHASER_OUT/PHASER_OUT_PHY (0%)
  - IDELAYCTRL (0%)
  - Bonded IOB (18%)
    - IOB Slave Pads
    - IOB Master Pads
  - Bonded OPADs (0%)
  - IBUFDS_GTE2 (0%)
  - GTPE2_CHANNEL (0%)
  - OLOGIC (0%)
  - ILOGIC (0%)
  - PHASER_REF (0%)

Gtkterm Observation: