COL215P: ASSIGNMENT 2

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Objective:

- The objective of this assignment is to learn how to display decimal or hexadecimal digits using 7- segment displays.

- We have designed a combination circuit that takes a decimal/hexadecimal digit encoded using 4 bits and produces 7-bit output for seven-segment displays of the BASYS3 FPGA board.

Implementation Overview:

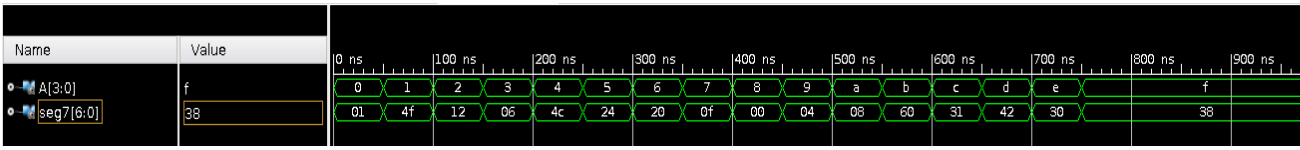
- In the implementation, we accept a 4-bit vector (x) as input from the switches and then set the 7-bit output vector (y) according to the values in the input(x).

- The vector y is used to set the cathodes of the 7-segment display. To display a digit, it is required to give a 1 as input to the anode and a 0 or 1 to each segment depending upon whether that segment needs to be lighted (0) or not (1).

- We have the following output (y) corresponding to the input(x)

Input(x)	Output(y)	Input(x)	Output(y)
0000	0000001	1000	0000000
0001	1001111	1001	0000100
0010	0010010	1010	0000010
0011	0000110	1011	1100000
0100	1001100	1100	0110001
0101	0100100	1101	1000010
0110	0100000	1110	0110000
0111	0001111	1111	0111000

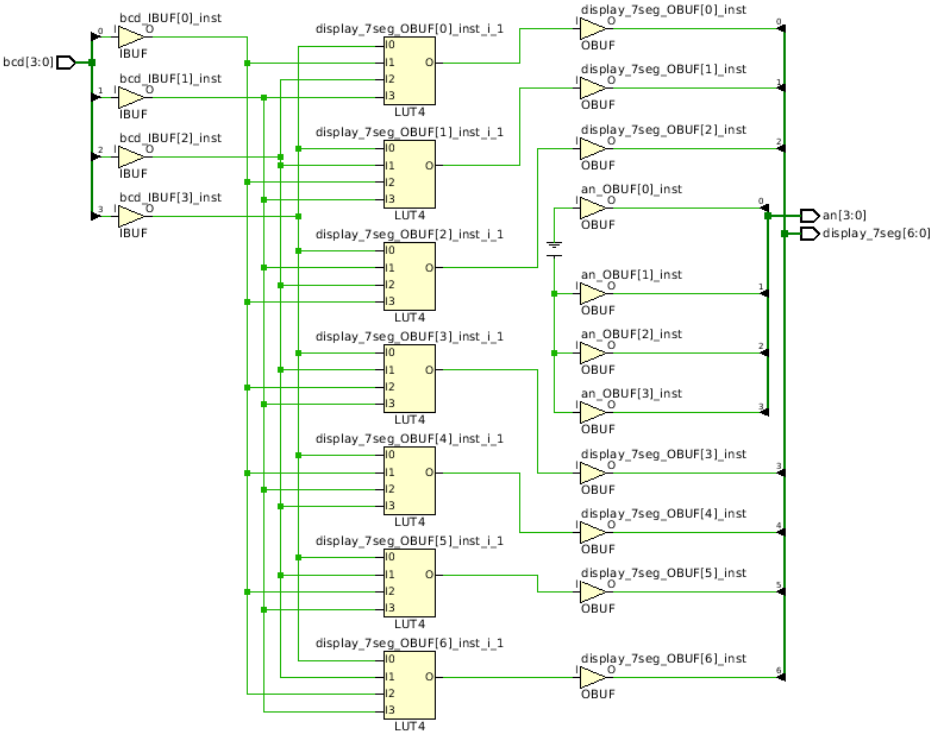
Simulation:



- A is the four-bit input vector containing the binary representation of hexadecimal digits. The first row contains different values of the input signal A.

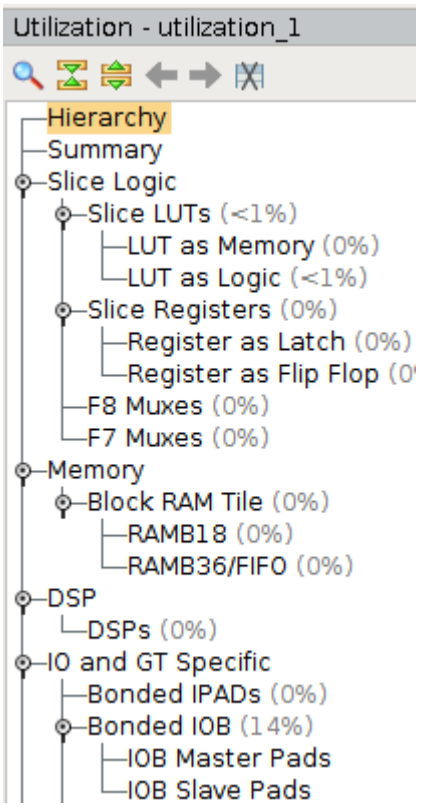
- Seg7 is the output signal. The appropriate value (in hexadecimal notation) of y corresponding to each input signal A is shown in the second row.

Schematic Diagram:



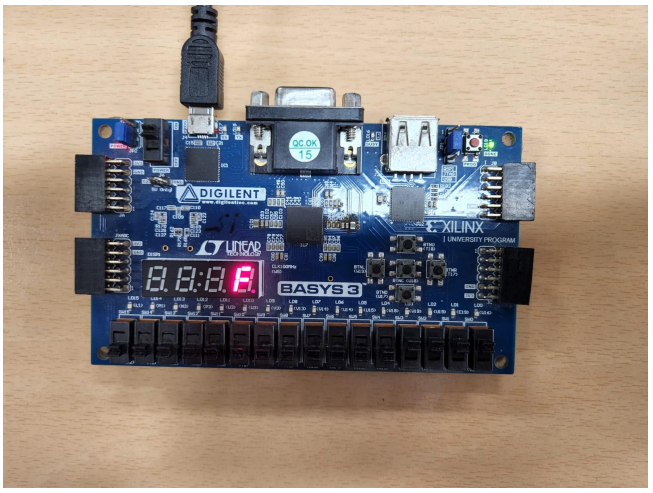
Resource Utilisation:

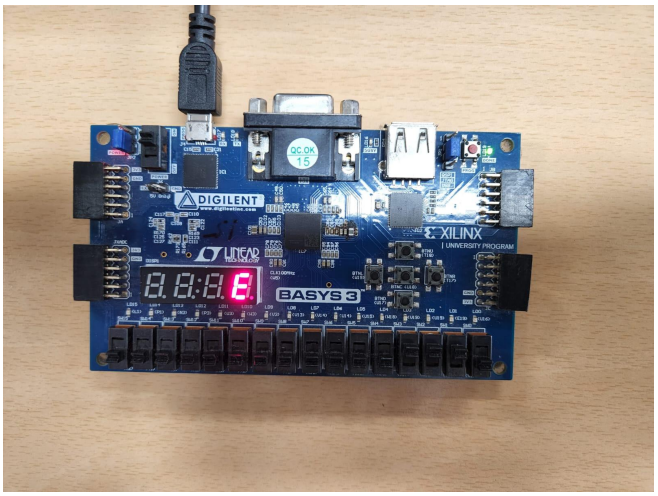
Name	Slice LUTs (20800)	Bonded IOB (106)
bcd_to_7seg_display	4	15

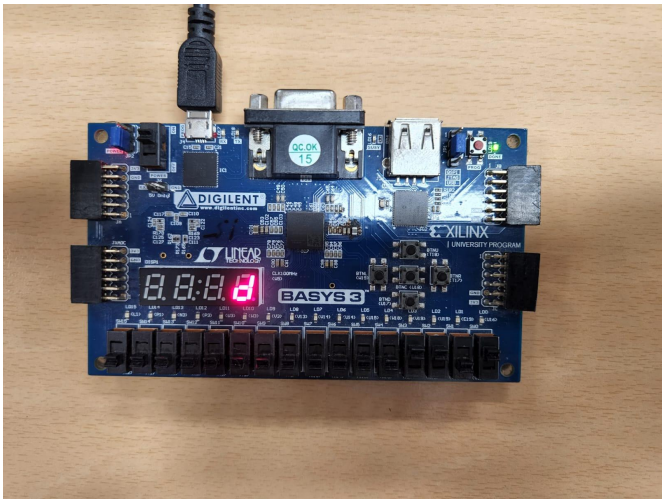


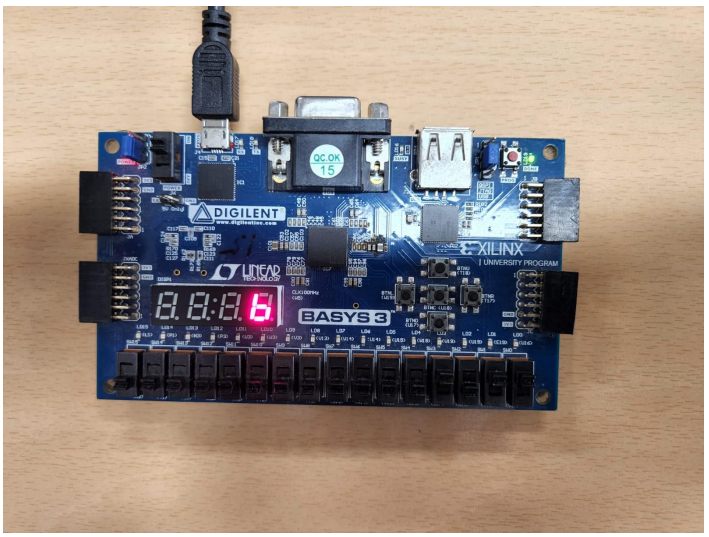
Resource	Utilisation(Count)	Utilisation (%)
LUT -Logic	4	0.02
IO	15	14%
Others	0	0

FPGA Observation:





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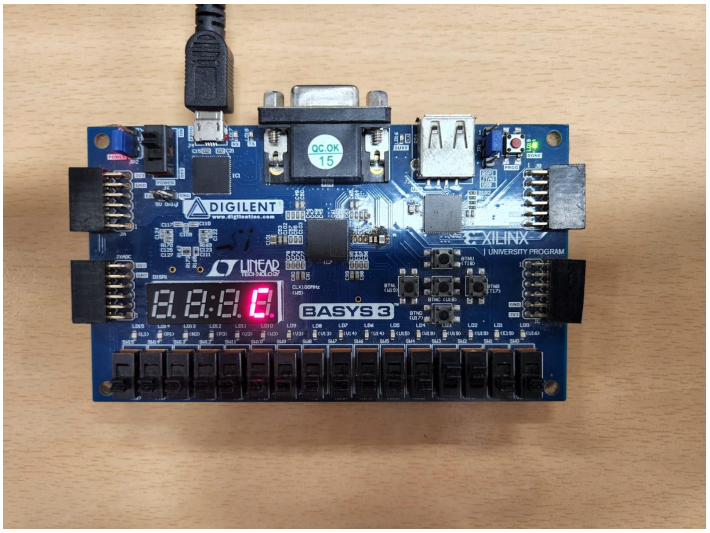
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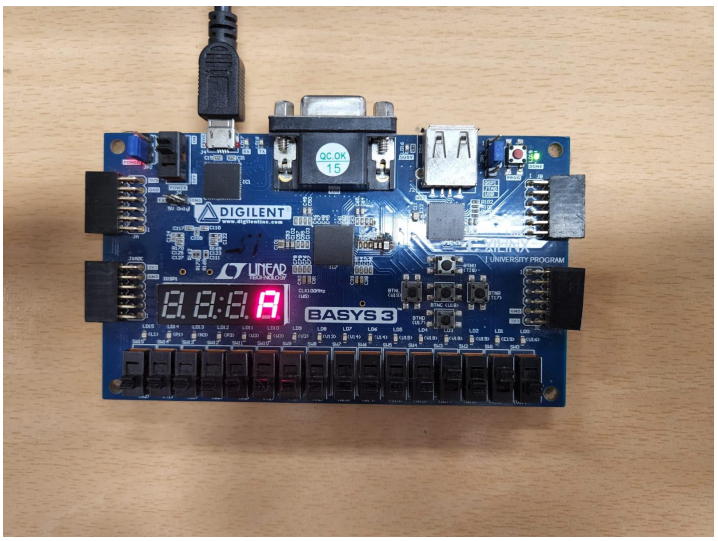
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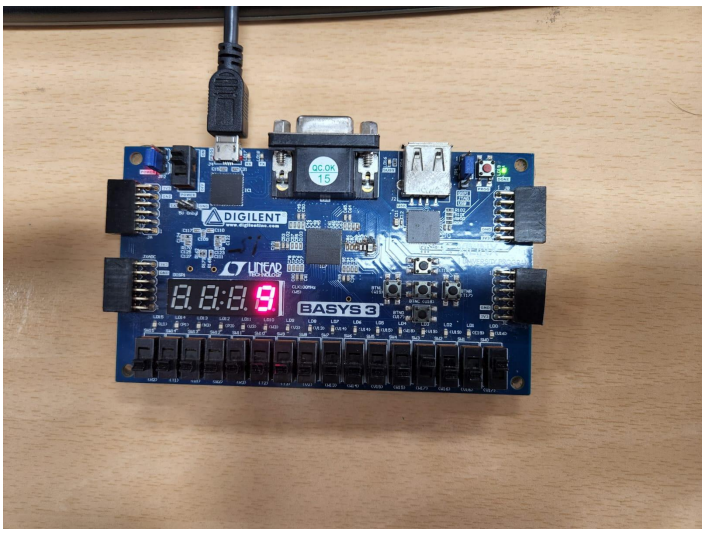
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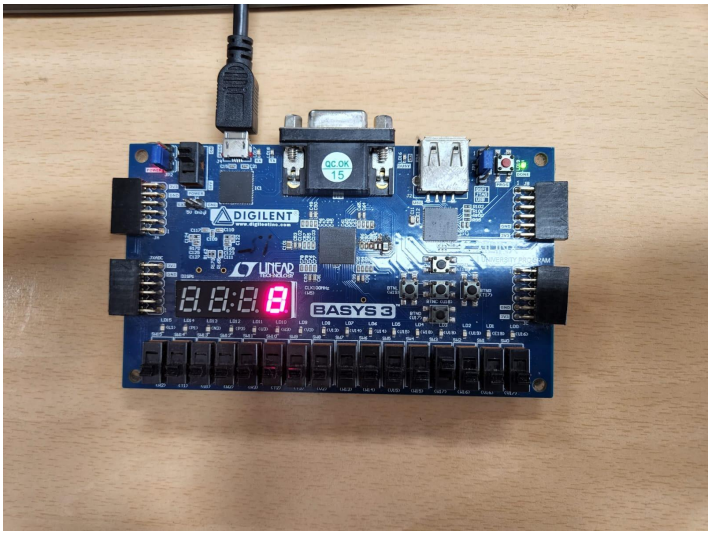
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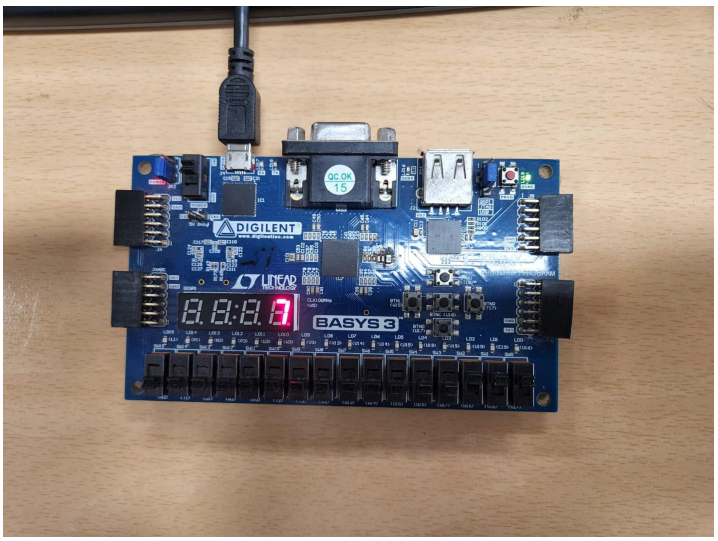
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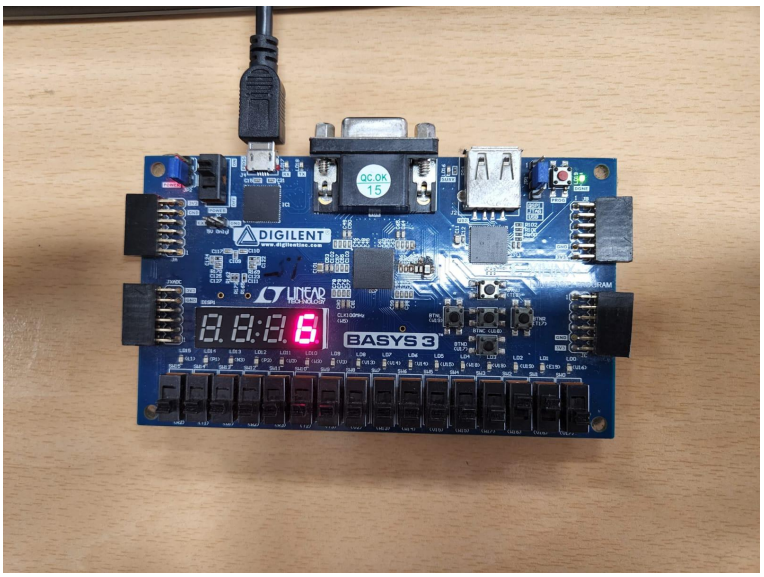
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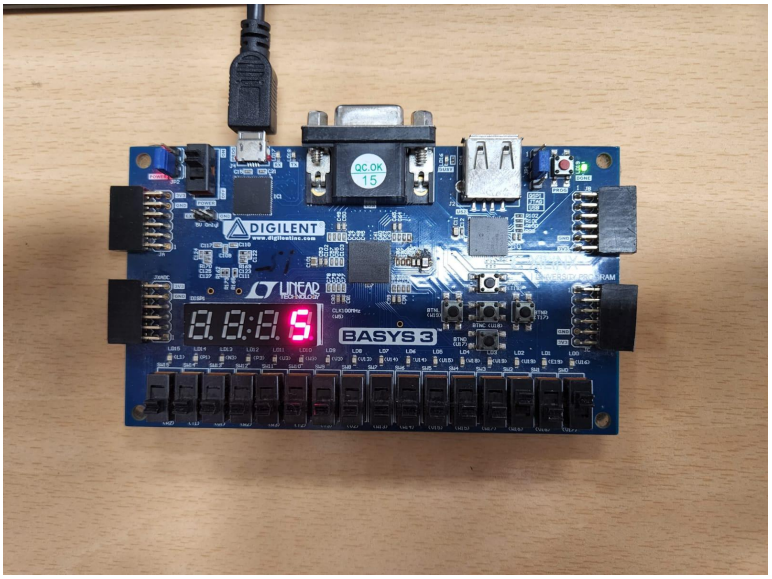
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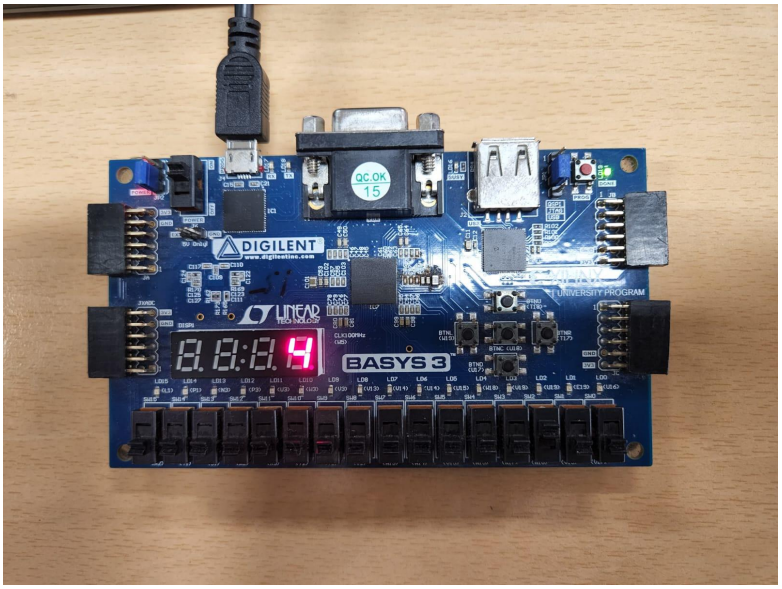
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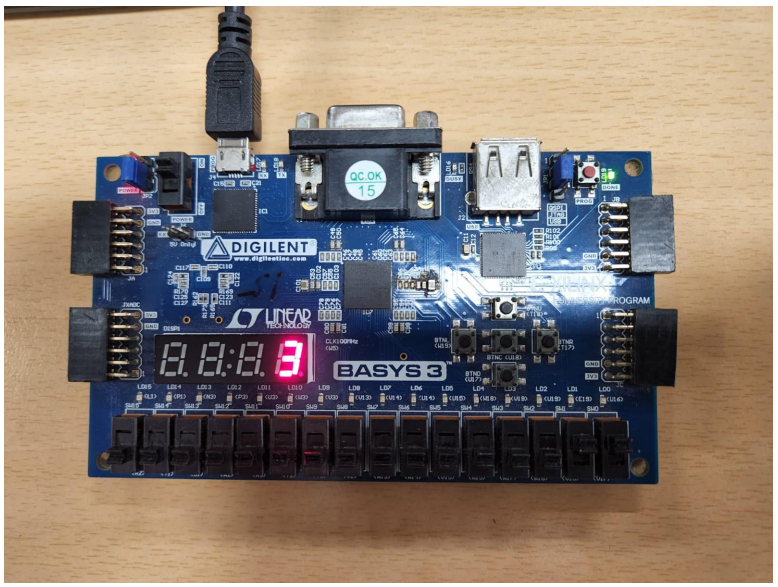
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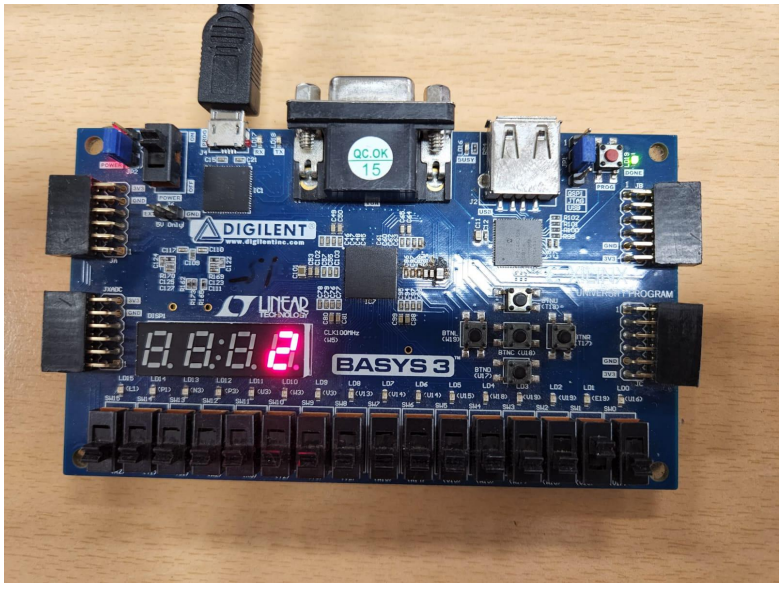
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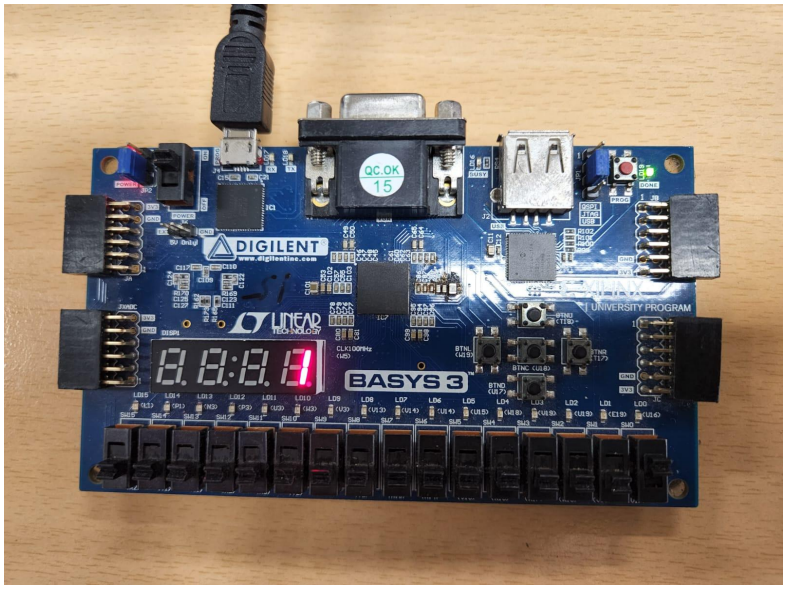
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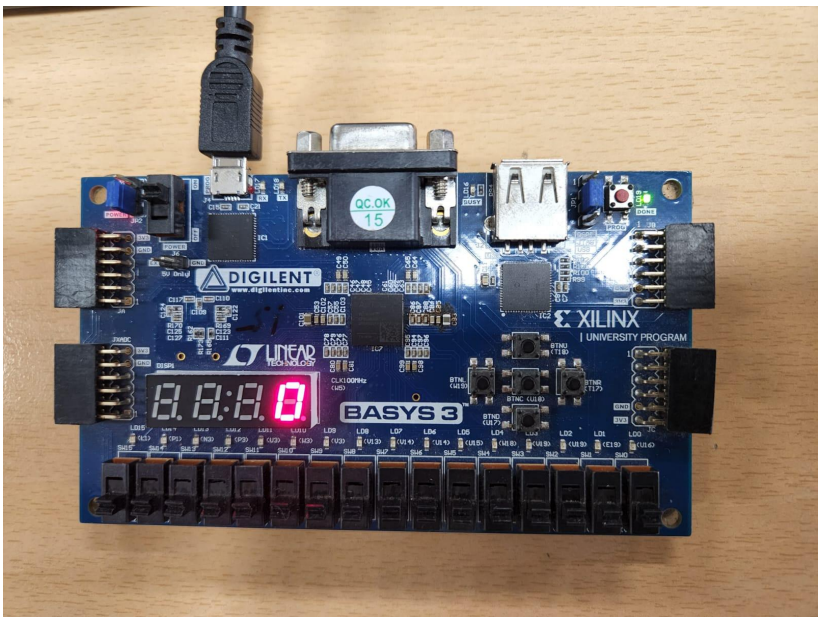
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