COL215P Assignment 1

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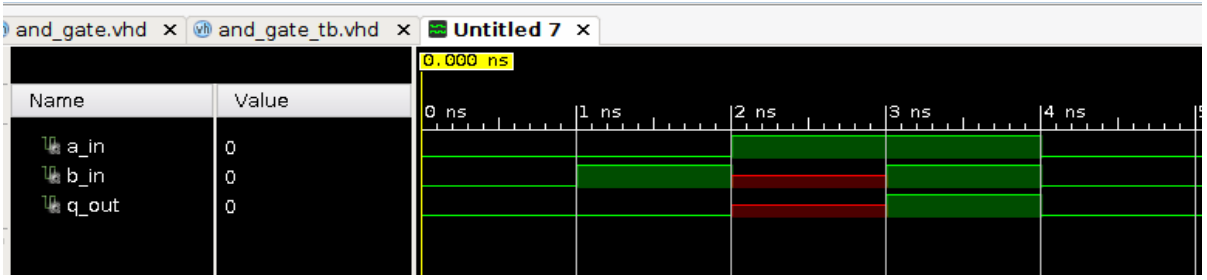
Introduction

- We implemented the logical AND gate IN VHDL and simulated it using a test bench. Then, we synthesised and implemented this on the BASYS3 FPGA board by loading the bit code into it.

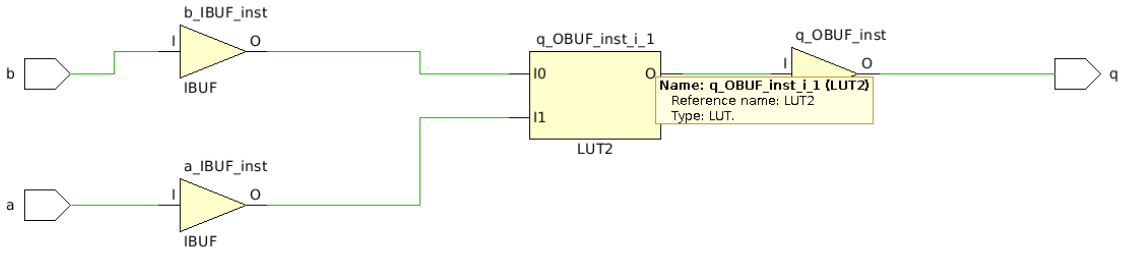
Observations

- Simulation Result:

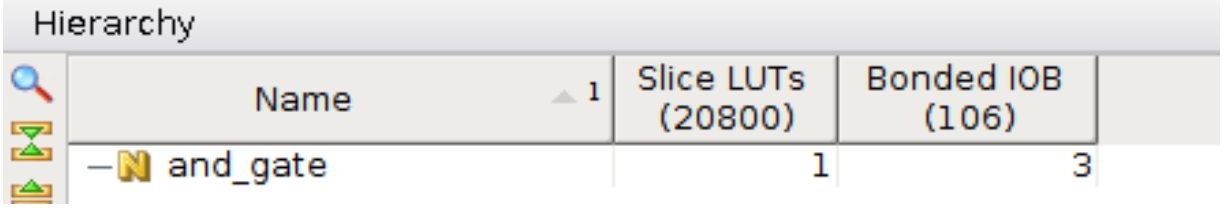


This is an implementation of AND gate. So, if a is 0 and b is 0 then q is 0. If a is 0 and b is 1, then q is 0. If both a and b are 1 then q is 1. If a is 1 and b is X then q is dependent on b and thus, q is X.

- Schematic Diagram obtained after Synthesis:

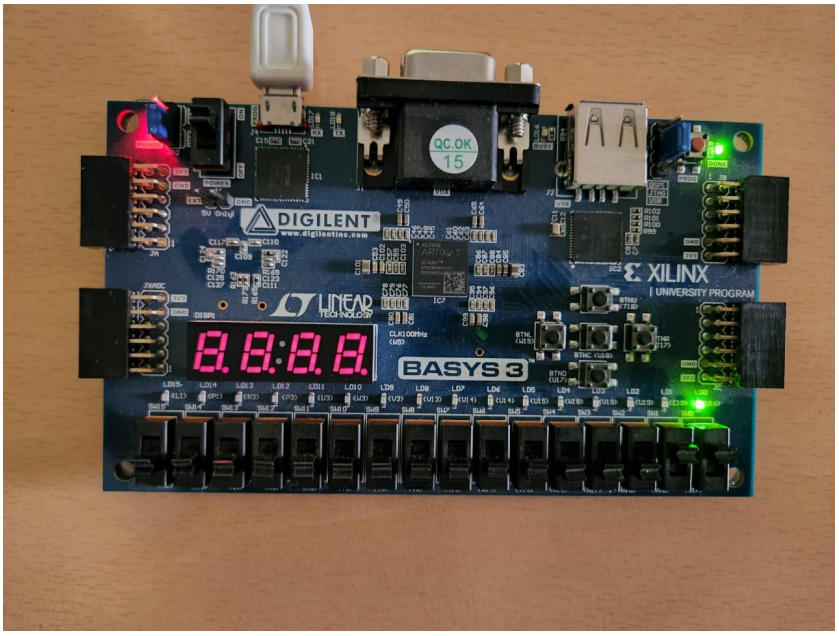


- Resource Utilisation:

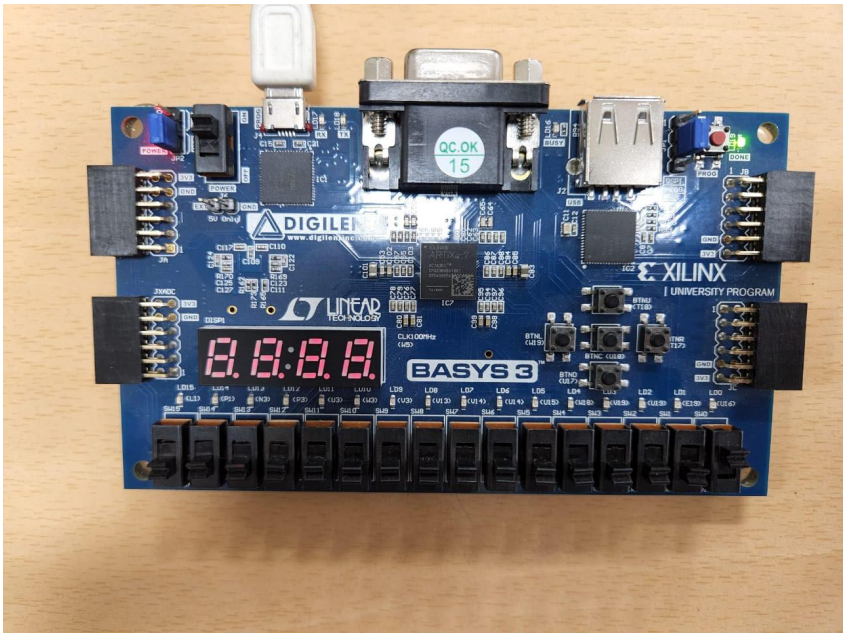


Number of LUTs used = 1
Number of BRAM used = 0
Number of Flip-Flop used = 0
Number of IOB used = 3

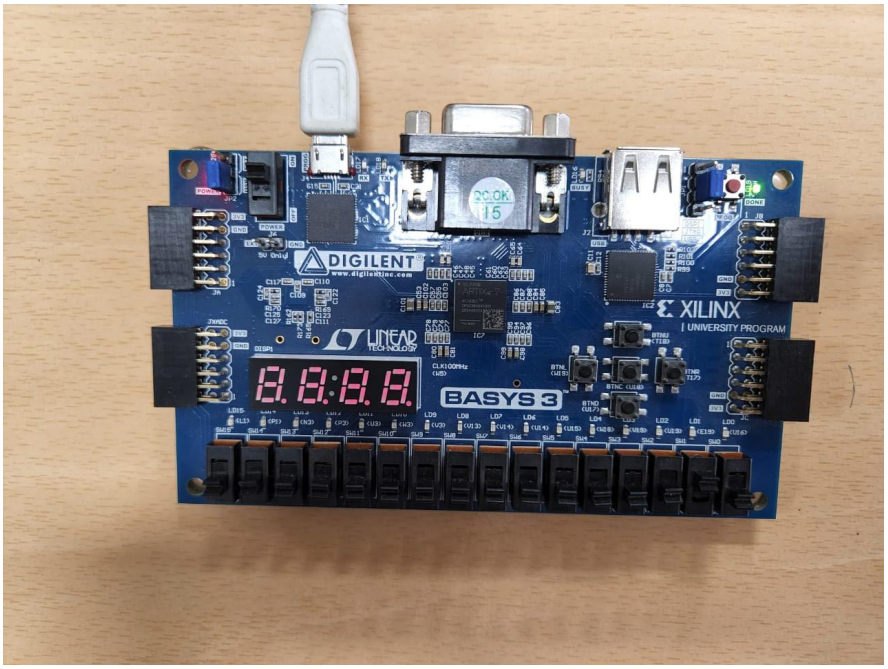
- Implementation on FPGA board:



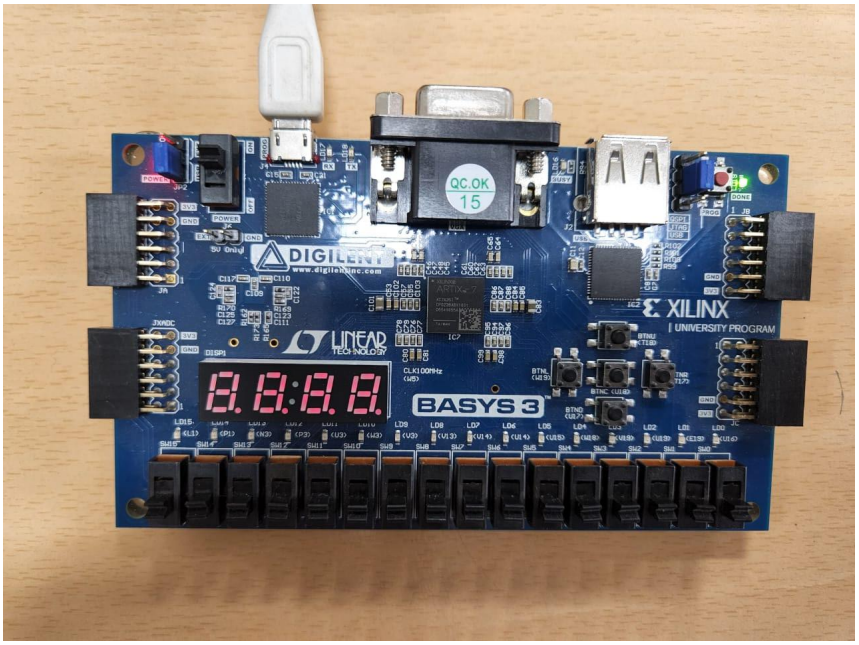
SW0(a) is on and SW1(b) is on



SW0(a) is on and SW1(b) is off



SW0(a) is off and SW1(b) is on



SW0(a) is off and SW1(b) is off