PROJECT REPORT

ON THE TOPIC

DESIGN OF RAISED SOURCE DRAIN MOSFET

Prepared in partial fulfillment of the course

DESIGN ORIENTED PROJECT (INSTR F376)

UNDER THE GUIDANCE OF PROF. MANISH GUPTA

BY

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TABLE OF CONTENTS

INTRODUCTION

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a crucial component in the realm of electronic devices and digital circuits. Comprising a gate, source, and drain, its pivotal function involves regulating the current flowing through the channel between the source and drain via the gate voltage (Vgs). According to Gordan Moore's Law, the transistor count on a microchip doubles every 24 months. Consequently, to sustain a constant chip size, the size of individual transistors must decrease, resulting in an ongoing reduction in transistor dimensions. The downsizing of MOSFETs has given rise to the prevalence of Short Channel Effects (SCEs), posing significant challenges in their design and optimization.

Short Channel Effects arise when the channel length of a MOSFET is diminished. Among these, Drain-Induced Barrier Lowering (DIBL) is the most significant. These effects lead to a decline in the threshold voltage. Another notable SCE is Subthreshold Slope Degradation, wherein the subthreshold slope degrades at shorter channel lengths.

To counter these issues, researchers have studied and analyzed various methods and designs. In this project, the Double Gate Design and the design of the Raised Soiurce Drain MOSFET have been studied and analyzed in detail with the help of simulation results using the software tool TCAD. The Raised Source Drain MOSFET has been carefully designed and discussed in detail to understand its behavior.

The Raised Source Drain MOSFET is an effective approach to mitigate the short-channel effects while improving the drain current. The concept of Negative Capacitance and its use in the RSD design is also discussed. The Raised Source Drain MOSFET, when coupled with the Negative Capacitance, can give rise to a transistor with reduced power consumption, better Drain Current, Faster Switching Speeds, and Improved energy efficiency. These improved devices and their potential wide-scale applications can help transform not just the electronics industry but also the global energy landscape.

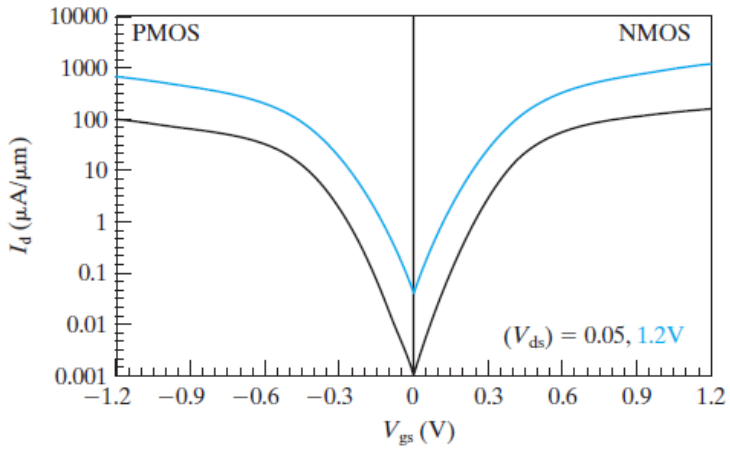
MOSFET SCALING

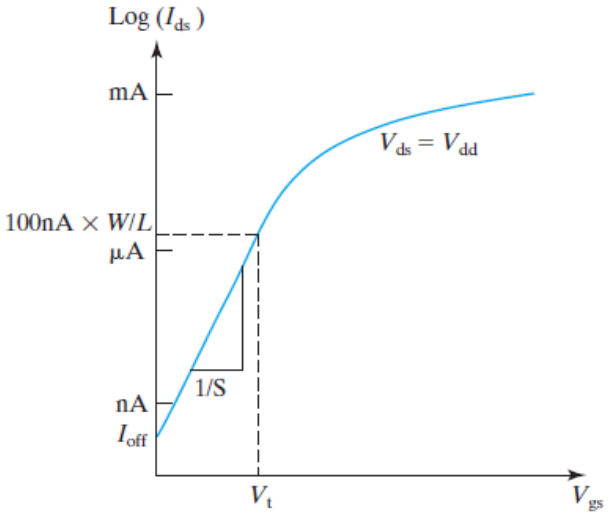
Scaling of MOSFET refers to reducing the physical size while maintaining or improving device performance. Scaling allows for more transistors to be packed on a certain chip. Gordon Moore made an empirical observation in 1965 that the number of devices on a chip doubles every 18 to 24 months or so. This **Moore's Law** is a succinct description of the rapid and persistent trend of miniaturization. The primary goal of scaling is to improve device performance, increase packing density, and reduce power consumption. As MOSFET dimensions scale down, several challenges arise.

SUBTHRESHOLD CURRENT AND LEAKAGES

Circuit speed improves with increasing Ion. Therefore, it would be desirable to use a small Vth (Threshold voltage). At Vgs < Vth, an N-channel MOSFET is in the off-state. However, a leakage current can still flow between the drain and the source. The MOSFET current observed at Vgs < Vth is called the **Subthreshold Current**. This is the main contributor to the MOSFET off-state current, Ioff.

Ioff is the Id measured at Vgs = 0 and Vds = Vdd. It is important to keep Ioff very small in order to minimize the static power that a circuit consumes when it is in standby mode. The given subthreshold current plot, consisting of a semi-log Ids vs. Vgs graph, shows that when Vgs is below Vt, Ids is clearly a straight line, i.e., an exponential function of Vgs.





A practical and common definition of Vt is the Vgs at which Ids= 100 nA× W/L.

$$I_{ds}(nA) = 100 \cdot \frac{W}{L} \cdot e^{q(V_{gs}-V_t)/\eta kT}$$

Subthreshold Swing (S) is equivalent to the change of Vgs with respect to changes in the Subthreshold Current. It is equal to the inverse of the slope in the subthreshold region.

$$S = \frac{dVg}{d(log\ Id)} \qquad S(mV/decade) = \eta.60mV.\frac{T}{300K}$$

Low Subthreshold Swing accounts for a more efficient transistor because a small change in the Gate Voltage (Vg) results in better control of the subthreshold current.
The Subthreshold Swing is improved by reducing Gate-Oxide thickness. If the gate is closer to the channel, it improves gate control. The subthreshold swing is high for heavy doping.
A desirable way to minimize the Off-current, for given W & L, is by reducing the Subthreshold Swing. This can be done by reducing ŋ, by increasing the Cox(by reducing the Tox), and by decreasing the Cdep (Wdep increases).
In addition to subthreshold leakage, another substantial source of leakage current arises from tunneling through extremely thin gate oxide layers. The third significant contributor to leakage is the current flowing through the junction between the drain and the transistor body.

SHORT CHANNEL EFFECTS

Gate length is the physical length of the gate and can be accurately measured. As MOSFET dimensions scale down, several problems arise. The main challenge in scaling is the occurrence of Short Channel Effects at smaller channel lengths.

The channel is controlled by the gate voltage (Vg), and when the gate length is of comparable size w.r.t drain and source, the source-channel barrier is also controlled by Vgs. At a particular gate voltage, there is an injection of electronics into the channel, and a barrier is reduced sufficiently.

In short channel effects, the drain is very near to the source and can impact it, As a result, the drain voltage can also cause the lowering of the barrier at the source end of the channel, causing the current to flow at the lower gate voltage (Vg). The increase in the area of the depletion region at the source and drain leads to a reduction of threshold voltage (Vth).

The concept that the drain can lower the source-channel barrier and reduce the threshold voltage (Vth) is called **Drain Induced Barrier Lowering (DIBL)**. DIBL effect occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of the drain electric field upon the application of a high drain voltage, which now increases the number of carriers injected into the channel from the source, leading to an increased drain off-current [1].

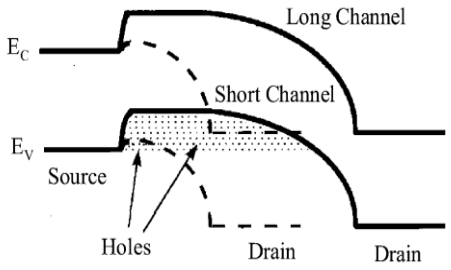
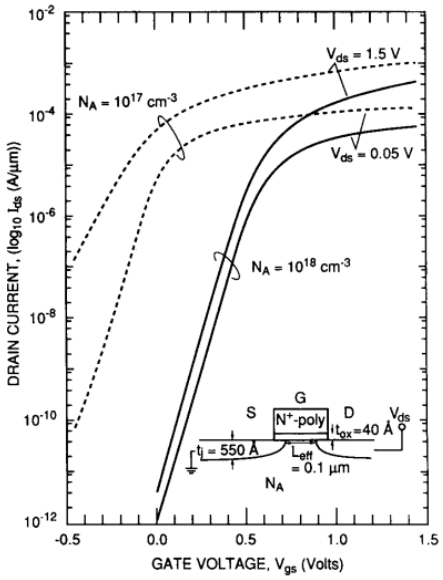


Fig. 3. Comparison of schematic energy band diagrams near the bottom of the body between the long and short-channel FD nMOSFETs [31].

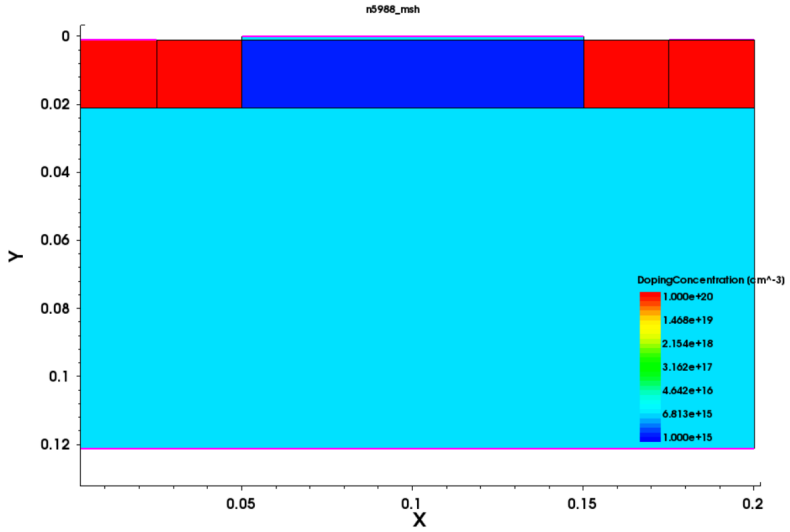
DIBL leads to an increase in Subthreshold Slope due to an increase in current at a lower value of Gate Voltage (Vg). Short channel effects can cause the MOSFET to enter the saturation region at lower Vds.



If the threshold voltage (Vth) goes too low, the Off-Current (Ioff) will increase sharply. The increased drain-off current is undesirable and harmful to the device. Thus, the Short Channel Effects arising from scaling down of MOSFET pose problems to device fabrication.

SINGLE GATE SOI MOSFET

In the Initial Structure, we study and analyze the Single Gate MOSFET structure given below.



Single Gate SOI MOSFET Structure

- **Varying Tsi and Id for given Tox and other values**

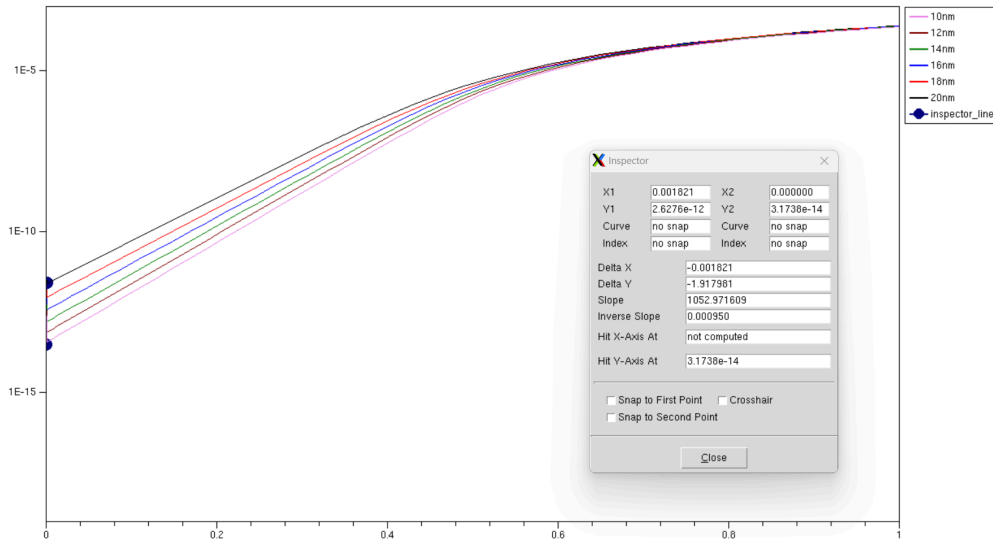
  As the Silicon Thickness (Tsi) varies, it has a proportional impact on the Vth. A Decrease in Tsi results in a decrease in the threshold voltage (Vth) and vice versa. This is because, with decreasing Tsi, the electric field has better control of the channel region, resulting in a decrease in the threshold voltage.

  Thus, a thinner Tsi leads to steeper Subthreshold Swing & better switching performance.

  With decreasing Tsi, however, the Short Channel Effects also increase, consequently leading to higher Off Current (Ioff) and leakage currents.

			SDE						SDEVICE			INSPECT	SDEVICE	SDEVICE				
	Tsi	Tox	Tbox	N	Lg		temp	Vd	Vg	WF					IdSat	Ioff	VtiSat	SSsat
1	[n5984]: 20	[n5985]: 1	[n5986]: 100	[n5987]: 1e15	[n5988]: 100	[n5989]: --	[n5990]: 300	[n5991]: 1.0	[n5992]: 1.0	[n5993]: 4.7	[n5994]: --	[n5995]: --	[n5996]: --		2.4505e-04	3.9809e-12	0.4365	80.0531
2	[n6560]: 18	[n6561]: 1	[n6562]: 100	[n6563]: 1e15	[n6564]: 100	[n6565]: --	[n6566]: 300	[n6567]: 1.0	[n6568]: 1.0	[n6569]: 4.7	[n6570]: --	[n6571]: --	[n6572]: --		2.4128e-04	2.4992e-12	0.4487	76.5930
3	[n6573]: 16	[n6574]: 1	[n6575]: 100	[n6576]: 1e15	[n6577]: 100	[n6578]: --	[n6579]: 300	[n6580]: 1.0	[n6581]: 1.0	[n6582]: 4.7	[n6583]: --	[n6584]: --	[n6585]: --		2.3730e-04	1.9202e-12	0.4601	73.6781
4	[n6586]: 14	[n6587]: 1	[n6588]: 100	[n6589]: 1e15	[n6590]: 100	[n6591]: --	[n6592]: 300	[n6593]: 1.0	[n6594]: 1.0	[n6595]: 4.7	[n6596]: --	[n6597]: --	[n6598]: --		2.3306e-04	1.6569e-12	0.4703	71.2094
5	[n6599]: 12	[n6600]: 1	[n6601]: 100	[n6602]: 1e15	[n6603]: 100	[n6604]: --	[n6605]: 300	[n6606]: 1.0	[n6607]: 1.0	[n6608]: 4.7	[n6609]: --	[n6610]: --	[n6611]: --		2.2847e-04	1.5046e-12	0.4802	69.1521
6	[n6612]: 10	[n6613]: 1	[n6614]: 100	[n6615]: 1e15	[n6616]: 100	[n6617]: --	[n6618]: 300	[n6619]: 1.0	[n6620]: 1.0	[n6621]: 4.7	[n6622]: --	[n6623]: --	[n6624]: --		2.2345e-04	1.3880e-12	0.4897	67.5304

Values obtained by carrying out Simulations using TCAD

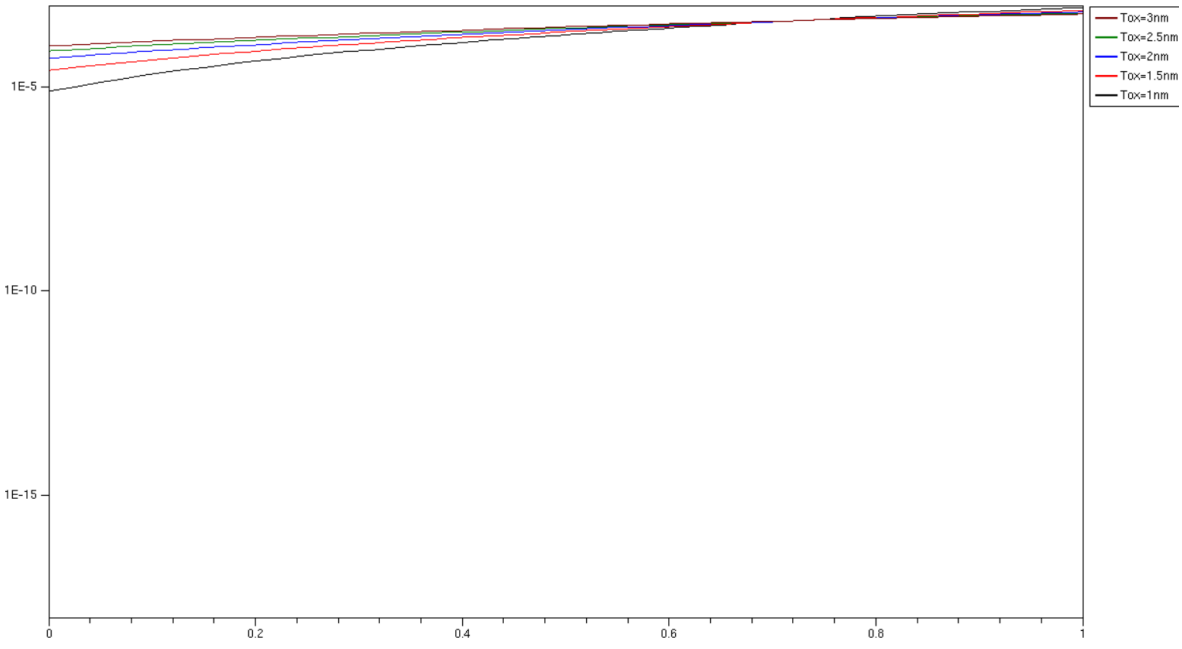


Varying Tsi and Id for Vgs=1V and Vds=1V

- **Varying Tox & Id for given Tsi and Other Parameters**

  On the other hand, Reducing the Oxide Thickness leads to an increase in the Gate Capacitance and thus a decrease in the Vth, threshold voltage.

  The Smaller the Tox, the steeper the Subthreshold Swing and Better Control of the MOSFET.

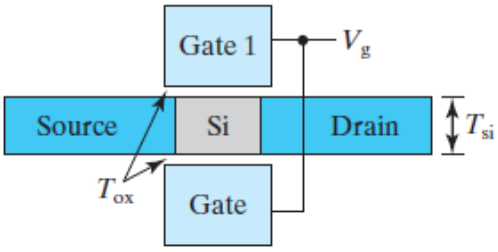


Varying Tox and Id for Vgs=1V and Vds=1V

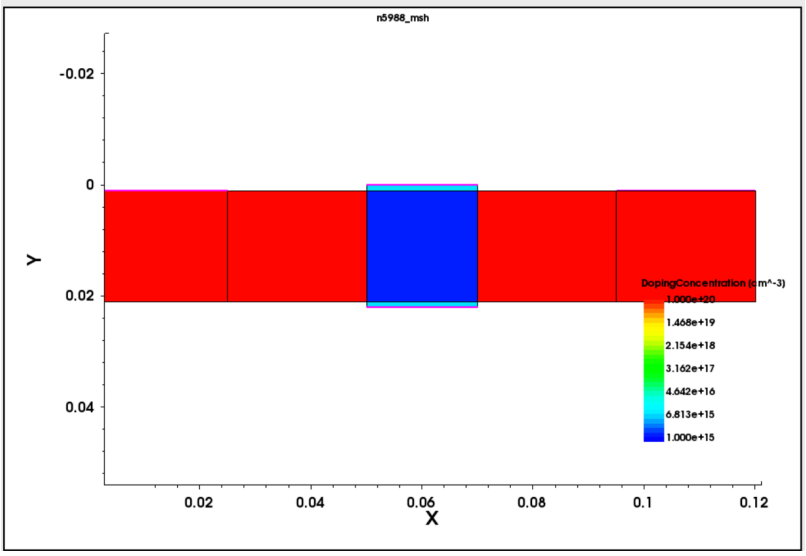
DOUBLE GATE SOI MOSFET

The Single Gate SOI MOSFET leads to multiple leakage currents and increased Short Channel Effects on scaling down.

To counter this we study and analyse Double Gate SOI MOSFET. Multiple Gates can eliminate deep channel submerged leakage paths. No current leakage path in the Si film is far from one of the gates [6]. Thus, the Double Gates can suppress the leakage current more effectively than the traditional MOSFET and give better Gate Control.



A schematic sketch of a double-gate MOSFET with gates connected

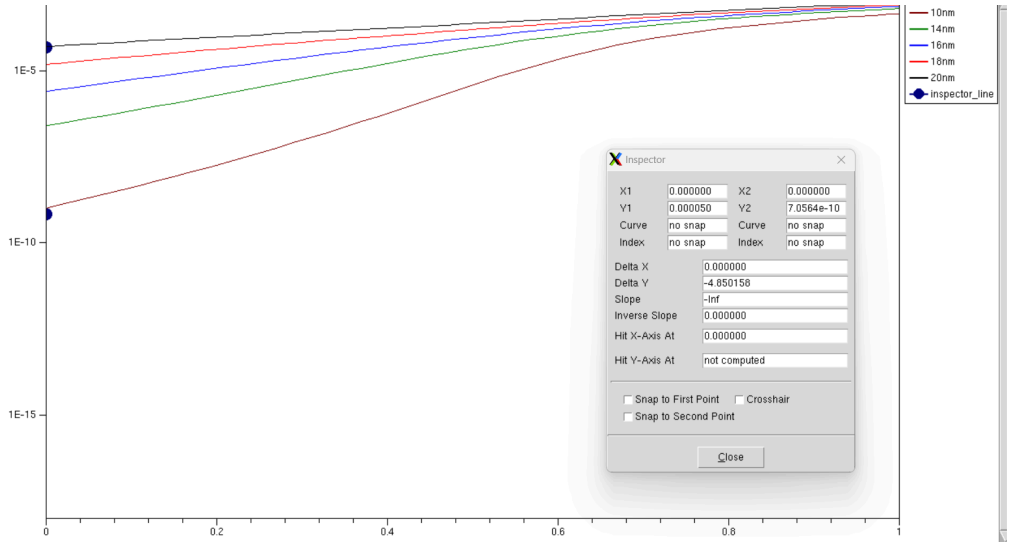


Double Gate SOI MOSFET Structure

- **Varying the Silicon Thickness (Tsi)**

  When the Tsi increases, it results in an increase in the Vth. There are 4 depletion regions formed - one at each gate, one at the source, and one at the drain terminal. Thus, an increase in the Tsi, leads to an increase in the DIBL. Thicker silicon leads to a larger depletion region between the drain and the channel.

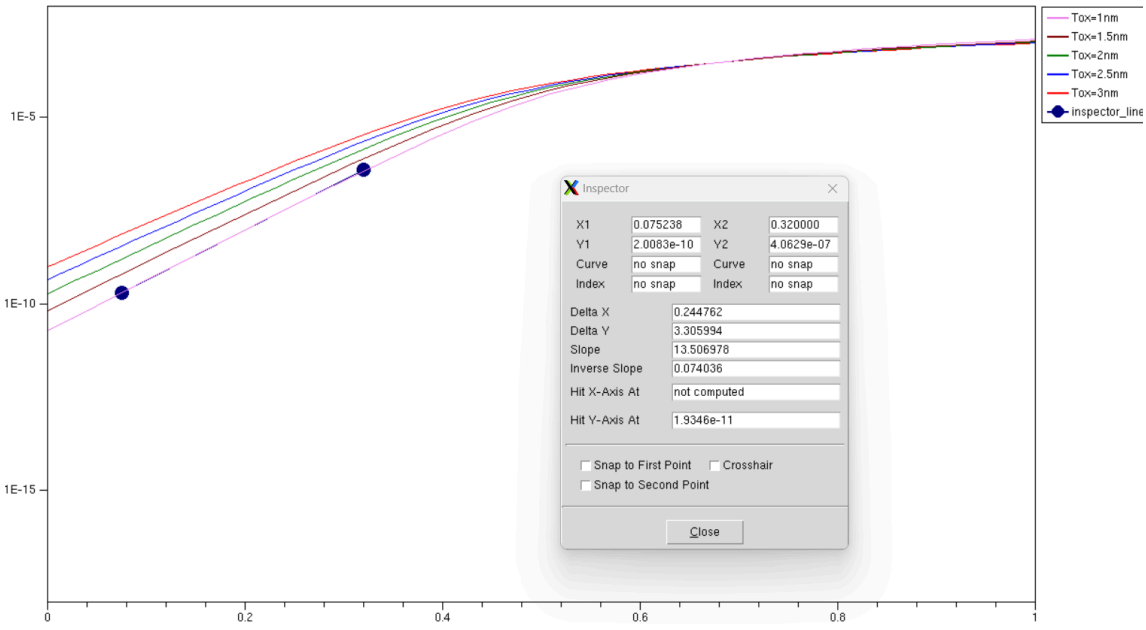
In the thinner Si, Vd (Drain Voltage) can easily influence the potential in the channel region, causing a lowering of energy between the source and the drain.



Varying Tsi and Id for Vgs=1V and Vds=1V

- **Varying the Oxide Thickness (Tox), keeping Tsi & other parameters constant**

  Increasing Tox, leads to a lower threshold voltage (Vth) and thus better gate control. For increasing Tox, there is decreasing Cox, which leads to lesser charge being required for changing the Gate Voltage (Vg). Thus, the Vth decreases.



Varying Tox and Id for Vgs=1V and Vds=1V

RAISED SOURCE DRAIN MOSFET

MOSFET Scaling leads to Short Channel Effects. As the gate length decreases, we see an increase in the DIBL and the Direct Source-to-Drain Tunneling (DSDT), thus leading to higher Off-Current (Ioff). DSDT refers to the tunneling of charge carriers from the source to the drain, bypassing the channel region under the influence of the gate voltage (Vg), leading to leakage currents and thereby reducing the overall performance of the device [8].

As the size of the source/drain decreases, parasitic resistance becomes a larger fraction of the total ON-state resistance, so the effective voltage is reduced.

Several studies show that the RSD design achieves much better drive current because the Dopant-Segregated Schottky Double Gate MOSFET has a longer effective channel length due to longer underlap between the gate and source/drain regions.

In addition, the RSD design provides superior performance at sub-30-nm device lengths because its current is not limited by a tunneling barrier at the source, as is the DSS Double Gate design [8].

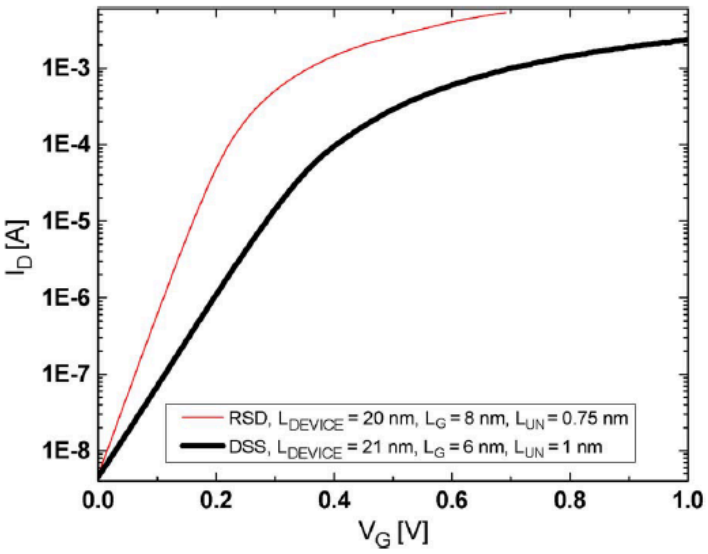
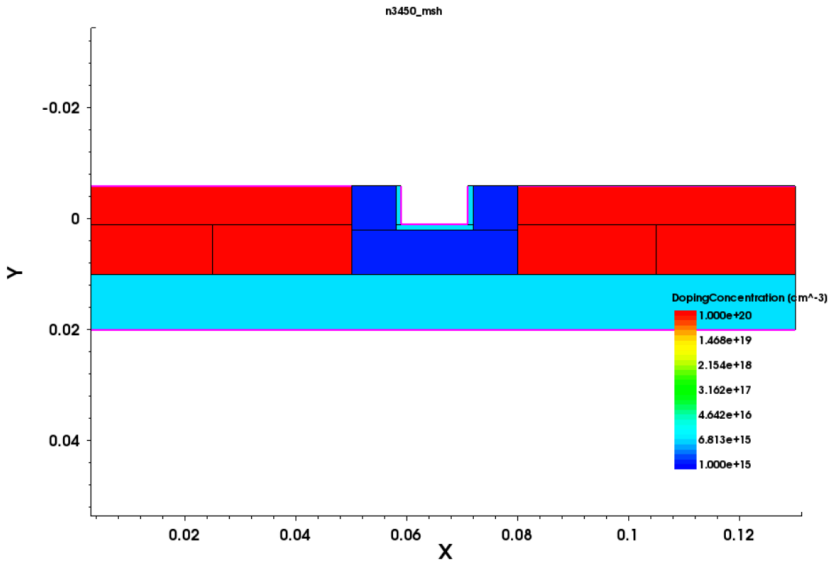


Fig. 10. Comparison of simulated transfer characteristics for optimized RSD and DSS double-gate MOSFET designs, for ~20-nm device length.

RAISED SOURCE DRAIN MOSFET STRUCTURE



Introduction of Underlap: The underlap refers to an extension of the Gate Structure beyond the source and the drain regions of the transistor. This extended region is not covered by the gate electrode, thus helping mitigate the Short Channel Effects by providing better Gate Control.

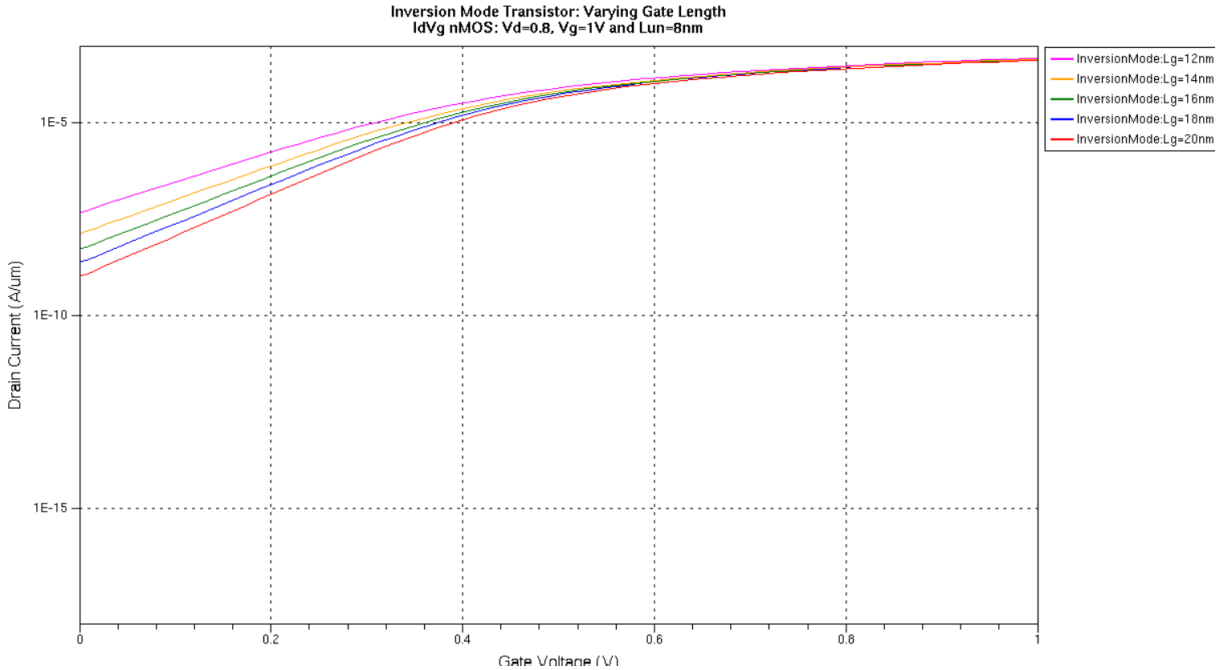
The above structure is used to incorporate an Underlap Length of 8nm.

Observations

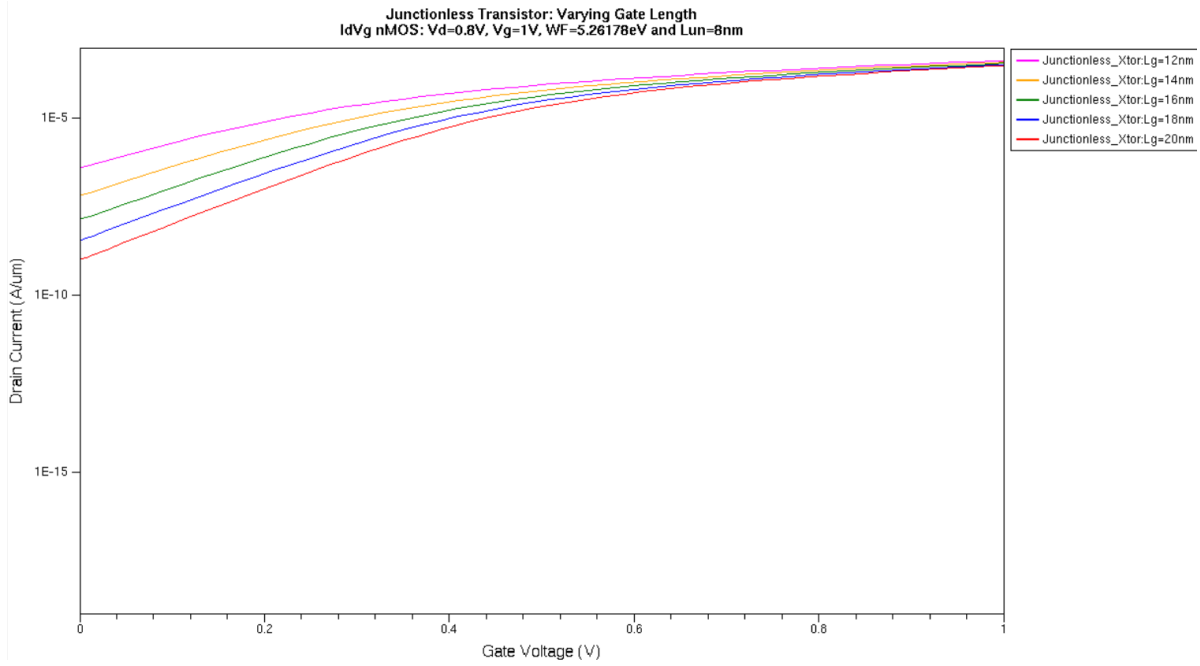
It was observed in simulations that when the Gate Length is increased, keeping the Lun (Underlap Length) constant, there is a decrease in the Drain Current (Id). An increasing Lg also increases the channel resistance, reducing drain current, Id. A shallower subthreshold slope makes the transistors less efficient at low current levels.

The following curves show the impact of Varying Gate Length (Lg) on the Id-Vgs curve of the Inversion Mode and Junctionless Transistors devices.

<u>Inversion Mode Transistor:</u> N-channel Doping is 10^{15} *& Work Function of 4.417 eV is used to get Ioff=1e-9 A/um*



Junctionless Transistor: N-channel Doping is 10^{19} *& after multiple simulations, it's found that the Work Function of 5.26178 eV gives the required Ioff=1e-9 A/um.*



The Raised Source Drain MOSFET provides for higher Ids (Drain Current), mitigates Short Channel Effects, and improves device performance.

NEGATIVE CAPACITANCE

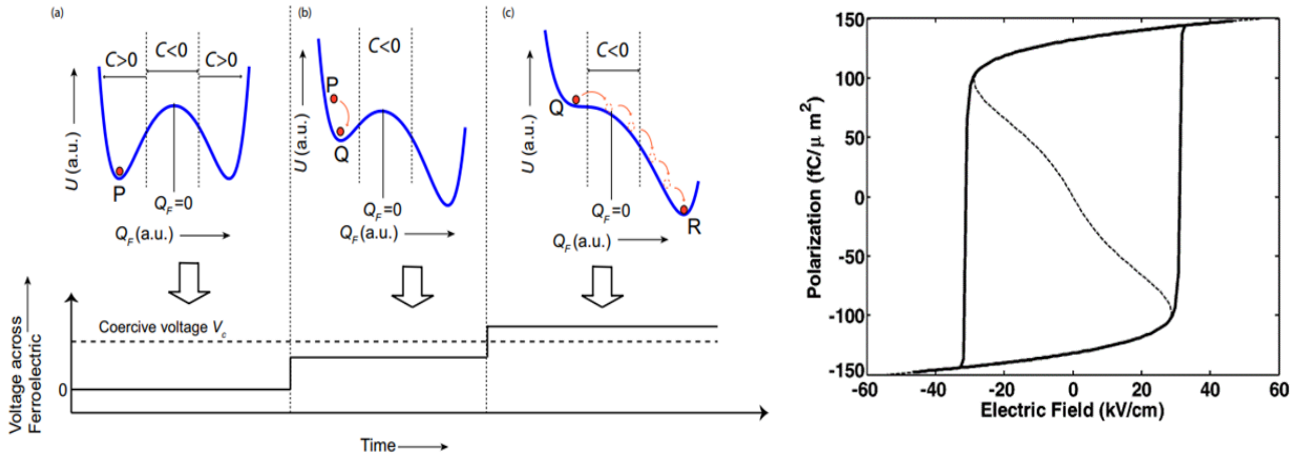
Ferromagnetic materials are dielectric materials that can be polarised when the direction of the electric field is changed. Polarisation can be reversed when the field direction is reversed.

In Negative Capacitance Devices, a ferromagnetic material is sandwiched between conductive electrodes. When the voltage increases, polarisation increases non-linearly and vice versa.

When a positive voltage is applied, polarisation increases and causes a decrease in the charge stored in the capacitor, Resulting in a Negative capacitance.

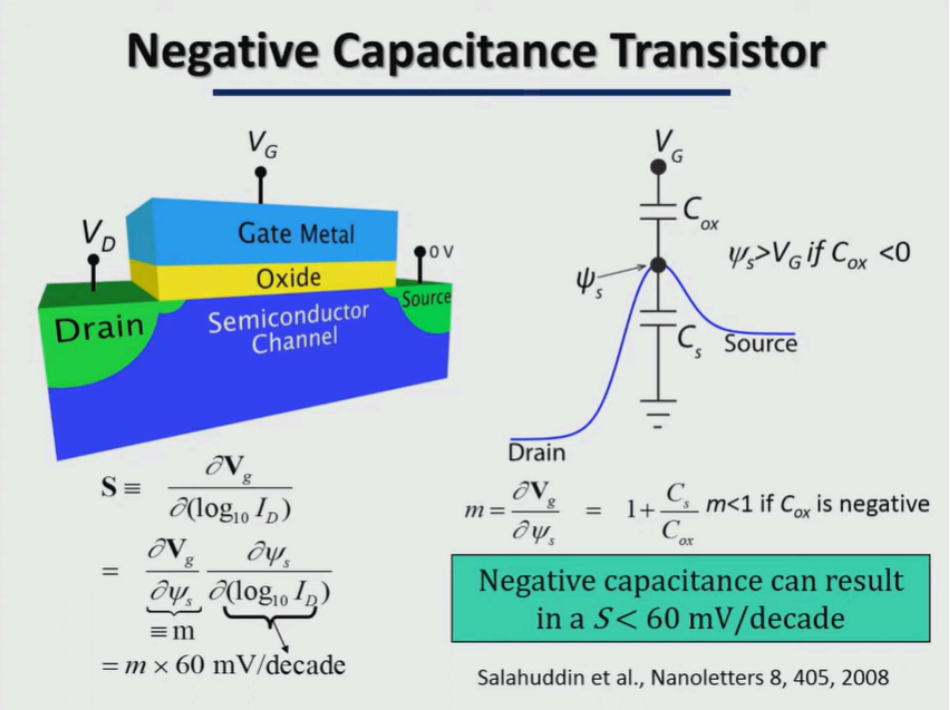
The hysteresis effect in ferroelectric materials enables the storage of energy and the enhancement of device performance.

The negative capacitance effect amplifies the voltage across the MOSFET, enhancing its performance and reducing power consumption.



Energy Landscape description of the ferroelectric negative capacitance

Using Negative Capacitance, low-power consuming transistors can be designed, and energy efficiency can be improved.



One of the primary benefits of negative capacitance MOSFETs is their ability to achieve sub-60 mV/dec subthreshold swing, which is significantly lower than the theoretical limit of 60 mV/dec for traditional MOSFETs. This can lead to lower power consumption and better performance in low-power applications.

Negative capacitance MOSFETs may exhibit improved Ion/Ioff ratios, leading to better overall performance in terms of the ratio between the on-state current (Ion) and the off-state current (Ioff).

Negative capacitance can also reduce the effective threshold voltage of the transistor. This means that the NC-MOSFET can turn on at lower gate voltages compared to traditional MOSFETs. In the Id-Vg graph, this can be observed as a leftward shift of the threshold voltage, indicating improved performance in terms of turn-on characteristics

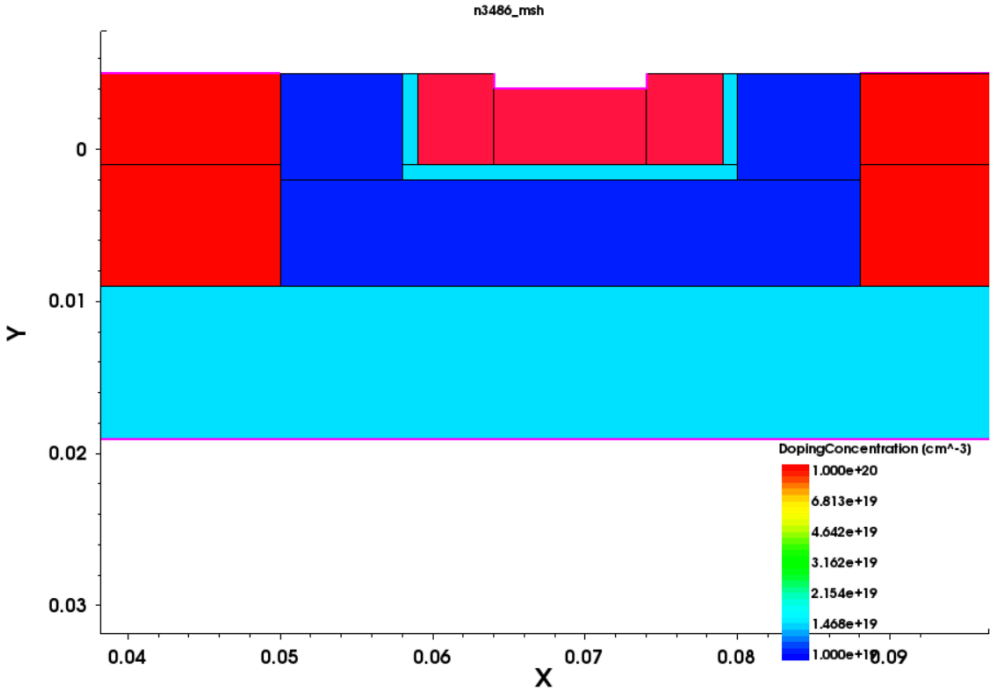
RAISED SOURCE DRAIN MOSFET WITH NEGATIVE CAPACITANCE

The addition of a ferroelectric in the Raised Source Drain MOSFET introduces the concept of Negative Capacitance in the Transistor.

A layer of HfO2, of thickness 5nm, is added on the top of the existing SiO2 layer. HfO2 has a relative dielectric constant (k) of ~24, six times larger than that of SiO2. A 6 nm thick HfO2 film is equivalent to a 1 nm thick SiO2 because both films produce the same Cox. The HfO2 film has an equivalent oxide thickness or EOT of 1 nm. However, the HfO2 film presents a thicker tunneling barrier to the electrons and holes. The consequence is that the leakage current through HfO2 is several orders of magnitude smaller than that through SiO2.

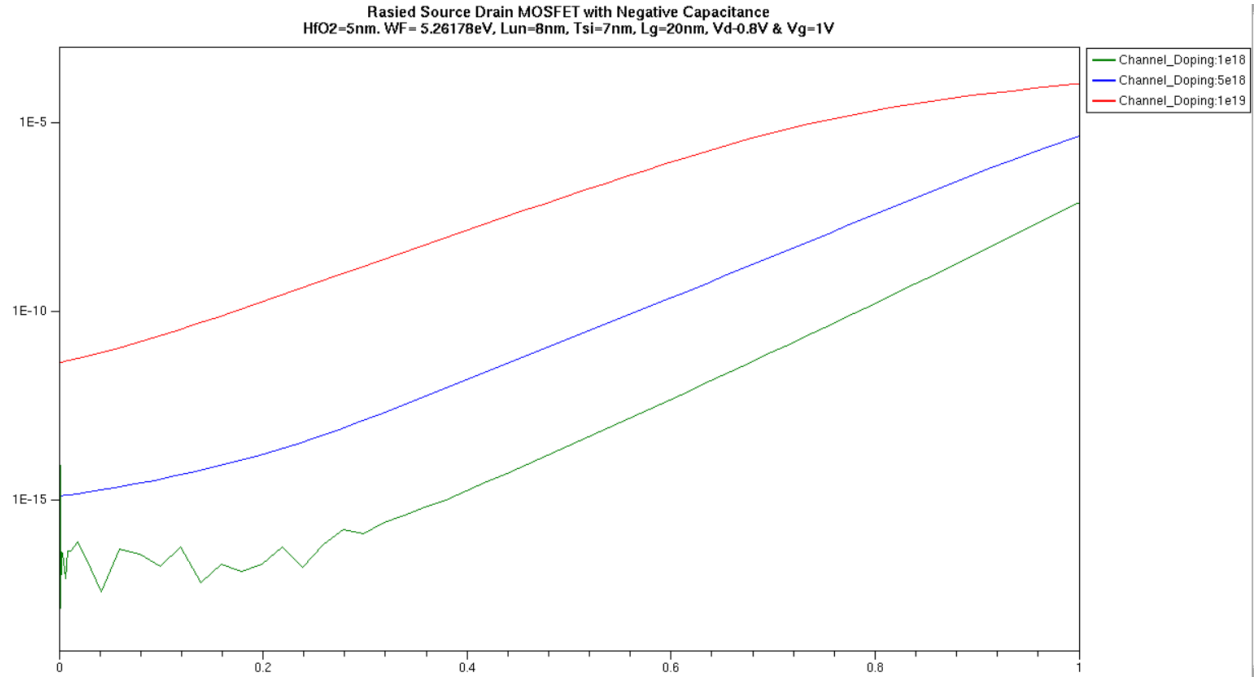
The difficulties of adopting high-k dielectrics in IC manufacturing are chemical reactions between them and the silicon substrate, lower surface mobility than the Si–SiO2 system, and more oxide charge. These problems are minimized by inserting a thin SiO2 interfacial layer between the silicon substrate and the high-k dielectric.

Thus, the new updated structure includes a 5nm HfO2 layer sandwiched between the existing SiO2 layer and the Gate Electrodes at the Front Gate, Left Gate and Right Gate.

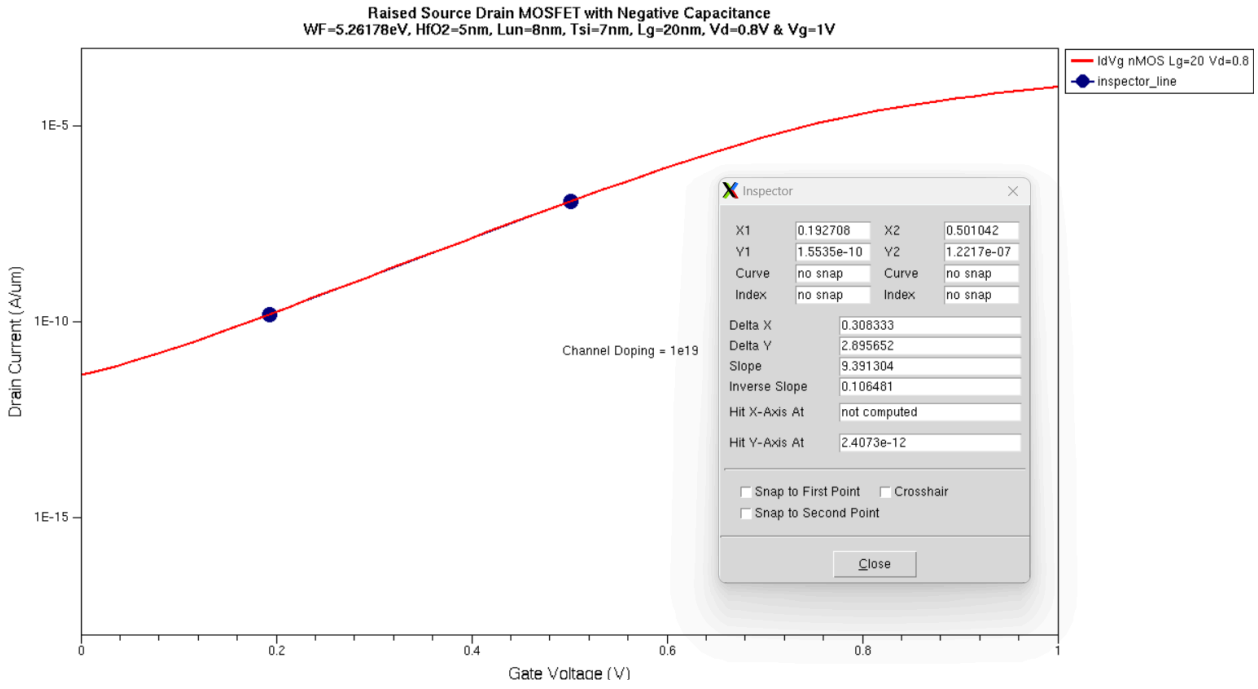


Latest Updated Structure with Negative Capacitance

The Id-Vgs graphs for varying values of channel doping were plotted for observation and analysis purposes, and these are the shapes of the graphs generated.



The Id-Vgs curve of the Raised Source Drain MOSFET for the appropriate N-Channel Doping of 1e19 was also plotted, exhibiting a reduced Ioff and Steeper Subthreshold Swing.



CONCLUSION

MOSFET scaling has played a significant role in developing high-performance electronics. However, as devices are scaled down to ever-smaller sizes, they face numerous challenges, such as short-channel effects. Several methods are discussed to address these issues.

The Single Gate SOI MOSFET showed increased Short Channel Effects that were countered by analysis and adoption of the Double Gate MOSFET Design. The Double Gate MOSFET Design provides much better Gate Control and suppresses all current leakage paths in the Silicon film.
However, this, too, had several negative consequences as multiple gates led to multiple depletion regions and a significant increase in the Drain-Induced Barrier Lowering. Thus, an increase in DIBL saw a decrease in the Vth (Threshold Voltage).

These issues were addressed in the Raised Source Drain MOSFET that incorporated the use of an underlap region, allowing it to counter the Short Channel Effects and the problems arising from it. The Raised Source Drain design achieves much better drive current than the conventional Double Gate MOSFET as it has a longer effective channel length due to longer underlap between the gate and source/drain regions. It also leads to superior device performance as it is not limited by any tunneling barrier as opposed to the previously studied structure.

Incorporating Negative Capacitance in the final structure by introducing a 5nm layer of HfO2 dielectric sandwiched between the existing layer of SiO2 and Gate Electrodes also has several benefits. Negative capacitance MOSFETs exhibit improved Ion/Ioff ratios, leading to better overall performance.

The Raised Source-Drain structure aims to reduce the impact of short-channel effects, which often degrade subthreshold swing in conventional MOSFETs. Negative capacitance has the potential to reduce subthreshold swing further. Combining these features results in a transistor with significantly improved subthreshold swing, enhancing its performance in low-power applications.

Negative capacitance can internally generate a voltage boost, and the Raised Source-Drain structure can help in minimizing the impact of parasitic capacitances. The combination might result in better voltage boosting, leading to faster switching speeds.

Thus, the combination of Raised Source Drain Design and Negative Capacitance effects leads to a transistor with reduced power consumption, better Drain Current, Faster Switching Speeds, and Improved energy efficiency.

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