

NMOS 16K (2K x 8) UV EPROM

- 2048 x 8 ORGANIZATION
- 525mW Max ACTIVE POWER, 132mW Max STANDBY POWER
- ACCESS TIME:
 - M2716-1 is 350ns
 - M2716 is 450ns
- SINGLE 5V SUPPLY VOLTAGE
- STATIC-NO CLOCKS REQUIRED
- INPUTS and OUTPUTS TTL COMPATIBLE DURING BOTH READ and PROGRAM MODES
- THREE-STATE OUTPUT with TIED-OR-CAPABILITY
- EXTENDED TEMPERATURE RANGE
- PROGRAMMING VOLTAGE: 25V

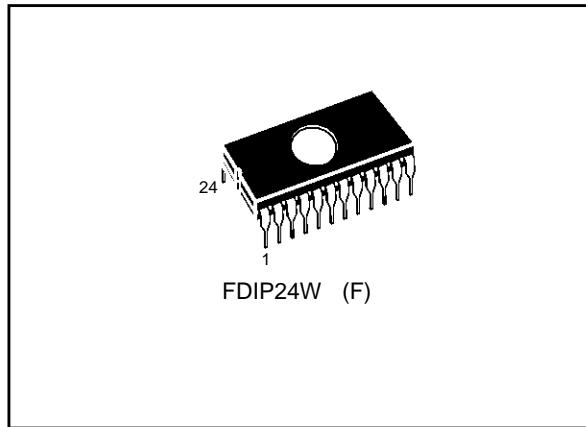
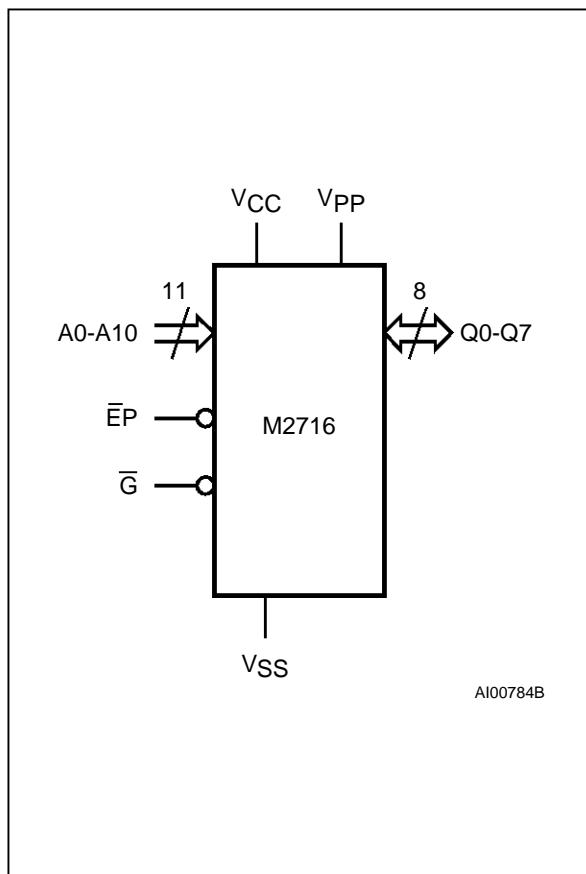
DESCRIPTION

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM, ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M2716 is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

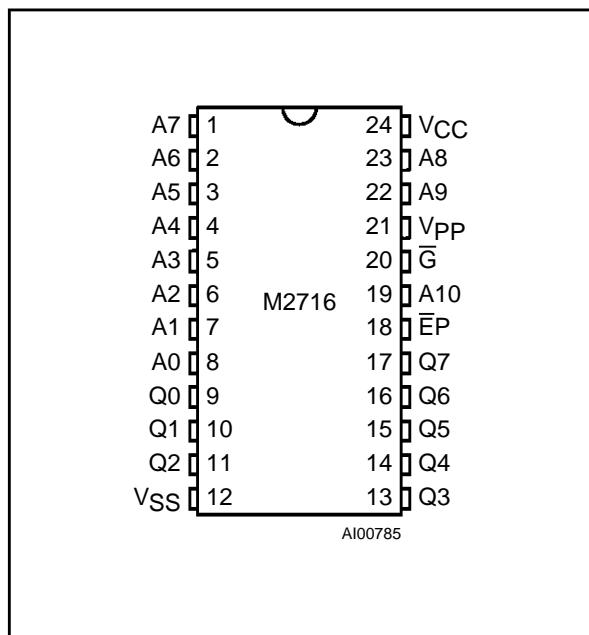
A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
\bar{EP}	Chip Enable / Program
\bar{G}	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

**Figure 1. Logic Diagram**

M2716**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 -40 to 85
T _{BIAS}	Temperature Under Bias	grade 1 grade 6	-10 to 80 -50 to 95
T _{TG}	Storage Temperature		-65 to 125
V _{CC}	Supply Voltage		-0.3 to 6
V _{IO}	Input or Output Voltages		-0.3 to 6
V _{PP}	Program Supply		-0.3 to 26.5
P _D	Power Dissipation		1.5

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections**DEVICE OPERATION**

The M2716 has 3 modes of operation in the normal system environment. These are shown in Table 3.

Read Mode. The M2716 read operation requires that $\bar{G} = V_{IL}$, $\bar{EP} = V_{IL}$ and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{AVQV} , t_{GLQV} or t_{ELQV} (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode. The M2716 is deselected by making $\bar{G} = V_{IH}$. This mode is independent of \bar{EP} and the condition of the addresses. The outputs are Hi-Z when $\bar{G} = V_{IH}$. This allows tied-OR of 2 or more M2716's for memory expansion.

Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making $\bar{EP} = V_{IH}$. This is independent of \bar{G} and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{AVQV} or t_{ELQV} (see Switching Time Waveforms).

Programming

The M2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table 3 shows the 3 programming modes.

Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (abyte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the \bar{EP} pin. All input voltage levels including the program pulse on chip enable are TTL compatible.

The programming sequence is: with $V_{PP} = 25V$, $V_{CC} = 5V$, $\bar{G} = V_{IH}$ and $\bar{EP} = V_{IL}$, an address is selected and the desired data word is applied to the output pins ($V_{IL} = 0$ and $V_{IH} = 1$ for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a

DEVICE OPERATION (cont'd)

pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than t_{PHPL} (max) on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming (as shown in Figure 6) or by reading all of the bytes out at the end of the programming sequence. This can be done with $V_{PP} = 25V$ or $5V$ in either case. V_{PP} must be at $5V$ for all operating modes and can be maintained at $25V$ for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\bar{G} = V_{IH}$ will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm² power rating is used. The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.

This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Table 3. Operating Modes

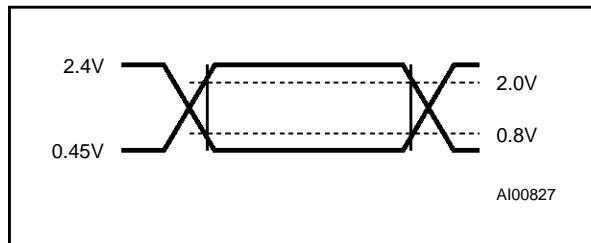
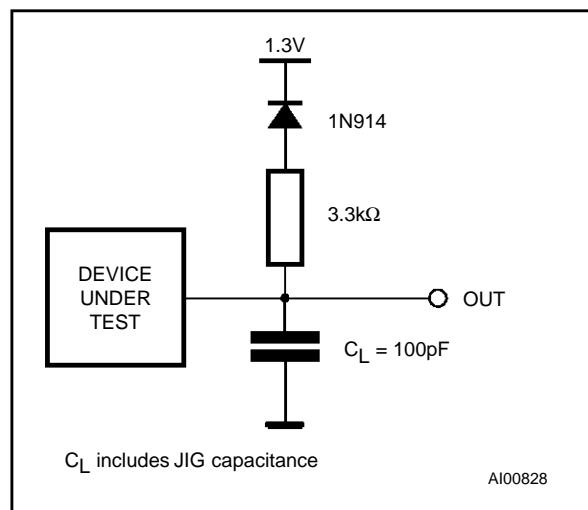
Mode	\bar{EP}	\bar{G}	V_{PP}	$Q_0 - Q_7$
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{PP} or V_{CC}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deselect	X	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL} .

M2716**AC MEASUREMENT CONDITIONS**

Input Rise and Fall Times	$\leq 20\text{ns}$
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms**Figure 4. AC Testing Load Circuit****Table 4. Capacitance⁽¹⁾ ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)**

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics⁽¹⁾
($T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 5\text{V} \pm 5\%$ or $5\text{V} \pm 10\%$; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$		± 10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$, $\bar{EP} = V_{CC}$		± 10	μA
I_{CC}	Supply Current	$\bar{EP} = V_{IL}$, $\bar{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\bar{EP} = V_{IH}$, $\bar{G} = V_{IL}$		25	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		-0.1	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$		0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Table 6. Read Mode AC Characteristics⁽¹⁾
 ($T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 5V \pm 5\%$ or $5V \pm 10\%$; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M2716				Unit	
				-1		blank			
				Min	Max	Min	Max		
tAVQV	tACC	Address Valid to Output Valid	$\bar{EP} = V_{IL}, \bar{G} = V_{IL}$		350		450	ns	
tELQV	tCE	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		350		450	ns	
tGLQV	toE	Output Enable Low to Output Valid	$\bar{EP} = V_{IL}$		120		120	ns	
tEHQZ ⁽²⁾	tOD	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	100	0	100	ns	
tGHQZ ⁽²⁾	tDF	Output Enable High to Output Hi-Z	$\bar{EP} = V_{IL}$	0	100	0	100	ns	
tAXQX	toH	Address Transition to Output Transition	$\bar{EP} = V_{IL}, \bar{G} = V_{IL}$	0		0		ns	

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

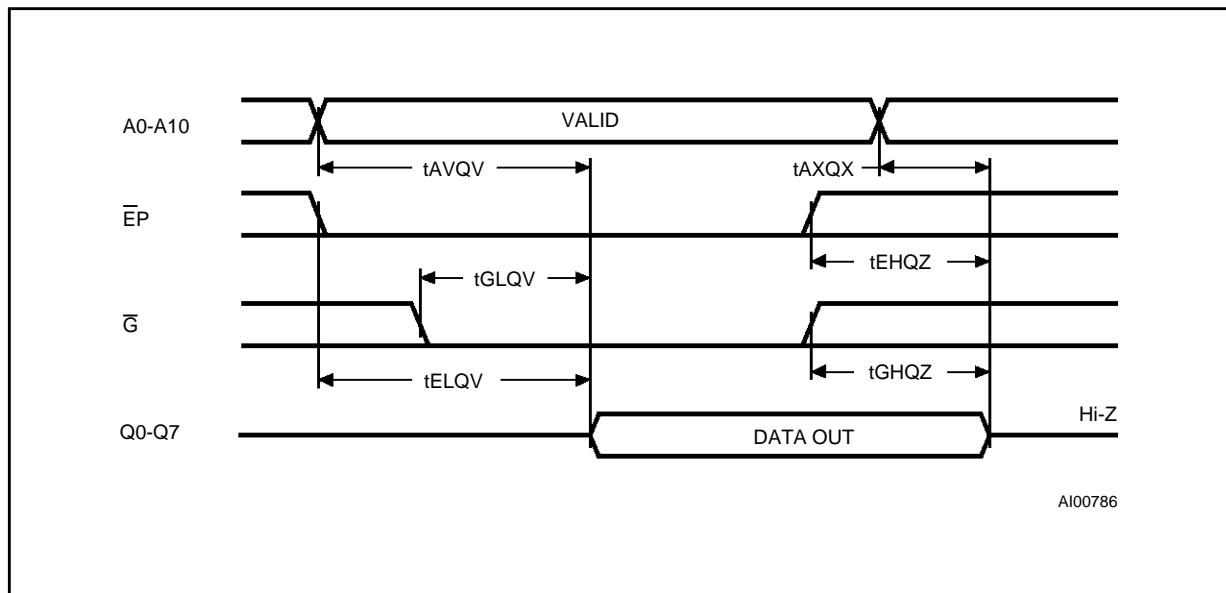


Table 7. Programming Mode DC Characteristics⁽¹⁾
 ($T_A = 25^\circ\text{C}$; $V_{CC} = 5V \pm 5\%$; $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		± 10	μA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current			5	mA
I_{PP1}	Program Current Pulse	$\bar{EP} = V_{IH}$ Pulse		30	mA
V_{IL}	Input Low Voltage		-0.1	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

M2716

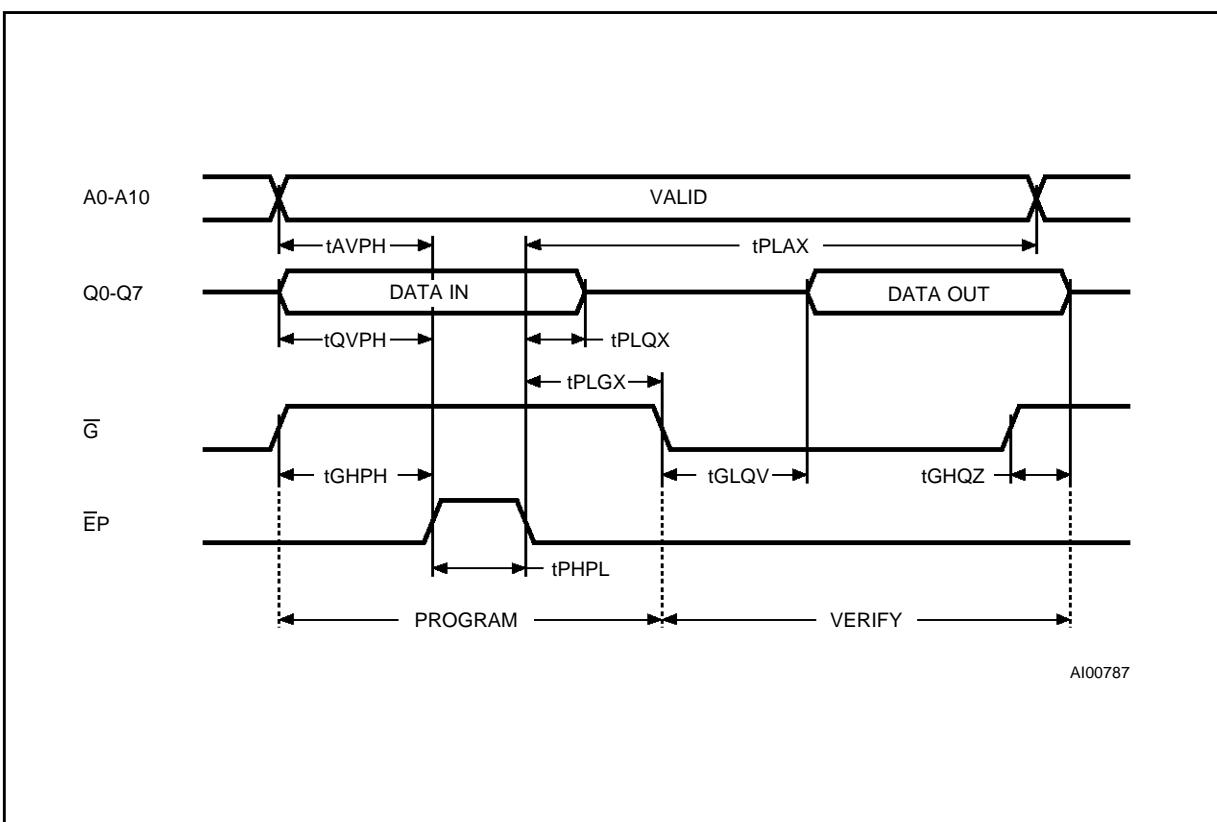
Table 8. Programming Mode AC Characteristics⁽¹⁾
 $(T_A = 25^\circ C; V_{CC} = 5V \pm 5\%; V_{PP} = 25V \pm 1V)$

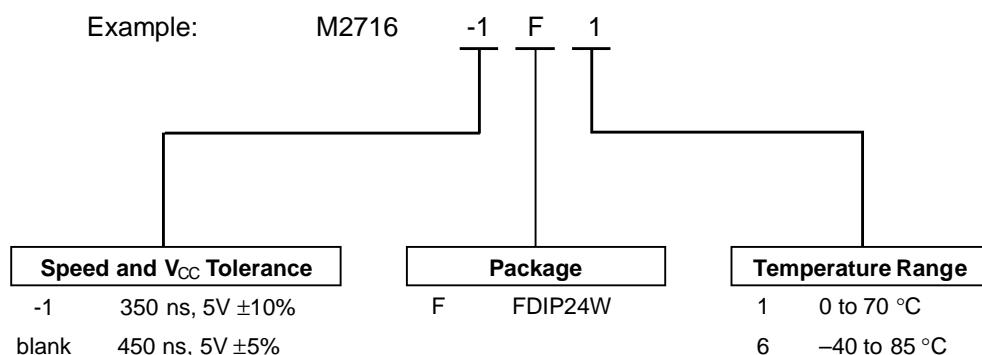
Symbol	Alt	Parameter	Test Condition	Min	Max	Units
tAVPH	tAS	Address Valid to Program High	$\bar{G} = V_{IH}$	2		μs
tQVPH	tDS	Input Valid to Program High	$\bar{G} = V_{IH}$	2		μs
tGPHH	tOS	Output Enable High to Program High		2		μs
tPL1PL2	tPR	Program Pulse Rise Time		5		ns
tPH1PH2	tPF	Program Pulse Fall Time		5		ns
tPHPL	tPW	Program Pulse Width		45	55	ms
tPLQX	tDH	Program Low to Input Transition		2		μs
tPLGX	tOH	Program Low to Output Enable Transition		2		μs
tGLQV	tOE	Output Enable to Output Valid	$\bar{EP} = V_{IL}$		120	ns
tGHQZ	tDF	Output Enable High to Output Hi-Z		0	100	ns
tPLAX	tAH	Program Low to Address Transition		2		μs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME

For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

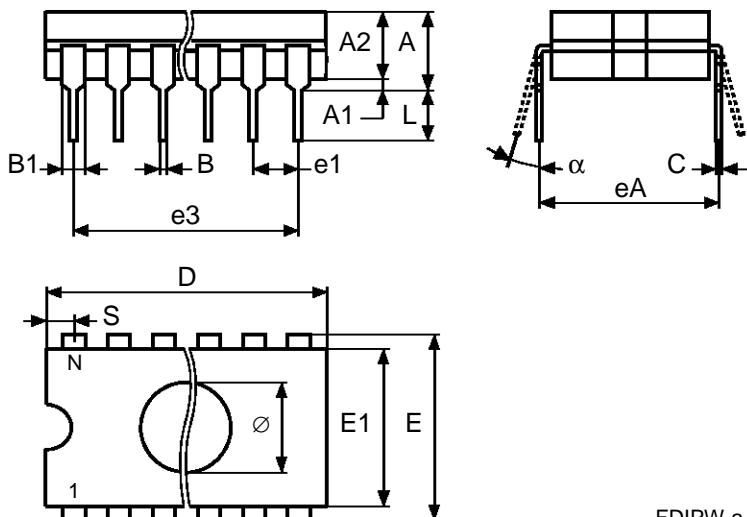
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

M2716

FDIP24W - 24 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			32.30			1.272
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	—	—	0.100	—	—
e3	27.94	—	—	1.100	—	—
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
Ø	7.11	—	—	0.280	—	—
α		4°	15°		4°	15°
N		24			24	

FDIP24W



Drawing is not to scale

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OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

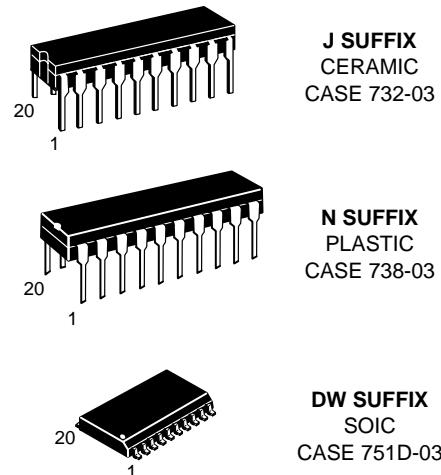
		LOADING (Note a)	
		HIGH	LOW
D ₀ -D ₇	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O ₀ -O ₇	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES:

- 1 TTL Units Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS373 SN54/74LS374

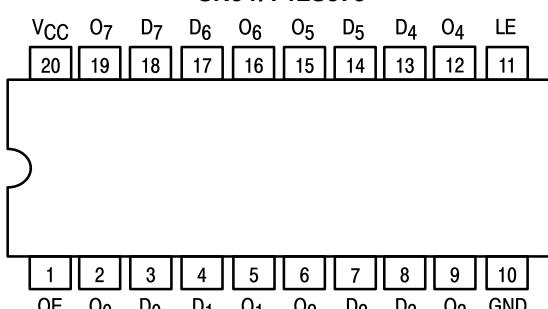
OCTAL TRANSPARENT LATCH
WITH 3-STATE OUTPUTS;
OCTAL D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUT
LOW POWER SCHOTTKY



ORDERING INFORMATION

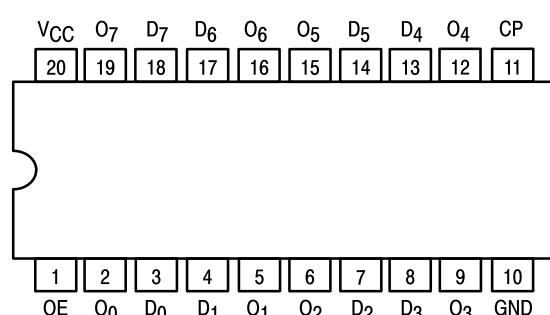
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

SN54/74LS373



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram)
as the Dual In-Line Package.

SN54/74LS374



SN54/74LS373 • SN54/74LS374

TRUTH TABLE

LS373

D _n	LE	OE	O _n
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z*

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

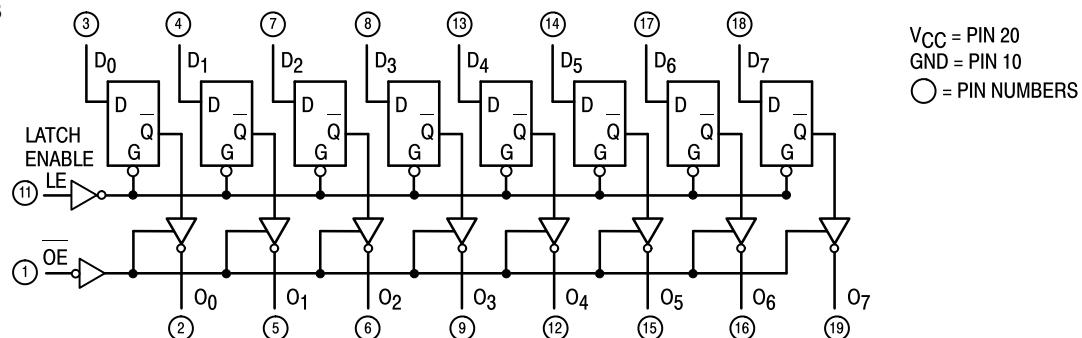
LS374

D _n	LE	OE	O _n
H	—	L	H
L	—	L	L
X	X	H	Z*

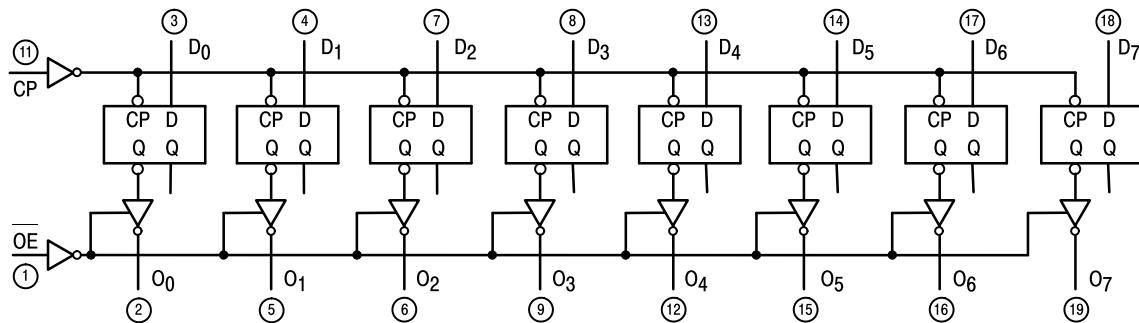
* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

LOGIC DIAGRAMS

SN54LS/74LS373



SN54LS/74LS374



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1			
V _{OL}	Output LOW Voltage	54, 74		0.25	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH			20	µA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW			-20	µA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current			20	µA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			40	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions		
		LS373			LS374						
		Min	Typ	Max	Min	Typ	Max				
f _{MAX}	Maximum Clock Frequency				35	50		MHz	C _L = 45 pF, R _L = 667 Ω		
t _{TPLH} t _{TPHL}	Propagation Delay, Data to Output		12 12	18 18				ns			
t _{TPLH} t _{TPHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns			
t _{TPZH} t _{TPZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns			
t _{TPHZ} t _{TPLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C _L = 5.0 pF		

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	
		LS373			LS374				
		Min	Max	Min	Max	Min	Max		
t _W	Clock Pulse Width	15		15		15		ns	
t _S	Setup Time	5.0		20		20		ns	
t _H	Hold Time	20		0		0		ns	

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN54/74LS373

AC WAVEFORMS

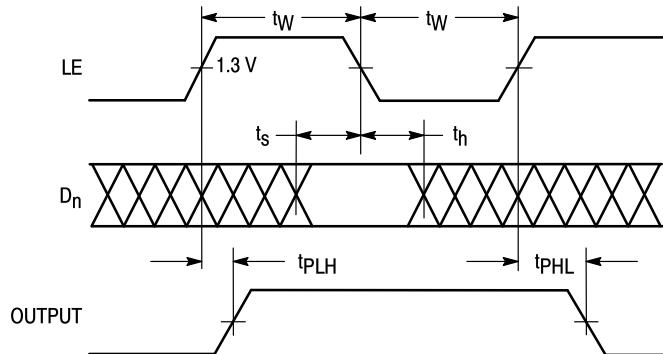


Figure 1

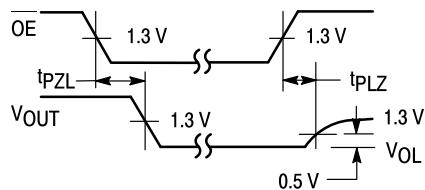


Figure 2

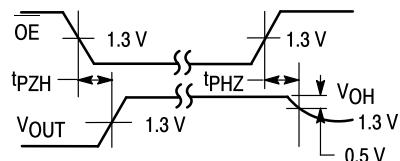
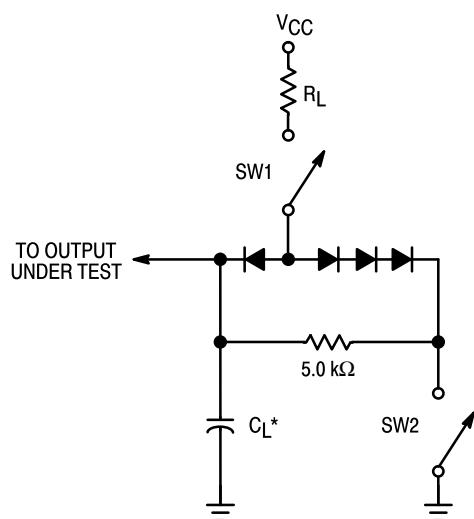


Figure 3

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 4

SN54/74LS374

AC WAVEFORMS

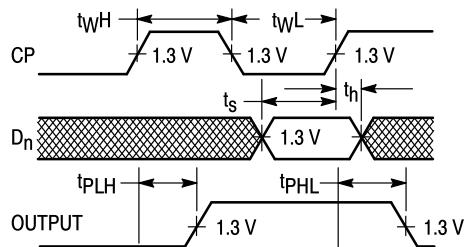


Figure 5

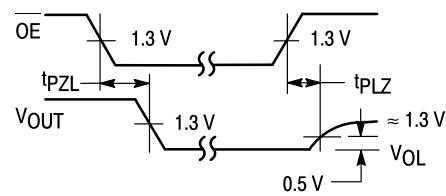


Figure 6

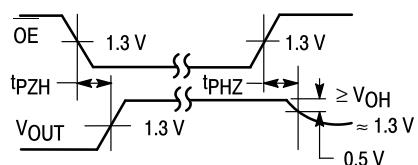
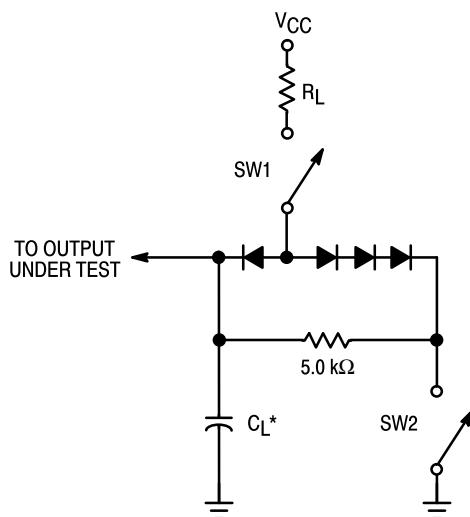


Figure 7

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

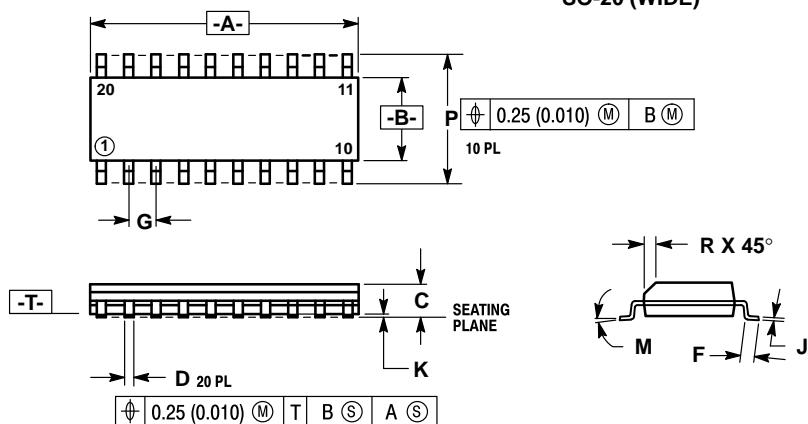
SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 8

Case 751D-03 DW Suffix

20-Pin Plastic

SO-20 (WIDE)



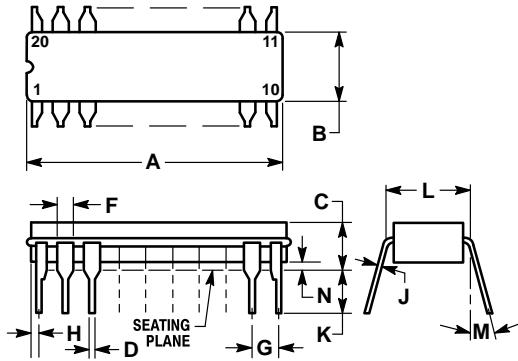
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC	0.050 BSC		
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Case 732-03 J Suffix

20-Pin Ceramic Dual In-Line



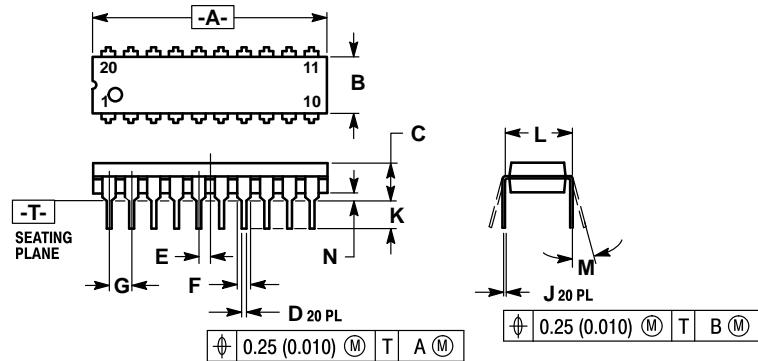
NOTES:

1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC	0.100 BSC		
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC	0.300 BSC		
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

Case 738-03 N Suffix

20-Pin Plastic



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. 738-02 OBSOLETE, NEW STANDARD 738-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC	0.050 BSC		
F	1.27	1.77	0.050	0.070
G	2.54 BSC	0.100 BSC		
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC	0.300 BSC		
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

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SYMBOL	SW1	SW2
tpZH	Open	Closed
tpZL	Closed	Open
tPLZ	Closed	Closed

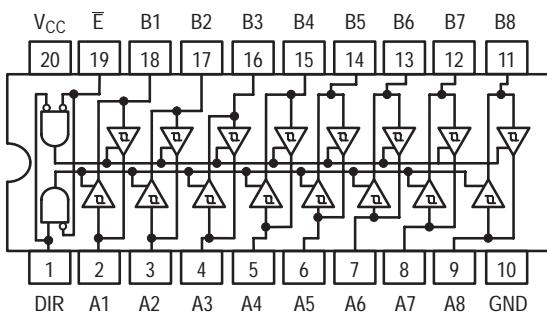
SN74LS245

Octal Bus Transceiver

The SN74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input (\bar{E}) can be used to isolate the buses.

- Hysteresis Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

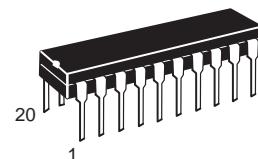


ON Semiconductor

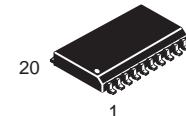
Formerly a Division of Motorola

<http://onsemi.com>

**LOW
POWER
SCHOTTKY**



PLASTIC
N SUFFIX
CASE 738



SOIC
DW SUFFIX
CASE 751D

TRUTH TABLE

INPUTS		OUTPUT
\bar{E}	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-3.0	mA
				-15	mA
I_{OL}	Output Current – Low			24	mA

ORDERING INFORMATION

Device	Package	Shipping
SN74LS245N	16 Pin DIP	1440 Units/Box
SN74LS245DW	16 Pin	2500/Tape & Reel

SN74LS245

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{T+}-V_{T-}$	Hysteresis	0.2	0.4		V	$V_{CC} = \text{MIN}$
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.4	3.4		V	$V_{CC} = \text{MIN}$, $I_{OH} = -3.0 \text{ mA}$
		2.0			V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 24 \text{ mA}$
I_{OZH}	Output Off Current HIGH			20	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 2.7 \text{ V}$
I_{OZL}	Output Off Current LOW			-200	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.4 \text{ V}$
I_{IH}	Input HIGH Current	A or B, DR or \bar{E}		20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
		DR or \bar{E}		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
		A or B		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 5.5 \text{ V}$
I_{IL}	Input LOW Current			-0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Output Short Circuit Current (Note 1)	-40		-225	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW Total at HIGH Z			70	mA	$V_{CC} = \text{MAX}$
				90		
				95		

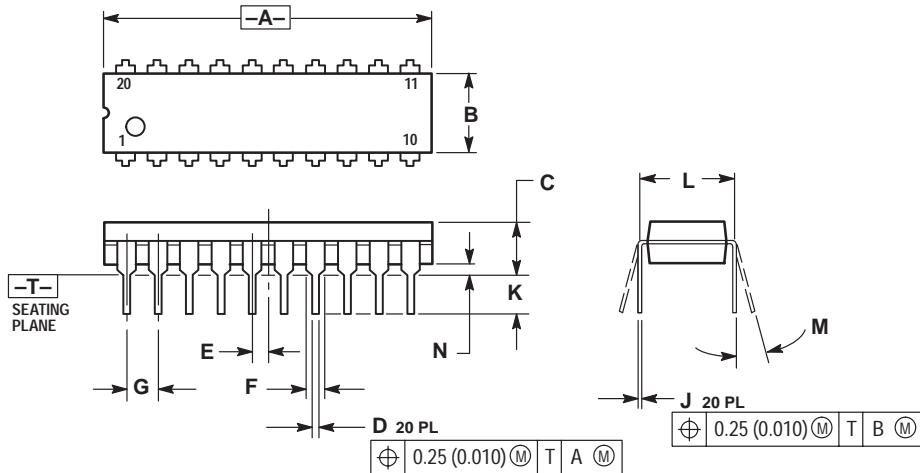
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$, $T_{RISE}/T_{FALL} \leq 6.0 \text{ ns}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	$C_L = 45 \text{ pF}$, $R_L = 667 \Omega$
t_{PZH}	Output Enable Time to HIGH Level		25	40	ns	
t_{PZL}	Output Enable Time to LOW Level		27	40	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25	ns	$C_L = 5.0 \text{ pF}$, $R_L = 667 \Omega$
t_{PHZ}	Output Disable Time from HIGH Level		15	25	ns	

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 738-03
ISSUE E

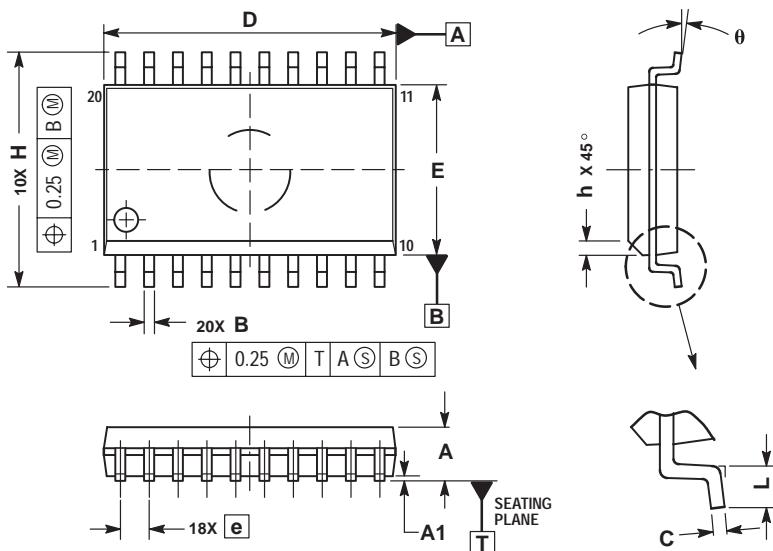


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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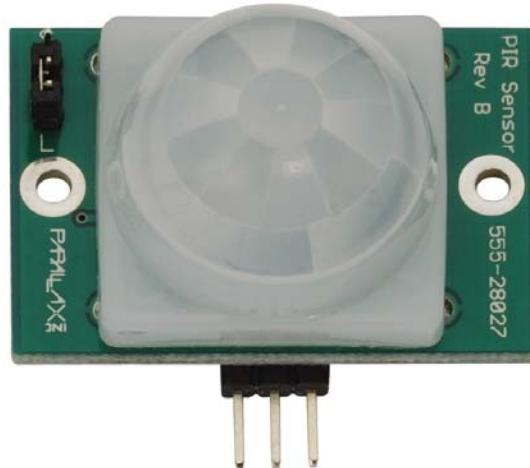
PIR Sensor (#555-28027)

The PIR (Passive Infra-Red) Sensor is a pyroelectric device that detects motion by sensing changes in the infrared (radiant heat) levels emitted by surrounding objects. This motion can be detected by checking for a sudden change in the surrounding IR pattern. When motion is detected the PIR sensor outputs a high signal on its output pin. This logic signal can be read by a microcontroller or used to drive an external load; see the source current limits in the features list below.

NOTE: Revision B of this sensor provides many updates and improvements from Revision A. If your PIR Sensor's PCB does not read "Rev B," please use the information found in the Revision History section on page 5.

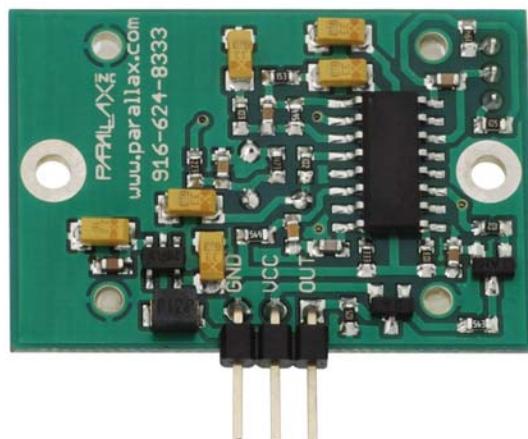
Features

- Detect a person up to approximately 30 ft away, or up to 15 ft away in reduced sensitivity mode
- Jumper selects normal operation or reduced sensitivity
- Source current up to 12 mA @ 3 V, 23 mA @ 5 V
- Onboard LEDs light up the lens for fast visual feedback when movement is detected
- Mounting holes for #2 sized screws
- 3-pin SIP header ready for breadboard or through-hole projects
- Small size makes it easy to conceal
- Easy interface to any microcontroller



Key Specifications

- Power Requirements: 3 to 6 VDC; 130 µA idle, 3 mA active (no load)
- Communication: Single bit high/low output
- Operating temperature: 32 to 122 °F (0 to 50 °C)
- Dimensions: 1.41 x 1.0 x 0.8 in (35.8 x 25.4 x 20.3 cm)



Application Ideas

- Motion-activated nightlight
- Alarm systems
- Holiday animated props

Theory of Operation

Pyroelectric devices, such as the PIR sensor, have elements made of a crystalline material that generates an electric charge when exposed to infrared energy. The changes in the amount of infrared energy striking the element change the voltages generated, which are measured by an on-board amplifier. The device contains a Fresnel lens, which focuses the infrared signals onto the element. As the ambient infrared signals change rapidly, the on-board amplifier trips the output to indicate motion.

The onboard jumper allows the user to select between normal operation and reduced sensitivity. The sensitivity of the PIR Sensor varies with temperature and other environmental conditions. Generally, when in reduced sensitivity mode, the PIR sensor will detect an object at up to half the distance it would in normal operating mode. For more information, see the Range section below.

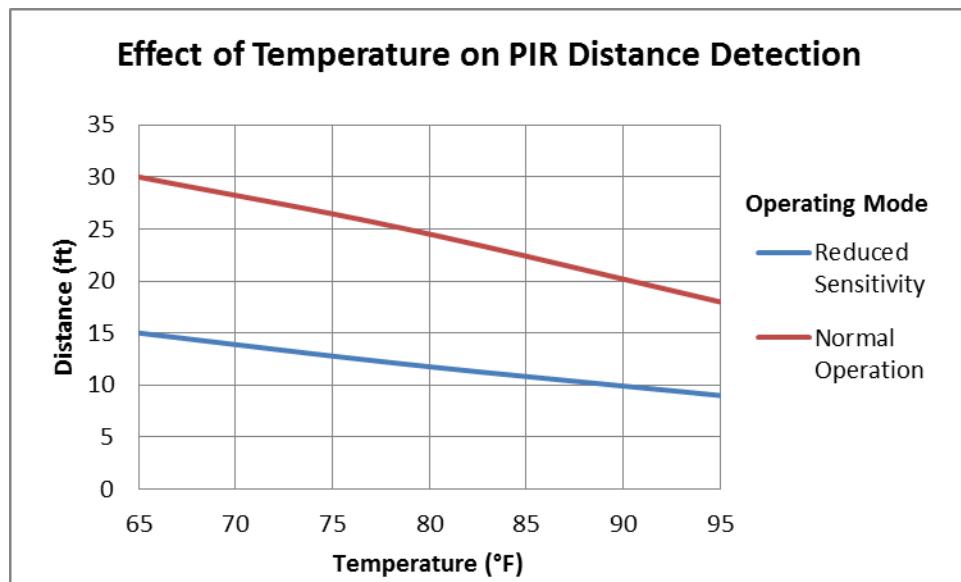
Range

The PIR Sensor's range is affected by:

- The sensitivity jumper setting
- The size and thermal properties of nearby objects
- Environmental conditions including ambient temperature and light sources

The graph below depicts the approximate effects of known ambient temperatures on the PIR Sensor's detection range of an average adult.

The graph below depicts the approximate effects of known temperatures on the PIR Sensor's detection range of an adult. *Note: This device is designed for indoor use. Operation outside or in extreme temperatures may negatively affect stability. Direct exposure to sunlight or other forms of radiant heating may cause undesired operation.*



Pin Definitions and Ratings

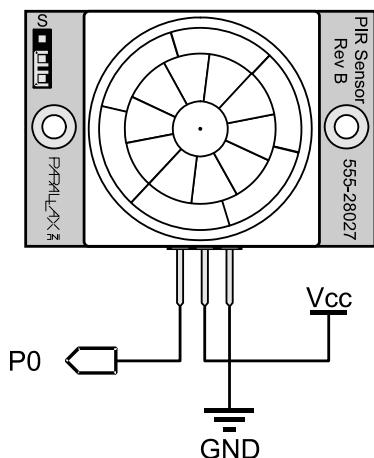
Pin	Name	Type	Function
1	GND	G	Ground: 0 V
2	Vcc	P	Supply Voltage: 3 to 6 VDC
3	OUT	O	PIR signaling; HIGH = movement/LOW = no movement

Pin Type: P = Power, G = Ground, I = Input, O = Output

Jumper Settings

Symbol	Description
S	Reduced sensitivity mode, for a shorter range, about 15 feet maximum
L	Normal operation, for a longer range, about 30 feet maximum

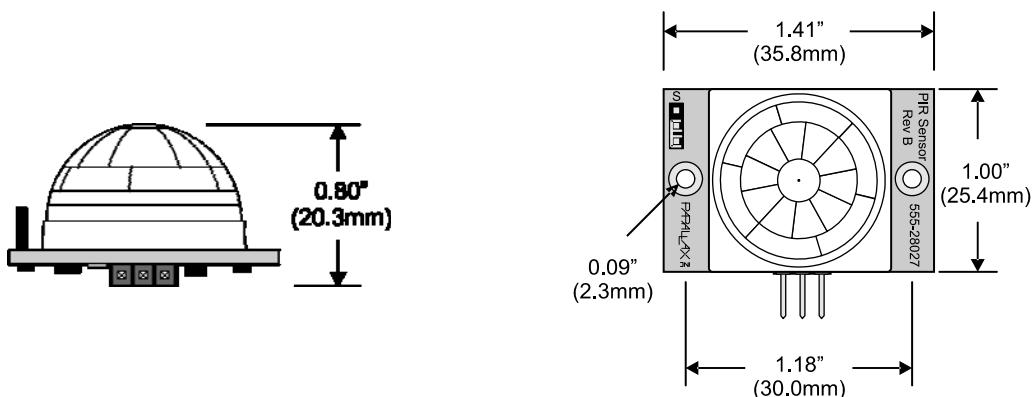
Quick-Start Circuit



Calibration

The PIR Sensor requires a warm-up time in order to function properly. This is due to the settling time involved in "learning" its environment. This could be up to 40 seconds. During this time, the LEDs under the lens will be on and there should be as little motion as possible in the sensors field of view.

Module Dimensions



BASIC Stamp® Example Code

This program will display the current state of the output pin from the PIR Sensor connected to P0 using the Debug Terminal. The Debug Terminal is built into the BASIC Stamp Editor software. The software is a free download from www.parallax.com/basicstampsoftware.

```
' PIR_Simple.bs2
' Displays the current state of the PIR Sensor connected to P0

' {$STAMP BS2}
' {$PBASIC 2.5}

PAUSE 40000                                ' PIR warm-up time

DO
    DEBUG HOME, BIN1 IN0                  ' Display state of P0
    PAUSE 100                            ' Small Delay
LOOP                                         ' Repeat Forever
```

Propeller™ P8X32A Example Code

Note: This application uses the Parallax Serial Terminal to display the device output. The object and the Parallax Serial Terminal itself are included with the Propeller Tool v1.2.7 or higher, which is available from the Downloads link at www.parallax.com/Propeller.

```
'' PIR_Simple.spin
'' Displays the current state of the PIR Sensor connected to P0

CON

_clkmode = xtall + pll16x                 ' Setting Clock Mode to Crystal 1 with 16 multiplier
_xinfreq = 5_000_000                       ' Propeller set to run at 80MHz

VAR

    byte state                           ' Declare variable state to store PIR output

OBJ

    pst : "Parallax Serial Terminal"

PUB PIR                                     ' Public Method name PIR

    dira[0]~                             ' Set pin 0 to input

    pst.start(115200)                     ' Start Parallax Serial Terminal at 115200 baud
    waitcnt(clkfreq * 40 + cnt)           ' PIR "warm-up" time
    pst.clear                            ' Clear the screen

    repeat
        state := ina[0]                   ' Save state of PIR Sensor
        pst.home                          ' Move cursor to position(0,0)
        pst.str(string(''IN0 = ''))       ' Display state
        pst.bin(state, 1)                 ' Small delay
        waitcnt(clkfreq/200 + cnt)
```

Revision History

The information that follows contains revision history for the PIR documentation.

V 2.0: PIR Sensor Rev A

Both revisions of this sensor use the same Fresnel lens, and basic functionality remains the same between the two (for example you can use the same test programs). However, there were a number of improvements and updates made to Revision B, and if using Revision A in your project the following information should be noted and used.

Features

- Detection range up to 20 feet away
- Single bit output
- Jumper selects single or continuous trigger output mode
- 3-pin SIP header ready for breadboard or through-hole project
- Small size makes it easy to conceal
- Compatible with BASIC Stamp, Propeller, and many other microcontrollers

Key Specifications

- Power Requirements: 3.3 to 5 VDC; >3 mA (**may vary**)
- Communication: Single bit high/low output
- Operating temperature: 32 to 122 °F (0 to 50 °C)
- Dimensions: 1.27 x 0.96 x 1.0 in (32.2 x 24.3 x 25.4 mm)

Key Differences

- Jumper setting controls triggering and not distance
- Driving an external load requires a transistor or MOSFET
- Detection range up to 20 ft away

Pin Definitions and Ratings

Pin	Name	Function
-	GND	Ground: 0 V
+	Vin	Supply Voltage: 3 to 6 VDC
OUT	Output	Connect to I/O pin set to INPUT mode (or transistor/MOSFET).

Jumper Settings

Symbol	Description
H	Output remains HIGH when sensor is retriggered repeatedly. Output is LOW when idle (not triggered).
L	Output goes HIGH then LOW when triggered. Continues motion results in repeated HIGH/LOW pulses. Output is LOW when idle.

V 2.1: The explanation of the sensitivity jumper setting have been updated throughout, and the Range section, including a temperature vs. range graph, were added.

V 2.1: Added information for load current to Features and Specifications.

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RJ Series Relays

Features

- Compact size:
Blade: 12.7 x 27 x 28.8 mm
PCB: 12.7 x 25.5 x 28.8 mm
- Contact rating:
Blade: 8A (DPDT), 12A (SPDT)
PCB: 8A (DPDT & DPST-NO), 12A (SPDT & SPST-NO),
16A (SPDT & SPST-NO)
- Operational life:
200K cycles at full resistive AC load;
50 million cycles, no load
- Blade model has optional green, non-polarized LED
- RoHS compliant



Specifications

General Information	Blade Models		PCB Models				
	RJ1S	RJ2S	RJ1V	(High Capacity)	RJ2V		
No. of poles	1	2	1	1	2		
Contact Configuration	SPDT	DPDT	SPDT, SPST-NO	DPDT, DPST-NO			
Contact Rating	12A	8A	12A	16A	8A		
Contact Material	AgNi		AgNi	AgSnIn	AgNi		
Enclosure Ratings	–		Flux protection				
Contact Resistance	50 milliohms max		50 milliohms max ^{Note 1}				
Operating Time	15ms max		15ms max ^{Note 2}				
Release Time	10ms max		10ms max ^{Note 2}				
Dielectric Strength	Between contact & coil	5,000V AC, 1 minute	5,000V AC, 1 minute				
	Between contacts of same poles	1,000V AC, 1 minute	1,000V AC, 1 minute				
	Between contacts of different poles	– 3,000V AC, 1 min.	–	3,000V AC, 1 min.			
Vibration Resistance	Damage limits	10-55Hz, amplitude 0.75mm	10-55Hz, amplitude 0.75mm				
	Operating extremes	10-55Hz, amplitude 0.75mm	10-55Hz, amplitude 0.75mm				
Shock Resistance	Damage limits	100m/s ² min (10G)	NO contact: 200m/s ² (20G) NC contact: 100m/s ² (10G)				
	Operating extremes	1,000m/s ² min (100G)	1,000m/s ² min (100G)				
Mechanical Life	AC	30,000,000 operations	30,000,000 operations				
	DC	50,000,000 operations	50,000,000 operations				
Electrical Life @	AC	200,000 operations	200,000 operations				
Full Rated Load	DC	100,000 operations	100,000 operations				
Operating Temperature	-40 to 70° C		-40 to 70° C ^{Note 3}				
Operating Humidity	5 to 85% RH		5 to 85% RH				
Dimensions (H x W x D mm)	12.7 x 27 x 28.8		12.7 x 25.5 x 28.8				
Weight (Approx.)	19g		SPDT: 17g, SPST-NO: 16g	DPDT: 17g, DPST-NO: 16g			

- Notes:
1. Measured using 5V DC, 1A voltage drop method.
 2. Measured at the rated voltage (at 20°C), excluding contact bounce time.
 3. 100% rated voltage.

Ordering Information

Blade Models

R J	S - C	-	Coil Voltage
Contact Configuration	Options		D12 - 12V DC D24 - 24V DC D48 - 48V DC D100 - 100-110V DC A24 - 24V AC A120 - 120V AC A240 - 240V AC
1 - SPDT 2 - DPDT	Blank - Standard L - LED		

PCB Models

R J	V	-	Number of Poles	Contact Configuration	Contact Configuration	Coil Voltage
			1 - SP (Single Pole) 2 - DP (Double Pole)	C - FORM C (DT Double Throw) A - FORM A (ST Single Throw)	Blank - Standard H - High Capacity Type (RJ1 only)	D5 - 5V DC D6 - 6V DC D12 - 12V DC D24 - 24V DC D48 - 48V DC D100 - 100-110V DC A24 - 24V AC A120 - 120V AC A240 - 240V AC

Contact Ratings

Contact Ratings	Type	Contact	Allowable Contact Power		Rated Load			Allowable Switching Current	Allowable Switching Voltage	Minimum Applicable Load
			Resistive Load	Inductive Load	Voltage	Resistive Load	Inductive Load cos = 0.3 L/R=7ms			
Blade Models	1 pole	NO	AC3000V	AC1875VA	250V AC	12A	7.5A	6A	AC250V	DC5V
		NC	AC3000V	AC1875VA	250V AC	12A	7.5A	6A/3A	DC30V	100mA
	2 poles	NO	AC2000V	AC1000VA	250V AC	8A	4A	4A	AC250V	DC5V
		NC	AC2000V	AC1000VA	250V AC	8A	4A	4A/2A	DC30V	100mA
	PCB Models	Standard Type	NO	AC3000V	AC1875VA	AC250V	12A	7.5A	12A	AC250V DC125V
			DC360W	DC180W	DC30V	12A	6A			
		High Capacity Type	NO	AC3000V	AC1875VA	AC250V	12A	7.5A		
			DC180W	DC90W	DC30V	6A	3A			
		1 pole	NO	AC4000V	AC2000VA	AC250V	16A	8A	16A	AC250V DC125V
			DC480W	DC240W	DC30V	16A	8A			
		2 poles	NO	AC4000V	AC2000VA	AC250V	16A	8A		
			DC240W	DC120W	DC30V	8A	4A			
		NC	AC2000V	AC1000VA	AC250V	8A	4A	8A	AC250V DC125V	DC5V 10mA
			DC120W	DC60W	DC30V	4A	2A			

Coil Ratings

AC	Rated Voltage	Coil Voltage Code	Rated Current (mA) ±15% (at 20°C)				Coil Resistance (ohms) ±10% (at 20°C)	Operating Characteristics ²			Power Consumption				
			Without LED ¹		With LED ¹			Minimum Pickup Voltage	Dropout Voltage	Maximum Allowable Voltage ³					
			50Hz	60Hz	50Hz	60Hz									
Blade & PCB Models	24V	A24	43.9	37.5	47.5	41.1	243	80% max	30% min	140%	0.9VA (60Hz)				
	120V	A120	8.8	7.5	8.7	7.4	6,400								
	240V	A240	4.3	3.7	4.3	3.7	25,570								
DC	Blade Models	Rated Voltage	Coil Voltage Code	Rated Current (mA) ±15% (at 20°C)				70% max	10% min	170%	0.53W				
				Without LED ¹		With LED ¹									
		12V	D12	44.2		48.0									
		24V	D24	22.1		25.7									
		48V	D48	11.0		10.7									
		100-110V	D100	5.3 - 5.8		5.2 - 5.7									
		5V	D5	106		—									
		6V	D6	88.3		—									
PCB Models	Blade Models	12V	D12	44.2		—		70% max	10% min	170%	0.53-0.64W				
		24V	D24	22.1		—									
		48V	D48	11.0		—									
		100-110V	D100	5.3 - 5.8		—									
		5V	D5	106		—									
		6V	D6	88.3		—									

Notes:

1. LED Indicator is only available on Blade relays.
2. Operating characteristics are against rated values at 20°C.
3. The maximum allowable voltage is the maximum value which can be applied to the relay coils.

Accessories

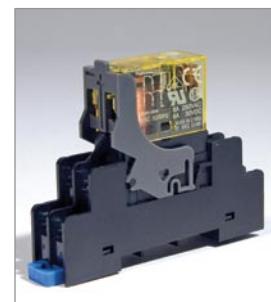
Socket Part Numbers

Relay Type	Socket Type	Socket Part Number
RJ1S (Std)	DIN Rail Standard	SJ1S-05B
	DIN Rail Fingersafe	SJ1S-07L
	PCB Mount	SJ1S-61
RJ1S-□ H (HC), RJ2S	DIN Rail Standard	SJ2S-05B
	DIN Rail Fingersafe	SJ2S-07L
	PCB Mount	SJ2S-61
RJ1V (Std)	DIN Rail Fingersafe	SQ1V-07B*
	PCB Mount	SQ1V-63
RJ1V-□ H (HC), RJ2V	DIN Rail Fingersafe	SQ2V-07B*
	PCB Mount	SQ2V-63

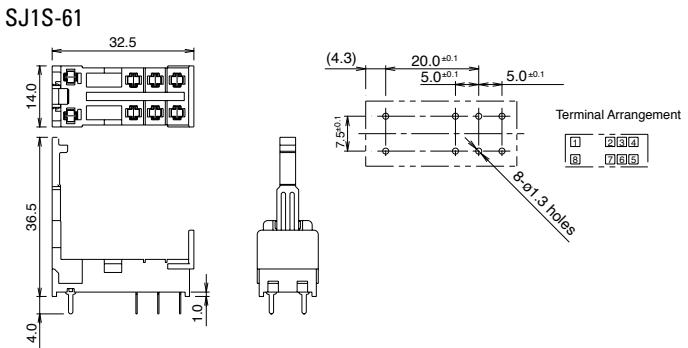
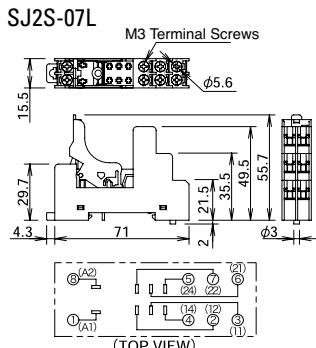
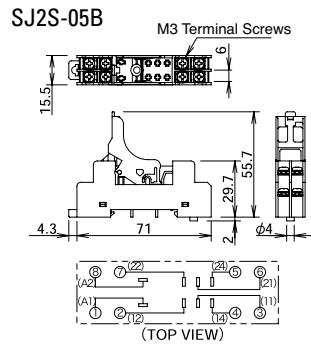
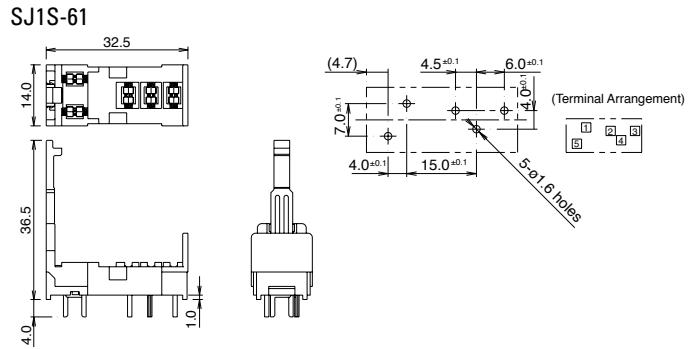
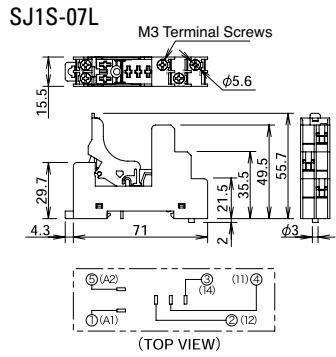
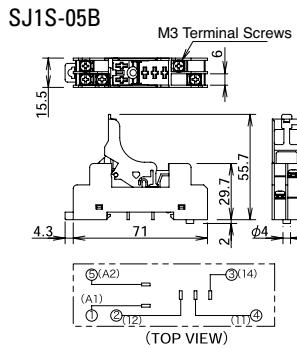
*Hold-down clip or spring must be removed to use with RJ relays.

Socket Specifications

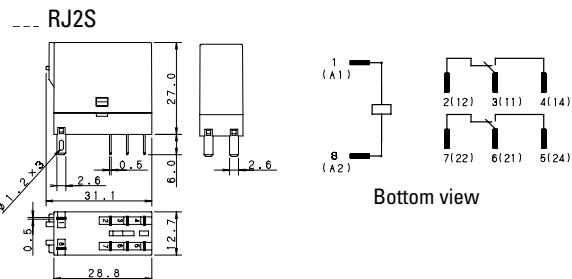
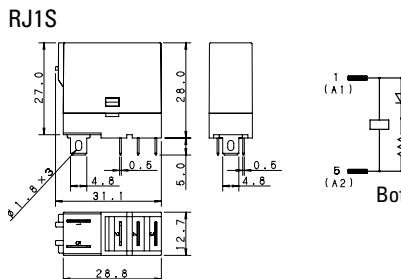
Specifications	SJ1S	SJ2S
Rated Insulation Voltage	250V AC/DC	
Applicable Wire	Max up to 2 - #14 AWG	
Applicable Crimping Terminal	2mm ² x 2	
Screw Size	M3 Slotted-Phillips screw	
Weight	30g	34g



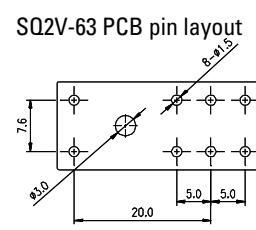
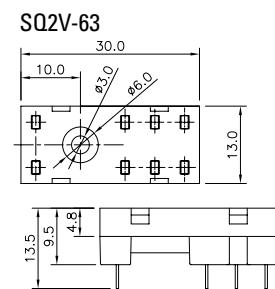
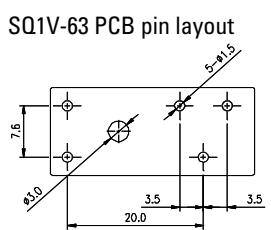
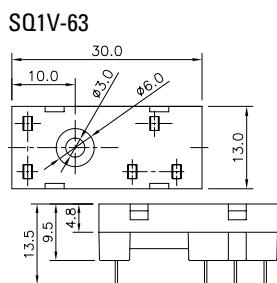
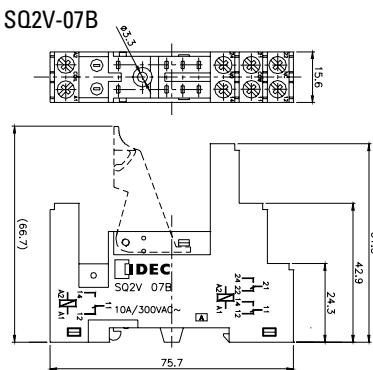
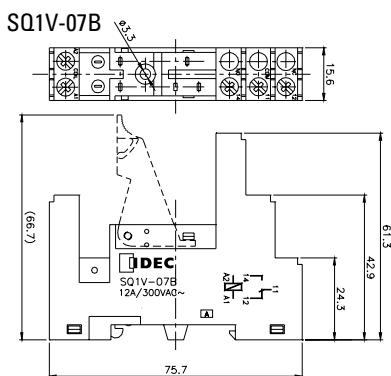
Socket Dimensions - for Blade Relays (mm)



Blade Relay Dimensions (mm)

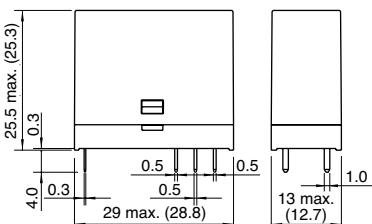


SQ Socket Dimensions - for PCB Relays (mm)

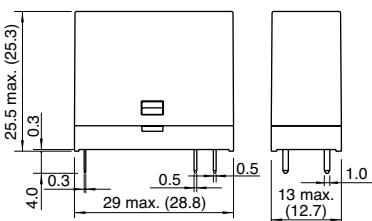


PCB Relay Dimensions (mm)

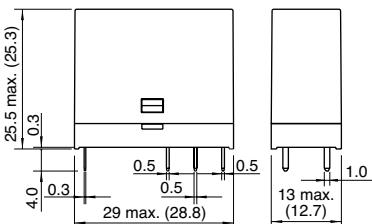
RJ1V-C-*
SPDT



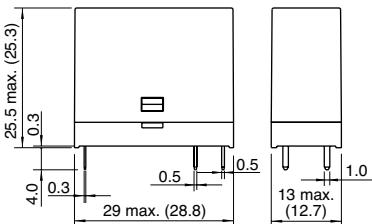
RJ1V-A-*
SPST-NO



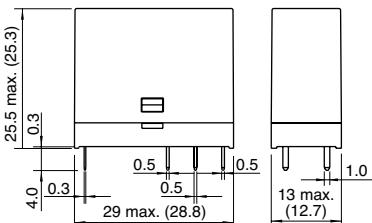
RJ1V-CH-*
SPDT
High Capacity



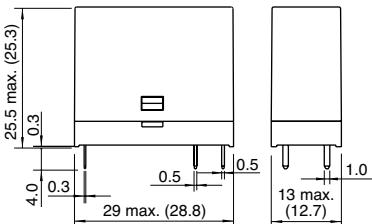
RJ1V-AH-*
SPST-NO
High Capacity



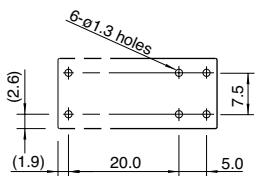
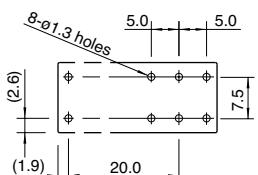
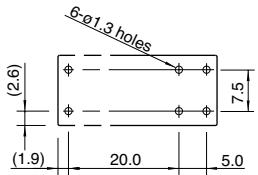
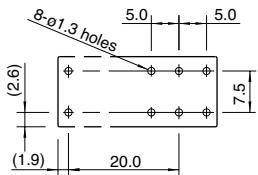
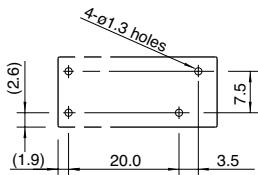
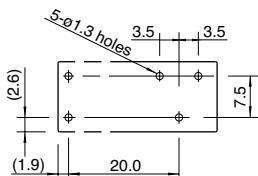
RJ2V-C-*
DPDT



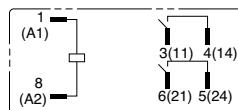
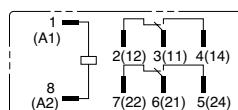
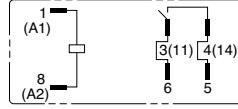
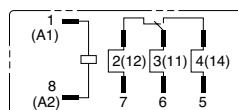
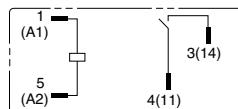
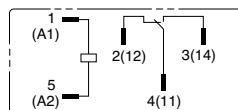
RJ1V-A-*
DPST-NO



PCB Mounting Hole Layout (Bottom View)



PCB Internal Circuit Diagrams (Bottom View)



For more information on the these
and other IDEC relays, visit:

www.idec.com/relay



August 1986
Revised March 2000

DM74LS138 • DM74LS139 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
 - Memory decoders
 - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
 - DM74LS138 21 ns
 - DM74LS139 21 ns
- Typical power dissipation
 - DM74LS138 32 mW
 - DM74LS139 34 mW

Ordering Code:

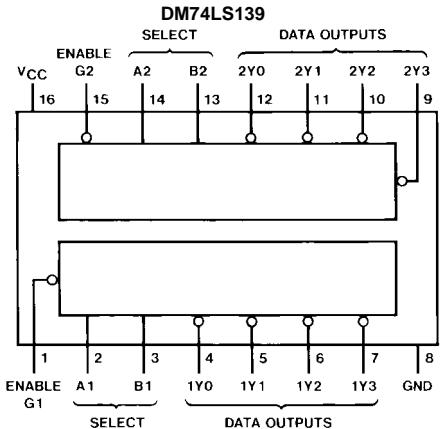
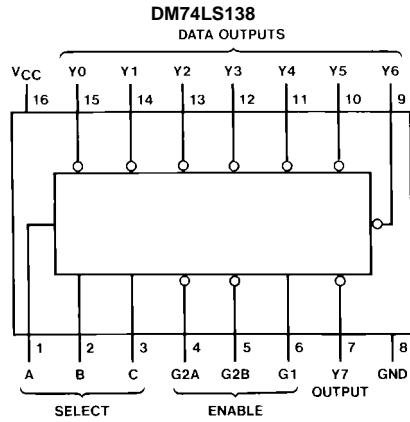
Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS139M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS139SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

DM74LS138 • DM74LS139 Decoder/Demultiplexer

DM74LS138 • DM74LS139

Connection Diagrams



Function Tables

DM74LS138

Inputs			Outputs										
Enable		Select	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
G ₁	G ₂ (Note 1)		X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H	H
H	L	L	H	L	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	L

DM74LS139

Inputs			Outputs			
Enable		Select	Y ₀	Y ₁	Y ₂	Y ₃
G	B	A	H	H	H	H
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level

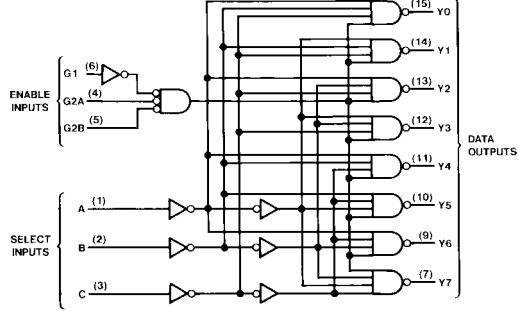
L = LOW Level

X = Don't Care

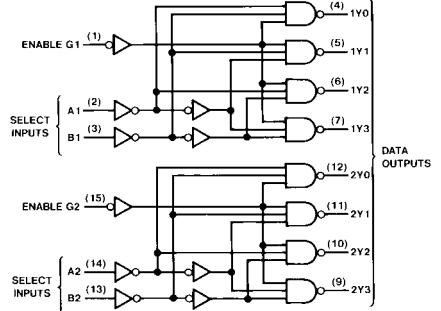
Note 1: G₂ = G_{2A} + G_{2B}

Logic Diagrams

DM74LS138



DM74LS139



Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS138 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

DM74LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IL} = Max, V _{IH} = Min		0.35	0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 4)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 5)		6.3	10	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R _L = 2 kΩ		Units	
				C _L = 15 pF			
				Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	2		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	2		27		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	3		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	3		27		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	2		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	2		24		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	3		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	3		28		

DM74LS139 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_h = -18 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$, $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$		0.35	0.5	V
		$V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$, $V_I = 7V$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$, $V_I = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$, $V_I = 0.4V$			-0.36	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 7)	-20		-100	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 8)		6.8	11	mA

Note 6: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

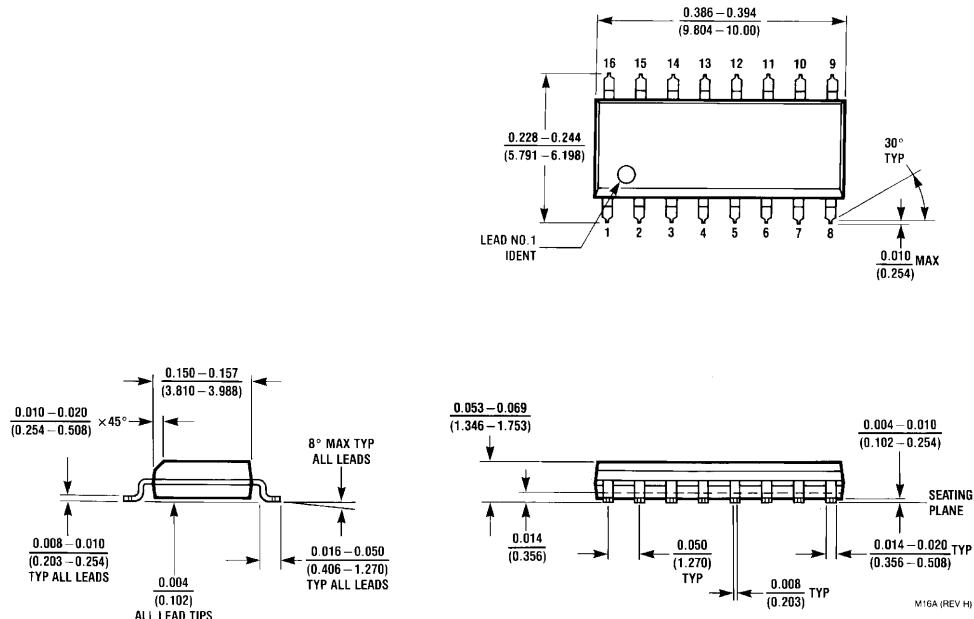
Note 8: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS139 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$

Symbol	Parameter	From (Input) To (Output)	$R_L = 2 \text{ k}\Omega$				Units	
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$			
			Min	Max	Min	Max		
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output		18		27	ns	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output		27		40	ns	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output		18		27	ns	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output		24		40	ns	

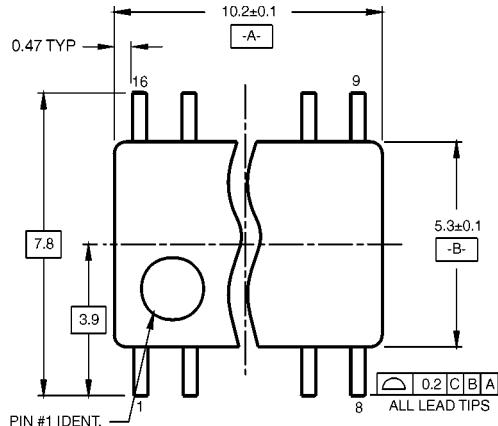
Physical Dimensions inches (millimeters) unless otherwise noted



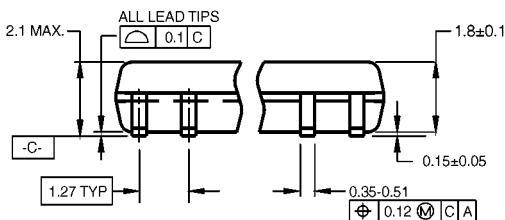
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

DM74LS138 • DM74LS139

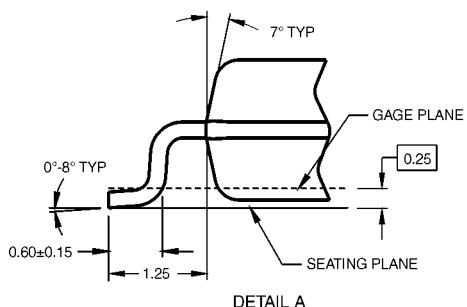
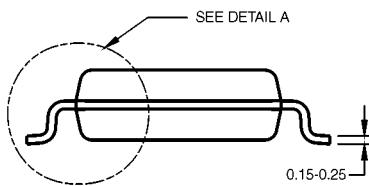
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



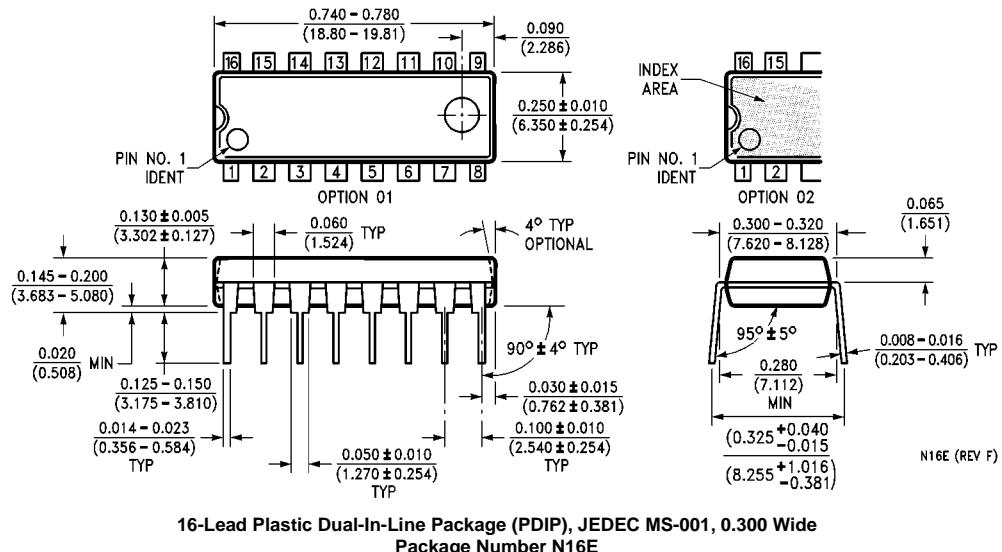
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

8284A/8284A-1

Clock Generator and Driver for 8086, 8088 Processors

8284A/8284A-1

3

DISTINCTIVE CHARACTERISTICS

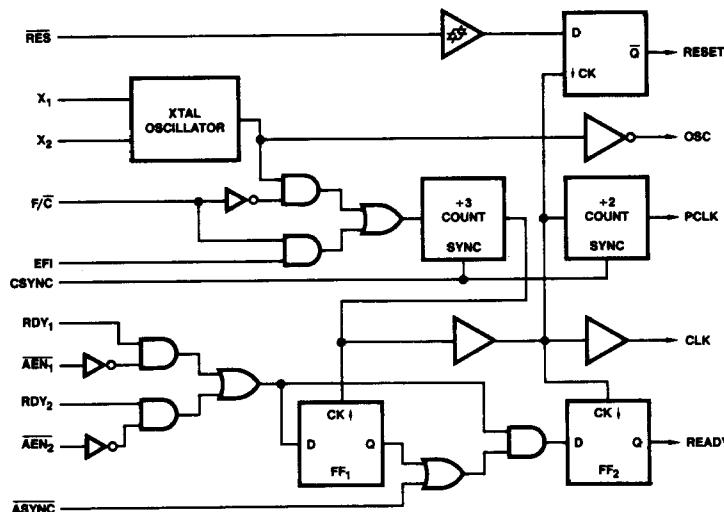
- Generates the System Clock for the 8086, 8088 Processors: 5MHz, 8MHz with 8284A; 10MHz with 8284A-1
- Uses a crystal or a TTL signal for frequency source
- Provides local READY and Multibus® READY synchronization
- Generates system reset output from Schmitt trigger input
- Capable of clock synchronization with other 8284As

GENERAL DESCRIPTION

The 8284A is a single chip clock generator/driver for the 8086, 8088 processors. The chip contains a crystal-con-

trolled oscillator, a divide-by-three counter, complete MULTIBUS® "Ready" synchronization and reset logic.

BLOCK DIAGRAM

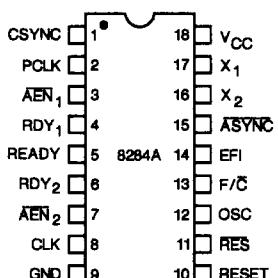


BD001440

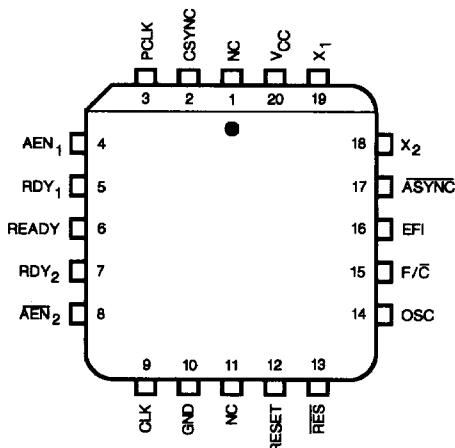
RELATED AMD PRODUCTS

Part No.	Description
Am8086	16-Bit Microprocessor
8288	Bus Controller

*MULTIBUS is a registered trademark of Intel Corp.

**CONNECTION DIAGRAMS
Top View****DIPs**

CD001582

PLCC

CD009272

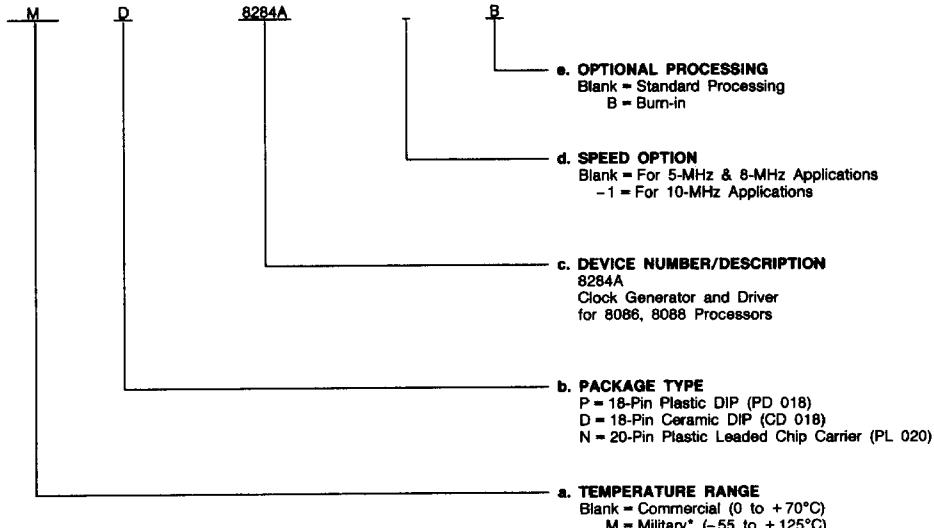
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: a. **Temperature Range**

- a. Temperature Range
 - b. Package Type
 - c. Device Number
 - d. Speed Option
 - e. Optional Processing



Valid Combinations

Valid Combinations	
MD, D, P, N	8284A
MD, D, P	8284AB
	8284A-1
D	8284A-1B

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

* Military temperature range products are NPL (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

PIN DESCRIPTION			
Pin No.	Name	I/O	Description
3, 7	AEN ₁ , AEN ₂	I	Address Enable. The AEN signal is used to qualify the Bus Ready signals (RDY ₁ or RDY ₂). AEN ₁ validates RDY ₁ while AEN ₂ validates RDY ₂ . It is possible for the processor to access two Multi-Master System Busses if you use both signals. Both signals are tied LOW in non Multi-Master Systems.
4, 6	RDY ₁ , RDY ₂	I	Bus Ready. These signals are indications from a device located on the system bus that it is available or data has been received. RDY ₁ and RDY ₂ are qualified by AEN ₁ and AEN ₂ respectively.
15	ASYNC	I	Ready Synchronous Select. The ASYNC signal defines the synchronization mode of the READY logic. When ASYNC is open (internal pull-up resistor is provided) or pulled HIGH, there is one stage of READY Synchronization. When ASYNC is LOW, there are two stages of READY Synchronization.
5	READY	O	Ready. READY is the synchronized RDY signal input. After the guaranteed hold time to the processor has been met, the READY signal is cleared.
7, 16	X ₁ , X ₂	I	Crystal In. These are the input pins for the attached crystal. The crystal frequency is 3 times the desired process clock frequency.
13	F/C	I	Frequency/Crystal Select. When F/C is strapped HIGH, CLK is generated from the EFI input. When strapped LOW, the F/C allows the processor clock to be generated by the crystal.
14	EFI	I	External Frequency. Used in conjunction with a HIGH signal on F/C, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
8	CLK	O	Processor Clock. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (including bipolar support chips and other MOS devices). An output HIGH of 4.5V (V _{CC} = 5V) is provided on this pin to drive MOS devices. The output frequency of CLK is 1/3 of the crystal on EFI input frequency and a 1/3 duty cycle.
2	PCLK	O	Peripheral Clock. This signal is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
12	OSC	O	Oscillator Output. This signal is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
11	RES	I	Reset In. This signal is used to generate a RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
10	RESET	O	Reset. This signal is used to reset the 8086 family processors.
1	CSYNC	I	Clock Synchronization. This signal is designed to allow multiple 8284As to be synchronized to provide clocks that are in phase. CSYNC HIGH will reset the internal counters, when CSYNC goes LOW the counters will resume counting. CSYNC needs to be externally synchronized to EFI. When used with the internal oscillator, CSYNC should be hard wired to ground.

DETAILED DESCRIPTION

OSCILLATOR

The oscillator circuit of the 8284A is designed primarily for use with a fundamental mode, series resonant crystal from which the operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X₁ and X₂ are the two crystal input crystal connections. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Two 510Ω series resistors are optional for systems which have a V_{CC} ramp time greater than (or equal to) 1V/ms and/or inherent board capacitance between X₁ or X₂ exceeding 10pF. This capacitance value should not include the 8284A's pin capacitance. By limiting the stray capacitance to less than 10pF on X₁ or X₂, the deviation from the desired fundamental frequency is minimized.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input, (CSYNC), allows the output clock to be synchronized with an external event (such as another 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284A (see Figure 1). This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/C input is a strapping pin that selects either the EFI input or the crystal oscillator as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 8086 or 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

RESET LOGIC

Reset logic for the 8284A is provided by a Schmitt trigger input (RES) and a synchronizing flip-flop to generate the reset timing.

The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY₁, RDY₂) are provided to accommodate two Multi-Master system busses. Each input has a qualifier (AEN₁ and AEN₂, respectively). The AEN signals validate their respective RDY signals. If a Multi-Master system is not being used the AEN pin should be tied LOW.

To assure RDY setup and hold times are met, synchronization is required for all asynchronous active going edges of either RDY input. Inactive-going edges of RDY (in normally ready systems) do not require synchronization, but must satisfy RDY setup and hold as a matter of proper system design.

The two modes of RDY synchronization operation are defined by the ASYNC input.

When ASYNC is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK; after which time the READY output will go active (HIGH). Negative-going asynchro-

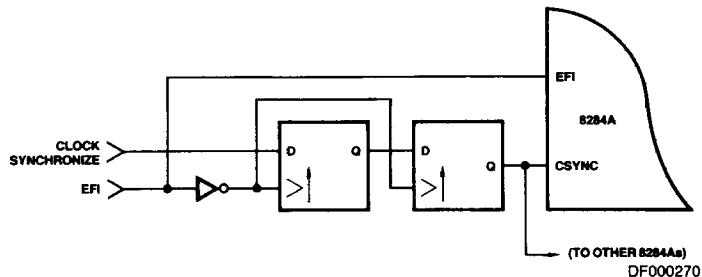
nous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous, (normally not ready), devices in the system which cannot be guaranteed by design to meet the required RDY setup timing t_{R1VCL} on each bus cycle.

When ASYNC is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. RDY inputs are

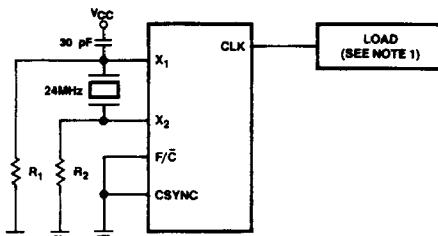
synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

ASYNC can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 1. CSYNC Synchronization

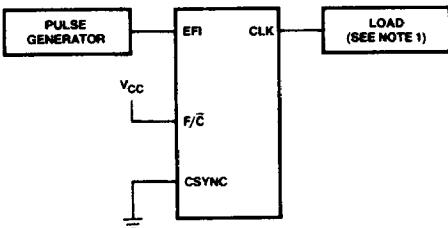


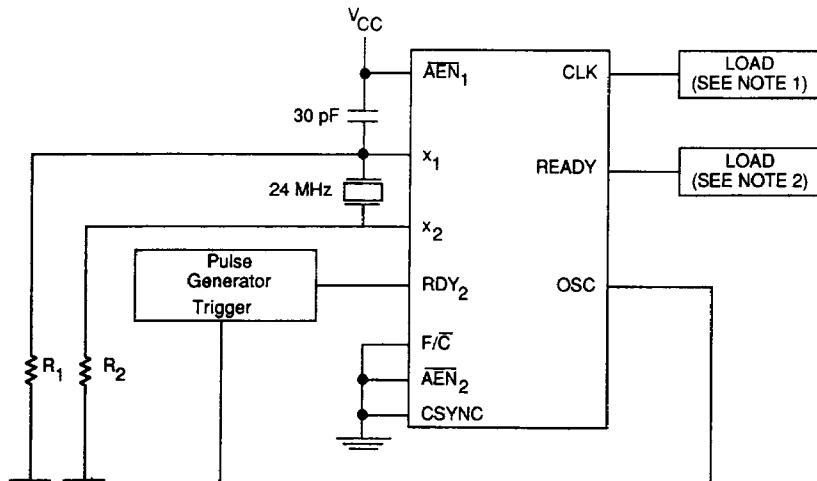
CLOCK HIGH AND LOW TIME (USING X_1 , X_2)



$$R_1 = R_2 = 510\Omega$$

CLOCK HIGH AND LOW TIME (USING EFI)

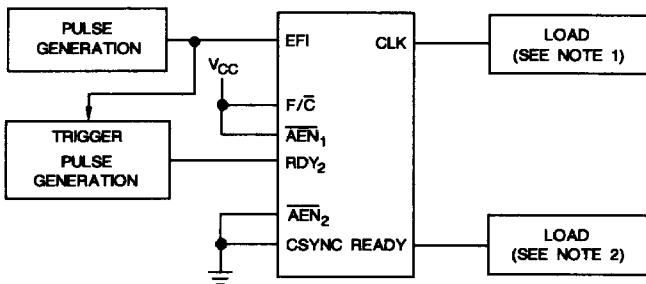


READY TO CLOCK (USING X₁, X₂)

AF004680

$$R_1 = R_2 = 510\Omega.$$

READY TO CLOCK (USING EFI)



AF000611

- Notes: 1. C_L = 100pF
 2. C_L = 30pF

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Powers Applied	
(COML, A-1)	0°C to +70°C
(MIL)	-55°C to +125°C
All Output and Supply Voltages	-0.5V to +7.0V
All Input Voltage.....	-1.0V to +5.5V
Power Dissipation	1W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

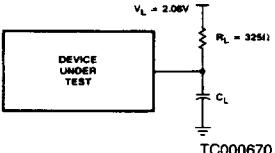
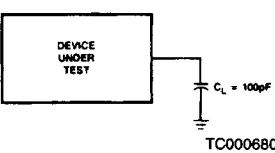
Commercial (C) Devices	
Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V
Military (M) Devices	
Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Description	Test Conditions	Min	Max	Units
I _F	Forward Input Current (ASYNC)	V _F = 0.45V		-1.3	mA
	Other Inputs	V _F = 0.45V		-0.5	
I _R	Reverse Input Current (ASYNC)	V _R = V _{CC}		50	μA
	Other Inputs	V _R = 5.25V		50	
V _C	Input Forward Clamp Voltage	I _C = -5mA		-1.0	Volts
I _{CC}	Power Supply Current			162	mA
V _{IL}	Input LOW Voltage			0.8	Volts
V _{IH}	Input HIGH Voltage		2.0		Volts
V _{IHR}	Reset Input HIGH Voltage		2.6		Volts
V _{OL}	Output LOW Voltage	5mA		0.45	Volts
V _{OH}	Output HIGH Voltage CLK	-1mA	4.0	2.5	Volts
	Other Outputs	-1mA	2.4		
V _{IHR} -V _{ILR}	RES Input Hysteresis (Note 1)		0.25		Volts

Note 1. This specification is provided for reference only.

SWITCHING TESTING CIRCUIT (CLK, READY)	SWITCHING TESTING CIRCUIT (CLK, READY)	SWITCHING TESTING WAVEFORM (Input, output)
 <p>VL = 2.08V RL = 325Ω CL TC000670</p>	 <p>DEVICE UNDER TEST CL = 100pF TC000680</p>	 <p>2.4 1.5 — TEST POINTS — 1.5 0.45 WF001870</p>
$C_L = 100\text{pF}$ for CLK $C_L = 30\text{pF}$ for READY	$C_L = 100\text{pF}$	AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 1.5V for both a logic "1" and "0".

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

TIMING REQUIREMENTS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
tEHEL	External Frequency HIGH Time	90% - 90% V _{IN}	13			ns
tELEH	External Frequency LOW Time	10% - 10% V _{IN}	13			ns
tEEL	EFI Period	MIL (Note 1) COM'L, A-1	tEHEL + tELEH + δ 33			ns
	XTAL Frequency		12		25	MHz
tR1VCL	RDY ₁ , RDY ₂ Active Setup to CLK	ASYNC = HIGH	35			ns
tR1VCH	RDY ₁ , RDY ₂ Active Setup to CLK	ASYNC = LOW	35			ns
tR1VCL	RDY ₁ , RDY ₂ Inactive Setup to CLK		35			ns
tCLR1X	RDY ₁ , RDY ₂ Hold to CLK		0			ns
tAYVCL	ASYNC Setup to CLK		50			ns
tCLAYX	ASYNC Hold to CLK		0			ns
tA1VR1V	AEN ₁ , AEN ₂ Setup to RDY ₁ , RDY ₂		15			ns
tCLA1X	AEN ₁ , AEN ₂ Hold to CLK		0			ns
tYHEH	CSYNC Setup to EFI		20			ns
tEHYL	CSYNC Hold to EFI	MIL COM'L, A-1	20 10			ns
tYHYL	CSYNC Width		2 · tEEL			ns
tI1HCL	RES Setup to CLK	(Note 2)	65			ns
tCLI1H	RES Hold to CLK	(Note 2)	20			ns
tILIH	Input Rise Time	From 0.8V to 2.0V			20	ns
tILIH	Input Fall Time	From 2.0V to 0.8V			12	ns

TIMING RESPONSES

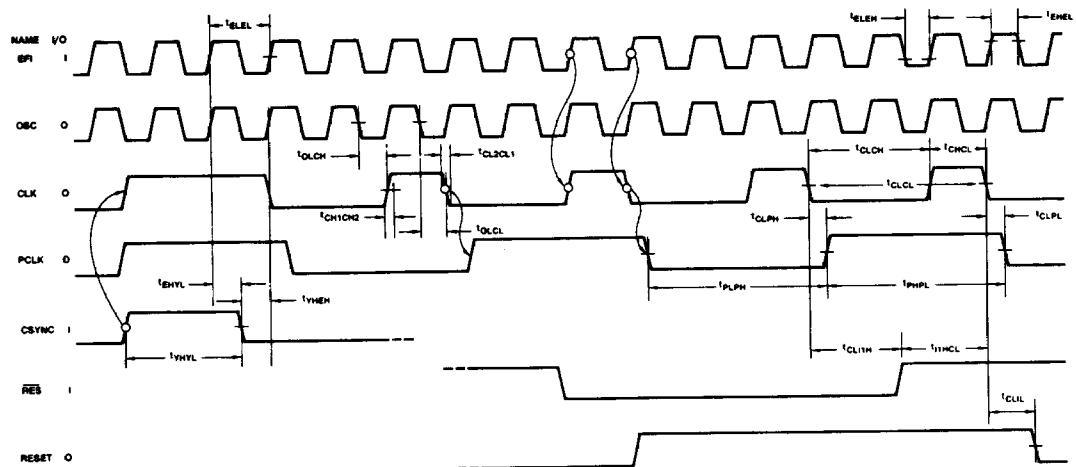
Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{CLCL}	CLK Cycle Period	MIL, COM'L	125			ns
		A-1	100			
t_{CHCL}	CLK HIGH Time	MIL, COM'L	(1/3 t_{CLCL}) + 2			ns
		A-1	39			
t_{CLCH}	CLK LOW Time	MIL, COM'L	(2/3 t_{CLCL}) - 15			ns
		A-1	53			
t_{CH1CH2}	CLK Rise or Fall Time	1.0V to 3.5V			10	ns
t_{CL2CL1}						
t_{PHPL}	PCLK HIGH Time		$t_{CLCL} - 20$			ns
t_{PLPH}	PCLK LOW Time		$t_{CLCL} - 20$			ns
t_{RYLCL}	Ready Inactive to CLK (See Note 4)		-8			ns
t_{RYHCH}	Ready Active to CLK (See Note 3)	MIL, COM'L	(2/3 t_{CLCL}) - 15			ns
		A-1	53			
t_{CLIL}	CLK to Reset Delay				40	ns
t_{CLPH}	CLK to PCLK HIGH Delay				22	ns
t_{CLPL}	CLK to PCLK LOW Delay				22	ns
t_{OLCH}	OSC to CLK HIGH Delay		-5		22	ns
t_{OLCL}	OSC to CLK LOW Delay		2		35	ns
t_{OLOH}	Output Rise Time (except CLK)	From 0.8V to 2.0V			20	ns
t_{OLOH}	Output Fall Time (except CLK)	From 2.0V to 0.8V			12	ns

Notes:

1. δ = E/FI rise (5ns max) + E/FI fall (5ns max).
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T_3 and T_W states.
4. Applies only to T_2 states.

SWITCHING WAVEFORMS

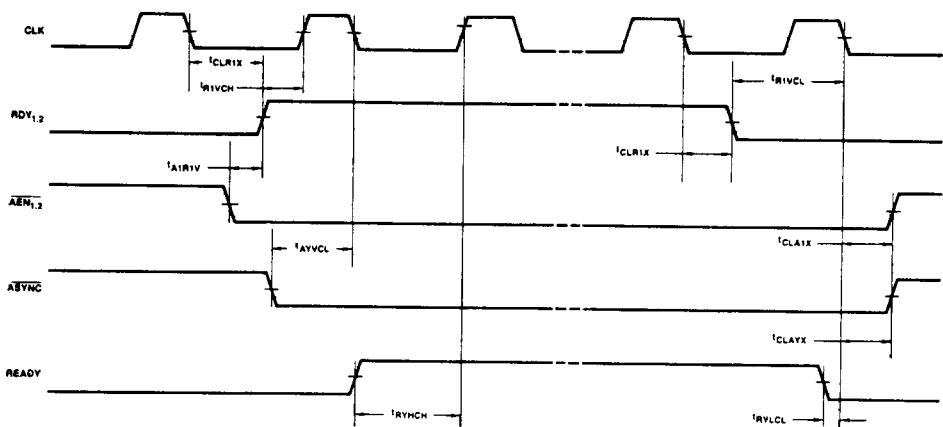
CLOCKS AND RESET SIGNALS



WF002530

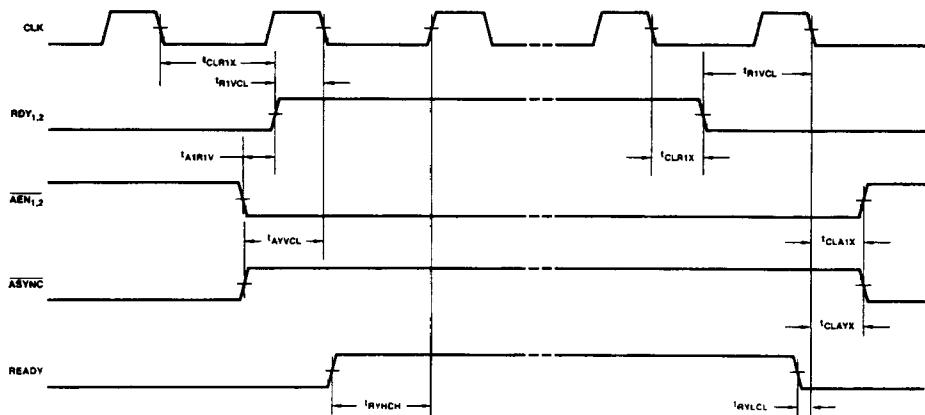
Note: All timing requirements are made at 1.5 volts, unless otherwise noted.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



WF002520

READY SIGNALS (FOR SYNCHRONOUS DEVICES)



WF002510

HM6116 Series

Maintenance Only

2048-word x 8-bit High Speed CMOS Static RAM

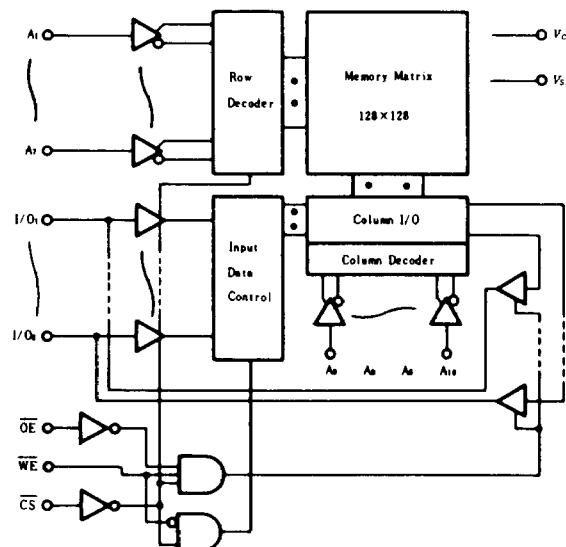
■ FEATURES

- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
 - Standby: 100 μ W (typ.)
 - Operation: 10 μ W (typ.) (L-version)
 - 200mW (typ.)
 - 175mW (typ.) (L-version)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6116P-2	120ns	600mil 24pin Plastic DIP
HM6116P-3	150ns	
HM6116P-4	200ns	
HM6116LP-2	120 ns	24pin Plastic SOP
HM6116LP-3	150 ns	
HM6116LP-4	200ns	
HM6116FP-2	120 ns	24pin Plastic SOP
HM6116FP-3	150 ns	
HM6116FP-4	200 ns	
HM6116LFP-2	120 ns	24pin Plastic SOP
HM6116LFP-3	150 ns	
HM6116LFP-4	200 ns	

■ FUNCTIONAL BLOCK DIAGRAM



HM6116P Series



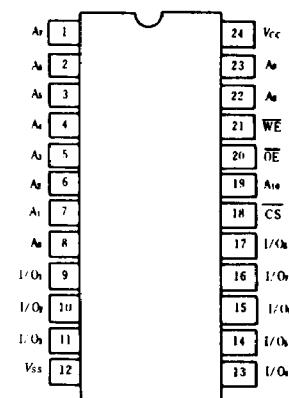
(DP-24)

HM6116FP Series



(FP-24D)

■ PIN ARRANGEMENT



Note) This device is not available for new application.

 HITACHI

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 ^{*1} to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bst}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. -3.5V for pulse width $\leq 50\text{ns}$

■TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	x	x	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-0.3 ^{*1}	—	0.8	V

Note) *1. -3.0V for pulse width $\leq 50\text{ns}$.

■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$, $T_a=0$ to +70°C)

Item	Symbol	Test Conditions	HM6116-2			HM6116-3/-4			Unit
			min	typ ^{*1}	max	min	typ ^{*1}	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{IN}=V_{SS}$ to V_{CC}	—	—	10	—	—	10	μA
			—	—	2 ^{*3}	—	—	2 ^{*3}	
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	—	—	10	—	—	10	μA
			—	—	2 ^{*3}	—	—	2 ^{*3}	
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0\text{mA}$	—	40	80	—	35	70	mA
			—	35 ^{*3}	70 ^{*3}	—	30 ^{*3}	60 ^{*3}	
Average Operating Current	I_{CC2}	Min. cycle, duty=100% $I_{I/O}=0\text{mA}$	—	35 ^{*3}	70 ^{*3}	—	30 ^{*3}	60 ^{*3}	mA
			—	40	80	—	35	70	
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
			—	4 ^{*3}	12 ^{*3}	—	4 ^{*3}	12 ^{*3}	
Output Voltage	V_{OL}	$\overline{CS} \geq V_{CC}-0.2\text{V}$, $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN}$	—	0.02	2	—	0.02	2	μA
			—	2 ^{*3}	50 ^{*3}	—	2 ^{*3}	50 ^{*3}	
	V_{OH}	$I_{OL}=4\text{mA}$	—	—	0.4	—	—	—	V
			—	—	—	—	—	0.4	
			2.4	—	—	2.4	—	—	V

Notes) *1. $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

*2. Reference Only

*3. This characteristics are guaranteed only for L-version.



CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{is}	$V_{i,0}=0\text{V}$	3	5	pF
Input/Output Capacitance	C_{io}	$V_{i,o}=0\text{V}$	5	7	pF

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($V_{CC}=5\text{V}\pm10\%$, $T_a=0$ to $+70^\circ\text{C}$)**AC TEST CONDITIONS**

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

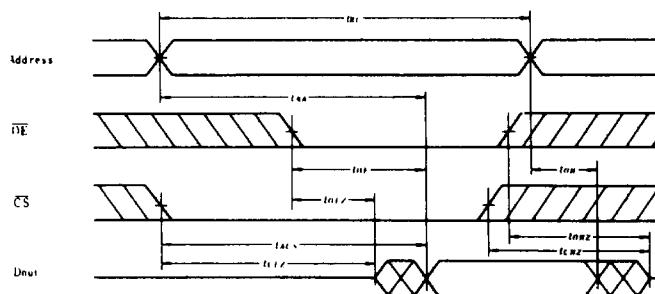
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

READ CYCLE

Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{ac}	120	—	150	—	200	—	ns
Address Access Time	t_{aa}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{acs}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{clz}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{oe}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{olz}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{chz}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{onz}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{oh}	10	—	15	—	15	—	ns

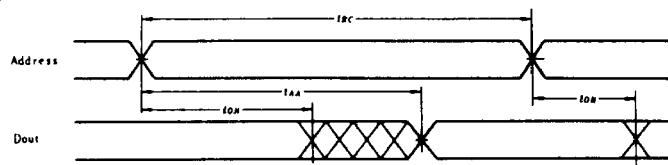
WRITE CYCLE

Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{wc}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{cw}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{aw}	105	—	120	—	140	—	ns
Address Set Up Time	t_{as}	20	—	20	—	20	—	ns
Write Pulse Width	t_{wp}	70	—	90	—	120	—	ns
Write Recovery Time	t_{wr}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{onz}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{wz}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{ow}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{oh}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{ow}	5	—	10	—	10	—	ns

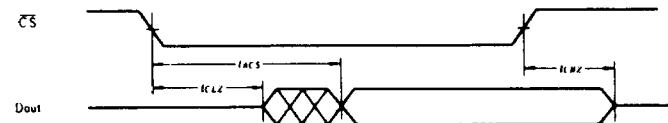
TIMING WAVEFORM**READ CYCLE (1)⁽¹⁾**

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● READ CYCLE (2) (1)(2)(4)

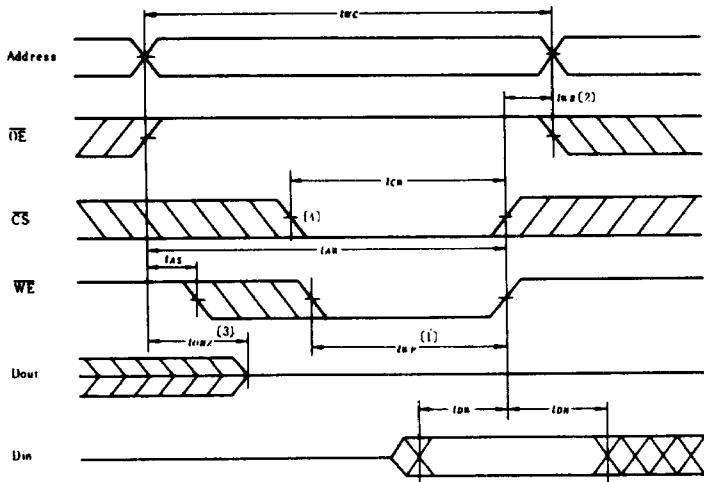


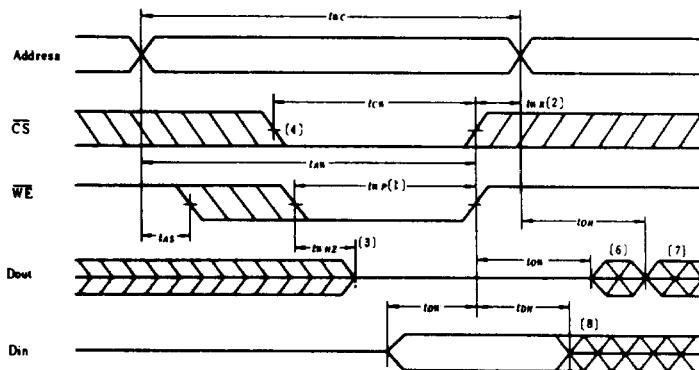
● READ CYCLE (3) (1)(3)(4)



- NOTES:
1. WE is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE (1)



● WRITE CYCLE (2)⁽⁵⁾

- NOTES:**
1. A write occurs during the overlap (t_{WP}) of a low CS and a low WE.
 2. t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
 5. OE is continuously low. ($OE = V_{IL}$)
 6. Dout is the same phase of write data of this write cycle.
 7. Dout is the read data of next address.
 8. If CS is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ C$)

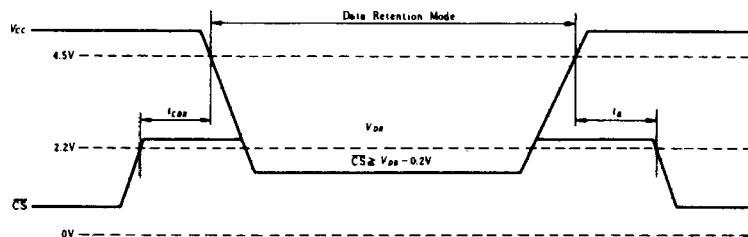
This characteristics are guaranteed only for L-version.

Item	Symbol	Test Conditions	min	typ	max	Unit
V _{cc} for Data Retention	V_{DR}	$CS \geq V_{cc} - 0.2V, V_{il} \geq V_{cc} - 0.2V$ or $V_{il} \leq 0.2V$	2.0	—	—	V
Data Retention Current	$I_{CCR}^{(1)}$	$V_{cc} = 3.0V, CS \geq 2.8V, V_{ih} \geq 2.8V$ or $OV \leq V_{in} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		$t_{AC}^{(2)}$	—	—	ns

Notes) *1. 10/ μA max at $T_a = 0^\circ C$ to $+40^\circ C$, V_{il} min = $-0.3V$

*2. t_{AC} = Read Cycle Time.

● Low Vcc Data Retention Waveform



PHILIPS**Lighting**

Ecofit Ledtubes T8

LEDtube 1200mm 16W 765 T8 AP C G

Upgrade to efficient, long-lasting LED tubes with the Ecofit LED tubes. Ecofit LED tubes are a fast and easy way to replace your old fluorescent tubes with modern, efficient LED technology. Good quality of light with a natural lighting effect for use in general lighting applications with low initial investment – an environmentally friendly solution.

Product data

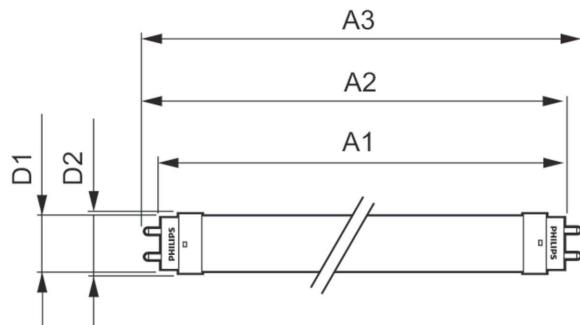
General information	
Cap-Base	G13 [Medium Bi-Pin Fluorescent]
EU RoHS compliant	Yes
Nominal Lifetime (Nom)	15000 h
Switching Cycle	50000
Light technical	
Color Code	765 [CCT of 6500K]
Beam Angle (Nom)	240 °
Luminous Flux (Nom)	1600 lm
Color Designation	Cool Daylight
Correlated Color Temperature (Nom)	6500 K
Luminous Efficacy (rated) (Nom)	100.00 lm/W
Color Consistency	<7
Color Rendering Index (Nom)	73
LLMF At End Of Nominal Lifetime (Nom)	70 %
Operating and electrical	
Input Frequency	50 to 60 Hz
Power (Nom)	16 W
Starting Time (Nom)	0.5 s
Warm Up Time to 60% Light (Nom)	0.5 s
Power Factor (Nom)	
Power Factor (Nom)	0.5
Voltage (Nom)	
Voltage (Nom)	220-240 V
Temperature	
T-Ambient (Max)	45 °C
T-Ambient (Min)	-20 °C
T-Storage (Range)	-40 °C to 65 °C
T-Storage (Max)	65 °C
T-Storage (Min)	-40 °C
T-Case Maximum (Nom)	60 °C
Controls and dimming	
Dimmable	No
Mechanical and housing	
Product Length	1200 mm
Bulb Shape	Tube, double-ended
Approval and application	
Energy Saving Product	Yes
Suitable For Accent Lighting	No
Approval Marks	RoHS compliance KEMA Keur certificate

Ecofit Ledtubes T8

Energy Consumption kWh/1000 h	16 kWh
Application conditions	
Ambient temperature range	-20 °C to 45 °C
Product data	
Full product code	871869652503600
Order product name	LEDtube 1200mm 16W 765 T8 AP C G
EAN/UPC - Product	8718696525036

Order code	929001184608
Numerator - Quantity Per Pack	1
Local code description	LEDtube Glass 1200mm 16W 765 220V T8 AP
Numerator - Packs per outer box	10
Material Nr. (12NC)	929001184608
Net Weight (Piece)	0.172 kg

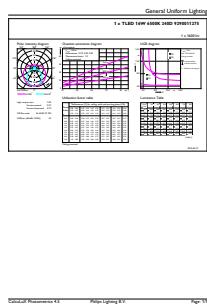
Dimensional drawing



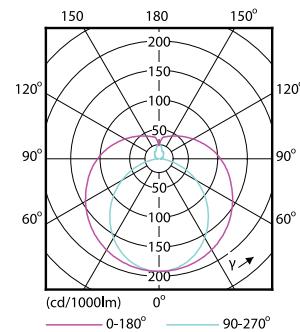
LEDtube 1200mm 16W 765 T8 AP C G

Product	D1	D2	A1	A2	A3	C	D
LEDtube 1200mm 16W 765 T8 AP C G	25.68	28 mm	1198	1205	1212	1212	27.8

Photometric data



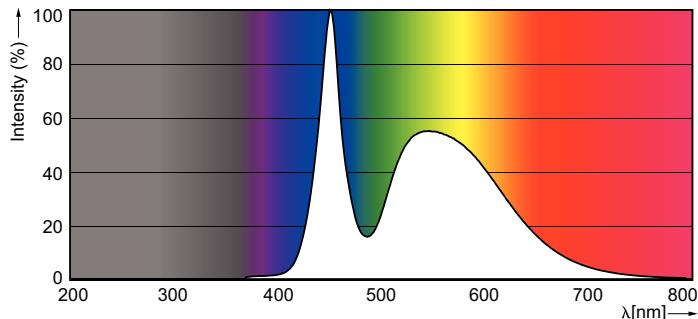
LEDtube 1200mm 16W 765 T8 CN I G



LEDtube 1200mm 16W 740 T8 CN I G

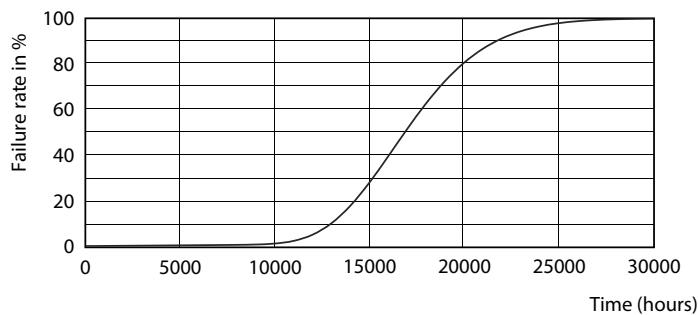
Ecofit Ledtubes T8

Photometric data

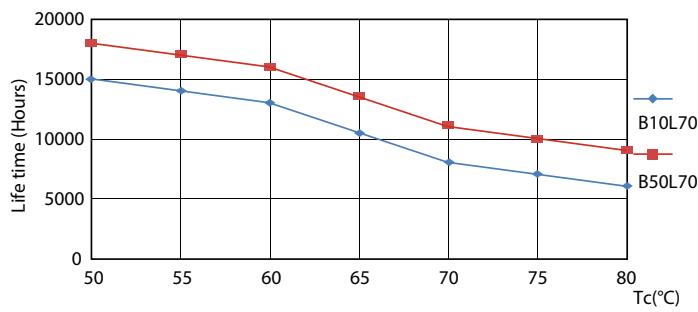
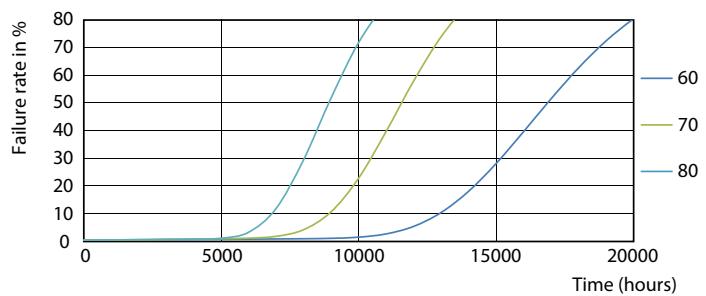


LEDtube 1200mm 16W G13 T8 765 1600lm AP C G

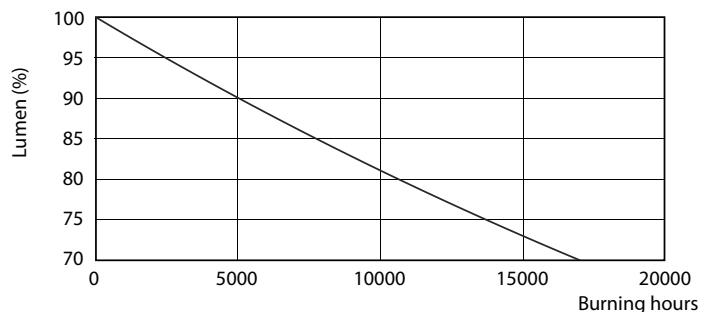
Lifetime



LEDtube 16W G13 740 T8 AP I G

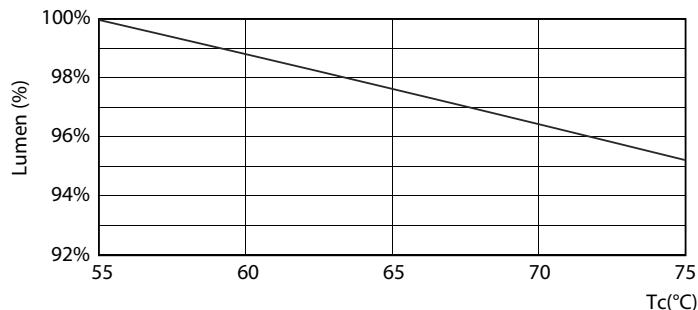


LEDtube 16W G13 740 T8 AP I G



Ecofit Ledtubes T8

Lifetime



LEDtube 16W G13 740 T8 AP I G



80130/80130-2

iAPX 86/30, 88/30, 186/30, 188/30

iRMX 86 OPERATING SYSTEM PROCESSORS

- High-Performance 2-Chip Data Processors Containing Operating System Primitives
- Standard iAPX 86/10, 88/10 Instruction Set Plus Task Management, Interrupt Management, Message Passing, Synchronization and Memory Allocation Primitives
- Fully Extendable To and Compatible With iRMX® 86
- Supports Five Operating System Data Types: Jobs, Tasks, Segments, Mailboxes, Regions
- 35 Operating System Primitives
- Built-In Operating System Timers and Interrupt Control Logic Expandable From 8 to 57 Interrupts
- 8086/80150/80150-2/8088/80186/80188 Compatible At Up To 8 MHz Without Wait States
- MULTIBUS® System Compatible Interface

The Intel iAPX 86/30 and iAPX 88/30 are two-chip microprocessors offering general-purpose CPU (8086) instructions combined with real-time operating system support. They provide a foundation for multiprogramming and multitasking applications. The iAPX 86/30 consists of an iAPX 86/10 (16-bit 8086 CPU) and an Operating System Firmware (OSF) component (80130). The 88/30 consists of the OSF and an iAPX 88/10 (8-bit 8088 CPU). (80186 or 80188 CPUs may be used in place of the 8086 or 8088.)

Both components of the 86/30 and 88/30 are implemented in N-channel, depletion-load, silicon-gate technology (HMOS) and are housed in 40-pin packages. The 86/30 and 88/30 provide all the functions of the iAPX 86/10, 88/10 processors plus 35 operating system primitives, hardware support for eight interrupts, a system timer, a delay timer and a baud rate generator.

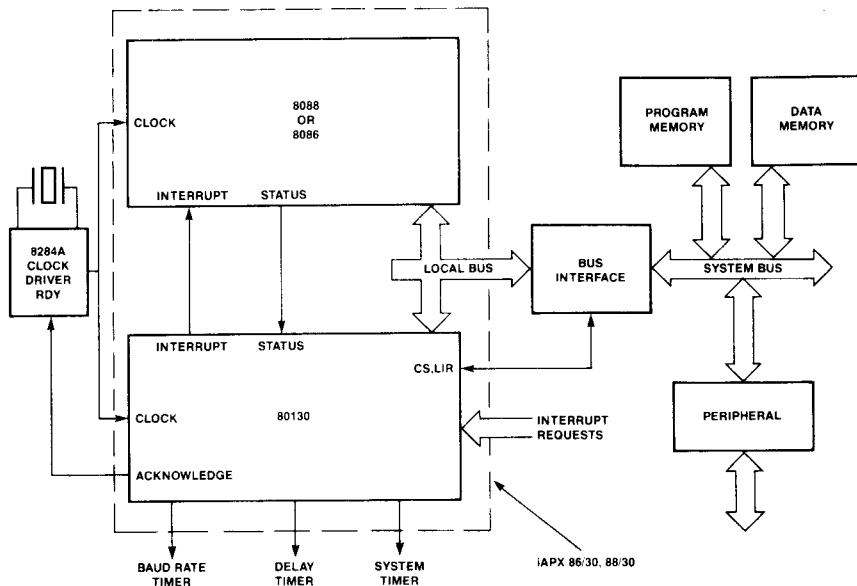


Figure 1. iAPX 86/30, 88/30 Block Diagram

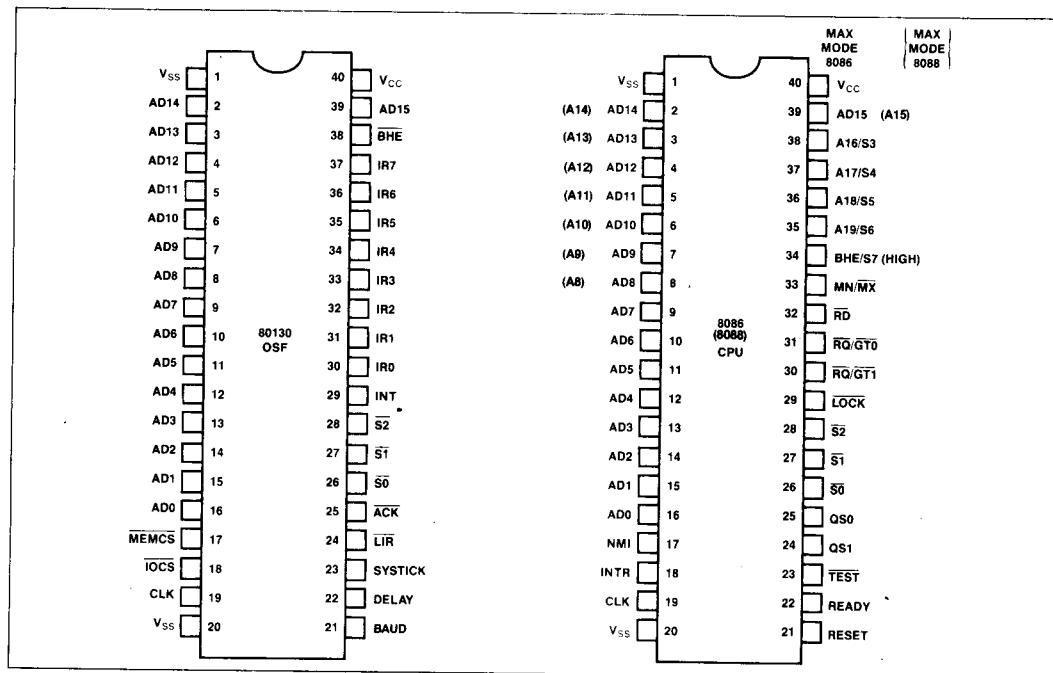


Figure 2. iAPX 86/30, 88/30 Pin Configuration

Table 1. 80130 Pin Description

Symbol	Type	Name and Function																																
AD ₁₅ -AD ₀	I/O	Address Data: These pins constitute the time multiplexed memory address (T ₁) and data (T ₂ , T ₃ , T _W , T ₄) bus. These lines are active HIGH. The address presented during T ₁ of a bus cycle will be latched internally and interpreted as an 80130 internal address if MEMCS or IOCS is active for the invoked primitives. The 80130 pins float whenever it is not chip selected, and drive these pins only during T ₂ -T ₄ of a read cycle and T ₁ of an INTA cycle.																																
BHE/S ₇		Bus High Enable: The 80130 uses the BHE signal from the processor to determine whether to respond with data on the upper or lower data pins, or both. The signal is active LOW. BHE is latched by the 80130 on the trailing edge of ALE. It controls the 80130 output data as shown. <table> <thead> <tr> <th>BHE</th> <th>A₀</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Word on AD₁₅-AD₀</td> </tr> <tr> <td>0</td> <td>1</td> <td>Upper byte on AD₁₅-AD₈</td> </tr> <tr> <td>1</td> <td>0</td> <td>Lower byte on AD₇-AD₀</td> </tr> <tr> <td>1</td> <td>1</td> <td>Upper byte on AD₇-AD₀</td> </tr> </tbody> </table>	BHE	A ₀		0	0	Word on AD ₁₅ -AD ₀	0	1	Upper byte on AD ₁₅ -AD ₈	1	0	Lower byte on AD ₇ -AD ₀	1	1	Upper byte on AD ₇ -AD ₀																	
BHE	A ₀																																	
0	0	Word on AD ₁₅ -AD ₀																																
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1	0	Lower byte on AD ₇ -AD ₀																																
1	1	Upper byte on AD ₇ -AD ₀																																
S ₂ , S ₁ , S ₀	I	Status: For the 80130, the status pins are used as inputs only. 80130 encoding follows: <table> <thead> <tr> <th>S₂</th> <th>S₁</th> <th>S₀</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>INTA</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>IORD</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>IOWR</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Passive</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Instruction fetch</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>MEMRD</td> </tr> <tr> <td>1</td> <td>1</td> <td>X</td> <td>Passive</td> </tr> </tbody> </table>	S ₂	S ₁	S ₀		0	0	0	INTA	0	0	1	IORD	0	1	0	IOWR	0	1	1	Passive	1	0	0	Instruction fetch	1	0	1	MEMRD	1	1	X	Passive
S ₂	S ₁	S ₀																																
0	0	0	INTA																															
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0	1	1	Passive																															
1	0	0	Instruction fetch																															
1	0	1	MEMRD																															
1	1	X	Passive																															

Table 1. 80130 Pin Description (Continued)

Symbol	Type	Name and Function																																																						
CLK	I	Clock: The system clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. The 80130 uses the system clock as an input to the SYSTICK and BAUD timers and to synchronize operation with the host CPU.																																																						
INT	O	Interrupt: INT is HIGH whenever a valid interrupt request is asserted. It is normally used to interrupt the CPU by connecting it to INTR.																																																						
IR ₇ -IR ₀	I	Interrupt Requests: An interrupt request can be generated by raising an IR input (LOW to HIGH) and holding it HIGH until it is acknowledged (Edge-Triggered Mode), or just by a HIGH level on an IR input (Level-Triggered Mode).																																																						
ACK	O	Acknowledge: This line is LOW whenever an 80130 resource is being accessed. It is also LOW during the first INTA cycle and second INTA cycle if the 80130 is supplying the interrupt vector information. This signal can be used as a bus ready acknowledgement and/or bus transceiver control.																																																						
MEMCS	I	Memory Chip Select: This input must be driven LOW when a kernel primitive is being fetched by the CPU. AD ₁₃ -AD ₀ are used to select the instruction.																																																						
IOCS	I	Input/Output Chip Select: When this input is low, during an IORD or IOWR cycle, the 80130's kernel primitives are accessing the appropriate peripheral function as specified by the following table:																																																						
		<table> <thead> <tr> <th>BHE</th> <th>A₃</th> <th>A₂</th> <th>A₁</th> <th>A₀</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>Passive</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>Passive</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>X</td> <td>X</td> <td>Passive</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>X</td> <td>0</td> <td>Interrupt Controller</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Systick Timer</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>Delay Counter</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>Baud Rate Timer</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Timer Control</td> </tr> </tbody> </table>	BHE	A ₃	A ₂	A ₁	A ₀		0	X	X	X	X	Passive	X	X	X	X	1	Passive	X	0	1	X	X	Passive	1	0	0	X	0	Interrupt Controller	1	1	0	0	0	Systick Timer	1	1	0	1	0	Delay Counter	1	1	1	0	0	Baud Rate Timer	1	1	1	1	0	Timer Control
BHE	A ₃	A ₂	A ₁	A ₀																																																				
0	X	X	X	X	Passive																																																			
X	X	X	X	1	Passive																																																			
X	0	1	X	X	Passive																																																			
1	0	0	X	0	Interrupt Controller																																																			
1	1	0	0	0	Systick Timer																																																			
1	1	0	1	0	Delay Counter																																																			
1	1	1	0	0	Baud Rate Timer																																																			
1	1	1	1	0	Timer Control																																																			
LIR	O	Local Bus Interrupt Request: This signal is LOW when the interrupt request is for a non-slave input or slave input programmed as being a local slave.																																																						
V _{CC}		Power: V _{CC} is the +5V supply pin.																																																						
V _{SS}		Ground: V _{SS} is the ground pin.																																																						
SYSTICK	O	System Clock Tick: Timer 0 Output. Operating System Clock Reference. SYSTICK is normally wired to IR2 to implement operating system timing interrupt.																																																						
DELAY	O	DELAY Timer: Output of timer 1. Reserved by Intel Corporation for future use.																																																						
BAUD	O	Baud Rate Generator: 8254 Mode 3 compatible output. Output of 80130 Timer 2.																																																						

FUNCTIONAL DESCRIPTION

The increased performance and memory space of iAPX 86/10 and 88/10 microprocessors have proven sufficient to handle most of today's single-task or single-device control applications with performance to spare, and have led to the increased use of these microprocessors to control *multiple* tasks or devices in real-time. This trend has created a new challenge to designers—development of real-time, multitasking application systems and software. Examples of such systems include control systems that monitor and react to external events in real-time, multifunction desktop and personal computers, PABX equipment which constantly controls the telephone traffic in a multiphone office, file servers/disk subsystems controlling and coordinating multiple disks and multiple disk users, and transaction processing systems such as electronics funds transfer.

The iAPX 86/30, 88/30 Operating System Processors

The Intel iAPX 86/30, 88/30 Operating System Processors (OSPs) were developed to help solve this

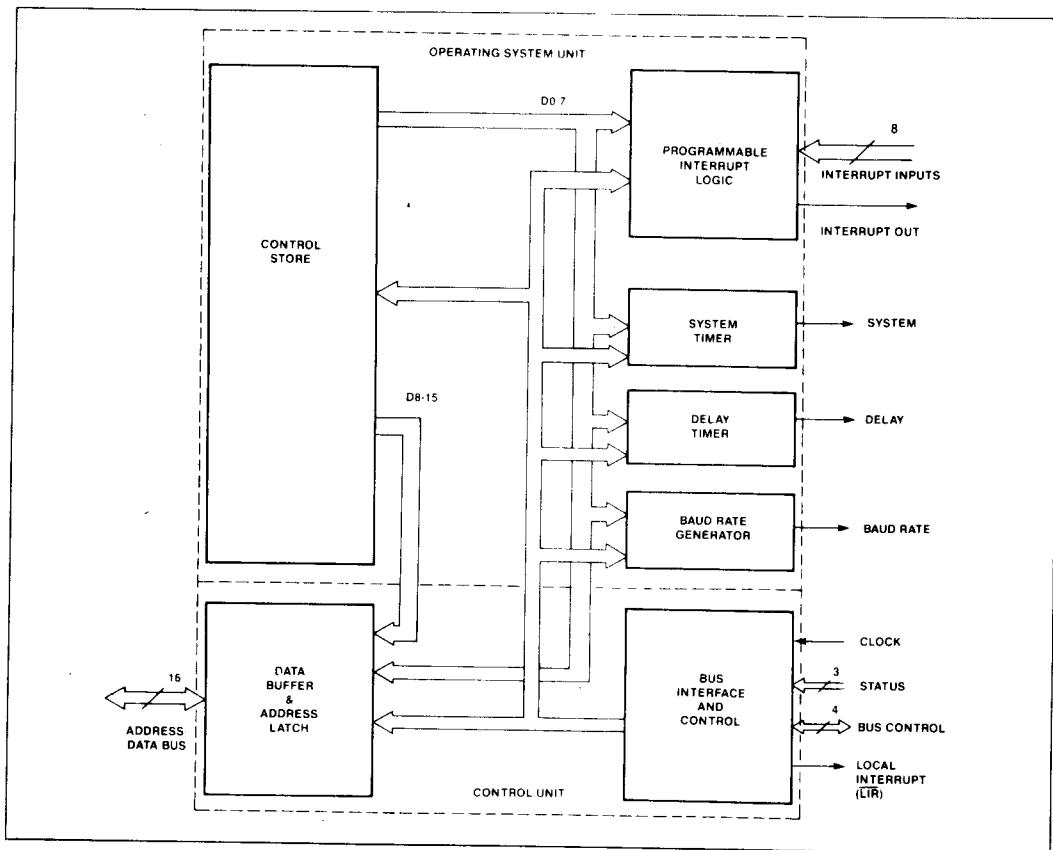


Figure 3. OSF Internal Block Diagram

problem. Their goal is to simplify the design of multitasking application systems by providing a well-defined, fully debugged set of operating system primitives implemented directly in the hardware, thereby removing the burden of designing multitasking operating system primitives from the application programmer.

Both the 86/30 and the 88/30 OSPs are two-chip sets consisting of a main processor, an 8086 or 8088 CPU, and the Intel 80130, Operating System Firmware component (OSF) (see Figure 1). The 80130 provides a set of multitasking kernel primitives, kernel control storage, and the additional support hardware, including system timers and interrupt control, required by these primitives. From the application programmer's viewpoint, the OSF extends the base iAPX 86, 88 architecture by providing 35 operating system primitive instructions, and supporting five new system data types, making the OSF a logical and

easy-to-use architectural extension to iAPX 86, 88 system designs.

The OSP Approach

The OSP system data types (SDTs) and primitive instructions allocate, manage and share low-level processor resources in an efficient manner. For example, the OSP implements task context management (managing a task state image consisting of both hardware register set and software control information) for either the basic 86/10 context or the extended 86/20 (8086+8087) numerics context. The OSP manages the entire task state image both while the task is actively executing and while it is inactive. Tasks can be created, put to sleep for specified periods, suspended, executed to perform their functions, and dynamically deleted when their functions are complete.

The Operating System Processors support event-oriented systems designs. Each event may be processed by an individual responding task or along with other closely related events in a common task. External events and interrupts are processed by the OSP interrupt handler primitives using its built-in interrupt controller subsystem as they occur in real-time. The multiple tasks and the multiple events are coordinated by the OSP integral scheduler whose preemptive, priority-based scheduling algorithm and system timers organize and monitor the processing of every task to guarantee that events are processed as they occur in order of relative importance. The 86/30 also provides primitives for intertask communication (by mailboxes) and for mutual exclusion (by regions), essential functions for multitasking applications.

Programming Language Support

Programs for the OSP can be written in ASM 86/88 or PL/M 86/88, Intel's standard system languages for iAPX 86,88 systems.

The Operating System Processor Support Package (iOSP 86) provides an interface library for application programs written in any model of PL/M-86. This library also provides 80130 configuration and initialization support as well as complete user documentation.

OSF PROGRAMMING INTERFACE

The OSF provides 35 operating system kernel primitives which implement multitasking, interrupt management, free memory management, intertask communication and synchronization. Table 4 shows each primitive, and Table 5 gives the execution performance of typical primitives.

OSP primitives are executed by a combination of CPU and OSF (80130) activity. When an OSP primitive is called by an application program task, the iAPX CPU registers and stacks are used to perform the appropriate functions and relay the results to the application programs.

OSP Primitive Calling Sequences

A standard, stack-based, calling sequence is used to invoke the OSF primitives. Before a primitive is called, its operand parameters must be pushed on the task stack. The SI register is loaded with the offset of the last parameter on the stack. The entry code for the primitive is loaded into AX. The primitive invocation call is made with a CPU software interrupt

(Table 4). A representative ASM86 sequence for calling a primitive is shown in Figure 4. In PL/M the OSP programmer uses a call to invoke the primitive.

```

SAMPLE ASSEMBLY LANGUAGE PRIMITIVE CALL
PUSH P1          ;PUSH PARAMETER 1
PUSH P2          ;PUSH PARAMETER 2
:
:
PUSH PN          ;PUSH PARAMETER N
PUSH BP             ;STACK CALLING CONVENTION
MOV BP,SP           ;
LEA SI,SS:NUM_BYTES_PARAM 2(BP)    ;SS:SI POINTS TO FIRST
                                     ;PARAMETER ON STACK
                                     ;BX SETS PRIMITIVE ENTRY CODE
                                     ;OSF INTERRUPT
MOV AX, ENTRY CODE
INT 184             ;
                                     ;OS PRIMITIVE INVOKED
POP BP              ;POP PARAMETERS
RET NUM_BYTES_PARAM ;CX CONTAINS EXCEPTION CODES
                     ;DL CONTAINS PARAMETER NUMBER
                     ;THAT CAUSED EXCEPTION (IF
                     ;CX IS NON ZERO)
                     ;AX CONTAINS WORD RETURN VALUE
                     ;ES:BX CONTAINS POINTER
                     ;RETURN VALUE

```

Figure 4. ASM/86 OSP Calling Convention

OSP Functional Description

Each major function of the OSP is described below. These are:

- Job and Task Management
- Interrupt Management
- Free Memory Management
- Intertask Communication
- Intertask Synchronization
- Environmental Control

The system data types (or SDTs) supported by the OSP are capitalized in the description. A short description of each SDT appears in Table 2.

JOB and TASK Management

Each OSP JOB is a controlled environment in which the applications program executes and the OSF system data types reside. Each individual application program is normally a separate OSP JOB, whether it has one initial task (the minimum) or multiple tasks. JOBS partition the system memory into pools. Each memory pool provides the storage areas in which the OSP will allocate TASK state images and other system data types created by the executing TASKs, and free memory for TASK working space. The OSP supports multiple executing TASKs within a JOB by managing the resources used by each, including the CPU registers, NPX registers, stacks, the system data types, and the available free memory space pool.

When a TASK is created, the OSP allocates memory (from the free memory of its JOB environment) for the TASK's stack and data area and initializes the additional TASK attributes such as the TASK priority level and its error handler location. (As an option, the caller of CREATE TASK may assign previously defined stack and data areas to the TASK.) Task priorities are integers between 0 and 255 (the lower the priority number the higher the scheduling priority of the TASK). Generally, priorities up to 128 will be assigned to TASKs which are to process interrupts. Priorities above 128 do not cause interrupts to be disabled; these priorities (129 to 255) are appropriate for non-interrupt TASKs. If an 8087 Numerics Processor Extension is used, the error recovery interrupt level assigned to it will have a higher priority than a TASK executing on it, so that error handling is performed correctly.

EXECUTION STATUS

A TASK has an execution status or execution state. The OSP provides five execution states: RUNNING, READY, ASLEEP, SUSPENDED, and ASLEEP-SUSPENDED.

- A TASK is RUNNING if it has control of the processor.
- A TASK is READY if it is not asleep, suspended, or asleep-suspended. For a TASK to become the running (executing) TASK, it must be the highest priority TASK in the ready state.
- A TASK is ASLEEP if it is waiting for a request to be granted or a timer event to occur. A TASK may put itself into the ASLEEP state.
- A TASK is SUSPENDED if it is placed there by another TASK or if it suspends itself. A TASK may have multiple suspensions; the count of suspensions is managed by the OSP as the TASK suspension depth.
- A TASK is ASLEEP-SUSPENDED if it is both waiting and suspended.

TASK attributes, the CPU register values, and the 8087 register values (if the 8087 is configured into the application) are maintained by the OSP in the TASK state image. Each TASK will have a unique TASK state image.

SCHEDULING

The OSP schedules the processor time among the various TASKs on the basis of priority. A TASK has an execution priority relative to all other TASKs in the system, which the OSP maintains for each TASK in its TASK state image. When a TASK of higher priority than the executing TASK becomes ready to execute,

the OSP switches the control of the processor to the higher priority TASK. First, the OSP saves the outgoing (lower priority) TASK's state including CPU register values in its TASK state image. Then, it restores the CPU registers from the TASK state image of the incoming (higher priority) TASK. Finally, it causes the CPU to start or resume executing the higher priority TASK.

TASK scheduling is performed by the OSP. The OSP's priority-oriented preemptive scheduler determines which TASK executes by comparing their relative priorities. The scheduler insures that the highest priority TASK with a status of READY will execute. A TASK will continue to execute until an interrupt with a higher priority occurs, or until it requests unavailable resources, for which it is willing to wait, or until it makes specific resources available to a higher priority TASK waiting for those resources.

TASKs can become READY by receiving a message, receiving control, receiving an interrupt, or by timing out. The OSP always monitors the status of all the TASKs (and interrupts) in the system. Preemptive scheduling allows the system to be responsive to the external environment while only devoting CPU resources to TASKs with work to be performed.

TIMED WAIT

The OSP timer hardware facilities support timed waits and timeouts. Thus, in many primitives, a TASK can specify the length of time it is prepared to wait for an event to occur, for the desired resources to become available or for a message to be received at a MAILBOX. The timing interval (or System Tick) can be adjusted, with a lower limit of 1 millisecond.

APPLICATION CONTROL OF TASK EXECUTION

Programs may alter TASK execution status and priority dynamically. One TASK may suspend its own execution or the execution of another TASK for a period of time, then resume its execution later. Multiple suspensions are provided. A suspended TASK may be suspended again.

The eight OSP Job and TASK management primitives are:

CREATE JOB	Partitions system resources and creates a TASK execution environment.
CREATE TASK	Creates a TASK state image. Specifies the location of the TASK code instruction stream, its execution priority, and the other TASK attributes.

DELETE TASK	Deletes the TASK state image, removes the instruction stream from execution and deallocates stack resources. Does not delete INTERRUPT TASKS.
SUSPEND TASK	Suspends the specified TASK or, if already suspended, increments its suspension depth by one. Execute state is SUSPEND.
RESUME TASK	Decrementsthe TASK suspension depth by one. If the suspension depth is then zero, the primitive changes the task execution status to READY, or ASLEEP (if ASLEEP/SUSPENDED).
SLEEP	Places the requesting TASK in the ASLEEP state for a specified number of System Ticks. (The TICK interval can be configured down to 1 millisecond.)
SET PRIORITY	Alters the priority of a TASK.

Interrupt Management

The OSP supports up to 256 interrupt levels organized in an interrupt vector, and up to 57 external interrupt sources of which one is the NMI (Non-Maskable Interrupt). The OSP manages each interrupt level independently. The OSF INTERRUPT SUBSYSTEM provides two mechanisms for interrupt management: INTERRUPT HANDLERS and INTERRUPT TASKS. INTERRUPT HANDLERS disable all maskable interrupts and should be used only for servicing interrupts that require little processing time. Within an INTERRUPT HANDLER only certain OSF Interrupt Management primitives (DISABLE, ENTER INTERRUPT, EXIT INTERRUPT, GET LEVEL, SIGNAL INTERRUPT) and basic CPU instructions can be used, other OSP primitives cannot be. The INTERRUPT TASK approach permits all OSP primitives to be issued and masks only lower priority interrupts.

Work flow between an INTERRUPT HANDLER and an INTERRUPT TASK assigned to the same level is regulated with the SIGNAL INTERRUPT and WAIT INTERRUPT primitives. The flow is asynchronous. When an INTERRUPT HANDLER signals an INTERRUPT TASK, the INTERRUPT HANDLER becomes immediately available to process another interrupt. The number of interrupts (specified for the level) the

INTERRUPT HANDLER can queue for the INTERRUPT TASK can be limited to the value specified in the SET INTERRUPT primitive. When the INTERRUPT TASK is finished processing, it issues a WAIT INTERRUPT primitive, and is immediately ready to process the queue of interrupts that the INTERRUPT HANDLER has built with repeated SIGNAL INTERRUPT primitives while the INTERRUPT TASK was processing. If there were no interrupts at the level, the queue is empty and the INTERRUPT TASK is SUSPENDED. See the Example (Figure 5) and Figures 6 and 7.

OSP external INTERRUPT LEVELS are directly related to internal TASK scheduling priorities. The OSP maintains a single list of priorities including both tasks and INTERRUPT LEVELS. The priority of the executing TASK automatically determines which interrupts are masked. Interrupts are managed by INTERRUPT LEVEL number. The OSP supports eight levels directly and may be extended by means of slave 8259As to a total of 57.

The nine Interrupt Management OSP primitives are:

DISABLE	Disables an external INTERRUPT LEVEL.
ENABLE	Enables an external INTERRUPT LEVEL.
ENTER INTERRUPT	Gives an Interrupt Handler its own data segment, separate from the data segment of the interrupted task.
EXIT INTERRUPT	Performs an "END of INTERRUPT" operation. Used by an INTERRUPT HANDLER which does not invoke an INTERRUPT TASK. Reenables interrupts, when the INTERRUPT HANDLER gives up control.
GET LEVEL	Returns the interrupt level number of the executing INTERRUPT HANDLER.
RESET INTERRUPT	Cancels the previous assignment made to an interrupt level by SET INTERRUPT primitive request. If an INTERRUPT TASK has been assigned, it is also deleted. The interrupt level is disabled.
SET INTERRUPT	Assigns an INTERRUPT HANDLER to an interrupt level and, optionally, an INTERRUPT TASK.

```

/* CODE EXAMPLE A  INTERRUPT TASK TO KEEP TRACK OF TIME-OF-DAY
DECLARE SECONDSCOUNT BYTE,
MINUTESCOUNT BYTE,
HOURS COUNT BYTE;
TIMESTASK: PROCEDURE;
DECLARE TIMES$EXCEPT$CODE WORD;
AC$CYCLES$COUNT=0;
CALL RQSSET$INTERRUPT(AC$INTERRUPT$LEVEL, 01H),
@AC$HANDLER,0,@TIME$EXCEPT$CODE);
CALL RQSRESET$INTERRUPT(AC$INTERRUPT$LEVEL, @TIME$EXCEPT$CODE);
DO HOURS$COUNT=0 TO 23;
DO MINUTES$COUNT=0 TO 59;
DO SECONDS$COUNT=0 TO 59;
CALL RQSWAIT$INTERRUPT(AC$INTERRUPT$LEVEL,
@TIME$EXCEPT$CODE);
IF SECONDS$COUNT MOD 5=0
THEN CALL PROTECTED$CRT$OUT(BEL);
END; /* SECOND LOOP */
END; /* MINUTE LOOP */
CALL RQSRESET$INTERRUPT(AC$INTERRUPT$LEVEL, @TIME$EXCEPT$CODE);
END Timestask;

/* CODE EXAMPLE B  INTERRUPT HANDLER TO SUBDIVIDE A.C. SIGNAL BY 60. */
DECLARE AC$CYCLES$COUNT BYTE;
AC$HANDLER: PROCEDURE INTERRUPT 59;
DECLARE AC$EXCEPT$CODE WORD;
AC$CYCLES$COUNT=AC$CYCLES$COUNT +1;
IF AC$CYCLES$COUNT>=60 THEN DO;
AC$CYCLES$COUNT=0;
CALL RQSIGNAL$INTERRUPT(AC$INTERRUPT$LEVEL,@AC$EXCEPT$CODE);
END;
END AC$HANDLER;

```

Figure 5. OSP Examples

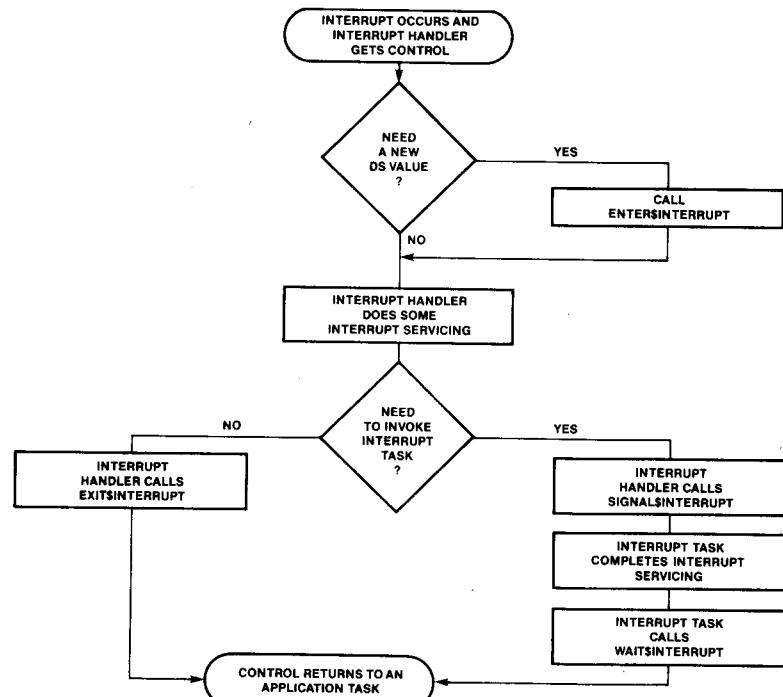


Figure 6. Interrupt Handling Flowchart

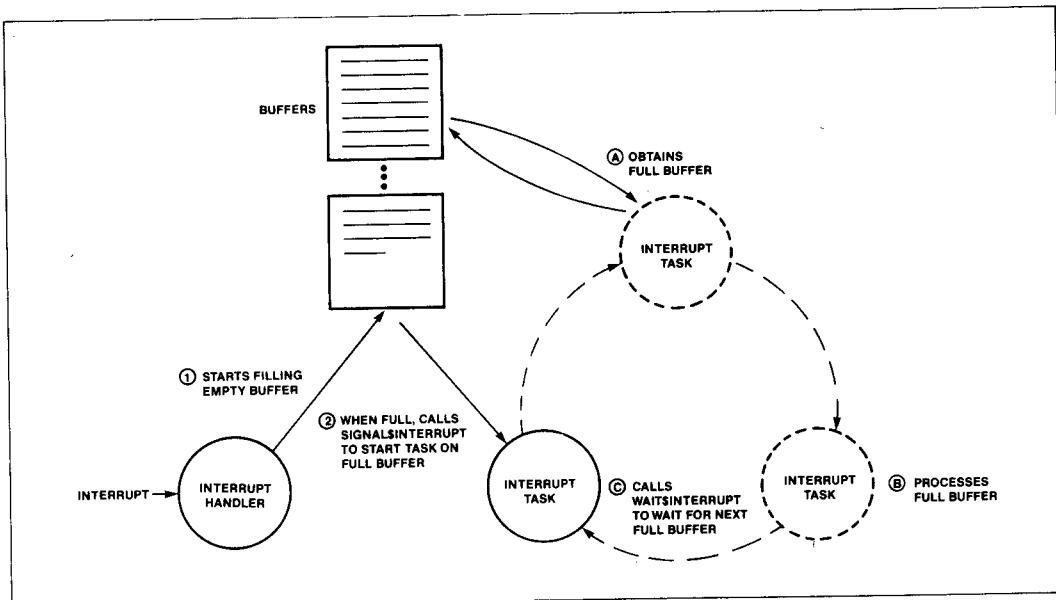


Figure 7. Multiple Buffer Example

SIGNAL INTERRUPT Used by an INTERRUPT HANDLER to activate an Interrupt Task.

WAIT INTERRUPT Suspends the calling Interrupt Task until the INTERRUPT HANDLER performs a SIGNAL INTERRUPT to invoke it. If a SIGNAL INTERRUPT for the task has occurred, it is processed.

FREE MEMORY MANAGEMENT

The OSP Free Memory Manager manages the memory pool which is allocated to each JOB for its execution needs. (The CREATE JOB primitive allocates the new JOB's memory pool from the memory pool of the parent JOB.) The memory pool is part of the JOB resources but is not yet allocated between the tasks of the JOB. When a TASK, MAILBOX, or REGION system data type structure is created within that JOB, the OSP implicitly allocates memory for it from the JOB's memory pool, so that a separate call to allocate memory is not required. OSP primitives that use free memory management implicitly include CREATE JOB, CREATE TASK, DELETE TASK, CREATE MAILBOX, DELETE MAILBOX, CREATE REGION, and DELETE REGION. The

CREATE SEGMENT primitive explicitly allocates a memory area when one is needed by the TASK. For example, a TASK may explicitly allocate a SEGMENT for use as a memory buffer. The SEGMENT length can be any multiple of 16 bytes between 16 bytes and 64K bytes in length. The programmer may specify any number of bytes from 1 byte to 64 KB, the OSP will transparently round the value up to the appropriate segment size.

The two explicit memory allocation/deallocation primitives are:

CREATE SEGMENT Allocates a SEGMENT of specified length (in 16-byte-long paragraphs) from the JOB Memory Pool.

DELETE SEGMENT Deallocates the SEGMENT's memory area, and returns it to the JOB memory pool.

Intertask Communication

The OSP has built-in intertask synchronization and communication, permitting TASKs to pass and share information with each other. OSP MAILBOXes contain controlled handshaking facilities which guarantee that a *complete* message will always be sent from a sending TASK to a receiving TASK. Each MAILBOX consists of two interlocked queues, one of TASKs

and the other of Messages. Four OSP primitives for intertask synchronization and communication are provided:

CREATE MAILBOX	Creates intertask message exchange.
DELETE MAILBOX	Deletes an intertask message exchange.
RECEIVE MESSAGE	Calling TASK receives a message from the MAILBOX.
SEND MESSAGE	Calling TASK sends a message to the MAILBOX.

The CREATE MAILBOX primitive allocates a MAILBOX for use as an information exchange between TASKs. The OSP will post information at the MAILBOX in a FIFO (First-In First-Out) manner when a SEND MESSAGE instruction is issued. Similarly, a message is retrieved by the OSP if a TASK issues a RECEIVE MESSAGE primitive. The TASK which creates the MAILBOX may make it available to other TASKs to use.

If no message is available, the TASK attempting to receive a message may choose to wait for one or continue executing.

The queue management method for the task queue (FIFO or PRIORITY) determines which TASK in the MAILBOX TASK queue will receive a message from the MAILBOX. The method is specified in the CREATE MAILBOX primitive.

Intertask Synchronization and Mutual Exclusion

Mutual exclusion is essential to multiprogramming and multiprocessing systems. The REGION system data type implements mutual exclusion. A REGION is represented by a queue of TASKS waiting to use a resource which must be accessed by only one TASK at a time. The OSP provides primitives to use REGIONS to manage mutually exclusive data and resources. Both critical code sections and shared data structures can be protected by these primitives from simultaneous use by more than one task. REGIONS support both FIFO (First-In First-Out) or Priority queueing disciplines for the TASKS seeking to enter the REGION. The REGION SDT can also be used to implement software locks.

Multiple REGIONS are allowed, and are automatically exited in the reverse order of entry. While in a REGION, a TASK cannot be suspended by itself or any other TASK, and thereby avoids deadlock.

There are five OSP primitives for mutual exclusion:

CREATE REGION	Create a REGION (lock).
SEND CONTROL	Give up the REGION.
ACCEPT CONTROL	Request the REGION, but do not wait if it is not available.
RECEIVE CONTROL	Request a REGION, wait if not immediately available.
DELETE REGION	Delete a REGION.

The OSP also provides dynamic priority adjustment for TASKs within priority REGIONS: If a higher-priority TASK issues a RECEIVE CONTROL primitive, while a (lower-priority) TASK has the use of the same REGION, the lower-priority TASK will be transparently, and temporarily, elevated to the waiting TASK's priority until it relinquishes the REGION via SEND CONTROL. At that point, since it is no longer using the critical resource, the TASK will have its normal priority restored.

OSP Control Facilities

The OSP also includes system primitives that provide both control and customization capabilities to a multitasking system. These primitives are used to control the deletion of SDTs and the recovery of free memory in a system, to allow interrogation of operating system status, and to provide uniform means of adding user SDTs and type managers.

DELETION CONTROL

Deletion of each OSP system data type is explicitly controlled by the applications programmer by setting a deletion attribute for that structure. For example, if a SEGMENT is to be kept in memory until DMA activity is completed, its deletion attribute should be disabled. Each TASK, MAILBOX, REGION, and SEGMENT SDT is created with its deletion attribute enabled (i.e., they may be deleted). Two OSP primitives control the deletion attribute: ENABLE DELETION and DISABLE DELETION.

ENVIRONMENTAL CONTROL

The OSP provides inquiry and control operations which help the user interrogate the application environment and implement flexible exception handling. These features aid in run-time decision making and in application error processing and recovery. There are five OSP environmental control primitives.

OS EXTENSIONS

The OSP architecture is defined to allow new user-defined System Data Types and the primitives to manipulate them to be added to OSP capabilities

provided by the built-in System Data Types. The type managers created for the user-defined SDTs are called user OS extensions and are installed in the system by the SET OS EXTENSION primitive. Once installed, the functions of the type manager may be invoked with user primitives conforming to the OSP interface. For well-structured extended architectures, each OS extension should support a separate user-defined system data type, and every OS extension should provide the same calling sequence and program interface for the user as is provided for a built-in SDT. The type manager for the extension would be written to suit the needs of the application. OSP interrupt vector entries (224-255) are reserved for user OS extensions and are not used by the OSP. After assigning an interrupt number to the extension, the extension user may then call it with the standard OSP call sequence (Figure 4), and the unique software interrupt number assigned to the extension.

ENABLE DELETION	Allows a specific SEGMENT, TASK, MAILBOX, or REGION SDT to be deleted.
DISABLE DELETION	Prevents a specific SEGMENT, TASK, MAILBOX, or REGION SDT from being deleted.
GET TYPE	Given a token for an instance of a system data type, returns the type code.
GET TASK TOKENS	Returns to the caller information about the current task environment.
GET EXCEPTION HANDLER	Returns information about the calling TASK's current information handler: its address, and when it is used.
SET EXCEPTION HANDLER	Provides the address and usage of an exception handler for a TASK.
SET OS EXTENSION	Modifies one of the interrupt vector entries reserved for OS extensions (224-255) to point to a user OS extension procedure.
SIGNAL EXCEPTION	For use in OS extension error processing.

EXCEPTION HANDLING

The OSP supports exception handlers. These are similar to CPU exception handlers such as OVERFLOW and ILLEGAL OPERATION. Their purpose is to

allow the OSP primitives to report parameter errors in primitive calls, and errors in primitive usage. Exception handling procedures are flexible and can be individually programmed by the application. In general, an exception handler if called will perform one or more of the following functions:

- Log the Error.
- Delete/Suspend the Task that caused the exception.
- Ignore the error, presumably because it is not serious.

An EXCEPTION HANDLER is written as a procedure. If PLM/86 is used, the "compact," "medium" or "large" model of computation should be specified for the compilation of the program. The mode in which the EXCEPTION HANDLER operates may be specified in the SET EXCEPTION HANDLER primitive. The return information from a primitive call is shown in Figure 4. CX is used to return standard system error conditions. Table 7 shows a list of these conditions, using the default EXCEPTION HANDLER of the OSP.

HARDWARE DESCRIPTION

The 80130 operates in a closely coupled mode with the iAPX 86/10 or 88/10 CPU. The 80130 resides on the CPU local multiplexed bus (Figure 8). The main processor is always configured for maximum mode operation. The 80130 automatically selects between its 88/30 and 86/30 operating modes.

The 80130 used in the 86/30 configuration, as shown in Figure 8 (or a similar 88/30 configuration), operates at both 5 and 8 MHz without requiring processor wait states. Wait state memories are fully supported, however. The 80130 may be configured with both an 8087 NPX and an 8089 IOP, and provides full context control over the 8087.

The 80130 (shown in Figure 3) is internally divided into a control unit (CU) and operating system unit (OSU). The OSU contains facilities for OSP kernel support including the system timers for scheduling and timing waits, and the interrupt controller for interrupt management support.

iAPX 86/30, iAPX 88/30 System Configuration

The 80130 is both I/O and memory mapped to the local CPU bus. The CPU's status S0-S2/ is decoded along with IOCS/ (with BHE and AD₃-AD₀) or MEMCS/ (with AD₁₃-AD₀). The pins are internally latched. See Table 1 for the decoding of these lines.

Memory Mapping

Address lines A₁₉-A₁₄ can be used to form MEMCS/ since the 80130's memory-mapped portion is aligned along a 16K-byte boundary. The 80130 can reside on any 16K-byte boundary excluding the highest (FC000H-FFFFFH) and lowest (00000H-003FFH). The 80130 control store code is position-independent except as limited above, in order to make it compatible with many decoding logic designs. AD₁₃-AD₀ are decoded by the 80130's kernel control store.

I/O Mapping

The I/O-mapped portion of the 80130 must be aligned along a 16-byte boundary. Address lines A₁₅-A₄ should be used to form IOCS/.

System Performance

The approximate performance of representative OSP primitives is given in Table 5. These times are shown for a typical iAPX 86/30 implementation with an 8 MHz clock. These execution times are very comparable to the execution times of similar functions in minicomputers (where available) and are an order of magnitude faster than previous generation microprocessors.

Initialization

Both application system initialization and OSP-specific initialization/configuration are required to use the OSP. Configuration is based on a "database" provided by the user to the iOSP 86 support package. The OSP-specific initialization and configuration information area is assigned to a user memory address adjacent to the 80130's memory-mapped location. (See Application Note 130 for further details.) The configuration data defines whether 8087 support is configured in the system, specifies if slave 8259A interrupt controllers are used in addition to the 80130, and sets the operating system time base (Tick Interval). Also located in the configuration area are the exception handler control parameters, the address location of the (separate) application system configuration area and the OSP extensions in use. The OSP application system configuration area may be located anywhere in the user memory and must include the starting address of the application instruction code to be executed, plus the locations of the RAM memory blocks to be managed by the OSP free memory manager. Complete application system support and the required 80130 configuration support are provided by the iAPX 86/30 and iAPX 88/30 OPERATING SYSTEM PROCESSOR SUPPORT PACKAGE (iOSP 86).

RAM Requirements

The OSP manages its own interrupt vector, which is assigned to low RAM memory. Working RAM storage is required as stack space and data area. The memory space must be allocated in user RAM.

OSP interrupt vector memory locations 0H-3FFH must be RAM based. The OSP requires 2 bytes of allocated RAM. The processor working storage is dynamically allocated from free memory. Approximately 300 bytes of stack should be allocated for each OSP task.

TYPICAL SYSTEM CONFIGURATION

Figure 8 shows the processing cluster of a "typical" iAPX 86/30 or iAPX 88/30 OSP system. Not shown are subsystems likely to vary with the application. The configuration includes an 8086 (or 8088) operating in maximum mode, an 8284A clock generator and an 8288 system controller. Note that the 80130 is located on the CPU side of any latches or transceivers. See Intel Application Note 130 for further details on configuration.

OSP Timers

The OSP Timers are connected to the lower half of the data bus and are addressed at even addresses. The timers are read as two successive bytes, always LSB followed by MSB. The MSB is always latched on a read operation and remains latched until read. Timers are not gatable.

Baud Rate Generator

The baud rate generator is 8254 compatible (square wave mode 3). Its output, BAUD, is initially high and remains high until the Count Register is loaded. The first falling edge of the clock after the Count Register is loaded causes the transfer of the internal counter to the Count Register. The output stays high for N/2 [(N+1)/2 if N is odd] and then goes low for N/2 [(N-1)/2 if N is odd]. On the falling edge of the clock which signifies the final count for the output in low state, the output returns to high state and the Count Register is transferred to the internal counter. The whole process is then repeated. Baud Rates are shown in Table 6.

The baud rate generator is located at 0CH (12), relative to the 16-byte boundary in the I/O space in which the 80130 component is located ("OSF" in the following example), the timer control word is located at

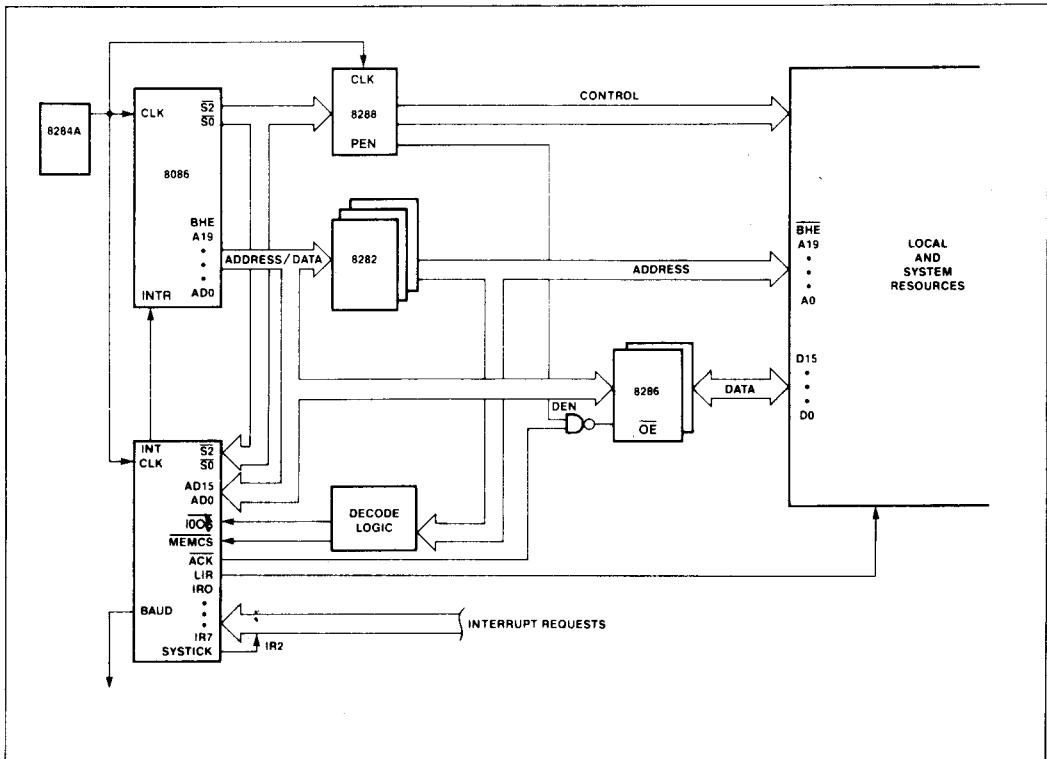


Figure 8. Typical OSP Configuration

relative address, 0EH(14). Timers are addressed with IOCS=0. Timers 0 and 1 are assigned to the use by the OSP, and should not be altered by the user.

For most baud-rate generator applications, the command byte

0B6H Read/Write Baud-Rate Delay Value

will be used. A typical sequence to set a baud rate of 9600 using a count value of 52 follows (see Table 6):

```

MOV AX,0B6H ;Prepare to Write Delay to
              ;Timer 3.
OUT OSF+14,AX ;Control Word.
MOV AX, 52
OUT OSF+12,AL ;LSB written first
XCHG AL,AH
OUT OSF+12,AL ;MSB written after.

```

The 80130 timers are subset compatible with 8254 timers.

Interrupt Controller

The Programmable Interrupt Controller (PIC), is also an integral unit of the 80130. Its eight input pins handle eight vectored priority interrupts. One of these pins must be used for the SYSTICK time function in timing waits, using an external connection as shown. During the 80130 initialization and configuration sequence, each 80130 interrupt pin is individually programmed as either level or edge sensitive. External slave 8259A interrupt controllers can be used to expand the total number of OSP external interrupts to 57.

In addition to standard PIC functions, 80130 PIC unit has an LIR output signal, which when low indicates an interrupt acknowledge cycle. LIR=0 is provided to control the 8289 Bus Arbiter SYSB/RESB pin. This will avoid the need of requesting the system bus to acknowledge local bus non-slave interrupts. The user defines the interrupt system as part of the configuration.

INTERRUPT SEQUENCE

The OSP interrupt sequence is as follows:

1. One or more of the interrupts is set by a low-to-high transition on edge-sensitive IR inputs or by a high input on level-sensitive IR inputs.
2. The 80130 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an interrupt acknowledge cycle which is encoded in S_2-S_0 .
4. Upon receiving the first interrupt acknowledge from the CPU, the highest-priority interrupt is set by the 80130 and the corresponding edge detect latch is reset. The 80130 does not drive the address/data bus during this bus cycle but does acknowledge the cycle by making $ACK=0$ and sending the LIR value for the IR input being acknowledged.
5. The CPU will then initiate a second interrupt acknowledge cycle. During this cycle, the 80130 will supply the cascade address of the interrupting input at T_1 on the bus and also release an 8-bit pointer onto the bus if appropriate, where it is read by the CPU. If the 80130 does supply the pointer, then ACK will be low for the cycle. This cycle also has the value LIR for the IR input being acknowledged.
6. This completes the interrupt cycle. The ISR bit remains set until an appropriate EXIT INTERRUPT primitive (EOI command) is called at the end of the Interrupt Handler.

OSP APPLICATION EXAMPLE

Figure 5 shows an application of the OSP primitives to keep track of time of day in a simplified example. The system design uses a 60 Hz A.C. signal as a time base. The power supply provides a TTL-compatible

signal which drives one of 80130 edge-triggered interrupt request pins once each A.C. cycle. The Interrupt Handler responds to the interrupts, keeping track of one second's A.C. cycles. The Interrupt Task counts the seconds and after a day deletes itself. In typical systems it might perform a data logging operation once each day. The Interrupt Handler and Interrupt Task are written as separate modular programs.

The Interrupt Handler will actually service interrupt 59 when it occurs. It simply counts each interrupt, and at a count of 60 performs a SIGNAL INTERRUPT to notify the Interrupt Task that a second has elapsed. The Interrupt Handler (ACS HANDLER) was assigned to this level by the SET INTERRUPT primitive. After doing this, the Interrupt Task performed the Primitive RESUME TASK to resume the application task (INITS TASKS TOKEN).

The main body of the task is the counting loop. The Interrupt Task is signaled by the SIGNAL INTERRUPT primitive in the Interrupt Handler (at interrupt level ACS INTERRUPTS LEVEL). When the task is signalled by the Interrupt Handler it will execute the loop exactly one time, increasing the time count variables. Then it will execute the WAIT INTERRUPT primitive, and wait until awakened by the Interrupt Handler. Normally, the task will now wait some period of time for the next signal. However, since the interface between the Handler and the Task is asynchronous, the handler may have already queued the interrupt for servicing, the writer of the task does not have to worry about this possibility.

At the end of the day, the task will exit the loop and execute RESET INTERRUPT, which disables the interrupt level, and deletes the interrupt task. The OSP now reclaims the memory used by the Task and schedules another task. If an exception occurs, the coded value for the exception is available in TIMES EXCEPTS CODE after the execution of the primitive.

A typical PL/M-86 calling sequence is illustrated by the call to RESET INTERRUPT shown in Figure 5.

Table 2. OSP System Data Type Summary

Job	Jobs are the means of organizing the program environment and resources. An application consists of one or more jobs. Each iAPX 86/30 system data type is contained in some job. Jobs are independent of each other, but they may share access to resources. Each job has one or more tasks, one of which is an initial task. Jobs are given pools of memory, and they may create subordinate offspring jobs, which may borrow memory from their parents.
Task	Tasks are the means by which computations are accomplished. A task is an instruction stream with its own execution stack and private data. Each task is part of a job and is restricted to the resources provided by its job. Tasks may perform general interrupt handling as well as other computational functions. Each task has a set of attributes, which is maintained for it by the iAPX 86/30, which characterize its status. These attributes are: its containing job its register context its priority (0-255) its execution state (asleep, suspended, ready, running, asleep/suspended). its suspension depth its user-selected exception handler its optional 8087 extended task state
Segment	Segments are the units of memory allocation. A segment is a physically contiguous sequence of 16-byte, 8086 paragraph-length, units. Segments are created dynamically from the free memory space of a Job as one of its Tasks requests memory for its use. A segment is deleted when it is no longer needed. The iAPX 86/30 maintains and manages free memory in an orderly fashion, it obtains memory space from the pool assigned to the containing job of the requesting task and returns the space to the job memory pool (or the parent job pool) when it is no longer needed. It does not allocate memory to create a segment if sufficient free memory is not available to it, in that case it returns an error exception code.
Mailbox	Mailboxes are the means of intertask communication. Mailboxes are used by tasks to send and receive message segments. The iAPX 86/30 creates and manages two queues for each mailbox. One of these queues contains message segments sent to the mailbox but not yet received by any task. The other mailbox queue consists of tasks that are waiting to receive messages. The iAPX 86/30 operation assures that waiting tasks receive messages as soon as messages are available. Thus at any moment one or possibly both of two mailbox queues will be empty.
Region	Regions are the means of serialization and mutual exclusion. Regions are familiar as "critical code regions." The iAPX 86/30 region data type consists of a queue of tasks. Each task waits to execute in mutually exclusive code or to access a shared data region, for example to update a file record.
Tokens	The OSP interface makes use of a 16-bit TOKEN data type to identify individual OSF data structures. Each of these (each instance) has its own unique TOKEN. When a primitive is called, it is passed the TOKENs of the data structures on which it will operate.

Table 3. System Data Type Codes and Attributes

S.D.T.	Code	Attributes
Jobs	1	Tasks Memory Pool S.D.T. Directory
Tasks	2	Priority Stack Code State Exception Handler
Mailboxes	3	Queue of S.D.T.s (generally segments) Queue of Tasks waiting for S.D.T.s
Region	5	Queue of Tasks waiting for mutually exclusive code or data
Segments	6	Buffer Length

Table 4. OSP Primitives

Class	OSP Primitive	Interrupt Number	Entry Code in AX	Parameters On Caller's Stack
J O B	CREATE JOB	184	0100H	*See 80130 User Manual
T A S K	CREATE TASK	184	0200H	Priority, IP Ptr, Data Segment, Stack Seg, Stack Size Task Information, ExcptPtr
	DELETE TASK	184	0201H	TASK, ExcptPtr
	SUSPEND TASK	184	0202H	TASK, ExcptPtr
	RESUME TASK	184	0203H	TASK, ExcptPtr
	SET PRIORITY	184	0209H	TASK, Priority, ExcptPtr
	SLEEP	184	0204H	Time Limit,ExcptPtr
I N T E R R U P T	DISABLE	190	0705H	Level, ExcptPtr
	ENABLE	184	0704H	Level #, ExcptPtr
	ENTER INTERRUPT	184	0703H	Level #, ExcptPtr
	EXIT INTERRUPT	186	NONE	Level #,ExcptPtr
	GET LEVEL	188	0702H	Level #, ExcptPtr
	RESET INTERRUPT	184	0706H	Level #, ExcptPtr
	SET INTERRUPT	184	0701H	Level, Interrupt Task Flag Interrupt Handler Ptr, Interrupt Handler DataSeg ExcptPtr
	SIGNAL INTERRUPT	185	NONE	Level, ExcptPtr
	WAIT INTERRUPT	187	NONE	Level, ExcptPtr
S E G M E N T	CREATE SEGMENT	184	0600H	Size, ExcptPtr
	DELETE SEGMENT	184	0603H	SEGMENT, ExceptPtr

Table 4. OSP Primitives (Continued)

Class	OSP Primitive	Interrupt Number	Entry Code in AX	Parameters On Caller's Stack
M A I L B O X	CREATE MAILBOX DELETE MAILBOX RECEIVE MESSAGE SEND MESSAGE	184 184 184 184	0300H 0301H 0303H 0302H	Mailbox flags, ExcptPtr MAILBOX, ExcptPtr MAILBOX, Time Limit ResponsePtr, ExcptPtr MAILBOX, Message Response, ExcptPtr
R E G I O N	ACCEPT CONTROL CREATE REGION DELETE REGION RECEIVE CONTROL SEND CONTROL	184 184 184 184 184	0504H 0500H 0501H 0503H 0502H	REGION, ExcptPtr Region Flags, ExcptPtr REGION, ExcptPtr REGION, ExcptPtr ExcptPtr
E N V I R O N M E N T A L	DISABLE DELETION ENABLE DELETION GET EXCEPTION HANDLER GET TYPE GET TASK TOKENS SET EXCEPTION HANDLER SET OS EXTENSION SIGNAL EXCEPTION	184 184 184 184 184 184 184 184	0001H 0002H 0800H 0000H 0206H 0801H 0700H 0802H	TOKEN, ExcptPtr TOKEN, ExcptPtr Ptr, ExcptPtr TOKEN, ExcptPtr Request, ExcptPtr Ptr, ExcptPtr Code, InstPtr, ExcptPtr Exception Code, Parameter Number, StackPtr, 0, 0, ExcptPtr

NOTES:

All parameters are pushed onto the OSP stack. Each parameter is one word. See Figure 3 for Call Sequence.

Explanation of the Symbols

JOB	OSP JOB SDT Token
TASK	OSP TASK SDT Token
REGION	OSP REGION SDT Token
MAILBOX	OSP MAILBOX SDT Token
SEGMENT	OSP SEGMENT SDT Token
TOKEN	Any SDT Token
Level	Interrupt Level Number
ExcptPtr	Pointer to Exception Code
Message	Message Token
Ptr	Pointer to Code, Stack etc. Address
Seg	Value Loaded into appropriate Segment Register
---	Value Parameter.

Table 5. OSP Primitive Performance Examples

Datatype Class	Primitive Execution Speed* (microseconds)
JOB	CREATE JOB
TASK	CREATE TASK (no preemption)
SEGMENT	CREATE SEGMENT
MAILBOX	SEND MESSAGE (with task switch)
	SEND MESSAGE (no task switch)
REGION	RECEIVE MESSAGE (task waiting)
	RECEIVE MESSAGE (message waiting)
	SEND CONTROL
	RECEIVE CONTROL

*8 MHz iAPX 86/30 OSP Configuration.

Table 6. Baud Rate Count Values (16X)

Baud Rate	8 MHz Count Value	5 MHz Count Value
300	1667	1042
600	833	521
1200	417	260
2400	208	130
4800	104	65
9600	52	33

Table 7a. Mnemonic Codes for Unavoidable Exceptions

E\$OK	Exception Code Value = 0 the operation was successful
E\$TIME	Exception Code Value = 1 the specified time limit expired before completion of the operations was possible
E\$MEM	Exception Code Value = 2 insufficient nucleus memory is available to satisfy the request
E\$BUSY	Exception Code Value = 3 specified region is currently busy
E\$LIMIT	Exception Code Value = 4 attempted violation of a job, semaphore, or system limit
E\$CONTEXT	Exception Code Value = 5 the primitive was called in an illegal context (e.g., call to enable for an already enabled interrupt)
E\$EXIST	Exception Code Value = 6 a token argument does not currently refer to any object; note that the object could have been deleted at any time by its owner
E\$STATE	Exception Code Value = 7 attempted illegal state transition by a task
E\$NOT\$CONFIGURED	Exception Code Value = 8 the primitive called is not configured in this system
E\$INTERRUPT\$SATURATION	Exception Code Value = 9 The interrupt task on the requested level has reached its user specified saturation point for interrupt service requests. No further interrupts will be allowed on the level until the interrupt task executes a WAIT\$INTERRUPT. (This error is only returned, in line, to interrupt handlers.)
E\$INTERRUPT\$OVERFLOW	Exception Code Value = 10 The interrupt task on the requested level previously reached its saturation point and caused an E\$INTERRUPT\$SATURATION condition. It subsequently executed an ENABLE allowing further interrupts to come in and has received another SIGNAL\$INTERRUPTcall, bringing it over its specified saturation point for interrupt service requests. (This error is only returned, in line, to interrupt handlers).

Table 7b. Mnemonic Codes for Avoidable Exceptions

E\$ZERO\$DIVIDE	Exception Code Value = 8000H divide by zero interrupt occurred
E\$OVERFLOW	Exception Code Value = 8001H overflow interrupt occurred
E\$TYPE	Exception Code Value = 8002H a token argument referred to an object tha was not of required type
E\$BOUNDS	Exception Code Value = 8003H an offset argument is out of segment bounds
E\$PARAM	Exception Code Value = 8004H a (non-token,non-offset) argument has an illegal value
E\$BAD\$CALL	Exception Code Value = 8005H an entry code for which there is no corresponding primitive was passed
E\$ARRAY\$BOUNDS = 8006H	Hardware or Language has detected an array overflow
E\$NDP\$ERROR	Exception Code Value = 8007H an 8087 (Numeric data Processor) error has been detected; (the 8087 status information is contained in a parameter to the exception handler)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bins	0°C to 70°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin With Respect to Ground	-1.0V to +7V
Power Dissipation	1.0 Watts

*NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

D.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.5$ to 5.5 V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + .5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2\text{mA}$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu\text{A}$
I_{CC}	Power Supply Current		200	mA	$T_A = 25^\circ\text{C}$
I_U	Input Leakage Current		10	μA	$0 < V_{IN} < V_{CC}$
I_{LR}	IR Input Load Current		10 -300	μA	$V_{IN} = V_{CC}$ $V_{IN} = 0$
I_{LO}	Output Leakage Current		10	μA	.45 = $V_{IN} = V_{CC}$
V_{CLL}	Clock Input Low		0.6	V	
V_{CHI}	Clock Input High	3.9		V	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		15	pF	
I_{CLL}	Clock Input Leakage Current		10 150 10	μA	$V_{IN} = V_{CC}$ $V_{IN} = 2.5\text{V}$ $V_{IN} = 0\text{V}$

A.C. CHARACTERISTICS ($T_A = 0$ to 70°C , $V_{CC} = 4.5$ to 5.5 Volt, V_{SS} = Ground)

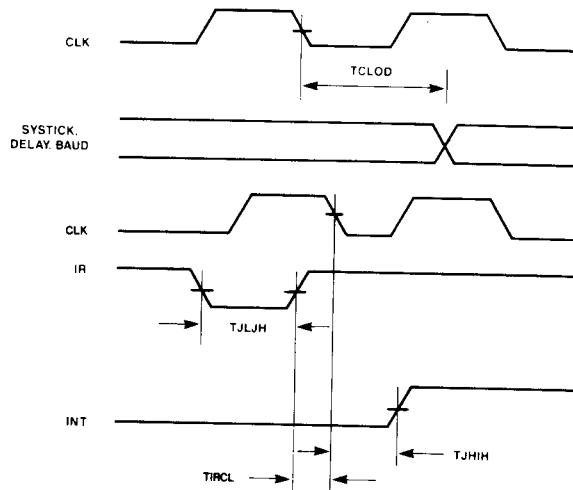
Symbol	Parameter	80130		80130-2		Units	Test Conditions
		Min.	Max.	Min.	Max.		
T_{CLCL}	CLK Cycle Period	200	—	125	—	ns	
T_{CLCH}	CLK Low Time	90	—	55	—	ns	
T_{CHCL}	CLK High Time	69	2000	44	2000	ns	
T_{SVCH}	Status Active Setup Time	80	—	65	—	ns	
T_{CHSV}	Status Inactive Hold Time	10	—	10	—	ns	
T_{SHCL}	Status Inactive Setup Time	55	—	55	—	ns	
T_{CLSH}	Status Active Hold Time	10	—	10	—	ns	
T_{ASCH}	Address Valid Setup Time	8	—	8	—	ns	
T_{CLAH}	Address Hold Time	10	—	10	—	ns	
T_{CSCL}	Chip Select Setup Time	20	—	20	—	ns	
T_{CHCS}	Chip Select Hold Time	0	—	0	—	ns	
T_{DSCL}	Write Data Setup Time	80	—	60	—	ns	
T_{CHDH}	Write Data Hold Time	10	—	10	—	ns	
T_{JLJH}	IR Low Time	100	—	100	—	ns	
T_{CLDV}	Read Data Valid Delay	—	140	—	105	ns	$C_L = 200\text{ pE}$
T_{CLDH}	Read Data Hold Time	10	—	10	—	ns	
T_{CLDX}	Read Data to Floating	10	100	10	100	ns	
T_{CLCA}	Cascade Address Delay Time	—	85	—	65	ns	

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	80130		80130-2		Units	Notes
		Min.	Max.	Min.	Max.		
T_{CLCF}	Cascade Addressee Hold Time	10	-	10	-	ns	
T_{IAVE}	INTA Status t Acknowledge	-	80	-	80	ns	
T_{CHEH}	Acknowledge Hold Time	0	-	0	-	ns	
T_{CSAK}	Chip Select to ACK	-	110	-	110	ns	
T_{SACK}	Status to ACK	-	140	-	140	ns	
T_{AACK}	Address to ACK	-	90	-	90	ns	
T_{CLOD}	Timer Output Delay Time	-	200	-	200	ns	$C_L = 100 \mu F$
T_{CLOD1}	Timer1 Output Delay Time	-	200	-	200	ns	$C_L = 100 \mu F$
T_{JHIH}	INT Output Delay	-	200	-	200	ns	
T_{IRCL}	IR Input Set Up	20		20		ns	

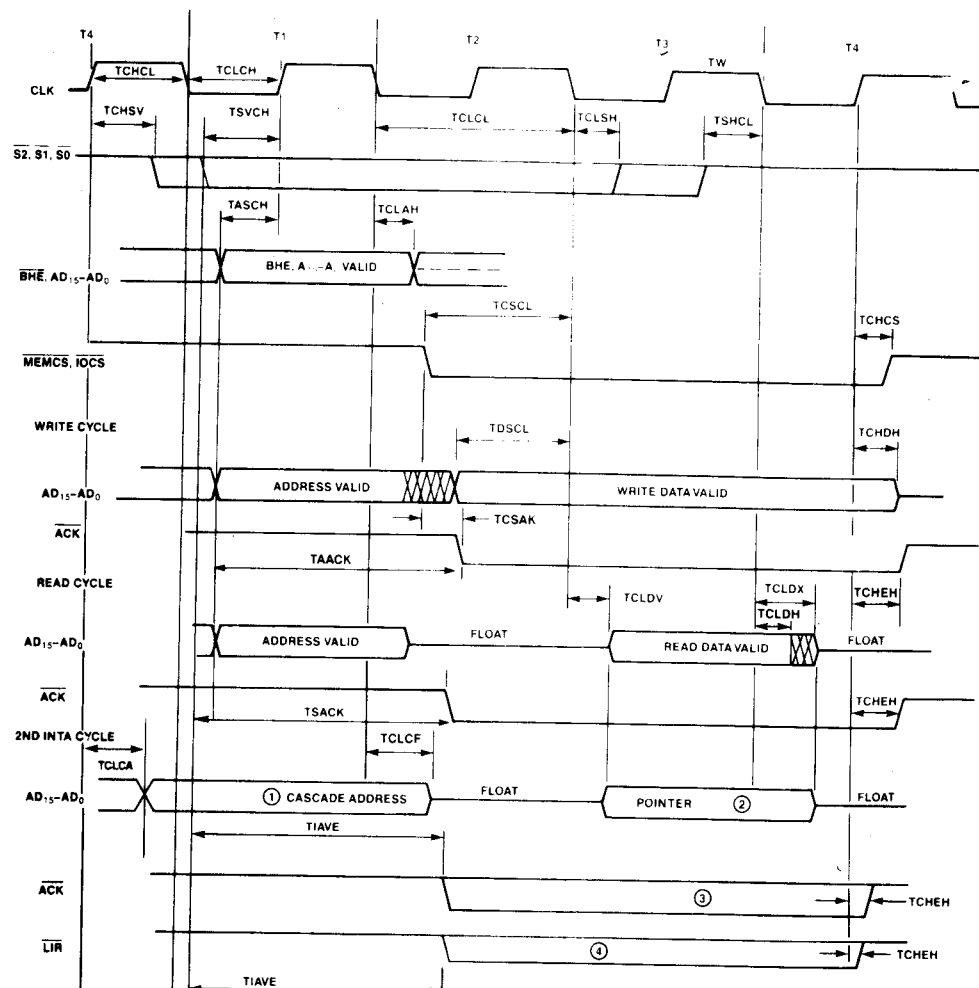
WAVEFORMS

A.C.



WAVEFORMS

A.C.



NOTES:

1. CASCADE ADDRESS PRESENTED ON AD8, AD9 AND AD10 CORRESPONDING TO CAS0, CAS1 AND CAS2 RESPECTIVELY AD11-AD15 LINES ARE ACTIVE AND HAVE UNKNOWN VALUES. AD0-AD7 ARE TRISTATE.
2. POINTER VALUE IS ACTIVE ONLY IF POINTER IS GENERATED FROM THE 80150 AND NOT FROM EXTERNAL SLAVE UNIT.
3. ACTIVE LOW ONLY WHEN POINTER DATA IS BEING SUPPLIED BY THE 80150.
4. LOW ONLY FOR LOCAL INTERRUPT.



8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics

- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range
- 40 Pin DIP Package

(See Intel Packaging: Order Number: 240800-001,
Package Type P)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

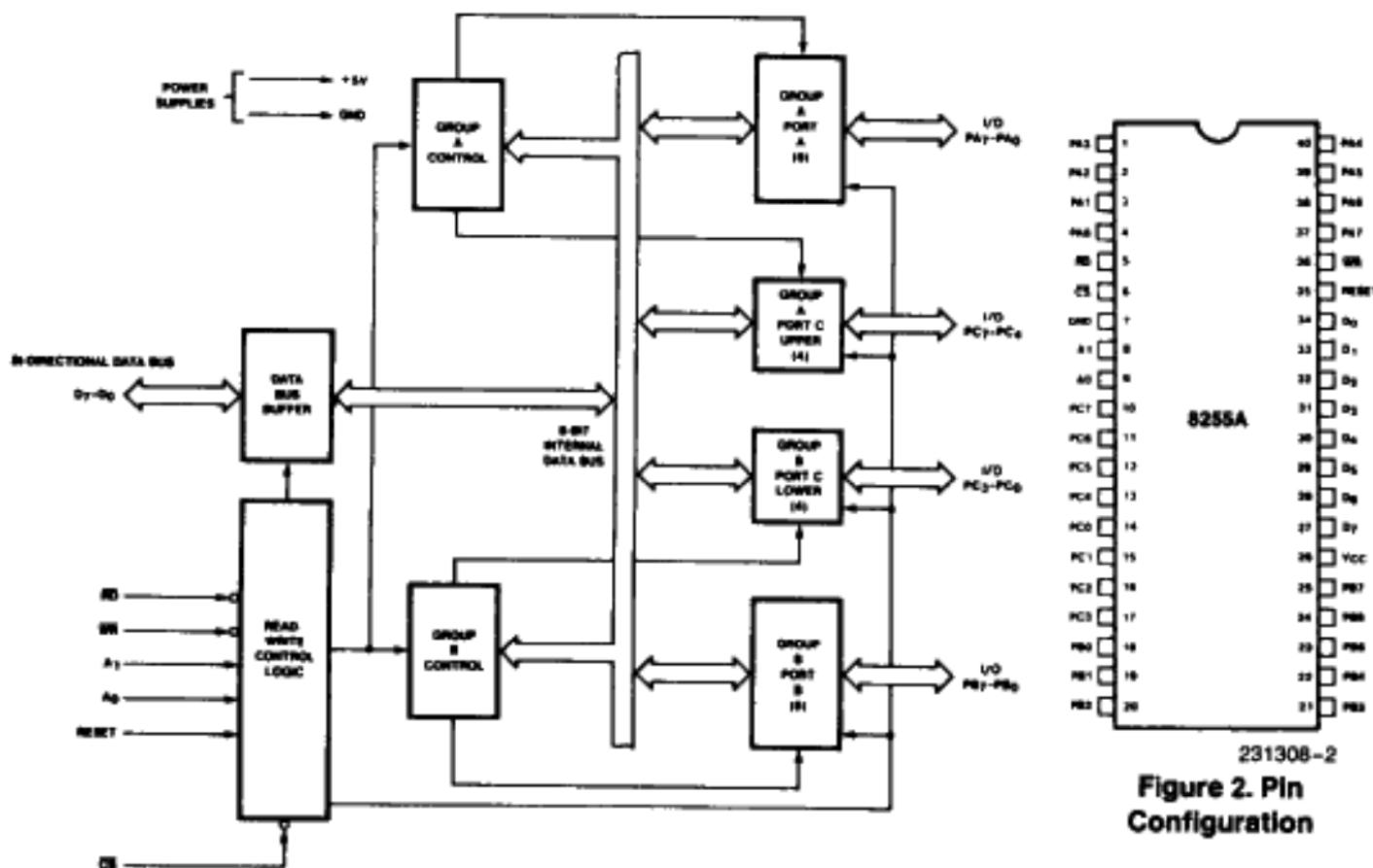


Figure 1. 8255A Block Diagram

231308-1

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the

CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

(RD)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

(WR)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

3

(A₀ and A₁)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A₀ and A₁).

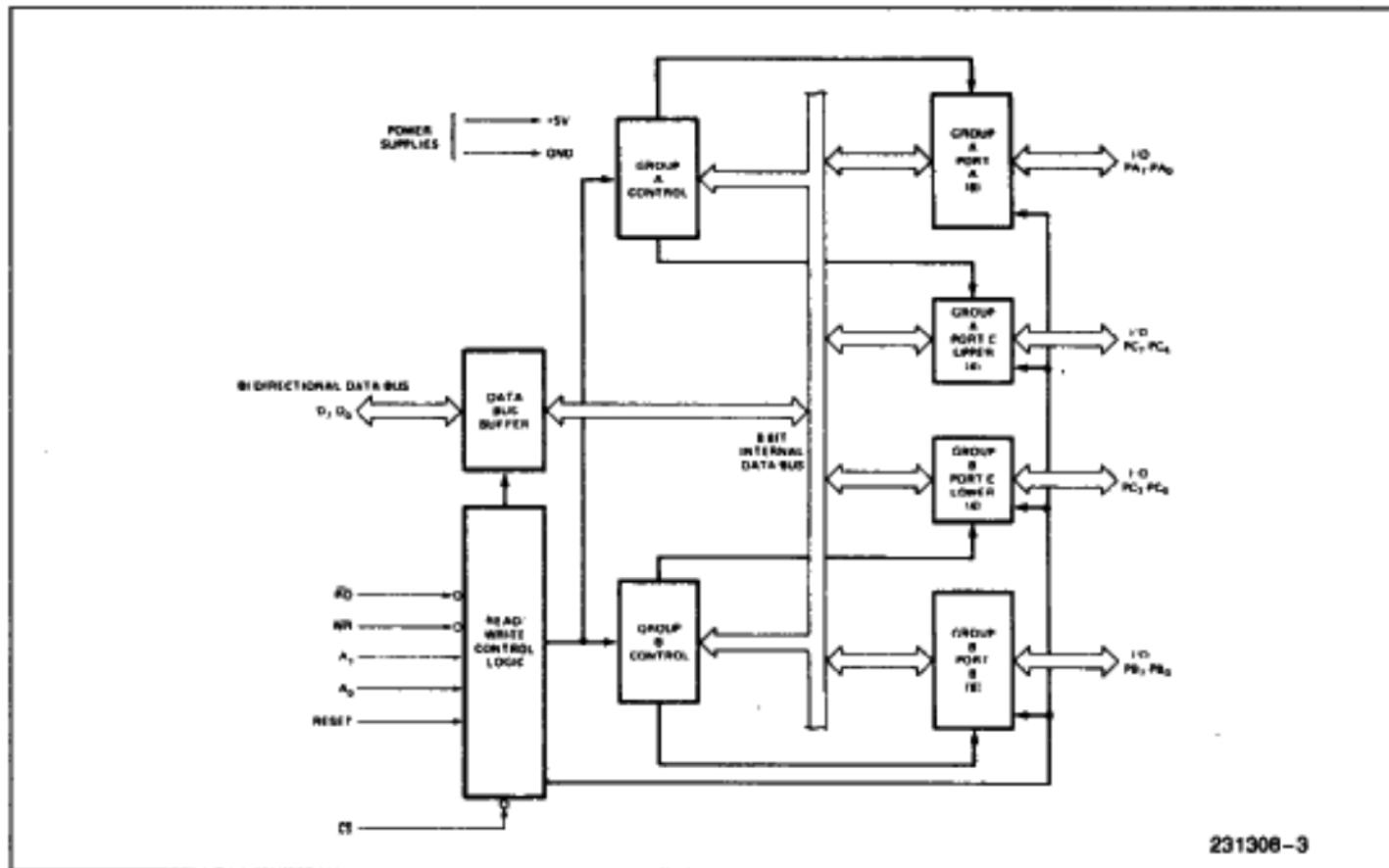


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

8255A BASIC OPERATION

A ₁	A ₀	RD	WR	CS	Input Operation (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
X	X	X	X	1	Data Bus → 3-State
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus → 3-State

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7-C4)
Control Group B—Port B and Port C lower (C3-C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

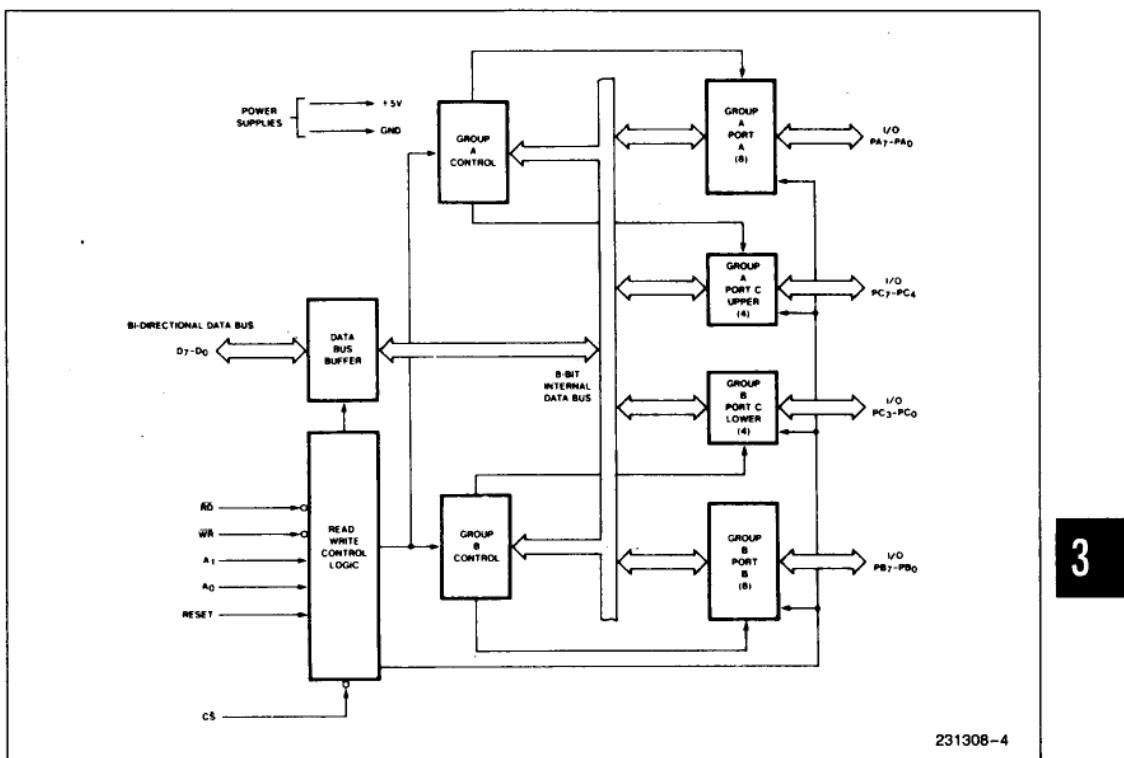
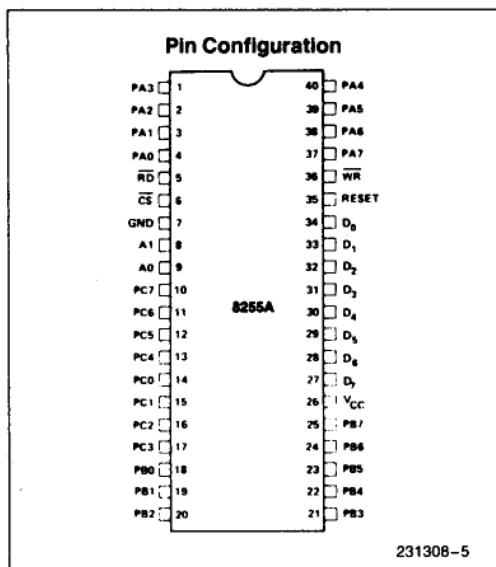


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions



Pin Names	
D ₇ -D ₀	Data Bus (Bi-Directional)
RESET	Reset Input
CS	Chip Select
RD	Read Input
WR	Write Input
A ₀ , A ₁	Port Address
PA7-PA0	Port A (BIT)
PB7-PB0	Port B (BIT)
PC7-PC0	Port C (BIT)
V _{CC}	+ 5 Volts
GND	0 Volts

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0—Basic Input/Output

Mode 1—Strobed Input/Output

Mode 2—Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

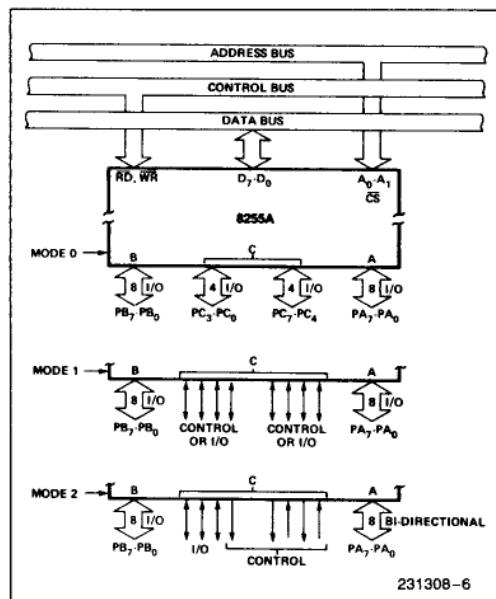


Figure 5. Basic Mode Definitions and Bus Interface

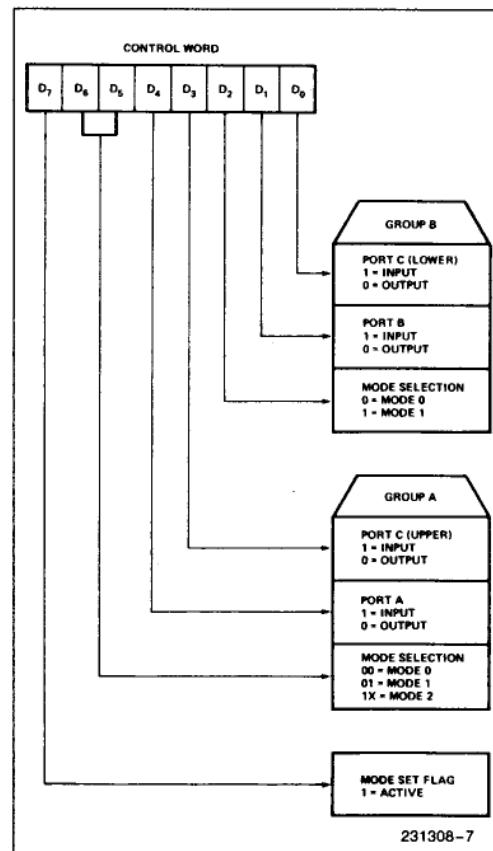


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

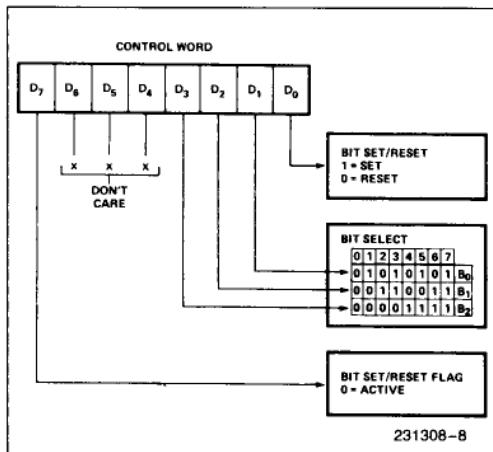


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is set—interrupt enable

(BIT-RESET)—INTE is RESET—interrupt disable

NOTE:

All Mask flip-flops are automatically reset during mode selection and device Reset.

3

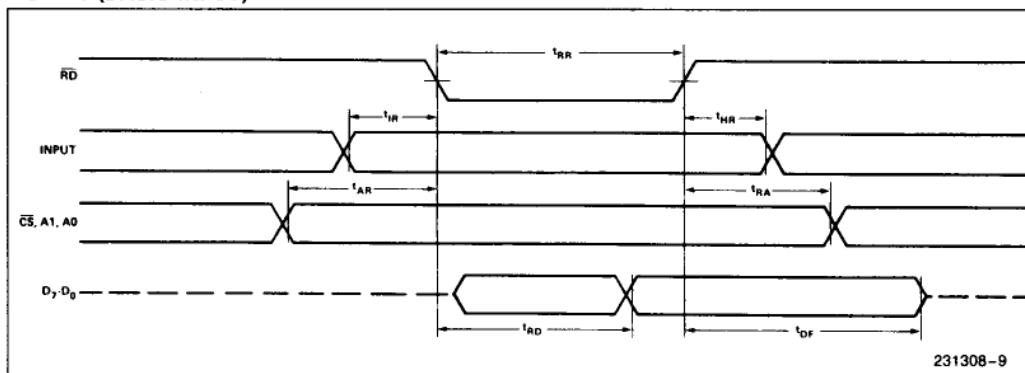
Operating Modes

MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

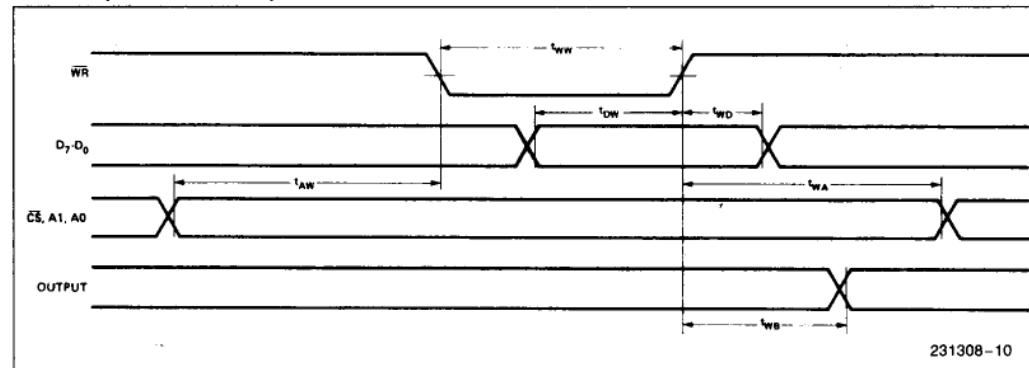
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



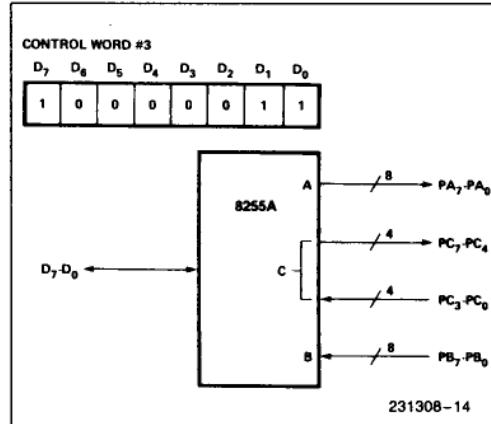
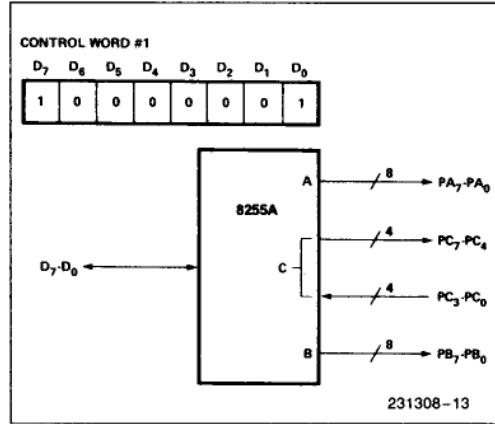
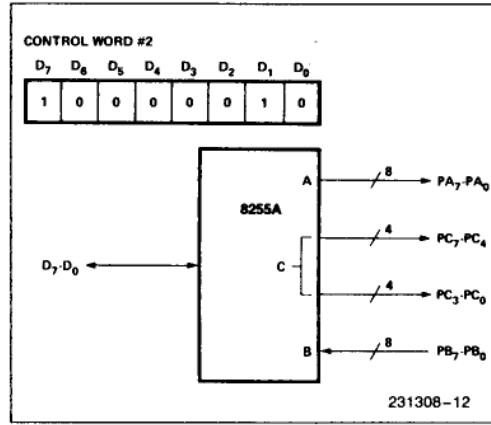
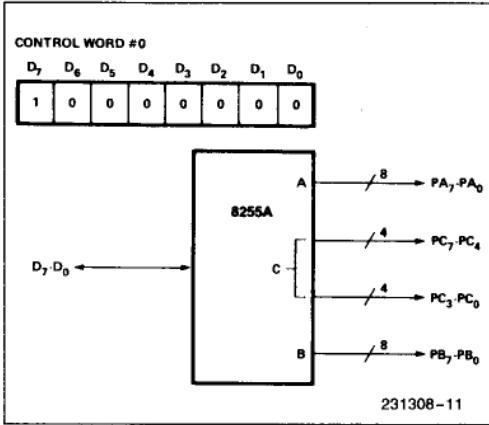
MODE 0 (BASIC OUTPUT)



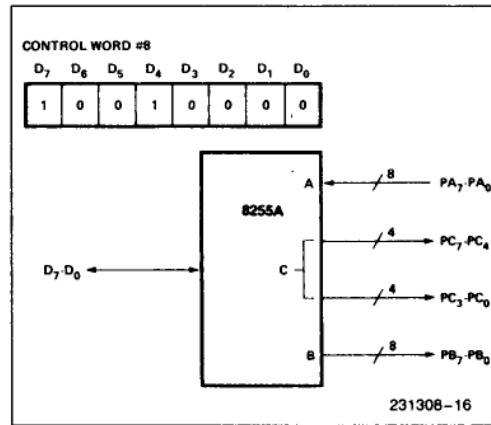
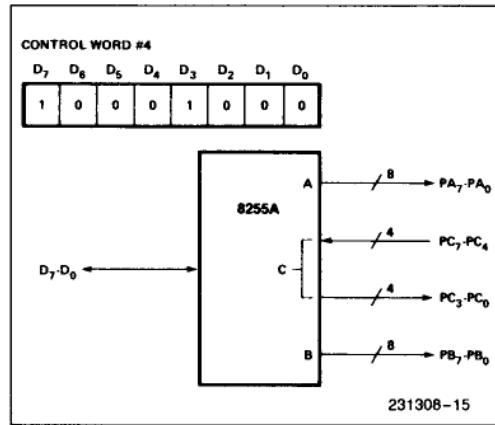
MODE 0 PORT DEFINITION

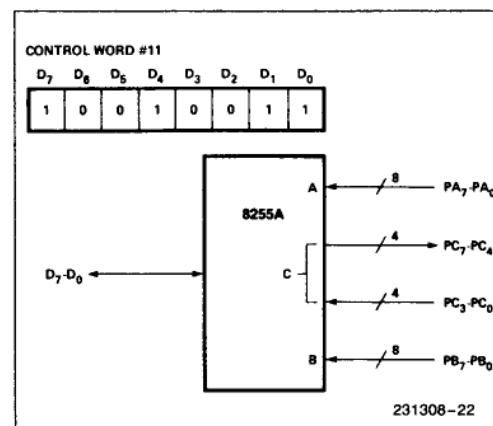
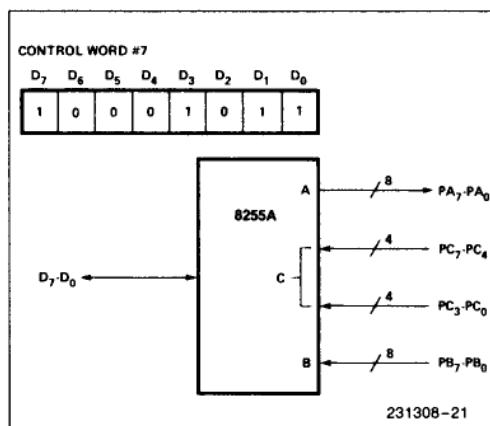
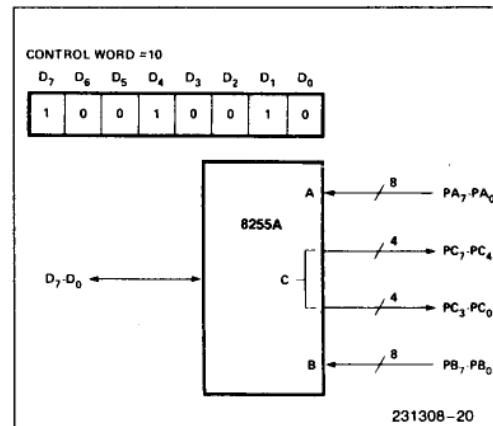
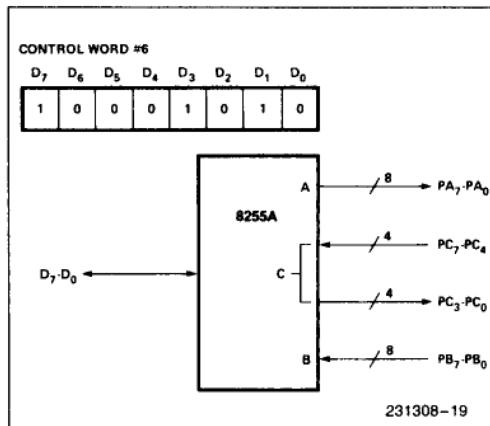
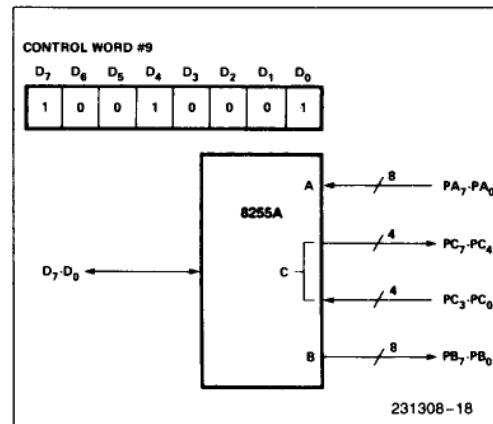
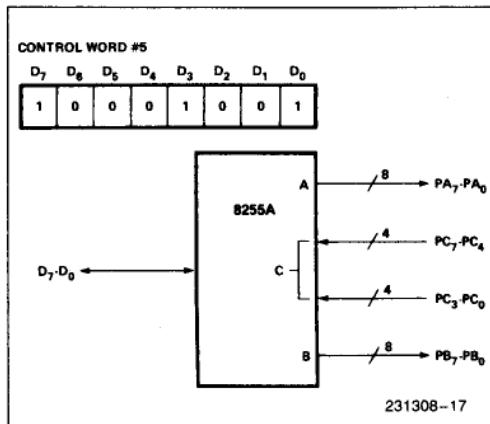
A		B		Group A		#	Group B	
D ₄	D ₃	D ₁	D ₀	Port A	Port C (Upper)		Port B	Port C (Lower)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

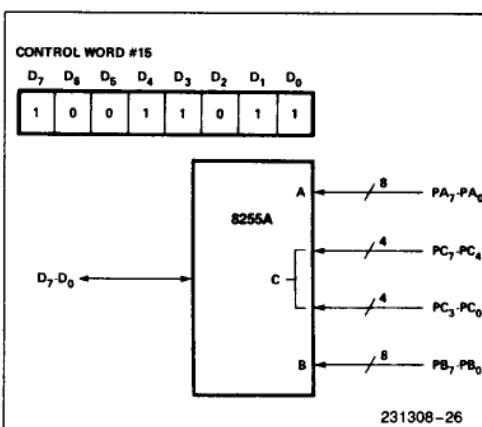
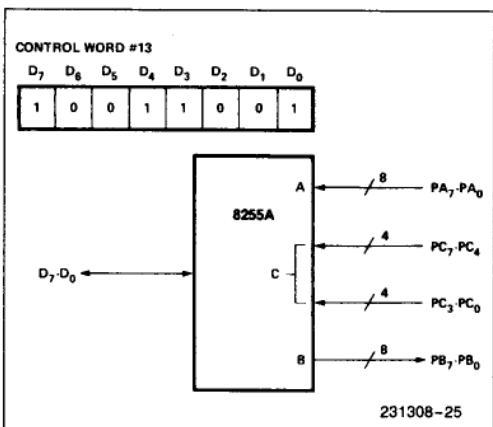
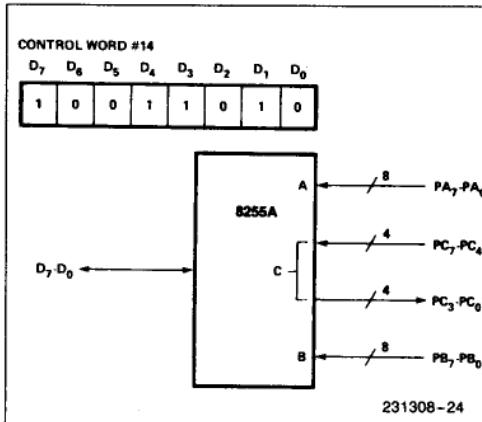
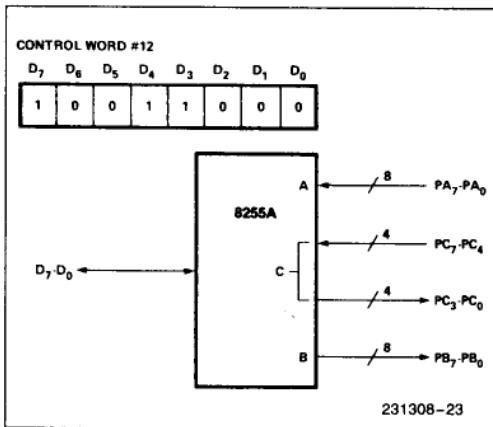
MODE CONFIGURATIONS



3







3

Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

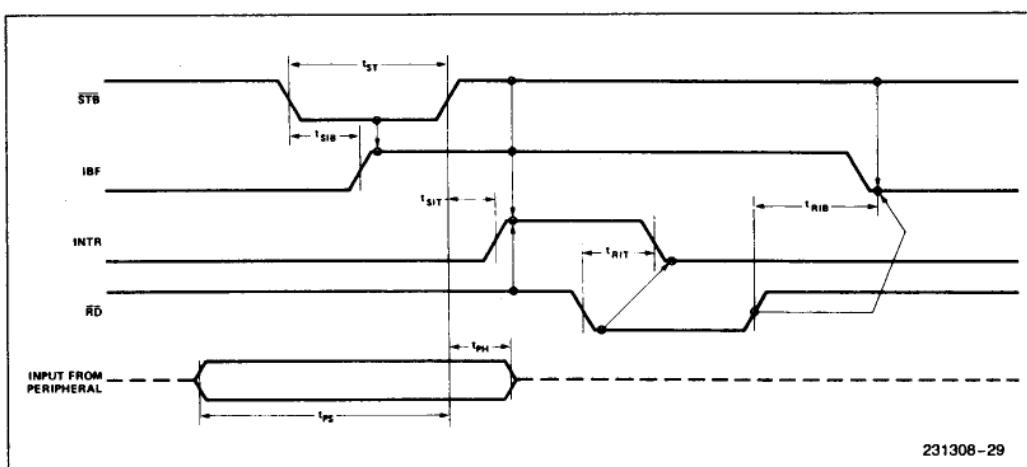
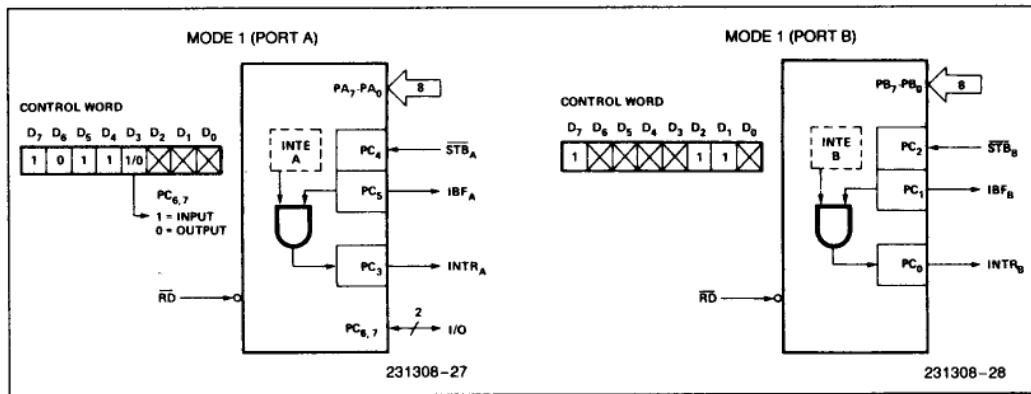
STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE AControlled by bit set/reset of PC₄.**INTE B**Controlled by bit set/reset of PC₂.**Figure 9. MODE 1 (Strobed Input)**

Output Control Signal Definition

OBF (Output Buffer Full F/F). The \overline{OBF} output will go "low" to indicate that the CPU has written data out to the specified port. The \overline{OBF} F/F will be set by the rising edge of the \overline{WR} input and reset by ACK input being low.

ACK (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output

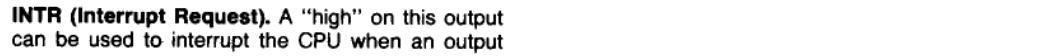
device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", \overline{OBF} is a "one", and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC₆.

INTE B

Controlled by bit set/reset of PC₂.



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Figure 10. MODE 1 Output

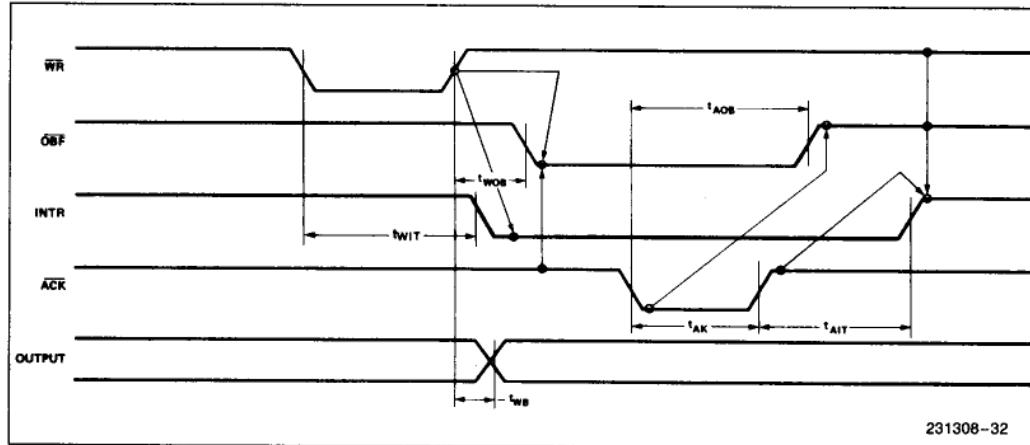


Figure 11. MODE 1 (Strobed Output)

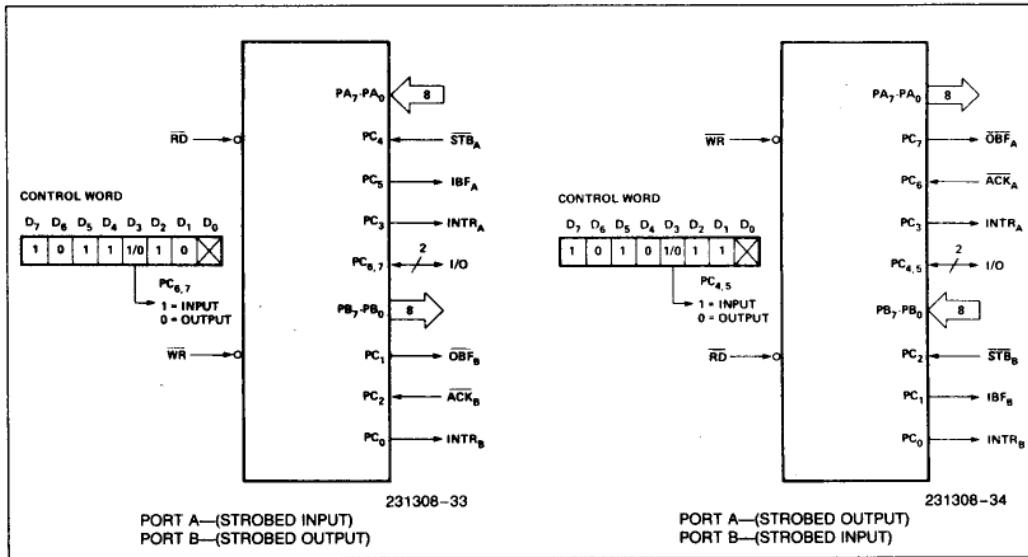


Figure 12. Combinations of MODE 1

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in MODE 1 to support a wide variety of strobed I/O applications.

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

OBF (Output Buffer Full). The OBF output will go "low" to indicate that the CPU has written data out to port A.

ACK (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC₆.

Input Operations

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC₄.

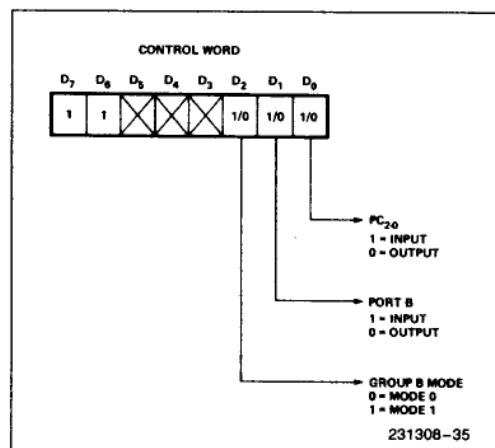
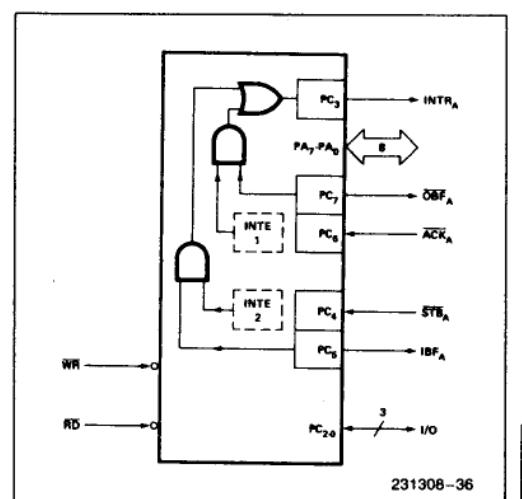


Figure 13. MODE Control Word



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Figure 14. MODE 2

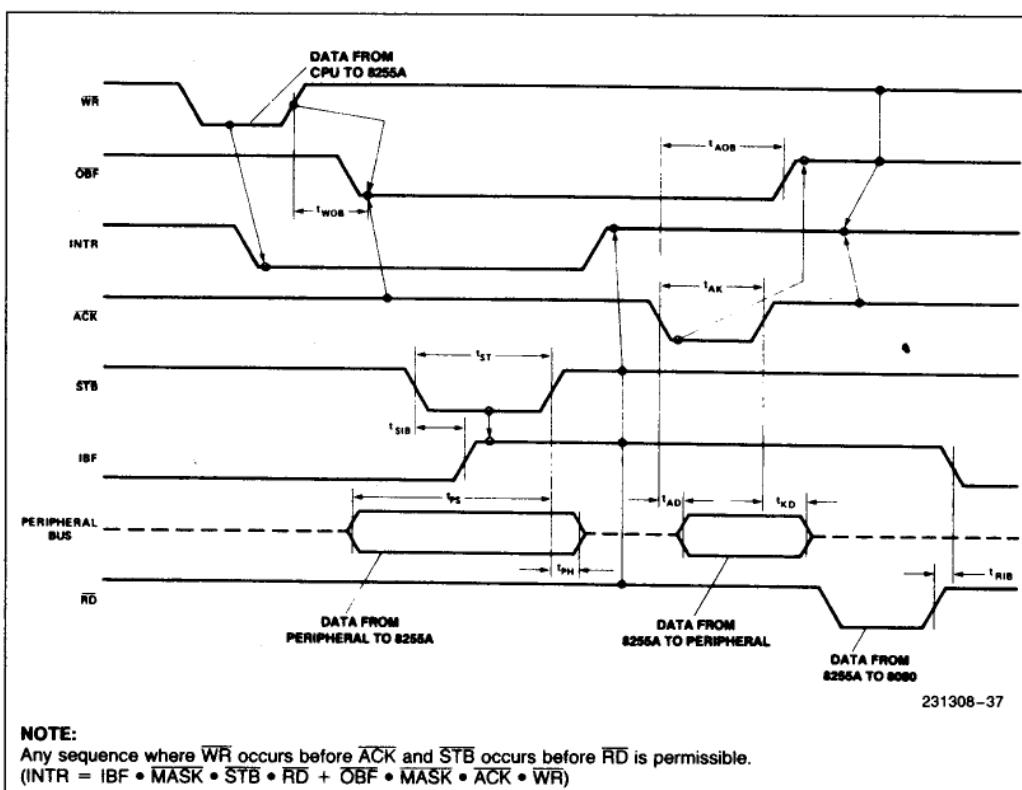


Figure 15. MODE 2 (Bidirectional)

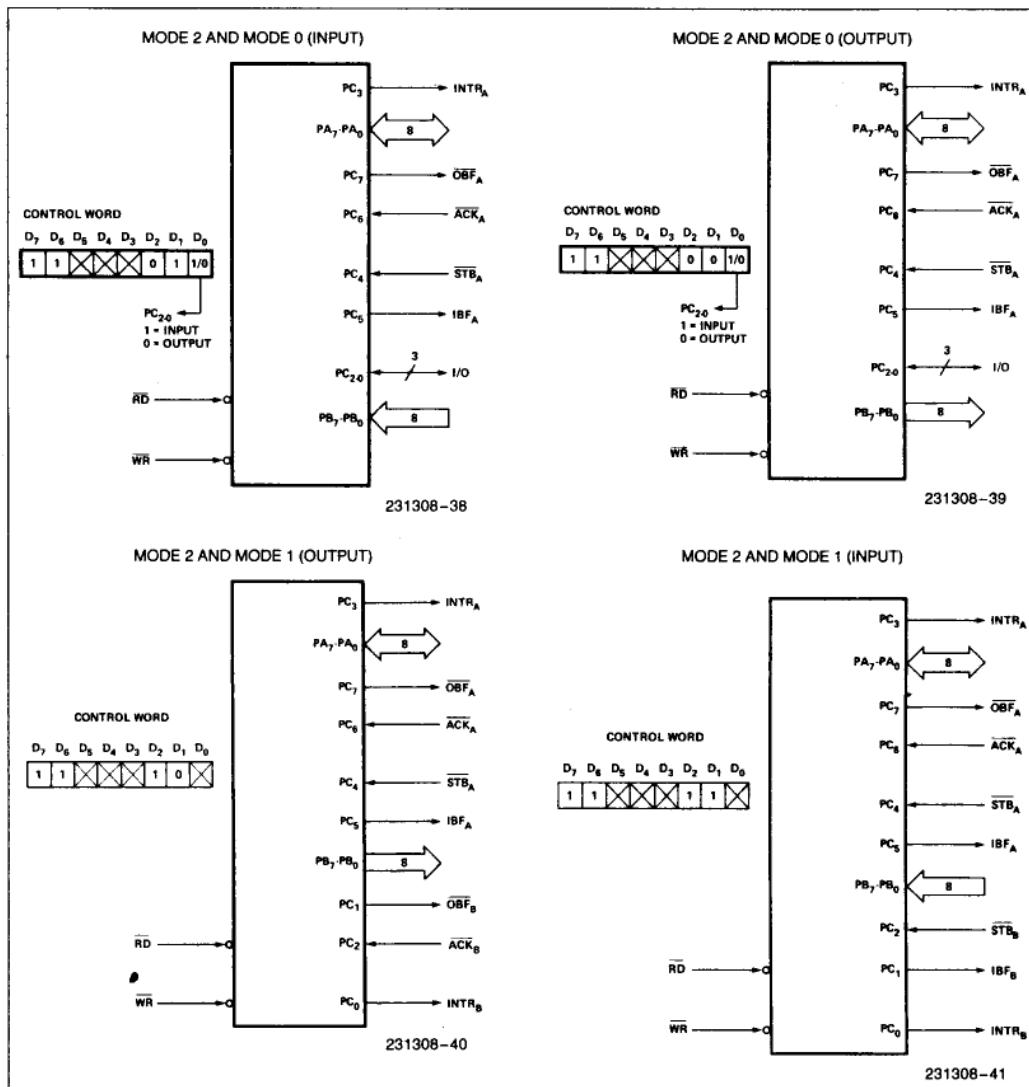


Figure 16. MODE 1/4 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA ₀	IN	OUT	IN	OUT	↔	
PA ₁	IN	OUT	IN	OUT	↔	
PA ₂	IN	OUT	IN	OUT	↔	
PA ₃	IN	OUT	IN	OUT	↔	
PA ₄	IN	OUT	IN	OUT	↔	
PA ₅	IN	OUT	IN	OUT	↔	
PA ₆	IN	OUT	IN	OUT	↔	
PA ₇	IN	OUT	IN	OUT	↔	
PB ₀	IN	OUT	IN	OUT	—	
PB ₁	IN	OUT	IN	OUT	—	
PB ₂	IN	OUT	IN	OUT	—	
PB ₃	IN	OUT	IN	OUT	—	
PB ₄	IN	OUT	IN	OUT	—	
PB ₅	IN	OUT	IN	OUT	—	
PB ₆	IN	OUT	IN	OUT	—	
PB ₇	IN	OUT	IN	OUT	—	
PC ₀	IN	OUT	INTR _B	INTR _B	I/O	
PC ₁	IN	OUT	IBF _B	OBF _B	I/O	
PC ₂	IN	OUT	STB _B	ACK _B	I/O	
PC ₃	IN	OUT	INTR _A	INTR _A	INTR _A	
PC ₄	IN	OUT	STB _A	I/O	STB _A	
PC ₅	IN	OUT	IBF _A	I/O	IBF _A	
PC ₆	IN	OUT	I/O	ACK _A	ACK _A	
PC ₇	IN	OUT	I/O	OBF _A	OBF _A	

MODE 0
OR MODE 1
ONLY

3

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs—

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs—

Bits in C upper (PC₇-PC₄) must be individually accessed using the bit set/reset function.

Bits in C lower (PC₃-PC₀) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1 mA at 1.5 volts.

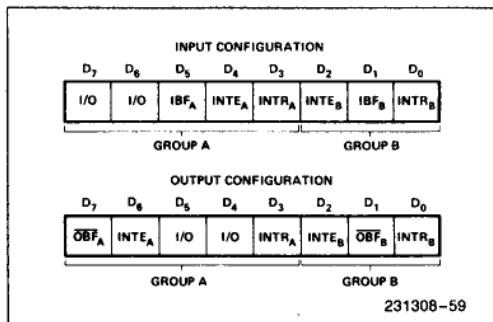


Figure 17. MODE 1 Status Word Format

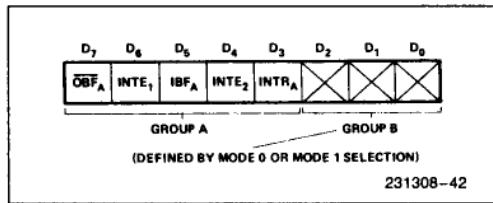


Figure 18. MODE 2 Status Word Format

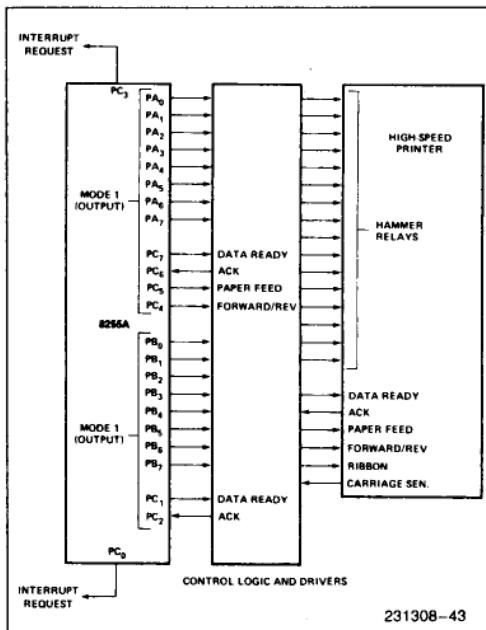


Figure 19. Printer Interface

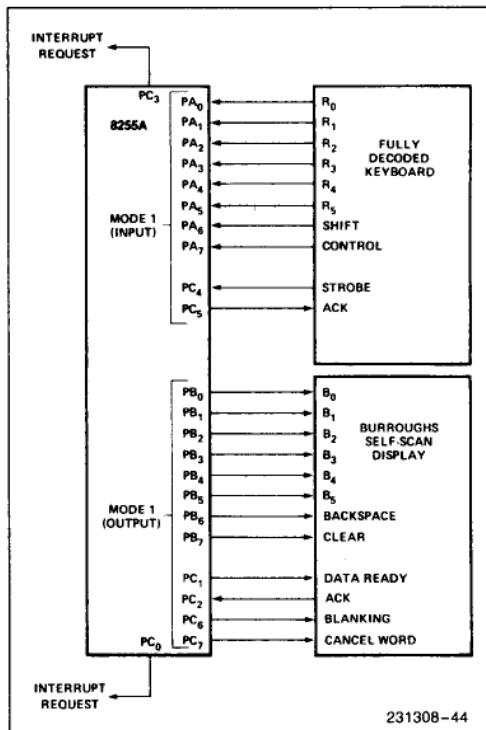
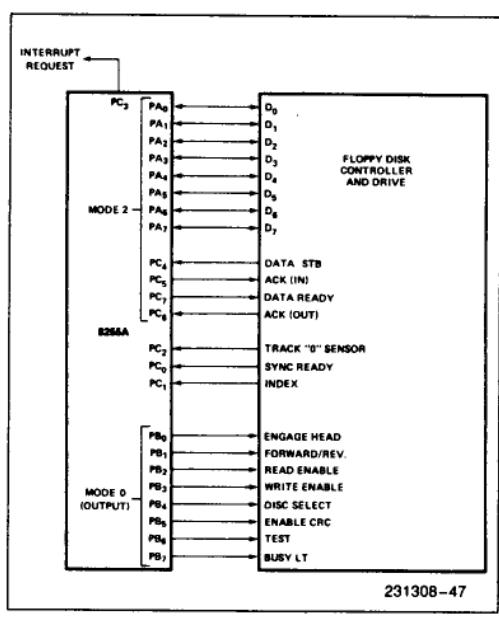
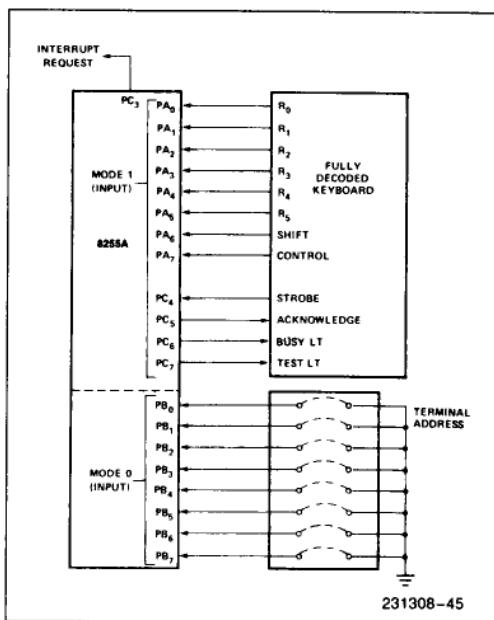
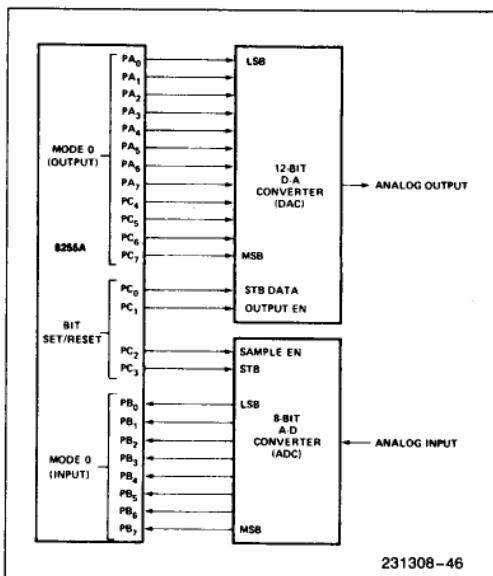
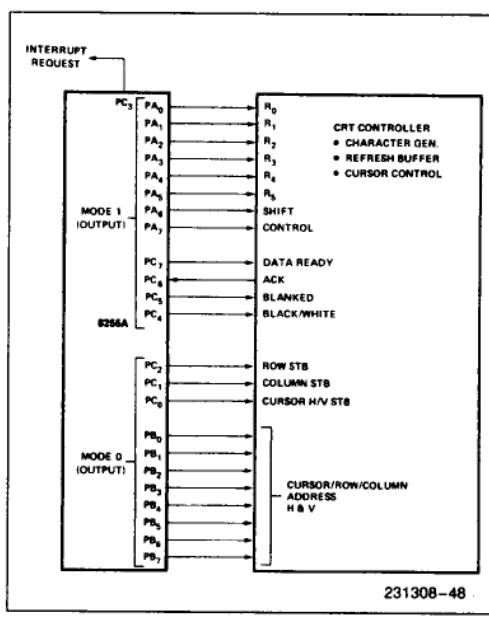


Figure 20. Keyboard and Display Interface



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Figure 23. Basic Floppy Disk Interface**Figure 22. Digital to Analog, Analog to Digital****Figure 24. Basic CRT Controller Interface**

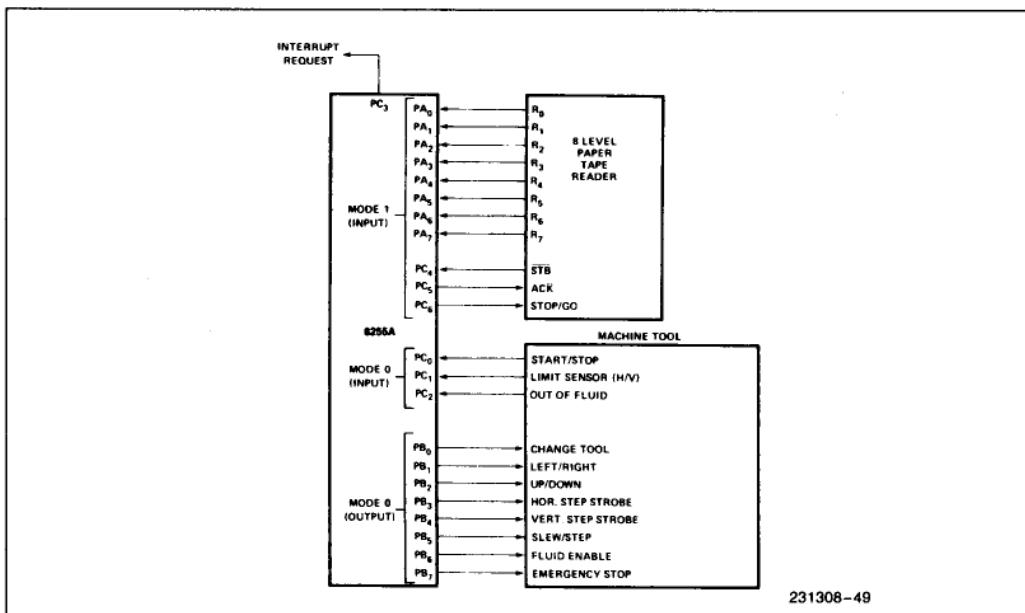


Figure 25. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to 70°C

Storage Temperature -65°C to +150°C

Voltage on Any Pin
with Respect to Ground -0.5V to +7V

Power Dissipation 1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{V} \pm 10\%$, $\text{GND} = 0\text{V}^*$

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
$V_{OL} (\text{DB})$	Output Low Voltage (Data Bus)		0.45*	V	$I_{OL} = 2.5\text{ mA}$
$V_{OL} (\text{PER})$	Output Low Voltage (Peripheral Port)		0.45*	V	$I_{OL} = 1.7\text{ mA}$
$V_{OH} (\text{DB})$	Output High Voltage (Data Bus)	2.4		V	$I_{OH} = -400\text{ }\mu\text{A}$
$V_{OH} (\text{PER})$	Output High Voltage (Peripheral Port)	2.4		V	$I_{OH} = -200\text{ }\mu\text{A}$
$I_{IDAR}^{(1)}$	Darlington Drive Current	-1.0	-4.0	mA	$R_{EXT} = 750\Omega$; $V_{EXT} = 1.5\text{V}$
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		± 10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		± 10	μA	$V_{OUT} = V_{CC}$ to 0.45V

NOTE:

1. Available on any 8 pins from Port B and C.

CAPACITANCE $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	$f_C = 1 \text{ MHz}^{(4)}$
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND ⁽⁴⁾

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{V} \pm 10\%$, $\text{GND} = 0\text{V}^*$

Bus Parameters

READ

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{AR}	Address Stable before READ	0		0		ns
t_{RA}	Address Stable after READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid from READ ⁽¹⁾		250		200	ns
t_{DF}	Data Float after READ	10	150	10	100	ns
t_{RV}	Time between READs and/or WRITEs	850		850		ns

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WRITE

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{AW}	Address Stable before WRITE	0		0		ns
t_{WA}	Address Stable after WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid after WRITE	30		30		ns

OTHER TIMINGS

Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{WB}	WR = 1 to Output ⁽¹⁾		350		350	ns
t_{IR}	Peripheral Data before RD	0		0		ns
t_{HR}	Peripheral Data after RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data before T.E. of STB	0		0		ns
t_{PH}	Per. Data after T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output ⁽¹⁾		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns

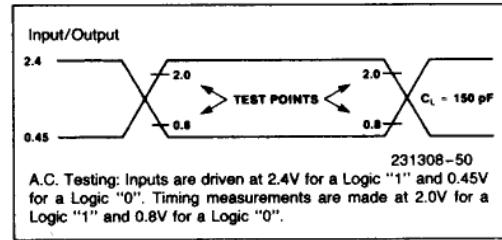
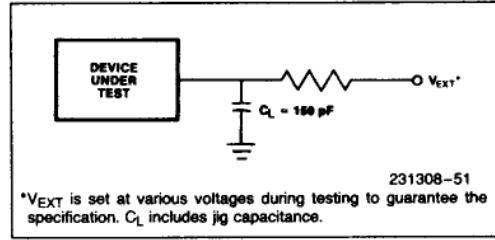
A.C. CHARACTERISTICS (Continued)**OTHER TIMINGS (Continued)**

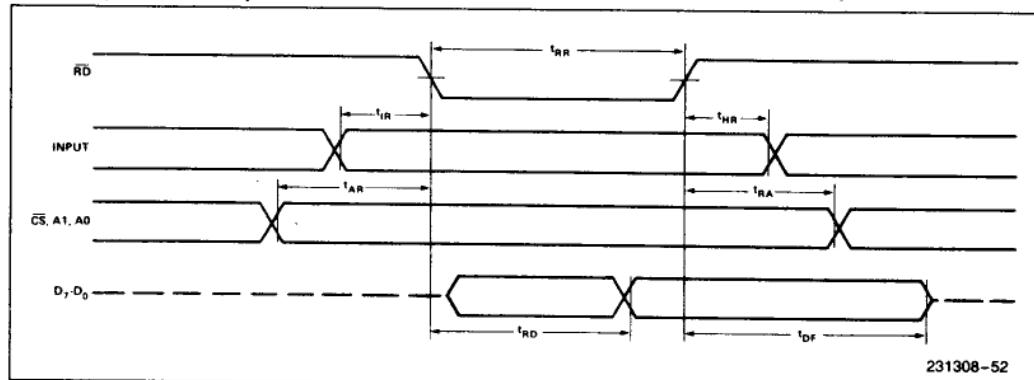
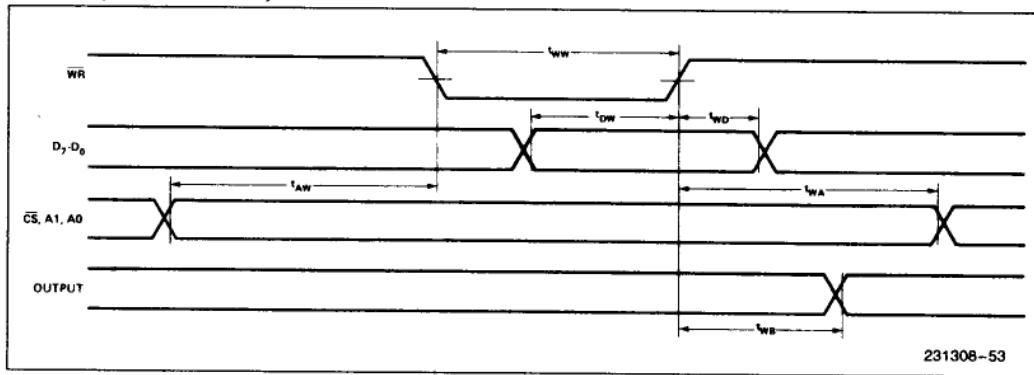
Symbol	Parameter	8255A		8255A-5		Unit
		Min	Max	Min	Max	
t_{WOB}	WR = 1 to OBF = 0(1)		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1(1)		350		350	ns
t_{SIB}	STB = 0 to IBF = 1(1)		300		300	ns
t_{RIB}	RD = 1 to IBF = 0(1)		300		300	ns
t_{RIT}	RD = 0 to INTR = 0(1)		400		400	ns
t_{SIT}	STB = 1 to INTR = 1(1)		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1(1)		350		350	ns
t_{WIT}	WR = 0 to INTR = 0(1, 3)		850		850	ns

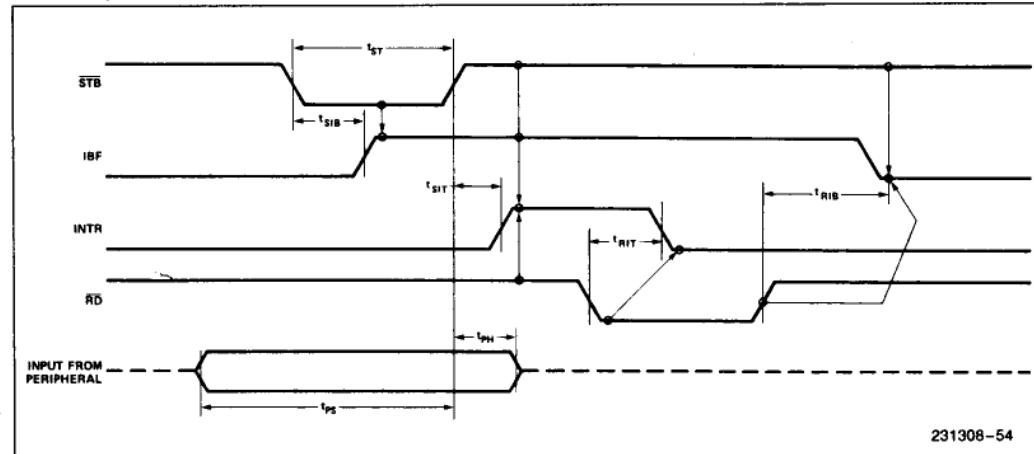
NOTES:

1. Test Conditions: $C_L = 150 \text{ pF}$.
2. Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR \uparrow may occur as early as $\overline{\text{WR}} \downarrow$.
4. Sampled, not 100% tested.

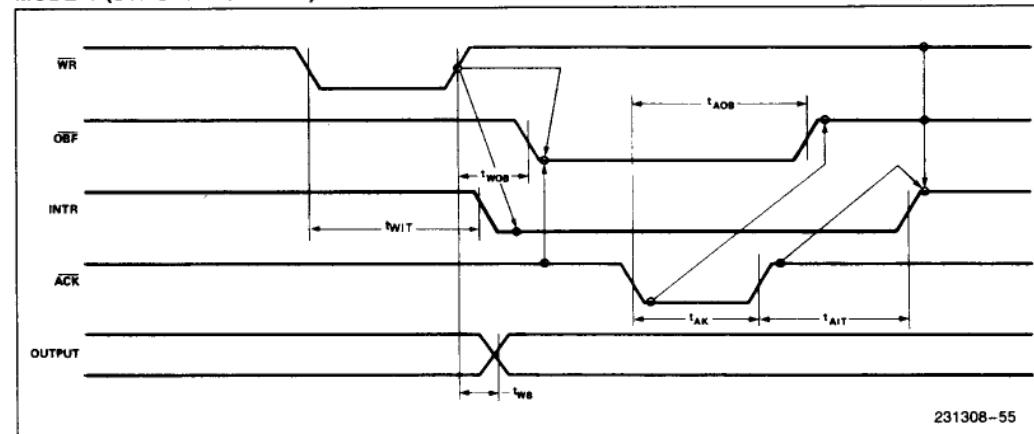
*For Extended Temperature EXPRESS, use M8255A electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM**A.C. TESTING LOAD CIRCUIT**

WAVEFORMS**MODE 0 (BASIC INPUT)****MODE 0 (BASIC OUTPUT)**

WAVEFORMS (Continued)**MODE 1 (STROBED INPUT)**

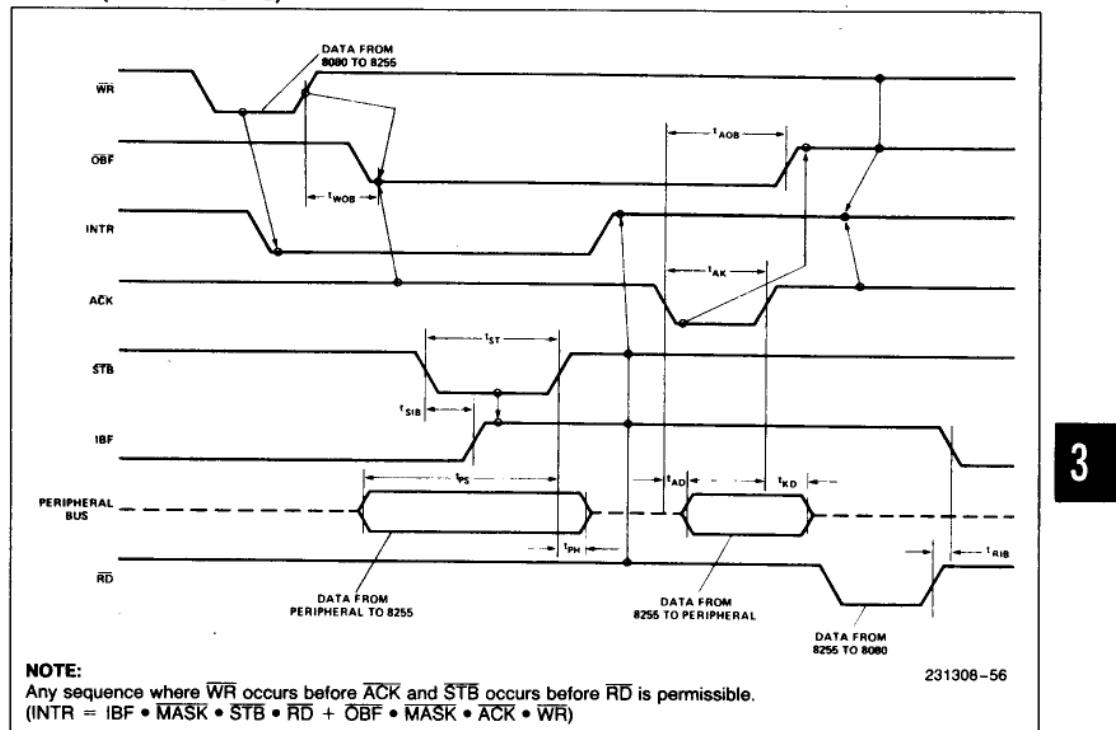
231308-54

MODE 1 (STROBED OUTPUT)

231308-55

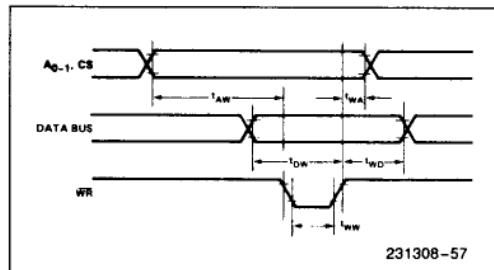
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)



3

WRITE TIMING



READ TIMING

