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We turn engineering into art

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C8051 Microcontroller

Overview

The C8051 is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C31. The C8051 serves software and hardware interrupts, provides an interface for serial communications and a timer system.

The C8051 is the microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking and with no internal tri-states. Reset is also synchronous. Therefore scan insertion is straightforward.

Applications

- 8-bit data processing applications
- Low power consumption applications
- Mixed-signal SoC control

Features

- Control Unit
  - Reduced instruction cycle time up to 12 times
- Arithmetic-Logic Unit
- 32-bit Input/Output ports
  - Four 8-bit I/O ports
  - Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- Two 16-bit Timer/Counters
- Serial Peripheral Interfaces in full duplex mode
  - Synchronous mode, fixed baud rate
  - 8-bit UART mode, variable baud rate
  - 9-bit UART mode, fixed baud rate
  - 9-bit UART mode, variable baud rate
  - Multiprocessor communication
- Interrupt Controller
  - Two Priority Levels
  - 5 interrupt sources
- Internal Data Memory interface
  - Can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface
  - Can address up to 64 KB of External Program Memory
  - Can address up to 64 KB of External Data Memory
  - De-multiplexed Address/Data Bus to allow easy connection to memories
  - Variable length MOVX to access fast/slow RAM/ or peripherals
  - Wait cycles to access fast/slow ROM
  - Dual data pointer register
  - Program Memory Write mode
- Special Function Registers interface
  - Services up to 103 External Special Function Registers
- Power Management Unit
  - Power management modes IDLE and STOP

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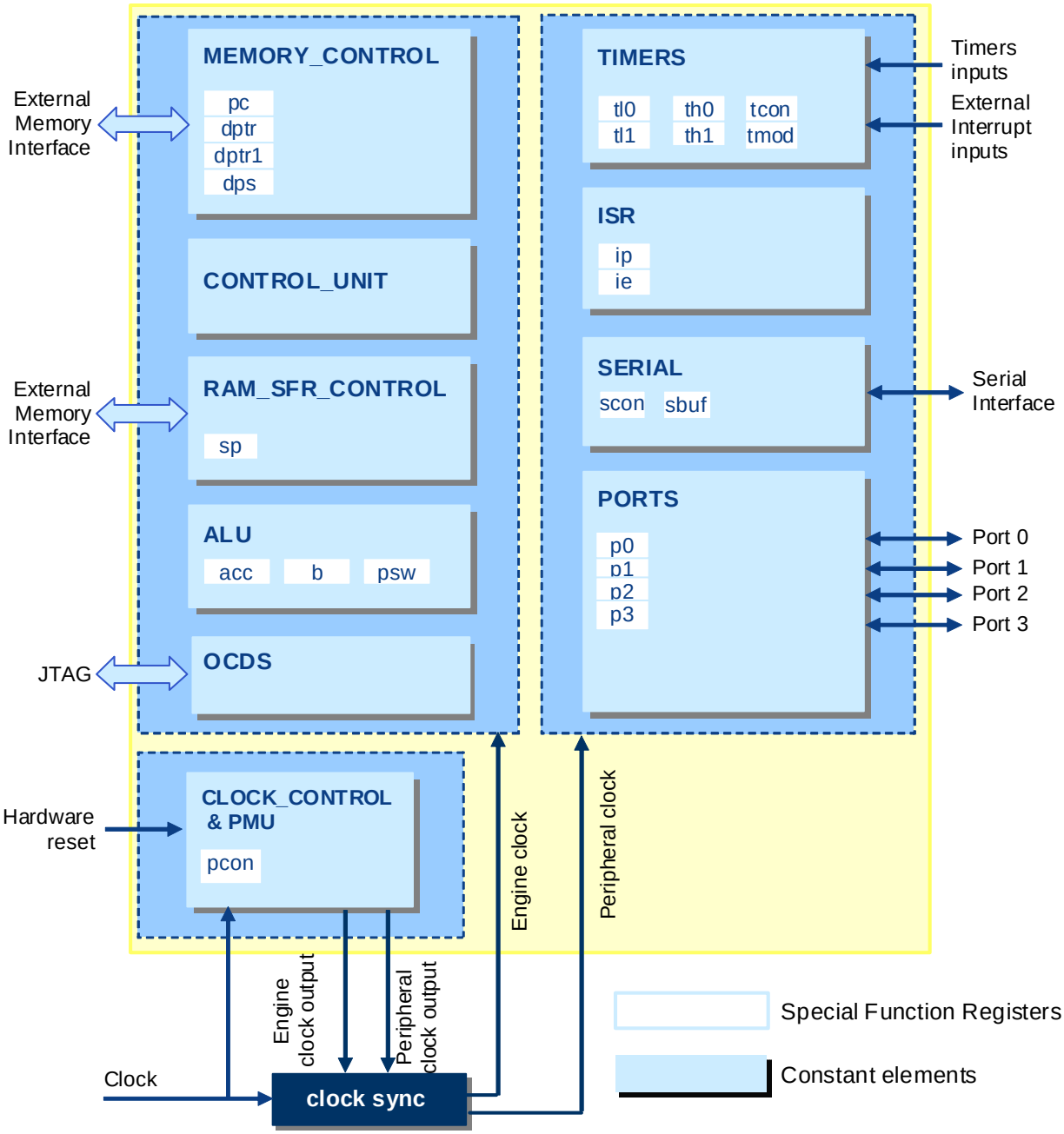
Block Diagram



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Functional Description

The C8051 core is partitioned into modules as shown in figure above and described below.

Control Processor Unit (CPU)

The C8051 CPU is composed of four components:

- Control unit
- Arithmetic-logic unit
- Memory control unit
- RAM and SFR control unit

The C8051 engine allows to fetch instruction from program memory and to execute using RAM or SFR.

The Arithmetic-logic unit serves:

- 8-bit arithmetic operations
- 8-bit logical operations
- Boolean manipulations
- 8 x 8-bit multiplication
- 8 / 8-bit division

The RAM and SFR control unit:

- Can address up to 256 bytes of Read/Write Data Memory Space
- Serves the Interface for off-core Special Function Registers

The Memory control unit:

- Can address up to 64 K bytes of External Program Memory Space
- Can address up to 64 K bytes of External Data Memory Space

Ports

Ports p0, p1, p2 and p3 are Special Function Registers. The contents of the SFR can be observed on corresponding pins on the chip. Writing a '1' to any of the ports causes the corresponding pin to be at high level (VCC), and writing a '0' causes the corresponding pin to be held at low level (GND). All four ports on the chip are bi-directional. Each of them consists of a Latch (SFR 'p0' to 'p3'), an output driver, and an input buffer, so the CPU can output or read data through any of these ports if they are not used for alternate purposes.

Clock Control & PMU

The Clock Control unit generates the internal synchronous reset. It also contains registers for selecting the clock for timers.

The PMU serves two power management modes IDLE and STOP.

Idle Mode: Setting the idle bit of pcon register invokes the IDLE mode. The IDLE mode leave internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

Stop Mode: Setting the stop bit of pcon register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state from a no-clocked external interrupt or a reset condition. Internally generated interrupts (timer, serial port ...) are not useful since they require clocking activity.

Serial

The serial buffer consists of two separate registers, a transmit buffer and a receive buffer. Writing data to the Special Function Register sbuf sets this data in serial output buffer and starts the transmission. Reading from the sbuf reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the first byte before transmission of the second byte is completed. The serial port can operate in 4 modes.

Timers 0 and 1

The C8051 has two 16-bit timer/counter registers: Timer 0 and Timer 1. Both can be configured for counter or timer operations. In timer mode, the register is incremented every machine cycle, which means that it counts up after every 12 oscillator periods. In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle (12 clock periods).

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (tmod and tcon) are used to select the appropriate mode.

Interrupt Service Routine

The C8051 provides 5 interrupt sources. There are 2 external interrupts accessible through pins int0 and int1, edge or level sensitive (falling edge or low level). There are, also, internal interrupts associated with Timer 0 and Timer 1, and an internal interrupt from the Serial Port.

OCDS

The OCDS unit serves interface for On-Chip Debug Support through an IEEE1149.1 (JTAG) port. The OCDS unit provides the following functions:

- Run, Stop, Single-step
- Software breakpoint
- Debugger program execution
- Hardware breakpoints
- Read/Write Access to Program Memory, External/Internal
- Data Memory and SFRs

Configurability

Additional parts of the system or modifications of core may be developed by Evatronix, according to the user's application. Please contact Evatronix directly to discuss any specific requirements.

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Performance

The C8051 is designed to run at frequencies up to 700 MHz on a typical 0.13-micron process. It uses less than 10K gates depending on the technology. The C8051 is a technology independent design that can be implemented in a variety of process technologies.

Performance	
MIPS	0,0094/MHz
Dhrystone	16,5/MHz
Wheatstone	1,8/MHz
Minimal area	--
Maximal speed	--
Power estimation (UMC 0.18): - Normal Operation - IDLE mode - STOP mode	 0.23 mW/MHz 0.??? mW/MHz 0.933 uW/MHz

Verification Methods

The C8051 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 chip, and the results compared with the core's simulation outputs.

The C8051 has been verified through extensive functional simulation and it has achieved high Code Coverage simulation results.

Code Coverage	Metric
Statement	100,00%
Branch	100,00%
Condition	95,60%
Triggering	89,2%
Path	69,4%
Toggle	98,4%

Pin Description

Name	Type	Polarity/ Bus size	Description
General signals			
clk	I	Rise	**Clock** pulse for internal clock counters and all synchronous circuits
clkcpu	I	Rise	**Engine clock** is a pulse for internal circuits, which are stopped when C8051 is in IDLE or STOP mode
clkcpuo	O	Rise/Low	**Engine clock output** is gated clk clock, it stays low when C8051 enters the IDLE or STOP mode. The clkcpuo is dedicated to be off-core connected to the clkcpu input.
clkper	I	Rise	**Peripheral clock** is a pulse for internal circuits, which are stopped when C8051 is in STOP mode.
clkpero	O	Rise/Low	**Peripheral clock** is gated clk clock, it stays low when C8051 enters into STOP mode. The clkpero is dedicated to be off-core connected to the clkper input.
reset	I	High	**Hardware reset input** A high on this pin for two clock cycles while the oscillator is running resets the device
ale	O	High	**Address Latch Enable:** The output pulse for latching the low byte of the Address during an access to external memory. In normal operations, 'ale' is driven at a constant rate of 1/6 the oscillator frequency.
ea	I	Low	**External Access Enable:** 'ea' must be externally held low to enable the device to fetch code from external program memory0000H and 0FFFH. If 'ea' is held high, the device executes from in-circuit program memory unless the Program counter contains an address greater than 0FFFH.
psen	O	Low	**Program Store Enable:** The read strobe to external program memory. When the C8051 is executing code from the external program memory, 'psen' is activated each machine cycle, 'psen' is not activated during fetches from in-circuit program memory.

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Pin Description (cont.)

Name	Type	Polarity/ Bus size	Description
Parallel Ports			
port0i port0o	I O	8 8	**Port 0** 8-bit bi-directional I/O port with separated inputs and outputs
port1i port1o	I O	8 8	**Port 1** 8-bit bi-directional I/O port with separated inputs and outputs
port2i port2o	I O	8 8	**Port 2** 8-bit bi-directional I/O port with separated inputs and outputs
port3i port3o	I O	8 8 Low Low High High Low Low - - -	**Port 3**: 8-bit bi-directional I/O port with separated inputs and outputs. Port 3 also serves the special features, as listed below: p3o.7 - rd: External data memory read strobe p3o.6 - wr: External data memory write strobe p3i.5 - t1: Timer 1 input p3i.4 - t0: Timer 0 input p3i.3 - int1: Ext. interrupt 1 p3i.2 - int0: Ext. interrupt 0 p3o.1 - txd0: Serial port 0 clock p3i.0 - rxd0i: Serial port 0 input p3o.0 - rxd0o: Serial port 0 output
Internal Program Memory interface			
romdatai romaddr romoe	I O O	8 14 High	Memory data input Memory address Data Memory enable
Internal Data Memory interface			
ramdatai ramdatao ramaddr ramwe ramoe	I O O O O	8 8 8 High High	Data bus input Data bus output Data file address Data file write enable Data file output enable
External Special Function Registers interface			
sfrdatai sfrdatao sfraddr sfrwe sfroe	I O O O O	8 8 7 High High	SFR data bus input SFR data bus output SFR address SFR write enable SFR output enable
Interface for On-Chip Instrumentation			
debugreq debugstep debugprog debugack flush fetch acc	I I I O O O O	High High High High High High 8	Debug mode request Debug mode single-step Debugger program select Debugger acknowledge signal Branch instruction fetch No-branch instruction fetch Accumulator register output

Standard Deliverables

- VHDL or Verilog source code for the C8051
- Synthesis support (Synopsys)
  A complete set of synthesis scripts
- Simulation support (MTI, Aldec, Cadence)
  A set of scripts and macros
- Example CHIP8051 – 8051 compatible design
  This design uses the C8051 and illustrates how to build and connect memories and port modules
- Extensive HDL Test Bench that instantiates:
  - Example design CHIP8051
  - External RAM
  - External ROM
  - Clock generator
  - Process that compares your simulation results with the expected results
- A collection of 8051 assembler programs which are executed directly by the Test Bench
- A set of expected results
- Additional documentation
  - Design Specification
  - Verification Specification and Test Plan
  - Integration Manual with User Guide
- Design support including consulting

Options

Typically the core is delivered as either VHDL or Verilog source code for ASIC implementations. Following options may be ordered according to user's requirements.

- EDIF netlist for FPGA and low volume production
- On-Chip debug support
- Reference design for propriety development board
- Annual maintenance
- On-site support

Third Party Reference

The C8051 core may be delivered with debug instrumentation implemented and ready to work with Keil debug environment.

Related Products

SPI-MS - Serial Peripheral Interface supporting slave as well as master capability with own rate generator and programmable polarity of serial clock. A dedicated set of slave selection signals facilitates integration in multi slave system;

I2C – controller which meets the original Philips I2C bus interface controller specification requirements. It may operate in one of the following transmission modes: Master Transmitter, Master Receiver, Slave Transmitter and Slave Receiver with transmission rates up to 400 kHz;

I2CS – controller compatible with the Philips I2C bus interface slave controller. It may operate in one of the following transmission modes: Slave Transmitter and Slave Receiver with transmission rates up to 400 kHz.

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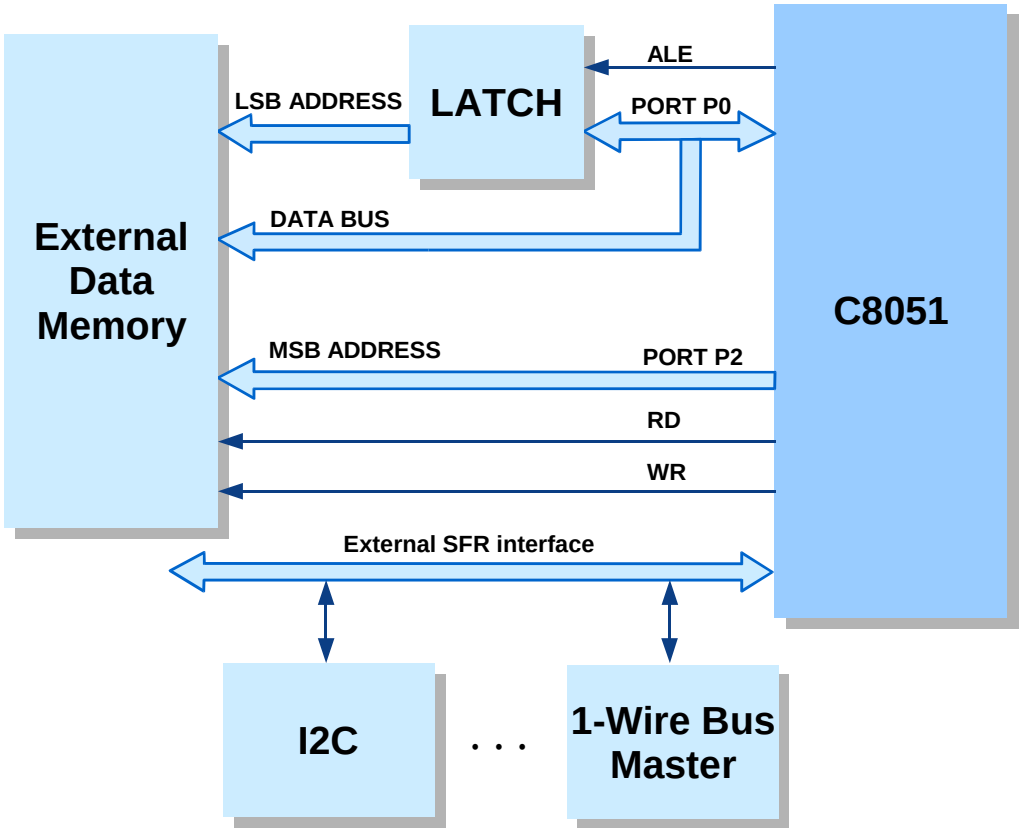
Example Application



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