

A Project Report on

**RTL2GDSII of Eight_Bit_Adder_using_Four_Bit_Adder
in Synopsys Tool**



SUBMITTED BY

Guntuku.Bhuvanchand
AP21110020092
Department of ECE-4th year
SRM University, AP

Contents

<u>s.no</u>	<u>Contents</u>	<u>Pg.no</u>
1	Introduction	3
2	Verilog Code for 8-bit Subtractor	4
3	RTL Synthesis	5-21
4	Floor planning	22-25
5	Power planning	26-31
6	Placement	32-42
7	Clock Tree Synthesis	43-58
8	Routing	59-75
9	Metal and vias	76-80
10	Timing Analysis	81-87
11	Exploring results	88-91
12	GDSII	92

1.Introduction:

- GDSII (Graphic Data Stream II) is a widely used file format in the semiconductor industry, crucial for sending design data to a foundry for the fabrication of integrated circuits (ICs).
- This format is in binary, ensuring efficient storage and transmission of complex design information.
- A GDSII file encapsulates all necessary details for IC fabrication, including the shapes and sizes of various components, input/output pins, power requirements, timing closure information, and more. This comprehensive data ensures that the IC can be manufactured to precise specifications.
- The process of creating a GDSII file is part of what is known as the ASIC (Application Specific Integrated Circuit) flow. This flow involves several steps, from initial design and simulation to final verification and file generation, ensuring the IC meets all performance and functional requirements.
- The ASIC flow is a semi-custom design process, balancing customization with standardization to optimize both performance and cost.
- For this particular project, we are employing 32nm technology, which refers to the feature size of the components on the IC. This technology node offers a balance between power efficiency and performance, suitable for a wide range of applications.

2.RTL Synthesis

RTL synthesis is the process of transforming HDL (Hardware Description Language) code into a gate-level mapped netlist. This netlist outlines the logical structure of the circuit using interconnected gates and is a critical step in the digital design flow.

- Write Verilog code for 8 bit adder using four bit adder in rtl directory in SRM_Workshop directory and save it as CLA1.v

```
module CLA8(
    input [3:0]a,b,
    input cin,
    output [3:0]sum,
    output cout
);

    assign {cout, sum} = a + b + cin;
endmodule

module CLA1 (
    input [7:0] a, b,
    input cin,clk,
    output [7:0] sum,
    output cout,
    output reg[7:0] fsum,
    output reg fcout
);
wire co;
    CLA8 A( a[3:0], b[3:0], cin, sum[3:0], co );
    CLA8 B( a[7:4], b[7:4], co, sum[7:4], cout);

    always @(posedge clk) begin
        fsum <= sum[7:0];
        fcout <= cout;
    end
endmodule
```

```
Compiler version V-2023.12_Full64; Runtime version V-2023.12_Full64; Jul 10 05:07 2024
Time =          0: a = 00000000, b = 00000000, cin = 0, fsum = xxxxxxxx, fcout = x
Time =          5: a = 00000000, b = 00000000, cin = 0, fsum = 00000000, fcout = 0
Time =         10: a = 00001111, b = 00000001, cin = 0, fsum = 00000000, fcout = 0
Time =         15: a = 00001111, b = 00000001, cin = 0, fsum = 00010000, fcout = 0
Time =         20: a = 11110000, b = 00001111, cin = 0, fsum = 00010000, fcout = 0
Time =         25: a = 11110000, b = 00001111, cin = 0, fsum = 11111111, fcout = 0
Time =         30: a = 01010101, b = 01010101, cin = 0, fsum = 11111111, fcout = 0
Time =         40: a = 11111111, b = 11111111, cin = 0, fsum = 11111111, fcout = 0
Time =         45: a = 11111111, b = 11111111, cin = 0, fsum = 11111110, fcout = 1
Time =         50: a = 00000000, b = 00000000, cin = 0, fsum = 11111110, fcout = 1
Time =         55: a = 00000000, b = 00000000, cin = 0, fsum = 00000000, fcout = 0
$stop at time 60 Scope: CLA1_tb File: CLA1.v Line: 67
```

```
File Edit View Terminal Tabs Help
[ws1_7@ws1 Desktop]$ cd SRM_Workshop/
[ws1_7@ws1 SRM_Workshop]$ ls
CONSTRAINTS DC ICCII PT ref rtl run_dc.tcl
[ws1_7@ws1 SRM_Workshop]$ cd rtl
[ws1_7@ws1 rtl]$ ls
CLA1.v full_adder_rtl.v novas.rc simv.daidir verdi_config_file VerdiLog
csrc novas.conf simv ucli.key verdilog vfastLog
[ws1_7@ws1 rtl]$ vi CLA1.v
```

- Reference Methodology

```
File Edit View Terminal Tabs Help
[ws1_7@ws1 Desktop]$ cd SRM_Workshop/
[ws1_7@ws1 SRM_Workshop]$ ls
CONSTRAINTS DC ICCII PT ref rtl run_dc.tcl
[ws1_7@ws1 SRM_Workshop]$ cd rtl
[ws1_7@ws1 rtl]$ ls
CLA1.v full_adder_rtl.v novas.rc simv.daidir verdi_config_file VerdiLog
csrc novas.conf simv ucli.key verdilog vfastLog
[ws1_7@ws1 rtl]$ cd ..
[ws1_7@ws1 SRM_Workshop]$ ls
CONSTRAINTS DC ICCII PT ref rtl run_dc.tcl
[ws1_7@ws1 SRM_Workshop]$ cd CONSTRAINTS/
[ws1_7@ws1 CONSTRAINTS]$ ls
CLA1.sdc full_adder.sdc
[ws1_7@ws1 CONSTRAINTS]$ cd ..
[ws1_7@ws1 SRM_Workshop]$ cd DC
[ws1_7@ws1 DC]$ ls
alib-52 command.log default.svf reports results rm_setup run_dc.tcl WORK
[ws1_7@ws1 DC]$ cd rm_setup/
[ws1_7@ws1 rm_setup]$ ls
common_setup.tcl dc_setup_filenames.tcl dc_setup.tcl
[ws1_7@ws1 rm_setup]$ vi common_setup.tcl
```

```

File Edit View Terminal Tabs Help
puts "RM-Info: Running script [info script]\n"

#####
# Variables common to all reference methodology scripts
# Script: common_setup.tcl
# Version: N-2017.09-SP4 (April 23, 2018)
# Copyright (C) 2007-2017 Synopsys, Inc. All rights reserved.
#####

set DESIGN_NAME          "CLA1" ;# The name of the top-level design
set PDK_PATH              "./../ref/" ; # to set the PDK path for the desi
gn
set DESIGN_REF_DATA_PATH  "" ;# Absolute path prefix variable for libr
ary/design data.
                                # Use this variable to prefix the common
absolute path
                                # to the common variables defined below.
                                # Absolute paths are mandatory for hiera
rchical
                                # reference methodology flow.

"common_setup.tcl" [dos] 79L 4835C 17.0-1 Top

```

Given design name as “CLA1”.

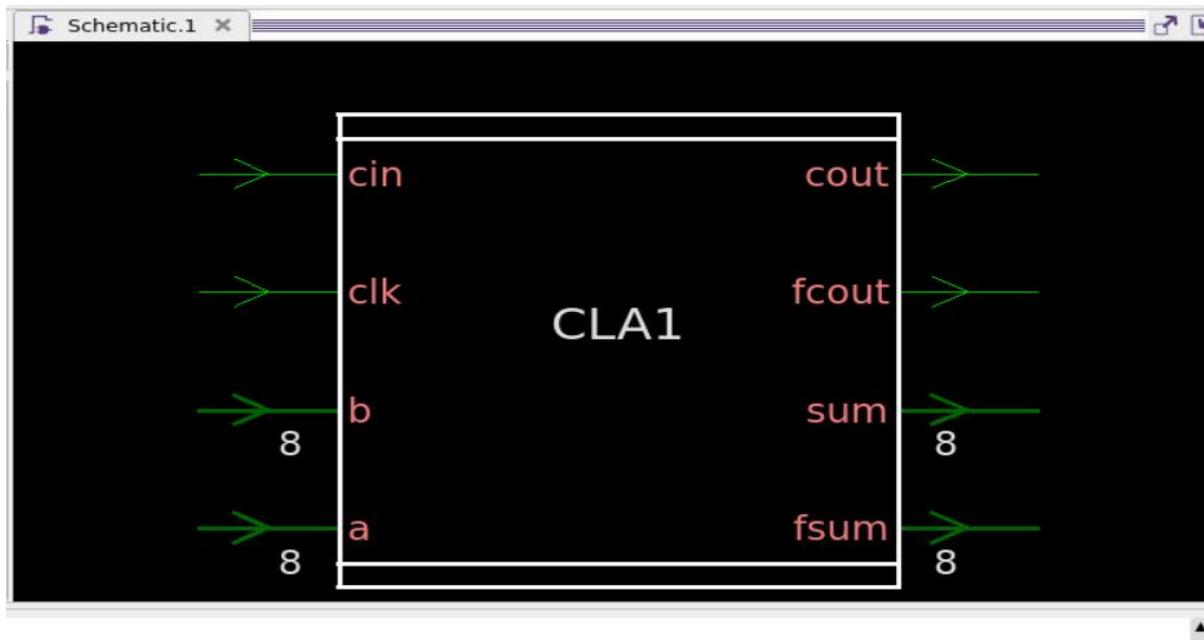
- In DC(Design Compiler), invoke dc_shell and execute run_dc.tcl script, Executed run_dc.tcl for Gate-level mapped netlist

```

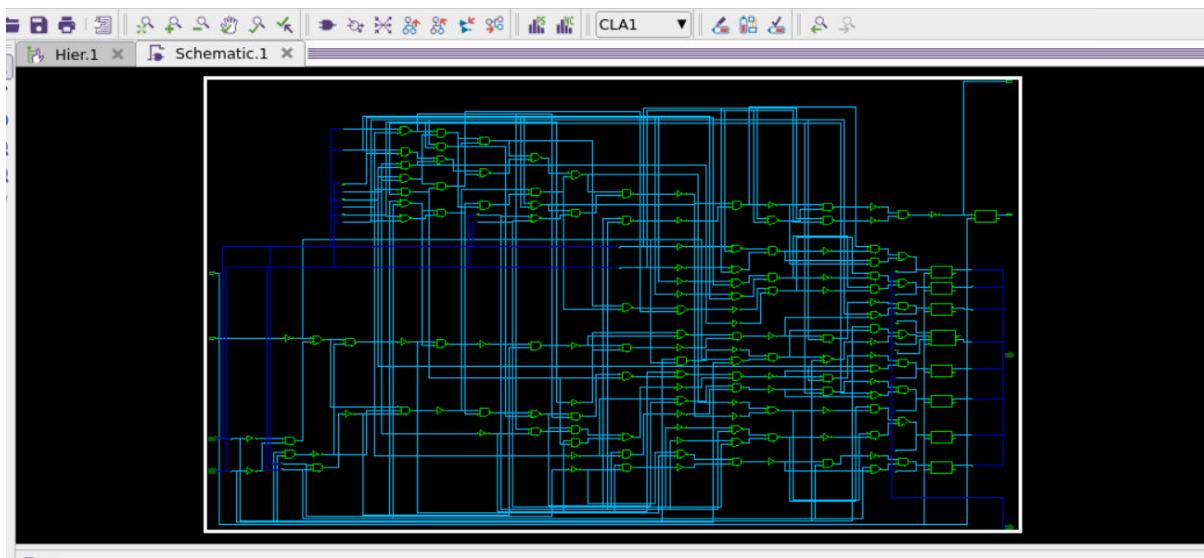
dc_shell> history
 1 start_gui
 2 source -echo -verbose ./rm_setup/dc_setup.tcl
 3 set RTL_SOURCE_FILES ./../rtl/CLA1.v
 4 set_dont_use [get_lib_cells */FADD*]
 5 set_dont_use [get_lib_cells */HADD*]
 6 set_dont_use [get_lib_cells */A0*]
 7 set_dont_use [get_lib_cells */OA*]
 8 set_dont_use [get_lib_cells */NAND*]
 9 set_dont_use [get_lib_cells */XOR*]
10 set_dont_use [get_lib_cells */NOR*]
11 set_dont_use [get_lib_cells */XNOR*]
12 set_dont_use [get_lib_cells */MUX*]
13 analyze -format verilog ${RTL_SOURCE_FILES}
14 elaborate ${DESIGN_NAME}
15 current_design
16 read_sdc ./../CONSTRAINTS/CLA1.sdc
17 compile_ultra
18 report_timing
19 report_qor
20 write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
21 history

```

Block diagram of Eight_bit_adder



Gate level diagram



SDC file – An SDC (Synopsys Design Constraints) file is a constraint file that outlines the limitations and requirements of a digital design.

```
File Edit View Terminal Tabs Help
create_clock -period 1 [get_ports clk]

set_input_delay -max 0.6 -clock [get_clocks clk] [all_inputs]
set_input_transition 0.15 [all_inputs]

set_output_delay -max 0.4 -clock [get_clocks clk] [all_outputs]

set_clock_uncertainty -setup -1.2 [get_clocks clk]
set_clock_uncertainty -hold -1 [get_clocks clk]

set_max_transition 0.250 [current_design]
set_max_transition -clock_path 0.100 [get_clocks clk]
~
```

‘Analyze & elaborate’ commands

```
dc_shell> analyze -format verilog ${RTL_SOURCE_FILES}
Running PRESTO HDLC
Compiling source file ../../rtl/CLA1.v
Presto compilation completed successfully.
1
dc_shell> elaborate ${DESIGN_NAME}
Loading db file '/usr/synopsys/syn/V-2023.12/libraries/syn/gtech.db'
Loading db file '/usr/synopsys/syn/V-2023.12/libraries/syn/standard.sldb'
  Loading link library 'gtech'
Running PRESTO HDLC

Inferred memory devices in process
  in routine CLA1 line 23 in file
    '../../rtl/CLA1.v'.
=====
|   Register Name   |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
```

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
fsum_reg	Flip-flop	8	Y	N	N	N	N	N	N
fcout_reg	Flip-flop	1	N	N	N	N	N	N	N

```
=====
Presto compilation completed successfully. (CLA1)
Elaborated 1 design.
Current design is now 'CLA1'.
Information: Building the design 'CLA8'. (HDL-193)
Presto compilation completed successfully. (CLA8)
```

‘Compile_ultra’ employs advanced techniques to optimize power, performance and area efficiency.

```
File Edit View Terminal Tabs Help
Current design is 'CLA1'.
dc_shell> dc_shell> current_design
Current design is 'CLA1'.
{CLA1}
dc_shell>
dc_shell> read_sdc ../../CONSTRAINTS/CLA1.sdc

Reading SDC version 2.1...
Current design is 'CLA1'.
l
dc_shell>
dc_shell> compile_ultra
Information: Performing leakage power optimization. (PWR-850)
CPU Load: 56%, Ram Free: 0 GB, Swap Free: 11 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
Alib files are up-to-date.
Information: Evaluating DesignWare library utilization. (UISN-27)

=====
| DesignWare Building Block Library | Version | Available |
=====
| Basic DW Building Blocks | V-2023.12-DWBB_202312.0 | * |
| Licensed DW Building Blocks | V-2023.12-DWBB_202312.0 | * |
=====

=====
| Flow Information |
|-----|
| Flow | Design Compiler WLM
| Command Line | compile_ultra
|-----|
| Design Information | Value |
|-----|
| Number of Scenarios | 0
| Leaf Cell Count | 13
| Number of User Hierarchies | 2
| Sequential Cell Count | 9
| Macro Count | 0
|-----|
File Edit View Terminal Tabs Help
=====
| Flow Information |
|-----|
| Flow | Design Compiler WLM
| Command Line | compile_ultra
|-----|
| Design Information | Value |
|-----|
| Number of Scenarios | 0
| Leaf Cell Count | 13
| Number of User Hierarchies | 2
| Sequential Cell Count | 9
| Macro Count | 0
| Number of Power Domains | 0
| Number of Path Groups | 2
| Number of VT Class | 1
| Number of Clocks | 1
| Number of Dont Touch Cells | 0
| Number of Dont Touch Nets | 0
| Number of Size Only Cells | 0
| Design with UPF Data | false
|-----|
Information: Sequential output inversion is enabled. SVF file must be used for formal verification. (OPT-1208)
Information: Uniquified 2 instances of design 'CLA8'. (OPT-1056)
Simplifying Design 'CLA1'

Loaded alib file './alib-52/saed32rvt_tt0p78vn40c.db.alib'
Building model 'DW01_NAND2'
Information: Ungrouping hierarchy A before Pass 1 (OPT-776)
Information: Ungrouping hierarchy B before Pass 1 (OPT-776)
Information: Ungrouping 2 of 3 hierarchies before Pass 1 (OPT-775)
CPU Load: 56%, Ram Free: 0 GB, Swap Free: 11 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
Information: State dependent leakage is now switched from on to off.

Beginning Pass 1 Mapping
-----
Processing 'CLA1'
```

```
File Edit View Terminal Tabs Help
Information: State dependent leakage is now switched from on to off.

Beginning Pass 1 Mapping
-----
Processing 'CLAI'
Implement Synthetic for 'CLAI'.
CPU Load: 56%, Ram Free: 0 GB, Swap Free: 11 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB

Updating timing information
Information: Updating design information... (UID-85)
Information: The library cell 'PMT3_RVT' in the library 'saed32rvt_tt0p78vn40c' is not characterized for internal power. (PWR-536)
Information: The library cell 'PMT2_RVT' in the library 'saed32rvt_tt0p78vn40c' is not characterized for internal power. (PWR-536)
Information: The library cell 'PMT1_RVT' in the library 'saed32rvt_tt0p78vn40c' is not characterized for internal power. (PWR-536)
Information: The library cell 'NMT3_RVT' in the library 'saed32rvt_tt0p78vn40c' is not characterized for internal power. (PWR-536)
Information: The library cell 'NMT2_RVT' in the library 'saed32rvt_tt0p78vn40c' is not characterized for internal power. (PWR-536)
Information: The library cell 'NMT1_RVT' in the library 'saed32rvt_tt0p78vn40c' is not characterized for internal power. (PWR-536)
Information: The target library(s) contains cell(s), other than black boxes, that are not characterized for internal power. (PWR-24)
```

```
Threshold voltage group cell usage:
>> saed32cell_svt 100.00%
```

```
Beginning Mapping Optimizations (Ultra High effort)
-----
Mapping Optimization (Phase 1)
Information: Added key list 'DesignWare' to design 'CLAI'. (DDB-72)
```

ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST	ENDPOINT	LEAKAGE POWER
0:00:04	382.2	0.42	2.7	44.4		826785.9375
0:00:04	380.7	0.42	2.7	44.4		821279.9375

```
Threshold voltage group cell usage:
>> saed32cell_svt 100.00%
```

```
File Edit View Terminal Tabs Help
```

```
Threshold voltage group cell usage:
>> saed32cell_svt 100.00%
```

```
Beginning Constant Register Removal
```

0:00:04	380.7	0.42	2.7	44.4	821279.9375
0:00:04	380.7	0.42	2.7	44.4	821279.9375

```
Threshold voltage group cell usage:
>> saed32cell_svt 100.00%
```

```
Beginning Global Optimizations
```

```
-----
Numerical Synthesis (Phase 1)
Numerical Synthesis (Phase 2)
Global Optimization (Phase 1)
Global Optimization (Phase 2)
Global Optimization (Phase 3)
Global Optimization (Phase 4)
Global Optimization (Phase 5)
Global Optimization (Phase 6)
Global Optimization (Phase 7)
Global Optimization (Phase 8)
Global Optimization (Phase 9)
Global Optimization (Phase 10)
Global Optimization (Phase 11)
Global Optimization (Phase 12)
Global Optimization (Phase 13)
Global Optimization (Phase 14)
Global Optimization (Phase 15)
Global Optimization (Phase 16)
Global Optimization (Phase 17)
Global Optimization (Phase 18)
Global Optimization (Phase 19)
Global Optimization (Phase 20)
Global Optimization (Phase 21)
```

```

File Edit View Terminal Tabs Help
Global Optimization (Phase 22)
Global Optimization (Phase 23)
Global Optimization (Phase 24)
Global Optimization (Phase 25)
Global Optimization (Phase 26)
Global Optimization (Phase 27)
Global Optimization (Phase 28)
Global Optimization (Phase 29)
Global Optimization (Phase 30)

Threshold voltage group cell usage:
>> saed32cell_svt 100.00%

Beginning Isolate Ports
-----

Threshold voltage group cell usage:
>> saed32cell_svt 100.00%

Beginning Delay Optimization
-----
0:00:04    280.1    0.45    2.0    0.0      592029.0625
0:00:05    304.2    0.33    1.7    0.0      687485.5625
0:00:05    304.2    0.33    1.7    0.0      687485.5625
0:00:05    304.2    0.33    1.7    0.0      687485.5625

Threshold voltage group cell usage:
>> saed32cell_svt 100.00%
0:00:05    304.2    0.33    1.7    0.0      687485.5625
0:00:05    304.2    0.33    1.7    0.0      687485.5625

Beginning WLM Backend Optimization
-----
0:00:05    291.0    0.33    1.4    0.0      606664.0625

```

Terminal - wsl_7@wsl:~/Desktop/SRM_Workshop/DC

```

File Edit View Terminal Tabs Help
0:00:05    304.2    0.33    1.7    0.0      687485.5625
0:00:05    304.2    0.33    1.7    0.0      687485.5625

Beginning WLM Backend Optimization
-----
0:00:05    291.0    0.33    1.4    0.0      606664.0625
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:05    290.5    0.33    1.4    0.0      599067.8125
0:00:06    308.5    0.27    1.0    49.8     627812.9375
0:00:06    308.5    0.27    1.0    49.8     627812.9375
0:00:06    308.3    0.25    1.0    49.8     626017.0625
0:00:06    308.3    0.25    1.0    49.8     626017.0625
0:00:07    332.7    0.12    0.3    0.0      646280.8125
0:00:07    332.7    0.12    0.3    0.0      646280.8125
0:00:07    332.4    0.10    0.3    0.0      645310.9375
0:00:07    332.4    0.10    0.3    0.0      645310.9375
0:00:07    355.5    0.09    0.2    0.0      660714.5625
0:00:07    355.5    0.09    0.2    0.0      660714.5625
0:00:08    347.2    0.07    0.2    0.0      632677.0000
0:00:08    347.2    0.07    0.2    0.0      632677.0000
0:00:08    365.0    0.05    0.1    0.0      666033.0000
0:00:08    365.0    0.05    0.1    0.0      666033.0000
0:00:09    364.4    0.05    0.1    0.0      664388.6875
0:00:09    364.4    0.05    0.1    0.0      664388.6875
0:00:10    367.7    0.03    0.0    0.0      663248.5625
0:00:10    374.1    0.02    0.0    0.0      693218.3125
0:00:10    374.1    0.02    0.0    0.0      693218.3125

Threshold voltage group cell usage:
>> saed32cell_svt 100.00%

```

Beginning Leakage Power Optimization (max_leakage_power 0)												
ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST	ENDPOINT	LEAKAGE POWER						
0:00:10	374.1	0.02	0.0	0.0		693218.3125						
0:00:10	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:11	374.1	0.02	0.0	0.0		693218.3125						
0:00:12	374.1	0.02	0.0	0.0		693218.3125						
0:00:12	374.1	0.02	0.0	0.0		693218.3125						
0:00:12	373.6	0.01	0.0	0.0		691574.0000						
0:00:12	373.6	0.01	0.0	0.0		691574.0000						
0:00:12	373.6	0.01	0.0	0.0		691574.0000						
0:00:12	373.6	0.01	0.0	0.0		691574.0000						
0:00:12	373.6	0.01	0.0	0.0		691574.0000						
0:00:12	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:13	373.6	0.01	0.0	0.0		691574.0000						
0:00:14	373.6	0.01	0.0	0.0		691574.0000						
ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST	ENDPOINT	LEAKAGE POWER						
0:00:14	373.6	0.01	0.0	0.0		691574.0000						
0:00:14	314.6	0.02	0.0	0.0		528806.0625						
0:00:14	312.1	0.01	0.0	0.0		532680.4375						
0:00:14	312.1	0.01	0.0	0.0		532680.4375						
0:00:14	312.1	0.01	0.0	0.0		532680.4375						
0:00:14	312.1	0.01	0.0	0.0		532680.4375						
0:00:14	312.3	0.01	0.0	0.0		536478.5625						
0:00:14	312.3	0.01	0.0	0.0		536478.5625						
0:00:14	312.3	0.01	0.0	0.0		536478.5625						
0:00:14	312.3	0.01	0.0	0.0		536478.5625						
0:00:14	312.3	0.01	0.0	0.0		536478.5625						
0:00:14	312.3	0.01	0.0	0.0		536478.5625						
U Load: 57%, Ram Free: 0 GB, Swap Free: 11 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB												
Reading db file '/ve/ws_home/ws1_7/Desktop/SRM_Workshop/ref/lib/stdcell_rvt/saed32rvt_tt0p78v												
Note: Symbol # after min delay cost means estimated hold TNS across all active scenarios												
Optimization Complete												
Information: State dependent leakage is now switched from off to on.												
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)												
U Load: 57%, Ram Free: 0 GB, Swap Free: 11 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB												
Information: Total number of MV cells in the design.												

```
Information: State dependent coverage is now switched from off to on...
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
CPU Load: 57%, Ram Free: 0 GB, Swap Free: 11 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
Information: Total number of MV cells in the design.

-----  
MV Cells          Total Number  
-----  
Level Shifter:      0  
Enable Level Shifter: 0  
Isolation Cell:     0  
Retention Cell:      0  
Retention Clamp Cell: 0  
Switch Cell:        0  
Always-On Cell:      0  
Repeater Cell:       0  
-----  
Unmapped MV Cells  
-----  
0 Isolation Cells are unmapped  
0 Retention Clamp Cells are unmapped  
-----  
1  
Current design is 'CLA1'.  
dc_shell> dc_shell> report_timing  
Information: Updating design information... (UID-85)  
*****  
Report : timing  
        -path full  
        -delay max  
        -max_paths 1  
Design : CLA1  
Version: V-2023.12  
Date   : Wed Jul 10 06:33:48 2024  
*****
```

‘report_qor’ known as Quality of Results, provides an overview of various parameters including design, area, power, and timing

```
1
dc_shell> report_qor
*****
Report : qor
Design : CLA1
Version: V-2023.12
Date   : Wed Jul 10 06:37:24 2024
*****


Timing Path Group 'clk'
-----
Levels of Logic:          15.00
Critical Path Length:    1.19
Critical Path Slack:     0.01
Critical Path Clk Period: 1.00
Total Negative Slack:    0.00
No. of Violating Paths:  0.00
Worst Hold Violation:   0.00
Total Hold Violation:   0.00
No. of Hold Violations: 0.00
-----


Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count:         152
Buf/Inv Cell Count:      48
Buf Cell Count:          0
Inv Cell Count:          48
CT Buf/Inv Cell Count:  0
Combinational Cell Count: 142
```

```

File Edit View Terminal Tabs Help
No. of Violating Paths: 0.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00
-----
Cell Count
-----
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 152
Buf/Inv Cell Count: 48
Buf Cell Count: 0
Inv Cell Count: 48
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 143
Sequential Cell Count: 9
Macro Count: 0
-----
Area
-----
Combinational Area: 254.398154
Noncombinational Area: 59.977986
Buf/Inv Area: 60.994560
Total Buffer Area: 0.00
Total Inverter Area: 60.99
Macro/Black Box Area: 0.000000
Net Area: 44.103603
-----
Cell Area: 314.376140
Design Area: 358.479742
-----
Design Rules
-----
Total Number of Nets: 172
Nets With Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0
-----
Hostname: ws1.trg.vlsiexpert.in
Compile CPU Statistics
-----
Resource Sharing: 0.00
Logic Optimization: 0.31
Mapping Optimization: 0.44
-----
Overall Compile Time: 5.28
Overall Compile Wall Clock Time: 9.76
-----
Design WNS: 0.00 TNS: 0.00 Number of Violating Paths: 0
Design (Hold) WNS: 0.00 TNS: 0.00 Number of Violating Paths: 0
-----
1
dc_shell> write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
Writing verilog file '/ve/ws home/ws1 7/Desktop/SRM Workshop/DC/results/CLAl.mapped.v'.

```

‘report_timing’ This command generates detailed timing reports for synthesized design like slack, delay and timing path.

```

File Edit View Terminal Tabs Help
Current design is 'CLA1'.
dc_shell> report_timing
Information: Updating design information... (UID-85)
*****
Report : timing
  -path full
  -delay max
  -max_paths 1
Design : CLA1
Version: V-2023.12
Date   : Wed Jul 10 06:36:43 2024
*****
Operating Conditions: tt0p78vn40c Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

Startpoint: a[0] (input port clocked by clk)
Endpoint: sum[4] (output port clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----              -----               -----
CLA1                8000                 saed32rvt_tt0p78vn40c

Point           Incr      Path
-----          -----
clock clk (rise edge)    0.00     0.00
clock network delay (ideal) 0.00     0.00
input external delay      0.60     0.60 f
a[0] (in)            0.00     0.60 f
U88/Y (INVX0_RVT)      0.10     0.70 r
U145/Y (AND2X1_RVT)    0.10     0.80 r
U146/Y (OR2X1_RVT)     0.08     0.88 r
U149/Y (AND3X1_RVT)    0.09     0.97 r
U109/Y (INVX0_RVT)     0.05     1.02 f
U188/Y (AND2X1_RVT)    0.08     1.10 f
U189/Y (OR2X1_RVT)     0.11     1.20 f
U190/Y (AND2X1_RVT)    0.09     1.29 f
U191/Y (OR2X1_RVT)     0.09     1.39 f
U192/Y (OR2X1_RVT)     0.08     1.47 f
U197/Y (AND2X1_RVT)    0.08     1.54 f
U101/Y (INVX0_RVT)     0.05     1.60 r
U198/Y (AND2X1_RVT)    0.08     1.68 r
U128/Y (INVX0_RVT)     0.04     1.72 f
U200/Y (AND2X1_RVT)    0.07     1.79 f
sum[4] (out)           0.00     1.79 f
data arrival time       1.79

clock clk (rise edge)    1.00     1.00
clock network delay (ideal) 0.00     1.00
clock uncertainty        1.20     2.20
output external delay     -0.40    1.80
data required time        1.80
data arrival time         -1.79

slack (MET)             0.01

```

Now we saved the gate-level mapped netlist file into results directory of DC directory. I assign name as '**CLA1.mapped.v**'

File location

```
File Edit View Terminal Tabs Help
-----
Resource Sharing:          0.00
Logic Optimization:        0.31
Mapping Optimization:      0.44
-----
Overall Compile Time:      5.28
Overall Compile Wall Clock Time: 9.76
-----
Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0
Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0
-----
1
dc_shell> write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
Writing verilog file '/ve/ws_home/ws1_7/Desktop/SRM_Workshop/DC/results/CLA1.mapped.v'.
1
dc_shell> quit
dc_shell> quit

Memory usage for this session 201 Mbytes.
Memory usage for this session including child processes 201 Mbytes.
CPU usage for this session 87 seconds ( 0.02 hours ).
Elapsed time for this session 1953 seconds ( 0.54 hours ).

Thank you...
[ws1_7@ws1 DC]$ ls
alib-52 command.log default.svf  reports  results  rm_setup  run_dc.tcl  WORK
[ws1_7@ws1 DC]$ cd results/
[ws1_7@ws1 results]$ ls
CLA1.mapped.v  eight_bit_adder.mapped.v  full_adder.mapped.v
[ws1_7@ws1 results]$ █

terminal - ws1_7@ws1:~/Desktop/SRM_Workshop/DC/results
File Edit View Terminal Tabs Help
[ws1_7@ws1 DC]$ cd SRM
bash: cd: SRM: No such file or directory
[ws1_7@ws1 DC]$ cd ..
[ws1_7@ws1 SRM_Workshop]$ ls
CONSTRAINTS  DC  ICCII  PT  ref  rtl  run_dc.tcl
[ws1_7@ws1 SRM_Workshop]$ cd DC/
[ws1_7@ws1 DC]$ ls
alib-52  CLA1-verilog.pvl  CLA8-verilog.pvl  default.svf  results  WORK
cksum_dir  CLA1-verilog.syn  CLA8-verilog.syn  filenames.log  rm_setup
CLA1.mr  CLA8.mr  command.log  reports  run_dc.tcl
[ws1_7@ws1 DC]$ cd results
[ws1_7@ws1 results]$ ls
CLA1.mapped.v  eight_bit_adder.mapped.v  full_adder.mapped.v
[ws1_7@ws1 results]$ vi CLA1.mapped.v █
```

CLA1.mapped.v file

```
File Edit View Terminal Tabs Help
//////////////////////////////////////////////////////////////////
// Created by: Synopsys DC Ultra(TM) in wire load mode
// Version   : V-2023.12
// Date      : Wed Jul 10 06:38:21 2024
//////////////////////////////////////////////////////////////////

module CLA1 ( a, b, cin, clk, sum, cout, fsum, fcout );
  input [7:0] a;
  input [7:0] b;
  output [7:0] sum;
  output [7:0] fsum;
  input cin, clk;
  output cout, fcout;
  wire n215, n216, n217, n218, n219, n220, n221, n222, n223, n224, n225,
        n226, n227, n228, n229, n230, n231, n232, n233, n234, n235, n236,
        n237, n238, n239, n240, n241, n242, n243, n244, n245, n246, n247,
        n248, n249, n250, n251, n252, n253, n254, n255, n256, n257, n258,
        n259, n260, n261, n262, n263, n264, n265, n266, n267, n268, n269,
        n270, n271, n272, n273, n274, n275, n276, n277, n278, n279, n280,
        n281, n282, n283, n284, n285, n286, n287, n288, n289, n290, n291,
        n292, n293, n294, n295, n296, n297, n298, n299, n300, n301, n302,
        n303, n304, n305, n306, n307, n308, n309, n310, n311, n312, n313,
        n314, n315, n316, n317, n318, n319, n320, n321, n322, n323, n324,
        n325, n326, n327, n328, n329, n330, n331, n332, n333, n334, n335,
        n336, n337, n338, n339, n340, n341, n342, n343, n344, n345, n346,
        n347, n348;

DFFX1_RVT \fsum_reg[6] ( .D(sum[6]), .CLK(clk), .Q(fsum[6]) );
DFFX1_RVT \fsum_reg[5] ( .D(sum[5]), .CLK(clk), .Q(fsum[5]) );
DFFX1_RVT \fsum_reg[4] ( .D(sum[4]), .CLK(clk), .Q(fsum[4]) );
DFFX1_RVT \fsum_reg[3] ( .D(sum[3]), .CLK(clk), .Q(fsum[3]) );
DFFX1_RVT \fsum_reg[2] ( .D(sum[2]), .CLK(clk), .Q(fsum[2]) );
DFFX1_RVT \fsum_reg[1] ( .D(sum[1]), .CLK(clk), .Q(fsum[1]) );
DFFX1_RVT fcout_reg ( .D(cout), .CLK(clk), .Q(fcout) );
DFFX1_RVT \fsum_reg[7] ( .D(sum[7]), .CLK(clk), .Q(fsum[7]) );
File Edit View Terminal Tabs Help
DFFX1_RVT \fsum_reg[5] ( .D(sum[5]), .CLK(clk), .Q(fsum[5]) );
DFFX1_RVT \fsum_reg[4] ( .D(sum[4]), .CLK(clk), .Q(fsum[4]) );
DFFX1_RVT \fsum_reg[3] ( .D(sum[3]), .CLK(clk), .Q(fsum[3]) );
DFFX1_RVT \fsum_reg[2] ( .D(sum[2]), .CLK(clk), .Q(fsum[2]) );
DFFX1_RVT \fsum_reg[1] ( .D(sum[1]), .CLK(clk), .Q(fsum[1]) );
DFFX1_RVT fcout_reg ( .D(cout), .CLK(clk), .Q(fcout) );
DFFX1_RVT \fsum_reg[7] ( .D(sum[7]), .CLK(clk), .Q(fsum[7]) );
DFFSSRX1_RVT \fsum_reg[0] ( .D(1'b0), .SETB(sum[0]), .RSTB(sum[1'b1]), .CLK(clk),
                           .QN(fsum[0]) );
INVX0_RVT U83 ( .A(n313), .Y(n324) );
INVX0_RVT U84 ( .A(n279), .Y(n280) );
INVX0_RVT U85 ( .A(n255), .Y(n256) );
INVX0_RVT U86 ( .A(n271), .Y(n268) );
INVX0_RVT U87 ( .A(b[0]), .Y(n220) );
INVX0_RVT U88 ( .A(a[0]), .Y(n219) );
INVX0_RVT U89 ( .A(n223), .Y(n311) );
INVX0_RVT U90 ( .A(n224), .Y(n326) );
INVX0_RVT U91 ( .A(n304), .Y(n306) );
INVX0_RVT U92 ( .A(b[7]), .Y(n274) );
INVX0_RVT U93 ( .A(n233), .Y(n234) );
INVX0_RVT U94 ( .A(n232), .Y(n235) );
INVX0_RVT U95 ( .A(n318), .Y(n320) );
INVX0_RVT U96 ( .A(n315), .Y(n316) );
INVX0_RVT U97 ( .A(n334), .Y(n336) );
INVX0_RVT U98 ( .A(n331), .Y(n332) );
INVX0_RVT U99 ( .A(n344), .Y(n346) );
INVX0_RVT U100 ( .A(n341), .Y(n342) );
INVX0_RVT U101 ( .A(n299), .Y(n301) );
INVX0_RVT U102 ( .A(n296), .Y(n297) );
INVX0_RVT U103 ( .A(b[5]), .Y(n250) );
INVX0_RVT U104 ( .A(n247), .Y(n248) );
INVX0_RVT U105 ( .A(n246), .Y(n249) );
INVX0_RVT U106 ( .A(b[6]), .Y(n260) );
INVX0_RVT U107 ( .A(n265), .Y(n266) );
INVX0_RVT U108 ( .A(n264), .Y(n267) );
INVX0_RVT U109 ( .A(n225), .Y(n285) );
```

```

File Edit View Terminal Tabs Help
INVX0_RVT U98 ( .A(n331), .Y(n332) );
INVX0_RVT U99 ( .A(n344), .Y(n346) );
INVX0_RVT U100 ( .A(n341), .Y(n342) );
INVX0_RVT U101 ( .A(n299), .Y(n301) );
INVX0_RVT U102 ( .A(n296), .Y(n297) );
INVX0_RVT U103 ( .A(b[5]), .Y(n250) );
INVX0_RVT U104 ( .A(n247), .Y(n248) );
INVX0_RVT U105 ( .A(n246), .Y(n249) );
INVX0_RVT U106 ( .A(b[6]), .Y(n260) );
INVX0_RVT U107 ( .A(n265), .Y(n266) );
INVX0_RVT U108 ( .A(n264), .Y(n267) );
INVX0_RVT U109 ( .A(n225), .Y(n285) );
INVX0_RVT U110 ( .A(cin), .Y(n222) );
INVX0_RVT U111 ( .A(a[7]), .Y(n275) );
INVX0_RVT U112 ( .A(b[1]), .Y(n314) );
INVX0_RVT U113 ( .A(n328), .Y(n330) );
INVX0_RVT U114 ( .A(n325), .Y(n327) );
INVX0_RVT U115 ( .A(b[2]), .Y(n329) );
INVX0_RVT U116 ( .A(a[3]), .Y(n339) );
INVX0_RVT U117 ( .A(a[4]), .Y(n293) );
INVX0_RVT U118 ( .A(a[5]), .Y(n251) );
INVX0_RVT U119 ( .A(a[6]), .Y(n261) );
INVX0_RVT U120 ( .A(n308), .Y(n309) );
INVX0_RVT U121 ( .A(n281), .Y(n278) );
INVX0_RVT U122 ( .A(n241), .Y(cout) );
INVX0_RVT U123 ( .A(n238), .Y(n239) );
INVX0_RVT U124 ( .A(n237), .Y(n240) );
INVX0_RVT U125 ( .A(n319), .Y(n322) );
INVX0_RVT U126 ( .A(n335), .Y(n338) );
INVX0_RVT U127 ( .A(n345), .Y(n348) );
INVX0_RVT U128 ( .A(n300), .Y(n303) );
INVX0_RVT U129 ( .A(n257), .Y(n254) );
INVX0_RVT U130 ( .A(n269), .Y(n270) );
OR2X1_RVT U133 ( .A1(b[3]), .A2(a[3]), .Y(n290) );
OR2X1_RVT U134 ( .A1(b[4]), .A2(a[4]), .Y(n216) );
AND2X1_RVT U135 ( .A1(n290), .A2(n216), .Y(n227) );

File Edit View Terminal Tabs Help
AND2X1_RVT U136 ( .A1(a[2]), .A2(b[2]), .Y(n286) );
AND2X1_RVT U137 ( .A1(n227), .A2(n286), .Y(n243) );
AND2X1_RVT U138 ( .A1(b[5]), .A2(a[5]), .Y(n215) );
AND2X1_RVT U139 ( .A1(a[4]), .A2(b[4]), .Y(n247) );
OR2X1_RVT U140 ( .A1(n215), .A2(n247), .Y(n217) );
AND2X1_RVT U141 ( .A1(a[3]), .A2(b[3]), .Y(n292) );
AND2X1_RVT U142 ( .A1(n216), .A2(n292), .Y(n244) );
OR2X1_RVT U143 ( .A1(n217), .A2(n244), .Y(n218) );
OR2X1_RVT U144 ( .A1(n243), .A2(n218), .Y(n229) );
AND2X1_RVT U145 ( .A1(n220), .A2(n219), .Y(n221) );
OR2X1_RVT U146 ( .A1(n222), .A2(n221), .Y(n312) );
AND2X1_RVT U147 ( .A1(b[0]), .A2(a[0]), .Y(n223) );
AND2X1_RVT U148 ( .A1(b[1]), .A2(a[1]), .Y(n224) );
AND3X1_RVT U149 ( .A1(n312), .A2(n311), .A3(n326), .Y(n225) );
OR2X1_RVT U150 ( .A1(b[1]), .A2(a[1]), .Y(n323) );
OR2X1_RVT U151 ( .A1(b[2]), .A2(a[2]), .Y(n226) );
AND2X1_RVT U152 ( .A1(n323), .A2(n226), .Y(n284) );
AND2X1_RVT U153 ( .A1(n284), .A2(n227), .Y(n228) );
AND2X1_RVT U154 ( .A1(n285), .A2(n228), .Y(n242) );
OR2X1_RVT U155 ( .A1(n229), .A2(n242), .Y(n264) );
OR2X1_RVT U156 ( .A1(b[5]), .A2(a[5]), .Y(n265) );
OR2X1_RVT U157 ( .A1(a[6]), .A2(b[6]), .Y(n230) );
AND2X1_RVT U158 ( .A1(n265), .A2(n230), .Y(n231) );
AND2X1_RVT U159 ( .A1(n264), .A2(n231), .Y(n232) );
AND2X1_RVT U160 ( .A1(b[6]), .A2(a[6]), .Y(n233) );
AND2X1_RVT U161 ( .A1(n235), .A2(n234), .Y(n279) );
OR2X1_RVT U162 ( .A1(b[7]), .A2(a[7]), .Y(n236) );
AND2X1_RVT U163 ( .A1(n280), .A2(n236), .Y(n237) );
AND2X1_RVT U164 ( .A1(b[7]), .A2(a[7]), .Y(n238) );
AND2X1_RVT U165 ( .A1(n240), .A2(n239), .Y(n241) );
OR2X1_RVT U166 ( .A1(n243), .A2(n242), .Y(n245) );
OR2X1_RVT U167 ( .A1(n245), .A2(n244), .Y(n246) );
AND2X1_RVT U168 ( .A1(n249), .A2(n248), .Y(n255) );
OR2X1_RVT U169 ( .A1(n250), .A2(a[5]), .Y(n253) );
OR2X1_RVT U170 ( .A1(n251), .A2(b[5]), .Y(n252) );
AND2X1_RVT U171 ( .A1(n253), .A2(n252), .Y(n257) );

```

```
File Edit View Terminal Tabs Help
OR2X1_RVT U176 ( .A1(n261), .A2(b[6]), .Y(n262) );
AND2X1_RVT U177 ( .A1(n263), .A2(n262), .Y(n269) );
OR2X1_RVT U178 ( .A1(n267), .A2(n266), .Y(n271) );
AND2X1_RVT U179 ( .A1(n269), .A2(n268), .Y(n273) );
AND2X1_RVT U180 ( .A1(n271), .A2(n270), .Y(n272) );
OR2X1_RVT U181 ( .A1(n273), .A2(n272), .Y(sum[6]) );
OR2X1_RVT U182 ( .A1(n274), .A2(a[7]), .Y(n277) );
OR2X1_RVT U183 ( .A1(n275), .A2(b[7]), .Y(n276) );
AND2X1_RVT U184 ( .A1(n277), .A2(n276), .Y(n281) );
AND2X1_RVT U185 ( .A1(n279), .A2(n278), .Y(n283) );
AND2X1_RVT U186 ( .A1(n281), .A2(n280), .Y(n282) );
OR2X1_RVT U187 ( .A1(n283), .A2(n282), .Y(sum[7]) );
AND2X1_RVT U188 ( .A1(n285), .A2(n284), .Y(n287) );
OR2X1_RVT U189 ( .A1(n287), .A2(n286), .Y(n340) );
AND2X1_RVT U190 ( .A1(n340), .A2(n290), .Y(n288) );
OR2X1_RVT U191 ( .A1(n288), .A2(n292), .Y(n289) );
OR2X1_RVT U192 ( .A1(n293), .A2(n289), .Y(n298) );
AND2X1_RVT U193 ( .A1(n290), .A2(n293), .Y(n291) );
AND2X1_RVT U194 ( .A1(n340), .A2(n291), .Y(n295) );
AND2X1_RVT U195 ( .A1(n293), .A2(n292), .Y(n294) );
OR2X1_RVT U196 ( .A1(n295), .A2(n294), .Y(n296) );
AND2X1_RVT U197 ( .A1(n298), .A2(n297), .Y(n299) );
AND2X1_RVT U198 ( .A1(n301), .A2(b[4]), .Y(n300) );
OR2X1_RVT U199 ( .A1(b[4]), .A2(n301), .Y(n302) );
AND2X1_RVT U200 ( .A1(n303), .A2(n302), .Y(sum[4]) );
AND2X1_RVT U201 ( .A1(a[0]), .A2(n222), .Y(n304) );
OR2X1_RVT U202 ( .A1(n222), .A2(a[0]), .Y(n305) );
AND2X1_RVT U203 ( .A1(n306), .A2(n305), .Y(n307) );
AND2X1_RVT U204 ( .A1(b[0]), .A2(n307), .Y(n310) );
OR2X1_RVT U205 ( .A1(n307), .A2(b[0]), .Y(n308) );
OR2X1_RVT U206 ( .A1(n310), .A2(n309), .Y(sum[0]) );
AND2X1_RVT U207 ( .A1(n312), .A2(n311), .Y(n313) );
OR2X1_RVT U208 ( .A1(n314), .A2(n324), .Y(n317) );
AND2X1_RVT U209 ( .A1(n324), .A2(n314), .Y(n315) );
AND2X1_RVT U210 ( .A1(n317), .A2(n316), .Y(n318) );
AND2X1_RVT U211 ( .A1(n320), .A2(a[1]), .Y(n319) );
```

```

File Edit View Terminal Tabs Help
AND2X1_RVT U194 ( .A1(n340), .A2(n291), .Y(n295) );
AND2X1_RVT U195 ( .A1(n293), .A2(n292), .Y(n294) );
OR2X1_RVT U196 ( .A1(n295), .A2(n294), .Y(n296) );
AND2X1_RVT U197 ( .A1(n298), .A2(n297), .Y(n299) );
AND2X1_RVT U198 ( .A1(n301), .A2(b[4]), .Y(n300) );
OR2X1_RVT U199 ( .A1(b[4]), .A2(n301), .Y(n302) );
AND2X1_RVT U200 ( .A1(n303), .A2(n302), .Y(sum[4]) );
AND2X1_RVT U201 ( .A1(a[0]), .A2(n222), .Y(n304) );
OR2X1_RVT U202 ( .A1(n222), .A2(a[0]), .Y(n305) );
AND2X1_RVT U203 ( .A1(n306), .A2(n305), .Y(n307) );
AND2X1_RVT U204 ( .A1(b[0]), .A2(n307), .Y(n310) );
OR2X1_RVT U205 ( .A1(n307), .A2(b[0]), .Y(n308) );
OR2X1_RVT U206 ( .A1(n310), .A2(n309), .Y(sum[0]) );
AND2X1_RVT U207 ( .A1(n312), .A2(n311), .Y(n313) );
OR2X1_RVT U208 ( .A1(n314), .A2(n324), .Y(n317) );
AND2X1_RVT U209 ( .A1(n324), .A2(n314), .Y(n315) );
AND2X1_RVT U210 ( .A1(n317), .A2(n316), .Y(n318) );
AND2X1_RVT U211 ( .A1(n320), .A2(a[1]), .Y(n319) );
OR2X1_RVT U212 ( .A1(a[1]), .A2(n320), .Y(n321) );
AND2X1_RVT U213 ( .A1(n322), .A2(n321), .Y(sum[1]) );
AND2X1_RVT U214 ( .A1(n324), .A2(n323), .Y(n325) );
AND2X1_RVT U215 ( .A1(n327), .A2(n326), .Y(n328) );
OR2X1_RVT U216 ( .A1(n329), .A2(n330), .Y(n333) );
AND2X1_RVT U217 ( .A1(n330), .A2(n329), .Y(n331) );
AND2X1_RVT U218 ( .A1(n333), .A2(n332), .Y(n334) );
AND2X1_RVT U219 ( .A1(n336), .A2(a[2]), .Y(n335) );
OR2X1_RVT U220 ( .A1(a[2]), .A2(n336), .Y(n337) );
AND2X1_RVT U221 ( .A1(n338), .A2(n337), .Y(sum[2]) );
OR2X1_RVT U222 ( .A1(n339), .A2(n340), .Y(n343) );
AND2X1_RVT U223 ( .A1(n340), .A2(n339), .Y(n341) );
AND2X1_RVT U224 ( .A1(n343), .A2(n342), .Y(n344) );
AND2X1_RVT U225 ( .A1(n346), .A2(b[3]), .Y(n345) );
OR2X1_RVT U226 ( .A1(b[3]), .A2(n346), .Y(n347) );
AND2X1_RVT U227 ( .A1(n348), .A2(n347), .Y(sum[3]) );
endmodule

```

The output of RTL synthesis

3.Floorplan:

- The initial layout in the physical design of an IC is called the floorplan, which defines the shape and size of the integrated circuit.
- The floorplan represents the tentative placement of various components, including standard cells, I/O ports, and macros.
- Inputs for creating this floorplan include the library file (.ndm), the mapped netlist file, and constraint files such as Tcl and SDC files.
- The floorplan serves as the foundation for the subsequent stages of the design flow, guiding the placement and routing of components to ensure optimal performance and manufacturability.
- We utilize IC Compiler II (ICCII) for tasks ranging from floorplanning to routing, leveraging its advanced capabilities to achieve an efficient and high-performance IC layout.
- During the floorplanning stage, careful consideration is given to factors such as signal integrity, power distribution, and thermal management, ensuring the design meets all functional and physical requirements.
- The floorplan helps to identify and mitigate potential design issues early in the process, enabling a more streamlined and efficient path to final design implementation.
- Effective floorplanning can significantly impact the overall quality and performance of the IC, making it a critical step in the physical design process.

Open ICCII directory and invoke `icc2_shell` and then open the `floorplan.tcl` file in scripts directory of ICCII.

Set the PDK path which includes lib and tech file (library and technology files).

Create a library “**EIGHT_BIT_ADDER1**” and design block “**eight_bit_adder**”.

```

Loading user preference file /ve/ws_home/ws1_7/.synopsys_icc2_guib/preferences.tcl
icc2_shell> start_gui
icc2_shell> set PDK_PATH ../../synopsys_icc2_guib/preferences.tcl
./../ref
icc2_shell> create lib -ref_lib $PDK_PATH/lib/ndm/saed32rvt_c.ndm EIGHT_BIT_ADDER_LIB1
{EIGHT_BIT_ADDER_LIB1}
icc2_shell> read_verilog {../../DC/results/CLA1(mapped.v)} -library EIGHT_BIT_ADDER_LIB1 -design eight_bit_adder.v -top full_adder
Information: Reading Verilog into new design 'eight_bit_adder.v' in library 'EIGHT_BIT_ADDER_LIB1'. (VR-012)
Loading verilog file '/ve/ws/home/ws1_7/Desktop/SRM_Workshop/DC/results/CLA1(mapped.v)'
Warning: Failed to find the specified top module 'full_adder'. (VR-005)
Number of modules read: 1
/Top level ports: 36
Total ports in all modules: 36
Total nets in all modules: 138
Total instances in all modules: 120
Elapsed = 00:00:06.45, CPU = 00:00:00.05
1
icc2_shell> link block
Using libraries: EIGHT_BIT_ADDER_LIB1 saed32rvt_c
Linking block EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design
Information: User units loaded from library 'saed32rvt_c' (LNK-040)
Design 'CLA1' was successfully linked.
1

```

- Initializing the floorplan with 60% core utilization and coincident boundary with offset {1 1}.

```

icc2_shell> initialize_floorplan -core_utilization 0.575 -coincident_boundary false -core_offset {1 1}
Removing existing floorplan objects
Creating core...
Core utilization ratio = 61.70%
Unplacing all cells...
Creating site array...
Creating routing tracks...
Initializing floorplan completed.

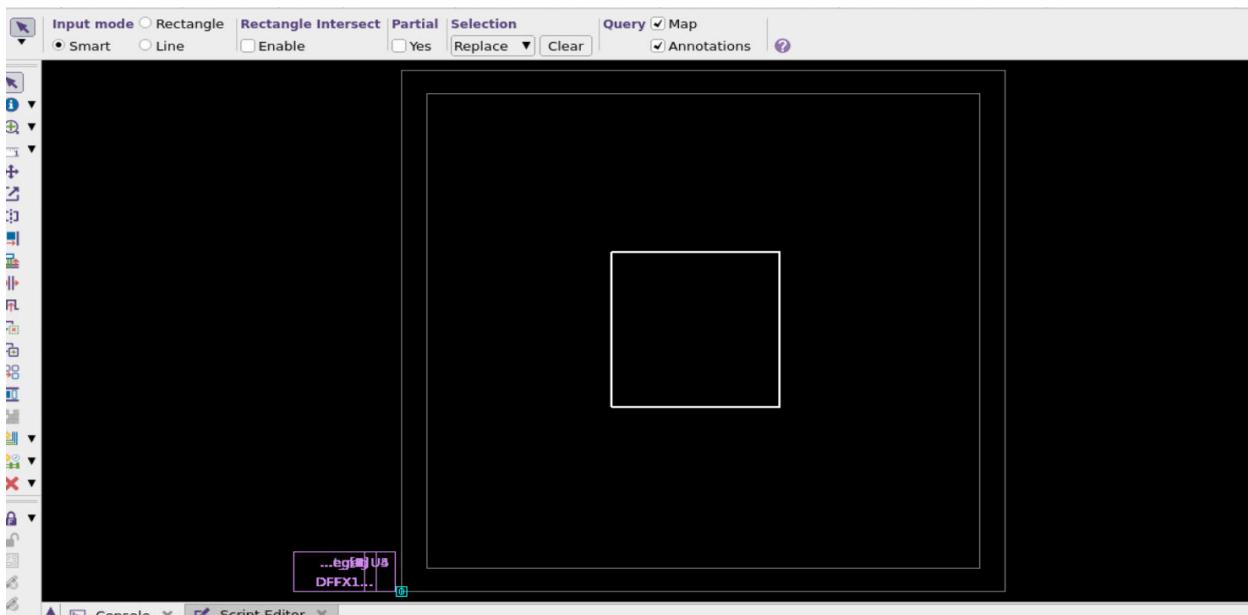
```

- Created hard type placement blockage

```

INITIALIZING FLOORPLAN COMPLETED.
icc2_shell> create_placement_blockage -type hard -boundary {{1 1} {1 7.5574} {7.5574 7.5574} {7.5574 1}}
{PB_0}
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -start MoveTool
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -start RulerTool
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -start MoveTool
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -drag {{5.500 3.946} {12.304 10.833}} -scale 0.041
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -start RulerTool
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -start MoveTool
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -drag {{10.214 11.119} {10.542 11.119}} -scale 0.041
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -start RulerTool
icc2_shell> gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -cancel
gui_mouse_tool -window [gui_get_current_window -types Layout -mrui] -cancel

```



- Placed input pins on side-1 and output pin on side-3

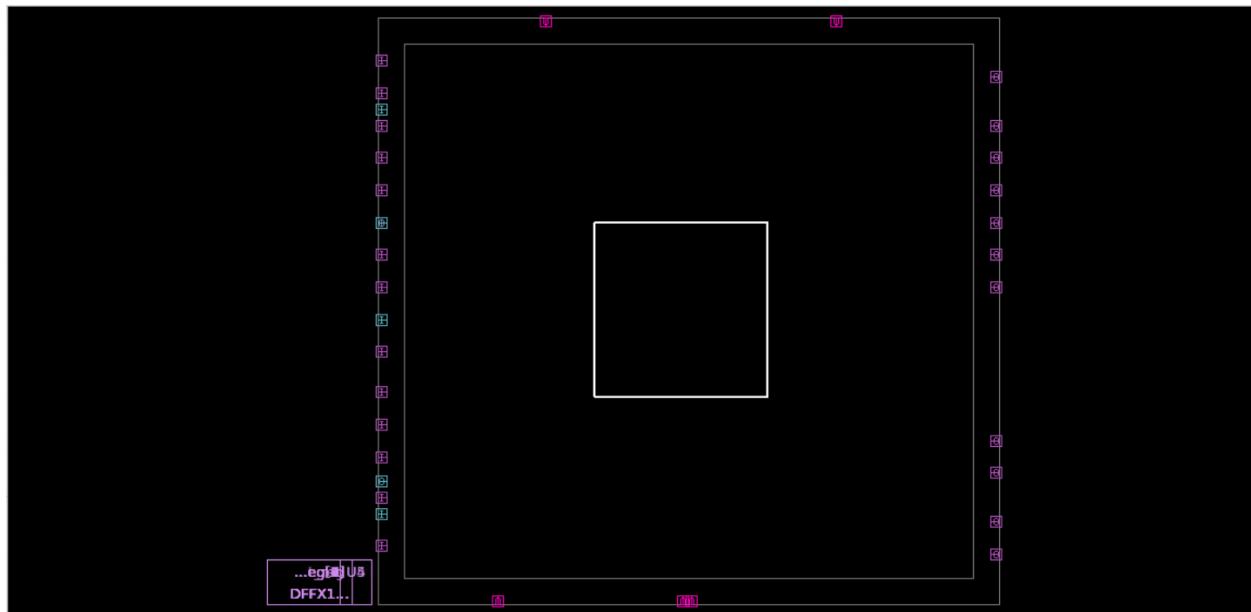
```

icc2_shell> set_individual_pin_constraints -ports [get_ports {a b clk cin}] -sides 1 -pin_spacing_distance 1
1
icc2_shell> set_individual_pin_constraints -ports [get_ports {fsum fcout}] -sides 3 -pin_spacing_distance 1
1
icc2_shell> place_pins -self
Information: Starting 'place_pins' (FLW-8000)
Information: Time: 2024-07-11 01:02:50 / Session: 00:15:15 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 461 MB (FLW-8100)
Load DB...
CPU Time for load db: 00:00:00.00u 00:00:00.01s 00:00:00.03e:

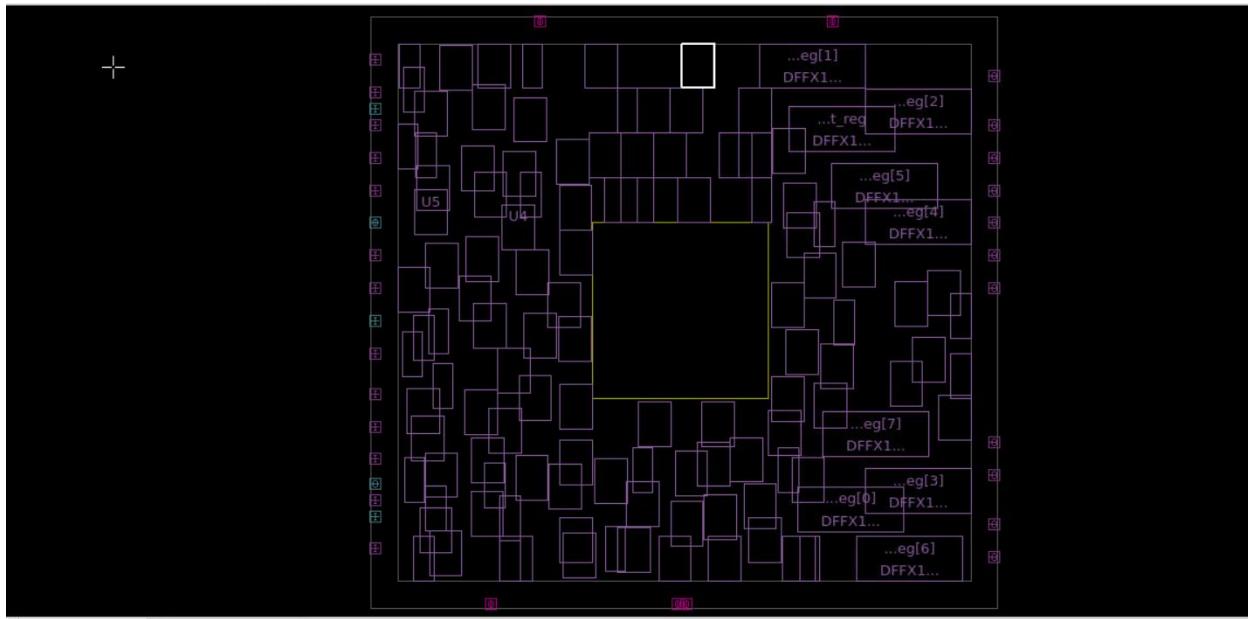
Min routing layer: M1
Max routing layer: MRDL

CPU Time for Top Level Pre-Route Processing: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Warning: found large number of corner keepout wiretracks on side 1 of block CLA1 on layer M9 and there is no enough wire tracks available on this side (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 2 of block CLA1 on layer MRDL and there is no enough wire tracks available on this side (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 3 of block CLA1 on layer M9 and there is no enough wire tracks available on this side (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 4 of block CLA1 on layer MRDL and there is no enough wire tracks available on this side (DPPA-096)
Number of block ports: 36
Number of block pin locations assigned from router: 0
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of PG ports on blocks: 0
Number of pins created: 36
CPU Time for Pin Creation: 00:00:00.01u 00:00:00.00s 00:00:00.01e:
Total Pin Placement CPU Time: 00:00:00.01u 00:00:00.01s 00:00:00.06e:
Information: Ending 'place_pins' (FLW-8001)
Information: Time: 2024-07-11 01:02:50 / Session: 00:15:15 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 461 MB (FLW-8100)
1
icc2_shell>

```



- Created placement with high effort command.



- Commands for the floorplan

```
cc2_shell> history
1 start_gui
2 set PDK_PATH ../../ref
3 create_lib -ref lib $PDK_PATH/lib/ndm/saed32rvt.c.ndm EIGHT_BIT_ADDER_LIB1
4 read_verilog {../../DC/results/CLA1.mapped.v} -library EIGHT_BIT_ADDER_LIB1 -design eight_bit_adder.v -top full_adder
5 link_block
6 initialize_floorplan -core_utilization 0.585 -coincident_boundary false -core_offset {1 1}
7 initialize_floorplan -core_utilization 0.575 -coincident_boundary false -core_offset {1 1}
8 create_placement_blockage -type hard -boundary {{1 1} {1 7.5574} {7.5574 7.5574} {7.5574 1}}
9 place_pins -self
10 set_individual_pin_constraints -ports [get_ports {a b clk cin}] -sides 1 -pin_spacing_distance 1
11 set_individual_pin_constraints -ports [get_ports {fsum fcout}] -sides 3 -pin_spacing_distance 1
12 place_pins -self
13 create_placement -floorplan
14 start_gui
15 initialize_floorplan -core_utilization 0.575 -coincident_boundary false -core_offset {1 1}
16 set_individual_pin_constraints -ports [get_ports {a b clk cin}] -sides 1 -pin_spacing_distance 1
17 set_individual_pin_constraints -ports [get_ports {fsum fcout}] -sides 3 -pin_spacing_distance 1
18 create_placement_blockage -type hard -boundary {{1 1} {1 7.5574} {7.5574 7.5574} {7.5574 1}}
19 place_pins -self
20 place_pins -self
21 create_placement -floorplan
22 initialize_floorplan -core_utilization 0.575 -coincident_boundary false -core_offset {1 1}
23 create_placement_blockage -type hard -boundary {{1 1} {1 7.5574} {7.5574 7.5574} {7.5574 1}}
24 set_individual_pin_constraints -ports [get_ports {a b clk cin}] -sides 1 -pin_spacing_distance 1
25 set_individual_pin_constraints -ports [get_ports {fsum fcout}] -sides 3 -pin_spacing_distance 1
26 place_pins -self
27 create_placement -floorplan
28 create_placement -floorplan
29 history
```

Floorplan is completed.

4.Powerplan:

- Power planning is the process of distributing power to the circuit through a Power Distribution Network (PDN).
- This is a pre-routing process.
- It involves creating a core power ring, generating a power mesh, and establishing standard cell rails across metal layers.
- Power planning is a crucial aspect of the physical design process, ensuring that the integrated circuit (IC) receives a stable and reliable power supply. This step is essential for the correct operation of the IC, preventing issues such as voltage drops and ground bounce that can lead to functional failures.

Core Power Ring:

- The core power ring surrounds the core area of the IC and serves as the primary distribution point for power.
- It helps in delivering a uniform power supply to the entire chip and minimizes the resistance and inductance in the power delivery path.

Power Mesh:

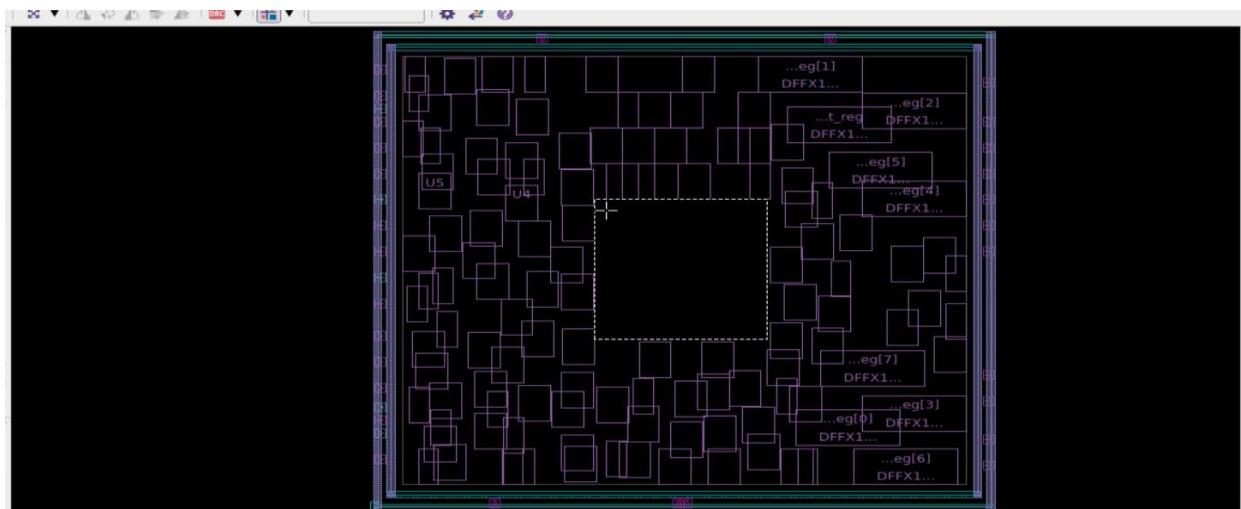
- A power mesh is created by interconnecting horizontal and vertical metal lines to form a grid over the entire chip.
- This mesh ensures that power is evenly distributed to all parts of the IC, reducing voltage drops and ensuring consistent performance across the chip.
- It also provides multiple paths for current flow, enhancing the robustness of the power distribution.

Standard Cell Rails:

- Standard cell rails are power lines that run across rows of standard cells within the IC.
- These rails supply power to individual standard cells, which are the basic building blocks of the digital circuit.
- Proper design of standard cell rails is crucial for maintaining signal integrity and overall power efficiency.

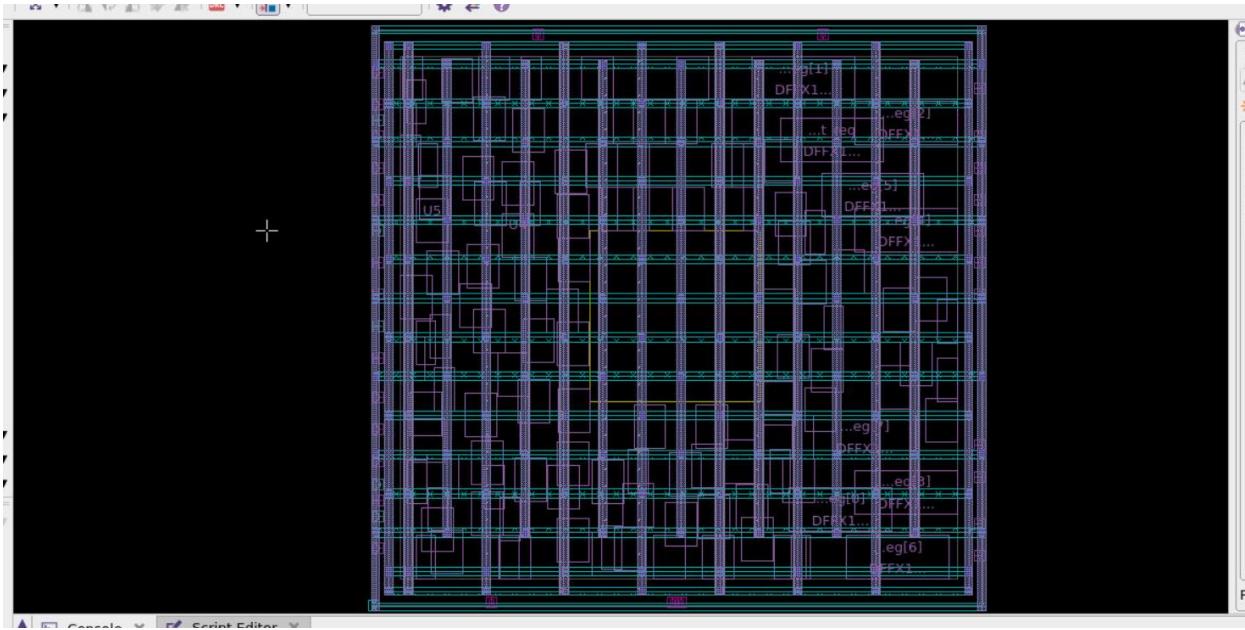
Creating VDD,VSS and Core power ring

```
icc2_shell> create_net -power {VDD}
{VDD}
icc2_shell> create_net -ground {VSS}
{VSS}
icc2_shell> connect_pg_net -all_blocks -automatic
*****
Report : Power/Ground Connection Summary
Design : CLA1
Version: V-2023.12
Date   : Thu Jul 11 01:34:29 2024
*****
P/G net name          P/G pin count(previous/current)
-----
Power net VDD          0/120
Ground net VSS         0/120
-----
Information: connections of 240 power/ground pin(s) are created or changed.
1
icc2_shell> create_pg_ring_pattern core_ring_pattern -horizontal_layer M7 -horizontal_width .3 -horizontal_spacing .3 -vertical_layer M8 -vertical_width
.3 -vertical_spacing .2
Information: The command 'create_pg_ring_pattern' cleared the undo history. (UNDO-016)
Successfully create PG ring pattern core_ring_pattern.
icc2_shell>
icc2_shell>
icc2_shell> set_pg_strategy core_power_ring -core -pattern {{name : core_ring_pattern}{nets : {VDD VSS}}{offset : {.3 .3}}}
Successfully set PG strategy core_power_ring.
icc2_shell>
icc2_shell> compile_pg -strategies core_power_ring
Sanity check for inputs.
No strategy-level via rule is specified, the default rule will be applied.
Automatic PG net connection through connect_pg_net is disabled.
Updating PG strategies.
Updating strategy core_power_ring.
Loading library and design information.
Number of Standard Cells: 120
Number of Hard Macros: 0
Number of Pads: 0
Creating rings.
Creating via connection between strategies and existing shapes.
Via DRC checking runtime 0.00 seconds.
Via connection runtime: 0 seconds.
Removing dangling/floating wire/vias after DRC check.
Start iteration 1:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias inside strategy core_power_ring.
Checking 4 stacked vias:0% 20% 50% 70% 100%
Finish removing all dangling or floating wires and vias.
Committing wires and vias.
Committing wires takes 0.00 seconds.
Committing vias takes 0.00 seconds.
Committed 8 wires.
Committed 4 vias.
Committed 0 wires for via creation.
Overall PG creation runtime: 0 seconds.
Overall runtime: 0 seconds.
1
gui mouse_tool -window [gui_get_current_window -types Layout -mru] -add_point {26.568 12.845} -scale 0.0408
icc2_shell> 1
```



Creating Power mesh and compiling the power mesh

```
icc2_shell> set_pg_strategy core_mesh -pattern { {pattern:mesh} {nets: VDD VSS} } -core -extension {stop: innermost_ring}
Successfully set PG strategy core_mesh.
icc2_shell>
icc2_shell>
icc2_shell> compile_pg -strategies core_mesh
Sanity check for inputs.
No strategy-level via rule is specified, the default rule will be applied.
Automatic PG net connection through connect_pg_net is disabled.
Updating PG strategies.
Updating strategy core_mesh.
Loading library and design information.
Number of Standard Cells: 120
Number of Hard Macros: 0
Number of Pads: 0
Creating straps and vias in power plan.
Creating wire shapes for strategies core_mesh .
Creating wire shapes runtime: 0 seconds
Blockage cutting and DRC fixing for wire shapes for strategies core_mesh .
Check and fix DRC for 42 wires for strategy core_mesh.
Number of threads: 1
Number of partitions: 3
Direction of partitions: vertical
Number of wires: 28
Checking DRC for 28 wires:5% 10% 20% 100%
Number of threads: 1
Number of partitions: 2
Direction of partitions: horizontal
Number of wires: 14
Checking DRC for 14 wires:100%
Creating 42 wires after DRC fixing.
Wire DRC checking runtime 1.00 seconds.
Creating via shapes for strategies core_mesh .
Working on strategy core_mesh.
Number of detected intersections: 196
Total runtime of via shapes creation: 0 seconds
Check and fix DRC for 196 stacked vias for strategy core_mesh.
Check and fix DRC for 196 stacked vias for strategy core_mesh.
Number of threads: 1
Number of partitions: 2
Direction of partitions: horizontal
Number of vias: 196
Checking DRC for 196 stacked vias:5% 10% 15% 25% 35% 40% 45% 50% 55% 60% 70% 75% 80% 85% 90% 95% 100%
Runtime of via DRC checking for strategy core_mesh: 0.00 seconds.
Creating via connection between strategies and existing shapes.
Check and fix DRCs for 56 stacked vias.
Number of threads: 1
Number of partitions: 2
Direction of partitions: horizontal
Number of vias: 56
Checking DRC for 56 stacked vias:5% 10% 15% 20% 25% 30% 35% 80% 85% 100%
Via DRC checking runtime 0.00 seconds.
Via connection runtime: 0 seconds.
Removing dangling/floating wire/vias after DRC check.
Start iteration 1:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias inside strategy core_mesh.
Checking 196 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Checking dangling/floating vias between strategies and existing shapes.
Checking 56 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Start iteration 2:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias inside strategy core_mesh.
Checking 196 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Checking dangling/floating vias between strategies and existing shapes.
Checking 56 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Finish removing all dangling or floating wires and vias.
Committing wires and vias.
Committing wires and vias.
Committing wires takes 0.00 seconds.
Committing vias takes 0.00 seconds.
Committed 42 wires.
Committed 252 vias.
Committed 0 wires for via creation.
Overall PG creation runtime: 1 seconds.
Successfully compiled PG.
Overall runtime: 1 seconds.
1
```



Creating and compiling standard cell rails

```
icc2_shell> create_pg_std_cell_conn_pattern std_cell_rail -layers {M1} -rail_width 0.06
Successfully create standard cell rail pattern std_cell_rail.
icc2_shell>
icc2_shell>
icc2_shell> set_pg_strategy rail_strat -core -pattern {{name: std_cell_rail} {nets: VDD VSS} }
Successfully set PG strategy rail_strat.
icc2_shell>
icc2_shell> compile_pg -strategies rail_strat
Sanity check for inputs.
No strategy-level via rule is specified, the default rule will be applied.
Automatic PG net connection through connect_pg_net is disabled.
Updating PG strategies.
Updating strategy rail_strat.
Loading library and design information.
Number of Standard Cells: 120
Number of Hard Macros: 0
Number of Pads: 0
Creating standard cell rails.
Creating standard cell rails for strategy rail_strat.
DRC checking and fixing for standard cell rail strategy rail_strat.
Number of threads: 1
Number of partitions: 2
Direction of partitions: horizontal
Number of wires: 13
Checking DRC for 13 wires:15% 30% 45% 60% 75% 90% 100%
Creating 13 wires after DRC fixing.
```

```

Creating 13 wires after DRC fixing.
Wire DRC checking runtime 0.00 seconds.
Creating via connection between strategies and existing shapes.
Check and fix DRCs for 182 stacked vias.
Number of threads: 1
Number of partitions: 2
Direction of partitions: horizontal
Number of vias: 182
Checking DRC for 182 stacked vias:5% 10% 15% 20% 25% 30% 35% 40% 45% 50% 55% 60% 65% 70% 75% 80% 85% 90% 95% 100%
91 regular vias are not fixed
Via DRC checking runtime 2.00 seconds.
via connection runtime: 3 seconds.
Removing dangling/floating wire/vias after DRC check.
Start iteration 1:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias between strategies and existing shapes.
Checking 91 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Start iteration 2:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias between strategies and existing shapes.
Checking 91 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Finish removing all dangling or floating wires and vias.
Committing wires and vias.
Committing wires takes 0.00 seconds.
Committing vias takes 0.00 seconds.
Committed 13 wires.
Committed 455 vias.
Committed 364 wires for via creation.
Overall PG creation runtime: 3 seconds.
Successfully compiled PG.
Overall runtime: 3 seconds.
1

```

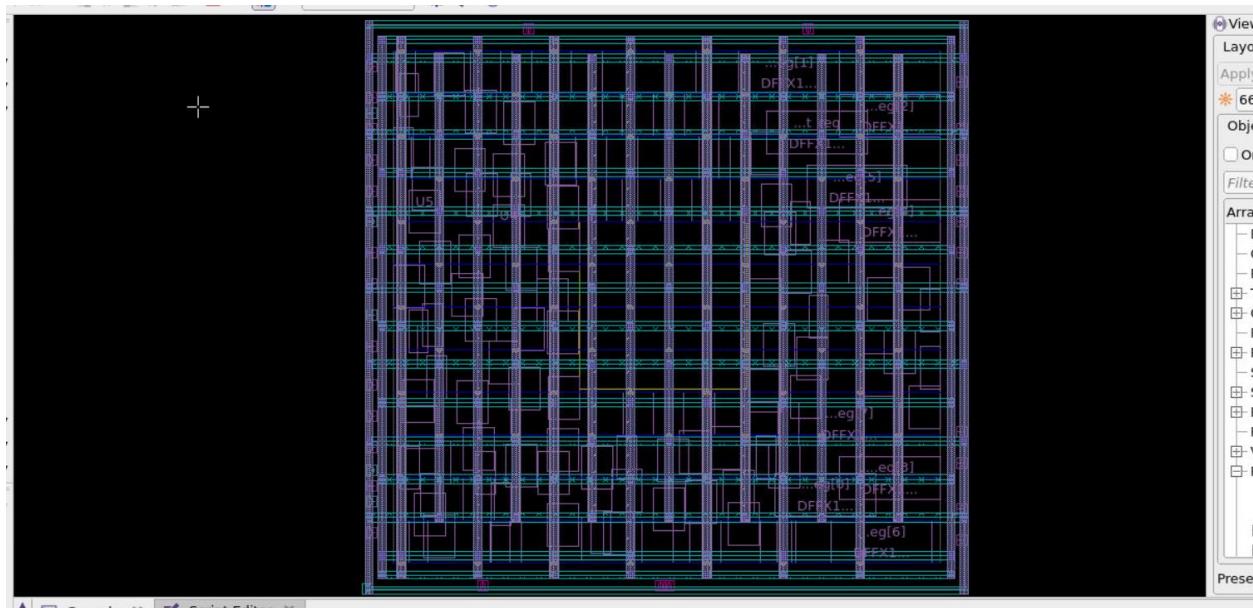
Save the block and lib.

```

1
icc2_shell> save_block
Information: Saving block 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'
1
icc2_shell> save_lib
Saving library 'EIGHT_BIT_ADDER_LIB1'
1

```

Output of the power planning



Commands of the power planning:

```
52 create_net -power {VDD}
53 create_net -ground {VSS}
54 connect_pg_net -all_blocks -automatic
55 create_pg_ring_pattern core_ring_pattern -horizontal_layer M7 -horizontal_width .3 -horizontal_spacing .2 -vertical_layer M8 -vertical_width .3 -vertical_spacing .2
56 set_pg_strategy core_power_ring -core -pattern {{name : core_ring_pattern}{nets : {VDD VSS}}{offset : {.3 .3}}}
57 compile_pg -strategies core_power_ring
58 create_pg_mesh_pattern mesh -layers { {{vertical_layer: M6}{width: .30} {spacing: interleaving}{pitch: 3} {offset: .3}} {{horizontal_layer: M7}{width: .34} {spacing: interleaving} {pitch: 3} {offset: .3}} {{vertical_layer: M8}{width: .34} {spacing: interleaving} {pitch: 3} {offset: .3}} }
59 set_pg_strategy core_mesh -pattern { {pattern:mesh} {nets: VDD VSS}} -core -extension {stop: innermost_ring}
60 compile_pg -strategies core_mesh
61 create_pg_std_cell_conn_pattern std_cell_rail -layers {M1} -rail_width 0.06
62 set_pg_strategy rail_strat -core -pattern {{name: std_cell_rail} {nets: VDD VSS} }
63 compile_pg -strategies rail_strat
64 save_block
65 save_lib
66 history
icc2_shell> █
```

5.Placement:

- **Placement** is the process of determining the optimal physical location for each cell within a block.
- This process involves using tools to identify the best locations for each component within the core area, aiming to minimize congestion and optimize timing performance.
- **Corner** refers to a set of libraries characterized for various PVT (Process, Voltage, Temperature) variations, which are used to model different operational conditions of the IC.
- **Mode** is defined by a specific combination of clocks, voltage levels, temperature conditions, and libraries, which together describe the operational context of the design.
- **Scenario** combines a Mode and a Corner, representing a comprehensive set of conditions under which the design is evaluated.

Ex: For 3 modes and 3 corners, we have 9 Scenarios.

Set PDK path and check pre-placement requirements in the design.

```
icc2_shell> set PDK_PATH ./../ref
./..../ref
icc2_shell> check_design -checks pre_placement_stage
*****
Report : check_design
Options: { pre_placement_stage }
Design : CLA1
Version: V-2023.12
Date   : Thu Jul 11 01:52:45 2024
*****  
  
Running mega-check 'pre_placement_stage':
  Running atomic-check 'design_mismatch'
  Running atomic-check 'scan_chain'
  Running atomic-check 'mv_design'
  Running atomic-check 'rp_constraints'
  Running atomic-check 'timing'
  Running atomic-check 'hier_pre_placement'  
  
*** EMS Message summary ***
-----  
Rule      Type  Count    Message
-----  
DFT-011  Info   1        The design has no scan chain defined in the scandef.  
TCK-001  Warn   27       The reported endpoint '%endpoint' is unconstrained. Reason: '%re...  
TCK-002  Warn   9        The register clock pin '%pin' has no fanin clocks. Mode:'%mode'.  
-----  
Total 37 EMS messages : 0 errors, 36 warnings, 1 info.  
-----  
  
*** Non-EMS message summary ***
-----  
Rule      Type  Count    Message
-----  
NDMUI-173  Info   1        There are no relative placement groups in the design.  
-----  
Total 1 non-EMS messages : 0 errors, 0 warnings, 1 info.  
-----  
  
Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)  
Information: EMS database is saved to file 'check_design.ems'.  
Information: Non-EMS messages are saved into file 'check_design2024Jul11015243.log'.  
1
```

Now, remove all the default mode, corner, scenarios and set corner, scenario and then create corner, mode and scenario.

```
icc2_shell> current_mode
{default}
icc2_shell> remove_modes -all; remove_corners -all; remove_scenarios -all
1
icc2_shell> set model "func"
func
icc2_shell> set corner1 "nom"
nom
icc2_shell> set scenario1 "${model}::${corner1}"
func::nom
icc2_shell> create_mode $model
1
icc2_shell> create_corner $corner1
1
icc2_shell> create_scenario -name func::nom -mode func -corner nom
Created scenario func::nom for mode func and corner nom
All analysis types are activated.
{func::nom}
```

‘report_scenarios’ – It provides information about different scenarios that contain corners and modes.

```
icc2 shell> report_scenarios
*****
Report : scenario
Design : CLA1
Version: V-2023.12
Date   : Thu Jul 11 01:59:55 2024
*****
Name      Mode     Corner      Active  Setup  Hold  Leakage  Dynamic
          Cell     Signal
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+
func::nom *   func       nom    true    true   true   true    true   true   true   true   false  false
-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+
1
```

After reading sdc file, Now set and read the parasitic capacitance i.e minimum and maximum capacitance in the tech files.

```
icc2_shell> set parasitic1 "p1"
p1
icc2_shell> set tluplus_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus"
../../ref/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus
icc2_shell> set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
../../ref/tech/star_rcxt/saed32nm_tf_itf_tluplus.map
icc2_shell>
icc2_shell> set parasitic2 "p2"
p2
icc2_shell> set tluplus_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus"
../../ref/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus
icc2_shell> set layer_map_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
../../ref/tech/star_rcxt/saed32nm_tf_itf_tluplus.map
icc2_shell>
icc2_shell> read_parasitic_tech -tlup $tluplus_filep1 -layermap $layer_map_filep1 -name p1
1
icc2_shell> read_parasitic_tech -tlup $tluplus_filep2 -layermap $layer_map_filep2 -name p2
1
icc2_shell>
icc2_shell> set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2
1
icc2_shell> set_app_options -name place.coarse.continue_on_missing_scandef -value true
place.coarse.continue_on_missing_scandef true
```

'place_pins -self' - Tool will start placement of cells. Tool will run many(thousands) iterations and it will choose the best iteration among them

```
lcc2_shell> place_pins -self
Information: Starting 'place_pins' (FLW-8000)
Information: Time: 2024-07-11 02:04:13 / Session: 01:16:39 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 562 MB (FLW-8100)
Load DB...
CPU Time for load db: 00:00:00.00u 00:00:00.01s 00:00:00.04e:

Min routing layer: M1
Max routing layer: MRDL

CPU Time for Top Level Pre-Route Processing: 00:00:00.01u 00:00:00.00s 00:00:00.02e:
Warning: found large number of corner keepout wiretracks on side 1 of block CLA1 on layer M9 and there is no enough wire tracks available on this side (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 2 of block CLA1 on layer MRDL and there is no enough wire tracks available on this side (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 3 of block CLA1 on layer M9 and there is no enough wire tracks available on this side (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 4 of block CLA1 on layer MRDL and there is no enough wire tracks available on this side (DPPA-096)
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = MRDL
Turn off antenna since no rule is specified
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer C0. (ZRT-022)
Warning: Ignore 2 top cell ports with no pins. (ZRT-027)

Block Pin Constraint  Min Pin Max Pin Reserve
                    Layer   Layer   Layer   Feedthroughs
-----  -----
CLA1      M2       MRDL    MRDL    Not allowed

Information: When applicable Min-max layer allow_pin connection mode will allow paths of length 3.55 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin connection mode will allow paths of length 3.55 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {0.001 -1.368} {23.431 -1.064} on layer M2. (ZRT-625)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {0.001 -1.368} {23.431 -1.064} on layer M2. (ZRT-625)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {0.001 23.128} {23.431 23.432} on layer M2. (ZRT-625)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {0.001 23.128} {23.431 23.432} on layer M2. (ZRT-625)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {0.001 23.128} {23.431 23.432} on layer M2. (ZRT-625)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 22.063} on layer M3. (ZRT-625)
Warning: Master cell eight_bit_adder.v has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 22.063} on layer M3. (ZRT-625)
Warning: Master cell eight_bit adder.v has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 22.063} on layer M3. (ZRT-625)
Warning: Master cell eight_bit adder.v has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 22.063} on layer M3. (ZRT-625)
Note - message 'ZRT-625' limit(10) exceeded. Remainder will be suppressed.
Warning: Cell U8 is placed overlapping with other cells at {{4.817 1.001} {5.577 2.673}}. (ZRT-763)
Start Global Route ...
[Init] Elapsed real time: 0:00:00
[Init] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Init] Stage (MB): Used 0 Alloctr 0 Proc 0
[Init] Total (MB): Used 45 Alloctr 45 Proc 3955
Printing options for 'route.common.*'

Printing options for 'route.global.*'
Begin global routing.
Constructing data structure ...
Design statistics:
Design Bounding Box (-1.67um,-1.67um,25.10um,23.74um)
Number of routing layers = 10
layer M1, dir Hor, min width = 0.05um, min space = 0.05um pitch = 0.152um
layer M2, dir Ver, min width = 0.056um, min space = 0.056um pitch = 0.152um
layer M3, dir Hor, min width = 0.056um, min space = 0.056um pitch = 0.304um
layer M4, dir Ver, min width = 0.056um, min space = 0.056um pitch = 0.304um
layer M5, dir Hor, min width = 0.056um, min space = 0.056um pitch = 0.608um
layer M6, dir Ver, min width = 0.056um, min space = 0.056um pitch = 0.608um
layer M7, dir Hor, min width = 0.056um, min space = 0.056um pitch = 1.216um
layer M8, dir Ver, min width = 0.056um, min space = 0.056um pitch = 1.216um
layer M9, dir Hor, min width = 0.16um, min space = 0.16um pitch = 2.432um
layer MRDL, dir Ver, min width = 2um, min space = 2um pitch = 4.864um
Current Stage stats:
[End of Build Tech Data] Elapsed real time: 0:00:00
[End of Build Tech Data] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Tech Data] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Build Tech Data] Total (MB): Used 49 Alloctr 49 Proc 3959
Net statistics:
Total number of nets to route for block pin placement = 38
Number of interface nets to route for block pin placement = 38
Number of single or zero port nets = 2
Net length statistics:
```

```

Net Count(Ignore Fully Rted) 72, Total Half Perimeter Wire Length (HPWL) 1021 microns
HPWL 0 ~ 50 microns: Net Count    72    Total HPWL      1021 microns
HPWL 50 ~ 100 microns: Net Count    0    Total HPWL      0 microns
HPWL 100 ~ 200 microns: Net Count    0    Total HPWL      0 microns
HPWL 200 ~ 300 microns: Net Count    0    Total HPWL      0 microns
HPWL 300 ~ 400 microns: Net Count    0    Total HPWL      0 microns
HPWL 400 ~ 500 microns: Net Count    0    Total HPWL      0 microns
HPWL 500 ~ 600 microns: Net Count    0    Total HPWL      0 microns
HPWL 600 ~ 700 microns: Net Count    0    Total HPWL      0 microns
HPWL 700 ~ 800 microns: Net Count    0    Total HPWL      0 microns
HPWL 800 ~ 900 microns: Net Count    0    Total HPWL      0 microns
HPWL 900 ~ 1000 microns: Net Count    0    Total HPWL      0 microns
HPWL > 1000 microns: Net Count    0    Total HPWL      0 microns
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build All Nets] Stage (MB): Used    0 Allocctr    0 Proc    2
[End of Build All Nets] Total (MB): Used   49 Allocctr   50 Proc 3961
Number of partitions: 1 (1 x 1)
Size of partitions: 10 gCells x 9 gCells
Average gCell capacity 17.43 on layer (1) M1
Average gCell capacity 14.90 on layer (2) M2
Average gCell capacity 8.68 on layer (3) M3
Average gCell capacity 7.40 on layer (4) M4
Average gCell capacity 4.18 on layer (5) M5
Average gCell capacity 3.51 on layer (6) M6
Average gCell capacity 1.34 on layer (7) M7
Average gCell capacity 1.51 on layer (8) M8
Average gCell capacity 1.00 on layer (9) M9
Average gCell capacity 0.40 on layer (10) MRDL
Average number of tracks per gCell 18.67 on layer (1) M1
Average number of tracks per gCell 17.78 on layer (2) M2
Average number of tracks per gCell 9.44 on layer (3) M3
Average number of tracks per gCell 9.44 on layer (3) M3
Average number of tracks per gCell 8.90 on layer (4) M4
Average number of tracks per gCell 4.89 on layer (5) M5
Average number of tracks per gCell 4.60 on layer (6) M6
Average number of tracks per gCell 2.56 on layer (7) M7
Average number of tracks per gCell 2.40 on layer (8) M8
Average number of tracks per gCell 1.44 on layer (9) M9
Average number of tracks per gCell 0.60 on layer (10) MRDL
Number of gCells = 900
Current Stage stats:
[End of Build Congestion Map] Elapsed real time: 0:00:00
[End of Build Congestion Map] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Congestion Map] Stage (MB): Used    0 Allocctr    0 Proc    0
[End of Build Congestion Map] Total (MB): Used   49 Allocctr   50 Proc 3962
Current Stage stats:
[End of Add Nets Demand] Elapsed real time: 0:00:00
[End of Add Nets Demand] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Add Nets Demand] Stage (MB): Used    0 Allocctr    0 Proc    0
[End of Add Nets Demand] Total (MB): Used   49 Allocctr   50 Proc 3962
Number of user frozen nets = 0
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used    1 Allocctr    1 Proc    2
[End of Build Data] Total (MB): Used   49 Allocctr   50 Proc 3962
Number of partitions: 1 (1 x 1)
Size of partitions: 10 gCells x 9 gCells
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Blocked Pin Detection] Stage (MB): Used   12 Allocctr  12 Proc  15
[End of Blocked Pin Detection] Total (MB): Used  61 Allocctr  62 Proc 3977
Information: Using 1 threads for routing. (ZRT-444)
Information: Buffer distance is estimated to be -862.0000um (257 gCells)

Start GR_phase 0
Number of partitions: 1 (1 x 1)
Size of partitions: 10 gCells x 9 gCells
[rtTop] Elapsed real time: 0:00:00
[rtTop] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Initial Routing] Stage (MB): Used    0 Allocctr    0 Proc    0
[End of Initial Routing] Total (MB): Used   61 Allocctr   62 Proc 3977
Initial. Routing result:
Initial. Both Dirs: Dmd-Cap = 0 Max = 0 GRCs = 0 (0.00%)
Initial. H routing: Dmd-Cap = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. V routing: Dmd-Cap = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. Both Dirs: Overflow = 0 Max = 0 GRCs = 0 (0.00%)
Initial. H routing: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. V routing: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M1: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M2: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M3: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M4: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M5: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M6: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M7: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M8: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M9: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. MRDL: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)

Initial. Total Wire Length = 188.37
Initial. Layer M1 wire length = 0.00
Initial. Layer M2 wire length = 50.82
Initial. Layer M3 wire length = 133.06
Initial. Layer M4 wire length = 4.48
Initial. Layer M5 wire length = 0.00

```

```

Initial. Layer M6 wire length = 0.00
Initial. Layer M7 wire length = 0.00
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 69
Initial. Via VIA12SQ.C count = 36
Initial. Via VIA23SQ.C count = 29
Initial. Via VIA34SQ.C count = 4
Initial. Via VIA45SQ.C count = 0
Initial. Via VIA56SQ.C count = 0
Initial. Via VIA67SQ.C count = 0
Initial. Via VIA78SQ.C count = 0
Initial. Via VIA89.C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used 13 Alloctr 13 Proc 18
[End of Whole Chip Routing] Total (MB): Used 61 Alloctr 62 Proc 3977
[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Global Routing] Stage (MB): Used 13 Alloctr 13 Proc 18
[End of Global Routing] Total (MB): Used 61 Alloctr 62 Proc 3977
[End of dbOut] Elapsed real time: 0:00:00
[End of dbOut] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of dbOut] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of dbOut] Total (MB): Used 53 Alloctr 53 Proc 3977
CPU Time for Global Route: 00:00:00.16u 00:00:00.14s 00:00:02.42e:
Number of block ports: 36
Number of block pin locations assigned from router: 36
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.01s 00:00:00.00e:

```

```

CPU Time for Pin Creation: 00:00:00.01u 00:00:00.02s 00:00:00.37e:
Total Pin Placement CPU Time: 00:00:00.19u 00:00:00.18s 00:00:03.06e:
Information: Ending 'place_pins' (FLW-8001)
Information: Time: 2024-07-11 02:04:17 / Session: 01:16:42 / Command: 00:00:03 / CPU: 00:00:00 / Memory: 618 MB (FLW-8100)
1

```

‘place_opt’ – Used to perform placement optimization w.r.t power, area, timing.

```

*****
Report : Placement Attempts
Site   : unit
*****
number of cells:          112
number of references:     15
number of site rows:      12
number of locations attempted: 1471
number of locations failed: 0  (0.0%)
Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

*****
Report : Cell Displacements
*****
number of cells aggregated:    112 (989 total sites)
avg row height over cells:    1.672 um
rms cell displacement:        0.000 um ( 0.00 row height)
rms weighted cell displacement: 0.000 um ( 0.00 row height)
max cell displacement:        0.000 um ( 0.00 row height)
avg cell displacement:        0.000 um ( 0.00 row height)
avg weighted cell displacement: 0.000 um ( 0.00 row height)
number of cells moved:        0
number of large displacements: 0
large displacement threshold:  3.000 row height

```

```

Displacements of worst 10 cells:
Cell: U45 (AND2X1_RVT)
  Input location: (5.56,11.032)
  Legal location: (5.56,11.032)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U42 (AND2X1_RVT)
  Input location: (6.776,7.688)
  Legal location: (6.776,7.688)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U40 (AND2X1_RVT)
  Input location: (1.912,16.048)
  Legal location: (1.912,16.048)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U35 (AND2X1_RVT)
  Input location: (2.216,6.016)
  Legal location: (2.216,6.016)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U4 (AND2X1_RVT)
  Input location: (6.168,16.048)
  Legal location: (6.168,16.048)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U33 (AND2X1_RVT)
  Input location: (1.152,11.032)
  Legal location: (1.152,11.032)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U30 (AND2X1_RVT)
  Input location: (2.368,14.376)
  Legal location: (2.368,14.376)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U26 (AND2X1_RVT)
  Input location: (4.04,11.032)
  Legal location: (4.04,11.032)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U24 (AND2X1_RVT)
  Input location: (6.776,9.36)
  Legal location: (6.776,9.36)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U50 (AND2X1_RVT)
  Input location: (14.984,9.36)
  Legal location: (14.984,9.36)
  Displacement: 0.000 um ( 0.00 row height)

-----
PATHGROUP QOR
-----
Scene PG      WNS      TNS      NSV      WHV      THV      NHV
  1   0.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0
  1   2.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0
  1   3.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0
  1   4.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0
  1   5.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0
  1   6.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0
  1   7.0000    0.0000    0.0000    0.0000    0.0000    0.0000    0

SCENARIO QOR
-----
Scene PG      WNS      TNS      R2RTNS     NSV      WHV      THV      NHV      MaxTrnV      MaxTranC      MaxCapV      Leakage
  1   * 0.0000  0.0000  0.0000    0   0.0000  0.0000    0.0000    0.0000    0.0000    0.0000    0.0000  523537632
-----
DESIGN QOR
-----
Scene PG      WNS      TNS      R2RTNS     NSV      WHV      THV      NHV      MaxTrnV      MaxTranC      MaxCapV      Leakage      Area      InstCnt      BufCnt
InvCnt      * 0.0000  0.0000  0.0000    0   0.0000  0.0000    0.0000    0.0000    0.0000    0.0000    0.0000  523537632  251.35       112          0
  27

Place-opt final QoR Summary      WNS      TNS      R2RTNS     NSV      WHV      THV      NHV      MaxTrnV      MaxCapV      Leakage      Area      InstCnt
Place-opt final QoR Summary  0.0000  0.0000  0.0000    0   0.0000  0.0000    0.0000    0.0000    0.0000    0.0000    0.0000  251.35       112

Place-opt command complete      CPU: 193 s ( 0.05 hr )  ELAPSE: 5284 s ( 1.47 hr )  MEM-PEAK: 993 MB
Place-opt command statistics  CPU=14 sec (0.00 hr)  ELAPSED=112 sec (0.03 hr)  MEM-PEAK=0.970 GB
[Tim-Power] Info: Cleared Leakage libCell cache.
[Tim-Power] Info: Cleared Leakage libCell cache.
Information: Running auto PG connection. (NDM-099)
Information: Ending 'place_opt' (FLW-8001)
Information: Time: 2024-07-11 02:15:41 / Session: 01:28:06 / Command: 00:03:31 / CPU: 00:00:31 / Memory: 993 MB (FLW-8100)
1

```

'legalize_placement' – It is used to ensure that the placement of cells in the core area adheres to the design rules and constraints. It includes adjustment of cell positions to eliminate overlap and other rules.

```

icc2_shell> legalize_placement
Information: Starting 'legalize_placement' (FLW-8000)
Information: Time: 2024-07-11 02:52:05 / Session: 02:04:30 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 993 MB (FLW-8100)
nplDplc2Placer::setParam(effort,1)
nplDplc2Placer::setParam(debug,0)
nplDplc2Placer::setParam(site_check,2)
nplDplc2Placer::setParam(app_wgt,0)
Warning: Routing direction of metal layer P0 is neither "horizontal" nor "vertical". PDC checks will not be performed on this layer. (PDC-003)
PDC app_options settings ======
    place.legalize.enable_prerouted_net_check: 1
    place.legalize.num_tracks_for_access_check: 1
    place.legalize.use_eol_spacing_for_access_check: 0
    place.legalize.allow_touch_track_for_access_check: 1
    place.legalize.reduce_conservatism_in_eol_check: 0
    place.legalize.preroute_shape_merge_distance: 0.0
    place.legalize.enable_non_preferred_direction_span_check: 0

Layer M1: cached 0 shapes out of 13 total shapes.
Layer M2: cached 91 shapes out of 91 total shapes.
Cached 182 vias out of 711 total vias.

Legalizing Top Level Design CLA1 ...
Information: Initializing classic cellmap without advanced rules enabled and without PDC enabled
Information: The following app options are used in cellmap
    place.legalize.enable_color_aware_placement : false
    place.legalize.use_nll_query_cm : false
    place.legalize.enable_advanced_legalizer : false
    place.legalize.enable_prerouted_net_check : true
    place.legalize.enable_advanced_prerouted_net_check : false
    place.legalize.always_continue : true
    place.legalize.limit_legality_checks : false
    place.common.pnet_aware_density : 1.0000
    place.common.pnet_aware_min_width : 0.0000
    place.common.pnet_aware_layers : []
    place.common.use_placement_model : false
    place.common.use_placement_model : false
    place.common.enable_advanced_placement_model : true
    cts.placement.cell_spacing_rule_style : maximum
Total 0.0300 seconds to build cellmap data
Information: Creating classic rule checker.
Warning: Routing direction of metal layer P0 is neither "horizontal" nor "vertical". PDC checks will not be performed on this layer. (PDC-003)
=====> Processed 15 ref cells (8 fillers) from library

Bounds/Regions In This Design:
  Area      Num Cells  Exclusive Name
  (square um)
  430.012       112      Yes DEFAULT_VA

Starting legalizer.
Warning: Exclusive bound 'DEFAULT' has no cells.
Optimizing Exclusive Bound 'DEFAULT_VA' (2/2)
  Done Exclusive Bound 'DEFAULT_VA' (2/2) (0 sec)
Legalization complete (0 total sec)

*****
Report : Placement Attempts
Site   : unit
*****
number of cells:          112
number of references:     15
number of site rows:      12
number of locations attempted: 1471
number of locations failed: 0 (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

*****

```

```

Report : Cell Displacements
*****
number of cells aggregated:      112 (989 total sites)
avg row height over cells:     1.672 um
rms cell displacement:        0.000 um ( 0.00 row height)
rms weighted cell displacement: 0.000 um ( 0.00 row height)
max cell displacement:        0.000 um ( 0.00 row height)
avg cell displacement:        0.000 um ( 0.00 row height)
avg weighted cell displacement: 0.000 um ( 0.00 row height)
number of cells moved:          0
number of large displacements:   0
large displacement threshold:    3.000 row height

Displacements of worst 10 cells:
Cell: U45 (AND2X1_RVT)
  Input location: (5.56,11.032)
  Legal location: (5.56,11.032)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U42 (AND2X1_RVT)
  Input location: (6.776,7.688)
  Legal location: (6.776,7.688)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U40 (AND2X1_RVT)
  Input location: (1.912,16.048)
  Legal location: (1.912,16.048)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U35 (AND2X1_RVT)
  Input location: (2.216,6.016)
  Legal location: (2.216,6.016)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U4 (AND2X1_RVT)
  Input location: (6.168,16.048)
  Legal location: (6.168,16.048)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U33 (AND2X1_RVT)
  Input location: (1.152,11.032)
  Legal location: (1.152,11.032)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U30 (AND2X1_RVT)
  Input location: (2.368,14.376)
  Legal location: (2.368,14.376)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U26 (AND2X1_RVT)
  Input location: (4.04,11.032)
  Legal location: (4.04,11.032)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U24 (AND2X1_RVT)
  Input location: (6.776,9.36)
  Legal location: (6.776,9.36)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U50 (AND2X1_RVT)
  Input location: (14.984,9.36)
  Legal location: (14.984,9.36)
  Displacement:  0.000 um ( 0.00 row height)

Legalization succeeded.
Total Legalizer CPU: 0.209
Total Legalizer Wall Time: 1.453
-----
Information: Ending  'legalize_placement' (FLW-8001)
Information: Time: 2024-07-11 02:52:06 / Session: 02:04:31 / Command: 00:00:01 / CPU: 00:00:00 / Memory: 993 MB (FLW-8100)
1

```

Now, save the block and lib

```

icc2_shell> save_block
Information: The command 'save block' cleared the undo history. (UNDO-016)
Information: Saving block 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'
1
icc2_shell> save_lib
Saving library 'EIGHT_BIT_ADDER_LIB1'
1

```

‘report_design’– It generates the report of the design which describes about the area, different type of cells in the design.

```
iccc2_shell> report_design
*****
Report : design
Design : CLA1
Version: V-2023.12
Date   : Thu Jul 11 02:59:03 2024
*****



Total number of std cells in library : 286
Total number of dont use lib cells : 85
Total number of dont_touch lib cells : 7
Total number of buffers : 11
Total number of inverters : 15
Total number of flip-flops : 106
Total number of latches : 12
Total number of ICGs : 12

Cell Instance Type Count Area
-----
TOTAL LEAF CELLS 112 251.348
unit 112 251.348
Standard cells 112 251.348
unit 112 251.348
Hard macro cells 0 0.000
unit 112 251.348
Soft macro cells 0 0.000
unit 112 251.348
Always on cells 0 0.000
unit 112 251.348
Physical only 0 0.000
unit 112 251.348
Fixed cells 0 0.000
unit 112 251.348
Moveable cells 112 251.348
unit 112 251.348
Placed cells 112 251.348
unit 112 251.348
Sequential 9 59.470
unit 112 251.348
Buffer/inverter 27 34.309
unit 112 251.348
ICG cells 0 0.000
unit 112 251.348

Logic Hierarchies : 0
Design Masters count : 7
Total Flat nets count : 132
Total FloatingNets count : 0
Total no of Ports : 38
Number of Master Clocks in design : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design : 7 (1 of them Non Default)
Number of Scan Chains in design : 0
List of Modes : func
List of Corners : nom
List of Scenarios : func::nom

Core Area : 430.012
Chip Area : 517.004
Total Site Row Area : 430.012
Number of Blockages : 1
Total area of Blockages : 42.994
Number of Power Domains : 1
Number of Voltage Areas : 1
Number of Group Bounds : 0
Number of Exclusive MoveBounds : 0
Number of Hard or Soft MoveBounds : 0
Number of Multibit Registers : 0
Number of Multibit LS/ISO Cells : 0
Number of Top Level RP Groups : 0
Number of Tech Layers : 71 (61 of them have unknown routing dir.)

Total wire length : 0.00 micron
Total number of wires : 0
Total number of contacts : 711
1
```

'report_timing' – It describes about the slack, timing path and delays of the saved design after the placement stage.

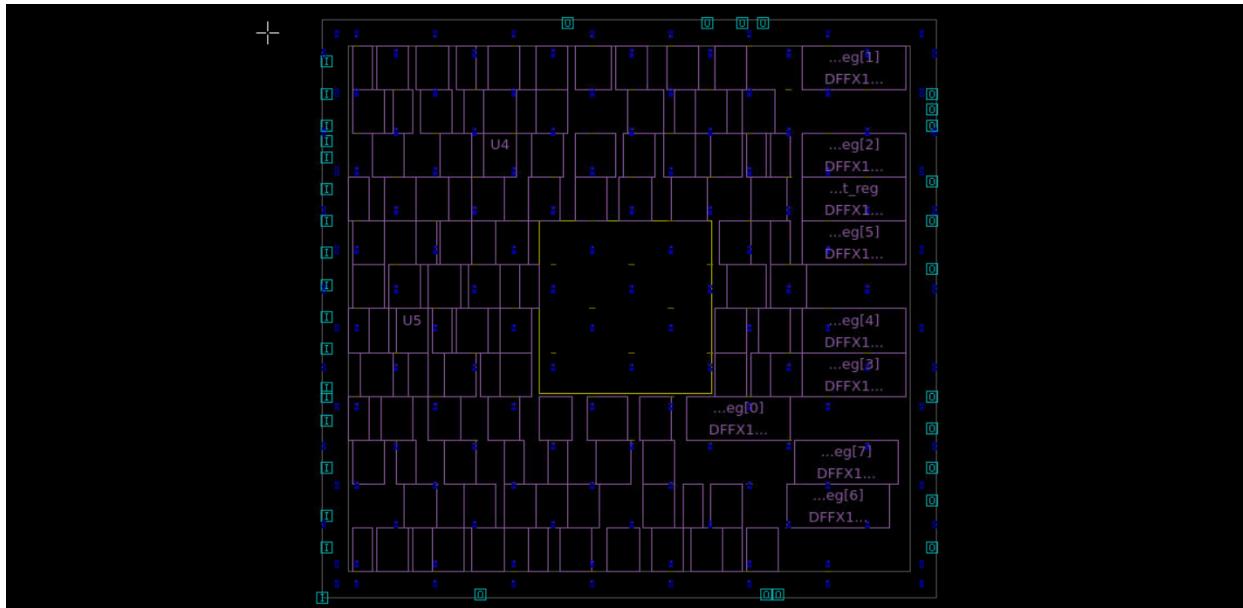
```
icc2_shell> report_timing
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -report_by design
Design : CLA1
Version: V-2023.12
Date   : Thu Jul 11 03:02:20 2024
*****
Startpoint: a[0] (input port clocked by clk)
Endpoint: sum[7] (output port clocked by clk)
Mode: func
Corner: nom
Scenario: func::nom
Path Group: **inout_default**
Path Type: max
Point           Incr    Path
-----
clock clk (rise edge)      0.00  0.00
clock network delay (ideal) 0.00  0.00
input external delay        0.60  0.60 f
a[0] (in)                  0.00  0.60 f
U3/Y (INVX1_RVT)           0.03  0.63 r
U5/Y (OR2X1_RVT)           0.04  0.67 r
U35/Y (AND2X1_RVT)          0.03  0.71 r
U37/Y (OR2X1_RVT)           0.03  0.74 r
U38/Y (INVX0_RVT)           0.02  0.76 f
U39/Y (OR2X1_RVT)           0.03  0.79 f
U4/Y (AND2X1_RVT)           0.04  0.83 f
cmTdsLR-1-3/Y (OR3X2_RVT)   0.03  0.86 f
cmTdsLR-1-7/Y (AND3X1_RVT)  0.04  0.90 f
cmTdsLR-1-8/Y (AND3X1_RVT)  0.05  0.95 f
cmTdsLR-1-10/Y (OR3X2_RVT)  0.04  0.99 f
cmTdsLR-1-1/Y (AND3X1_RVT)  0.04  1.03 f
U101/Y (INVX0_RVT)          0.02  1.07 r
U102/Y (AND2X1_RVT)          0.03  1.07 r
sum[7] (out)                 0.00  1.07 r
data arrival time            1.07
-----  

clock clk (rise edge)      1.00  1.00
clock network delay (ideal) 0.00  1.00
clock uncertainty           1.20  2.20
output external delay        -0.40 1.80
data required time           1.80
-----  

data required time           1.80
data arrival time            -1.07
-----  

slack (MET)                  0.73
1
```

Output of placement stage :



Commands for placement –

```
46 set PDK_PATH ../../ref
47 check_design -checks pre_placement_stage
48 current_mode
49 remove_modes -all; remove_corners -all; remove_scenarios -all
50 set model "func"
51 set corner1 "nom"
52 set scenario1 "${model}::${corner1}"
53 create_mode $model
54 create_corner $corner1
55 create_scenario -name func::nom -mode func -corner nom
56 report_scenarios
57 source ./CONSTRAINTS/CLAI.sdc
58 set dont_use [get_lib_cells */FADD*]
59 set dont_use [get_lib_cells */HADD*]
60 set dont_use [get_lib_cells */A0*]
61 set dont_use [get_lib_cells */OA*]
62 set dont_use [get_lib_cells */NAND*]
63 set dont_use [get_lib_cells */XOR*]
64 set dont_use [get_lib_cells */NOR*]
65 set dont_use [get_lib_cells */XNOR*]
66 set dont_use [get_lib_cells */MUX*]
67 set parasitic1 "P1"
68 set tluplus_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmax.tluplus"
69 set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
70 set parasitic2 "P2"
71 set tluplus_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmin.tluplus"
72 set layer_map_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
73 read_parasitic_tech -tlup $tluplus_file$parasitic1 -layermap $layer_map_file$parasitic1 -name p1
74 read_parasitic_tech -tlup $tluplus_file$parasitic2 -layermap $layer_map_file$parasitic2 -name p2
75 set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2
76 set_app_options -name place.coarse.continue_on_missing_scandef -value true
77 place_pins -self
78 place_pins
79 place_opt
80 legalize_placement
81 save_block
82 save_lib
83 report_design
84 report_timing
85 history
icc2_shell> █
```

6.Clock Tree Synthesis

- **Distribution of Clock to Entire Circuit:** Ensure the clock signal reaches every sequential circuit with minimal skew.
- **Synthesize Clock Tree:** Generate a network of buffers and drivers to distribute the clock signal across the entire circuit with minimal skew.

```
icc2 shell> check_design -checks pre_clock_tree_stage
*****
Report : check_design
Options: { pre_clock_tree_stage }
Design : CLAI
Version : V-2023.12
Date   : Thu Jul 11 04:30:07 2024
*****  
  
Running mega-check 'pre_clock_tree_stage';
  Running atomic-check 'design_mismatch'
  Running atomic-check 'scan_chain'
  Running atomic-check 'mv_design'
  Running atomic-check 'legality'
  Running atomic-check 'timing'
  Running atomic-check 'clock_trees'
  Running atomic-check 'hier_pre_clock_tree'  
  
*** EMS Message summary ***  
-----  
Rule      Type  Count   Message  
-----  
CTS-914   Warn   1       set_input_transition %constraint on clock port %port exceeds the...  
DFT-011   Info   1       The design has no scan chain defined in the scandef.  
-----  
Total 2 EMS messages : 0 errors, 1 warnings, 1 info.  
  
*** Non-EMS message summary ***  
-----  
Rule      Type  Count   Message  
-----  
CTS-101   Info   1       %s will work on the following scenarios.  
CTS-107   Info   1       %s will work on all clocks in active scenarios, including %d mas...  
CTS-973   Info   1       The value of option cts.compile.enable_cell_relocation has been ...  
PDC-003   Warn   2       Routing direction of metal layer %s is neither "horizontal" nor ...  
-----  
Total 5 non-EMS messages : 0 errors, 2 warnings, 3 info.  
  
Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)  
Information: EMS database is saved to file 'check_design.ems'.  
Information: Non-EMS messages are saved into file 'check_design2024Jul11043005.log'.  
1  
icc2 shell> synthesize_clock_tree
Information: Starting 'synthesize_clock_trees' (FLW-8000)
Information: Time: 2024-07-11 04:41:15 / Session: 03:53:40 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 993 MB (FLW-8100)
Information: The value of option cts.compile.enable_cell_relocation has been overridden to "leaf_only" to support latency-driven placement. (CTS-973)
*****  
* CTS STEP: Design Initialization for Clock Synthesis
*****  
Information: All clock objects will be converted from ideal to propagated clock during CTS. (CTS-105)
Information: CTS will work on the following scenarios. (CTS-101)
  func::nom  (Mode: func; Corner: nom)
Information: CTS will work on all clocks in active scenarios, including 1 master clocks and 0 generated clocks. (CTS-107)
Output units used in this log:
  Time    : 1.00ns
  Resistance : 1.00MΩ
  Capacitance : 1.00fF
  Power     : 1.00pW
  Length    : 1.00um
Information: Clock derating is disabled
CTS related app options set by user:
  No CTS related app option is set.
Buffer/Inverter reference list for clock tree synthesis:
  saed32rvt c/DELLN1X2 RVT
```

```

saed32rvt_c/DELLN2X2_RVT
saed32rvt_c/DELLN3X2_RVT
saed32rvt_c/NBUFFX16_RVT
saed32rvt_c/NBUFFX2_RVT
saed32rvt_c/NBUFFX32_RVT
saed32rvt_c/NBUFFX4_RVT
saed32rvt_c/NBUFFX8_RVT
saed32rvt_c/IBUFX16_RVT
saed32rvt_c/IBUFX2_RVT
saed32rvt_c/IBUFX32_RVT
saed32rvt_c/IBUFX4_RVT
saed32rvt_c/IBUFX8_RVT
saed32rvt_c/INVX0_RVT
saed32rvt_c/INVX16_RVT
saed32rvt_c/INVX1_RVT
saed32rvt_c/INVX2_RVT
saed32rvt_c/INVX32_RVT
saed32rvt_c/INVX4_RVT
saed32rvt_c/INVX8_RVT

ICG reference list:
saed32rvt_c/CGLNPRX2_RVT
saed32rvt_c/CGLNPRX8_RVT
saed32rvt_c/CGLNPSX16_RVT
saed32rvt_c/CGLNPSX2_RVT
saed32rvt_c/CGLNPSX4_RVT
saed32rvt_c/CGLNPSX8_RVT
saed32rvt_c/CGLPPRX2_RVT
saed32rvt_c/CGLPPRX8_RVT
saed32rvt_c/CGLPPSX16_RVT
saed32rvt_c/CGLPPSX2_RVT
saed32rvt_c/CGLPPSX4_RVT
saed32rvt_c/CGLPPSX8_RVT

Information: 'nom' is identified as primary corner for initial clock tree building. (CTS-103)
Number of Site types in the design = 1
Setting up Chip Core
Chip Core shape: (10000 10000) (224320 210640)
Number of VARs = 1
Number of unique PDs = 1
Number of Power Domains = 1
Number of Voltage Areas = 1
Number of supply Nets = 2
Number of used supplies = 0
Blocked VAs:
Warning: No clock routing rule is specified. (CTS-038)

Clock cell spacing rule list:
No clock cell spacing rule is found.
Information: The run time for design initialization is 0 hr : 0 min : 0.70 sec, cpu time is 0 hr : 0 min : 0.15 sec. (CTS-104)
*****
* CTS STEP: Existing Clock Tree Removal
*****
No buffer or inverter has been removed.
Information: The run time for design initialization is 0 hr : 0 min : 0.70 sec, cpu time is 0 hr : 0 min : 0.15 sec. (CTS-104)
*****
* CTS STEP: Existing Clock Tree Removal
*****
No buffer or inverter has been removed.
Information: The run time for existing clock tree removal is 0 hr : 0 min : 0.00 sec, cpu time is 0 hr : 0 min : 0.00 sec. (CTS-104)
*****
* CTS STEP: Clock Tree Initialization
*****
Drc Mode Option: auto
Information: Initializing classic cellmap without advanced rules enabled and with PDC enabled
Information: The following app options are used in cellmap
    place.legalize.enable_color_aware_placement : false
    place.legalize.use_nlt_query_cm : false
    place.legalize.enable_advanced_legalizer : false
    place.legalize.enable_prerouted_net_check : true
    place.legalize.enable_advanced_prerouted_net_check : false
    place.legalize.always_continue : true
    place.legalize.limit_Tegality_checks : false
    place.common.pnet_aware_density : 1.0000
    place.common.pnet_aware_min_width : 0.0000
    place.common.pnet_aware_layers : {}
    place.common.use_placement_model : false
    place.common.enable_advanced_placement_model : true
    cts.placement.cell_spacing_rule_style : maximum
Information: Creating classic rule checker.
Warning: Routing direction of metal layer P0 is neither "horizontal" nor "vertical". PDC checks will not be performed on this layer. (PDC-003)
PDC app_options settings =====
    place.legalize.enable_prerouted.net_check: 1
    place.legalize.num_tracks_for_access_check: 1

```

```

place.legalize.use_eol_spacing_for_access_check: 0
place.legalize.allow_touch_track_for_access_check: 1
place.legalize.reduce_conservatism_in_eol_check: 0
place.legalize.preroute_shape_merge_distance: 0.0
place.legalize.enable_non_preferred_direction_span_check: 0

Layer M1: cached 0 shapes out of 13 total shapes.
Layer M2: cached 91 shapes out of 91 total shapes.
Cached 182 vias out of 711 total vias.
Total 0.0400 seconds to build cellmap data
INFO: creating 3(r) x 3(c) GridCells YDim 8.36 XDim 8.36
INFO: number of GridCells (0x992f1c20): 9
INFO: creating 3(r) x 3(c) GridCells YDim 8.36 XDim 8.36
INFO: number of GridCells (0x992f0bd0): 9
Total 0.0000 seconds to load 112 cell instances into cellmap
Moveable cells: 112; Application fixed cells: 0; Macro cells: 0; User fixed cells: 0
Average cell width 1.3422, cell height 1.6720, cell area 2.2442 for total 112 placed and application fixed cells
Information: Legalizer's PDC rule check is enabled
Information: Legalizer's advanced rule check is enabled
Corner Scaling is off, multiplier is 1.000000
ORB Clustering Route Center Bias is on
Automatic Zbuf-CTS Mode: total_powerInformation: Running Max-CTS

Start Auto-Exception Derivations...
No internal pin was found.
No conflict pin was found.
No macro pin was found for clock balance point settings.
No macro pin was found for disabling self arcs.
Info: 9 sinks and boundary insts are collected
Information: The run time for clock tree initialization is 0 hr : 0 min : 0.48 sec, cpu time is 0 hr : 0 min : 0.12 sec. (CTS-104)
Drc Mode Option: auto
Corner Scaling is off, multiplier is 1.000000
ORB Clustering Route Center Bias is on
Automatic Zbuf-CTS Mode: total_powerInformation: Running Max-CTS
Enable multi-thread Tasks, number of thread is 1
Info: run cts with the following settings: _runCts 1 _runCto 1 _runSnapClockSinks 1
Information: The stitching and editing of coupling caps is turned OFF for design 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'. (TIM-125)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 130, routed nets = 0, across physical hierarchy nets = 0, parasitics cached nets = 1, delay annotated nets = 0, parasitics annotated nets = 0, multi-voltage nets = 0. (TIM-112)
*****
* CTS STEP: Clock Cell Relocation
*****
A total of 0 clock cells have been relocated
Information: The run time for clock cell relocation is 0 hr : 0 min : 0.01 sec, cpu time is 0 hr : 0 min : 0.00 sec. (CTS-104)
Information: The run time for netlink placement is 0 hr : 0 min : 0.00 sec, cpu time is 0 hr : 0 min : 0.00 sec. (CTS-104)
*****
* CTS STEP: Gate-by-Gate Clock Tree Synthesis
*****
Design rule constraints:
    max_fanout = 1000000
Computing criticality for all echelons
Warning: No clock routing rules were specified. Use set_clock_routing_rules to specify routing rules for accurate clock latency estimation. (OPT-902)
Num of echelons 1
Level 0 Num Nodes: 1
Processing Echelon 1
Processing parameter set (max_tran 0.10000 max_cap 0.600000)
Design scenario: CTS_DRC_OFF_SCEN0 (corner = nom, mode = func)
Zbuf-HFS: gathering all scenarios
Scenario: Active:Y Setup:Y Leakage:Y Dynamic:Y MaxTran:N (-1) MaxCap:N (-1) Hold:Y Scen=CTS_DRC_OFF_SCEN0 (func:nom)
Zbuf Constraints: maxTran=inf maxCap=inf
Max-CTS: All active scenarios
    Mode: func Corner: nom Scenario: CTS_DRC_OFF_SCEN0
Max-CTS: All active leakage power scenarios
    Mode: func Corner: nom Scenario: CTS_DRC_OFF_SCEN0
Max-CTS: All active dynamic power scenarios
    Mode: func Corner: nom Scenario: CTS_DRC_OFF_SCEN0
orb constraints: using power mt scenarios
ORB: timingScenario CTS_DRC_OFF_SCEN0 timingCorner nom
INFO: Using corner nom for worst leakage corner
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Warning: No default voltage defined in the design, taking it as zero for power calculations. (POW-080)
Note - message 'POW-080' limit (10) exceeded. Remainder will be suppressed.
INFO: Using corner nom for worst dynamic corner
Using default layer M4
new cutoff lpd: 2.13467e-02
corner scaling: maxCornerId = 1
corner=nom, tran factor=1.000000 (0.085493 / 0.085493)
ORB: Nominal = 0.0285335 Design MT = 0.095000 Target = 0.0854931 (2.996 nominal) MaxRC = 0.057861
ORB: Fast Target = 0.037050 ( 1.298 nominal )
ORB: stageDelay=0.059042, stageLength=4488435
bmap: stepx = stepy = 83600
creating bmap
DB units per micron : 10000
Core Area = 3 X 3 ()
    10% ...Number of Drivers Sized: 0 [0.00%]

```

```

Echelon 1 gate by gate clock synthesis
Gate level 1 clock tree synthesis
Driving pin = clk
Clocks:
  clk (func)
Design rule constraints:
  max transition = 0.100000
  max capacitance = 600.000000
Number of Sinks = 9
Number of Gates = 8
Number of Loads = 9
Added 0 Repeaters (B: 0 I: 0). Built 0 Repeater Levels for driver clk
Phase delay: (max r/f: 0.000420/nan min r/f: 0.000420/nan) : clk
Information: The run time for gate-by-gate clock tree synthesis is 0 hr : 0 min : 1.54 sec, cpu time is 0 hr : 0 min : 0.95 sec. (CTS-104)
*****
* CTS STEP: DRC Fixing Beyond Exceptions
*****
Design rule constraints:
  max fanout = 1000000
Num of echelons 0
Information: The run time for DRC fixing beyond exceptions is 0 hr : 0 min : 0.04 sec, cpu time is 0 hr : 0 min : 0.04 sec. (CTS-104)
There are 0 buffers and 0 inverters added (total area 0.00) by Clock Tree Synthesis.
Information: 0 out of 0 clock cells have been moved due to NDR or via ladder related legalization rules.
Info: Clock cell and register co-legalization is disabled since advanced legalizer is disabled.
=====Displacement Report for clock sink=====
Clock sink moved: 0 out of 9, orientation changed without moving: 0
Clock sink displacement max = 0.000000 um, average = 0.000000 um
Clock sink with large displacement: 0 (Threshold: 5.016000 um)
=====
Information: The run time for snapping registers is 0 hr : 0 min : 0.00 sec, cpu time is 0 hr : 0 min : 0.00 sec. (CTS-104)
*****
* CTS STEP: Clock Net Global Routing
*****
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = MRDL
Turn off antenna since no rule is specified
Turn off antenna since no rule is specified
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer C0. (ZRT-022)
Warning: Port VDD of cell eight_bit_adder.v
  is unplaced. This may impact routing result. (ZRT-740)
Warning: Port VSS of cell eight_bit_adder.v
  is unplaced. This may impact routing result. (ZRT-740)
Warning: Ignore 2 top cell ports with no pins. (ZRT-027)
Info: number of net_type_blockage: 0
Information: Via ladder engine would be activated for pattern must join connection in certain commands. Please refer to man-page for the command list. (ZRT-619)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)
Performing initial clock net global routing ...
Loading parasitics information to the router ...
parasitics information loaded to the router.
[End of Loading Timing] Elapsed real time: 0:00:00
[End of Loading Timing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
Information: The net parasitics of block CLA1 are cleared. (TIM-123)
Total number of global routed clock nets: 1
Information: The run time for clock net global routing is 0 hr : 0 min : 3.17 sec, cpu time is 0 hr : 0 min : 0.60 sec. (CTS-104)
Information: The stitching and editing of coupling caps is turned OFF for design 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'. (TIM-125)
Information: Design eight_bit_adder.v has 132 nets, 1 global routed, 0 detail routed. (NEX-024)
Information: The RC mode used is CTO for design 'CLA1'. (NEX-022)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 130, routed nets = 1, across physical hierarchy nets = 0, parasitics cached nets = 1, delay annotated nets = 0, parasitics annotated nets = 0, multi-voltage nets = 0. (TIM-112)
Information: The netlist change observers are disabled for incremental timing updates. (TIM-119)
Information: The netlist change observers are disabled for incremental extraction. (TIM-126)
CTSSC route status detected: clock (VR 0, GR 19, DR 0), data (VR 129, GR 0, DR 0); stage = auto, isPostRoute = FALSE
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = MRDL
Turn off antenna since no rule is specified
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer C0. (ZRT-022)
Warning: Port VDD of cell eight_bit_adder.v
  is unplaced. This may impact routing result. (ZRT-740)
Warning: Port VSS of cell eight_bit_adder.v
  is unplaced. This may impact routing result. (ZRT-740)
Warning: Ignore 2 top cell ports with no pins. (ZRT-027)
Info: number of net_type_blockage: 0
Information: Via ladder engine would be activated for pattern must join connection in certain commands. Please refer to man-page for the command list. (ZRT-619)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)
GR Routing Service: Started IMRD
GR Routing Service: ndmAttrDef 'usr_tmng_crit' created with default value 0
GR Routing Service: ndmAttrDef 'rtd_by_minDly' created with default value 0
GR Routing Service: ndmAttrDef 'port_subnet_crit_blkConn' created with default value 0
GR Routing Service: ndmAttrDef 'port_subnet_crit_blkPort' created with default value 0
Loading timing information to the router ...
Design Scenario func::nom (Mode func Corner nom)
Timing information loaded to the router.
GR Routing Service: Setting costIdx to 3
GR Routing Service: rebuildCongmap: itr = 3
Number of partitions: 1 (1 x 1)
Size of partitions: 14 gCells x 14 gCells
Average gCell capacity 3.15 on layer (1) M1
Average gCell capacity 9.78 on layer (2) M2
Average gCell capacity 4.62 on layer (3) M3
Average gCell capacity 4.83 on layer (4) M4
Average gCell capacity 2.41 on layer (5) M5
Average gCell capacity 2.02 on layer (6) M6
Average gCell capacity 0.71 on layer (7) M7
Average gCell capacity 0.85 on layer (8) M8
Average gCell capacity 0.57 on layer (9) M9
Average gCell capacity 0.21 on layer (10) MRDL

```

```

Average number of tracks per gCell 10.43      on layer (1)    M1
Average number of tracks per gCell 11.07      on layer (2)    M2
Average number of tracks per gCell 5.29      on layer (3)    M3
Average number of tracks per gCell 5.64      on layer (4)    M4
Average number of tracks per gCell 2.71      on layer (5)    M5
Average number of tracks per gCell 2.86      on layer (6)    M6
Average number of tracks per gCell 1.43      on layer (7)    M7
Average number of tracks per gCell 1.50      on layer (8)    M8
Average number of tracks per gCell 0.79      on layer (9)    M9
Average number of tracks per gCell 0.36      on layer (10)   MRDL
Number of gCells = 1960
[updNetsDmd] Elapsed real time: 0:00:00
[updNetsDmd] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
Created 1 thread routing service with costIdx = 3. (tbbMode 0)
GR Routing Service: Setting costIdx to 1
rtapi Thread-server 0: startup
Mgr Thread-server 0: Ctor
*****
* CTS STEP: Initial DRC fixing
*****
[cto] Starting InitDrc.1
start cto; name: eight_bit_adder.v; type: design; tot_drc_vio: 1; buf_ct: 0; buf_area: 0.000000; cell_area: 0.000000
start cto; name: func:clk; type: clock; latency: 0.000381; gskew: 0.000134; tot_drc_vio: 1; wtran: 0.049992; wcap: 0.000000; buf_ct: 0; buf_area: 0.000000; cell_area: 0.000000
-----
Optimizing clock tree DRC
clock: clk mode: func root: clk
Clock QoR Before DRC Optimization:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Pre Initial DRC Fixing: GlobalSkew = 0.0001; ID = 0.0004; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 0;
Clock QoR Before DRC Optimization:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Pre Initial DRC Fixing: GlobalSkew = 0.0001; ID = 0.0004; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 0;
ClockBufArea = 0.0000; ClockCellArea = 0.0000; ClockWireLen = 37.5880; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)

Begin Pre-Opt Drc Fixing
Starting multithread based drc fixing Pre opt drc fixing
Iteration 1 (effort: high)
Iteration 2 (effort: high)

Optimization Summary
-----
# Drivers Attempted      =      1
# Skipped during isValid and estimate      =      0
# Failed subgraph evaluation      =      0
# Failed main graph commit      =      0
# Successful main graph commit      =      1
# Subgraph evaluation success rate in percent = 1.0000
# Sg2Main acceptance ratio in percent      = 1.0000
# NumCTCells changed      =      1

# Accepted      buffering moves =      1

# Total CPU time      = 00h:00m:00s
# Total elapsed time      = 00h:00m:07s
# Flow total speed up      = 0.0058
# Commit CPU time      = 00h:00m:00s
# Commit elapsed time      = 00h:00m:02s
# Commit speed up      = 0.0496
# Generator CPU time      = 00h:00m:00s
# Generator elapsed time      = 00h:00m:00s
# Generator speed up      = 0.1151
# Sg CPU time      = 00h:00m:00s
# Sg elapsed time      = 00h:00m:03s
# Sg speed up      = 0.1019
# The rest of flow speed up      = 0.1031

-----
Pre-Opt drc fixing cpu time 00:00:00.87u 00:00:00.03s 00:00:09.07e:
Clock QoR After Pre-Opt Drc Fixing:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Post Initial DRC Fixing: GlobalSkew = 0.0002; ID = 0.0383; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 1;
ClockBufArea = 6.0995; ClockCellArea = 6.0995; ClockWireLen = 35.6380; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)
The elapsed time for optimization of clock tree is 0 hr : 0 min : 9.50 sec, cpu time is 0 hr : 0 min : 0.93 sec.
Information: The run time for Initial DRC fixing is 0 hr : 0 min : 9.61 sec, cpu time is 0 hr : 0 min : 0.94 sec. (CTS-104)
[cto] Finished InitDrc.1: PASS
*****
* CTS STEP: Path-based global latency and skew optimization
*****
[cto] Starting GLS.1
Select the tightest corner nom on transition constraint
Selecting clock clk mode func corner: nom
-----
Optimizing clock tree global latency and skew

```

```

clock: clk mode: func root: clk
Clock QoR Before Global latency and skew opt:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Pre Optimization: GlobalSkew = 0.0002; ID = 0.0383; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 1; ClockBufArea = 6.0995; ClockCellArea = 6.0995; ClockWireLen = 35.6380; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)

Begin Global Latency and Skew Optimization
Starting multithread based global latency and skew optimization

Optimization Summary

-----
# Drivers Attempted          =      3          # Skipped during isValid and estimate =      0
# Failed subgraph evaluation =      2          # Failed main graph committ       =      0
# Successful main graph commit =      1          # Subgraph evaluation success rate in percent =  0.3333
# Sg2Main acceptance ratio in percent =  1.0000
# NumCTCells changed        =      -1

# Accepted removal moves =      1

# Total CPU time           = 00h:00m:00s
# Total elapsed time       = 00h:00m:09s
# Flow total speed up     =  0.0823
# Commit CPU time         = 00h:00m:00s
# Commit elapsed time     = 00h:00m:02s
# Commit speed up         =  0.0415
# Generator CPU time     = 00h:00m:00s
# Generator elapsed time = 00h:00m:00s

# Generator speed up      =  0.3920
# Sg CPU time              = 00h:00m:00s
# Sg elapsed time          = 00h:00m:06s
# Sg speed up               =  0.0831
# The rest of flow speed up =  0.0937

-----
Optimization Summary

-----
# Drivers Attempted          =      2          # Skipped during isValid and estimate =      0
# Failed subgraph evaluation =      2          # Failed main graph committ       =      0
# Successful main graph commit =      0          # Subgraph evaluation success rate in percent =  0.0000
# NumCTCells changed        =      0

# Total CPU time           = 00h:00m:00s
# Total elapsed time       = 00h:00m:00s
# Flow total speed up     =  0.5257

-----
Global latency and skew opt cpu time 00:00:00.24u 00:00:01.02s 00:00:11.13e:
Clock QoR After Global latency and skew opt:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Post Network Flow Optimization: GlobalSkew = 0.0001; ID = 0.0004; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 0; ClockBufArea = 0.0000; ClockCellArea = 0.0000; ClockWireLen = 36.5710; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)
Longest path:
(0) 0.0004    0.0000    fsum_reg[1]/CLK
Shortest path:
(0) 0.0002    0.0000    fsum_reg[0]/CLK
The elapsed time for optimization of clock tree is 0 hr : 0 min : 11.65 sec, cpu time is 0 hr : 0 min : 1.34 sec.
Information: The run time for Path-based global latency and skew optimization is 0 hr : 0 min : 11.77 sec, cpu time is 0 hr : 0 min : 1.43 sec. (CTS-104)
[cto] Finished GLS.1: PASS
*****
* CTS STEP: Area recovery
*****
[cto] Starting AR.1
Select the tightest corner nom on transition constraint
Selecting clock clk mode func corner: nom
-----
Optimizing clock tree area
clock: clk mode: func root: clk
Starting multithread based area recovery and subtree balancing
Iteration 2 (effort: low)

Optimization Summary

-----
# Drivers Attempted          =      0          # Skipped during isValid and estimate =      0
# Failed subgraph evaluation =      0          # Failed main graph committ       =      0
# Successful main graph commit =      0          # NumCTCells changed        =      0

# Total CPU time           = 00h:00m:00s

```

```

# Total elapsed time      = 00h:00m:00s
# Flow total speed up    =     0.1309

-----
Clock QoR After Area Recovery and Subtree Balancing:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Post Area Recovery Resizing: GlobalSkew = 0.0001; ID = 0.0004; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 0; ClockBufArea = 0.0000; ClockCellArea = 0.0000; ClockWireLen = 36.5710; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)
Area recovery and subtree balancing cpu time 00:00:00.09u 00:00:00.03s 00:00:01.12e:
The elapsed time for optimization of clock tree is 0 hr : 0 min : 1.15 sec, cpu time is 0 hr : 0 min : 0.13 sec.
Information: The run time for Area recovery is 0 hr : 0 min : 1.22 sec, cpu time is 0 hr : 0 min : 0.13 sec. (CTS-104)
[cto] Finished AR.1: PASS

*****+
* CTS STEP: Final DRC fixing
*****+

[cto] Starting PostDrc.1
-----
Optimizing clock tree DRC
clock: clk mode: func root: clk
Clock QoR Before DRC Optimization:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Pre Final DRC Fixing: GlobalSkew = 0.0001; ID = 0.0004; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 0; ClockBufArea = 0.0000; ClockCellArea = 0.0000; ClockWireLen = 36.5710; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)

Begin Post-Opt Drc Fixing
Starting multithread based drc fixing Post opt drc fixing

Optimization Summary
-----

# Drivers Attempted      =      0
# Skipped during isValid and estimate      =      0
# Failed subgraph evaluation      =      0
# Failed main graph committ      =      0
# Successful main graph commit      =      0
# NumCTCells changed      =      0

# Accepted buffering moves =      2

# Total CPU time      = 00h:00m:00s
# Total elapsed time      = 00h:00m:03s
# Flow total speed up      =     0.0613
# Commit CPU time      = 00h:00m:00s
# Commit elapsed time      = 00h:00m:01s
# Commit speed up      =     0.0451
# Generator CPU time      = 00h:00m:00s
# Generator elapsed time      = 00h:00m:00s
# Generator speed up      =     0.0811
# Sg CPU time      = 00h:00m:00s
# Sg elapsed time      = 00h:00m:00s
# Sg speed up      =     0.1203
# The rest of flow speed up      =     0.0892

-----
Post-Opt drc fixing cpu time 00:00:00.12u 00:00:00.09s 00:00:03.35e:
Clock QoR After Post-Opt Drc Fixing:
Clock: clk, Mode: func, Root: clk
Information: CTS QoR Post Final DRC Fixing: GlobalSkew = 0.0001; ID = 0.0004; NetsWithDRC = 1; Worst Tran/Cap cost = 0.0500/0.0000; ClockBufCount = 0; ClockBufArea = 0.0000; ClockCellArea = 0.0000; ClockWireLen = 36.5710; Clock = clk; Mode = func; Corner = nom; ClockRoot = clk. (CTS-037)
The elapsed time for optimization of clock tree is 0 hr : 0 min : 3.38 sec, cpu time is 0 hr : 0 min : 0.21 sec.
Information: The run time for Final DRC fixing is 0 hr : 0 min : 3.38 sec, cpu time is 0 hr : 0 min : 0.21 sec. (CTS-104)
[cto] Finished PostDrc.1: PASS
[rap] Thread-server 0: shutdown
Mgr Thread-server 0: Dtor

No. startProblems      =      8

No. doRoutes      =      75
No. doUnroutes      =      39
No. redoRoutes      =      2
No. redoUnroutes      =      1
No. undoRoutes      =      75
No. undoUnroutes      =      39
No. commitRoutes      =      3
No. commitUnroutes      =      3
No. uncommitRoutes      =      0
No. doRoute fails      =      0
No. doUnroute fails      =      0

No. viaLadderQueries      =      0
No. doDelVias      =      0
No. doAddVias      =      0
No. redoDelVias      =      0
No. redoAddVias      =      0
No. undoDelVias      =      0
No. undoAddVias      =      0
No. commitChangeVias      =      0
No. uncommitChangeVias      =      0
No. doDelVias fails      =      0
No. doAddVias fails      =      0

```

```

no. 00A0001as fails = 0
Updating congestion ...
Updating congestion ...
GR Routing Service: Wrote GR congmap to NDM
Information: The netlist change observers are enabled for incremental timing updates. (TIM-120)
Information: The netlist change observers are enabled for incremental extraction. (TIM-127)
Information: The net parasitics of block CLA1 are cleared. (TIM-123)
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = MRDL
Turn off antenna since no rule is specified
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer C0. (ZRT-022)
Warning: Port VDD of cell eight_bit_adder.v
    is unplaced. This may impact routing result. (ZRT-740)
Warning: Port VSS of cell eight_bit_adder.v
    is unplaced. This may impact routing result. (ZRT-740)
Warning: Ignore 2 top cell ports with no pins. (ZRT-027)
Info: number of net_type.blockage: 0
Information: Via ladder engine would be activated for pattern must join connection in certain commands. Please refer to man-page for the command list. (ZRT-619)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)
Start Global Route ...
[Init] Elapsed real time: 0:00:00
[Init] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Init] Stage (MB): Used 0 Alloctr 0 Proc 0
[Init] Total (MB): Used 26 Alloctr 27 Proc 4696
Printing options for 'route.common.*'
common.verbose_level : 0

Printing options for 'route.global.*'
global.crosstalk_driven : false
global.timing_driven : false

Begin global routing.
Loading parasitics information to the router ...
parastics information loaded to the router.
[End of Loading Timing] Elapsed real time: 0:00:00
[End of Loading Timing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
Constructing data structure ...
Design statistics:
Design Bounding Box (0.00um,0.00um,23.43um,22.06um)
Number of routing layers = 10
layer M1, dir Hor, min width = 0.05um, min space = 0.05um pitch = 0.152um
layer M2, dir Ver, min width = 0.056um, min space = 0.056um pitch = 0.152um
layer M3, dir Hor, min width = 0.056um, min space = 0.056um pitch = 0.304um
layer M4, dir Ver, min width = 0.056um, min space = 0.056um pitch = 0.304um
layer M5, dir Hor, min width = 0.056um, min space = 0.056um pitch = 0.608um
layer M6, dir Ver, min width = 0.056um, min space = 0.056um pitch = 0.608um
layer M7, dir Hor, min width = 0.056um, min space = 0.056um pitch = 1.216um
layer M8, dir Ver, min width = 0.056um, min space = 0.056um pitch = 1.216um
layer M9, dir Hor, min width = 0.16um, min space = 0.16um pitch = 2.432um
layer MRDL, dir Ver, min width = 2um, min space = 2um pitch = 4.864um
Current Stage stats:
[End of Build Tech Data] Elapsed real time: 0:00:00
[End of Build Tech Data] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Tech Data] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Build Tech Data] Total (MB): Used 30 Alloctr 31 Proc 4696
Net statistics:
Total number of nets = 132
Number of nets to route = 1
3 nets are fully connected,
of which 2 are detail routed and 1 are global routed.
Net length statistics:
Net Count(Ignore Fully Rted) 0. Total Half Perimeter Wire Length (HPWL) 0 microns
HPWL 0 ~ 50 microns: Net Count 0 Total HPWL 0 microns
HPWL 50 ~ 100 microns: Net Count 0 Total HPWL 0 microns
HPWL 100 ~ 200 microns: Net Count 0 Total HPWL 0 microns
HPWL 200 ~ 300 microns: Net Count 0 Total HPWL 0 microns
HPWL 300 ~ 400 microns: Net Count 0 Total HPWL 0 microns
HPWL 400 ~ 500 microns: Net Count 0 Total HPWL 0 microns
HPWL 500 ~ 600 microns: Net Count 0 Total HPWL 0 microns
HPWL 600 ~ 700 microns: Net Count 0 Total HPWL 0 microns
HPWL 700 ~ 800 microns: Net Count 0 Total HPWL 0 microns
HPWL 800 ~ 900 microns: Net Count 0 Total HPWL 0 microns
HPWL 900 ~ 1000 microns: Net Count 0 Total HPWL 0 microns
HPWL > 1000 microns: Net Count 0 Total HPWL 0 microns
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build All Nets] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Build All Nets] Total (MB): Used 31 Alloctr 31 Proc 4696
Number of partitions: 1 (1 x 1)
Size of partitions: 14 gCells x 14 gCells
Average gCell capacity 3.15 on layer (1) M1
Average gCell capacity 0.70 on layer (2) M2

```

```

Average gCell capacity 3.76 on layer (2) M2
Average gCell capacity 4.62 on layer (3) M3
Average gCell capacity 4.83 on layer (4) M4
Average gCell capacity 2.41 on layer (5) M5
Average gCell capacity 2.02 on layer (6) M6
Average gCell capacity 0.71 on layer (7) M7
Average gCell capacity 0.85 on layer (8) M8
Average gCell capacity 0.57 on layer (9) M9
Average gCell capacity 0.21 on layer (10) MRDL
Average number of tracks per gCell 10.43 on layer (1) M1
Average number of tracks per gCell 11.07 on layer (2) M2
Average number of tracks per gCell 5.29 on layer (3) M3
Average number of tracks per gCell 5.64 on layer (4) M4
Average number of tracks per gCell 2.71 on layer (5) M5
Average number of tracks per gCell 2.86 on layer (6) M6
Average number of tracks per gCell 1.43 on layer (7) M7
Average number of tracks per gCell 1.50 on layer (8) M8
Average number of tracks per gCell 0.79 on layer (9) M9
Average number of tracks per gCell 0.36 on layer (10) MRDL
Number of gCells = 1960
Current Stage stats:
[End of Build Congestion Map] Elapsed real time: 0:00:00
[End of Build Congestion Map] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Congestion Map] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Build Congestion Map] Total (MB): Used 31 Alloctr 31 Proc 4696
Current Stage stats:
[End of Add Nets Demand] Elapsed real time: 0:00:00
[End of Add Nets Demand] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Add Nets Demand] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Add Nets Demand] Total (MB): Used 31 Alloctr 31 Proc 4696
Current Stage stats:
[End of Add Nets Demand] Elapsed real time: 0:00:00
[End of Add Nets Demand] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Add Nets Demand] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Add Nets Demand] Total (MB): Used 31 Alloctr 31 Proc 4696
Number of user frozen nets = 0
Information: RC layer preference is turned on for this design. (ZRT-613)
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used 1 Alloctr 1 Proc 0
[End of Build Data] Total (MB): Used 31 Alloctr 31 Proc 4696
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Blocked Pin Detection] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Blocked Pin Detection] Total (MB): Used 31 Alloctr 31 Proc 4696
Information: Using 1 threads for routing. (ZRT-444)
Information: Multiple gcell levels ON
Information: Buffer distance is estimated to be -862.0000um (515 gCells)

Start GR phase 0
Number of partitions: 1 (1 x 1)
Size of partitions: 14 gCells x 14 gCells
[rtAllBotParts] Elapsed real time: 0:00:00
[rtAllBotParts] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[rtTop] Elapsed real time: 0:00:00
[rtTop] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Initial Routing] Stage (MB): Used 68 Alloctr 68 Proc 0
[End of Initial Routing] Total (MB): Used 99 Alloctr 99 Proc 4696
Number of user frozen nets = 0
Information: RC layer preference is turned on for this design. (ZRT-613)
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used 1 Alloctr 1 Proc 0
[End of Build Data] Total (MB): Used 31 Alloctr 31 Proc 4696
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Blocked Pin Detection] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of Blocked Pin Detection] Total (MB): Used 31 Alloctr 31 Proc 4696
Information: Using 1 threads for routing. (ZRT-444)
Information: Multiple gcell levels ON
Information: Buffer distance is estimated to be -862.0000um (515 gCells)

Start GR phase 0
Number of partitions: 1 (1 x 1)
Size of partitions: 14 gCells x 14 gCells
[rtAllBotParts] Elapsed real time: 0:00:00
[rtAllBotParts] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[rtTop] Elapsed real time: 0:00:00
[rtTop] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Initial Routing] Stage (MB): Used 68 Alloctr 68 Proc 0
[End of Initial Routing] Total (MB): Used 99 Alloctr 99 Proc 4696
Initial Routing result:
Initial. Both Dirs: Dmd-Cap = 0 Max = 0 GRCs = 0 (0.00%)
Initial. H routing: Dmd-Cap = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. V routing: Dmd-Cap = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. Both Dirs: Overflow = 0 Max = 0 GRCs = 0 (0.00%)
Initial. H routing: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)

```

```

Initial. V routing: Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M1 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M2 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M3 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M4 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M5 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M6 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M7 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M8 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. M9 Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)
Initial. MRDL Overflow = 0 Max = 0 (GRCs = 0) GRCs = 0 (0.00%)

Initial. Total Wire Length = 35.59
Initial. Layer M1 wire length = 0.00
Initial. Layer M2 wire length = 17.00
Initial. Layer M3 wire length = 18.59
Initial. Layer M4 wire length = 0.00
Initial. Layer M5 wire length = 0.00
Initial. Layer M6 wire length = 0.00
Initial. Layer M7 wire length = 0.00
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 13

Initial. Via VIA12SQ_C count = 9
Initial. Via VIA23SQ_C count = 2
Initial. Via VIA34SQ_C count = 1
Initial. Via VIA45SQ_C count = 1
Initial. Via VIA56SQ_C count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.

[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used 69 Alloctr 69 Proc 0
[End of Whole Chip Routing] Total (MB): Used 99 Alloctr 99 Proc 4696

Congestion utilization per direction:
Average vertical track utilization = 0.67 %
Peak vertical track utilization = 13.33 %
Average horizontal track utilization = 0.53 %
Peak horizontal track utilization = 11.11 %

[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Global Routing] Stage (MB): Used 68 Alloctr 68 Proc 0
[End of Global Routing] Total (MB): Used 99 Alloctr 99 Proc 4696
Updating congestion ...
Updating congestion ...
[End of dbOut] Elapsed real time: 0:00:00
[End of dbOut] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of dbOut] Stage (MB): Used 0 Alloctr 0 Proc 0
[End of dbOut] Total (MB): Used 58 Alloctr 59 Proc 4696
Skip track assign
Skip detail route
Updating the database ...
There are 0 buffers added and 0 inverters added by Clock Tree Optimization.
*****
* CTS STEP: Postlode
*****
Mark clock trees...
Marking clock synthesized attributes

Marking spacing rules

Clock cell spacing rule list:
No clock cell spacing rule is found.
Info: 9 sinks and boundary insts are set as application_fixed
nplDlc2Placer::setParam(effort,1)
nplDlc2Placer::setParam(debug,0)
nplDlc2Placer::setParam(site_check,2)
nplDlc2Placer::setParam(app_firm_wgt,0)
Warning: Routing direction of metal layer P0 is neither "horizontal" nor "vertical". PDC checks will not be performed on this layer. (PDC-003)
PDC app_options settings =====
place.legalize.enable_prerouted_net_check: 1
place.legalize.num_tracks_for_access_check: 1
place.legalize.use_eol_spacing_for_access_check: 0
place.legalize.allow_touch_track_for_access_check: 1

```

```

place.legalize.reduce_conservatism_in_eol_check: 0
place.legalize.preroute_shape_merge_distance: 0.0
place.legalize.enable_non_preferred_direction_span_check: 0

Layer M1: cached 0 shapes out of 16 total shapes.
Layer M2: cached 91 shapes out of 99 total shapes.
Cached 182 vias out of 724 total vias.

Legalizing Top Level Design CLA1 ...
Information: Initializing classic cellmap without advanced rules enabled and without PDC enabled
Information: The following app options are used in cellmap
    place.legalize.enable_color_aware_placement : false
    place.legalize.use_nll_query_cm : false
    place.legalize.enable_advanced_legalizer : false
    place.legalize.enable_prerouted_net_check : true
    place.legalize.enable_advanced_prerouted_net_check : false
    place.legalize.always_continue : true
    place.legalize.limit_legality_checks : false
    place.common.pnet_aware_density : 1.0000
    place.common.pnet_aware_min_width : 0.0000
    place.common.pnet_aware_layers : {}
    place.common.use_placement_model : false
    place.common.enable_advanced_placement_model : true
    cts.placement.cell_spacing_rule_style : maximum
Total 0.0200 seconds to build cellmap data
Information: Creating classic rule checker.
Warning: Routing direction of metal layer P0 is neither "horizontal" nor "vertical". PDC checks will not be performed on this layer. (PDC-003)
=====> Processed 15 ref cells (8 fillers) from library

Bounds/Regions In This Design:
  Area   Num Cells  Exclusive Name
  (square um)
  430.012      112      Yes DEFAULT_VA

Starting legalizer.
Warning: Exclusive bound 'DEFAULT' has no cells.
Optimizing Exclusive Bound 'DEFAULT_VA' (2/2)
  Done Exclusive Bound 'DEFAULT_VA' (2/2) (0 sec)

Legalization complete (0 total sec)

*****
Report : Placement Attempts
Site  : unit
*****
number of cells:          112
number of references:     15
number of site rows:      12
number of locations attempted: 1345
number of locations failed: 0  (0.0%)
Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

*****
Report : Cell Displacements
*****
number of cells aggregated:      103 (755 total sites)
avg row height over cells:      1.672 um
rms cell displacement:          0.000 um ( 0.00 row height)
rms weighted cell displacement: 0.000 um ( 0.00 row height)
max cell displacement:          0.000 um ( 0.00 row height)
avg cell displacement:          0.000 um ( 0.00 row height)
avg weighted cell displacement: 0.000 um ( 0.00 row height)
number of cells moved:          0
number of large displacements:   0
large displacement threshold:    3.000 row height

Displacements of worst 10 cells:
Cell: U45 (AND2X1_RVT)
  Input location: (5.56,11.032)
  Legal location: (5.56,11.032)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U42 (AND2X1_RVT)
  Input location: (6.776,7.688)
  Legal location: (6.776,7.688)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U40 (AND2X1_RVT)
  Input location: (1.912,16.048)
  Legal location: (1.912,16.048)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U35 (AND2X1_RVT)
  Input location: (2.216,6.016)
  Legal location: (2.216,6.016)
  Displacement:  0.000 um ( 0.00 row height)
Cell: U4 (AND2X1_RVT)
  Input location: (6.168,16.048)
  Legal location: (6.168,16.048)

```

```

Displacement: 0.000 um ( 0.00 row height)
Cell: U33 (AND2X1_RVT)
  Input location: (1.152,11.032)
  Legal location: (1.152,11.032)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U30 (AND2X1_RVT)
  Input location: (2.368,14.376)
  Legal location: (2.368,14.376)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U26 (AND2X1_RVT)
  Input location: (4.04,11.032)
  Legal location: (4.04,11.032)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U24 (AND2X1_RVT)
  Input location: (6.776,9.36)
  Legal location: (6.776,9.36)
  Displacement: 0.000 um ( 0.00 row height)
Cell: U50 (AND2X1_RVT)
  Input location: (14.984,9.36)
  Legal location: (14.984,9.36)
  Displacement: 0.000 um ( 0.00 row height)

Info: 9 sinks and boundary insts are unset from application_fixed
Successfully legalize placement.
Information: The run time for postlude is 0 hr : 0 min : 2.88 sec, cpu time is 0 hr : 0 min : 0.24 sec. (CTS-104)
***** CTS STEP: Summary report *****
There are 1 flat clock tree nets.
There are 0 non-sink instances (total area 0.00) on clock trees including 0 instances dont_touch.
Clock tree synthesize and optimization added 0 buffers and 0 inverters (total area 0.00).
Information: The stitching and editing of coupling caps is turned OFF for design 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'. (TIM-125)
Information: The run time for postlude is 0 hr : 0 min : 2.88 sec, cpu time is 0 hr : 0 min : 0.24 sec. (CTS-104)
***** CTS STEP: Summary report *****
There are 1 flat clock tree nets.
There are 0 non-sink instances (total area 0.00) on clock trees including 0 instances dont_touch.
Clock tree synthesize and optimization added 0 buffers and 0 inverters (total area 0.00).
Information: The stitching and editing of coupling caps is turned OFF for design 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'. (TIM-125)
Information: Design eight_bit_adder.v has 132 nets, 1 global routed, 0 detail routed. (NEX-024)
Information: The RC mode used is CTO for design 'CLAI'. (NEX-022)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 130, routed nets = 1, across physical hierarchy nets = 0, parasitics cached nets = 1, delay annotated nets = 0, parasitics annotated nets = 0, multi-voltage nets = 0. (TIM-112)
Compilation of clock trees finished successfully
Run time for cts 00:00:04.44u 00:00:01.63s 00:00:44.03e:

Summary of messages during CTS:
=====
Tag   Count  Type          Description
-----
CTS-038  1  Warning  No clock routing rule is specified.
Information: Ending 'synthesize_clock_trees' (FLW-8001)
Information: Time: 2024-07-11 04:42:00 / Session: 03:54:25 / Command: 00:00:45 / CPU: 00:00:04 / Memory: 1337 MB (FLW-8100)
1

```

Enabling the optimization of local clock skew

```

icc2_shell> set_placement_layer_usage -layers {M1 M2 M3 M4 M5 M6}
Error: unknown command 'set_placement_layer_usage' (CMD-005)
icc2_shell> set_app_options -name cts.optimize.enable_local_skew -value true
cts.optimize.enable_local_skew true
icc2_shell> set_app_options -name cts.compile.enable_local_skew -value true
cts.compile.enable_local_skew true
icc2_shell> set_app_options -name cts.compile.enable_global_route -value false
cts.compile.enable_global_route false
icc2_shell> set_app_options -name clock_opt.flow.enable_ccd -value true
clock_opt.flow.enable_ccd true

```

‘clock_opt’ – It aims at optimization of the clock w.r.t power, area, timing.

```
*****
* CTS STEP: Summary report
*****
There are 2 flat clock tree nets.
There are 1 non-sink instances (total area 3.81) on clock trees including 0 instances dont_touch.
Clock tree synthesize and optimization added 1 buffers and 0 inverters (total area 3.81).
Compilation of clock trees finished successfully
Run time for cts 00:00:03.13u 00:00:00.94s 00:00:30.28e:
[Tim-Power] Info: Cleared Leakage libCell cache.

Summary of messages during CTS:
=====
Tag Count Type Description
-----
CTS-038 1 Warning No clock routing rule is specified.
Info: restoring CTS-GR option to: 0
Info: clearin CTO-GR option
Information: The stitching and editing of coupling caps is turned OFF for design 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder.v.design'. (TIM-125)
Information: Design eight_bit_adder.v has 133 nets, 2 global routed, 0 detail routed. (NEX-024)
Number of Site types in the design = 1
Setting up Chip Core
Chip Core shape: (10000 10000) (224320 210640)
Number of VARs = 1
Number of unique PDs = 1
Number of Power Domains = 1
Number of Voltage Areas = 1
Number of supply Nets = 2
Number of used supplies = 0
Clock-opt final QoR

Scenario Mapping Table
1: func::nom

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2req_default**
5: **reg2out_default**
6: **in2out_default**
7: clk

-----
PATHGROUP QoR

-----
Scene PG WNS TNS NSV WHV THV NHV
1 1 0.0000 0.0000 0 0.0000 0.0000 0
1 2 0.0000 0.0000 0 0.0000 0.0000 0
1 3 0.0000 0.0000 0 0.0000 0.0000 0
1 4 0.0000 0.0000 0 0.0000 0.0000 0
1 5 0.0000 0.0000 0 0.0000 0.0000 0
1 6 0.0000 0.0000 0 0.0000 0.0000 0
1 7 0.0000 0.0000 0 0.0000 0.0000 0

-----
SCENARIO QoR

-----
Scene PG WNS TNS R2RTNS NSV WHV THV NHV MaxTrnV MaxTranC MaxCapV Leakage
1 * 0.0000 0.0000 0.0000 0 0.0000 0.0000 0 0.0000 0 0 556546240

-----
DESIGN QoR

-----
Scene PG WNS TNS R2RTNS NSV WHV THV NHV MaxTrnV MaxTranC MaxCapV Leakage Area InstCnt BufCnt
InvCnt * * 0.0000 0.0000 0.0000 0 0.0000 0.0000 0 0.0000 0 556546240 255.16 113 1
27

-----
Clock-opt final QoR Summary WNS TNS R2RTNS NSV WHV THV NHV MaxTrnV MaxCapV Leakage Area InstCnt
Clock-opt final QoR Summary 0.0000 0.0000 0.0000 0 0.0000 0.0000 0 0 0 556546240 255.16 113

Clock-opt command complete CPU: 380 s ( 0.11 hr ) ELAPSE: 17015 s ( 4.73 hr ) MEM-PEAK: 1441 MB
Clock-opt command statistics CPU=7 sec (0.00 hr) ELAPSED=56 sec (0.02 hr) MEM-PEAK=1.407 GB
[Tim-Power] Info: Cleared Leakage libCell cache.

Information: Ending _clock_opt / build_clock (FLW-8001)
Information: Time: 2024-07-11 05:31:11 / Session: 04:43:36 / Command: 00:01:24 / CPU: 00:00:11 / Memory: 1442 MB (FLW-8100)
TEST: runCore bidCLKEnd-end
TEST: runCore final-init
TEST: runCore final-end
[Tim-Power] Info: Cleared Leakage libCell cache.
Information: Running auto PG connection. (NDM-099)
Information: Ending '_clock_opt -to build_clock' (FLW-8001)
Information: Time: 2024-07-11 05:31:11 / Session: 04:43:36 / Command: 00:01:25 / CPU: 00:00:11 / Memory: 1442 MB (FLW-8100)
1
icc2 shell> 
```

‘report_design’ – It generates the report of the design after cts stage.

```
*****
Report : design
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 06:03:01 2024
*****



Total number of std cells in library : 286
Total number of dont_use lib cells : 85
Total number of dont_touch lib cells : 7
Total number of buffers : 11
Total number of inverters : 15
Total number of flip-flops : 106
Total number of latches : 12
Total number of ICGs : 12

Cell Instance Type Count Area
-----
TOTAL LEAF CELLS 113 256.431
unit 113 256.431
Standard cells 113 256.431
unit 113 256.431
Hard macro cells 0 0.000
unit 113 256.431
Soft macro cells 0 0.000
unit 113 256.431
Always on cells 0 0.000
unit 113 256.431
Physical only 0 0.000
unit 113 256.431
Fixed cells 0 0.000
unit 113 256.431
Moveable cells 113 256.431
unit 113 256.431
Placed cells 112 251.348
unit 113 256.431
Sequential 9 59.470
unit 113 256.431
Buffer/inverter 28 39.392
unit 113 256.431
ICG cells 0 0.000
unit 113 256.431

Logic Hierarchies : 0
Design Masters count : 8
Total Flat nets count : 133
Total FloatingNets count : 0
Total no of Ports : 38
Number of Master Clocks in design : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design : 7 (1 of them Non Default)
Number of Scan Chains in design : 0
List of Modes : func
List of Corners : nom
List of Scenarios : func::nom

Core Area : 430.012
Chip Area : 517.004
Total Site Row Area : 430.012
Number of Blockages : 1
Total area of Blockages : 42.994
Number of Power Domains : 1
Number of Voltage Areas : 1
Number of Group Bounds : 0
Number of Exclusive MoveBounds : 0
Number of Hard or Soft MoveBounds : 0
Number of Multibit Registers : 0
Number of Multibit LS/ISO Cells : 0
Number of Top Level RP Groups : 0
Number of Tech Layers : 71 (61 of them have unknown routing dir.)

Total wire length : 29.42 micron
Total number of wires : 18
Total number of contacts : 1194
```

‘report_timing’ – It generates the report of slack, timing paths, delays after cts stage.

```

report timing
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -report_by design
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 06:05:55 2024
*****



Startpoint: a[0] (input port clocked by clk)
Endpoint: sum[7] (output port clocked by clk)
Mode: func
Corner: nom
Scenario: func::nom
Path Group: **in2out_default**
Path Type: max

Point           Incr   Path
-----
clock clk (rise edge)      0.00  0.00
clock network delay (propagated) 0.04  0.04
input external delay        0.60  0.64 f
a[0] (in)                  0.00  0.64 f
U3/Y (INVX0_RVT)           0.03  0.67 r
U5/Y (OR2X1_RVT)            0.04  0.71 r
U35/Y (AND2X1_RVT)          0.03  0.74 r
U37/Y (OR2X1_RVT)           0.03  0.78 r
U38/Y (INVX0_RVT)           0.02  0.79 f
U39/Y (OR2X1_RVT)           0.03  0.82 f
U4/Y (AND2X1_RVT)            0.04  0.86 f
ctmTdsLR_1_5/Y (OR3X1_RVT)  0.03  0.89 f
ctmTdsLR_1_7/Y (AND3X1_RVT) 0.04  0.93 f
ctmTdsLR_1_8/Y (AND3X1_RVT) 0.05  0.98 f
ctmTdsLR_1_10/Y (OR3X1_RVT) 0.03  1.01 f
ctmTdsLR_1_1/Y (AND3X1_RVT) 0.04  1.05 f
U101/Y (INVX0_RVT)           0.01  1.07 r
U102/Y (AND2X1_RVT)          0.03  1.10 r
sum[7] (out)                 0.00  1.10 r
data arrival time           1.10

clock clk (rise edge)      1.00  1.00
clock network delay (propagated) 0.04  1.04
clock uncertainty           1.20  2.24
output external delay       -0.40  1.84
data required time          1.84

data required time          1.84
data arrival time           -1.10
-----
slack (MET)                0.74

```

1

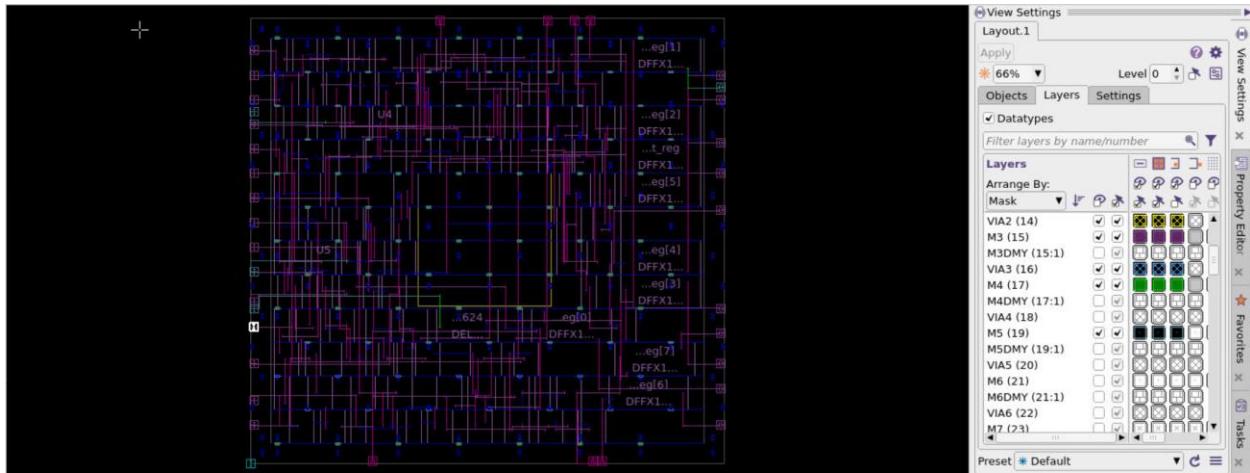
Commands for CTS

```

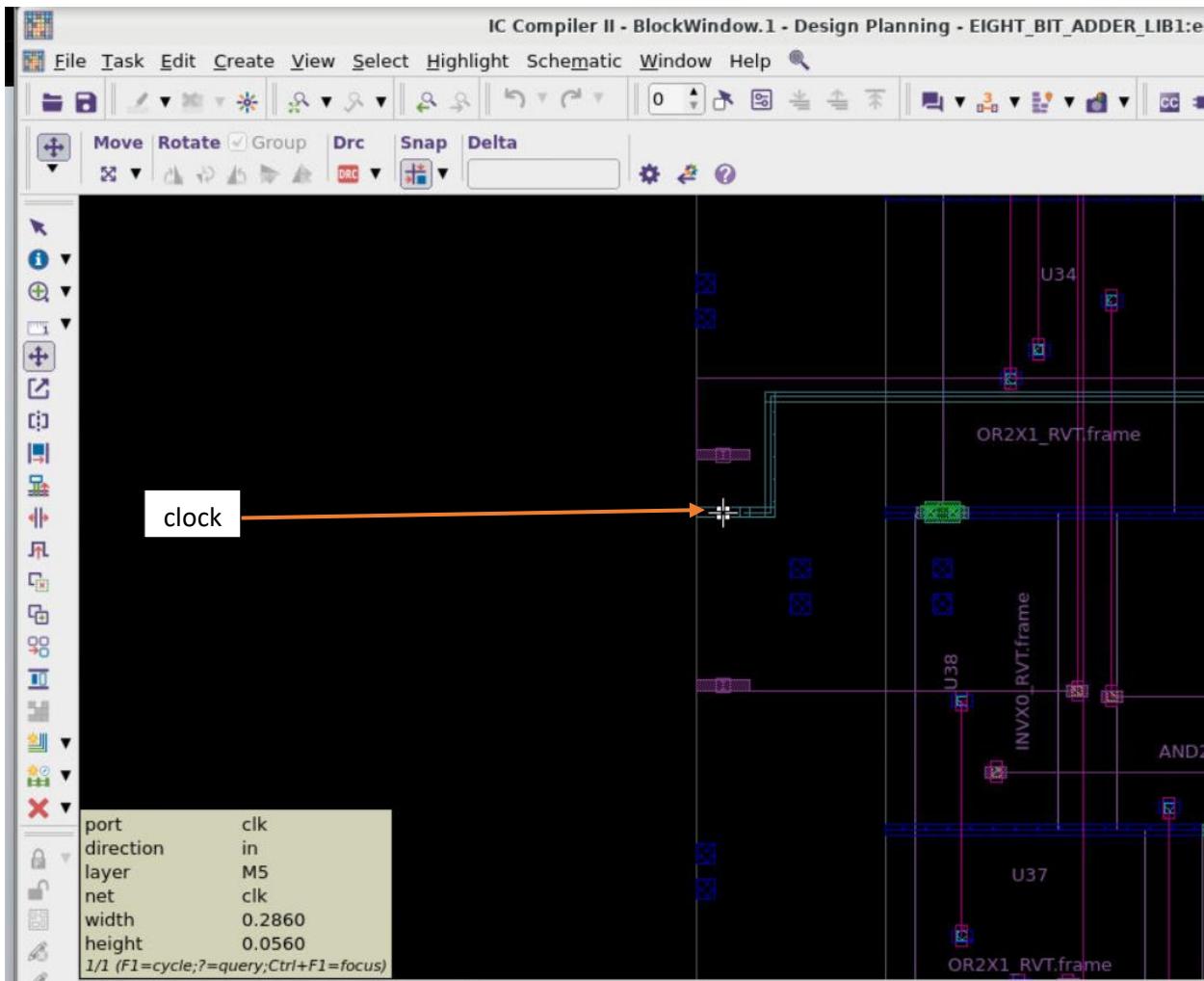
100 check_design -checks pre_clock_tree_stage
101 synthesize_clock_tree
102 set_app_options -name cts.optimize.enable_local_skew -value true
103 set_app_options -name cts.compile.enable_local_skew -value true
104 set_app_options -name cts.compile.enable_global_route -value false
105 set_app_options -name clock_opt.flow.enable_ccd -value true
106 clock_opt -to build_clock
107 clock_opt -from route_clock -to route_clock
108 clock_opt
109 report_design
110 report_timing
111 history

```

Output of CTS Stage



Clock pin is highlighted here



7.Routing

- **Objective:** Connect all components and logic blocks of the IC with physical wires that have resistive (R) and capacitive (C) properties.
- **Global Routing:** Plan the general paths for interconnections, considering overall layout and congestion.
- **Detailed Routing:** Precisely connect individual wires to their specific pins, ensuring accurate placement.

Set all the various conditions needed for routing.

```
icc2_shell> set_app_options -name route.global.timing_driven -value true
route.global.timing_driven true
icc2_shell> set_app_options -name route.global.crosstalk_driven -value false
route.global.crosstalk_driven false
icc2_shell>
icc2_shell> set_app_options -name route.track.timing_driven -value true
route.track.timing_driven true
icc2_shell> set_app_options -name route.track.crosstalk_driven -value true
route.track.crosstalk_driven true
icc2_shell> set_app_options -name route.detail.timing_driven -value true
route.detail.timing_driven true
icc2_shell> set_app_options -name route.detail.save_after_iterations -value false
Error: Invalid value 'false' specified for option 'route.detail.save_after_iterations'
      Use error_info for more info. (CMD-013)
icc2_shell> set_app_options -name route.detail.force_max_number_iterations -value false
route.detail.force_max_number_iterations false
icc2_shell> set_app_options -name route.detail.antenna -value true
route.detail.antenna true
icc2_shell> set_app_options -name route.detail.antenna_fixing_preference -value use_diodes
route.detail.antenna_fixing_preference use_diodes
icc2_shell> set_app_options -name route.detail.diode_libcell_names -value */ANTENNA_RVT
route.detail.diode_libcell_names */ANTENNA_RVT
```

‘route_opt’ – It includes route_global, route_track and route_detail. It includes Global routing , track assignment for routing and detailed routing.

```
*****
Report : Cell Displacements
*****  
  
number of cells aggregated: 112 (989 total sites)  
avg row height over cells: 1.672 um  
rms cell displacement: 0.000 um ( 0.00 row height)  
rms weighted cell displacement: 0.000 um ( 0.00 row height)  
max cell displacement: 0.000 um ( 0.00 row height)  
avg cell displacement: 0.000 um ( 0.00 row height)  
avg weighted cell displacement: 0.000 um ( 0.00 row height)  
number of cells moved: 0  
number of large displacements: 0  
large displacement threshold: 3.000 row height  
  
Displacements of worst 10 cells:  
Cell: U45 (AND2X1_RVT)  
    Input location: (5.712,11.032)  
    Legal location: (5.712,11.032)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U42 (AND2X1_RVT)  
    Input location: (6.472,7.688)  
    Legal location: (6.472,7.688)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U40 (AND2X1_RVT)  
    Input location: (1.608,16.048)  
    Legal location: (1.608,16.048)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U35 (AND2X1_RVT)  
    Input location: (2.216,6.016)  
    Legal location: (2.216,6.016)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U4 (AND2X1_RVT)  
    Input location: (6.016,16.048)  
    Legal location: (6.016,16.048)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U33 (AND2X1_RVT)  
    Input location: (1.152,11.032)  
    Legal location: (1.152,11.032)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U30 (AND2X1_RVT)  
    Input location: (2.368,14.376)  
    Legal location: (2.368,14.376)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U26 (AND2X1_RVT)  
    Input location: (4.344,11.032)  
    Legal location: (4.344,11.032)  
    Displacement: 0.000 um ( 0.00 row height)  
Cell: U24 (AND2X1_RVT)  
    Input location: (6.928,9.36)
```

```

Net Count(Ignore Fully Rted) 1, Total Half Perimeter Wire Length (HPWL) 5 microns
HPWL 0 ~ 50 microns: Net Count 1 Total HPWL 5 microns
HPWL 50 ~ 100 microns: Net Count 0 Total HPWL 0 microns
HPWL 100 ~ 200 microns: Net Count 0 Total HPWL 0 microns
HPWL 200 ~ 300 microns: Net Count 0 Total HPWL 0 microns
HPWL 300 ~ 400 microns: Net Count 0 Total HPWL 0 microns
HPWL 400 ~ 500 microns: Net Count 0 Total HPWL 0 microns
HPWL 500 ~ 600 microns: Net Count 0 Total HPWL 0 microns
HPWL 600 ~ 700 microns: Net Count 0 Total HPWL 0 microns
HPWL 700 ~ 800 microns: Net Count 0 Total HPWL 0 microns
HPWL 800 ~ 900 microns: Net Count 0 Total HPWL 0 microns
HPWL 900 ~ 1000 microns: Net Count 0 Total HPWL 0 microns
HPWL > 1000 microns: Net Count 0 Total HPWL 0 microns
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build All Nets] Stage (MB): Used 0 AllocTr 0 Proc 0
[End of Build All Nets] Total (MB): Used 31 AllocTr 31 Proc 4803
Number of partitions: 1 (1 x 1)
Size of partitions: 14 gCells x 14 gCells
Average gCell capacity 3.23 on layer (1) M1
Average gCell capacity 9.70 on layer (2) M2
Average gCell capacity 4.62 on layer (3) M3
Average gCell capacity 4.83 on layer (4) M4
Average gCell capacity 2.41 on layer (5) M5
Average gCell capacity 2.02 on layer (6) M6
Average gCell capacity 0.71 on layer (7) M7
Average gCell capacity 0.85 on layer (8) M8
Average gCell capacity 0.57 on layer (9) M9
Average gCell capacity 0.21 on layer (10) MRDL
Average number of tracks per gCell 10.43 on layer (1) M1
Average number of tracks per gCell 11.07 on layer (2) M2
Average number of tracks per gCell 5.29 on layer (3) M3
Average number of tracks per gCell 5.64 on layer (4) M4
Average number of tracks per gCell 2.71 on layer (5) M5
Average number of tracks per gCell 2.86 on layer (6) M6
Average number of tracks per gCell 1.43 on layer (7) M7
Average number of tracks per gCell 1.50 on layer (8) M8
Average number of tracks per gCell 0.79 on layer (9) M9
Average number of tracks per gCell 0.36 on layer (10) MRDL
Number of gCells = 1960

```

```
Initial. Total Wire Length = 656.59
Initial. Layer M1 wire length = 26.53
Initial. Layer M2 wire length = 352.13
Initial. Layer M3 wire length = 264.54
Initial. Layer M4 wire length = 2.46
Initial. Layer M5 wire length = 10.93
Initial. Layer M6 wire length = 0.00
Initial. Layer M7 wire length = 0.00
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 468
Initial. Via VIA12SQ_C count = 276
Initial. Via VIA23SQ_C count = 184
Initial. Via VIA34SQ_C count = 4
Initial. Via VIA45SQ_C count = 4
Initial. Via VIA56SQ_C count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
```

```
phasel. Total Wire Length = 656.59
phasel. Layer M1 wire length = 26.53
phasel. Layer M2 wire length = 352.13
phasel. Layer M3 wire length = 264.54
phasel. Layer M4 wire length = 2.46
phasel. Layer M5 wire length = 10.93
phasel. Layer M6 wire length = 0.00
phasel. Layer M7 wire length = 0.00
phasel. Layer M8 wire length = 0.00
phasel. Layer M9 wire length = 0.00
phasel. Layer MRDL wire length = 0.00
phasel. Total Number of Contacts = 468
phasel. Via VIA12SQ_C count = 276
phasel. Via VIA23SQ_C count = 184
phasel. Via VIA34SQ_C count = 4
phasel. Via VIA45SQ_C count = 4
phasel. Via VIA56SQ_C count = 0
phasel. Via VIA67SQ_C count = 0
phasel. Via VIA78SQ_C count = 0
phasel. Via VIA89_C count = 0
phasel. Via VIA9RDL count = 0
phasel. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used 177 AllocTr 177 Proc 0
[End of Whole Chip Routing] Total (MB): Used 207 AllocTr 207 Proc 4803
```

```
Congestion utilization per direction:
Average vertical track utilization = 12.40 %
Peak vertical track utilization = 42.86 %
Average horizontal track utilization = 11.22 %
Peak horizontal track utilization = 50.00 %
```

```
Start initial assignment
```

```
Assign Horizontal partitions, iteration 0
Routed partition 1/14
Routed partition 2/14
Routed partition 3/14
Routed partition 4/14
Routed partition 5/14
Routed partition 6/14
Routed partition 7/14
Routed partition 8/14
Routed partition 9/14
Routed partition 10/14
Routed partition 11/14
Routed partition 12/14
Routed partition 13/14
Routed partition 14/14
```

```
Assign Vertical partitions, iteration 0
Routed partition 1/14
Routed partition 2/14
Routed partition 3/14
Routed partition 4/14
Routed partition 5/14
Routed partition 6/14
Routed partition 7/14
Routed partition 8/14
Routed partition 9/14
Routed partition 10/14
Routed partition 11/14
Routed partition 12/14
Routed partition 13/14
Routed partition 14/14
```

```
Number of wires with overlap after iteration 0 = 519 of 880
```

Wire length and via report:

```
-----  
Number of M1 wires: 108 : 0  
Number of M2 wires: 346 VIA12SQ_C: 312  
Number of M3 wires: 161 VIA23SQ_C: 250  
Number of M4 wires: 7 VIA34SQ_C: 12  
Number of M5 wires: 4 VIA45SQ_C: 4  
Number of M6 wires: 0 VIA56SQ_C: 0  
Number of M7 wires: 0 VIA67SQ_C: 0  
Number of M8 wires: 0 VIA78SQ_C: 0  
Number of M9 wires: 0 VIA89_C: 0  
Number of MRDL wires: 0 VIA9RDL: 0  
Total number of wires: 626 vias: 578
```

```
Total M1 wire length: 49.2  
Total M2 wire length: 379.0  
Total M3 wire length: 275.6  
Total M4 wire length: 13.7  
Total M5 wire length: 11.1  
Total M6 wire length: 0.0  
Total M7 wire length: 0.0  
Total M8 wire length: 0.0  
Total M9 wire length: 0.0  
Total MRDL wire length: 0.0  
Total wire length: 728.6
```

```
Longest M1 wire length: 5.5  
Longest M2 wire length: 13.4  
Longest M3 wire length: 9.0  
Longest M4 wire length: 5.2  
Longest M5 wire length: 4.1  
Longest M6 wire length: 0.0  
Longest M7 wire length: 0.0  
Longest M8 wire length: 0.0  
Longest M9 wire length: 0.0
```

Nets that have been changed:

Net 1 = a[7]
Net 2 = a[6]
Net 3 = a[5]
Net 4 = a[4]
Net 5 = a[3]
Net 6 = a[2]
Net 7 = a[1]
Net 8 = a[0]
Net 9 = b[7]
Net 10 = b[6]
Net 11 = b[5]
Net 12 = b[4]
Net 13 = b[3]
Net 14 = b[2]
Net 15 = b[1]
Net 16 = b[0]
Net 17 = cin
Net 18 = clk
Net 19 = sum[7]
Net 20 = sum[6]
Net 21 = sum[5]
Net 22 = sum[4]
Net 23 = sum[3]
Net 24 = sum[2]
Net 25 = sum[1]
Net 26 = sum[0]
Net 27 = cout
Net 28 = fsum[7]
Net 29 = fsum[6]
Net 30 = fsum[5]
Net 31 = fsum[4]
Net 32 = fsum[3]
Net 33 = fsum[2]
Net 34 = fsum[1]
Net 35 = fsum[0]
Net 36 = fcout

Net 36 = fcout
Net 37 = n1
Net 38 = n2
Net 39 = n3
Net 40 = n4
Net 41 = n5
Net 42 = n7
Net 43 = n8
Net 44 = n9
Net 45 = n10
Net 46 = n11
Net 47 = n12
Net 48 = n13
Net 49 = n14
Net 50 = n15
Net 51 = n16
Net 52 = n17
Net 53 = n18
Net 54 = n19
Net 55 = n20
Net 56 = n21
Net 57 = ctosc_drc_0
Net 58 = n23
Net 59 = n24
Net 60 = n25
Net 61 = n26
Net 62 = n27
Net 63 = n28
Net 64 = n31
Net 65 = n32
Net 66 = n35
Net 67 = n36
Net 68 = n37
Net 69 = n38
Net 70 = n40
Net 71 = n41
Net 72 = n42

```
Net 68 = n37
Net 69 = n38
Net 70 = n40
Net 71 = n41
Net 72 = n42
Net 73 = n43
Net 74 = n45
Net 75 = n46
Net 76 = n47
Net 77 = n48
Net 78 = n49
Net 79 = n50
Net 80 = n51
Net 81 = n52
Net 82 = n53
Net 83 = n54
Net 84 = n56
Net 85 = n57
Net 86 = n58
Net 87 = n59
Net 88 = n60
Net 89 = n61
Net 90 = n62
Net 91 = n63
Net 92 = n64
Net 93 = n65
Net 94 = n66
Net 95 = n67
Net 96 = n68
Net 97 = n69
Net 98 = n70
Net 99 = n71
Net 100 = n72
.... and 31 other nets
Total number of changed nets = 131 (out of 133)
```

```

SCENARIO QOR
-----
Scene PG WNS TNS R2RTNS NSV WHV THV NHV MaxTrnV MaxTranC MaxCapV Leakage
1 * 0.0000 0.0000 0.0000 0 0.0000 0.0000 0 0 0 0.0000 0 522977472

DESIGN QOR
-----
Scene PG WNS TNS R2RTNS NSV WHV THV NHV MaxTrnV MaxTranC MaxCapV Leakage Area InstCnt
* * 0.0000 0.0000 0.0000 0 0.0000 0.0000 0 0 0 0.0000 0 522977472 256.43 113

Route-opt final QoR Summary WNS TNS R2RTNS NSV WHV THV NHV MaxTrnV MaxCapV Leakage Area InstCnt
Route-opt final QoR Summary 0.0000 0.0000 0.0000 0 0.0000 0.0000 0 0 0 0 0.0000 0 256.43 113
Route-opt optimization complete 0.00 0.00 0.00 7 256.43 522977472.00 113 5.53 1443
Route-opt command complete CPU: 513 s ( 0.14 hr ) ELAPSE: 19919 s ( 5.53 hr ) MEM-PEAK: 1443 MB

```

Saving spef(standard parasitic exchange format) file in the results directory of ICCII directory.

Spef file contains parasitic capacitance and resistance of the design (nodes, wires & pins).

```

132 create_routing_blockage -layers {HS} -bbox [ -expr $ctrl_height -$blockage_w
133 write_verilog ./results/CLA1.routed.v
134 write_sdc -output ./results/CLA1.routed.sdc
135 write_parasitics -format spef -output ./results/CLA1.spef
136 history

```

spef file has been saved in results of ICCII.

```

Terminal - ws1_7@ws1:~/Desktop/SRM_Workshop/ICCII/results
File Edit View Terminal Tabs Help
over_utilization_default.tcl
over_utilization_default.tcl.old
over_utilization_default.tcl.old.01
over_utilization_default.tcl.old.02
over_utilization_default.tcl.old.03
reports
results
scripts
work_dir
[ws1_7@ws1 ICCII]$ cd scripts/
[ws1_7@ws1 scripts]$ ls
clock.tcl      icc2_command.log  placement.tcl      route.tcl
floorplan.tcl  icc2_output.txt   power_planning.tcl
[ws1_7@ws1 scripts]$ vi clock.tcl
[ws1_7@ws1 scripts]$ vi route.tcl
[ws1_7@ws1 scripts]$ cd ..
[ws1_7@ws1 ICCII]$ cd results
[ws1_7@ws1 results]$ ls
CLA1.routed.sdc          full_adder_func::nom.spef.p1_125.spef
CLA1.routed.v            full_adder_func::nom.spef.p2_125.spef
CLA1.spef.p1_125.spef   full_adder_func::nom.spef.spef_scenario
CLA1.spef.p2_125.spef   full_adder.routed.sdc
CLA1.spef.spef_scenario full_adder.routed.v
[ws1_7@ws1 results]$ 

```

Sub.routed.v file

```
Terminal - wsl_7@wsl:~/Desktop/SRM_Workshop/ICCI/results

File Edit View Terminal Tabs Help
// IC Compiler II Version V-2023.12 Verilog Writer
// Generated on 7/11/2024 at 6:34:27
// Library Name: EIGHT_BIT_ADDER_LIB1
// Block Name: eight_bit_adder.v
// User Label:
// Write Command: write_verilog ./results/CLA1.routed.v
module CLA1 ( a , b , cin , clk , sum , cout , fsum , fcout ) ;
input [7:0] a ;
input [7:0] b ;
input cin ;
input clk ;
output [7:0] sum ;
output cout ;
output [7:0] fsum ;
output fcout ;

DFFX1_RVT \fsum_reg[7] ( .D ( sum[7] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[7] ) ) ;
DFFX1_RVT \fsum_reg[6] ( .D ( sum[6] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[6] ) ) ;
DFFX1_RVT \fsum_reg[5] ( .D ( sum[5] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[5] ) ) ;
DFFX1_RVT \fsum_reg[4] ( .D ( sum[4] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[4] ) ) ;
DFFX1_RVT \fsum_reg[3] ( .D ( sum[3] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[3] ) ) ;
DFFX1_RVT \fsum_reg[2] ( .D ( sum[2] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[2] ) ) ;
DFFX1_RVT \fsum_reg[1] ( .D ( sum[1] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[1] ) ) ;
DFFX1_RVT \fsum_reg[0] ( .D ( sum[0] ) , .CLK ( ctosc_drc_0 ) ,
.Q ( fsum[0] ) ) ;
DFFX1_RVT fcout_reg ( .D ( cout ) , .CLK ( ctosc_drc_0 ) , .Q ( fcout ) ) ;
INVX0_RVT U3 ( .A ( a[0] ) , .Y ( n1 ) ) ;
AND2X1_RVT U4 ( .A1 ( n90 ) , .A2 ( n89 ) , .Y ( n91 ) ) ;
OR2X1_RVT U5 ( .A1 ( n1 ) , .A2 ( b[0] ) , .Y ( n9 ) ) ;
```

File Edit View Terminal Tabs Help

```

AND2X1_RVT U82 ( .A1 ( a[5] ) , .A2 ( b[5] ) , .Y ( n71 ) ) ;
AND2X1_RVT U83 ( .A1 ( a[6] ) , .A2 ( n59 ) , .Y ( n62 ) ) ;
OR2X1_RVT U84 ( .A1 ( n59 ) , .A2 ( a[6] ) , .Y ( n60 ) ) ;
OR2X1_RVT U85 ( .A1 ( n62 ) , .A2 ( n61 ) , .Y ( n74 ) ) ;
OR2X1_RVT U86 ( .A1 ( n63 ) , .A2 ( n74 ) , .Y ( n66 ) ) ;
AND2X1_RVT U87 ( .A1 ( n74 ) , .A2 ( n63 ) , .Y ( n64 ) ) ;
INVX0_RVT U88 ( .A ( n64 ) , .Y ( n65 ) ) ;
AND2X1_RVT U89 ( .A1 ( n66 ) , .A2 ( n65 ) , .Y ( sum[6] ) ) ;
AND2X1_RVT U90 ( .A1 ( a[7] ) , .A2 ( n67 ) , .Y ( n70 ) ) ;
OR2X1_RVT U91 ( .A1 ( n67 ) , .A2 ( a[7] ) , .Y ( n68 ) ) ;
OR2X1_RVT U92 ( .A1 ( n70 ) , .A2 ( n69 ) , .Y ( n78 ) ) ;
AND2X1_RVT U93 ( .A1 ( a[6] ) , .A2 ( b[6] ) , .Y ( n75 ) ) ;
OR2X1_RVT U96 ( .A1 ( n75 ) , .A2 ( n74 ) , .Y ( n77 ) ) ;
AND2X1_RVT U97 ( .A1 ( n80 ) , .A2 ( n77 ) , .Y ( n76 ) ) ;
OR2X1_RVT U98 ( .A1 ( n78 ) , .A2 ( n76 ) , .Y ( n82 ) ) ;
AND3X1_RVT ctmTdsLR_3_4 ( .A1 ( n35 ) , .A2 ( tmp_net0 ) , .A3 ( tmp_net1 ) ,
.Y ( sum[4] ) ) ;
INVX0_RVT U101 ( .A ( n84 ) , .Y ( n81 ) ) ;
AND2X1_RVT U102 ( .A1 ( n82 ) , .A2 ( n81 ) , .Y ( sum[7] ) ) ;
AND2X1_RVT U103 ( .A1 ( a[7] ) , .A2 ( b[7] ) , .Y ( n83 ) ) ;
OR2X1_RVT U104 ( .A1 ( n83 ) , .A2 ( n84 ) , .Y ( cout ) ) ;
AND2X1_RVT U105 ( .A1 ( n85 ) , .A2 ( n10 ) , .Y ( n88 ) ) ;
AND2X1_RVT U106 ( .A1 ( cin ) , .A2 ( n86 ) , .Y ( n87 ) ) ;
OR2X1_RVT U107 ( .A1 ( n88 ) , .A2 ( n87 ) , .Y ( sum[0] ) ) ;
OR2X1_RVT U108 ( .A1 ( n90 ) , .A2 ( n89 ) , .Y ( n93 ) ) ;
AND2X1_RVT U109 ( .A1 ( n93 ) , .A2 ( n92 ) , .Y ( sum[1] ) ) ;
OR2X1_RVT U110 ( .A1 ( n95 ) , .A2 ( n94 ) , .Y ( n98 ) ) ;
AND2X1_RVT U111 ( .A1 ( n98 ) , .A2 ( n97 ) , .Y ( sum[2] ) ) ;
OR2X1_RVT U112 ( .A1 ( n100 ) , .A2 ( n99 ) , .Y ( n103 ) ) ;
AND2X1_RVT U113 ( .A1 ( n103 ) , .A2 ( n102 ) , .Y ( sum[3] ) ) ;
OR3X1_RVT ctmTdsLR_1_0 ( .A1 ( n36 ) , .A2 ( n46 ) , .A3 ( n101 ) ,
.Y ( n35 ) ) ;
AND3X1_RVT ctmTdsLR_1_1 ( .A1 ( n80 ) , .A2 ( n77 ) , .A3 ( n78 ) ,
.Y ( n84 ) ) ;
endmodule

```

Sub.routed.sdc file

```
Terminal - wsl_7@wsl:~/Desktop/SRM_Workshop/ICClI/results
File Edit View Terminal Tabs Help
#####
# Design name: eight_bit_adder.v
#
# Created by icc2 write_sdc on Thu Jul 11 06:35:06 2024
#
#####
set sdc_version 2.1
set_units -time ns -resistance M0hm -capacitance fF -voltage V -current uA
#####
#
# Units
# time_unit : 1e-09
# resistance_unit : 1000000
# capacitive_load_unit : 1e-15
# voltage_unit : 1
# current_unit : 1e-06
# power_unit : 1e-12
#####

# Mode: func
# Corner: nom
# Scenario: func::nom

# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 1
create_clock -name clk -period 1 -waveform {0 0.5} [get_ports {clk}]
set_propagated_clock [get_clocks {clk}]
# Warning: Libcell power domain derates are skipped!

# Set latency for io paths.
# -origin useful_skew
set_clock_latency -min 0.03582 [get_clocks {clk}]
# -origin useful_skew
"CLA1.routed.sdc" 152L, 8715C
```

```
Terminal - wsl_7@wsl:~/Desktop/SRM_Workshop/ICClI/results
File Edit View Terminal Tabs Help
set_input_transition 0.15 [get_ports {a[0]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[7]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[6]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[5]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[4]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[3]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[2]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[1]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {b[0]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {cin}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 4
set_input_transition 0.15 [get_ports {clk}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[7]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[6]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[5]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[4]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[3]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[2]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
set_input_delay -clock [get_clocks {clk}] -max 0.6 [get_ports {a[1]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 3
```

```
Terminal - wsl_7@wsl:~/Desktop/SRM_Workshop/ICClI/results

File Edit View Terminal Tabs Help
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[6]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[5]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[4]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[3]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[2]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[1]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {sum[0]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {cout}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[7]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[6]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[5]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[4]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[3]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[2]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[1]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fsum[0]}]
# /ve/ws_home/wsl_7/Desktop/SRM_Workshop/CONSTRAINTS/CLA1.sdc, line 6
set_output_delay -clock [get_clocks {clk}] -max 0.4 [get_ports {fcout}]
set_max_transition 0.25 [current_design]
Set_max_transition 0.1 [get_clocks {clk}] -clock_path
```

Sub.spef – It is spef file of p1 parasitic.

```
*SPEF "1481-1998"
*DESIGN "CLAI"
*DATE "Thu Jul 11 06:35:42 2024"
*VENDOR "Synopsys, Inc."
*PROGRAM "icc2 /usr/synopsys/icc2/V-2023.12/linux64/nwtn/bin/icc2_exec"
*VERSION "V-2023.12 Nov 23, 2023"
*DESIGN_FLOW "ICC2 SPEF DR"
*DIVIDER /
*DELIMITER :
*BUS_DELIMITER [ ]
*T_UNIT 1 NS
*C_UNIT 1 FF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY

// XY_UNIT 1 UM
// PARASITIC_TECH p1 at 125.000 degree

*NAME_MAP
*1 a[7]
*2 a[6]
*3 a[5]
*4 a[4]
*5 a[3]
*6 a[2]
*7 a[1]
*8 a[0]
*9 b[7]
*10 b[6]
*11 b[5]
*12 b[4]
*13 b[3]
*14 b[2]
*15 b[1]
*16 b[0]
*17 cin
```

Sub.spef – It is spef file of p2 parasitic.

```
*SPEF "1481-1998"
*DESIGN "CLAI"
*DATE "Thu Jul 11 06:35:42 2024"
*VENDOR "Synopsys, Inc."
*PROGRAM "icc2 /usr/synopsys/icc2/V-2023.12/linux64/nwtn/bin/icc2_exec"
*VERSION "V-2023.12 Nov 23, 2023"
*DESIGN_FLOW "ICC2 SPEF DR"
*DIVIDER /
*DELIMITER :
*BUS_DELIMITER [ ]
*T_UNIT 1 NS
*C_UNIT 1 FF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY

// XY_UNIT 1 UM
// PARASITIC_TECH p2 at 125.000 degree

*NAME_MAP
*1 a[7]
*2 a[6]
*3 a[5]
*4 a[4]
*5 a[3]
*6 a[2]
*7 a[1]
*8 a[0]
*9 b[7]
*10 b[6]
*11 b[5]
*12 b[4]
*13 b[3]
*14 b[2]
*15 b[1]
*16 b[0]
*17 cin
```

‘report_design’ – It generates the report of the design summary after routing stage.

```
lcc2_shell> report_design
*****
Report : design
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 07:13:30 2024
*****
Total number of std cells in library : 286
Total number of dont_use lib cells : 85
Total number of dont_touch lib cells : 7
Total number of buffers : 11
Total number of inverters : 15
Total number of flip-flops : 106
Total number of latches : 12
Total number of ICGs : 12

Cell Instance Type Count      Area
-----
TOTAL LEAF CELLS    113    256.431
unit                 113    256.431
Standard cells       113    256.431
unit                 113    256.431
Hard macro cells     0      0.000
unit                 113    256.431
Soft macro cells     0      0.000
unit                 113    256.431
Always on cells      0      0.000
unit                 113    256.431
Physical only        0      0.000
unit                 113    256.431
Fixed cells          0      0.000
unit                 113    256.431
Moveable cells        113    256.431
unit                 113    256.431
Placed cells         112    251.348
unit                 113    256.431

Logic Hierarchies      : 0
Design Masters count  : 7
Total Flat nets count : 133
Total FloatingNets count : 0
Total no of Ports     : 38
Number of Master Clocks in design : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design : 7 (1 of them Non Default)
Number of Scan Chains in design : 0
List of Modes          : func
List of Corners        : nom
List of Scenarios      : func::nom

Core Area              : 430.012
Chip Area              : 517.004
Total Site Row Area    : 430.012
Number of Blockages    : 1
Total area of Blockages: 42.994
Number of Power Domains: 1
Number of Voltage Areas: 1
Number of Group Bounds : 0
Number of Exclusive MoveBounds: 0
Number of Hard or Soft MoveBounds: 0
Number of Multibit Registers: 0
Number of Multibit LS/ISO Cells: 0
Number of Top Level RP Groups: 0
Number of Tech Layers   : 71 (61 of them have unknown routing dir.)

Total wire length      : 756.81 micron
Total number of wires   : 677
Total number of contacts: 1283
```

'report_timing' – It generates timing report of slack, timing path and delays after routing stage.

```
icc2 shell> report timing
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -report_by design
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 07:16:00 2024
*****
Startpoint: a[0] (input port clocked by clk)
Endpoint: sum[7] (output port clocked by clk)
Mode: func
Corner: nom
Scenario: func::nom
Path Group: **in2out_default**
Path Type: max

Point           Incr   Path
-----
clock clk (rise edge)      0.00   0.00
clock network delay (propagated) 0.04   0.04
input external delay        0.60   0.64 f
a[0] (in)                 0.00   0.64 f
U3/Y (INVX0_RVT)          0.03   0.67 r
U5/Y (OR2X1_RVT)          0.04   0.71 r
U35/Y (AND2X1_RVT)         0.03   0.74 r
U37/Y (OR2X1_RVT)          0.03   0.78 r
U38/Y (INVX0_RVT)          0.02   0.79 f
U39/Y (OR2X1_RVT)          0.03   0.82 f
U4/Y (AND2X1_RVT)          0.04   0.86 f
ctmTdsLR_1_5/Y (OR3X1_RVT) 0.03   0.89 f
ctmTdsLR_1_7/Y (AND3X1_RVT) 0.04   0.93 f
ctmTdsLR_1_8/Y (AND3X1_RVT) 0.05   0.98 f
ctmTdsLR_1_10/Y (OR3X1_RVT) 0.03   1.01 f
ctmTdsLR_1_1/Y (AND3X1_RVT) 0.04   1.05 f
U101/Y (INVX0_RVT)          0.01   1.07 r
U102/Y (AND2X1_RVT)         0.03   1.09 r
sum[7] (out)                0.00   1.09 r
data arrival time           1.09

clock clk (rise edge)      1.00   1.00
clock network delay (propagated) 0.04   1.04
clock uncertainty           1.20   2.24
output external delay       -0.40   1.84
data required time          1.84

data required time           1.84
data arrival time            1.09

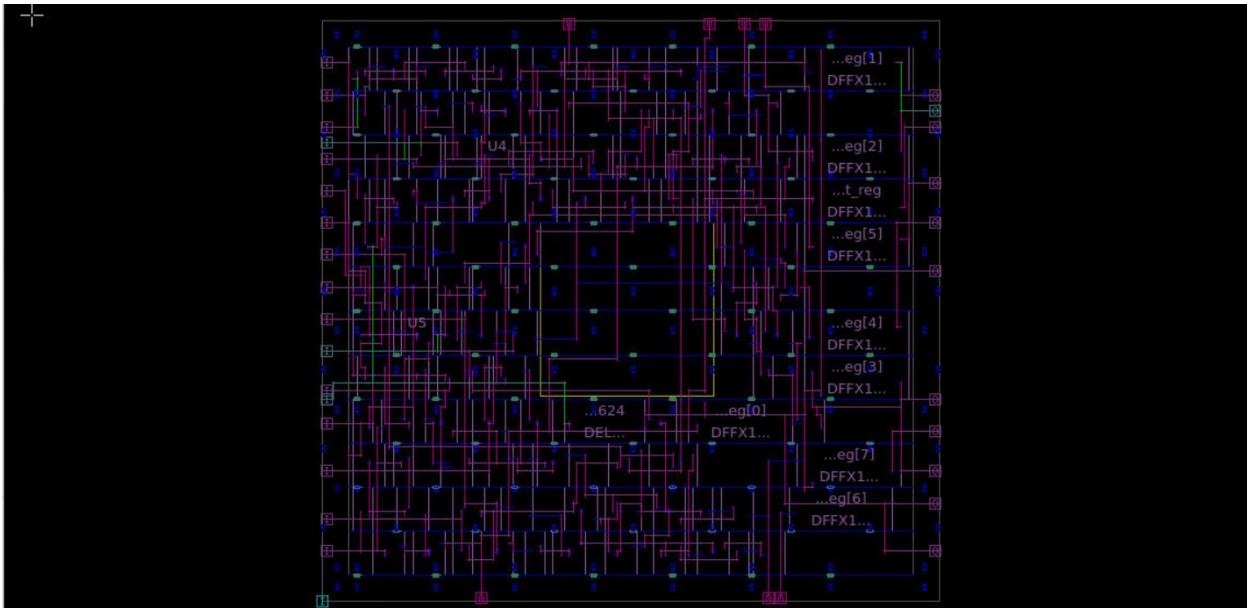
-----
slack (MET)                  0.74
```

1

Command for Routing Stage

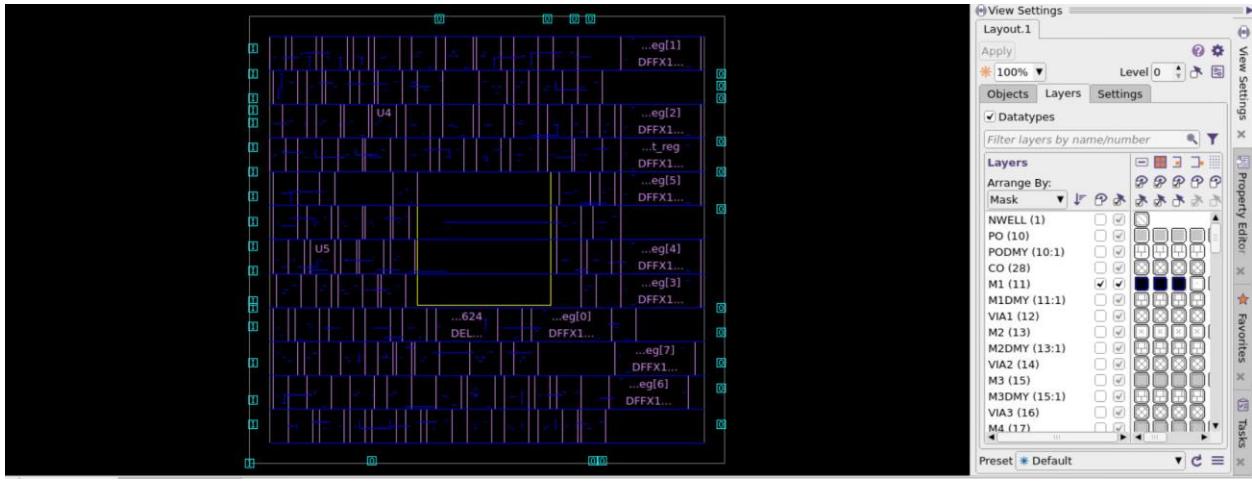
```
114 set_app_options -name route.global.timing_driven -value true
115 set_app_options -name route.global.crosstalk driven -value false
116 set_app_options -name route.track.timing_driven -value true
117 set_app_options -name route.track.crosstalk driven -value true
118 set_app_options -name route.detail.timing_driven -value true
119 set_app_options -name route.detail.save_after_iterations -value false
120 set_app_options -name route.detail.force_max_number_iterations -value false
121 set_app_options -name route.detail.antenna -value true
122 set_app_options -name route.detail.antenna_fixing_preference -value use_diodes
123 set_app_options -name route.detail.diode_libcell_names -value */ANTENNA_RVT
124 route_opt
125 history
126 set min_width_M3 0.1
127 set blockage_width [expr $min_width_M3 * 2]
128 create_routing_blockage -layers {M3} -bbox {0 0 $chip_width $blockage_width} ; # bottom boundary
129 create_routing_blockage -layers {M3} -bbox {0 [expr $chip_height -$blockage_width] $chip_width $chip_height} ; #top boundary
130 create_routing_blockage -layers {M3} -bbox {0 [expr $chlo_height -$blockage_width] $chip_width $chip_height} ;#top boundary
131 create_routing_blockage -layers {M3} -bbox {0 0 $chip_width $blockage_width} ; # left boundary
132 create_routing_blockage -layers {M3} -bbox {[expr $chlo_height -$blockage_width] $chip_width $chip_height} ;#right boundary
133 write_verilog ./results/CLAI.routed.v
134 write_sdc -output ./results/CLAI.routed.sdc
135 write_parasitics -format spef -output ./results/CLAI.spef
136 history
cc2 shell> 
```

Output for routing:



- **Save Design and Library:** It is crucial to save the design and library after each stage. These intermediate results should be saved in the ICCII directory.
- **Generate Reports:** Obtain design and timing reports after every stage of the design process to ensure accuracy and track progress.

Metal-1: Used in power rails and detailed route



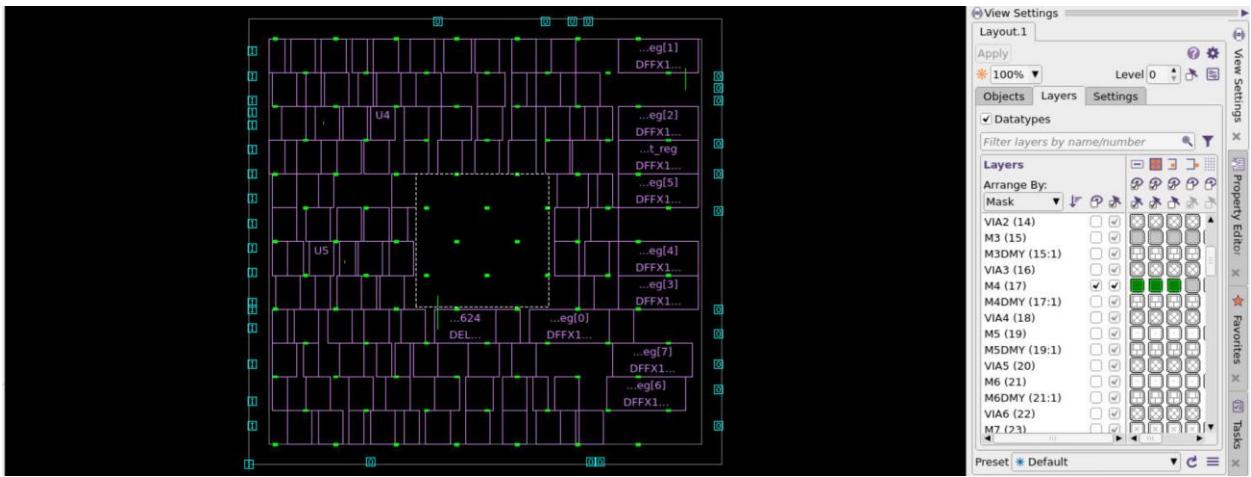
Metal-2:



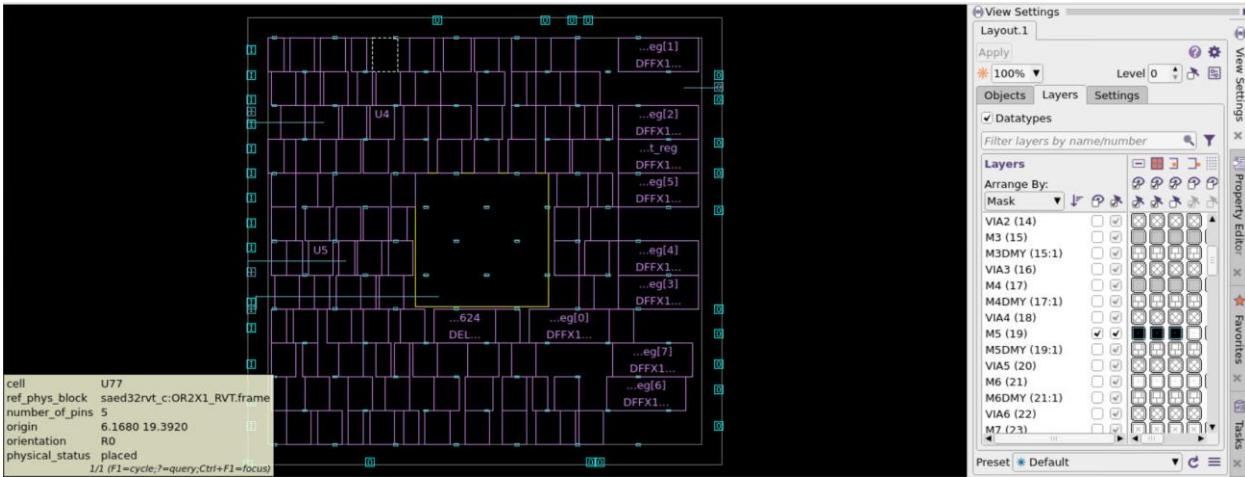
Metal-3



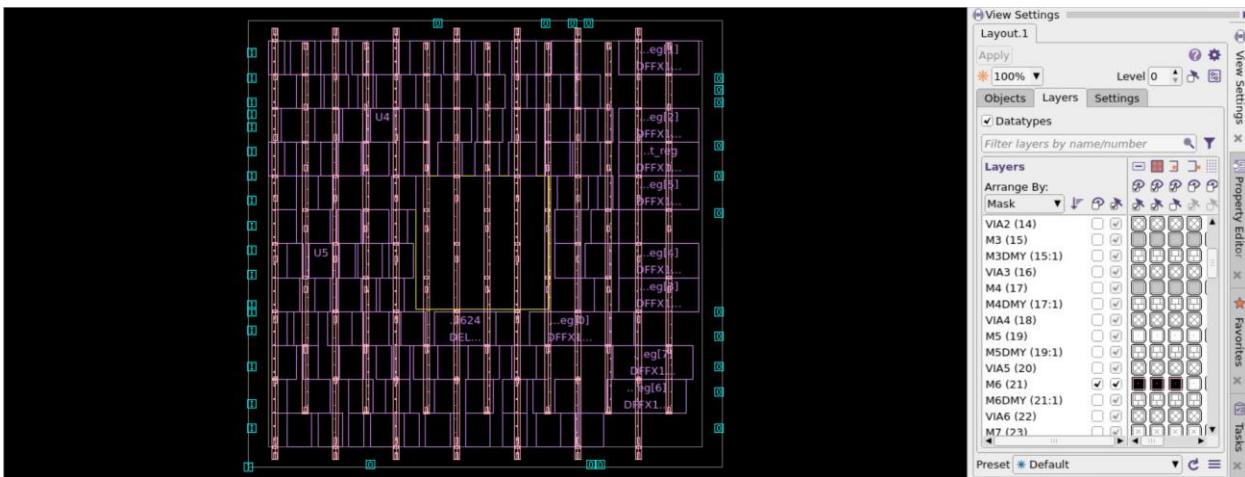
Metal-4



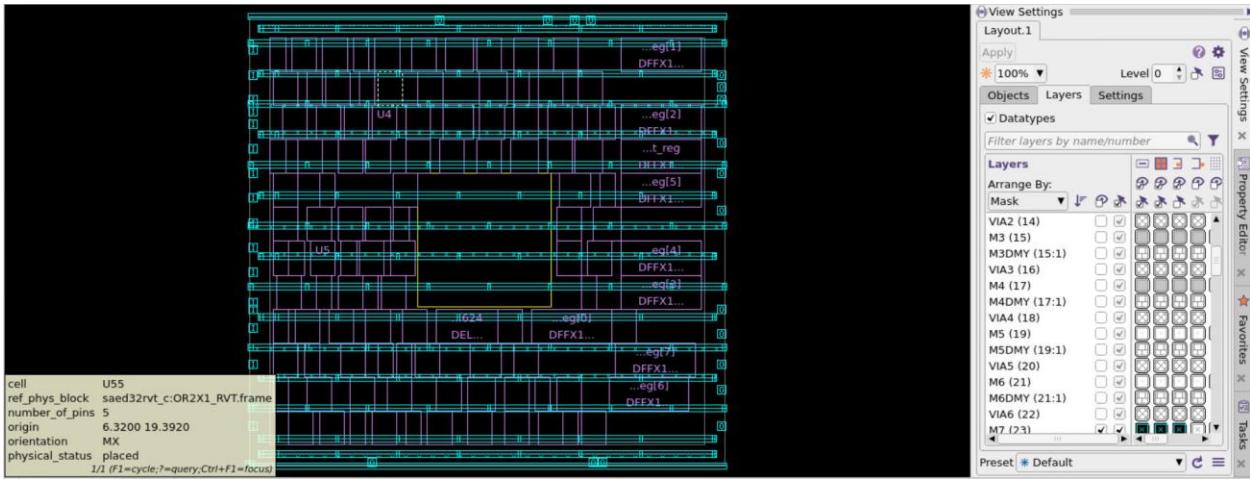
Metal-5



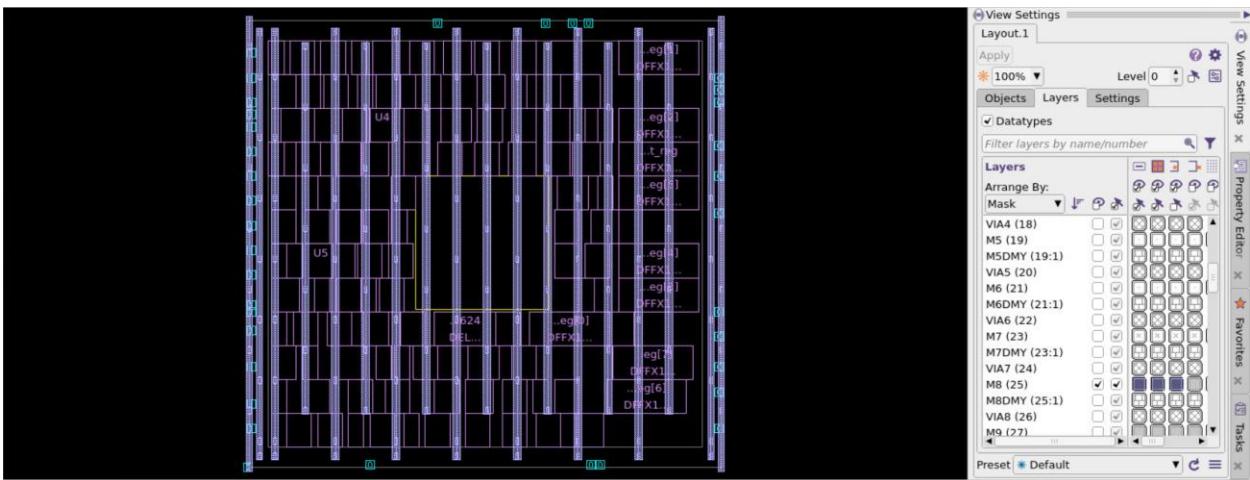
Metal-6



Metal-7



Metal-8



All Vias connections:



8.Timing Analysis:

- **Critical Process:** Timing analysis is essential for ensuring the design meets its timing specifications.
- **Key Components:** This process includes setup and hold times, delays, timing paths, propagation delay, clock skew, and slack.
- **Tool Used:** PrimeTime (PT) is used for timing analysis.

Instructions for PT

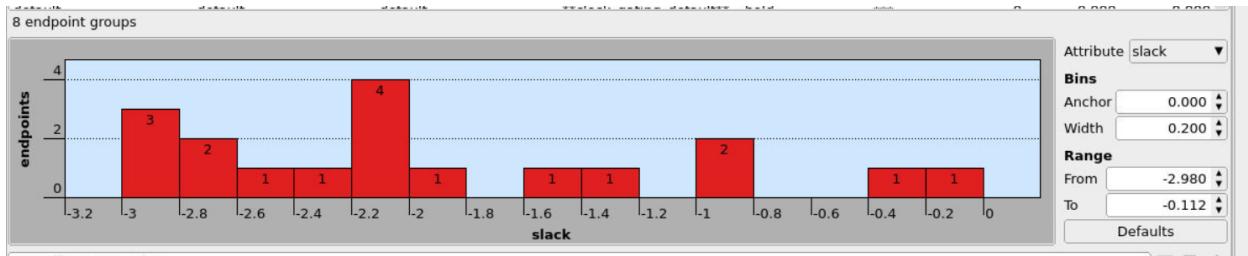
- **Invoke PrimeTime:** Go to the PT directory and run pt_shell.
- **Set Path:** The first step is to set the path for stdcell_rvt in the library file. RVT stands for Regular Voltage Threshold, offering a balance between High Voltage Threshold (HVT) and Low Voltage Threshold (LVT).

Then read routed .v, .sdc and .spf files

```
pt_shell> start gui
pt_shell> set link_path "../../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db"
../../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db
pt_shell> read_verilog "../../ICCII/results/CLAI.routed.v"
l
pt_shell> link_design
Loading db file '/ve/ws_home/wsl_7/Desktop/SRM_Workshop/ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db'
Loading verilog file '/ve/ws_home/wsl_7/Desktop/SRM_Workshop/ICCII/results/CLAI.routed.v'
Linking design CLAI...
Information: 287 (97.62%) library cells are unused in library saed32rvt_ss0p7vn40c..... (LNK-045)
Information: total 287 library cells are unused (LNK-046)
Design 'CLAI' was successfully linked.
Information: There are 150 leaf cells, ports, hiers and 131 nets in the design (LNK-047)
l
pt_shell> current_design CLAI
{"CLAI"}
pt_shell> read_sdc ../../CONSTRAINTS/CLAI.sdc

Reading SDC version 2.1...
Warning: Setting input delay on clock port (clk) relative to a clock (clk) defined at the same port. Command is ignored. (UITE-489)
Warning: Negative clock uncertainty specified: -1.2 (UITE-302)
Warning: Negative clock uncertainty specified: -1 (UITE-302)
l
l
pt_shell>
pt_shell> read_parasitics "../../ICCII/results/CLAI_func::nom.spf.p1.l25.spf"
Information: Log for 'read_parasitics' command will be generated in 'parasitics_command.log'. (PARA-107)
Information: read_parasitics command is executed in background
l
pt_shell>
pt_shell> update_timing -full
Information: Using automatic max wire load selection group 'predcaps'. (ENV-003)
Information: Using automatic min wire load selection group 'predcaps'. (ENV-003)
Information: Building multi voltage information for entire design. (MV-022)
l
pt_shell> ■
```

In GUI, we get the timing analysis



‘report_design’ – It generates the report of the design after timing analysis

```
pt shell> report design
*****
Report : design
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 14:13:55 2024
*****

Design Attribute          Value
-----
Operating Conditions:
analysis_type           on_chip_variation
operating_condition_min_name ss0p7vn40c
process_min              0.99
temperature_min          -40
voltage_min              0.7
tree_type_min            best_case

operating_condition_max_name ss0p7vn40c
process_max                0.99
temperature_max             -40
voltage_max                 0.7
tree_type_max               best_case

Wire Load:
wire_load_mode           (use report_wire_load for more information)
wire_load_model_max       enclosed
wire_load_model_library_max 8000
wire_load_selection_type_max saed32rvt_ss0p7vn40c
wire_load_model_min        automatic-by-area
8000
wire_load_model_library_min saed32rvt_ss0p7vn40c
wire_load_selection_type_min automatic-by-area
wire_load_selection_group_max predcaps
predcaps
wire_load_selection_group_min predcaps
predcaps
wire_load_min_block_size 0

Design Rules:
max_capacitance          --
min_capacitance          --
max_fanout                --
max_transition             0.25
static_integrity           --
dynamic_integrity          --
max_coupled_transition    0.25
max_area                  --

Timing Ranges:
early_factor               --
late_factor                --

Pin Input Delays:
None specified.

Pin Output Delays:
None specified.
Fast Analysis:             disabled

1
```

report_timing – It generates timing report after timing analysis stage.

```
pt_shell> report_timing
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -sort_by slack
Design : CLAI
Version: V-2023.12
Date  : Thu Jul 11 14:11:46 2024
*****



Startpoint: b[0] (input port clocked by clk)
Endpoint: fsm_reg[7]
          (Rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point           Incr      Path
-----
clock clk (rise edge)    0.00      0.00
clock network delay (ideal) 0.00      0.00
input external delay       0.60      0.60 f
b[0] (in)                0.00      0.60 f
U6/Y (INVX0_RVT)          0.16      0.76 r
U34/Y (OR2X1_RVT)          0.19      0.95 r
U35/Y (AND2X1_RVT)          0.25      1.20 r
U37/Y (OR2X1_RVT)          0.22      1.42 r
U38/Y (INVX0_RVT)          0.08      1.50 f
U39/Y (OR2X1_RVT)          0.31      1.80 f
U4/Y (AND2X1_RVT)           0.29      2.09 f
ctmTdsLR_1_5/Y (OR3X1_RVT) 0.45      2.54 f
ctmTdsLR_1_7/Y (AND3X1_RVT) 0.37      2.91 f
ctmTdsLR_1_8/Y (AND3X1_RVT) 0.39      3.30 f
ctmTdsLR_1_10/Y (OR3X1_RVT) 0.49      3.78 f
U97/Y (AND2X1_RVT)          0.30      4.08 f
U98/Y (OR2X1_RVT)           0.32      4.40 f
U102/Y (AND2X1_RVT)          0.25      4.65 f
fsum_reg[7]/D (DFFX1_RVT)   0.00      4.65 f
data' arrival time          4.65

clock clk (rise edge)      1.00      1.00
clock network delay (ideal) 0.00      1.00
clock reconvergence pessimism 0.00      1.00
clock uncertainty           1.20      2.20
fsum_reg[7]/CLK (DFFX1_RVT) 2.20      2.20
library setup time          -0.53      1.67
data required time           1.67
-----  

data required time           1.67
data arrival time            -4.65
-----  

slack (VIOLATED)           -2.98
```

We are getting negative slack, so we are updating/changing the clock time in CONSTRAINTS.

```
create_clock -period 1 [get_ports clk]

set_input_delay -max 0.6 -clock [get_clocks clk] [all_inputs]
set_input_transition 0.15 [all_inputs]

set_output_delay -max 0.4 -clock [get_clocks clk] [all_outputs]

set_clock_uncertainty -setup -4.2 [get_clocks clk]
set_clock_uncertainty -hold -4 [get_clocks clk]

set_max_transition 0.250 [current_design]
set_max_transition -clock_path 0.100 [get_clocks clk]
~  
~
```

Report timing after changing the clock value:

```
pt_shell> report_timing
Information: Building multi voltage information for entire design. (MV-022)
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -sort_by slack
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 14:20:49 2024
*****  
  
Startpoint: b[0] (input port clocked by clk)
Endpoint: fsm_reg[7]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max  
  
Point           Incr      Path
-----  
clock clk (rise edge)    0.00      0.00
clock network delay (ideal) 0.00      0.00
input external delay       0.60      0.60 f
b[0] (in)                 0.00      0.60 f
U6/Y (INVX0_RVT)          0.16      0.76 r
U34/Y (OR2X1_RVT)          0.19      0.95 r
U35/Y (AND2X1_RVT)         0.25      1.20 r
U37/Y (OR2X1_RVT)          0.22      1.42 r
U38/Y (INVX0_RVT)          0.08      1.50 f
U39/Y (OR2X1_RVT)          0.31      1.80 f
U4/Y (AND2X1_RVT)          0.29      2.09 f
ctmTdsLR 1 5/Y (OR3X1_RVT) 0.45      2.54 f  
  
ctmTdsLR_1_7/Y (AND3X1_RVT) 0.37      2.91 f
ctmTdsLR_1_8/Y (AND3X1_RVT) 0.39      3.30 f
ctmTdsLR_1_10/Y (OR3X1_RVT) 0.49      3.78 f
U97/Y (AND2X1_RVT)          0.30      4.08 f
U98/Y (OR2X1_RVT)           0.32      4.40 f
U102/Y (AND2X1_RVT)         0.25      4.65 f
fsm_reg[7]/D (DFFX1_RVT)   0.00      4.65 f
data arrival time           4.65  
  
clock clk (rise edge)      1.00      1.00
clock network delay (ideal) 0.00      1.00
clock reconvergence pessimism 0.00      1.00
clock uncertainty           4.20      5.20
fsm_reg[7]/CLK (DFFX1_RVT)  5.20      5.20 r
library setup time           -0.53     4.67
data required time           4.67  
  
data required time           4.67
data arrival time             -4.65  
  
slack (MET)                  0.02
```

Now we are getting slack as 0.32

Now we fixed the clock in CONSTRAINTS in ‘CL1.sdc’ .So we are checking the report and report time.

a) Report_timing:

```
pt_shell> report_timing
Information: Building multi voltage information for entire design. (MV-022)
*****
Report : timing
  -path_type full
  -delay_type max
  -max_paths 1
  -sort_by slack
Design : CLAI_
Version: V-2023.12
Date  : Thu Jul 11 14:20:49 2024
*****  
  
Startpoint: b[0] (input port clocked by clk)
Endpoint: fsm_reg[7]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max  
  
Point           Incr      Path
-----  
clock clk (rise edge)    0.00      0.00
clock network delay (ideal) 0.00      0.00
input external delay       0.60      0.60 f
b[0] (in)                 0.00      0.60 f
U6/Y (INVX0_RVT)          0.16      0.76 r
U34/Y (OR2X1_RVT)          0.19      0.95 r
U35/Y (AND2X1_RVT)         0.25      1.20 r
U37/Y (OR2X1_RVT)          0.22      1.42 r
U38/Y (INVX0_RVT)          0.08      1.50 f
U39/Y (OR2X1_RVT)          0.31      1.80 f
U4/Y (AND2X1_RVT)          0.29      2.09 f
ctmTdsLR 1 5/Y (OR3X1_RVT) 0.45      2.54 f  
  
ctmTdsLR_1_7/Y (AND3X1_RVT) 0.37      2.91 f
ctmTdsLR_1_8/Y (AND3X1_RVT) 0.39      3.30 f
ctmTdsLR_1_10/Y (OR3X1_RVT) 0.49      3.78 f
U97/Y (AND2X1_RVT)          0.30      4.08 f
U98/Y (OR2X1_RVT)           0.32      4.40 f
U102/Y (AND2X1_RVT)         0.25      4.65 f
fsm_reg[7]/D (DFFX1_RVT)   0.00      4.65 f
data arrival time           4.65  
  
clock clk (rise edge)      1.00      1.00
clock network delay (ideal) 0.00      1.00
clock reconvergence pessimism 0.00      1.00
clock uncertainty           4.20      5.20
fsm_reg[7]/CLK (DFFX1_RVT)  5.20      5.20 r
library setup time           -0.53     4.67
data required time           4.67  
  
-----  
data required time           4.67
data arrival time             -4.65  
  
-----  
slack (MET)                  0.02
```

1

b) report_design:

```

report_design
*****
Report : design
Design : CLA1
Version: V-2023.12
Date   : Thu Jul 11 14:34:00 2024
*****



Design Attribute          Value
-----
Operating Conditions:
analysis_type           on_chip_variation
operating_condition_min_name ss0p7vn40c
process_min              0.99
temperature_min          -40
voltage_min              0.7
tree_type_min            best_case

operating_condition_max_name ss0p7vn40c
process_max               0.99
temperature_max           -40
voltage_max               0.7
tree_type_max             best_case

Wire Load:
wire_load_mode           (use report_wire_load for more information)
enclosed                  8000
wire_load_model_max       saed32rvt_ss0p7vn40c
wire_load_model_library_max automatic-by-area
wire_load_selection_type_max 8000
wire_load_model_min       saed32rvt_ss0p7vn40c
wire_load_library_min     automatic-by-area
wire_load_selection_type_min predcaps
wire_load_selection_group_max predcaps
wire_load_selection_group_min predcaps
wire_load_min_block_size  0

Design Rules:
max_capacitance          --
min_capacitance          --
max_fanout                --
max_transition            0.25
static_integrity           --
dynamic_integrity          --
max_coupled_transition    0.25
max_area                  --

Timing Ranges:
early_factor              --
late_factor                --

Pin Input Delays:
None specified.

Pin Output Delays:
None specified.

Fast Analysis:           disabled

```

c) Get ports and pins : gives all ports and pins from the design

```
pt shell> get_ports
["a[7]", "a[6]", "a[5]", "a[4]", "a[3]", "a[2]", "a[1]", "a[0]", "b[7]", "b[6]", "b[5]", "b[4]", "b[3]", "b[2]", "b[1]", "b[0]", "cin", "clk", "sum[7]", "sum[6]", "sum[5]", "sum[4]", "sum[3]", "sum[2]", "sum[1]", "sum[0]", "cout", "fsum[7]", "fsum[6]", "fsum[5]", "fsum[4]", "fsum[3]", "fsum[2]", "fsum[1]", "fsum[0]", "fcout"]
pt shell> 
```

d) report_clock and saving:

```

pt_shell> report_clock
*****
Report : clock
Design : CLAI
Version: V-2023.12
Date  : Thu Jul 11 14:39:20 2024
*****  

Attributes:
  p - Propagated clock
  G - Generated   clock
  I - Inactive    clock  

Clock          Period      Waveform        Attrs      Sources
-----{clk}-----{1.00}-----{0 0.5}-----{clk}
1
pt_shell> check_timing -verbose > ./reports/check_timing/check_timing.pl_report
pt_shell> report_global_timing > ./reports/timing/report_global_timing.pl_report
pt_shell> report_clock_skew -attribute > ./reports/clock/report_clock.pl_report
pt_shell> report_analysis_coverage > ./reports/analysis_coverage/report_analysis_coverage.pl_report
pt_shell> report_timing -slack_lesser_than 0.0 -delay min_max -nosplit -input -net > ./reports/timing/report_timing.pl_report
pt_shell> 1

```

e) Reports are saved successful or not. we are checking the files

```
[wsl_7@wsl Desktop]$ cd SRM_Workshop/
[wsl_7@wsl SRM Workshop]$ ls
CONSTRAINTS_DC_ICCII_PT_ref_rtl_run_dc.tcl
[wsl_7@wsl SRM Workshop]$ cd CONSTRAINTS/
[wsl_7@wsl CONSTRAINTS]$ ls
CLAI.sdc full_adder.sdc
[wsl_7@wsl CONSTRAINTS]$ cd CLAI.sdc
bash: cd: CLAI.sdc: Not a directory
[wsl_7@wsl CONSTRAINTS]$ vi CLAI.sdc
[wsl_7@wsl CONSTRAINTS]$ vi CLAI.sdc
[wsl_7@wsl CONSTRAINTS]$ cd ..
[wsl_7@wsl SRM Workshop]$ cd PT
[wsl_7@wsl PT]$ ls
parasitics_command.log pt_shell_command.log reports scripts
[wsl_7@wsl PT]$ cd reports/
[wsl_7@wsl reports]$ ls
analysis_coverage check_timing clock timing
[wsl_7@wsl reports]$ cd check_timing/
[wsl_7@wsl check_timing]$ ls
check_timing.pl_report
[wsl_7@wsl check_timing]$ vi check_timing.pl_report
[wsl_7@wsl check_timing]$ cd ..
[wsl_7@wsl reports]$ cd clock/
[wsl_7@wsl clock]$ ls
report_clock.pl_report
[wsl_7@wsl clock]$ vi report_clock.pl_report
[wsl_7@wsl clock]$ cd ..
[wsl_7@wsl reports]$ cd timing/
[wsl_7@wsl timing]$ ls
report_global_timing.pl_report report_timing.pl_report
[wsl_7@wsl timing]$
```

f) same as p2 results:

```
[wsl_7@wsl reports]$ ls
analysis_coverage check_timing clock timing
[wsl_7@wsl reports]$ cd check_timing/
[wsl_7@wsl check_timing]$ ls
check_timing.pl_report check_timing.p2_report
[wsl_7@wsl check_timing]$ cd ..
[wsl_7@wsl reports]$ cd clock
[wsl_7@wsl clock]$ ls
report_clock.pl_report report_clock.p2_report
[wsl_7@wsl clock]$ cd ..
[wsl_7@wsl reports]$ cd timing/
[wsl_7@wsl timing]$ ls
report_global_timing.pl_report report_global_timing.p2_report report_timing.pl_report report_timing.p2_report
[wsl_7@wsl timing]$
```

Hence all outputs are saved successfully

9.Exploring the Results:

P1:

- Analysis coverage:

```
*****  
Report : analysis_coverage  
Design : CLA1  
Version: V-2023.12  
Date : Thu Jul 11 14:40:39 2024  
*****  


| Type of Check   | Total | Met       | Violated | Untested  |
|-----------------|-------|-----------|----------|-----------|
| setup           | 9     | 9 (100%)  | 0 ( 0%)  | 0 ( 0%)   |
| hold            | 9     | 0 ( 0%)   | 0 ( 0%)  | 9 (100%)  |
| min_pulse_width | 18    | 18 (100%) | 0 ( 0%)  | 0 ( 0%)   |
| out_setup       | 18    | 18 (100%) | 0 ( 0%)  | 0 ( 0%)   |
| out_hold        | 18    | 0 ( 0%)   | 0 ( 0%)  | 18 (100%) |
| All Checks      | 72    | 45 ( 63%) | 0 ( 0%)  | 27 ( 38%) |

  
1
```

- Check timing

```
Information: Checking 'no_input_delay'.  
Information: Checking 'no_driving_cell'.  
Information: Checking 'unconstrained_endpoints'.  
Information: Checking 'unexpandable_clocks'.  
Failed clocks set      Related clocks          Original Period     Expanded Period    Added Edges      Voltage Config  
-----  
Information: Checking 'latch_fanout'.  
Information: Checking 'no_clock'.  
Information: Checking 'partial_input_delay'.  
Warning: There are 17 ports with partially defined input delays.  
Ports  
-----  
a[0]  
a[1]  
a[2]  
a[3]  
a[4]  
a[5]  
a[6]  
a[7]  
b[0]  
b[1]  
b[2]  
b[3]  
b[4]  
b[5]  
b[6]  
b[7]  
cin  
Information: Checking 'generic'.  
Information: Checking 'loops'.  
Information: Checking 'generated_clocks'.  
Information: Checking 'pulse_clock_non_pulse_clock_merge'.  
Information: Checking 'pll_configuration'.  
Information: Checking 'voltage_level'.  
Check cell voltage level related issues including rail voltages  
Cell Name           min/max   Issues found  
-----  
0
```

- Clock:

```
*****
Report : clock_skew
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 14:40:39 2024
*****
Object      Min Rise  Min Fall  Max Rise  Max Fall   Hold    Setup    Related
              Delay     Delay    Delay     Delay   Uncertainty  Uncertainty Clock
clk          0.00     0.00     0.00     0.00    -4.00      -4.20    --
*****
Report : clock
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 14:40:39 2024
*****
Attributes:
  p - Propagated clock
  G - Generated   clock
  I - Inactive    clock
Clock        Period      Waveform      Attrs      Sources
clk          1.00       {0 0.5}       {clk}
1
```

- Timing:

1. Global timing:

```
*****
Report : global_timing
-format { narrow }
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 14:40:38 2024
*****
No setup violations found.
No hold violations found.
1
```

2. Report timing:

```
*****
Report : timing
-path_type full
-delay_type min_max
-input_pins
-nets
-slack_lesser_than 0.00
-max_paths 1
-sort_by slack
Design : CLA1
Version: V-2023.12
Date  : Thu Jul 11 14:40:43 2024
*****
No constrained paths.
No paths with slack less than 0.00.
1
```

- Commands to open P1 reports

```
[wsl 7@wsl reports]$ cd check_timing/
[wsl 7@wsl check_timing]$ ls
check_timing.p1_report  check_timing.p2_report
[wsl 7@wsl check_timing]$ vi check_timing.p1_report
[wsl 7@wsl check_timing]$ cd ..
[wsl 7@wsl reports]$ cd clock/
[wsl 7@wsl clock]$ ls
report_clock.p1_report  report_clock.p2_report
[wsl 7@wsl clock]$ vi report_clock.p1_report
[wsl 7@wsl clock]$ cd timi
bash: cd: timi: No such file or directory
[wsl 7@wsl clock]$ cd ..
[wsl 7@wsl reports]$ cd timing/
[wsl 7@wsl timing]$ ls
report_global_timing.p1_report  report_global_timing.p2_report  report_timing.p1_report  report_timing.p2_report
[wsl 7@wsl timing]$ vi report_global_timing.p1_report
[wsl 7@wsl timing]$ vi report_timing.p1_report
```

P2:

- Analysis coverage:

```
*****  
Report : analysis_coverage  
Design : CLA1  
Version: V-2023.12  
Date  : Thu Jul 11 14:52:54 2024  
*****  


| Type of Check   | Total | Met       | Violated | Untested  |
|-----------------|-------|-----------|----------|-----------|
| setup           | 9     | 9 (100%)  | 0 ( 0%)  | 0 ( 0%)   |
| hold            | 9     | 0 ( 0%)   | 0 ( 0%)  | 9 (100%)  |
| min_pulse_width | 18    | 18 (100%) | 0 ( 0%)  | 0 ( 0%)   |
| out_setup       | 18    | 18 (100%) | 0 ( 0%)  | 0 ( 0%)   |
| out_hold        | 18    | 0 ( 0%)   | 0 ( 0%)  | 18 (100%) |
| All Checks      | 72    | 45 ( 63%) | 0 ( 0%)  | 27 ( 38%) |

  
1
```

- Check timing

```
Information: Checking 'no_input_delay'.  
Information: Checking 'no_driving_cell'.  
Information: Checking 'unconstrained_endpoints'.  
Information: Checking 'unexpandable_clocks'.  
Failed clocks set      Related clocks          Original Period     Expanded Period    Added Edges    Voltage Config  
-----  
Information: Checking 'latch_fanout'.  
Information: Checking 'no_clock'.  
Information: Checking 'partial_input_delay'.  
Warning: There are 17 ports with partially defined input delays.  
Ports  
-----  
a[0]  
a[1]  
a[2]  
a[3]  
a[4]  
a[5]  
a[6]  
a[7]  
b[0]  
b[1]  
b[2]  
b[3]  
b[4]  
b[5]  
b[6]  
b[7]  
cin  
Information: Checking 'generic'.  
Information: Checking 'loops'.  
Information: Checking 'generated_clocks'.  
Information: Checking 'pulse_clock_non_pulse_clock_merge'.  
Information: Checking 'pll_configuration'.  
Information: Checking 'voltage_level'.  
Check cell voltage level related issues including rail voltages  
Cell Name           min/max   Issues found  
-----  
0
```

- Clock:

```
*****
Report : clock_skew
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 14:52:54 2024
*****
Object      Min Rise  Min Fall  Max Rise  Max Fall  Hold      Setup      Related
              Delay     Delay    Delay     Delay   Uncertainty  Uncertainty Clock
clk          0.000000 0.000000 0.000000 0.000000 -4.000000 -4.200000  --
*****
Report : clock
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 14:52:54 2024
*****
Attributes:
  p - Propagated clock
  G - Generated clock
  I - Inactive clock
Clock        Period      Waveform      Attrs      Sources
clk          1.000000 {0.000000 0.500000} {clk}
1
-
```

- Timing:

1.Global timing:

```
*****
Report : global_timing
-format { narrow }
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 14:52:53 2024
*****
No setup violations found.
No hold violations found.
1
-
```

2.Report timing:

```
*****
Report : timing
-path_type full
-delay_type min_max
-input_pins
-mets
-slack_lesser_than 0.000000
-max_paths 1
-sort_by slack
Design : CLAI
Version: V-2023.12
Date   : Thu Jul 11 14:52:54 2024
*****
No constrained paths.
No paths with slack less than 0.000000.
1
-
```

- Commands to open P1 reports

```
[wsl1_7@wsl1 reports]$ cd analysis/coverage/
[wsl1_7@wsl1 analysis/coverage]$ vi report_analysis_coverage.p2_report
[wsl1_7@wsl1 analysis/coverage]$ cd ..
[wsl1_7@wsl1 reports]$ cd check_timing/
[wsl1_7@wsl1 check_timing]$ ls
check_timing.p1_report check_timing.p2_report
[wsl1_7@wsl1 check_timing]$ vi check_timing.p2_report
[wsl1_7@wsl1 check_timing]$ cd ..
[wsl1_7@wsl1 reports]$ cd clock/
[wsl1_7@wsl1 clock]$ ls
report_clock.p1_report report_clock.p2_report
[wsl1_7@wsl1 clock]$ vi report_clock.p2_report
[wsl1_7@wsl1 reports]$ cd timing/
[wsl1_7@wsl1 timing]$ ls
report_global_timing.p1_report report_global_timing.p2_report report_timing.p1_report report_timing.p2_report
[wsl1_7@wsl1 timing]$ vi report_global_timing.p2_report
[wsl1_7@wsl1 timing]$ vi report_timing.p2_report
[wsl1_7@wsl1 timing]$
```

9.GDSII:

A binary file format used to describe the physical layout of an integrated circuit is primarily used for transferring IC layout data between design tools and the fabrication process.

- Open the ICCII directory
- Invoke icc2_shell
- Open the library and block
- The command used for ‘gdsii’ is

```
icc2_shell> open block eight_bit_adder_placement1
Information: User units loaded from library 'saed32rvt_c' (LNK-040)
Opening block 'EIGHT_BIT_ADDER_LIB1:eight_bit_adder_placement1.design' in edit mode
(EIGHT_BIT_ADDER_LIB1:eight_bit_adder_placement1.design)
icc2_shell> export gdsii1
Using libraries: EIGHT_BIT_ADDER_LIB1 saed32rvt_c
Visiting block EIGHT_BIT_ADDER_LIB1:eight_bit_adder_placement1.design
Design 'CLAI' was successfully linked.
Encrypting...
1
```

- From there we exported the ‘gdsii’ and it has been saved in ICCII directory
- Now the commands used to see ‘gdsii’

```
997  icc2_shell
998  cd SRM_Workshop/
999  cd ICCII/
1000 cd
1001 cd Desktop/
1002 cd SRM_Workshop/
1003 cd ICCII/
1004 ls
1005 vi gdsiil.gz
1006 history
[wsl_7@wsl ICCII]$
```

- The output of gdsii is

```
0Ii2ã³*òÿ^@Ã<89>"Ã^Ht^S^T<99>rÿB}ó}6BT<90>^?ÃÇW<98>8çñÃni¶óç"ñ Þ<86>?hiM0<9b>N«í<9c>IÑ~òé<9f>Ó$e^B<9c>fù<84>I<88>>}^R<8c>[#Ñ<97>t^]J^D"<8c>q<87>¬Ãÿ?L,W ^mw6^Ní¥^P`.^K>Ã ¥jo^0Óomb<8f>Û<Ñ8q<92>^ÖL<91>±^V»^Lk<84>w^<94>MxÃk^^<82>çx^C½idEò©^N^
[lr^H^a[<87>^?2rPây:ç@Ãé¥^P<9d>èÆ={%- *RÈçê^TéÃ s<8a><84>¹Ct»Î|Iða
~
```

GDSII is successfully generated in ICCII.