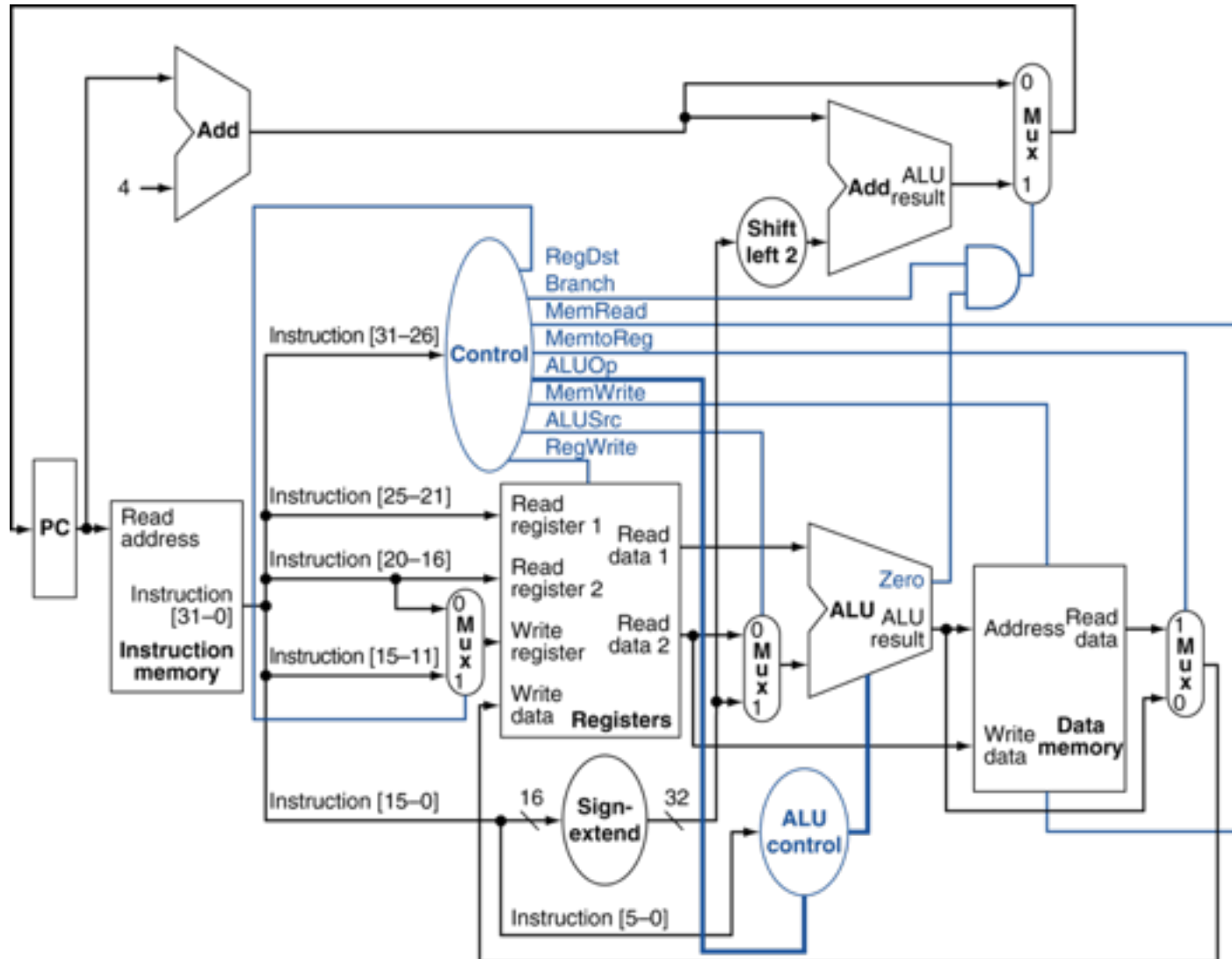


Topic 15

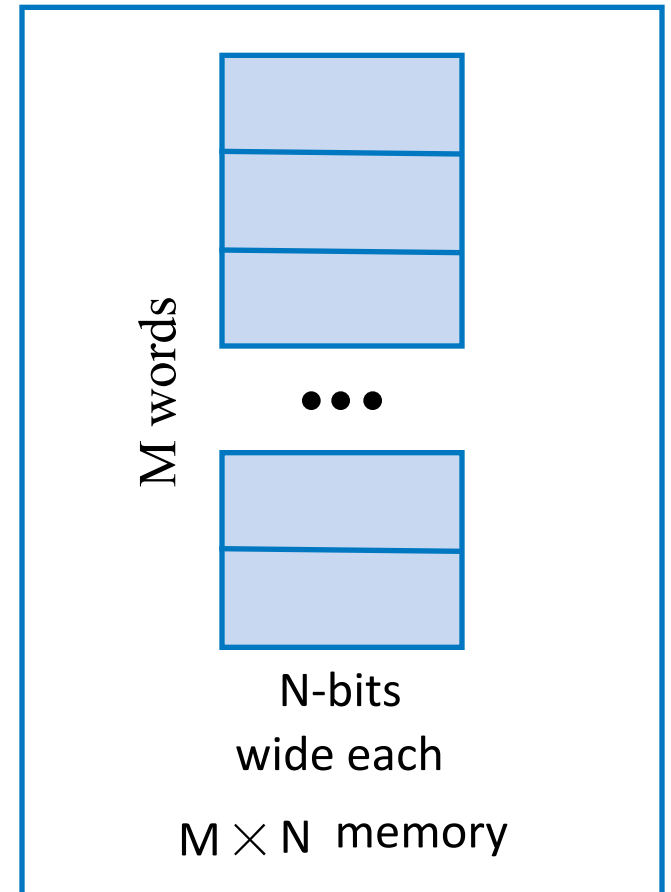
Memory

Big Picture - Single Cycle Computer



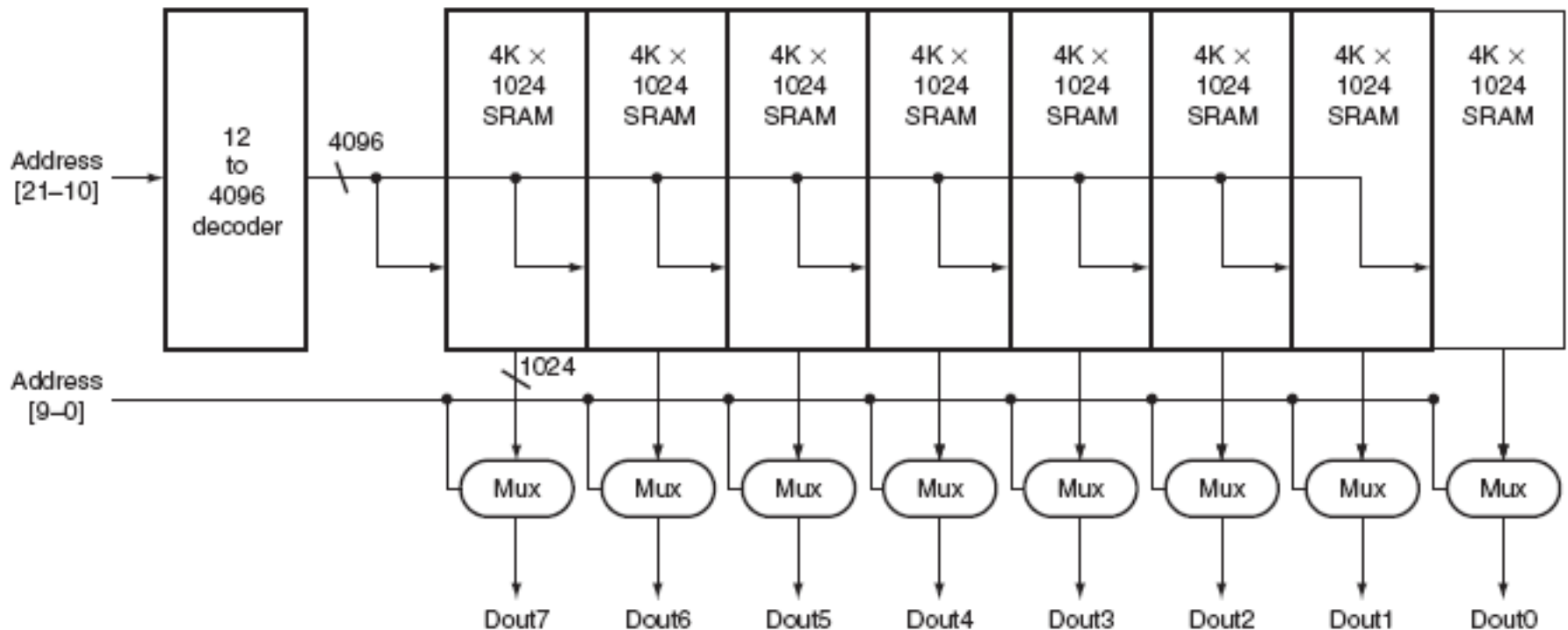
Memory Components

- ***MxN memory***
 - M words (row)
 - N bits (column) wide each
- Types of memory
 - RAM
 - ROM



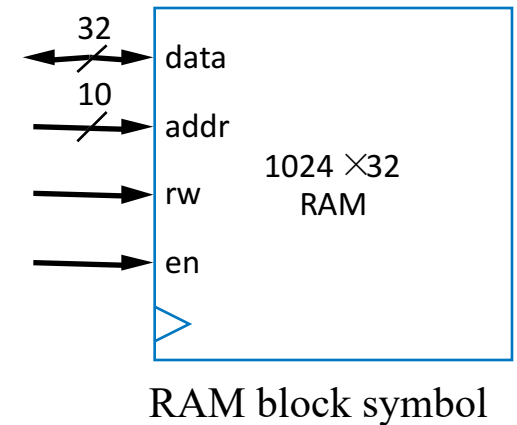
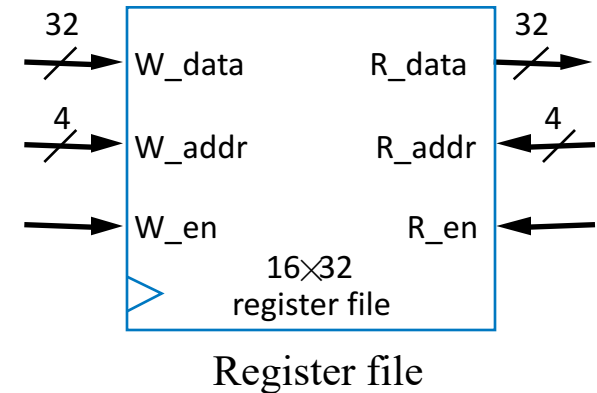
Two-Level Memory Addressing

- Typical memory organization

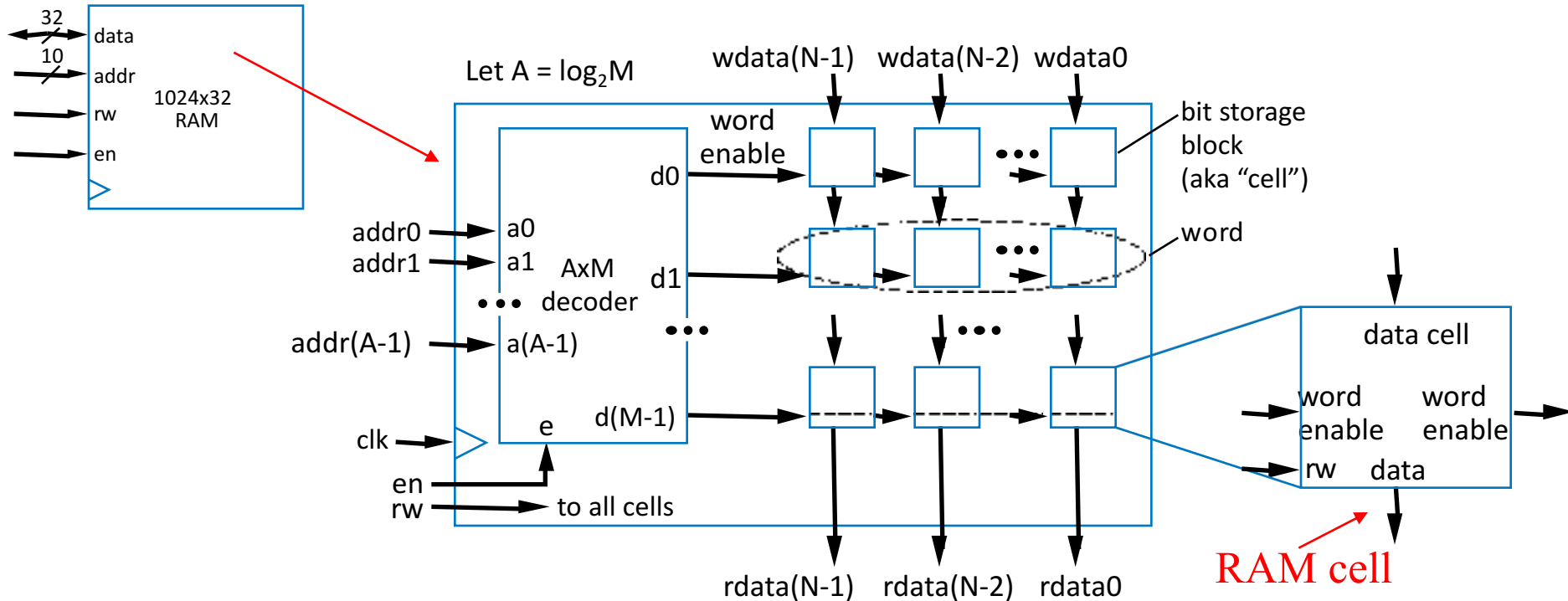


Random Access Memory (RAM)

- RAM – readable and writable memory
 - Traditionally: “random access memory”
 - Logically same as register file
 - Memory with address inputs, data inputs/outputs, and control
 - RAM vs. register file
 - RAM is typically larger
 - RAM typically stores bits more efficiently than flip flops
 - RAM typically implemented on a chip in a square rather than rectangular shape – keeps longest wires (hence delay) short

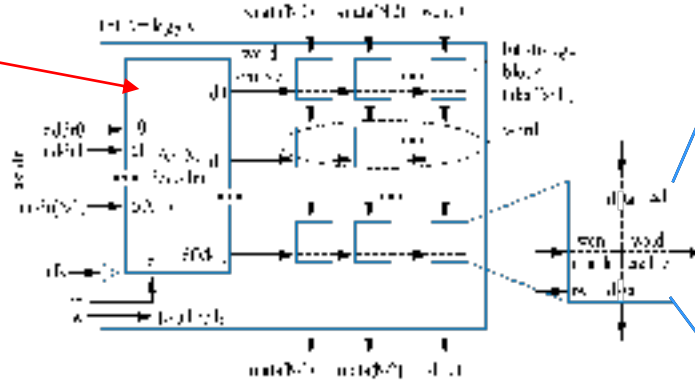
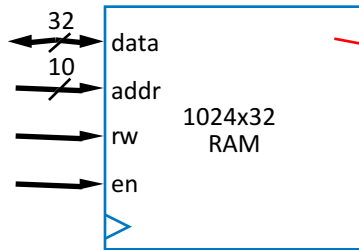


RAM Internal Structure

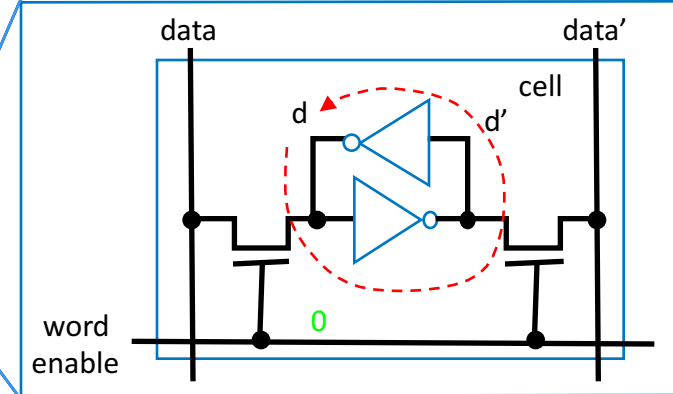


- Similar internal structure as register file
 - Decoder enables appropriate word based on address inputs
 - rw controls whether cell is written or read

Static RAM (SRAM)

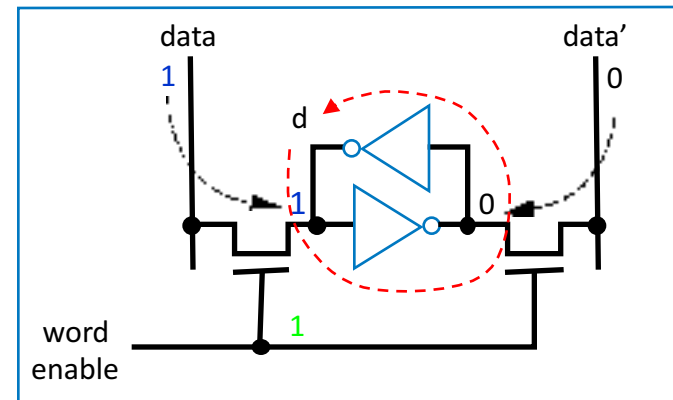


SRAM cell



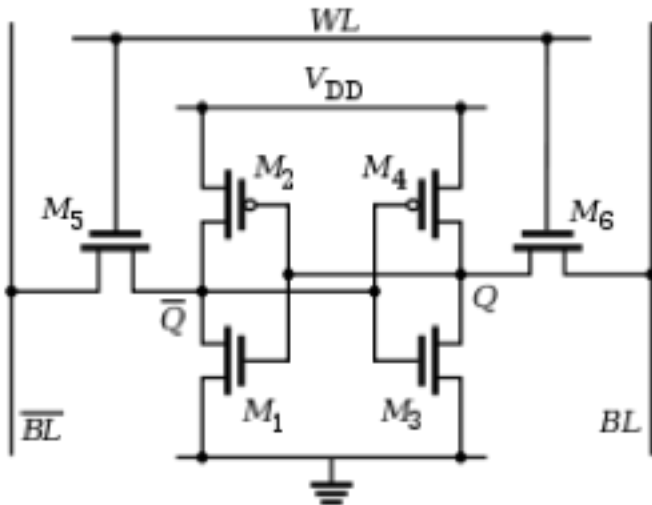
- “Static” RAM cell
 - 6 transistors (recall inverter is 2 transistors)
 - Writing this cell
 - *word enable* input comes from decoder
 - When 0, value *d* loops around inverters
 - That loop is where a bit stays stored
 - When 1, the *data* bit value enters the loop
 - *data* is the bit to be stored in this cell
 - *data'* enters on other side
 - Example shows a “1” being written into cell

SRAM cell

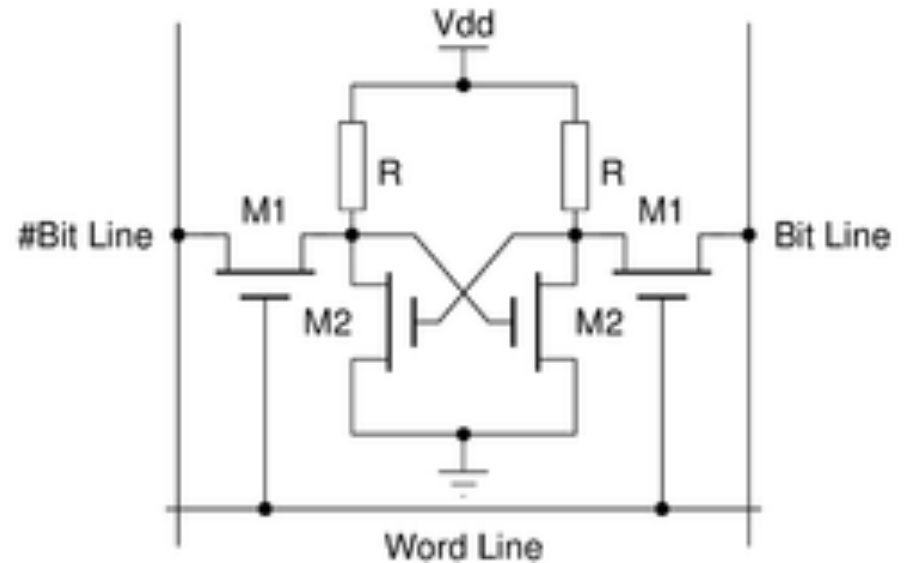


Static RAM (SRAM)

Implementation with 6 transistors

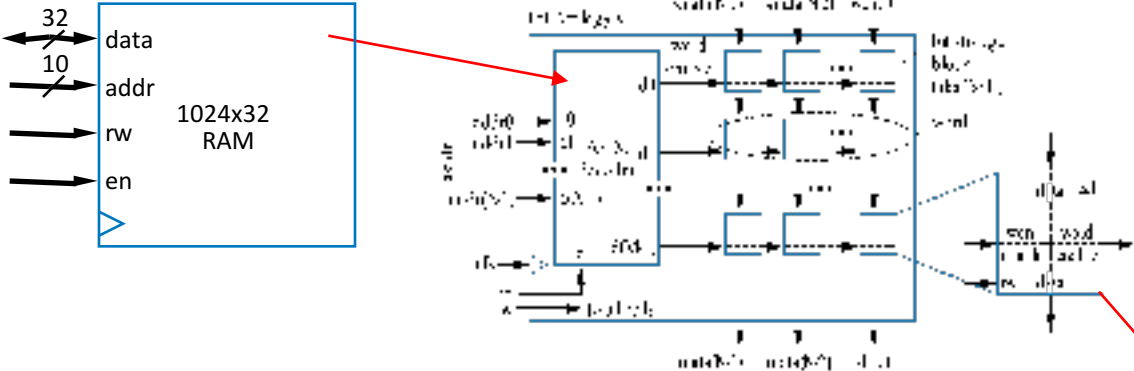


Implementation with 4 transistors

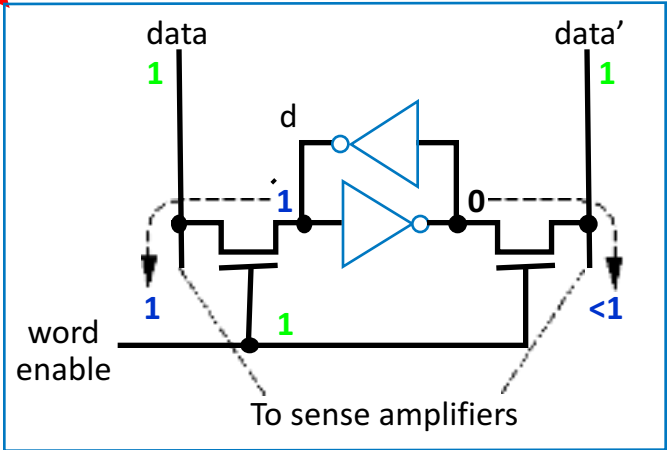


Source: wikipedia

Static RAM (SRAM)

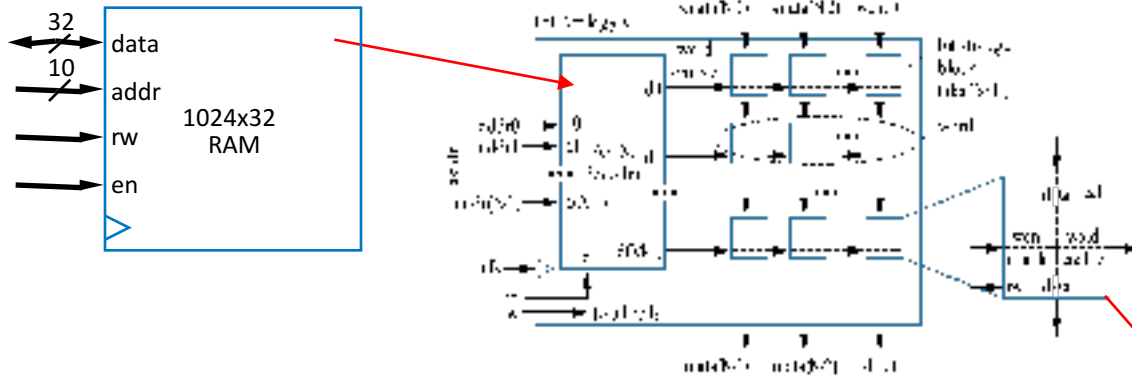


SRAM cell



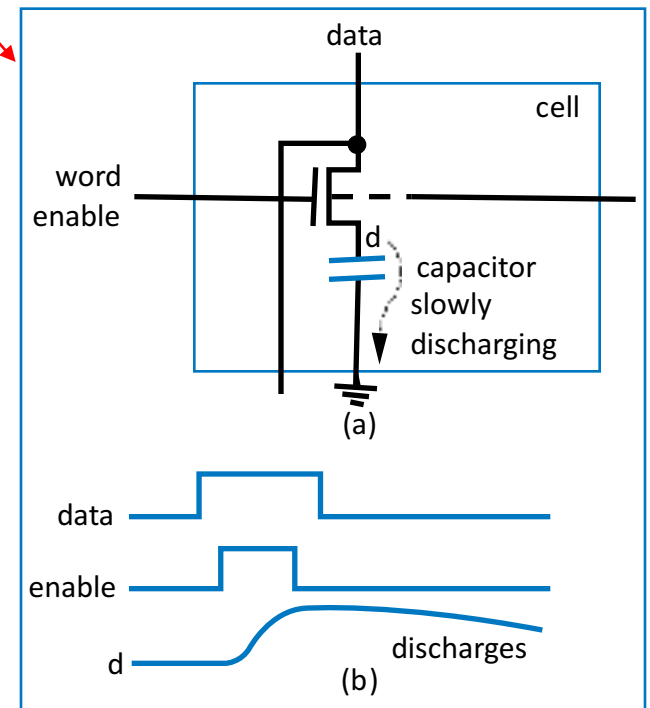
- “Static” RAM cell
 - Reading this cell
 - Somewhat trickier
 - When *rw* set to read, the RAM logic sets both *data* and *data'* to 1
 - The stored bit *d* will pull either the left line or the right line down slightly below 1
 - “Sense amplifiers” detect which side is slightly pulled down

Dynamic RAM (DRAM)



DRAM cell

- “Dynamic” RAM cell
 - 1 transistor (rather than 6)
 - Relies on large capacitor to store bit
 - Write: Transistor conducts, data voltage level gets stored on top plate of capacitor
 - Read: sense amplifier on the data line
 - Problem: Capacitor discharges over time
 - Must “refresh” regularly, by reading d and then writing it right back

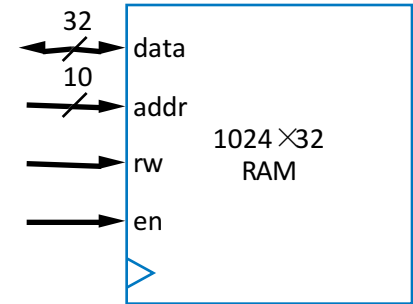


Comparing Memory Types

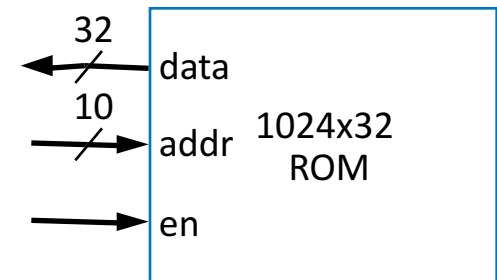
- Register file
 - Fastest
 - But small capacity and biggest size
- SRAM
 - Fast
 - More compact than register file
- DRAM
 - Slowest
 - And refreshing takes time
 - But very compact
- Use register file for small items, SRAM for large items, and DRAM for huge items
 - Note: DRAM's big capacitor requires a special chip design process, so DRAM is often a separate chip

Read-Only Memory – ROM

- Memory that can only be read from, not written to
 - Data lines are output only
 - No need for *rw* input
- Advantages over RAM
 - Compact: May be smaller
 - **Nonvolatile**: Saves bits even if power supply is turned off
 - Faster Speed: especially than DRAM
 - Low power: Doesn't need power supply to save bits, so can extend battery life
- Choose ROM over RAM if stored data won't change (or won't change often)

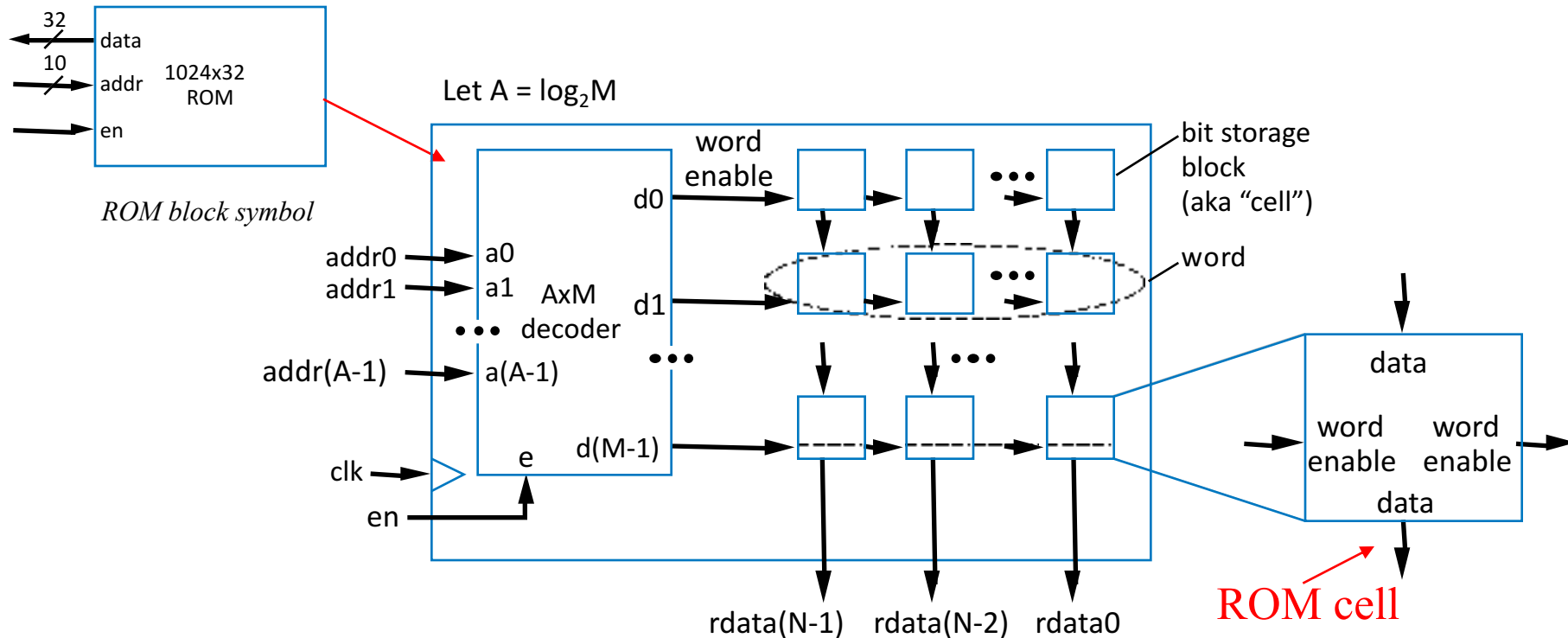


RAM block symbol



ROM block symbol

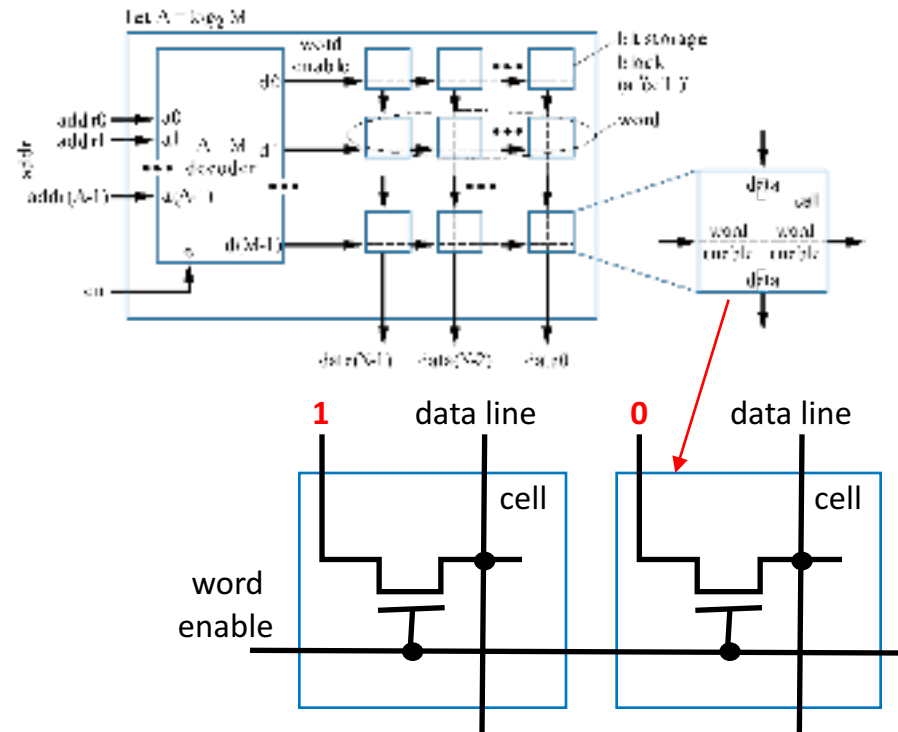
Read-Only Memory – ROM



- Internal logical structure similar to RAM, without the data input lines

ROM Types

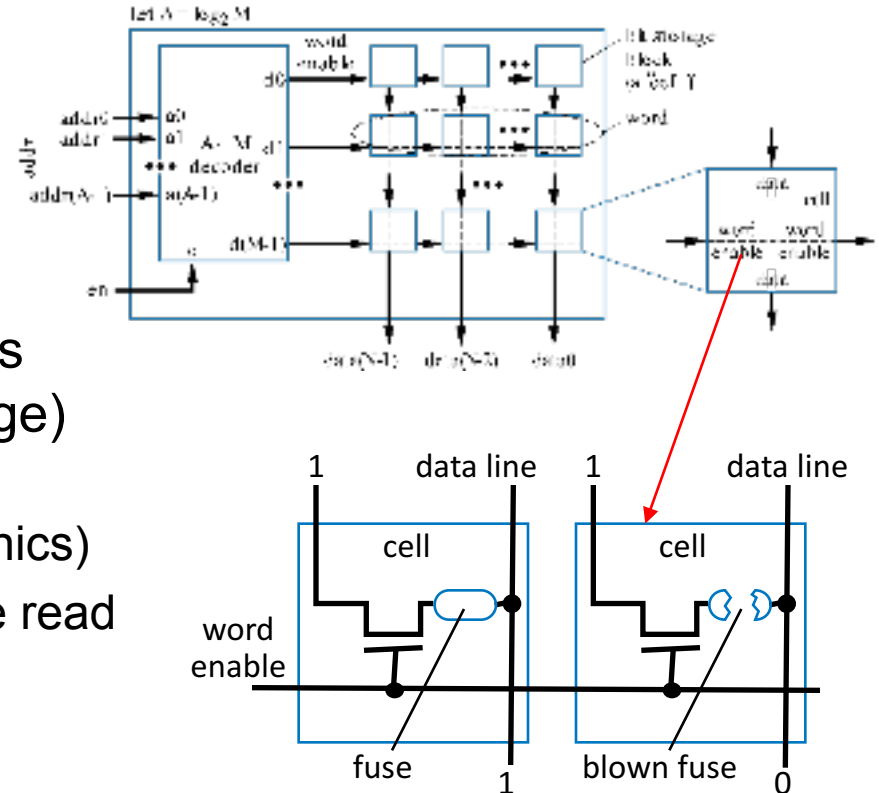
- How are bits stored in ROM?
 - Storing bits in a ROM known as *programming*
 - Several methods



ROM Types

- **Fuse-Based Programmable ROM**

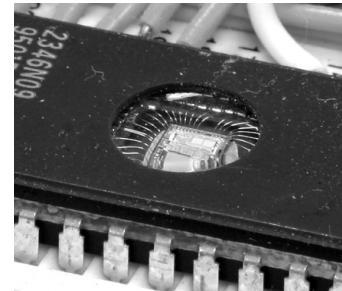
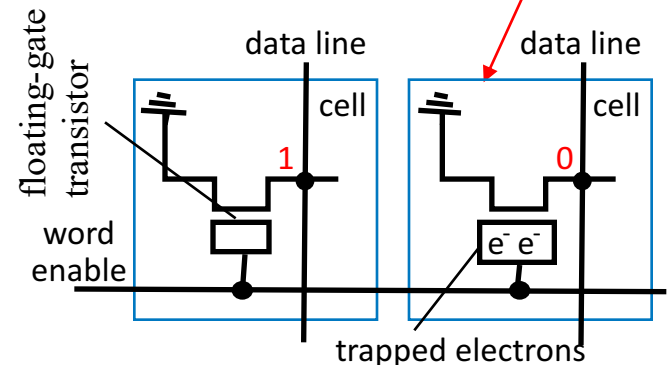
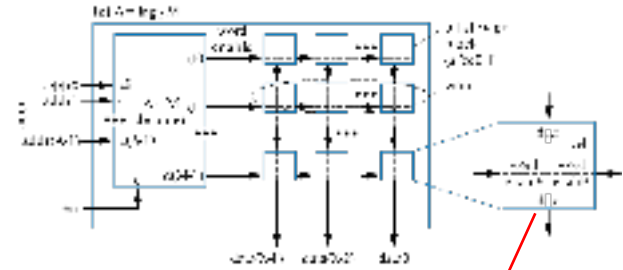
- Each cell has a fuse
- A special device, known as a programmer, blows certain fuses (using higher-than-normal voltage)
 - Those cells will be read as 0s (involving some special electronics)
 - Cells with unblown fuses will be read as 1s
 - 2-bit word on right stores “10”
- Also known as **One-Time Programmable (OTP) ROM**



ROM Types

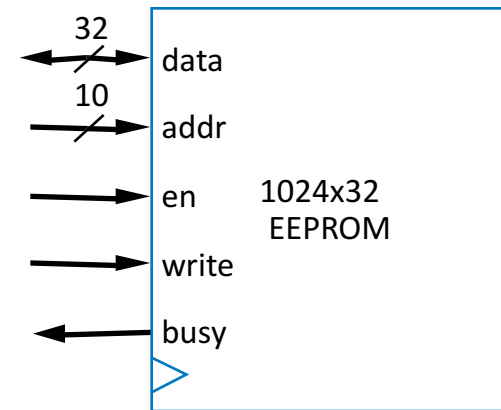
- **Erasable Programmable ROM (EPROM)**

- Uses “**floating-gate transistor**” in each cell
- Special programmer device uses higher-than-normal voltage to cause electrons to *tunnel* into the gate
 - Electrons become trapped in the gate
 - Only done for cells that should store 0
 - Other cells (without electrons trapped in gate) will be 1
- To erase, shed ultraviolet light onto chip
 - Gives trapped electrons energy to escape
 - Requires chip package to have window



ROM Types

- **Electronically-Erasable Programmable ROM (EEPROM)**
 - Similar to EPROM
 - But erasing done *electronically*, not using UV light
- **Flash memory**
 - Like EEPROM, but all words (or large blocks of words) can be erased *simultaneously*
 - Become common in late 1990s
- Both types are in-system programmable
 - Can be programmed with new stored bits while in the system in which the ROM operates
 - Requires bi-directional data lines, and write control input
 - Also need **busy** output to indicate that erasing is in progress – erasing takes some time



Blurring of Distinction Between ROM and RAM

- Traditionally
 - RAM is readable and writable
 - ROM is read-only
- But some ROMs act almost like RAMs
 - EEPROM and Flash are in-system programmable
- And, some RAMs act almost like ROMs
 - Non-Volatile RAMs: Can save their data without the power supply
 - E.g.: Built-in battery, may work for up to 10 years
 - Another e.g.: Includes ROM backup for RAM – controller writes RAM contents to ROM before turning off
 - e.g., Magnetoresistive RAM
- Bottom line
 - Lot of choices available to designer, must find best fit with design goals

