**Ve270 Introduction to Logic Design Homework 4**

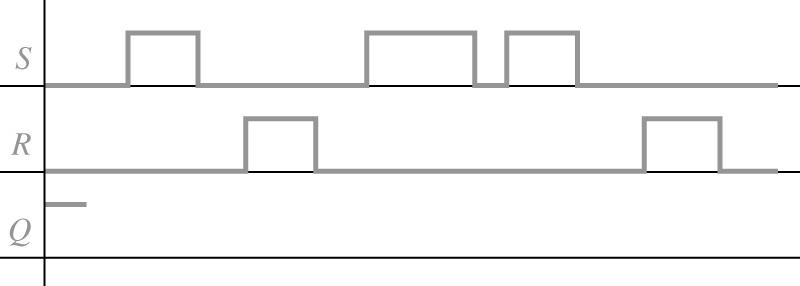
**Assigned: October 11, 2018**

**Due: October 18, 2018, 4:00pm.**

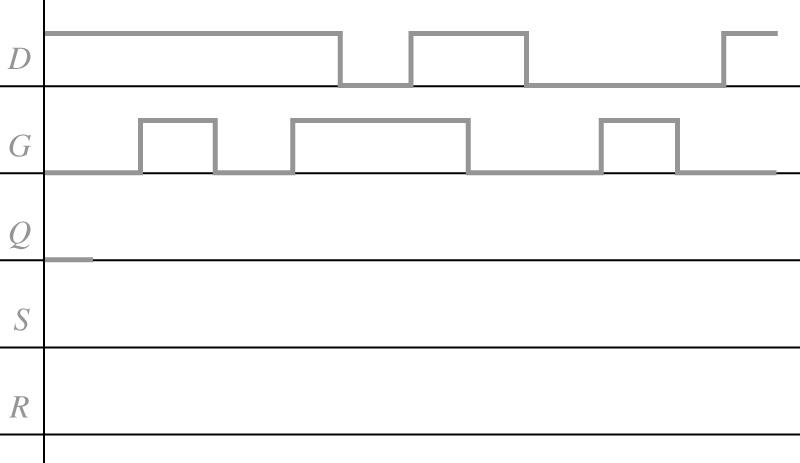
**The homework should be submitted in hard copies.**

***Note****: you may ignore the gate delay when drawing a timing diagram unless required differently.*

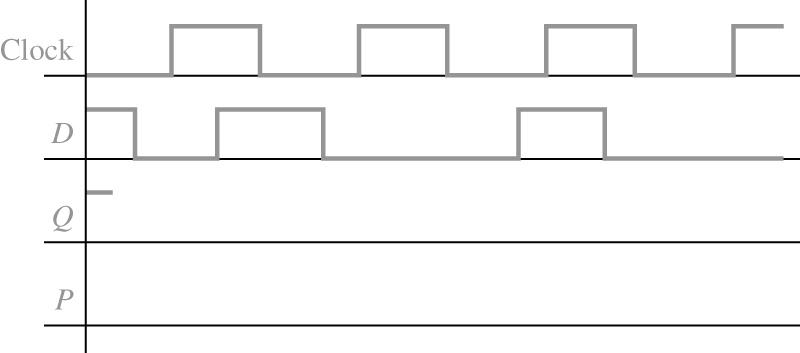
1. (10 points) Complete the following timing diagram for an SR latch. Assume Q begins at 1.



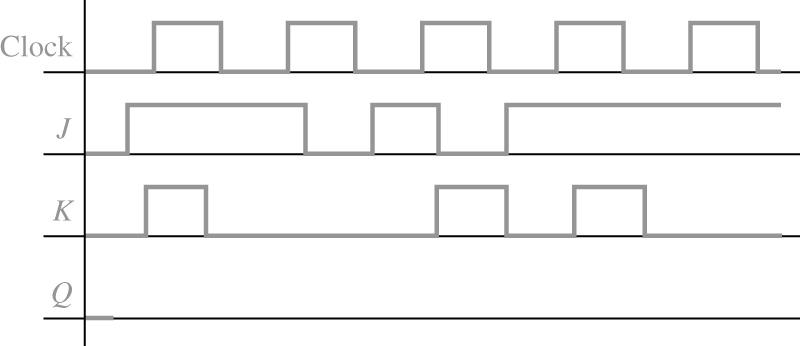
1. (10 points) Complete the following timing diagrams for a gated D latch. Assume Q begins at 0.



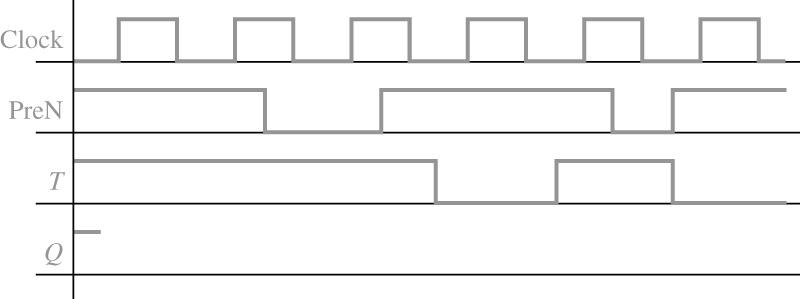
1. (10 points) Complete the following diagrams for the rising-edge triggered D flip-flop. Assume Q begins at 1.



1. (10 points) Fill in the timing diagram below for a falling-edge triggered J-K flip-flop. Assume Q begins at 0.



1. (15 points) Fill in the following timing diagram for a rising-edge triggered T flip-flop with an asynchronous active-low preset input (PreN, equivalent to set). Assume Q begins at 1.





1. (15 points) Design a 4-bit register with an enable signal “EN”, such that when EN = 0, nothing can be loaded into the register, and when EN = 1, the register works as normal.
2. (15 points) Problem 3.19. Draw schematic.
3. (15 points) Problem 3.20.

