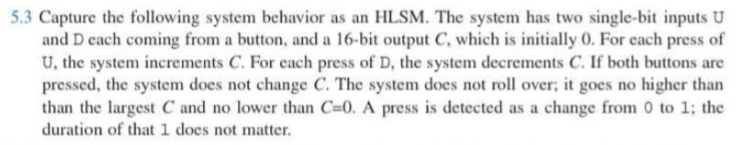
**Ve270 Introduction to Logic Design Homework 9**

**Assigned: November 22, 2018**

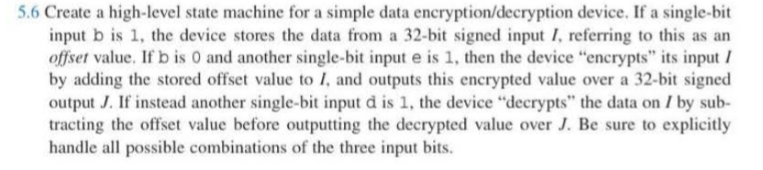
**Due: November 29, 2018, 4:00pm.**

**The homework should be submitted in hard copies.**

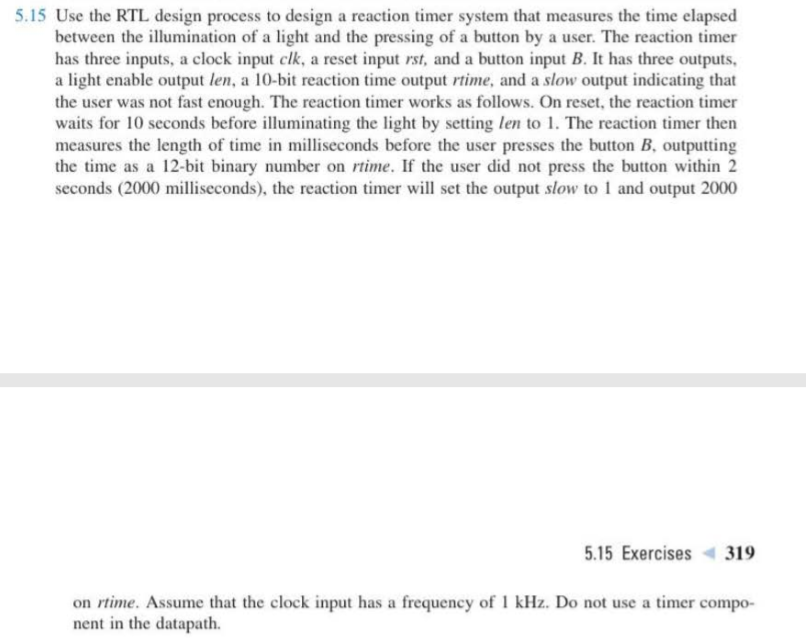
1. Problem 5.3 (15 points)



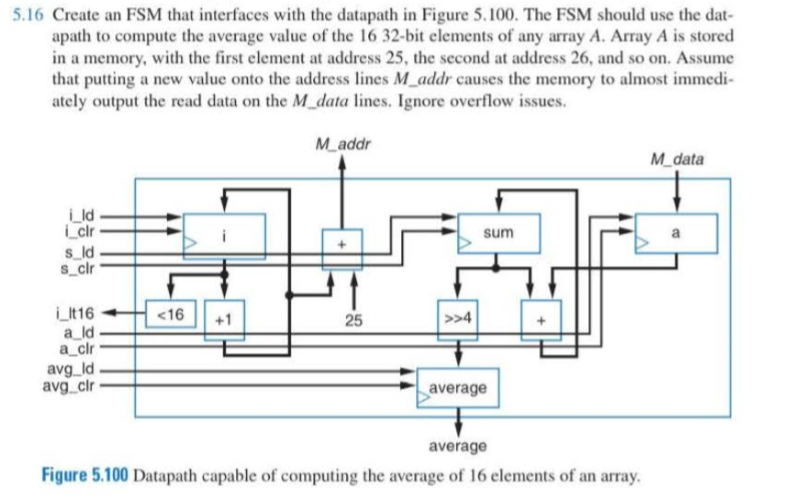
1. Problem 5.6 (15 points)



1. Problem 5.15. (20 points)



1. Problem 5.16 (25 points)



1. Design a circuit called ***Receiver*** that receives two single bit signals, **Valid** and **Data\_in**, from another device called ***Transmitter***. The **Valid** signal sent from the ***Transmitter*** will be a 1-clock cycle pulse. After the ***Receiver*** receives the **Valid** pulse, it will start receiving 8 bits through port **Data\_in**, bit by bit. After the 8 bits of data is received, they should be copied into an 8-bit register called **RxReg**. (25 points)