[Total No. of Questions - 9] [Total No. of Printed Pages - 2]

Dec-24-0095 (CBCS/NEP)

EEEPC-312 (Digital System Design)

(Common ECEPC-312)

B.Tech. 3rd

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, selecting one question each from section A, B, C & D. Section E is Compulsory.

SECTION - A

1. How can we minimize Boolean expression of the below function?
   F=XY+X(Y+Z)+Y(Y+Z). (10)

2. Minimize the following logic function using K-maps and realize using NAND and NOR gates.
   $F(A, B, C, D) = \Sigma m (1,3,5,8,9,11,15) + d (2,13)$. (10)

SECTION - B

3. Implement the following Boolean function $F=\Sigma m (0,3,5,8,9,10,12,14)$. Using 8:1 Multiplexer. (10)

4. Draw the circuit of TTL NAND gate and explain its operation. Compare the TTL and ECL logic families. (10)

SECTION - C

5. Explain working of Master slave JK Flip-Flop along with waveforms. Explain race around condition. How is it eliminated? (10)

6. How does a ripple counter differ from a synchronous counter? Explain with suitable example. (10)

SECTION - D

7. Apply structural modeling in Verilog HDL to describe 3 to 8 decoder in detail. (10)

8. Explain, in detail, different modeling styles of VHDL with suitable examples. (10)

SECTION - E (Compulsory)

9. (a) Convert $(125)_{10}$ into hexadecimal numbers.
   (b) What is shift register?
   (c) How can a DEMUX be used as a decoder?
   (d) State De-Morgan's theorem and mention its use.
   (e) What is finite state Machine?
   (f) Define Structural model.
   (g) Compare VHDL with Verilog.
   (h) Define positive logic and negative logic system.
   (i) Prove that Y+XY = Y.
   (j) What is Volatile and Non-Volatile memory? (10×2=20)