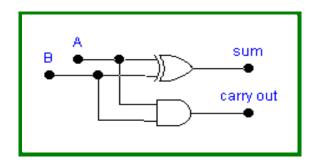
USE THE LAB INSTRUCTIONS -CONNECTING LOGIC GATE CIRCUITS TO COMPLETE THIS LAB.

VERY IMPORTANT: DISCONNECT THE POWER SUPPLY FROM YOUR CIRCUIT WHEN WIRING YOUR CIRCUITS.

Purpose: To study the operation of various logic gates.

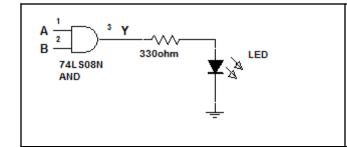
Name:



Part A - Basic Gates

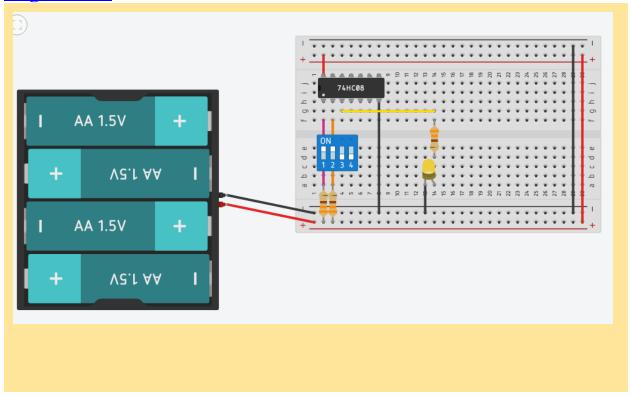
• Wire each of the following circuits in your breadboard. Complete the truth table for each circuit.

1. AND Gate

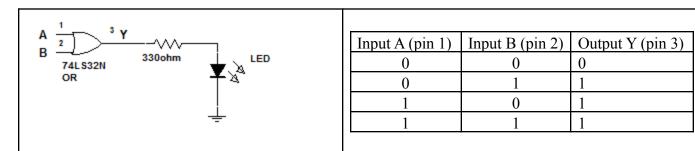


| Input A (pin 1) | Input B (pin 2) | Output Y (pin 3) |
|-----------------|-----------------|------------------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

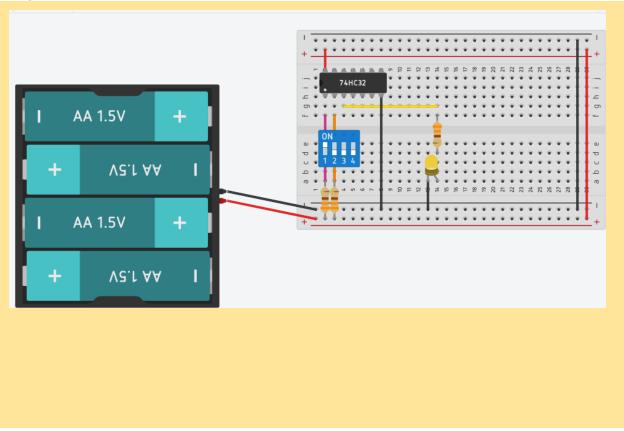
Name:



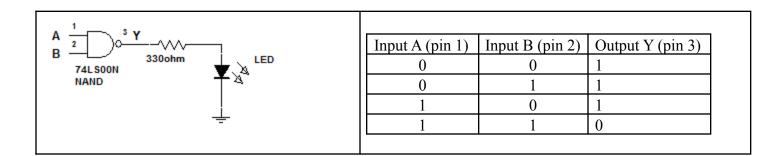
2. OR Gate



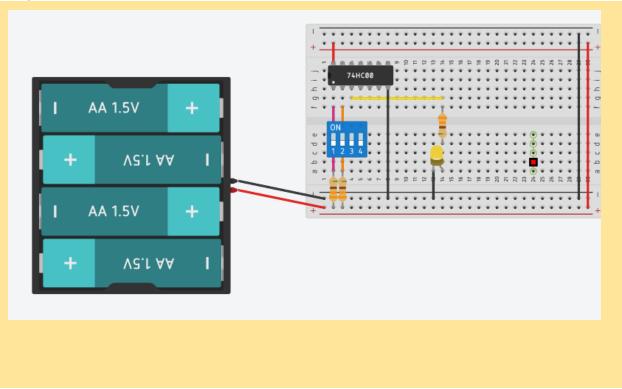




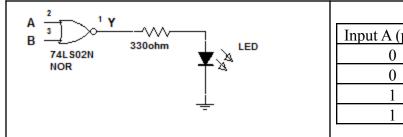
3. NAND Gate





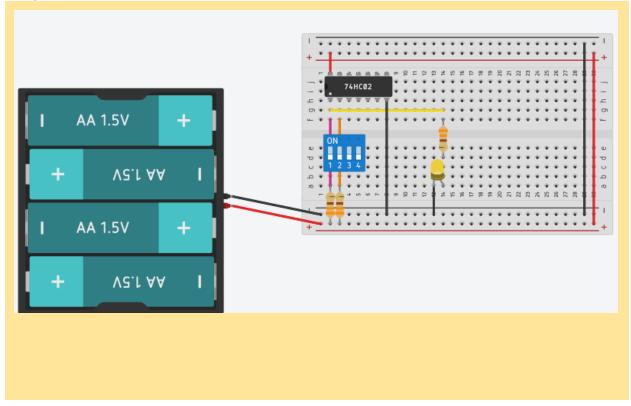


4. NOR Gate

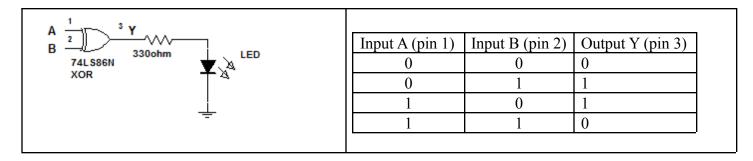


| Input A (pin 2) | Input B (pin 3) | Output Y (pin 1) |
|-----------------|-----------------|------------------|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

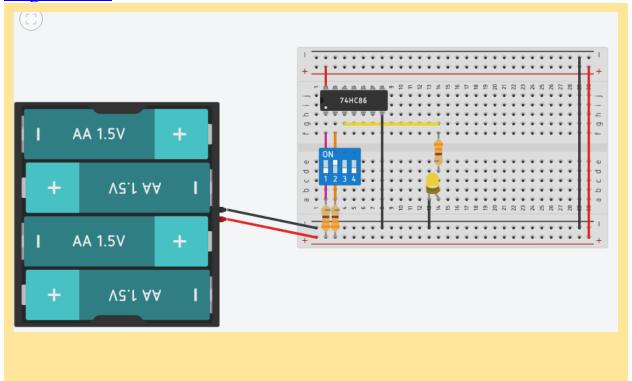




5. Exclusive OR (XOR) Gate



Name:



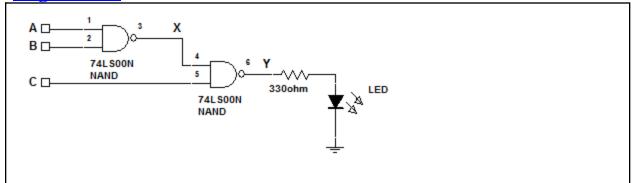
Part B - Combining Logic Gates

Purpose: To investigate two gates of a 74LS00 (NAND) chip to create a three input OR gate.

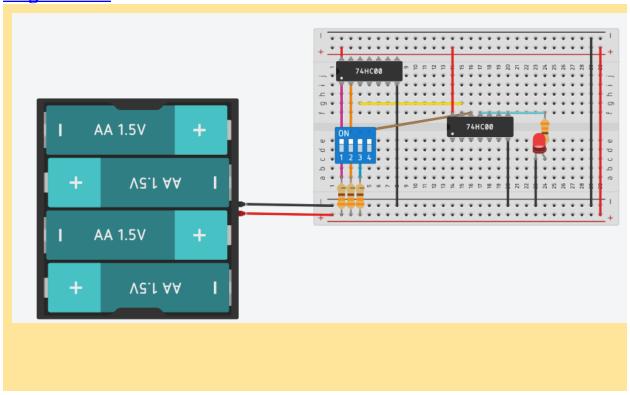
- Wire each of the following circuits in your breadboard. Complete the truth table for each circuit.
- Note that the output of one gate in one chip goes into the input of a second gate in the same chip.

1. Combining two NAND gates.

Name:

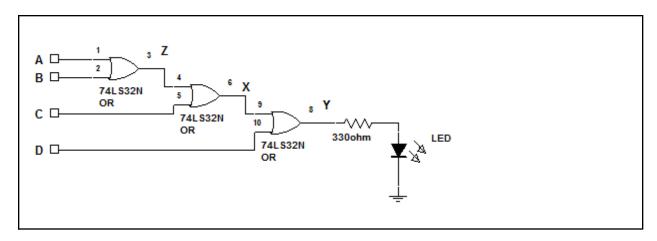


| В | A | A•B | $\overline{\mathbf{A} \bullet \mathbf{B}} = \mathbf{X}$ | C | C•X | <u>C•X</u> =Y |
|---|---|-----|---|---|-----|---------------|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |



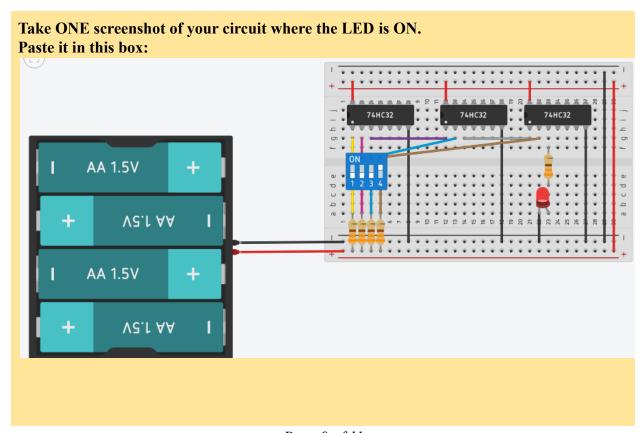
Name:

2. Combining three OR gates.



| 1 | N | _ | n | ۵. |
|---|----|---|----|----|
| | IN | а | rr | ıe |

| D | C | В | A | A+B=Z | Z+C=X | D+X=Y |
|---|---|---|---|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |



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Questions:

- 1. Given your knowledge of **AND** gates,
 - a. What would be the output of a three input AND gate circuit if the inputs were low, high, low (0 1 0)?

The output would be 0 or Low.

- b. What three inputs would produce a high output?

 The three input that would produce a high output are (1, 1, 1),
- 2. Given what you know about **NAND** gates, create the truth table of a **three** input NAND gate.

| Input A | Input B | Input C | Output X |
|---------|---------|---------|----------|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |

3. Given your knowledge of **XOR** gates, create the truth table of a **three** input XOR gate.

Name:

| Input A | Input B | Input C | Output X |
|---------|---------|---------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

| 4. | Complete | the senter | nce with the | correct gate: |
|-----|----------|--------------|-----------------|---------------|
| • • | Compiete | tile belitel | 100 111011 0110 | confect gate. |

Circuit 2 in part B above, is a four input _____OR____ (AND, OR, NAND, NOR, XOR) gate.