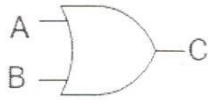
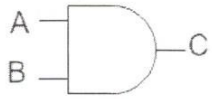
# Logic Gates Worksheet

0 = _____ 1 = _____



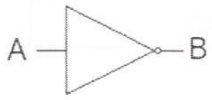

OR Gate

| A (input 1) | B (input 2) | C (Output) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



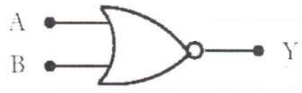

AND Gate

| A (input 1) | B (input 2) | C (Output) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |




NOT Gate

| A (input) | B (output) |
|---|---|
| 0 | 1 |
| 1 | 0 |



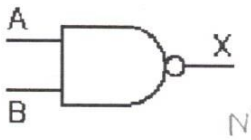

NOR Gate

| A (input 1) | B (input 2) | Y (Output) |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

# Logic Gates Worksheet


XOR Gate

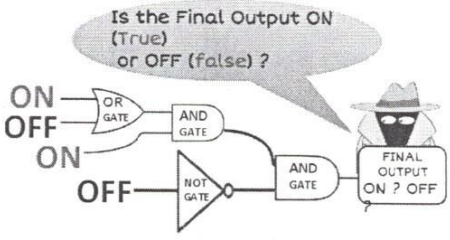
| A (input 1) | B (input 2) | Y (Output) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




NAND Gate

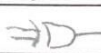
| A (input 1) | B (input 2) | Y (Output) |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

## Practice (show your work along the way)




**Output:** _____

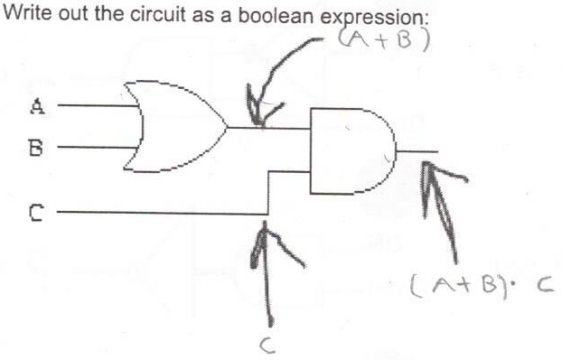
**Boolean Expressions**

| Gate | Symbol | Operator |
|---|---|---|
| And |  | • |
| OR |  | + |
| NOT |  | – NOT $Y=\overline{A}$ |
| NAND |  | $\overline{\cdot}$ |
| NOR |  | $\overline{+}$ |
| XOR |  | ⊕ |

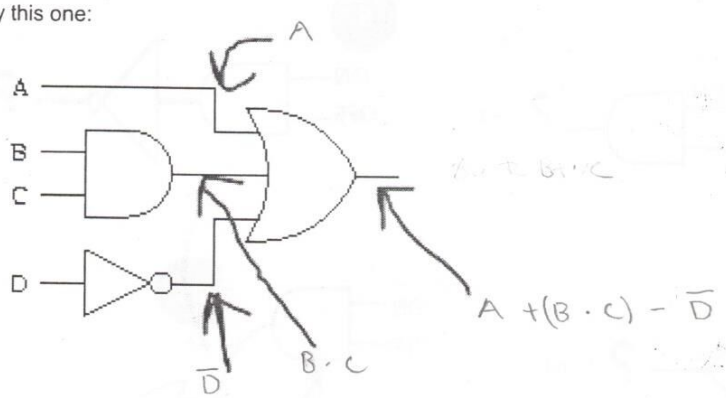
# Logic Gates Worksheet

**Class Example:**

Write out the circuit as a boolean expression:



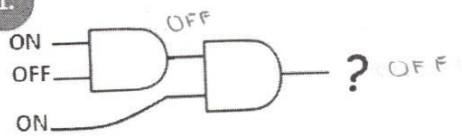

Try this one:



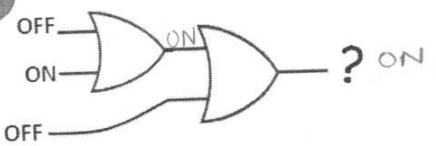
## Logic Gate Worksheet - TEJ3M

Name:

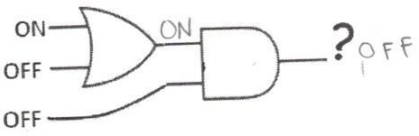
1.



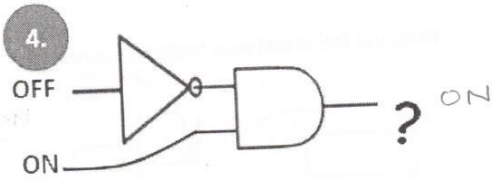

2.



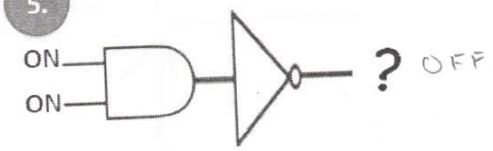

3.



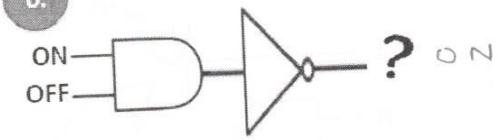

4.




5.

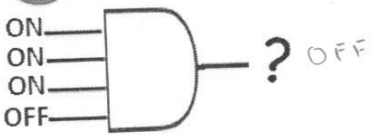



6.

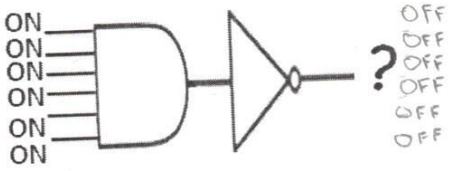



7.

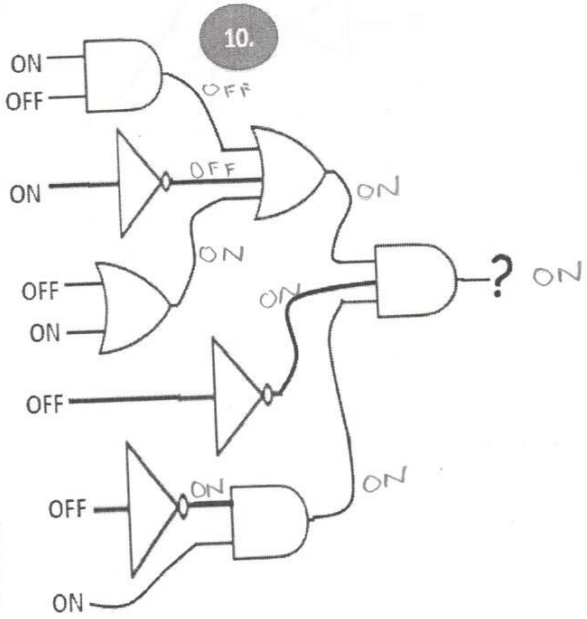

8.



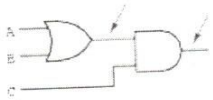

9.



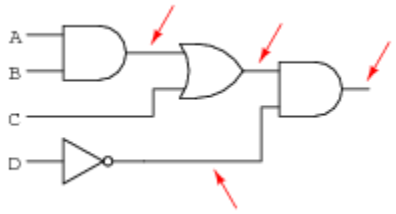

10.




11. Convert the following logic gate circuit into a Boolean equation, writing Boolean sub-expressions next to each gate output in the diagram:

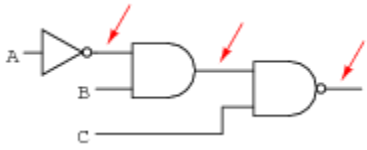


12. Convert the following logic gate circuit into a Boolean equation, writing Boolean sub-expressions next to each gate output in the diagram:




(AB + C) D’

13. Convert the following logic gate circuit into a Boolean equation, writing Boolean sub-expressions next to each gate output in the diagram:

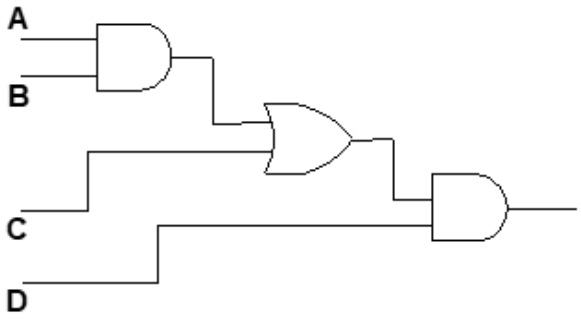



((A’B) C)’

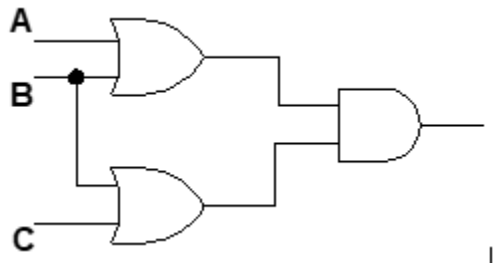
14. Draw the following logic gate circuit based on the expressions below:

(AB + C)D

(AB + C)D




(A + B)(B + C)




A’B + (B+C)’