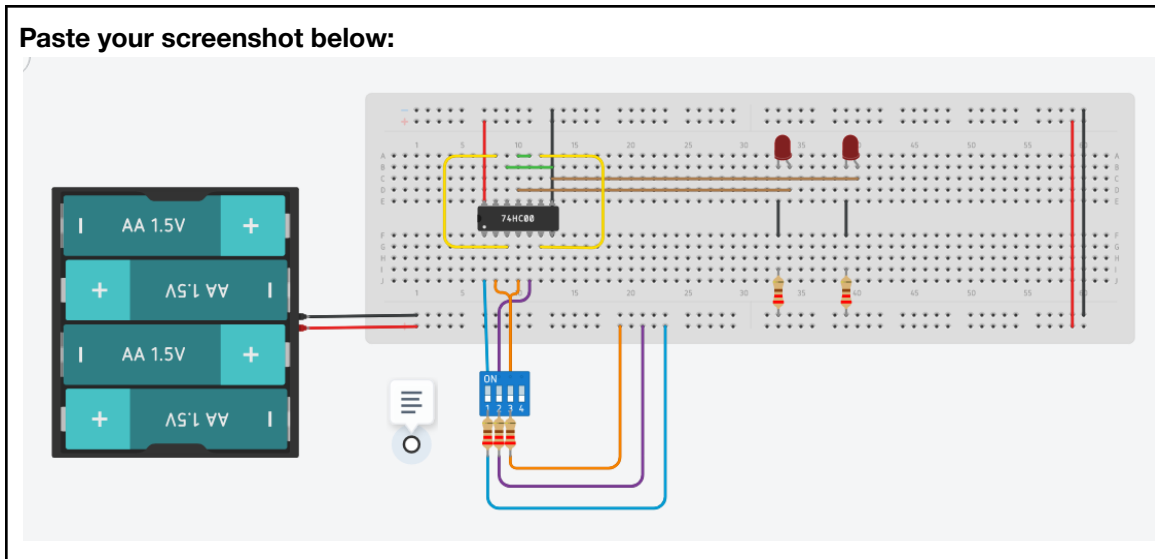


The diagram shows a D flip-flop circuit implemented with four 7400 NAND gates. The inputs are labeled as Input A (S), Input B (R), and Input C (CP - Clock Pulse). The circuit includes two 220Ω resistors and two LEDs labeled Q and  $\bar{Q}$  connected to GND. The gates are numbered 1 through 6, and the inputs are numbered 9 through 13.

**PROCEDURE:**

1. Assemble the circuit on the bread board. The inputs will come from the three push buttons.

Paste your screenshot below:



2. Toggle the inputs A, B and C, while observing the output for each of the input states listed in the observations chart below. Record your observations in the chart below. **Make sure that you set the inputs in the exact order given in the chart below.**

**OBSERVATIONS:**

		A	B	C	X	Y
Circuit Inputs and Outputs		S	R	C (Clock)	Q	Q'
Step	a	1	0	1	1	0
	b	1	0	0	1	1
	c	1	0	1	1	0
	d	0	0	0	1	0
	e	0	1	0	1	0
	f	0	1	1	0	1
	g	0	0	1	0	1
	h	1	0	1	1	0
	i	0	1	1	0	1
	j	0	1	0	0	1
	k	1	0	1	1	0
	l	1	0	0	1	0
	m	1	1	1	1	1
	n	0	0	1	1	0

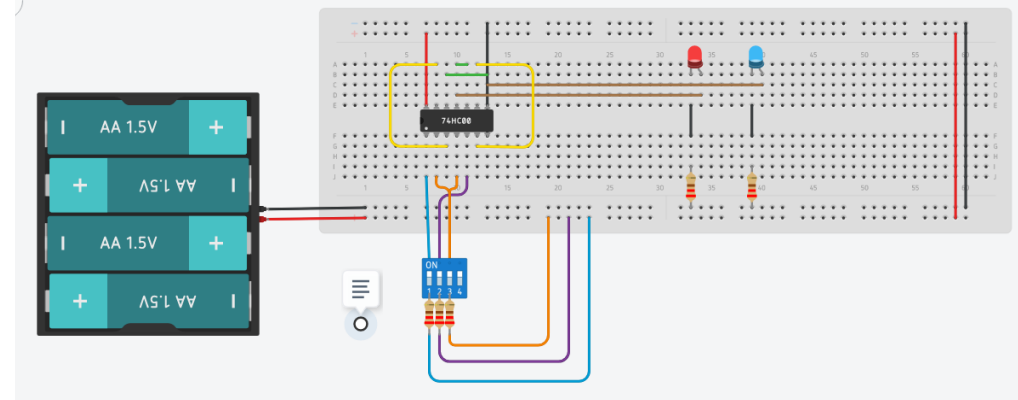
**Questions for Part B:**

1. Explain why the outputs change (or are stored from the previous output) when moving from steps a through m of the Truth Table.

When moving from steps “a” through “m” of the truth table, the output changes when every clock pulse goes from low to high.

2. Are the outputs for step m of the Truth Table complements? Could this indicate a problem?

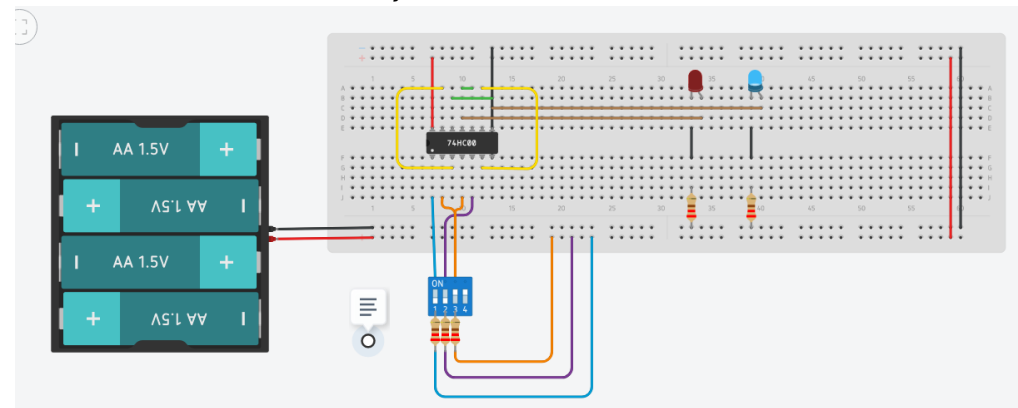
No, the outputs for step m are not complements of each other as Q and Q' are both 1.



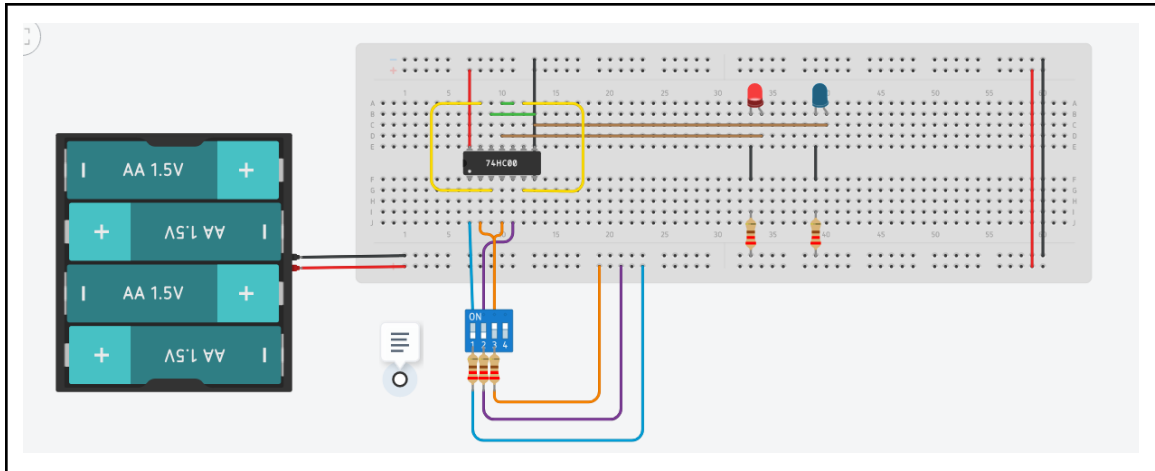
3. Move from step m to step n of the Truth Table several times. Are the outputs consistent?

The outputs are not consistent as it depends on the order of turning off S and R.

When S is turned off, followed by R



When R is turned off, followed by S



4. What is the “forbidden state”?

The forbidden state is when all inputs are 1, as the outputs of Q and Q' are both 1. This is forbidden because Q and Q' are complements of each other hence they cannot be in the same state.