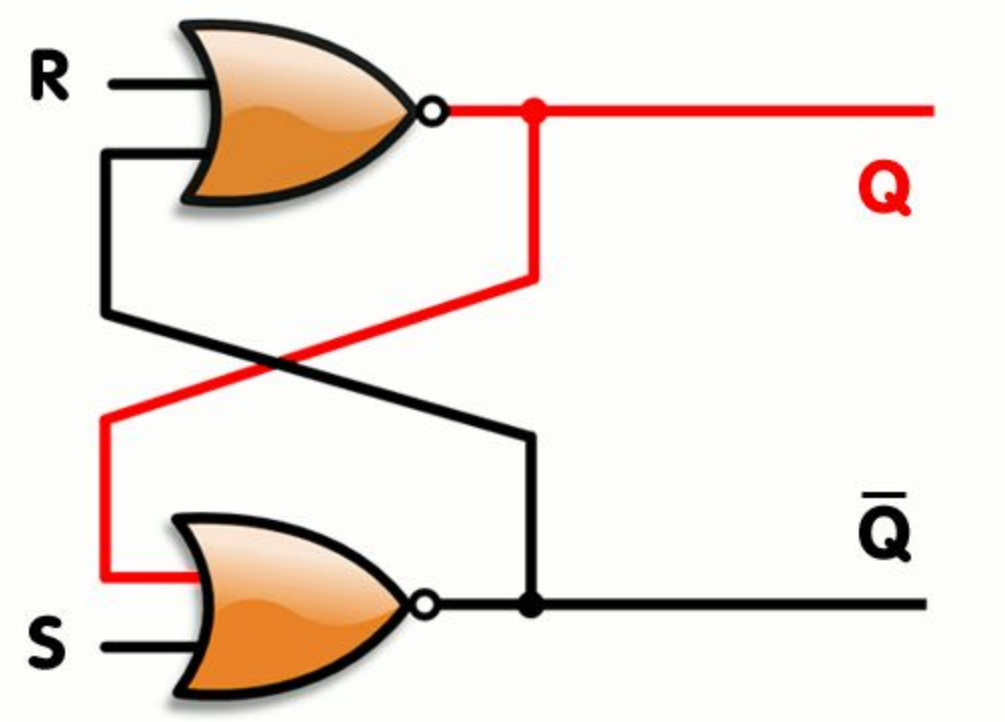
Flip-Flop Circuits



What are they used for?

For Memory circuits

For Logic Control Devices

For Counter Devices

For Register Devices

Video

Watch Both Videos on the SR Flip Flop:

https://youtu.be/-aQH0ybMd3U

https://youtu.be/HxAhOETcvr4

Types of Digital Logic Circuits

Two main types:

- Combinational Logic Circuits
- Sequential Logic Circuits

Combinational Logic Circuits

Combinational Logic Circuits:

- The AND, OR, NOR, NAND, NOT gate circuits we have built up to now.
- Inputs result in an immediate output.
- Only one output for each combination of inputs.
- No storage or memory capability.

Sequential Logic Circuits

Sequential Logic Circuits:

- Built with logic gates.
- Have memory capability (building blocks of RAM)
- Output depends upon both current value of inputs and also on the previous value of inputs.
- Outputs can be controlled by a clock pulse.
- Can have more than one output value for each combination of inputs.

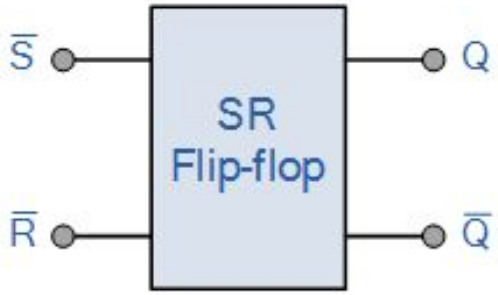
Flip-Flops

- Basic building blocks of sequential circuits.
- Several types with different capabilities
    - RS Flip-Flop
    - Clocked RS Flip-Flop
    - D Flip-Flop
    - J-K Flip-Flop (most common)

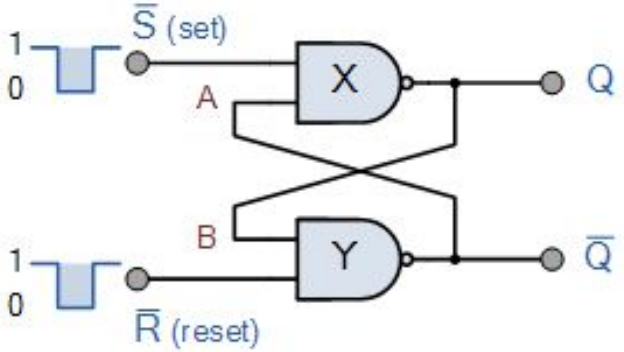
RS Flip-Flop

- Built with NOR or NAND gates
- Simplest type of flip-flops

- **Two Inputs**
  - Set (S)
  - Reset (R)
- **Two Outputs**
  - Normal Output (Q)
  - Complementary (Q')



Symbol



Circuit

The Clock

- In synchronous device, the exact times at which any output can change states are controlled by a signal commonly called the clock.

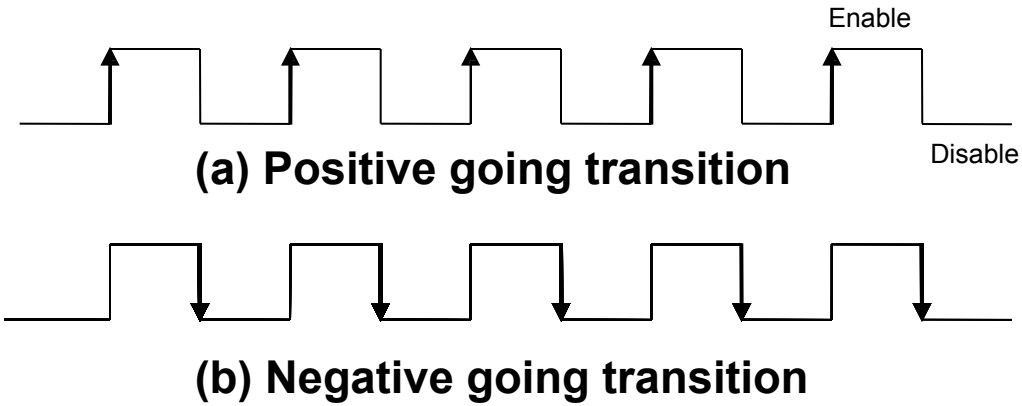
-The clock signal is generally a rectangular pulse train or a square wave

-The clock is distributed to all parts of the system, and most of the system outputs can change state only when the clock makes a transition.

The Clock

- When the clock changes from a LOW state to a HIGH state, this is called the positive-going transition (PGT) or positive edge triggered.

- When the clock changes from a HIGH state to a LOW state, it is called negative going transition (NGT) or negative edge triggered.

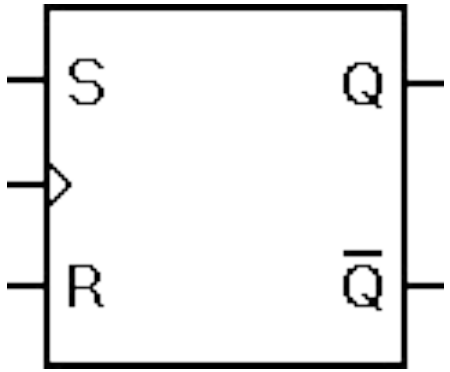


(a) Positive going transition

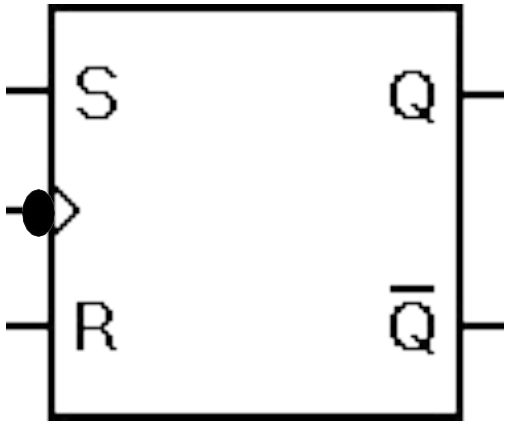
(b) Negative going transition

PGT vs NGT Schematics

- PGT



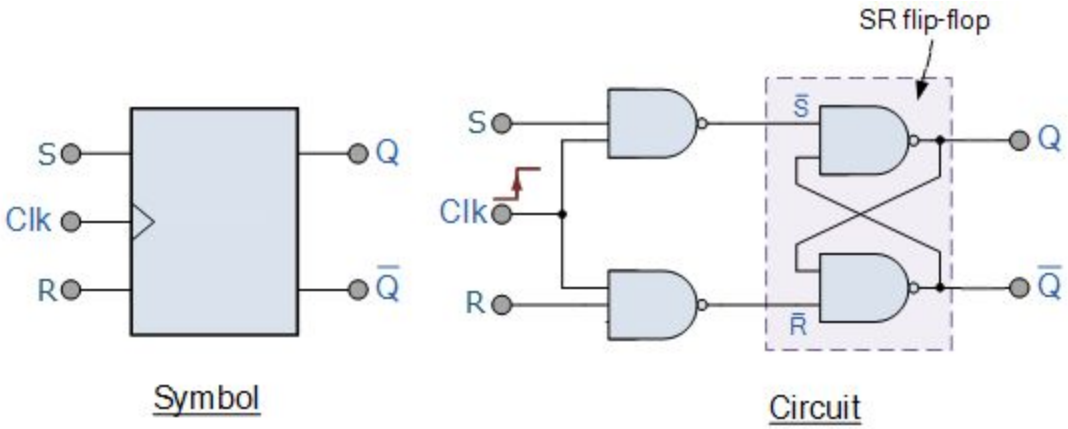
NGT



Clocked RS Flip-Flop

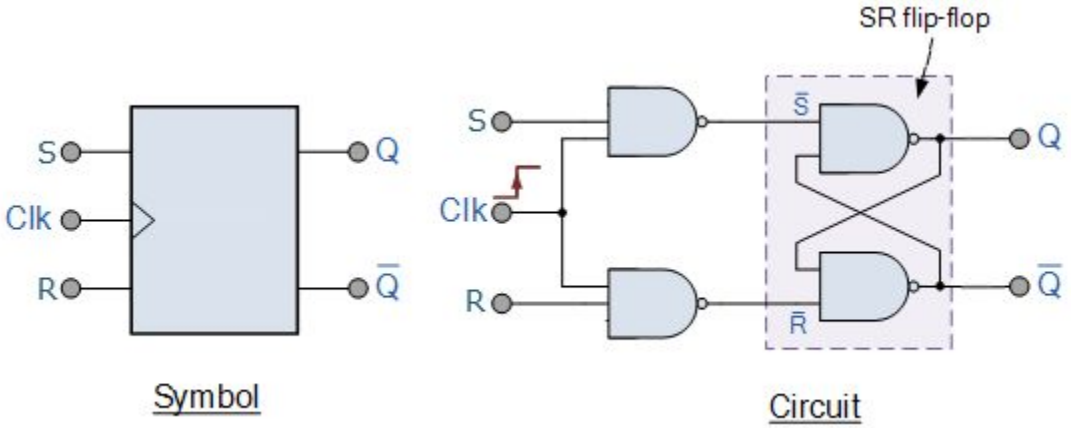
- Built with NOR or NAND gates
- PGT (Positive Going Transition)
- Clock

- Three Inputs
  - Set (S)
  - Reset (R)
  - Clock (C)
- Two Outputs
  - Normal (Q)
  - Complementary (Q')



Symbol Circuit

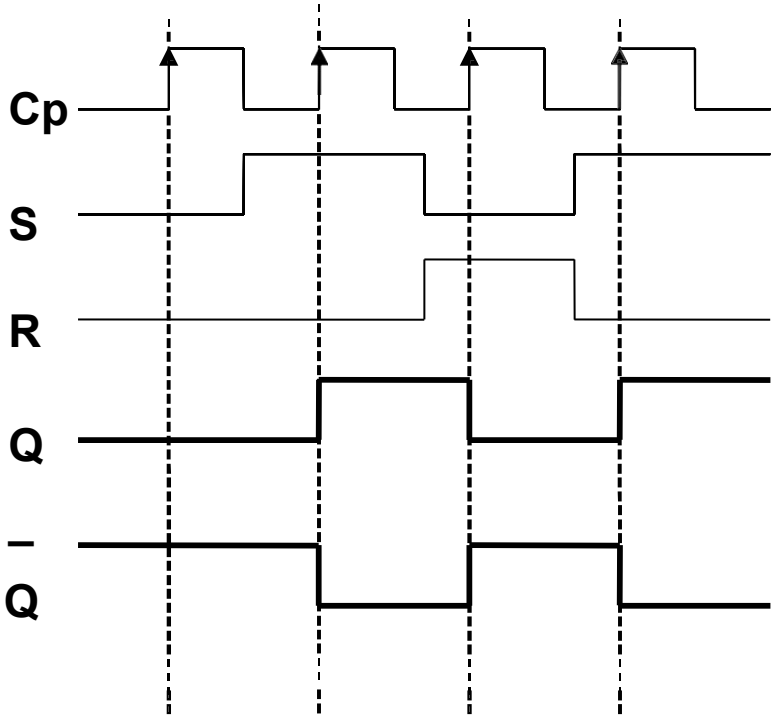
Clocked RS Flip-Flop



PGT Example

- **Example:**
  Determine the output of an active hight, **PGT** clocked RS flip flop which Q initially 0 for the given input waveforms.

  S and R are active HIGH.



NGT Example

- Determine the output of an active high, **NGT** clocked RS flip flop which **Q initially 0** for the given input waveforms.