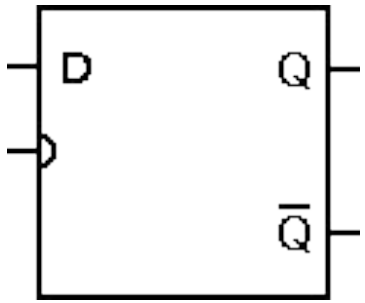
D & JK FLIP FLOPS

(Sequential Circuits)

D Flip Flop

- Also Known as Data Flip flop
- Can be constructed from RS Flip Flop or JK Flip flop by addition of an inverter.
- Inverter is connected so that the R input is always the inverse of S (or J input is always complementary of K).
- The D flip flop will act as a storage element for a single binary digit (Bit).

D Flip flop symbol



D Flip Flop - Symbol

PGT

NGT

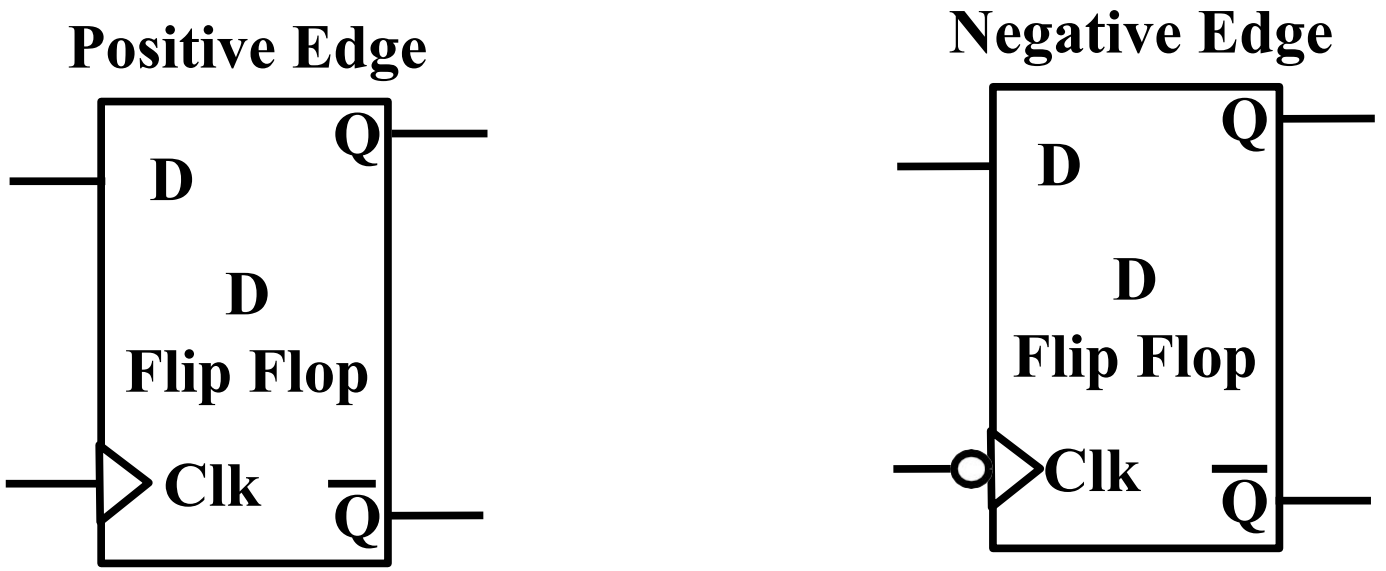
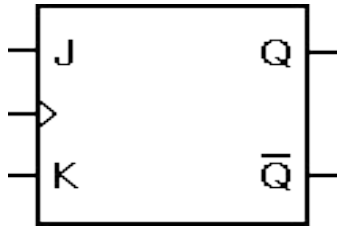


Figure 4.6.2 : D Flip flop symbol using JK Flip Flop / SR Flip Flop

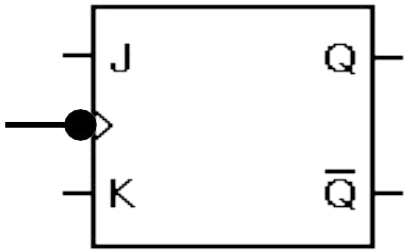
JK Flip Flop - Symbol

- Another types of Flip flop is JK flip flop.
- It differs from the RS flip flops when J=K=1 condition is not indeterminate but it is defined to give a very useful changeover (toggle) action.
- Toggle means that **Q** and **Q'** will switch to their opposite states.
- The JK Flip flop has clock input Cp and two control inputs J and K.
- Operation of Jk Flip Flop is completely described by truth table in Figure 4.3.3.

- **PGT JK Flip flop symbol**



- **NGT JK Flip flop symbol**

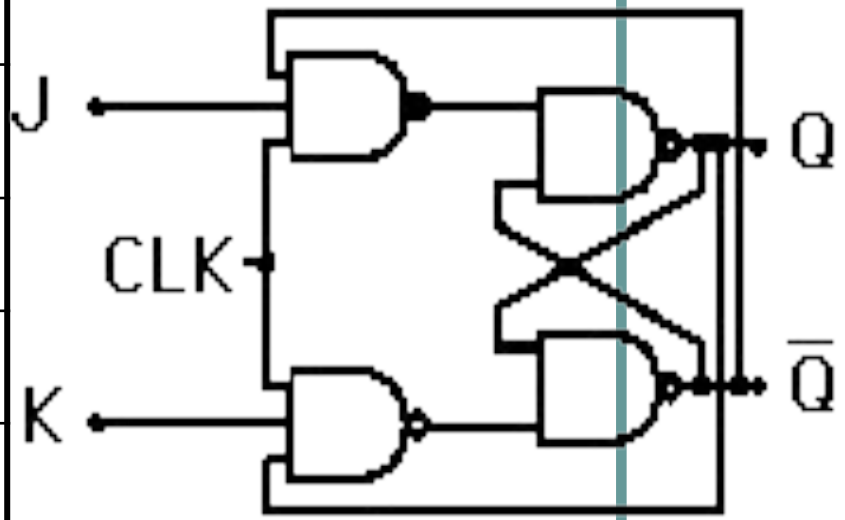


JK Flip Flop – Truth Table And Logic Circuit

Truth Table for JK Flip Flop

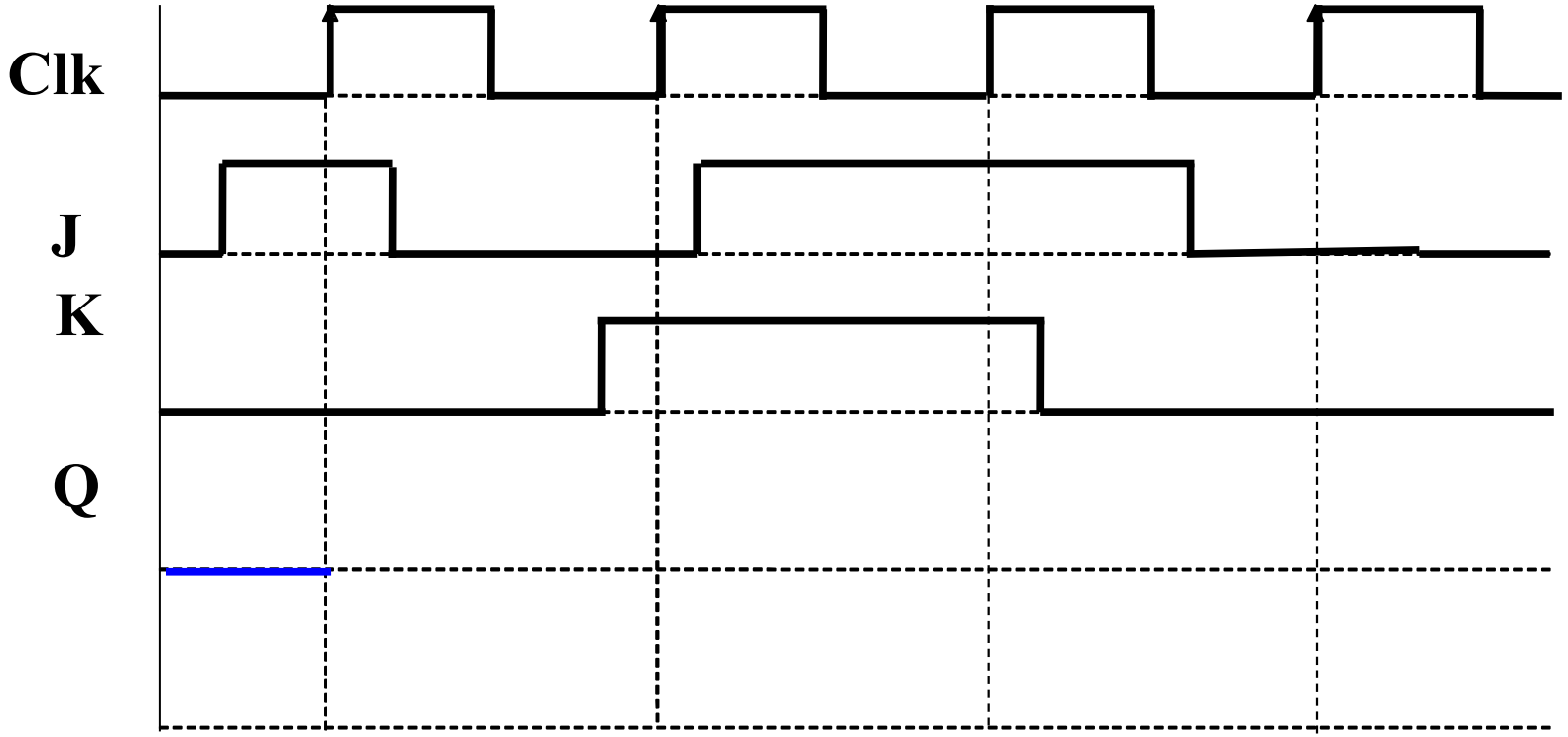
clock	J	K	Q	Q’	STATUS
↑	0	0	Q	Q’	HOLD (No Change)
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	Q'	Q	Toggle

JK FLIP FLOP LOGIC CIRCUIT



JK Flip Flop - waveforms

Example: Determine the output of PGT clocked JK flip flop for the given input waveforms which the Q initially 0.

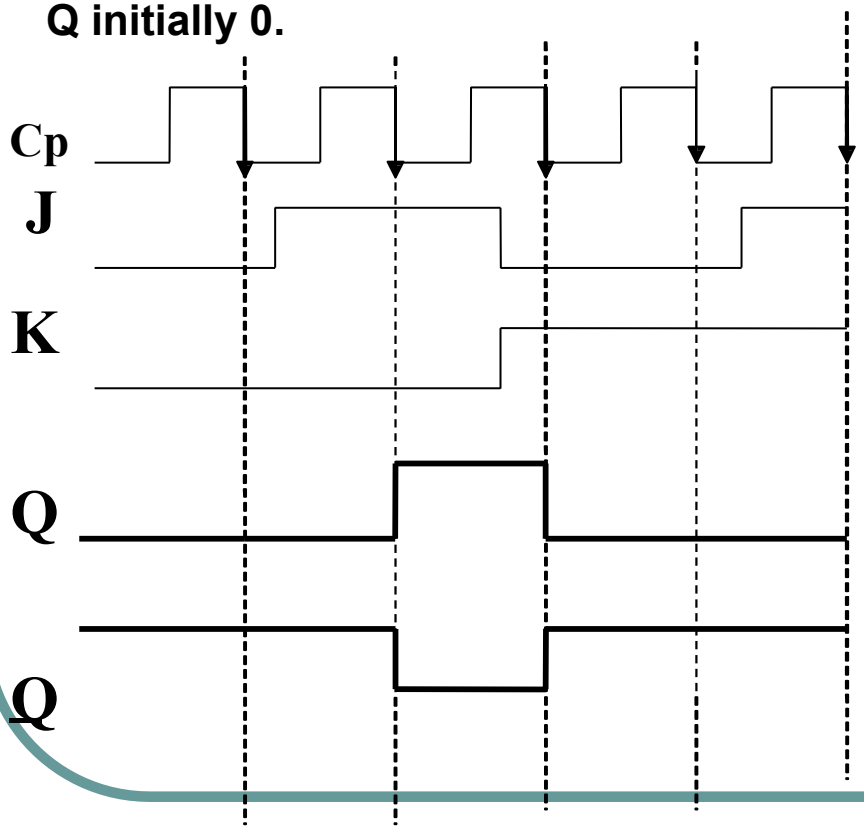


JK Flip Flop - Completed Diagram

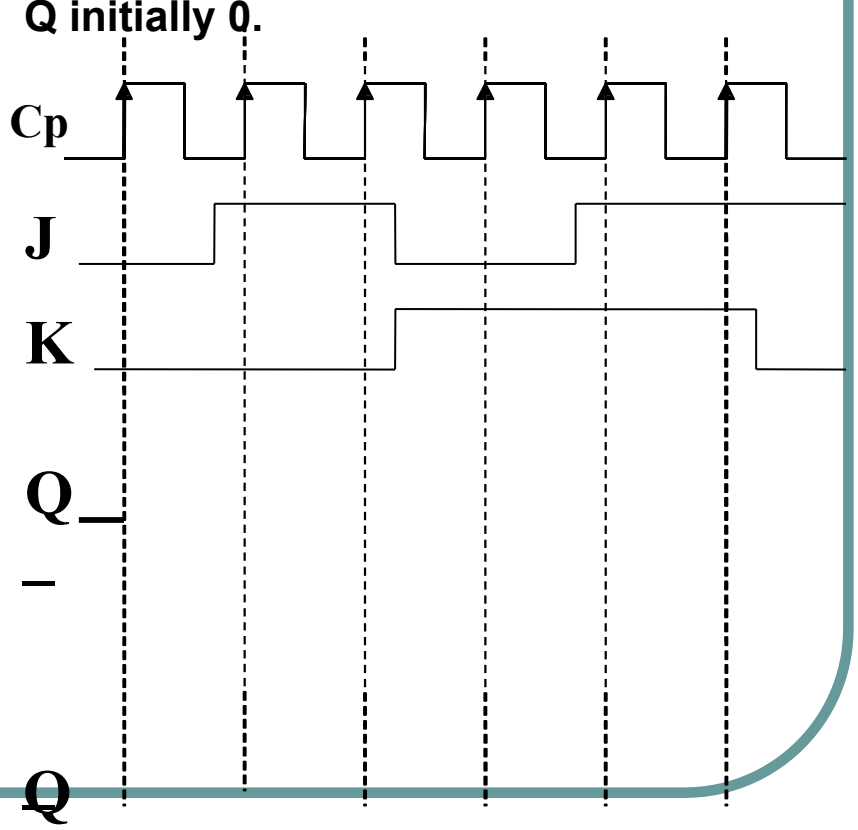
Example: Determine the output of PGT clocked JK flip flop for the given input waveforms which the Q initially 0.

JK Flip Flop - waveforms

E$_{\textbf{xercise}}$:Determine the output of **NGT** clocked JK flip flop for the given input waveforms which the **Q initially 0.**



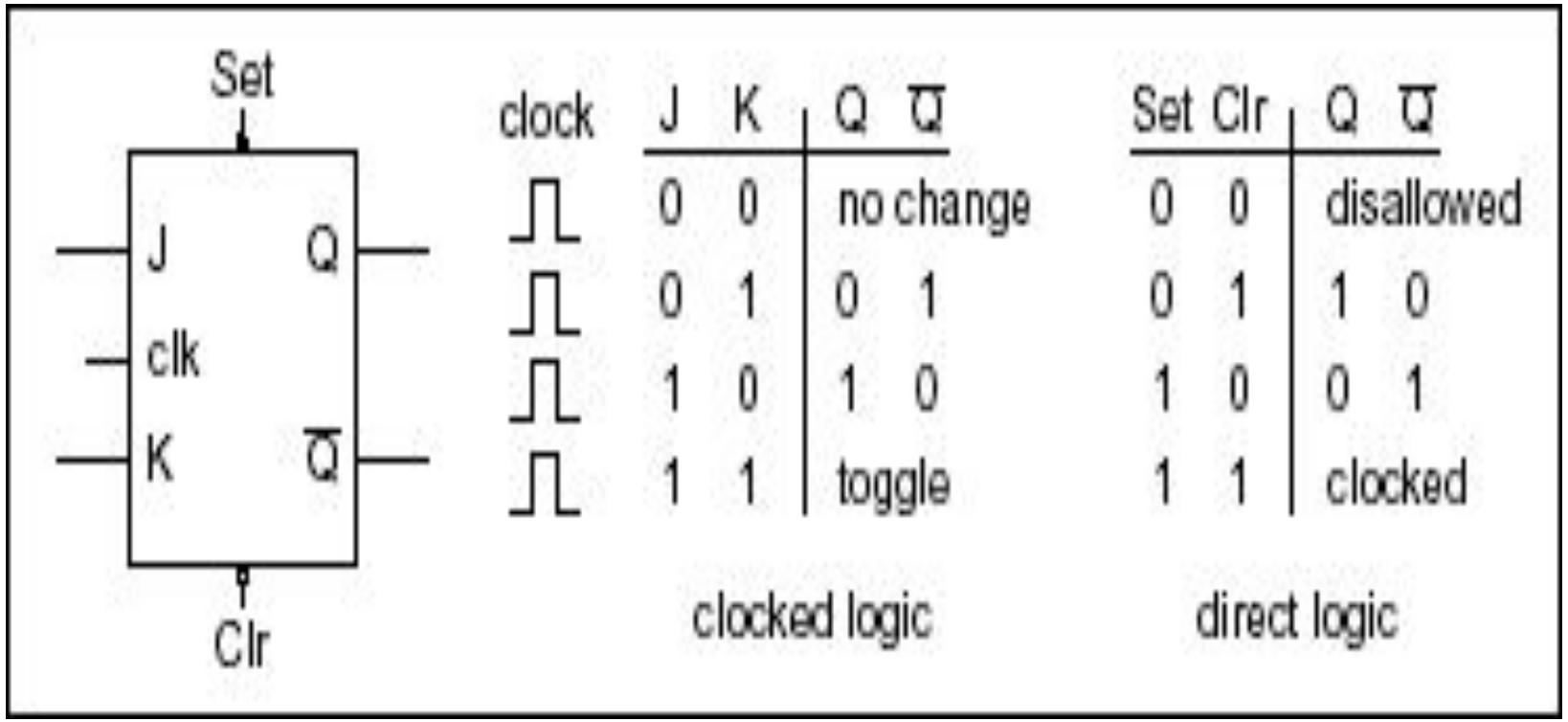
Exercise:Determine the output of **PGT** clocked JK flip flop for the given input waveforms which the **Q initially 0.**



JK Flip Flop with Asynchronous Input

- The J and K inputs are called synchronous inputs since they only influence the state of the flip flop when the clocked pulse is present.
- This flip flop can also have other inputs called Preset (or SET) and clear that can be used for setting the flip flop to 1 or resetting it to 0 by applying the appropriate signal to the Preset and Clear inputs.
- These inputs can change the state of the flip flop regardless of synchronous inputs or the clock.

JK Flip Flop with Preset and Clear



clock	J	K	Q	Q̄
	0	0	no change	
	0	1	0	1
	1	0	1	0
	1	1	toggle	

clocked logic

Set	Clr	Q	Q̄
0	0	disallowed	
0	1	1	0
1	0	0	1
1	1	clocked	

direct logic

Figure 4.4.1 : Symbol and Truth Table

JK Flip Flop with Asynchronous Input

- **Example** : The output of clocked JK flip flop which output **initially 0** for the given input waveforms. Clock (NGT)