CHAPTER 7

Flip-Flops

Learning Outcomes

This chapter will help you to:

7-1 *Explain* the function of each input and output on the R-S flip-flop. *Use* key words dealing with flip-flops, including set, reset, hold, active LOW, and active HIGH. *Describe* some uses of latches and their operation.

7-2 *Interpret* clocked R-S flip-flop waveforms and truth tables. *Explain* the modes of operation.

7-3 *Analyze* the truth table with modes of operation for the 7474 D flip-flop.

7-4 *Predict* the operation of several J-K flip-flop ICs, including the toggle mode.

7-5 *Describe* the use and operation of the 7475 4-bit latch in a simple system.

7-6 *Classify* flip-flops as synchronous or asynchronous and *compare* triggering.

7-7 *Describe* the operation of Schmitt-triggered devices and *cite* some applications.

7-8 *Compare* traditional with IEEE/ANSI flip-flop symbols.

7-9 *Analyze* and *explain* the operation of a latched encoder-decoder system.

Engineers classify logic circuits into two groups. We have already worked with *combination logic circuits* using AND, OR, and NOT gates. The other group of circuits is classified as *sequential logic circuits*. Sequential circuits involve timing and memory devices. The basic building block for combinational logic circuits is the logic gate. The basic building block for sequential logic circuits is the *flip-flop (FF)*. This chapter covers several types of flip-flop circuits. In later chapters you will wire flip-flops together. Flip-flops are wired to form *counters*, *shift registers*, and various *memory devices*.

Combination logic circuits

Sequential logic circuits

Counters

Shift registers

Memory devices

7-1 The R-S Flip-Flop

R-S flip-flop

The logic symbol for the *R-S flip-flop* is drawn in Fig. 7-1. Notice that the R-S flip-flop has two inputs, labeled S and R. The two outputs are labeled Q and $\overline{Q}$ (say "not Q" or "Q not"). In flip-flops the outputs are always opposite, or *complementary*. In other words, if output $Q = 1$, then output $\overline{Q} = 0$, and so on. The R-S flip-flop symbol from Fig. 7-1 labels the outputs as *normal* and *complementary*. The letters S and R at the left of the R-S flip-flop symbol are often referred to as the *set* and *reset* inputs. The inputs are *active LOW* (see bubble).

Complementary

Set and reset

The R-S flip-flop may also be referred to as an *R-S latch*. The term "latch" refers to its use as a temporary memory device. A latch such as the R-S flip-flop in Fig. 7-1 can hold one bit of information.

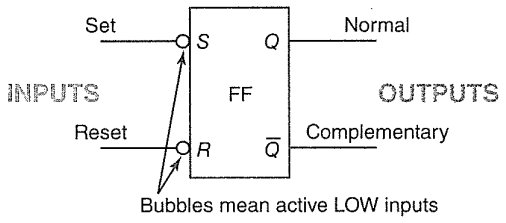


Fig. 7-1 Logic symbol for an R-S flip-flop.

Table 7-1 Truth Table for R-S Flip-flop

Mode of operation	Inputs S	Inputs R	Outputs Q	Outputs $\overline{Q}$	Effect on output Q
Prohibited	0	0	1	1	Prohibited: Do not use
Set	0	1	1	0	For setting Q to 1
Reset	1	0	0	1	For resetting Q to 0
Hold	1	1	Q	$\overline{Q}$	Depends on previous state

The truth table in Table 7-1 details the operation of the R-S flip-flop. When the S and R inputs are both 0, both outputs go to a logical 1. This is called a *prohibited state* for the flip-flop and is not used. The second line of the truth table shows that when input S is 0 and R is 1, the Q output is set to logical 1. This is called the *set condition*. The third line shows that when input R is 0 and S is 1, output Q is reset (cleared) to 0. This is called the *reset condition*. Line 4 in the truth table shows both inputs (R and S) at 1. This is the idle or at rest condition and leaves Q and $\overline{Q}$ in their previous complementary states. This is called the *hold condition*.

From Table 7-1, it may be observed that it takes a logical 0 to activate the set (set Q to 1). It also takes a logical 0 to activate the reset, or clear (clear Q to 0). Because it takes a logical 0 to enable, or activate, the flip-flop, the logic symbol in Fig. 7-1 has invert bubbles at the R and S inputs. These invert bubbles indicate that the set and reset inputs are activated by a logical 0.

R-S flip-flops can be purchased in an IC package, or they can be wired from logic gates, as shown in Fig. 7-2. The NAND gates in Fig. 7-2 form an R-S flip-flop. This NAND-gate R-S flip-flop operates according to the truth table in Table 7-1. Technically, the R-S flip-flop in Fig. 7-2 might be referred to as an $\overline{R}$-$\overline{S}$ flip-flop or $\overline{R}$-$\overline{S}$ latch. The overbars above the R and S mean these are active LOW inputs. These overbars are used by some industry sources.

Many times *timing diagrams*, or *waveforms*, are given for sequential logic circuits. These diagrams show the voltage level and timing between inputs and outputs and are similar to what you would observe on an oscilloscope. The horizontal distance is *time*, and the vertical distance is *voltage*. Figure 7-3 shows the input waveforms (R, S)

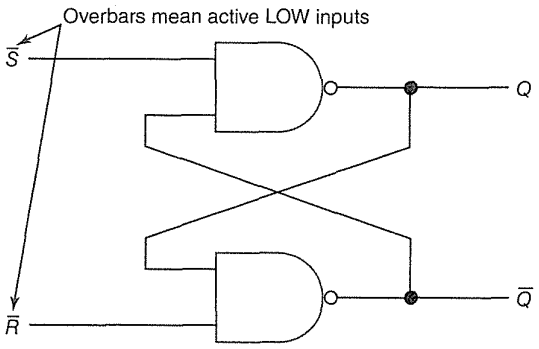


Fig. 7-2 Wiring an $\overline{R}$-$\overline{S}$ flip-flop using NAND gates.

and the output waveforms (Q, $\overline{Q}$) for the R-S flip-flop. The bottom of the diagram lists the lines of the truth table from Table 7-1. The Q waveform shows the set and reset conditions of the output; the logic levels (0, 1) are on the right side of the waveforms. Waveform diagrams of the type shown in Fig. 7-3 are very common when dealing with sequential logic circuits. Study this diagram to see what it tells you. The waveform diagram is really a type of truth table.

Hold condition

Recall that there are three types of multivibrators (MVs). They are the monostable MV, the astable MV, and the bistable multivibrator. The R-S flip-flop is one of several bistable MVs. The R-S flip-flop is most commonly known as a *latch* and is listed under this heading in IC catalogs. A latch is a fundamental binary memory device for holding data. Latches are commonly used at the output of a digital device to hold the data until the next device is ready to receive the input. Latches are commonly organized into groups of 4-bits, 8-bits, or more into *registers*. An 8-bit register would be a group of eight latches holding a byte of information. You may recall that R-S flip-flops were also used for switch debouncing.

R-S latch

Waveform diagram

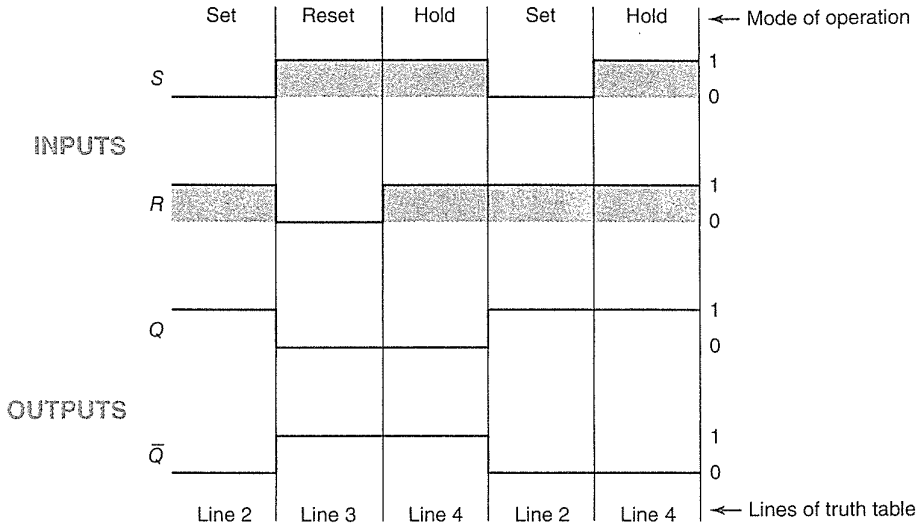


Fig. 7-3 Waveform diagram for an R-S flip-flop.

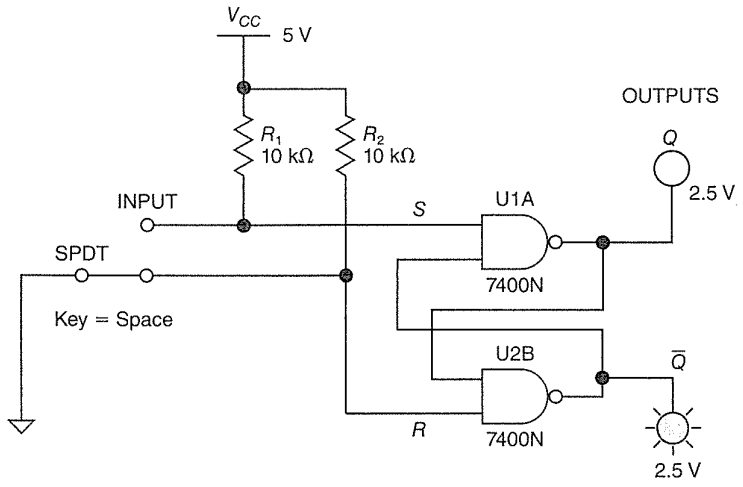


Fig. 7-4 SPDT switch debouncing circuit.

Internet Connection

Look up latch or SR latch at en.wikipedia.org.

Figure 7-4 shows the application of an R-S flip-flop in an SPDT switch debouncing circuit.

Commercial versions of the R-S flip-flop are available. One example is the *74LS279 Quad* $\overline{S}$-$\overline{R}$ *Latch IC*. It contains four latches like the one you studied from Fig. 7-2. Later in this chapter you will study the *7475/74LS75/74HC75 4-bit latch* in detail.

Do you know the logic symbol and truth table for the R-S flip-flop? Do you know the four modes of operation for the R-S flip-flop?

Self-Test

Answer the following questions.

1. The R-S flip-flop in Fig. 7-1 has active _____ (HIGH, LOW) inputs.
2. List the mode of operation of the R-S flip-flop for each input pulse shown in Fig. 7-5. Answer with the terms "set," "reset," "hold," and "prohibited."
3. List the binary output at the normal output (Q) of the R-S flip-flop for each of the pulses shown in Fig. 7-5.

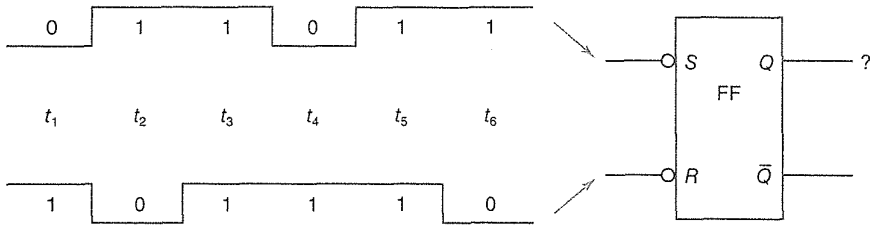


Fig. 7-5 R-S flip-flop pulse-train problem.

7-2 The Clocked R-S Flip-Flop

Clocked R-S flip-flop

The logic symbol for a *clocked R-S flip-flop* is shown in Fig. 7-6. Observe that it looks almost like an R-S flip-flop except that it has one extra input labeled *CLK* (for clock).

The operation of the clocked R-S flip-flop is detailed in Fig. 7-7. The *CLK input* is at the top of the diagram. Notice that the clock pulse (1) has no effect on output Q with inputs S and R in the 0 position. The flip-flop is in the *idle*, or *hold*, mode during clock pulse 1. At the preset S position, the S (set) input is moved to 1, but output Q is not yet set to 1. The rising edge of clock pulse 2 permits Q to go to 1. Pulses 3 and 4 have no effect on output Q. During pulse 3, the flip-flop is in its set mode, and during pulse 4, it is in its hold mode. Next, input R is preset to 1. On the rising edge of clock pulse 5, the Q output is reset (or cleared) to 0. The flip-flop is in the reset mode during both clock pulses 5 and 6. The flip-flop is in its hold mode during clock pulse 7; therefore, the normal output (Q) remains at 0.

CLK input

Notice that the outputs of the clocked R-S flip-flop *change only on a clock pulse.* We say that this flip-flop operates *synchronously;*

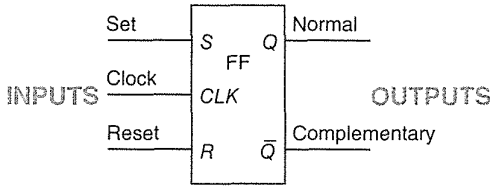


Fig. 7-6 Logic symbol for a clocked R-S flip-flop.

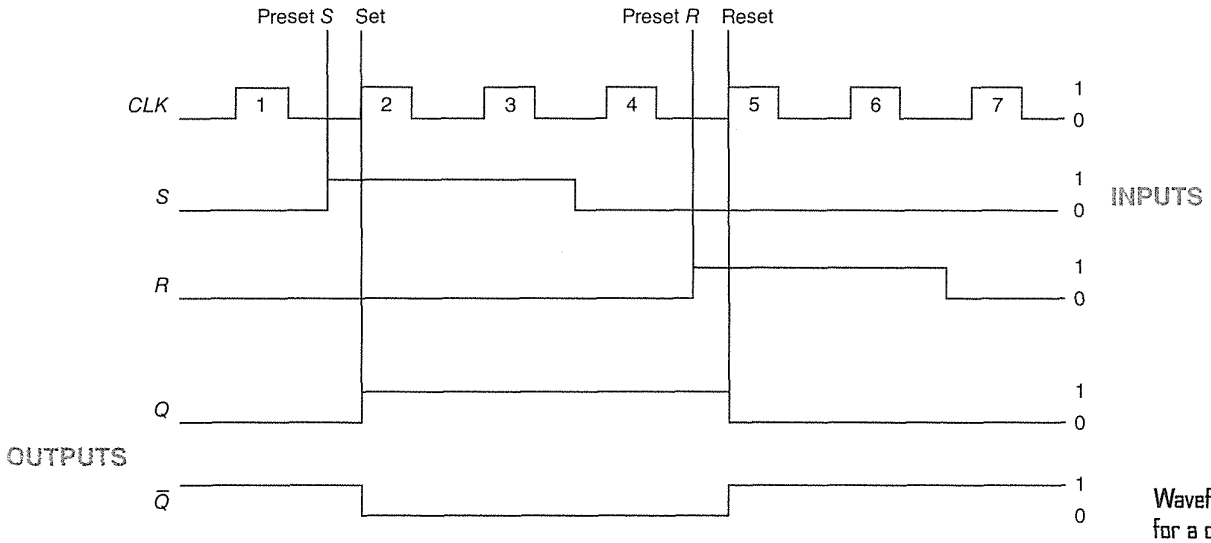


Fig. 7-7 Waveform diagram for a clocked R-S flip-flop.

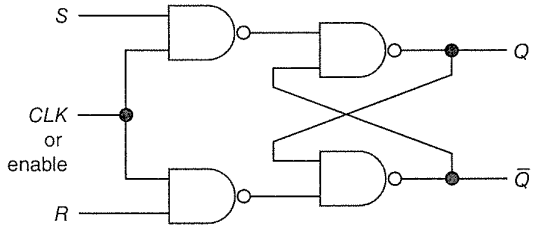
Waveform diagram for a clocked R-S flip-flop

Truth table for a clocked R-S flip-flop

Mode of operation	INPUTS			OUTPUTS		
	CLK	*S*	*R*	*Q*	$\bar{Q}$	Effect on output *Q*
Hold		0	0	No change		No change
Reset		0	1	0	1	Reset or cleared to 0
Set		1	0	1	0	Set to 1
Prohibited		1	1	1	1	Prohibited—do not use

(*a*)

Wiring a clocked R-S flip-flop using NAND gates



(*b*)

Fig. 7-8 (*a*) Truth table for a clocked R-S flip-flop (*b*) Wiring a clocked R-S flip-flop using NAND gates.

Synchronous operation

it operates *in step with* the clock. *Synchronous operation* is very important in most digital circuits, where each step must happen in an exact order.

Another characteristic of the clocked R-S flip-flop is that once it is set or reset, it stays that way even if you change some inputs. This is a *memory characteristic*, which is extremely valuable in many digital circuits. This characteristic is evident during the hold mode of operation. In the waveform diagram in Fig. 7-7, this flip-flop is in the hold mode during clock pulses 1, 4, and 7.

Memory characteristic

Figure 7-8(*a*) shows a truth table for the clocked R-S flip-flop. Notice that only the top three lines of the truth table are usable; the bottom line is prohibited and not used. Observe that the *R* and *S* inputs to the clocked R-S flip-flop are active HIGH inputs. That is, it takes a HIGH on input *S* while $R = 0$ to cause output *Q* to be set to 1.

Figure 7-8(*b*) shows a wiring diagram of a clocked R-S flip-flop. Notice that two NAND gates have been added to the inputs of the R-S flip-flop to add the clocked feature. The *CLK* input may be labeled with a *C* or *E* for enable by various manufacturers.

It is important to remember that the memory characteristics exhibited by flip-flops are among the fundamental reasons why digital technology has become so widely used in modern electronic products. It is strongly suggested that you actually experiment with R-S and clocked R-S flip-flops either on a circuit simulator or with actual ICs on a solderless breadboard. Operating flip-flops in the lab will help you better understand their operation.

Self-Test

Answer the following questions.

4. The set and reset inputs *(S, R)* of the clocked R-S flip-flop in Fig. 7-6 are active _____ (HIGH, LOW) inputs.
5. List the mode of operation of the clocked R-S flip-flop for each input pulse shown in Fig. 7-9. Answer with the terms "set," "reset," "hold," and "prohibited."
6. List the binary output at the normal output (Q) of the clocked R-S flip-flop for each of the pulses shown in Fig. 7-9.
7. To *set* a flip-flop means to cause the normal output (Q) to go _____ (HIGH, LOW).
8. Refer to Fig. 7-9. The *CLK* on this clocked R-S flip-flop might be labeled *EN* for _____ (encoder, enable) by some manufacturers.

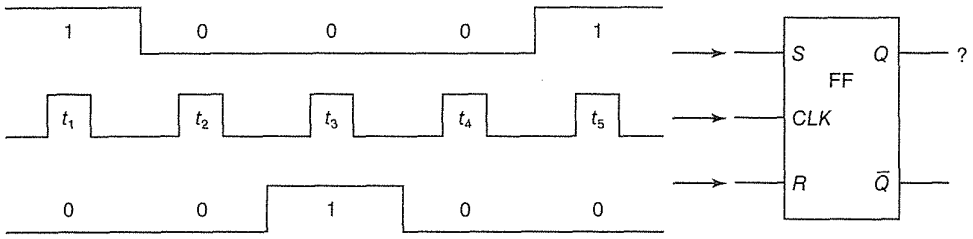


Fig. 7-9 Clocked R-S flip-flop pulse-train problem.

7-3 The D Flip-Flop

The logic symbol for the *D flip-flop* is shown in Fig. 7-10(*a*). It has only one *data input* (*D*) and a clock input (*CLK*). The outputs are labeled Q and $\overline{Q}$. The D flip-flop is often called a *delay flip-flop*. The word "delay" describes what happens to the data, or information, at input *D*. The data (a 0 or 1) at input *D* is *delayed one clock pulse* from getting to output Q. A simplified truth table for the D flip-flop is shown in Fig. 7-10(*b*). Notice that output Q follows input *D after one clock pulse* (see Q^{n+1} column).

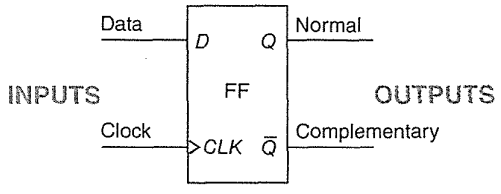
A D flip-flop may be formed from a clocked R-S flip-flop by adding an inverter, as shown in Fig. 7-11. More commonly you will use a D flip-flop contained in an IC. Figure 7-12(*a*) shows a typical commercial D flip-flop. Two extra inputs [*PS* (preset) and *CLR* (clear)] have been added to the D flip-flop in Fig. 7-12(*a*). The *PS* input sets output Q to 1 when enabled by a logical 0. The *CLR* input clears output Q to 0 when enabled by a logical 0. The *PS* and *CLR* inputs will override the *D* and *CLK* inputs. The *D* and *CLK* inputs operate as they did in the D flip-flops in Fig. 7-10.

Note the addition of a small triangle on the *CLK* input of the IC symbol in Fig. 7-12(*a*). This small triangle inside the 7474 IC symbol in Fig. 7-12(*a*) means the flip-flop is *edge-triggered.*

D flip-flop

Delay flip-flop

Edge triggering



(*a*)

Input	Output
D	Q^{n+1}
0	0
1	1

(*b*)

Fig. 7-10 D flip-flop. (*a*) Logic symbol (*b*) Simplified truth table.