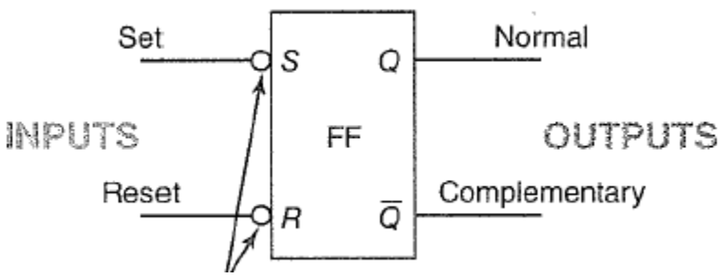
RS Flip Flop Self-Test Questions

Question #1 is referring to the picture below.



1. The R-S flip-flop in Fig. 7-1 has active _____ (HIGH, LOW) inputs.

Answer: Low because it contains a circle in the input

The following two questions depend on viewing the diagram below:

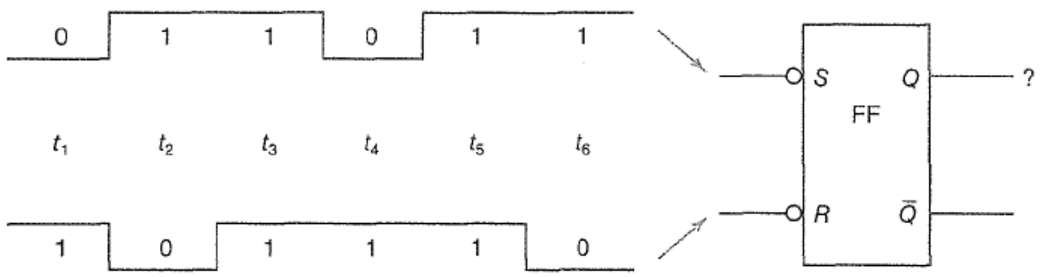


Fig. 7-5 R-S flip-flop pulse-train problem.

2. List the mode of operation of the R-S flip-flop for each input pulse shown in Fig. 7-5. Answer with the terms "set," "reset," "hold," and "prohibited."

Answer:

1. Set
2. Reset
3. Hold
4. Set
5. Hold
6. Reset
7. Q = 0 Q'= 1

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3. List the binary output at the normal output (Q) of the R-S flip-flop for each of the pulses shown in Fig. 7-5.

Answer:
1. 1
2. 0
3. 0
4. 1
5. 1
6. 0

4. The set and reset inputs (S, R) of the clocked R-S flip-flop in Fig. 7-6 are active _____ (HIGH, LOW) inputs.

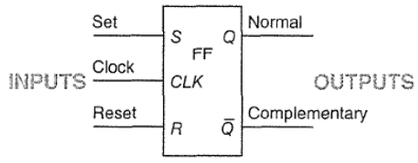

Fig. 7-6 Logic symbol for a clocked R-S flip-flop.

Answer:
High

The next two questions depend on viewing the diagram below:

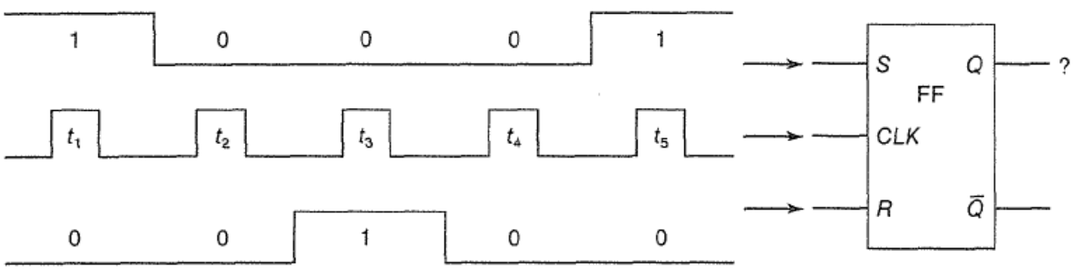

Fig. 7-9 Clocked R-S flip-flop pulse-train problem.

5. List the mode of operation of the clocked R-S flip-flop for each input pulse shown in Fig. 7-9. Answer with the terms "set," "reset," "hold," and "prohibited."

Answer:
1. Set
2. Hold
3. Reset
4. Hold
5. Set

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6. List the binary output at the normal output (Q) of the clocked R-S flip-flop for each of the pulses shown in Fig. 7-9.

Answer:
1. 1
2. 1
3. 0
4. 0
5. 1

7. To *set* a flip-flop means to cause the normal output (Q) to go _____ (HIGH, LOW).

Answer:
High

8. Refer to Fig. 7-9. The *CLK* on this clocked R-S flip-flop might be labeled *EN* for _____ (encoder, enable) by some manufacturers.

Answer:
Enable