Student Name: \_\_\_\_\_

## **TEJ4M0 Boolean Algebra Summative Project**

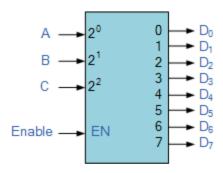
Student #:

## **OBJECTIVE**

Build a decoder using truth tables, logic gates and simplify the expressions using K-Maps. You will need to provide schematics made in Logisim and you will also wire your circuit virtually using Tinkercad.

### You have three options:

**Option #1:** Max 80%: In class we created a 2-to-4 binary decoder. You will be creating a 3-to-8 binary decoder with an enable bit. This decode will work slightly differently.



This decoder should take 3 binary inputs (A (least significant bit), B, and C (most significant bit), and produce 8 binary outputs. The enable bit, when in the off position, will completely disable ALL outputs.

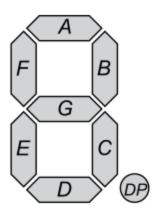
This decoder works a little bit differently than the one that we did in class. Let's forget about the enable bit for a second. When A, B, and C are all 0 only D0 should light up. All other outputs will be 0. When A is 1 and BC are both 0, D0 and D1 will light up. All other outputs are off. When the binary inputs evaluate to 2 in decimal, D0, D1 and D2 will be on and the other outputs will remain off. See the pattern? Create the truth table first and don't forget about the Enable bit!

#### Option #2:

Producing a <u>common cathode display</u> capable of displaying the capital letters A, B, C, E, F, G, H, L, O, P, S, U will be eligible for a mark up to 90%. You may use X's in your K-Map if you would like to. X's appear in a kmap when an input is not required to show a specific output. X's

Student Name: Student #:

can be counted as a 1 or a 0. You would count an 'X' as a '1' if it helps to make a larger grouping of 1's.



Once you are done, add in a fifth input as the Enable bit (this fifth bit will not be in your K-Map). You will add this bit in your virtual circuit When this bit is 0, it turns off the whole circuit.

## Option #3:

Producing a <u>common anode display</u> of 2 digits, capable of displaying any number of values 28 and greater will receive 100%. When the ABCD inputs are all 0, the display should read 28. When ABCD evaluates to 1, the number 29 should be displayed. When ABCD evaluates to 2 in decimal, the number 30 should be displayed. You will go all the way until 43. You will need to use two seven segment displays side by side. Once you are done, add in a fifth input as the Enable bit (this fifth bit will not be in your K-Map). You will add this bit in your virtual circuit. When this bit is 0, it turns off the whole circuit.

# **STEPS:**

In order to build this project, you will need to do the following steps in order:

- 1. You must learn and understand how to wire a common cathode 7-segment display. Learn how to light up each individual segment and understand what each of the pins represent.
- 2. Create the truth table and then organize your K-map. Get the simplest equation for each output.
- 3. Use Logisim to wire your circuit. Keep it organized so that each wire can be easily seen. Save the file so that you can upload it later to the Google Classroom. A screenshot will be needed to go in your report.
- 4. Wire your circuit in Tinkercad. You will need to use the DIP switch to send inputs to the Logic gates.

Student Name:	Student #:

In the field of electronics it's not good enough for your circuit to simply function correctly; the circuit must be designed and built in a fashion which allows for easy troubleshooting. You will be graded on both functionality and neatness of the breadboard circuit. Ensure you use standard industry wire colour guidelines when building your circuit (see Helpful Hints section below).

### PROJECT DELIVERABLES

- 1. Design and build the circuit (see below for Circuit Operation Requirements).
- 2. Demonstrate the circuit working through a SHARED Tinkercad link in this report and explain your circuit design in your report.
- 3. Submit a project report (see below for Project Report Requirements).

# **CIRCUIT OPERATION REQUIREMENTS:**

- 1. The 7-segment display we will be using is **common cathode / anode type**
- 2. Use as few logic gate chips as possible
- 3. Tidy up wiring for easy troubleshooting.
- 4. Use appropriate wire colours (RED +, BLACK -, all other connections must be different than black/red).

Student Name:	Student #:

### PROJECT REPORT REQUIREMENTS

In addition to building and demonstrating your circuit, you will need to submit a neatly **typed** project report which contains the following sections:

- 1. A Cover Page (with a picture of your circuit on it, your name, teacher's name, course code, and date).
- 2. A Table of Contents (needs to have page #'s and specific headings on it)
- 3. A *Summary* page describing the purpose and functionality of the circuit. Explain how to test your circuit (ex: Which switch is A/B/C/D/E?)
- 4. A *Parts List* indicating all components used and quantities.
- 5. A section called *Process Work* where you will provide a truth table, K-Map, and all final output expressions. This also includes planning work organizing your Tinkercad circuit. This can include your Logisim circuit OR screenshots on paper of your work.
- 6. Screenshot of your Logisim Circuit as well as the Logisim file attached to the Assignment post. Make sure that all components are included.
- 7. Shared link to your circuit. This way I can test out your completed circuit. To get a shareable link to your circuit, click on SHARE in Tinkercad. Click on INVITE PEOPLE. Next, click on GENERATE NEW LINK and then click on COPY. Include the address within your report.

## **HELPFUL HINTS**

- 1. When wiring your breadboard, follow the following wire colour standard:
  - i. RED All connections to +5V
  - ii. BLACK All connections to 0 V
  - iii. Yellow/White/Other Colours Remaining control wiring

Student Name:	Student #:	
	Digital Unit Summative Project– Evaluation Rubric	
·	Total· / 70	

**Note:** You will be required to show your work throughout the periods allocated for this assignment. Be prepared to submit progress reports on the Google Classroom. I will make dropbox submissions for each week.

week.				
Criteria	Level 1 (50 – 59%)	Level 2 (60 – 69%)	Level 3 (70 – 79%)	<b>Level 4</b> (80 – 100%)
Understanding of scenario: truth tables, K-Maps (most reduced form), schematic symbols, electronic components (Knowledge)	Demonstrates limited understanding of  Solving K-Maps Creating Truth Table Electronic components (resistors, LEDs switches, logic gates)	Demonstrates some understanding of  □ Solving  K-Maps □ Creating Truth  Table □ Electronic  components  (resistors, LEDs  switches, logic  gates)	Demonstrates considerable understanding of □ Solving K-Maps □ Creating Truth Table □ Electronic components (resistors, LEDs switches, logic gates)	Demonstrates outstanding understanding of  Solving K-Maps Creating Truth Table Electronic components (resistors, LEDs switches, logic gates)
Circuit design and breadboard wiring. (Thinking / Inquiry)  Planning Work (Logisim File OR other planning documents) with evidence of sufficient organizational skills  Breadboard Organization & Layout  Colour Coding of Wires	Circuit design and breadboard wiring  Circuit not functional.  Wiring is not neat.  Wiring does not follow colour standards  Organized Logisim schematic	Circuit design and breadboard wiring  Circuit is somewhat functional.  Wiring is somewhat neat.  Wiring does not always follow colour standards  Organized Logisim schematic	Circuit design and breadboard wiring  Circuit is functional.  Wiring is neat.  Wiring always follows colour standards  All required functionality present.  Organized Logisim schematic	Circuit design and breadboard wiring  Wiring is exceptionally neat.  Wiring always follows colour standards  Organized Logisim schematic

Student Name:	Student #:

Logisim and virtual circuit correctly working (Application)/25	□ Some required functionality present and somewhat working for a small subset of test cases	□ Some required functionality present and working correctly	☐ Required functionality present and working correctly except for the enable bit	All required functionality present and working correctly with enable bit
Project Report	Project	Project	Project	Project
Documentation	Documentation:	Documentation:	Documentation:	Documentation:
	<ul> <li>Few or limited project report requirements met.</li> <li>Report not</li> </ul>	<ul> <li>□ Some project         report         requirements         met.</li> <li>□ Report</li> </ul>	<ul> <li>Most project report requirements met.</li> <li>Report neatly</li> </ul>	<ul> <li>□ All project         report         requirements         met.</li> <li>□ Report typed</li> </ul>
Requirements met	neatly	somewhat	typed/presented	and presented
(Communication)	typed/presented	neatly		extremely well.
	<ul> <li>Contains many spelling mistakes.</li> </ul>	typed/presented . Contains some spelling mistakes.	☐ Contains only a few spelling mistakes.	☐ Contains no spelling mistakes.