

1) For the circuit shown in Figure 1, place a  $2\text{ k}\Omega$  resistor in series with the emitter. Find the minimum value of  $h_{FE}$  required for the BJT to be in the saturation.

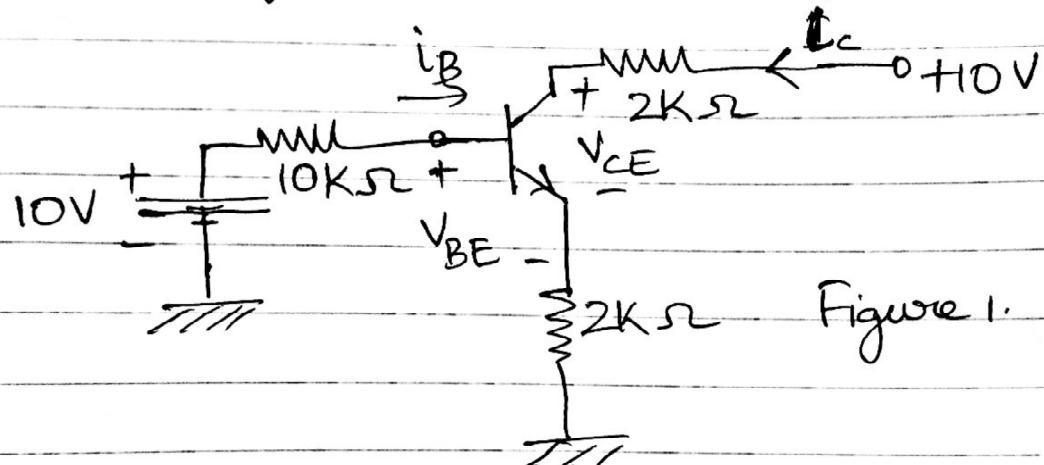


Figure 1.

2) For the circuit shown in Figure 2, suppose that  $V_{BB} = 3\text{ V}$ ,  $h_{FE} = 100$  for both BJTs,  $Q_1$  is ON, and  $Q_2$  is OFF. Given that  $R_1 = 4\text{ k}\Omega$  and  $R_2 = 2.5\text{ k}\Omega$ , find the range of values of  $R_E$  for which  $Q_1$  will remain ON and  $Q_2$  will remain OFF.

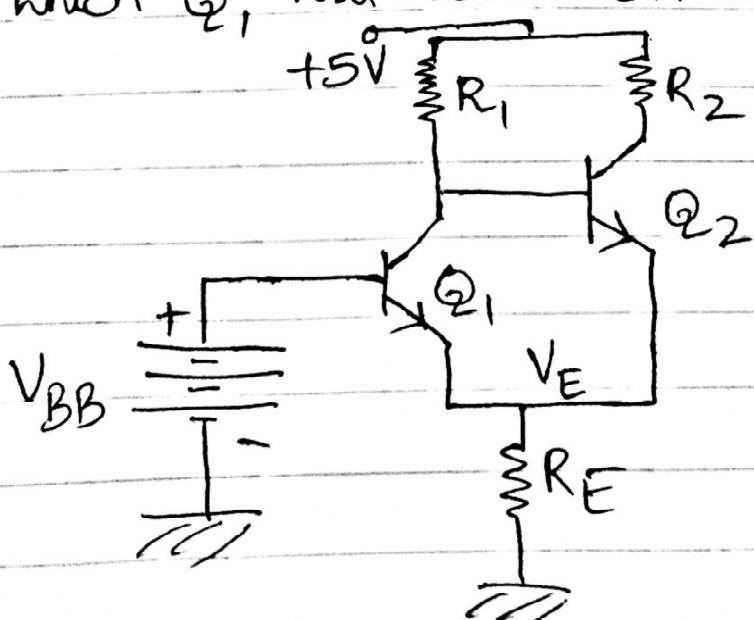
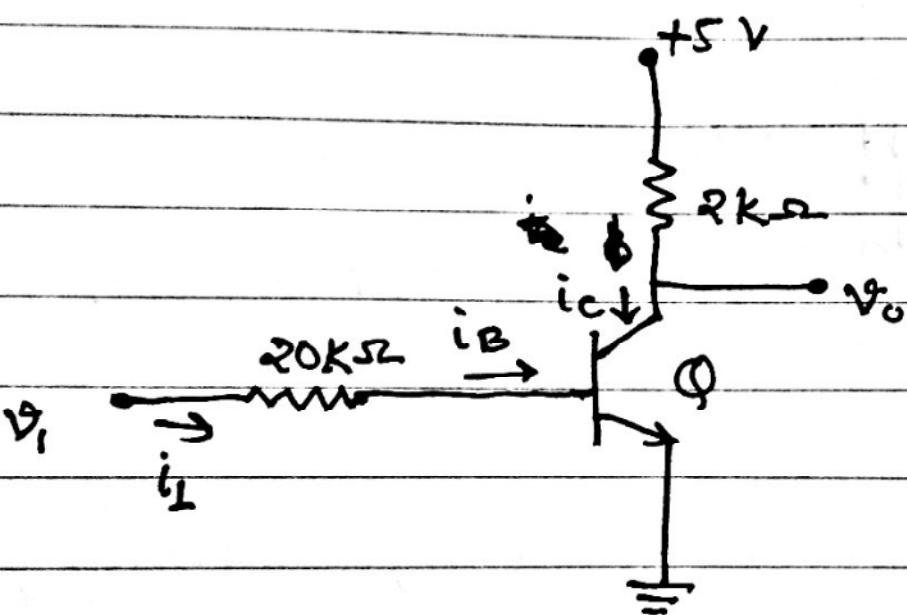


Figure 2

For the inverter given below, connect a  $50k\Omega$  resistor between the base of the BJT and second power supply of  $-5V$ . (The additional power supply will result in Q turning OFF faster after the input goes low by producing a negative base current which removes excess stored minority carriers from the base region of the BJT.) Find the minimum value of  $h_f$  required for the resulting inverter.



Q.4) For the inverter given below, connect a  $50\text{k}\Omega$  resistor between the base of the BJT and a second power supply of  $-5\text{V}$ . Suppose that the BJT has  $h_{FE} = 100$ . Find the noise margins  $NM_L$  and  $NM_H$  for the resulting inverter.

(Hint: find  $V_{IL}$  by determining the value of  $V_I$  for which  $V_{BE} = 0.5\text{V}$ , and find  $V_{IH}$  by determining the value of  $V_I$  for which  $V_{BE} = 0.8\text{V}$ )

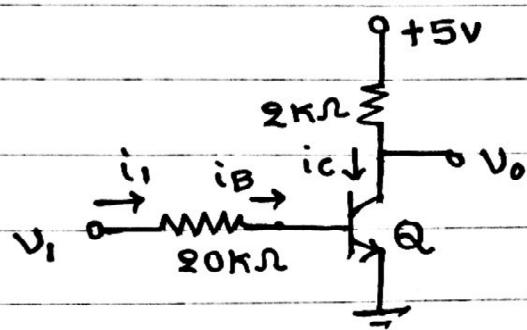


Fig. A BJT inverter.

Q.5

Determine the power dissipated by the NAND gate given below.

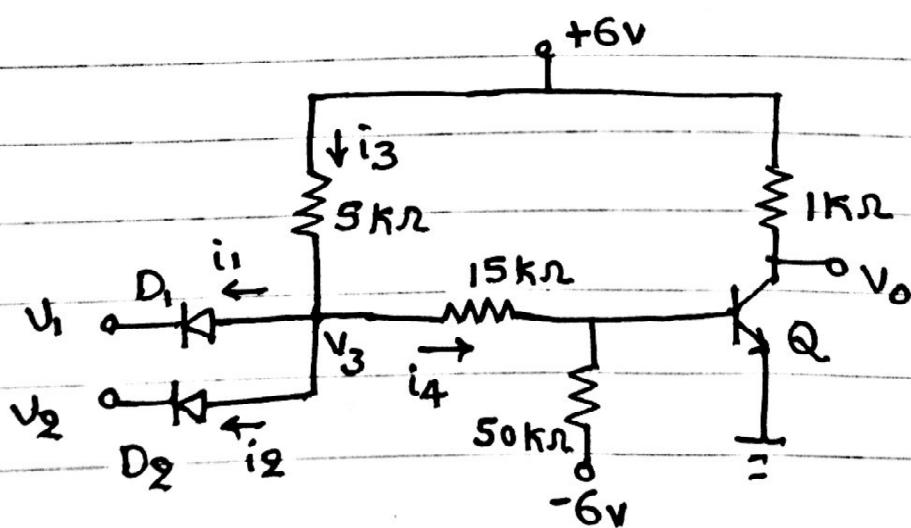


Fig. A DTL NAND gate