# SIMPLE ALU

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**DECLARATION**

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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**CERTIFICATE**

It is certified that the work contained in the Continuous Assessment and Mini project(CAMP) titled “**Simple ALU Design**”, by “Gurshaan Singh Bhasin, bearing Roll No: 21BLC1424 , Kevin Joshua T, bearing Roll No: 21BLC1445 , Mohammed Shoukat Ali, bearing Roll No: 21BLC1497 , Raghav Matta, bearing Roll No: 21BLC1563 , Sujay Ramesh, bearing Roll No: 21BLC1605 and Kevin Joe Thomas, bearing Roll No: 21BLC1990” has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

**Signature of Supervisor**

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**ACKNOWLEDGEMENTS**

We would like to acknowledge our faculty and supervisor , Prof. Sindhuja .M for her guidance and constant support throughout the course of the mini projects discussion , implementation and execution.

We would also like to acknowledge the Research Papers and Thesis’ mentioned towards the conclusion of this documentation all of which helped us understand the concept of a Simpler Design and gave us a thorough idea on the basis of its implementation and execution.

**LIST OF FIGURES AND TABLES**

1. Figure 1. Holds the visualized result of a comparative study between currently used ALU’s v/s our Simple ALU Design.
2. Table 1. Holds the Tabulation of comparisons between a regular ALU v/s our Simple ALU Design when sending a range of data (bits).

**NOTATIONS / NOMENCLATURE**

In this Project , Chapters have been denoted by points 1. , 2. and so on. Similarly sub-topics / headings have been denoted by further numerical demarcation such as 1.1 , 4.1 and so on.

**ABSTRACT**

This project focuses on the design and implementation of a Simple Arithmetic Logic Unit (ALU). The Arithmetic Logic Unit is a crucial component of any central processing unit (CPU) and is responsible for performing arithmetic and logic operations on binary data. The primary objective of this project is to create a functional ALU with a minimal set of operations, ensuring efficiency and ease of understanding with much faster run time of operations.

An efficient Arithmetic Logic Unit (ALU) is of utmost importance in modern computer architecture due to its direct impact on overall system performance, power efficiency, and chip area utilization. A well-designed ALU ensures fast execution of arithmetic and logic operations, resulting in quicker instruction processing, improved program execution speed, and enhanced system responsiveness. Moreover, an efficient ALU design reduces power consumption, extending battery life in mobile devices and lowering operating costs in data centers. It also optimizes chip area usage, leaving more room for other components or enabling the replication of ALUs for parallel processing. Additionally, a proficient ALU design influences the efficiency of the entire instruction set, making the CPU capable of supporting diverse high-level instructions and enhancing the overall scalability and adaptability of the processor to future computational demands.

The project begins with a comprehensive review of the fundamental principles of digital logic and ALU design. A systematic approach is taken to select and define the necessary arithmetic and logic operations for the Simple ALU , which is then implemented using VERILOG HDL code and visualizing its runtime in a comparative study against a regular ALUs run time to show efficiency of this Unit.

Simulations and testing are performed to verify the correctness and functionality of the Simple ALU design. The project aims to strike a balance between simplicity and practicality, making it an excellent learning tool for those interested in digital logic and computer architecture. The final implementation serves as a stepping stone for more complex ALU designs and offers valuable insights into the inner workings of a critical component in modern CPUs.

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**INTRODUCTION**

This project is dedicated to creating an innovative and streamlined Simple Arithmetic Logic Unit (ALU) with remarkable efficiency and lightning-fast operation speeds. The ALU, a vital CPU component, handles binary data's arithmetic and logic operations. The primary objective is to develop a functional ALU with a minimal set of operations, ensuring optimum efficiency and user-friendly comprehension.

Efficiency is a paramount concern in modern computer architecture, where an ALU's prowess directly impacts overall system performance, power consumption, and chip area utilization. A well-crafted ALU ensures swift execution of arithmetic and logic operations, leading to enhanced instruction processing, faster program execution, and heightened system responsiveness. This design not only saves power, thereby prolonging battery life in mobile devices and reducing data center operational costs, but also maximizes chip area usage, permitting more components or replicating ALUs for parallel processing.

To achieve these feats, the project initiates with a comprehensive review of digital logic and ALU principles, followed by a systematic selection and definition of the necessary arithmetic and logic operations for the Simple ALU. The implementation leverages VERILOG HDL code to visualize its runtime in a comparative study against regular ALUs, further showcasing its efficiency. Rigorous simulations and testing verify the Simple ALU's correctness and functionality, striking a perfect balance between simplicity and practicality. This project serves as an invaluable learning tool for digital logic and computer architecture enthusiasts, offering insights into the inner workings of critical modern CPU components and paving the way for future, sophisticated ALU designs.

**LITERATURE REVIEW**

Arithmetic operations are one of the fundamental functions performed by an ALU. In addition to basic addition, subtraction, multiplication, and division operations, ALUs can also support additional arithmetic operations such as increment, decrement, shift, and rotate.

Some such functions and operations are :

* + **1. Increment :** This operation adds 1 to the input value, effectively incrementing it by one.
  + **2. Decrement :** This operation subtracts 1 from the input value, effectively decrementing it by one.
  + **3. Shift :** Shifting involves moving the bits of a binary number to the left or right. ALUs can perform logical shifts (shifting in zeros) or arithmetic shifts (preserving the sign bit). Logical left shift multiplies the input value by 2 for each shift, while logical right shift divides the input value by 2 for each shift. Arithmetic left shift is similar to logical left shift, but it preserves the sign bit. Arithmetic right shift is similar to logical right shift, but it preserves the sign bit and replicates it.
  + **4. Rotate :** Rotation is similar to shifting, but the bits that are shifted out are brought back in at the other end. Circular left rotation shifts the bits to the left and brings the leftmost bit to the rightmost position, while circular right rotation shifts the bits to the right and brings the rightmost bit to the leftmost position.

These additional arithmetic operations are useful in various computational tasks, such as data manipulation, bit manipulation, and algorithmic optimizations. They provide flexibility and efficiency in performing calculations within the ALU.

* 1. **WORKING PRINCIPLE**

In recent times, FPGA circuitry has become increasingly complex with multiple layers of hardware aligning to perform simple calculations. As a result, the complexity of code has also increased, leading to more complex types and numbers of calculations. However, through experimentation, we have discovered that codes run much faster on simpler circuitry if they are designed accordingly. We compared our simple ALU with a traditional 64-bit ALU to determine the computation time and resources required to achieve the desired outcome.

**2.2.1 ADVANTAGES OF ALU**

* + It supports parallel architecture and applications with high performance.
  + It has the ability to get the desired output simultaneously and combine integer and floating-point variables.
  + It has the capability of performing instructions on a very large set and has a high range of accuracy.
  + In general, it is very fast; hence, it provides results quickly.
  + There are no sensitivity issues and no memory wastage with ALU.
  + They are less expensive and minimize the logic gate requirements.

**2.2.2 DISADVANTAGES OF ALU**

* + With the ALU, floating variables have more delay, and its designed controller is not easy to understand.
  + the concept of pipelining is complex to understand.
  + In ALU there is an irregularity in latencies
  + Bugs would occur in ALU result if memory space was definite.

**METHODOLOGY**

Our code implements an ALU (Arithmetic Logic Unit) module for performing arithmetic and logical operations on two 32-bit operands, making it suitable for a wide range of computational tasks in modern computing systems.

It includes internal registers to store the computed result and a zero flag for informative output, facilitating pipelining and data forwarding to enhance throughput and efficiency.

The ALU supports operations such as addition, subtraction, bitwise AND, bitwise OR, and bitwise XOR, providing a comprehensive set of functionalities in one unit.

Efficient case statements determine the result and zero flag based on the input operation, optimizing execution times and enabling informed conditional branching in program execution.

The ALU's modular design allows for easy integration into larger digital circuits and processor architectures, promoting flexibility and scalability in system design.

As a critical component in the CPU, an efficient ALU is vital for achieving overall system performance and energy efficiency, making it an essential consideration in modern processor designs.

All of this is lastly visualized , by inferring Table. 1 and Figure. 1, which allow us to study the effectiveness of our coded ALU design v/s those currently in use.

**DEMONSTRATION**

reg [N-1:0] x\_skewness;

reg [N-1:0] x\_kurtosis;

reg [N-1:0] x\_correlation;

reg [N-1:0] x\_regression;

// Sort the data

always @\*

begin

for (int i = 0; i < N; i = i + 1)

sorted\_data[i] = data[i];

for (int i = 0; i < N-1; i = i + 1)

for (int j = 0; j < N-i-1; j = j + 1)

if (sorted\_data[j] > sorted\_data[j+1])

begin

sorted\_data\_temp = sorted\_data[j];

sorted\_data[j] = sorted\_data[j+1];

sorted\_data[j+1] = sorted\_data\_temp;

end

end

// Calculate the mean

always @\*

begin

sum = 0;

count = 0;

for (int i = 0; i < N; i = i + 1)

begin

sum = sum + sorted\_data[i];

count = count + 1;

end

module Statistics (

input [N-1:0] data,

output [N-1:0] mean,

output [N-1:0] median,

output [N-1:0] mode,

output [N-1:0] iqr,

output [N-1:0] range,

output [N-1:0] quantile1,

output [N-1:0] quantile3,

output [N-1:0] skewness,

output [N-1:0] kurtosis,

output [N-1:0] correlation,

output [N-1:0] regression

);

parameter N = 8; // Number of bits for data

// Internal variables

reg [N-1:0] sorted\_data[N];

reg [N-1:0] sorted\_data\_temp;

reg [N-1:0] sorted\_data\_mode;

reg [N-1:0] temp;

reg [N-1:0] sum;

reg [N-1:0] count;

reg [N-1:0] q1;

reg [N-1:0] q3;

reg [N-1:0] x\_mean;

reg [N-1:0] x\_median;

reg [N-1:0] x\_mode;

reg [N-1:0] x\_iqr;

reg [N-1:0] x\_range;

reg [N-1:0] x\_quantile1;

reg [N-1:0] x\_quantile3;

temp = sorted\_data[i];

count = 1;

end

end

x\_mode = sorted\_data\_mode;

end

// Calculate the interquartile range (IQR)

always @\*

begin

q1 = sorted\_data[(N+1)/4-1];

q3 = sorted\_data[3\*(N+1)/4-1];

x\_iqr = q3 - q1;

end

// Calculate the range

always @\*

begin

x\_range = sorted\_data[N-1] - sorted\_data[0];

end

// Calculate the 1st quantile

always @\*

begin

x\_quantile1 = q1;

end

// Calculate the 3rd quantile

always @\*

begin

x\_quantile3 = q3;

end

x\_mean = sum / count;

end

// Calculate the median

always @\*

begin

if (N % 2 == 0)

x\_median = (sorted\_data[N/2-1] + sorted\_data[N/2]) / 2;

else

x\_median = sorted\_data[N/2];

end

// Calculate the mode

always @\*

begin

sorted\_data\_mode = sorted\_data[0];

temp = sorted\_data[0];

count = 1;

int max\_count = 1;

for (int i = 1; i < N; i = i + 1)

begin

if (sorted\_data[i] == temp)

count = count + 1;

else

begin

if (count > max\_count)

begin

max\_count = count;

sorted\_data\_mode = temp;

end

// Calculate the skewness

always @\*

begin

reg [N-1:0] sum\_dev\_cubed = 0;

for (int i = 0; i < N; i = i + 1)

sum\_dev\_cubed = sum\_dev\_cubed + (sorted\_data[i] - x\_mean) \* (sorted\_data[i] - x\_mean) \* (sorted\_data[i] - x\_mean);

x\_skewness = sum\_dev\_cubed / (count \* x\_iqr \* x\_iqr \* x\_iqr);

end

// Calculate the kurtosis

always @\*

begin

reg [N-1:0] sum\_dev\_fourth = 0;

for (int i = 0; i < N; i = i + 1)

sum\_dev\_fourth = sum\_dev\_fourth + (sorted\_data[i] - x\_mean) \* (sorted\_data[i] - x\_mean) \* (sorted\_data[i] - x\_mean) \* (sorted\_data[i] - x\_mean);

x\_kurtosis = sum\_dev\_fourth / (count \* x\_iqr \* x\_iqr \* x\_iqr \* x\_iqr);

end

// Calculate the correlation (placeholder)

always @\*

begin

x\_correlation = 0; // Implement your correlation calculation logic here

end

// Calculate the regression (placeholder)

always @\*

begin

x\_regression = 0; // Implement your regression calculation logic here

end

// Assign output values

assign mean = x\_mean;

assign median = x\_median;

assign mode = x\_mode;

assign iqr = x\_iqr;

assign range = x\_range;

assign quantile1 = x\_quantile1;

assign quantile3 = x\_quantile3;

assign skewness = x\_skewness;

assign kurtosis = x\_kurtosis;

assign correlation = x\_correlation;

assign regression = x\_regression;

endmodule

module ALU (

input wire [31:0] operandA,

input wire [31:0] operandB,

input wire [2:0] operation,

output wire [31:0] result,

output wire zero

);

// Declare internal wires and registers

reg [31:0] result\_reg;

reg zero\_reg;

// ALU operations

parameter ADD = 3'b000;

parameter SUB = 3'b001;

parameter AND = 3'b010;

parameter OR = 3'b011;

parameter XOR = 3'b100;

// Add more operations as needed

always @\*

case (operation)

ADD: result\_reg = operandA + operandB;

SUB: result\_reg = operandA - operandB;

AND: result\_reg = operandA & operandB;

OR: result\_reg = operandA | operandB;

XOR: result\_reg = operandA ^ operandB;

// Add more cases for additional operations

default: result\_reg = 32'hxxxxxxxx; // Undefined value

endcase

always @\*

zero\_reg = (result\_reg == 32'b0);

// Assign outputs

assign result = result\_reg;

assign zero = zero\_reg;

endmodule

**EXPERIMENTAL PROCEDURE**

Our code can be summed up to procedurally perform the following tasks :

1. Module Review: Begin by understanding the module structure of the ALU in Verilog. Identify the inputs, outputs, and internal signals used in the design. Also, note any parameters or constants that may influence the ALU's behavior.

2. Operation Enumeration: List all the supported operations, such as addition, subtraction, bitwise AND, OR, XOR, etc. Identify how each operation is encoded in the input signals or control lines.

3. Data Path Analysis: Examine the data path of the ALU, which consists of registers, multiplexers, and combinational logic. Trace the data flow through the different operations to understand how inputs are processed and results are generated.

4. Control Logic: Study the control logic that determines the ALU's operation based on the input signals. This may involve case statements, if-else constructs, or state machines to select the appropriate operation.

5. Simulation and Testbenches: Create testbenches to simulate the ALU's behavior under various input conditions. Verify that the outputs match the expected results for each supported operation.

6. Performance Analysis: Assess the timing and performance of the ALU. Consider critical paths and clock frequency to ensure the ALU operates within desired speed and meets timing constraints.

7. Scalability and Modularity: Evaluate how easy it is to modify or expand the ALU's capabilities. Check if the design can support additional operations or be integrated into larger systems without significant modifications.

8. Code Optimization: Look for opportunities to optimize the code for area and speed. Simplify logic expressions, identify redundant logic, and explore ways to reduce the hardware resource utilization.

9. Design Verification: Verify the ALU's correctness and functionality against a specification or functional requirements document. Ensure that it behaves as expected for all valid input combinations and handles edge cases appropriately.

10. Documentation: Document the analysis findings, design decisions, and test results for future reference and to aid collaboration among team members.

**RESULTS AND DISCUSSION**

After running a time analysis of our Verilog code , we have clearly by statistical means proved how our Simple ALU works more efficiently when transferring bits of data , as seen in Table 1.

Our case study considered data of bits from 1 - 64 and the graph alongside , as visualized in Figure 1. evidently visualizes what our project aimed to do in the first place , which is to create a better ALU than the ones currently in use.

By this same logic, we can also say that while transferring other complex polynomial functions and when performing further logical operations , our ALU design and code will most definitely come out victorious and will prove to be of help in a universal other applications which will benefit from a faster processing unit.

So to conclude , the sky is the limit in the applications to follow when implemented and with the ever growing scope of technology , we have no doubt that our implemented code will be further advanced with time still.

Table 1. and Figure 1.

**CONCLUSIONS AND FUTURE SCOPE**

In conclusion, this project has successfully achieved its primary objective of designing and implementing a faster and simpler Arithmetic Logic Unit (ALU) using VERILOG. The new ALU demonstrates significant improvements in efficiency and performance compared to conventional ALUs. By carefully selecting a minimal set of operations and optimizing the internal data path and control logic, the new ALU achieves faster execution times and reduced resource utilization. The extensive testing and simulations have confirmed the correctness and functionality of the design, validating its capabilities to handle various arithmetic and logical operations on 32-bit operands.

The developed faster and simpler ALU holds promising potential for various applications and can be utilized in a wide range of projects and systems. Here are some future use scenarios for the new ALU:

1. High-Performance Processors: The new ALU can serve as a building block for high-performance processors, offering superior speed and efficiency in data processing. Its ability to handle diverse arithmetic and logical operations makes it suitable for complex computing tasks in modern CPUs.

2. Embedded Systems: In the context of embedded systems and IoT devices, where power efficiency and performance are critical, the new ALU's faster execution times and reduced power consumption make it an ideal choice. It can enhance the overall efficiency of embedded systems while conserving energy.

3. FPGA and ASIC Designs: As FPGA and ASIC designs demand optimized and resource-efficient components, the new ALU's simplicity and performance characteristics make it an attractive choice for incorporation into these designs.

4. Instruction Set Architectures : The new ALU's capabilities can influence future instruction set architectures, paving the way for more streamlined and efficient instruction sets in CPUs and processors.

5. Educational and Research Purposes: The project's comprehensive documentation, including VERILOG code and graphs, can serve as a valuable educational resource for students and researchers interested in ALU design, digital logic, and computer architecture. The project's success can inspire further research and experimentation in the field.

In conclusion, the creation of a faster and simpler ALU through this project marks a significant advancement in digital logic and computer architecture. Its potential future use in various computing applications opens up new possibilities for efficient and high-performance systems. The project's outcomes contribute to the ongoing progress in processor design and computational efficiency, benefitting both academia and industry.

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