NIT-D:

→ Metal oxide Semiconductor field Effect transistor

MOSFET Cirail:

Limitation of BJT ?

6

1. It has low imput impedance because of forward biased emitter-base junction.
2. It has considerable noise level.

BJT

→ Current-controlled device

ve Ip controls **the** outpul current Ic

→ Three terminal

collector, Base, Emitter

→ Current conduction is due to both
é and holes. Lo
bipolar transistor.

Control currait
IB)

B

(Base

C (collector)

LBJT

E

Cemitter.

→

FET

It is a

three-terminal,
voltage-

controlled Semi-conducter device in which
current conduction is due to
the flow of
only
of

charg

e

Kinds

or holes.

input

one

The two

carriers sie election

ie. Vas controls the

output current

ID-

→

Three terminal

Drain (D)

Source (s)

gate (4)

~ FET com

→

perform better

amplification and

Switching

operatio

n.

Current conduction is due to

only

one

of

The two type charge carriers.

I or hole. So FET is called Unipolar tranchistor.

D (Drain)

(Control voltye)

NGS FET

(gu ide

´s

(Source .

six

advomila ge.

Smallerine Jain

→ The operation

The device depends on electric field intensity

→ High 9/p resistance

small

→ Power dissipation is **Son** all

Majority

Carrasier device

> No minority Carriers.

in the channel

→ No leakage current and temperature effect on the device is very less and

•. excellent thermal stability

60

→ FFT is Small in size, and easy to

- Smeller gair bandwidth product.

fabric ade.

JFET

FET

n.channel

MOSFE
T

Depletio
n

MOSFET

Enhancement

BIOSFET

p-chann

el

n-channel

p-channel.

Regions of FET:-

Source: It is the source of majority Carrier. i.e. It is the terminal by which majority carrier will be entering into device.

Drain: It drains the majority Carrier. It is the termina carrier will be leaving the device.

b y which majority

gate. It is the derminal which control majority Carriers moving from Source To dram.

channel: It is the region blow two gates.

hing of MOSPET S

Sym
bol.

C

in-chamel Enhancail MOSFET.

,

ग्

substrat

body

and

take p:type

body

contouc
h

[Nys
5744

Jannel.

Deflatio
n
région

.

-

how to is created?

mitel

Brady

Fer

interna

lly

Connected

So that it

channel

&MOSPET

diffuse tar on-lype

Semiconductor as in fig.

can be undered

as one terminal

(SiO2

(very then)

Was + Is.

to generile

current-

I work as an insuletor (no charge

passes thor

no current flow,

Current flows **from** Dram to Source:

→ Depletion region

VD S

m

the Chijl potabiel.

P low potential

→ no currut（!D20）

* V1s=0, no channel connecting

Souce & drain e ID=0

CEMOSFET generally off)

(رمان)

copacilor P. Pr

collect
charge

H
ol

of &
dielectric in
pla
ce

characla
uch

threshe
dd
voltage

restrict flow
of
charge. (insulator 9

trasfer
charict.
Grain charect.

ereity the layer of the TUFET

typ
e

P-typ
e

Substr
ity

insulated
ga
te

E.F (+ true,

> Vus +ve

∞

id J,

Reverse

Bies.

L

So depletion region
des means.

flow for Drain to
force.

charges can't
flow fr

↓

se Appliciter of a bettery
4/0 Oran and source no

currat flows. So

heal is to

H/W

gate

attached a

bellery

& source.

→s Induced n-channel.

Transf

er

es

chevecterislie,

130)

It is the plot How dram current and gale-source roldage.

(of Vas

<Naglth), there

is no induced channel. and Ip=0.

√us =

vas(th)

ID

Y(th) Yus

EMOSFET ON and induced channel

vas >

Vasth

width of induced channel increases hence

20 Des.

n-channel Depitelion

PloS FET:

mb
oli

PlOS
FET

D (Dram)

get
e

mistruition
/wooding

S WSource
+
NDS

ϥ
A
Metallic contact.
5102

m
m-chan n

Depletion
region
diffuse
n-channel.

0
Pritype
.

Substrate terminal

3. ways to operate:

DMOSFET

1.

45

148=0

Vas?

(ID,)

VDs → + V →→

To

flow

s.

was Vos tes ID tes, at certain point ring

Vos ID doesn't change

J-e Ip becomes constant.

b

The reverse

biaring depletion

region becomes

wider and wider, and channel becomes Thinner

위의)

21) V1p = -ve

you (54457")

دفتر

Vas

In this case. The -ne dermined at the gate foushes & towards

the substrate

p

where the é recombines & the holes, which results in Thinner diffuse channel s'e Io des.

=> vas

--ve =) Ip ties.

i Vas - +ve

(PFF9)

(320)

In this case.

The

the dermind at gate attracts the e

resulting in thicker

Vys = +ve = ID

Conclusio n-

Aes

diff use

channel.

Eg" for transconductance;

for Vas >
Vas

(s/p.

ID = X (145
√45 (84)) 2

curre
d.)

K =
ID (ou) (V1sen-(x))2.

ID

нере
з

Nus

* Drain characteristics:

The drain charactenstics is the graph of drain current (FD) .

and drain - Source voltage

(VDS).

from the

that most

grup

h,

it can be seen

of the part of

the

fa

curve is horizontal,

showing

constant drain current. Hence

in this past

of

curve the

EMOSFET behaves as a

contant

Current Source.

Q. The data sheet

for

an

Jo

-V1s = +154

Yus = + lov

Vos

E-MOSFET gives ID (m) 500mA at Vas = lov and Vas (th) = 1V. Determine the drain current for Vag = SV.

here Vascon) =
10V

1D = K (Vas - Vascon))2

Svo ma

26.17mA/v
2

(Vuscon) - Vasconi) 2
(10-11)2

k = ID
(on)

put values in E 0

ID = 6.17
(5V-1√) 2

ID = 98.7m A.

MOSFET as a

Switchi
n

MOSFET
characteristics:

t

[

tranfer charr.

is Dram characterskes. (ID VS VDs)

To (MA)

Drain charac.

203

101

lor

Vas = + ve

448=0

Vus = -ve

Y
P

Pinch off voltage.

JD3 > ID, >102

103 (1)

It is the minimum dram-source voltage at which the drain current becomes constant.

di) **Trompfer**

characteristics . (ID Vs Vas).

10 √45=0 ID = IDSS

we fuss is the value of

In when gate and Source

terminal are shorted. i-e Vac=0

i Vas-ve,

when Vas is -ve

Zelo

ii Var Ave

ID(MA)

Depletion (10 <IDSs)

Joss

Enhancement (507 Joss)

das

Nas (16)

Yas

(v)

In des below the value of loss till To reaches Nas – Vas (off).

when Vas is the, Is tes above the value of foss ·

Drain Current: To
contortance

outf
ent
curat

ID = IDSs /
2- Vas

Vas
(obb

>
2

Control variable (input voltage)

→ Shockley's Eq.
7

Consta
nt

MOSFET as a

Switch is. as ar

Dram characteristics of E. MOSFET; (ID VS VDs) for a given Vas

→ Cut-off Region (V4s < Voh)

In This regio n

7

Triode

Saturation region (Active region)

ID

Wihear ry!

The MOSFET

Switc h

ON

Yosk uste Vos > Vas-Vonh

+5V

+10v

cut-

Bass Von (off state)

Switch OFF

VDS 7

is is off state, as there is no induced channel ofw dram & Source

→ In both Lincer and Saturation region, the MOSFET is " ON state.

difference is that in Linear and ID & to the channel verkfance of the

→ In Saturation

→ j-e regio n , DS region :

The channel is continuous

as VDs > Vas – Yth the channel pinch off.

in a consent Drain current seto.

broadens of resulting in a

To understand the operation of MOS FET as a Switch, we Courider The Simple circuit as Fig. 1.

Qu

Vin

o

> In order to o forte & MOSSET as a Switch sil must be ofporated in cut-off and

linear region.

Rin

- Assume the device is initially OFF.

is vas > You (Switch ON).

Fig. 1.

No.

Lam p.

• Yout

Yas is made positive, the MOSFET enters in the linear region and The Switch is ON. This makes the light to turn

ON.

ii) Vas < Von (or ~0). (Switch off):

of the input vas in O or < Vah

The MOSFET enters in cut-off

state and turn off. This in turn will make the light to turn off.

of

MOSFET

!

من

VDD

ins

RD

mall **Signal**

operating model

purpo

se of

To

main

to find the

No

Hage

.

Small

signal

ac Current and ac

So Let us consider a ciruil

which

consist

o

f

both ac and

do source.

Nus

Voltages:

(3-Types)

lg

s

→ ac

voltage

Vus → DC

voltage

vas

↑

V

gs

Total

voltage

+ Vas

Similarly

Current:-

id ac current To do current

is total current

10=√1+3

0

2

Jus

(im

Saturation

regio)

is current id:

Now:

Kn

Constant

To = + km W (Vas -

V1)

2

L

threshold

voltage

cll

.

3

↳ transistor aspect ratio

je width-

lengt

h

je.

So,

total

Currat.

toll Voltage

· + kn W. ((Vgs

+ Vas) – V1)2

2 km W ((V1st Vgs) - V+) =

(a+b-c)2 = a2 + b2 + c2 + 2ab -2bc-2ca

um

considering

The ac

+ 2 √45 Vgs - 2 Vgs Vt – **2** V1 V1s]

compo nent,

id = + kn W. [2

Vas: Vga - 2 g x4]

id = √ Kn W [2 Ngs (V1s V2)]

2

k

ud = kn Wx [Vgo (V11s - V2]]

ac Current i'm a Small Signal of MOSFET

Trans conductance: (gm)

ac

id < output

Current

Trams & P

%

L/

P

Conductance

current

/pollage.

s

↑

So

impul ac

rottage.

trans

Conductance

(g

m)

I

m

Ld

.

V

50/ar

go

心

心

for small signal i = k n 1.

[Vgs (V1s - Vt)]

L

Jm = Km 1. [

Nas- Vt] |

L

vo Hage

gam: (Av)

voltage gam: output

voltage

Av =

Vars.

Ig

s

Ay = id ·

RD.

Vg

s.

Av = gm.

Ro

↑

voltage

gain

Input

voltage

Small Signal

Equivalent Model so

id

S

id

MOSFE
T

4

5

× 208

ϥ

Og
s

s

gm
vgs

gri
Vgs

ro

id=gm:
Vgs

valig
s

gm
=

Av = gm.
RUD

No.

Vo

i'd

without internet

Resistance *Yo*

Av=gm.

(Robb **Y1).**

with internal

resistance ro

Procedure for Small Signal Modelis

is Consider 3 terminals 4.D.S.

ii) There is no Connection of is Gate and Source and there is no

Current (impot) flowing b/w Gate and Source.

ii) But there is a current flow byw Dram and Source terminels.

- that is the constant current, why : in the saturation region

current is constant, so we can

Small signal current Source

Img s

represent it with constant

u're

id.

I ac.current.

Vo

ET Amplifier Configuration

:

↳ is Common

Source

ii) Common Gate

1) Common drain

Conce

pts

R

D

محمد

Configu

ration |

CS

i/

p

M

GND

gmerel 4- 4/p. D/P.

J

D

0/

P

СИ

GND

"/

P

/P

/P

ND

CD

P

o

n

Vi

Step
s:

Amplifier circuil is converted to
Small Signal

i) Get expression
from Rin, Ro.

iii) Get gam, Av.

Vis Vo.

model

190SFET Amplifier

Configuration : s.

Without Rs.

16 Common Source Configuration - I, with Re

→with Rs.

Risi
q

RD
.

Yo
is Small

Roi
g

sign
al

o

model:

Vo

M

Iesi

g

Input resistance : (Rim)

√ Rm =

Roig = ∞C

R12 V = V = ∞

i

Output resistance (Rrout) :

Rout = roll

RD

N>>RD

Rout = roRD.

Rout =

RD

No+RD

ro Ro-

801

Jur) voltage

Gain (Av) :

Av = **No.**

Av

V; =-iα (RD 1180) .

Vgs -gm (RD 1180)

s s

(4) as exput

Any Configuration with gate (4) as have Rm =00!! is current is Lew.

((R1llr.)] ("
+ x/~gn)

Over all gan :-

(4x)

G1 = No.

=

Vis
ig

Vi

-g
m)

-ia

(Rollru).

V

gs

UD

-Julholly..

;

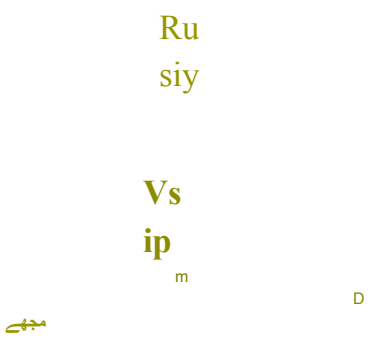
[Gr= – gm

(Rollro)

Yo

mmm

Source Configuration : (with Rg)



Input resistance: (Rim)

Rmn =

Roig =

= ∞

i output resistance: (Ro):

Ro=RD

iv)

Voltage gam

Ay =
Vo.
Vi Av=-id
RD
(Ar):

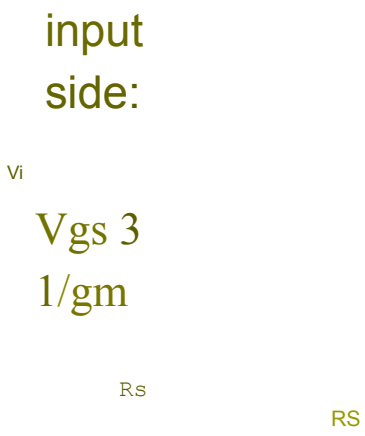
to get Vinput
consider
the imput
part: as

Ngs =
1/gm. v;

Roy
G

RD Yo

Vin Vsię


input
side:
Vi
Vgs 3
1/gm
Rs
RS

f

gm +

Rs

kle have used voltage divider formula, blich states that resistance in

that branch divided

Source

voltage.

Ngs

=

14

It gm

Rs

Vi

Vi Ngs (It gmRx) .

b y the sum **of** the resistance multiplied with

Av = -id . RD.

Ygs (It gm Rs).

Av = -gm RD.

(1+g m Rs)

& Common dram

(as d-**gm**) V gs

ia

Configur ation : 2

In Common drain Configuration the dram terminal is common between input and outfit. So Dram terminal connected **to** ground

outful and Gate as input.

Source an

*If there is a resistance connected to source termind, then hybrid T- model is considered for the

MOSF

ET

Vivere

ıp

w

Input resistance :

Ri

0

| Rm = Rsip = α

ig=0

all outful resistance:

Ro.

Ro=

[R2

=

Ro=

1/

g

m

11 Rs

- Res

>>>

//gm

(Ro=

(R2 =

gm Rs.

Y

gm

Y

gm

+

Rs

)

Ni

19

m

R

s

gm

Rs

(Vm = 0

Conclusion /

Remarks:

+ The CS amplifiers has infinite imput impedance and a moderately high output resistance, and a high voltage gain

↑

a es amplifier, but

Reducing Ro reduces the output resistances of unfortunately, the voltage gain is also reduced

desi

gn"

Alternate

resistance.

A GS

can be **employed** to reduce the outpul

es amplifier suffers from poor high frequency performance. as most transistor amplifiers du.

Stage gain

(AV):

Corridoring

the outfit fort

usi

ng

The

voltage

divider

formu

la

No =

Rs.

R2+

ɛ

Av

Rs.

Rs/gm

Vi

Xé **(an**

Airs V.)

• Ay = Rs.

R&+

Total / overall

gam:

Gu= Vo

Gv = Rs.

Rs+ /

Gy.

R

1

Yg

m