UNIT- V

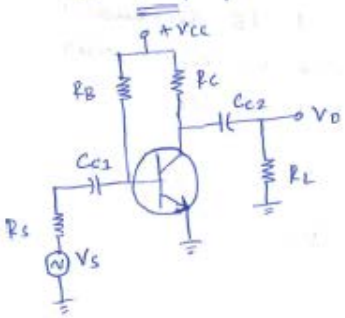
Transistor Biasing and Thermal Stabilization

Need for biasing, operating point, load line analysis, BJT biasing- methods, basic stability, fixed bias, collector to base bias, self bias, Stabilization against variations in V_{BE}, Ic, and β, Stability factors, (S, S', S''), Bias compensation, Thermal runaway, Thermal stability.

FET Biasing- methods and stabilization.

Load Line Analysis

CE Amplifier



* The basic function of a transistor is to do amplification.
* The weak signal is given to the transistor & amplified output is obtained from the collector.
* The process of raising the strength of weak signal without any change in its general shape is known as Amplification.
* A Transistor must be properly biased to operate as an amplifier.

* In CE amplifier the capacitor C_{c1} is a DC blocking capacitor & couples Ac input signal to the base of the Transistor.
* the capacitor C_{c2} is used to couple Ac output of the amplifier to load R_L

DC Analysis:

For DC, $f = 0$

$$X_c = \frac{1}{2\pi f c} = \frac{1}{0} = \infty$$

* The DC equivalent circuit is obtained by replacing all capacitors by open circuit.

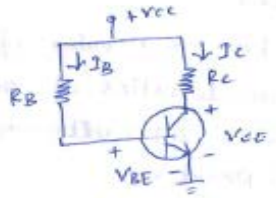


Fig: Dc Equivalent circuit

Load line:

* Applying KVL to the collector-Emitter circuit

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$V_{cc} - V_{CE} = I_c R_c$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad -①$$

* The eqn ① represent the DC load line with slope is $-\frac{1}{R_C}$ & 'y' intercept of $\frac{V_{CC}}{R_C}$.

* When $I_C = 0$ ie the transistor is in cutoff region

$$① \Rightarrow \quad 0 = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

$$\frac{V_{CE}}{R_C} = \frac{V_{CC}}{R_C}$$

$$V_{CE} = V_{CC}$$

* When $V_{CE} = 0$ ie the transistor is in saturation region

$$① \Rightarrow \quad I_C = -\frac{1}{R_C}(0) + \frac{V_{CC}}{R_C}$$

$$I_C = \frac{V_{CC}}{R_C}$$

* The two endpoints are $(V_{CC}, 0)$ & $\left(0, \frac{V_{CC}}{R_C}\right)$.

* A line passing through these points is called DC load line as the slope of this line depends on the DC load R_C.

Quiescent point

* Applying KVL to the base-Emitter circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

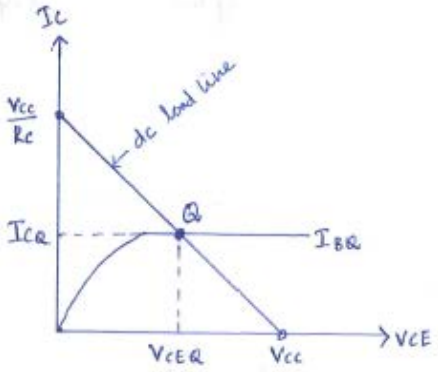


Fig: Load line and Q point

* This equation gives the value of base current.
* For this value of base current, o/p characteristics of the amplifier is plotted which intersects the DC load line at Q-point.
* Hence, Q point indicates quiescent (inactive, still) value of collector-Emitter voltage V_{CE} & collector current I_C.

Need for Biasing

* The Transistor can be operated in 3 regions: cutoff, active & Saturation by applying proper biasing conditions

Region of operation	Emitter-Base junction	collector-Base junction
cutoff	Reverse biased	Reverse biased
Active	forward biased	Reverse biased
Saturation	forward biased	Forward biased

* In order to operate Transistor in the desired region we have to apply external dc voltage of correct polarity & magnitude to the 2 junctions of the Transistor. This is called biasing of the Transistor.
* Dc biasing is used to establish proper values of I_C & V_{CE} called the Dc operating point (or) quiescent point (or) Q point.
* The value of I_C & V_{CE} is expressed interms of operating point (or) Q point.
* For faithful amplification, Q point must be selected properly.
* The fulfilment of the below condition is known as transistor biasing

1. proper zero signal collector current I_C
2. proper base-emitter voltage V_{BE}
3. proper collector-emitter voltage V_{CE}

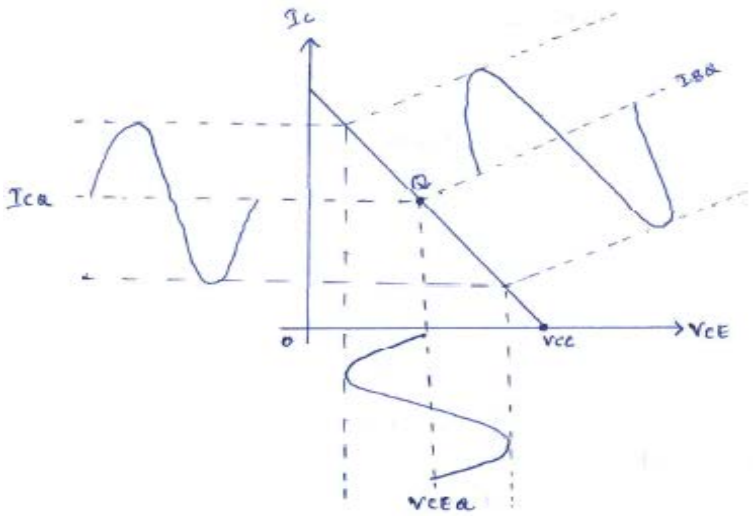
Selection of operating point:

* While fixing the Q-point it has to be seen that the o/p of the amplifier is a proper sinusoidal waveform for sinusoidal input without distortion.

* If an amplifier is not biased properly, it can go into saturation (or) cutoff when an i/p signal is applied.

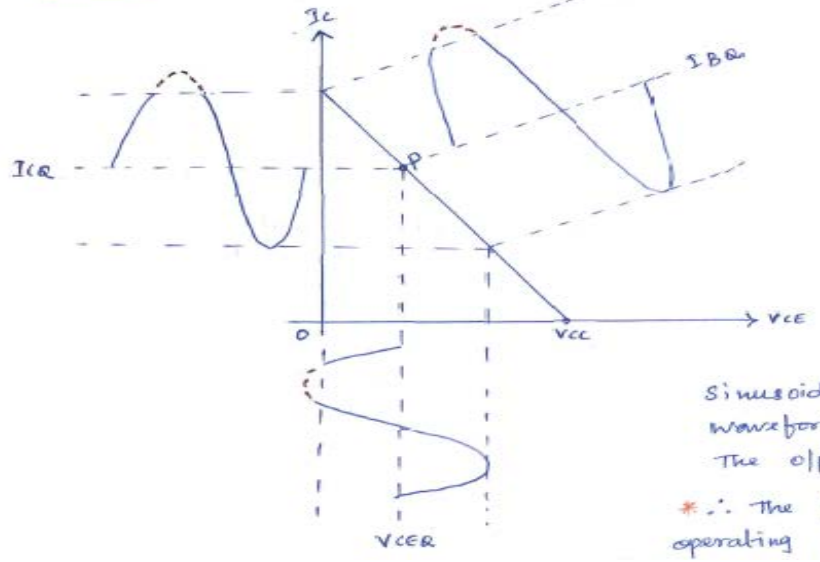
* By fixing the Q-point at different positions, we can observe the variation in I_C & V_{CE} corresponding to a given variation of I_B.

Case 1: When the Q point is located in the middle of the Dc load line (or) center of the Active region



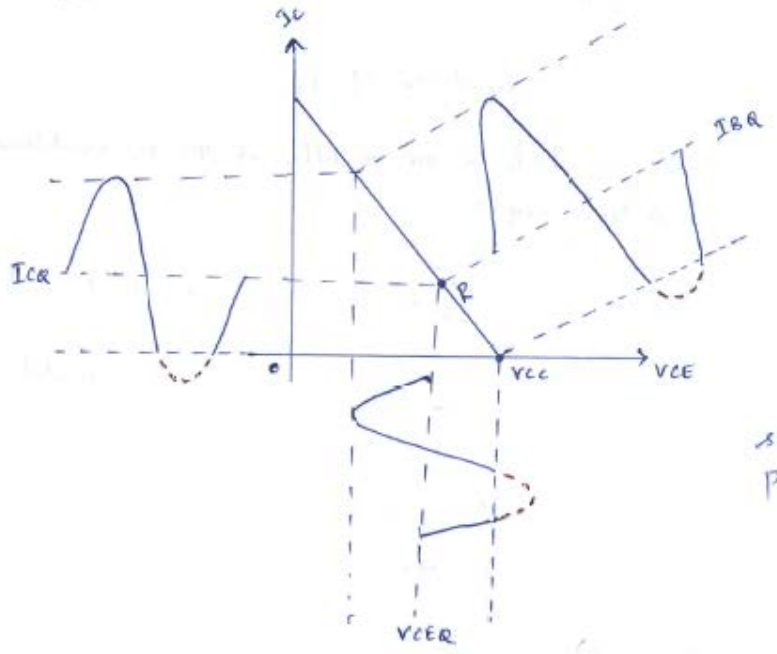
* The Q point is fixed at point Q.
* The o/p signal is sinusoidal waveform without any distortion
* Thus the point Q is the best operating point.

Case 2: When the Q point is located near the saturation region.



* The Q point is fixed at point P.
* The point P is very near to saturation region.
* The collector current I_C is clipped only at the positive half cycle.
* Even though the I_B varies sinusoidally, I_C is not a sinusoidal waveform i.e distortion is present at the o/p.
* ∴ The point P is not a suitable operating point.

Case 3: When the Q-point is located near the cut-off region



* The Q point is fixed at point R.
* The point R is very near to the cut off region.
* The Ic is clipped at the negative half cycle.
* So point R is also not a suitable Q point (or) operating point.

Variation of Q-point (or) Factors Affecting stability of Q-point

* The biasing circuit should be designed to fix the operating point (or Q-point at the centere of the active region.
* But only fixing of the operating point is not sufficent.
* While designing the biasing circuit, care should be taken so that the Q-point will not shift into an undesirable region (ie cutoff or saturat
* Designing the bias circuit to stabilize the Q-point is taken as bias stability.

Temperature

1) **I_{CO}**

* The flow of current in the circuit produces heat at the junctions.
* This heat increases the temperature at the junctions.
* We know that the minority carriers are temperature dependent
* They increase with Temperature.
* The increase in the minority carriers increases the leakage curre I_{CEO}.

$$\because I_{CEO} = (1+\beta) I_{CBO}$$

* I_{CBO} doubles for every 10°c rise in temperature.

* Increase in I_{CEO} is turn Increase in the collector current.

$$\therefore I_C = \beta I_B + I_{CEO}$$

* The increase in I_C further raises the temperature at the collector junction & the same cycle repeats.

* The excessive increase in I_C shifts the Q-point into the saturation region, changing the operating condition set by biasing circuit.

* The power dissipation at collector base junction is

$$P_D = V_C I_C$$

* The increase in the I_C increases the power dissipated at the collector junction.

* This in turn further increase the temperature of the junction & hence increase the I_C.

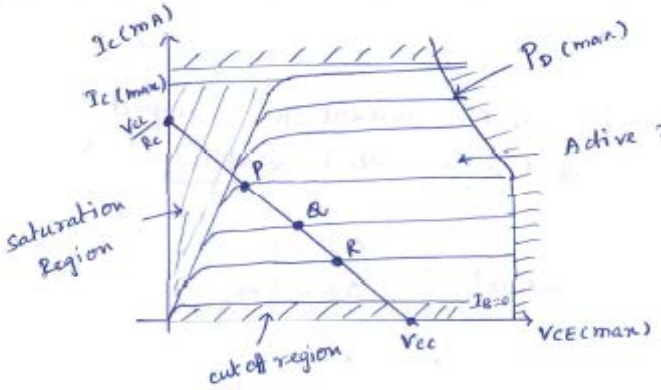
* The power is cumulative.

* The excess heat produced at the collector base junction may even burn & destroy the transistor.

* This situation is called Thermal runaway of the transistor.

* For any Transistor the maximum power dissipation is always a fixed value.

* This known as maximum power dissipation rating of a Transistor.



* The hyperbola give the maximum power dissipation for Transistor

* If this limit is crossed the device will fail.

2) V_{BE}

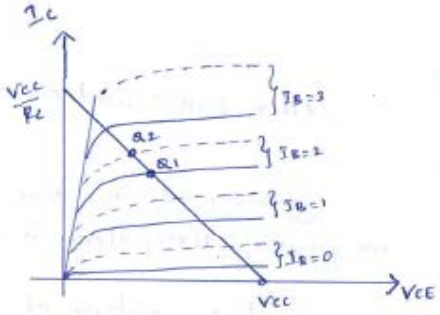
* V_{BE} changes with temperature at the rate of 2.5 mV/°C
* I_B depends upon V_{BE}
* I_B depends on V_{BE} & I_C depends on I_B. I_C depends on V_{BE}.
* $\therefore I_C$ changes with temperature due to changes in V_{BE}
* The change in I_C changes the Q-point.

3) β_{dc}

* It's also temperature dependent.
* As β_{dc} varies, I_c also varies, since $I_c = \beta I_B$
* The change in I_c change the Q-point.

Transistor current gain h_{FE} | β

* There are changes in the Transistor parameters among different units of the same type, same number.
* If we take 2 transistor units of same type & use them in the circuit, there is change in the β value in actual practice.
* The biasing circuit is designed according to the required β value.
* But due to change in β from unit to unit, the Q-point may shift.



* This fig: shows the CE o/p characteristics for 2 Transistor of the same type.
* The dashed characteristics are for a Transistor whose β is much larger than that of the Transistor represented by solid curves.

Stability Factors

S:

* The rate of change of collector current (I_c) with respect to collector leakage current (I_{CO}) at constant V_{BE} & β is called stability factor.

$$S = \frac{\partial I_c}{\partial I_{CO}}\Big|_{V_{BE} \& \beta \text{ constant}} = \frac{\Delta I_c}{\Delta I_{CO}}\Big|_{V_{BE} \& \beta \text{ constant}}$$

$$= \frac{\Delta I_{C2} - \Delta I_{C1}}{\Delta I_{CO2} - \Delta I_{CO1}}\Big|_{V_{BE} \& \beta \text{ constant}}$$

S':

* The rate of change of collector current (I_c) with respect to V_{BE} at constant I_{CO} & β is called stability factor S'.

$$S' = \frac{\partial I_c}{\partial V_{BE}}\Big|_{I_{CO} \& \beta \text{ constant}} = \frac{\Delta I_c}{\Delta V_{BE}}\Big|_{I_{CO} \& \beta \text{ constant}} = \frac{\Delta I_{C2} - \Delta I_{C1}}{\Delta V_{BE2} - \Delta V_{BE1}}\Big|_{I_{CO} \& \beta \text{ constant}}$$

S'':

* The rate of change of collector current (I_c) with respect to β at constant I_{CO} & V_{BE} is called stability factor S''.

$$S'' = \frac{\partial I_c}{\partial \beta}\Big|_{I_{CO} \& V_{BE} \text{ constant}} = \frac{\Delta I_c}{\Delta \beta}\Big|_{I_{CO} \& V_{BE} \text{ constant}}$$

$$= \frac{\Delta I_{c2} - \Delta I_{c1}}{\Delta \beta_2 - \Delta \beta_1}\Big|_{I_{CO} \& V_{BE} \text{ constant}}$$

The total change in collector current over a specified temperature range is obtained by expressing this change as the sum of individual changes due to 3 stability factors.

$$\Delta I_c = S \Delta I_{CO} + S' \Delta V_{BE} + S'' \Delta \beta$$

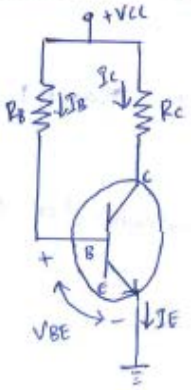
Questions:

1. What is the need for transistor biasing?
2. Define operating point of BJT.
3. Mention the importance of DC and AC Load lines.
4. Define stability factor.
5. Define the stability factors S′ and S″.
6. Explain the factors affecting stability of Q Point.
7. What is thermal runaway? How to overcome the problem of thermal runaway in BJT?

Different types of Biasing circuits / Various biasing Methods for BJT

1. Fixed Bias
2. Collector to Base Bias / Biasing with Feedback Resistor
3. Self Bias or Voltage Divider Bias

1. Fixed Bias / Base Bias



Dc Analysis:

* For Dc $f = 0$

$$X_C = \frac{1}{2\pi fC} = \frac{1}{0} = \infty$$

Collector current (I_C):

* Apply KVL to the Base-Emitter circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

* When V_{CC} & R_B are selected for a circuit I_B is fixed. Hence, the circuit is called Fixed bias circuit.

$$I_C = \beta I_B = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$$

Collector Emitter Voltage (V_{CE})

* Apply KVL to the collector - Emitter circuit

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$V_{CE} = V_{cc} - I_c R_c$$

Load line Analysis

* Apply KVL to the collector - Emitter circuit

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$I_c R_c = -V_{CE} + V_{cc}$$

$$I_c = -\frac{1}{R_c} V_{CE} + \frac{V_{cc}}{R_c}$$

* This eqn represents dc load line with slope of $-\frac{1}{R_c}$ & y-intercept of $\frac{V_{cc}}{R_c}$.

* When $I_c = 0$ i.e. the transistor is in cutoff region

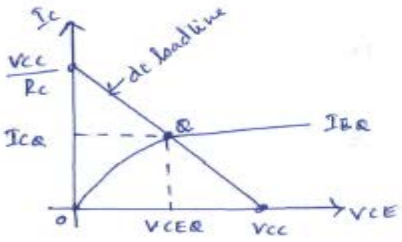
$$V_{CE} = V_{cc}$$

* When $V_{CE} = 0$ i.e. the transistor is in saturation region

$$I_c = \frac{V_{cc}}{R_c}$$

* Thus the 2 end points are $(V_{cc}, 0)$ & $\left(0, \frac{V_{cc}}{R_c}\right)$
  (x) (y) — $x \downarrow V_{CE}$, $y \downarrow I_c$

* By joining this 2 end points Dc load line is drawn.



* The saturation current for the circuit is $I_{c\,sat} = \frac{V_{cc}}{R_c}$.

Stability factors

S:

$$S = \frac{\partial I_c}{\partial I_{co}} \Big|_{V_{BE} \& \beta \text{ constant}} \quad (\text{or}) \quad \frac{\Delta I_c}{\Delta I_{co}} \Big|_{V_{BE} \& \beta \text{ constant}}$$

* We know that

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

* No collector current present in this equation. So $\frac{\partial I_B}{\partial I_c} = 0$ — (1)

* We know I_c

$$I_c = \beta I_B + (1+\beta) I_{co}$$

* differentiate I_c with respect to I_c we get

$$\frac{\partial I_c}{\partial I_c} = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta) \frac{\partial I_{co}}{\partial I_c} \qquad \because \frac{\partial I_c}{\partial I_{co}} = S$$

$$1 = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta) \times \frac{1}{S}$$

$$1 - \beta \frac{\partial I_B}{\partial I_c} = \frac{1+\beta}{S}$$

$$\boxed{S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_c}}} \quad -②$$

* Substitute ① in ②

$$S = \frac{1+\beta}{1-\beta(0)}$$

$$\boxed{S = 1+\beta}$$

S' :

$$S' = \frac{\partial I_c}{\partial V_{BE}} \Big|_{I_{co} \text{ \& } \beta \text{ constant}} \quad (\text{or}) \quad \frac{\Delta I_c}{\Delta V_{BE}} \Big|_{I_{co} \text{ \& } \beta \text{ constant}}$$

* W.k.T

$$I_c = \beta I_B + (1+\beta) I_{co}$$

* Substitute I_B in I_c

$$I_c = \beta \left(\frac{V_{cc} - V_{BE}}{R_B} \right) + (1+\beta) I_{co}$$

$$I_c = \frac{\beta V_{cc}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{co} \quad -③$$

* differentiate w.r.to V_{BE}

$$\frac{\partial I_c}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0$$

$$\boxed{S' = -\frac{\beta}{R_B}}$$

Relation between S & S'

$$S = 1+\beta \qquad S' = \frac{-\beta}{R_B}$$

In S' Multiply numerator & denominator by $(1+\beta)$ we get

$$S' = \frac{-\beta(1+\beta)}{R_B(1+\beta)} = \frac{-\beta S}{R_B(1+\beta)} \qquad \because S = 1+\beta$$

S'' :

$$S'' = \frac{\partial I_C}{\partial \beta}\Big|_{V_{BE} \& I_{CO} \text{ constant}} = \frac{\Delta I_C}{\Delta \beta}\Big|_{V_{BE} \& I_{CO} \text{ constant}}$$

From (3)

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CO}$$

differentiate w.r. to 'β'

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} + I_{CO} \qquad \because I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= I_B + I_{CO} \qquad \because I_B \gg I_{CO}$$

$$= I_B + 0 \qquad \because I_B = \frac{I_C}{\beta}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}$$

$$\boxed{S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}}$$

Relation b/w S & S''

$$S = 1+\beta \qquad S'' = \frac{I_C}{\beta}$$

In S'' Multiply Numerator & denominator by $(1+\beta)$ we get

$$S'' = \frac{I_C(1+\beta)}{\beta(1+\beta)} = \frac{I_C S}{\beta(1+\beta)} \qquad \because S = 1+\beta$$

Advantages :

* Simple circuit which uses very few components.
* The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B. Thus it provides maximum flexibility in the design.

Disadvantages

1. Thermal stability is not provided by this circuit. so the operating point is not maintained.

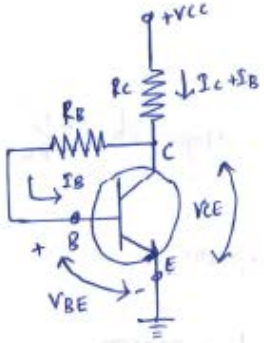
$$I_C = \beta I_B + I_{CEO}$$

2. Since $I_C = \beta I_B$ & I_B is already fixed; I_C depends on β which changes unit to unit & shifts the operating point.

The stabilization of operating point is very poor in the fixed bias circuit. Because of this reason the fixed bias circuit need some modifications.

In the modified circuit, R_B is connected b/w collector & base. Hence the circuit is called collector to base bias circuit.

2. Collector to Base Bias / Biasing with Feedback Resistor



* It's an improvement over the fixed bias method
* The resistor is connected b/w the base & the collector of the transistor. Hence the circuit is called collector to base bias circuit.
* Then I_B flows through R_B & $(I_C + I_B)$ flows through the R_C.

Dc Analysis

* For DC $f = 0$

$$X_C = \frac{1}{2\pi f C} = \frac{1}{0} = \infty$$

Collector Current I_C

* Apply KVL to the base - Emitter circuit

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B((\beta+1)R_C + R_B) - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B\left((\beta+1)R_C + R_B\right)$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_C}}$$

* If there is a change in β due to piece to piece variation b/w Transistors, Then I_C tends to increase. As the result voltage drop across R_C increases.
* The supply voltage V_{CC} is constant, due to increase in $I_C R_C$, V_{CE} decreases. Due to reductic in V_{CE}, I_B decreases. This I_B reduction is lead to increase I_C.

W.K.T $I_B = \frac{I_c}{\beta} \Rightarrow I_c = \beta I_B$

$$I_c = \beta \left[\frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_c} \right]$$

Collector Emitter Voltage V_{CE}

* Apply KVL to the collector - Emitter circuit

$$V_{cc} - (I_B + I_c) R_c - V_{CE} = 0$$

$$V_{CE} = V_{cc} - (I_B + I_c) R_c$$

Load Line Analysis

* Apply KVL to the collector - Emitter circuit

$$V_{cc} - (I_B + I_c) R_c - V_{CE} = 0$$

* Assume $I_B + I_c \simeq I_c$

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$I_c = -\frac{1}{R_c} V_{CE} + \frac{V_{cc}}{R_c}$$

* The equation represents a DC Load line with slope of $-\frac{1}{R_c}$ & y-intercept $\frac{V_{cc}}{R_c}$.

* When $I_c = 0$ i.e Transistor is in cut-off region

$$V_{CE} = V_{cc}$$

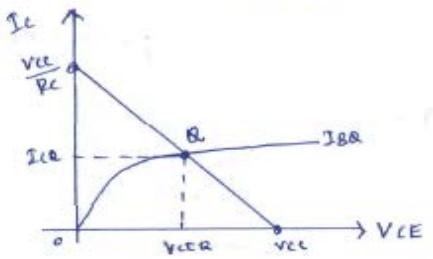
* When $V_{CE} = 0$ i.e Transistor is in saturation region

$$I_c = \frac{V_{cc}}{R_c}$$

* Thus the 2 end points are $(V_{cc}, 0)$ & $(0, \frac{V_{cc}}{R_c})$. by joining the 2 end points DC Load line is drawn.

* From Base - Emitter circuit

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_c}$$



The saturation current for the circuit is $I_{c\,sat} = \frac{V_{cc}}{R_c}$

Stability Factors

S:

* Apply KVL to the base - Emitter junction

$$V_{CC} = I_C R_C + I_B (R_C + R_B) + V_{BE}$$

* When I_B changes by ∂I_B & I_C changes by ∂I_C There is no effect on V_{CC} & V_{BE}

* So the equation becomes

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B) + 0$$

$$\partial I_B (R_C + R_B) = -\partial I_C R_C$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B} \quad -(1)$$

* substitute (1) in S

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_C+R_B}\right)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

* The collector - Base bias circuit is having Lesser stability factor than fixed bias circuit.

* Hence the circuit provides better stability than fixed bias circuit

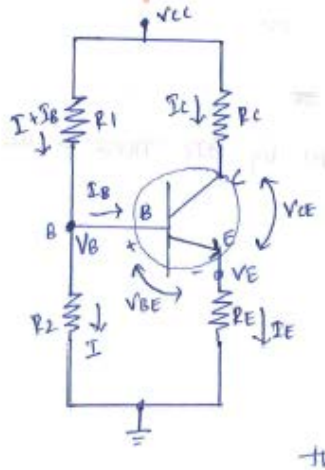
S':

$$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$$

S'':

$$S'' = \frac{I_C}{\beta}\left(\frac{S}{1+\beta}\right)$$

3. Voltage Divider Bias / Self Bias / potential divider Bias



* The biasing is provided by R_1, R_2 & R_E.
* The resistors R_1 & R_2 act as a potential divider giving a fixed voltage to point B ie base.
* If I_C increases due to change in temperature or β, the I_E also increases & the voltage drop across R_E increases, decreasing the V_{BE}.
* Due to reduction in V_{BE}, I_B & I_C also reduced.
* ∴ We can say that negative feedback exist in the Emitter bias circuit.

* The voltage across R_2 is the base voltage V_B.
* Apply voltage divider theorem to find V_B we get

$$V_B = \frac{R_2 (I)}{R_1(I+I_B) + R_2(I)} \times V_{cc}$$

∵ $I >> I_B$ so we can omit I & I_B

So

$$V_B = \frac{R_2}{R_1 + R_2} V_{cc}$$

* The voltage across R_E is V_E

$$V_E = I_E R_E = V_B - V_{BE}$$

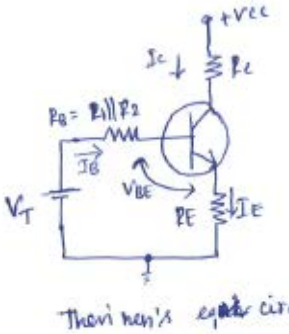
$$\therefore I_E = \frac{V_B - V_{BE}}{R_E}$$

* Apply KVL to the collector - Emitter circuit we get

$$V_{cc} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore V_{CE} = V_{cc} - I_C R_C - I_E R_E$$

Modified circuit



Thevenin's equivalent circuit

* Here, R_1 & R_2 are replaced by R_B & V_T, where R_B is the parallel combination of R_1 & R_2 & V_T is the Thevenin's voltage.
* R_B is calculated as $R_B = \frac{R_1 R_2}{R_1 + R_2}$

* Apply KVL to the Base - Emitter junction

$$V_T = I_B R_B + V_{BE} + I_E R_E \qquad \because I_E = I_C + I_B$$

$$= I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$= I_B R_B + V_{BE} + I_C R_E + I_B R_E$$

$$V_T = I_B (R_B + R_E) + V_{BE} + I_C R_E$$

$$V_{BE} = V_T - I_B (R_B + R_E) - I_C R_E$$

Stability Factors

S

* Here the Therinen's voltage V_T is given by

$$V_T = \frac{R_2 V_{cc}}{R_1 + R_2}$$ & R_1 & R_2 replaced by R_B.

* Apply KVL to the base - Emitter junction

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E \quad — (1)$$

*differentiate eqn (1) w.r. to I_C & V_{BE} to be independent of I_C we get

$$0 = \frac{\partial I_B}{\partial I_C} R_B + 0 + \frac{\partial I_B}{\partial I_C} R_E + \frac{\partial I_C}{\partial I_C} R_E$$

$$0 = \frac{\partial I_B}{\partial I_C} (R_B + R_E) + R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \quad — (2)$$

* W.K.T

$$S = \frac{1+\beta}{1 - \beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1 - \beta\left(\frac{-R_E}{R_B + R_E}\right)} = \frac{1+\beta}{1 + \beta\left(\frac{R_E}{R_B + R_E}\right)}$$

* Take LCM

$$S = \frac{(1+\beta)(R_B + R_E)}{R_B + R_E + \beta R_E} = \frac{(1+\beta)(R_B + R_E)}{R_B + (1+\beta) R_E}$$

* Dividing each term by R_E we get

$$S = \frac{(1+\beta)\left(\frac{R_B}{R_E} + \frac{R_E}{R_E}\right)}{\frac{R_B}{R_E} + (1+\beta)\frac{R_E}{R_E}} = \frac{(1+\beta)\left(1 + \frac{R_B}{R_E}\right)}{(1+\beta) + \frac{R_B}{R_E}}$$

* The ratio R_B/R_E controls value of stability factor S.
* If $R_B/R_E \ll 1$ Then $S = \frac{1+\beta}{1+\beta} = 1$

S'

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big| \; I_{CO} \& \beta \text{ constant}$$

* W.K.T

$$I_C = (1+\beta) I_{CO} + \beta I_B \quad — (1)$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E \quad — (2)$$

$$V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C \quad — (3)$$

* By rewriting the eqn (1) interms of I_B

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \quad — (4)$$

* Substitute I_B in eqn (3) we get

(3) $V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C$

$$= V_T - (R_E + R_B) \left[\frac{I_C - (1+\beta) I_{CO}}{\beta} \right] - R_E I_C$$

$$= V_T - \frac{(R_E + R_B) I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} - R_E I_C$$

* Take the common terms Outside

$$V_{BE} = V_T - \left[\frac{(1+\beta) R_E + R_B}{\beta} \right] I_C + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} \quad — (5)$$

* differentiate eqn (5) w.r.to V_{BE}

$$\frac{\partial V_{BE}}{\partial V_{BE}} = 0 - \left(\frac{(1+\beta) R_E + R_B}{\beta} \right) \frac{\partial I_C}{\partial V_{BE}} + 0$$

$$1 = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$$S' = \frac{-\beta}{R_B + (1+\beta) R_E}$$

S'':

$$S'' = \frac{\partial I_C}{\partial \beta} \Big| \; I_{CO} \& V_{BE} \text{ as constants}$$

$$V_{BE} = V_T - \frac{(R_B + (1+\beta)R_E)I_C}{\beta} + \underbrace{\left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right]I_{CO}}_{V'}$$

$$= V_T - \frac{[R_B + (1+\beta)R_E]I_C}{\beta} + V' \quad -(6)$$

* We can rewrite the eqn (6) interms of I_C

$$\frac{[R_B + (1+\beta)R_E]I_C}{\beta} = V_T - V' - V_{BE}$$

$$I_C = \frac{(V_T - V' - V_{BE})\beta}{R_B + (1+\beta)R_E} \quad -(7) \Rightarrow \frac{u}{v} \text{ format}$$

↳ $\frac{v\,du - u\,dv}{v^2}$

* differentiating eqn (7) w.r.to β

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + (1+\beta)R_E\,(V_T - V' - V_{BE}) - \beta(V_T - V' - V_{BE})R_E}{(R_B + (1+\beta)R_E)^2}$$

* Multiply numerator & denominator by $(1+\beta)$ & β

$$= \frac{(1+\beta)(R_B + R_E)(V_T - V' - V_{BE})\beta}{\beta(1+\beta)[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]}$$

S $\quad$ I_C

$$\frac{\partial I_C}{\partial \beta} = \frac{S}{\beta(1+\beta)} \times I_C$$

$$S'' = \frac{I_C\,S}{\beta(1+\beta)}$$

Advantages

* The stability factor S for voltage divider bias is less as compared to another biasing circuit
* So this circuit is more stable & hence it's most commonly used.

Load line Analysis for voltage divider bias

* Apply KVL to the collector-Emitter circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

* Assume $I_E \simeq I_C$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$I_C = -\frac{1}{R_C + R_E} V_{CE} + \frac{V_{CC}}{R_C + R_E}$$

* This equation represents the dc load line with slope of $-\frac{1}{R_C + R_E}$ & y-intercept of $\frac{V_{CC}}{R_C + R_E}$

* When $I_C = 0$ i.e the transistor is in cut-off region

$$V_{CE} = V_{CC}$$

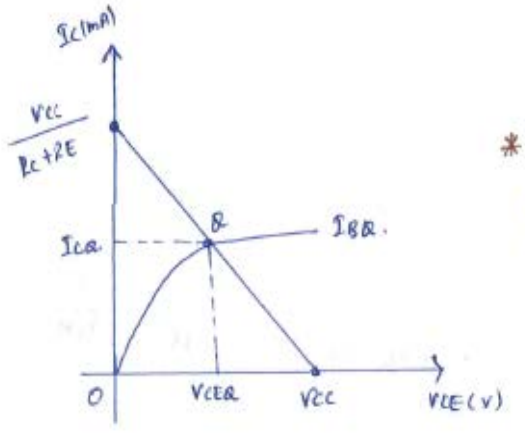
* When $V_{CE} = 0$ i.e the transistor is in saturation region

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

* Thus the 2 end points are $(V_{CC}, 0)$ & $\left(0, \frac{V_{CC}}{R_C + R_E}\right)$ By joining these 2 end points, a DC load line is drawn.

* From the base-emitter circuit

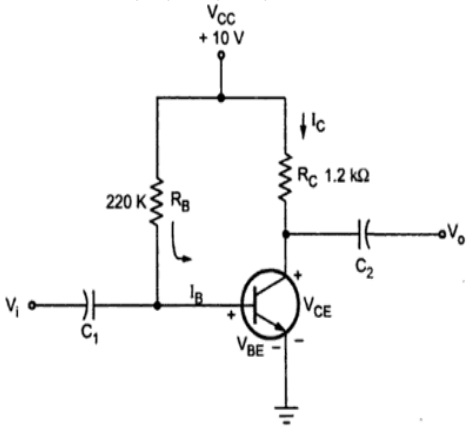
$$I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta) R_E}$$



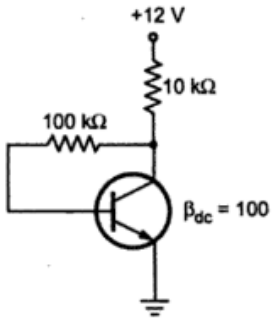
* The saturation current for the circuit is $I_{C\,sat} = \frac{V_{CC}}{R_C + R_E}$

Questions:

1. What are the different types of biasing techniques for BJT?
2. Draw a Fixed Bias Circuit of BJT. Derive the three stability factors.
3. What are the advantages and disadvantages of Fixed Bias Circuit?
4. With neat diagram, explain Collector to Base Bias Circuit of BJT. Derive S, S′ and S″.
5. Mention the advantages and disadvantages of Collector to Base Bias Circuit.
6. Which biasing method provides more stabilization against the three types of biasing methods? Why?
7. With neat diagram, explain Voltage Divider Bias Circuit of BJT. Derive S, S′ and S″.
8. Write the advantages and disadvantages of Voltage Divider Bias.
9. For the circuit shown in Figure, Calculate I_B, I_C, V_{CE}, V_B , V_C and V_{BC}. Assume that V_{BE} = 0.7V and β = 50.



10. Calculate the Q point values (I_C and V_{CE}) for the circuit shown in the Figure.



Bias compensation / Methods of stabilizing the Q-point

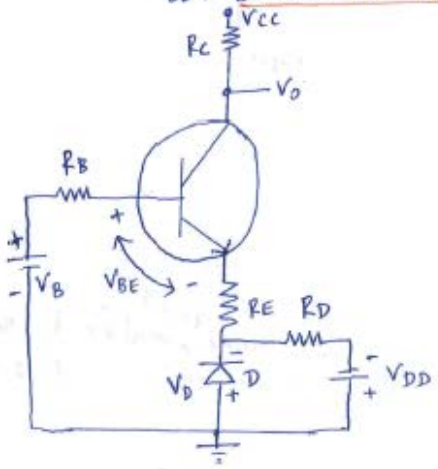
* The compensation Techniques uses Temperature sensitive devices such as diodes, Transistors. Thermistors etc.. to maintain the operating point constant.

1. Diode compensation Techniques
   1. compensation for VBE
      a) Diode in Emitter circuit
      b) Diode in Voltage Divider circuit
   2. compensation for Ico
2. Thermistor compensation Technique
3. Sensistor compensation Technique

1. Diode compensation Technique

1. Compensation for V_{BE}

a) Diode in Emitter circuit



* Here, separate supply VDD is used to keep diode in Forward bias condition.

* If the diode & Transistor are of same material, the voltage across the Diode will have the same temperature coefficient (−2.5 mV/°C) as the V_{BE}.

* So the V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D & $\partial V_D \simeq \partial V_{BE}$, the change tend to cancel each other.

* We know,

$$V_{BE} = V_T - \left[\frac{R_B + (1+\beta)R_E}{\beta}\right] I_C + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

$$\left[\frac{R_B + (1+\beta)R_E}{\beta}\right] I_C = V_T - V_{BE} + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

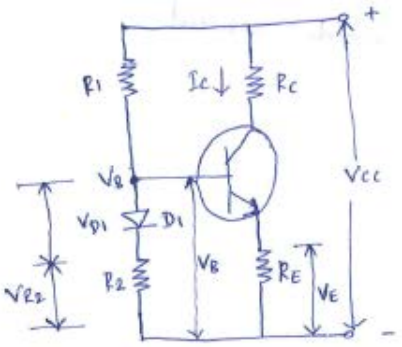
$$I_C = \frac{\beta\left[V_T - V_{BE}\right] + \beta\left[\frac{(R_E + R_B)(1+\beta)}{\beta} I_{CO}\right]}{R_B + (1+\beta)R_E}$$

* We modify the equation

$$I_C = \frac{\beta [V - (V_{BE} - V_D)] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

* I_C will be insensitive to variations in V_{BE}.

b) Diode in voltage Divider circuit



* Here, the diode is connected in series with resistance R_2 in the voltage divider circuit & it is in forward bias condition.

* We derived for voltage divider bias

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

also $I_E = \frac{V_E}{R_E}$ & $I_C \simeq I_E$.

$$I_C \simeq \frac{V_B - V_{BE}}{R_E} \quad — (1)$$

* When V_{BE} change with temperature I_C also changes.

* The voltage at the base V_B is now

$$V_B = V_{R2} + V_D \quad — (2)$$

* sub eqn (2) in (1)

$$(1) \Rightarrow I_C \simeq \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

* If the diode & the Transistor are of the same type & material, the voltage across the diode will have the same temperature coefficient ($-2.5\ mV/°C$) as the V_{BE}.

* So the V_{BE} changes by ∂V_{BE} with change in temperature. V_D changes by ∂V_D & $\partial V_D \simeq \partial V_{BE}$. The change tend to cancel each other.

* The collector current as

$$I_C \simeq \frac{V_{R2}}{R_E}$$

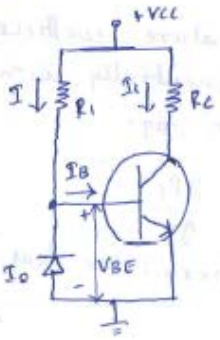
* Which is unaffected due to change in V_{BE}.

* The biasing is provided by R_1, R_2 & R_E.

* The change in V_{BE} due to temperature are compensated by changes in the diode voltage which keeps I_C stable at Q-point.

2. Compensation for I_{CO} / Diode compensation for germanium Transistor

* In case of Ge, changes in I_{CO} with Temperature are comparatively larger than Si Transistor.



* It plays more role in I_C stability than the change in V_{BE}.
* It offers stabilization against variation in I_{CO}.
* Here, the diode is kept in reverse bias condition
* In reverse bias condition the current flowing through diode is only the leakage current (I_O).

* If the diode & the Transistor are of the same type & material, The leakage current I_O of the diode will increase with temperature at the same rate as the collector leakage current I_{CO}.

$$I = \frac{V_{CC} - V_{BE}}{R_1} \quad \& \quad I = I_B + I_O$$

$$\therefore I_B = I - I_O \quad \text{---} (1)$$

* For Ge Transistor $V_{BE} = 0.2\ V$, which is very small & neglecting change in V_{BE} with temperature.

* We can write

$$I \simeq \frac{V_{CC}}{R_1} \simeq \text{constant}$$

* We know

$$I_C = \beta I_B + (1+\beta) I_{CO} \quad \text{---} (2)$$

Sub (1) in (2)

$$(2) \Rightarrow I_C = \beta (I - I_O) + (1+\beta) I_{CO}$$

$$= \beta I - \beta I_O + (1+\beta) I_{CO}$$

* if $\beta >> 1$ we get

$$I_C = \beta I - \beta I_O + \beta I_{CO}$$

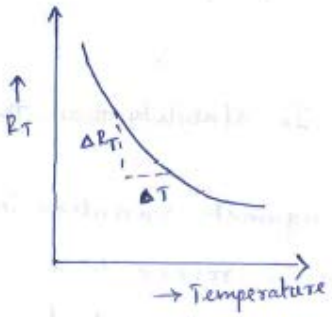
* We assume

$$I_O = I_{CO} \text{ we get}$$

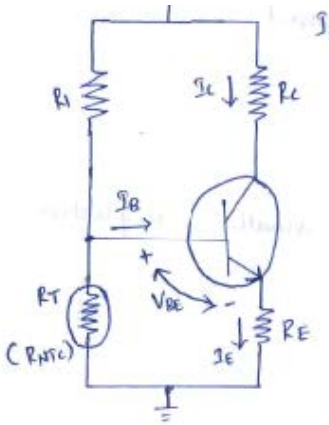
$$I_C = \beta I$$

* As I is constant, I_C remains fairly constant.
* We can say that changes by I_{CO} with temperature are compensated by diode & Thus collector current remains fairly constant.

2. Thermistor compensation Technique



* This method uses Temperature sensitive devices such as Thermistors rather than diode (or) Transistor
* It has negative temperature coefficient. it's resistance decreases exponentially with increasing Temperature : as shown in fig:
* Slope of this curve $= \frac{\partial R_T}{\partial T}$
* The $\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor has negative temperature coefficient resistance (NTC).

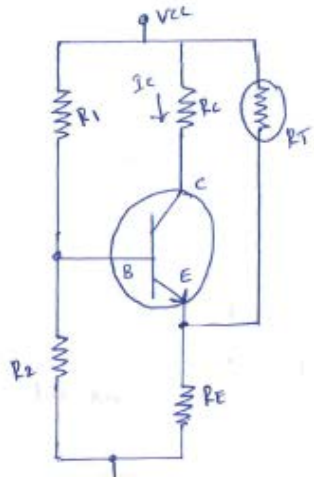


In This figure :

* R_2 is replaced by Thermistor R_T in self bias circuit.
* With increase in Temperature R_T decreases.
* Hence the voltage drop across it also decreases.
* The voltage drop is nothing but voltage at the base with respect to ground. Hence V_{BE} decreases which decrease I_B.

* This behaviour will tend to offset the increase in I_C with Temperature
* We know,

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$ → In this equation, There is increase in I_{CBO} & decrease in I_B which keeps I_C almost constant.



In this Fig:

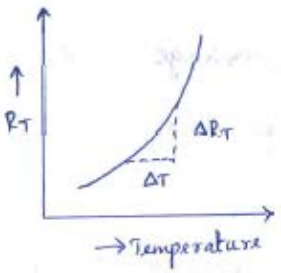
* The Thermistor is connected b/w Emitter & Vcc to minimize the increase in I_C due to changes in I_{CO}, β (or) V_{BE} with Temperature.
* I_C increases with Temperature & R_T decreases with increase in Temperature.
* ∴ The current flow through R_E increases, which increase the voltage drop across it.
* The Emitter-Base junction is forward biased.

* But due to increase in voltage drop across RE, emitter is made more positive which decreases the forward bias voltage V_{BE}.
* Hence base current decreases.
* I_C is given by

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

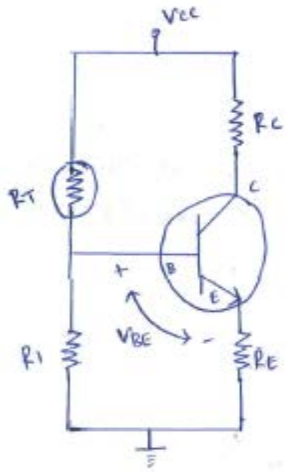
* As I_{CBO} increases with Temperature, I_B decreases & hence I_C remains fairly constant.

3. Sensistor Compensation Technique



* This method uses temperature sensitive devices such as sensistor rather than diode or Transistor.
* It has a positive temperature coefficient. its resistance increases exponentially with increase temperature.

* slope of this curve = $\frac{\partial R_T}{\partial T}$.
* $\frac{\partial R_T}{\partial T}$ is the temperature coefficient for sensistor & the slope is positive
* So we can say that sensistor have positive temperature coefficient of resistance (PTC)



In this fig:

* R_1 is replaced by sensistor R_T in self bias circuit.
* Now R_T & R_2 are 2 resistors of the potential divider
* As temperature increases, R_T increases which decrease the current flowing through it.
* Hence the current through R_2 decreases which decrease the voltage drop across it.
* Voltage drop across R_2 is the voltage b/w base & ground.
* So V_{BE} decreases which decreases I_B.

* $I_C = \beta I_B + (1+\beta) I_{CBO}$ → When I_{CBO} increases with increase in Temperature, I_B decreases due to reduction in V_{BE}, maintaining I_C fairly constant.

Thermal Stability

* The maximum average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction & may lie in the range from a few milliwatts to 200 W.

* The power dissipated within the transistor is predominantly the power dissipated at its collector base junction.

* For Si transistor this temperature is in the range 150 to 225°C & for Ge transistor it's between 60 to 100°C.

* The collector - base junction temperature may rise because of 2 reasons.

1. Due to rise in ambient temperature
2. Due to self heating.

⇓

* The increase in collector current (I_C) increase the power dissipated at the collector junction. This in turn further increa the temperature of the junction & hence increase in the collector current (I_C). The process is cumulative & it's referred to as Self heating. The excess heat produced at the collector base junction may even burn & destroy the transistor. This situatic is called thermal runaway of the transistor.

2 Mark

1. Thermal Resistance

* The stead state temperature rise at the collector junction is proportional to the power dissipated at the junction.

* It's given as

$$\partial T = T_j - T_A = \theta P_D \quad -①$$

Where

T_j - junction temperature in °C
T_A - Ambient temperature in °C.
P_D - power in watts dissipated at the collector junction
θ - constant of proportionality.

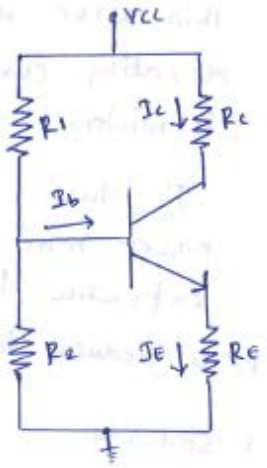
$$\frac{\partial P_D}{\partial T_j} \simeq \frac{1}{\theta} \quad \text{— (4)}$$

* substitute eqn 4 in (3) we get

$$\frac{\partial P_c}{\partial T_j} < \frac{1}{\theta}$$ (5) → This condition must be satisfied to prevent thermal runaway.

* By proper design of biasing circuit it's possible to ensure that the transistor can't runaway below a specified ambient temperature (or) even under any condition.

Voltage Divider Bias Circuit



* P_c = Heat generated at the collector junction.

= D.c power input to the circuit − power lost as I^2R in R_c & R_E

So

$$P_c = V_{cc} \times I_c - I_c^2 R_c - I_E^2 R_E \quad \text{— (6)}$$

$\because I_c \cong I_E$

$$P_c = V_{cc} \times I_c - I_c^2 R_c - I_c^2 R_E$$

$$= V_{cc} \times I_c - I_c^2 (R_c + R_E) \quad \text{— (7)}$$

* Differentiate eqn (7) w.r.to I_c we get

$$\frac{\partial P_c}{\partial I_c} = V_{cc} - 2I_c (R_c + R_E) \quad \text{— (8)}$$

* Rewrite eqn (5)

$$\frac{\partial P_c}{\partial I_c} \cdot \frac{\partial I_c}{\partial T_j} < \frac{1}{\theta} \quad \text{— (9)}$$

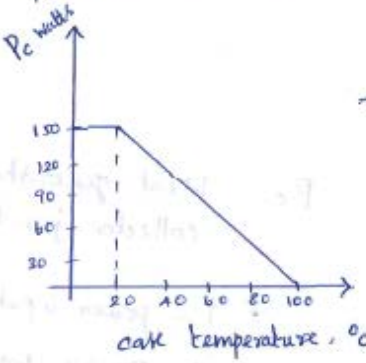
* The θ, which is constant of proportionality is referred to as Thermal resistance.

$$\theta = \frac{T_j - T_A}{P_D} \quad -(2)$$

* The Unit of θ is Thermal resistance, is °c/watt.

* The θ various from 0.2 °c/W for a high power transistor with an efficient heat sink to 1000 °c/W for a low power transistor

* The maximum collector power P_c allowed for safe operation is specified at 25°c.



→ * This curve is power - temperature derating curve for a germanium transistor.

* It shows that above 25 °c, collector power must be decreased at the extreme temperature at which the transistor may operate, P_c is reduced to zero.

2. Condition for Thermal Stability

* The Thermal runaway may even burn & destroy The transistor. it's necessary to avoid Thermal runaway

* The required condition to avoid Thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated.

2 Mark

* It's given by

$$\frac{\partial P_c}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad -(3)$$

* Differentiate eqn (1) we get

$T_j - T_A = \theta P_D$ w.r. to T_j we get

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

* The $\frac{\partial I_c}{\partial T_j}$ can be written as

$$\frac{\partial I_c}{\partial T_j} = S \frac{\partial I_{co}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j} \quad -(10)$$

* The junction temperature affect the I_c by affecting, I_{co}, V_{BE} & β.

* But for thermal runaway the affect of I_{co} dominates.

$$\frac{\partial I_c}{\partial T_j} = \frac{\partial I_{co}}{\partial T_j} \quad -(11)$$

* As the reverse saturation current (I_{co}) for both Si & Ge transistor increases about 7% / °C.

$$\frac{\partial I_{co}}{\partial T_j} = 0.07 I_{co} \quad -(12)$$

* Substitute values of $\frac{\partial I_c}{\partial T_j}$ & $\frac{\partial P_c}{\partial I_c}$ in eqn (11) we get

$$\frac{\partial I_c}{\partial T_j} = S \times 0.07 I_{co} \quad -(13)$$

* Now substitute the values of $\frac{\partial I_c}{\partial T_j}$ & $\frac{\partial P_c}{\partial I_c}$ from eqn (13) & (8) in eqn (9) we get,

$$[V_{cc} - 2I_c (R_c + R_E)] S (0.07 I_{co}) < \frac{1}{\theta} \quad -(14)$$

$\because V_{cc} < 2 I_c (R_c + R_E)$

$\because \frac{V_{cc}}{2} < I_c (R_E + R_E) \quad -(15)$

* Apply KVL to the collector-Emitter junction of voltage divider bias circuit we get

$$V_{cc} - I_c R_c - I_E R_E - V_{CE} = 0 \qquad \because I_c \cong I_E$$

$$V_{CE} = V_{cc} - I_c (R_L + R_E)$$

$$I_c (R_c + R_E) = V_{cc} - V_{CE}$$

* Substitute value of $I_C(R_C + R_E)$ in eqn (15) we get

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$V_{CE} < \frac{V_{CC}}{2}$$

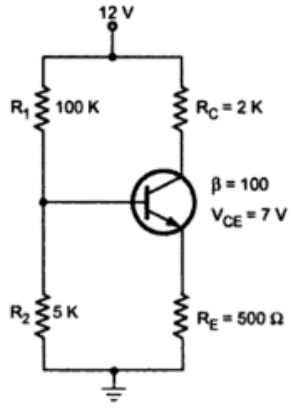
* Thus if $V_{CE} < \frac{V_{CC}}{2}$, the stability is ensured.

* But in transformer coupled circuit R_C & R_E are quite small & $V_{CE} \cong V_{CC}$.

* Hence it's necessary to design transformer coupled circuits with stability factor as close to 1 as possible to avoid thermal runaway.

Questions:

1. What do you understand by bias stabilization and bias compensation? Why it is necessary in transistor amplifiers?
2. What is a condition for thermal stability?
3. Explain bias compensation using sensistors.
4. Write notes on bias compensation using thermistors.
5. Explain the diode compensation technique.
6. Derive the condition for thermal stability.
7. Calculate the value of thermal resistance θ for the transistor in the circuit shown in the Figure. In order to make circuit thermally stable. Assume that I_{CO} = 1 nA at 25^{0}C.



Design of biasing for JFET

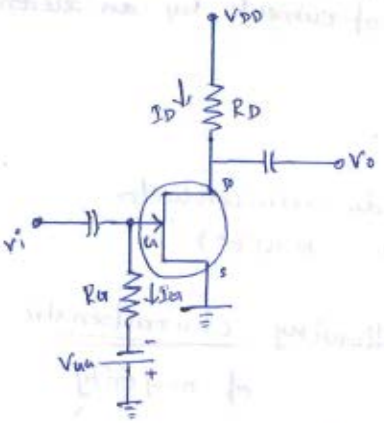
* FET - Field Effect Transistor - It's a semiconductor device which depends for its operation on the control of current by an electric field.

FET
- Junction field Effect Transistor (or) FFT
- Metal-Oxide-semiconductor Transistor (MOSFET)

FET differs from the BJT in the following characteristics

1. It's operation depends upon the flow of majority carriers Only.
2. It's simpler to fabricate & occupies less space.
3. It exhibits a high input resistance, typically many megaohms.
4. It's less noisy compared to BJT.
5. It exhibits no offset voltage at zero drain current

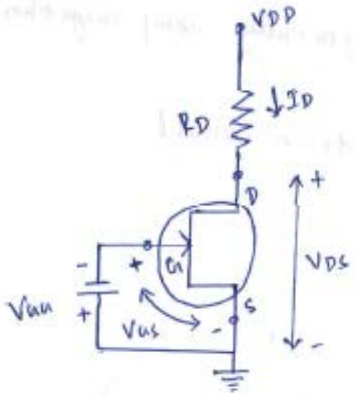
1. Fixed Bias | Gate Bias



* To make the Gate-source junction reverse biased a separate supply V_{GG} is connected such that gate is more negative than the source.

Dc Analysis:

* For dc analysis coupling capacitors are open circuited.
* The current through R_G is I_G which is 0.
* This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit.



* We know for dc analysis

$I_G = 0$ amps

* Apply KVL to the Gate to source junction

$V_{GS} + V_{GG} = 0$

$\therefore V_{GS} = -V_{GG}$

* Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude & hence the name fixed bias circuit

* For fixed bias circuit the I_D can be calculated as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

* Apply KVL to the Drain to Source junction

$V_{DS} + I_D R_D - V_{DD} = 0$

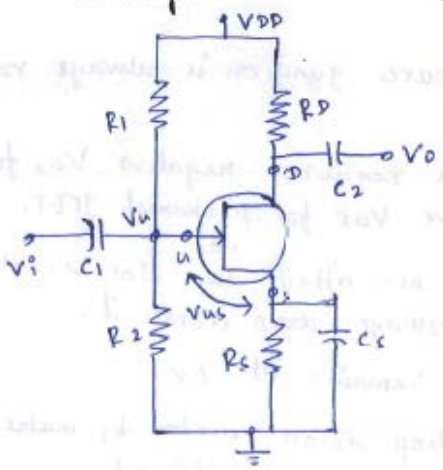
$\therefore V_{DS} = V_{DD} - I_D R_D$

Q-Point

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$V_{DSQ} = V_{DD} - I_{DQ} R_D$

2. Voltage Divider Bias / potential Divider Bias



* The voltage at the source of the JFET must be more positive than the voltage at the Gate in Order to keep the Gate - Source junction reverse biased.

* The source voltage is

$$V_S = I_S R_S \qquad \because I_S = I_D$$

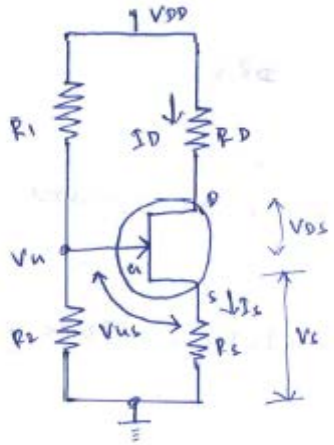
$$V_S = I_D R_S$$

* The Gate voltage is set by resistors R_1 & R_2 as expressed by the following equation using The voltage divider formula

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD} \qquad \because I_G = 0$$

Dc Analysis :

* For dc analysis the coupling capacitors are open circuited



* Apply KVL to the Gate - source junction

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_{in} - V_S$$

$$= V_{in} - I_S R_S \qquad \because I_S = I_D$$

$$= V_{in} - I_D R_S$$

$$\therefore V_{GS} = V_{in} - I_D R_S$$

* Apply KVL to the Drain - Source junction.

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - \overset{V_S}{I_D R_S}$$

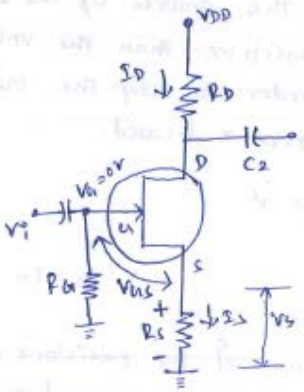
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Q-point :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$

3. Self Bias



* The Gate-Source junction is always reverse biased.
* The condition requires negative V_{GS} for n-channel JFET & a positive V_{GS} for p-channel JFET.
* The R_G does not affect the bias because it has essentially no voltage drop across it.
* ∴ the Gate remains at 0V.
* The voltage drop across resistor R_S make the Gate-Source junction reverse biased.

* Is produces voltage drop across R_S & make the source positive w.r.to ground.

Since

$$I_S = I_D \text{ & } V_G = 0 \quad \text{Then} \quad V_S = I_S R_S = I_D R_S$$

* The Gate-Source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For p channel:

* The voltage drop across R_S & make the source negative w.r.h ground.

Since

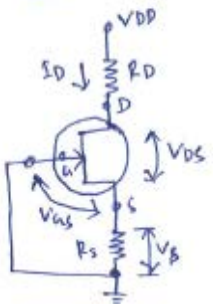
$$I_S = I_D \text{ & } V_G = 0 \quad \text{then} \quad V_S = -I_S R_S = -I_D R_S$$

* The Gate-Source voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = I_D R_S$$

DC Analysis:

For n-channel



For dc analysis the coupling capacitors are replaced by open circuit & R_G is replaced by short circuit equivalent. Since $I_G = 0$.

W.K.T

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad -(1)$$

Substitute the value of V_{GS} in eqn ①

$$① \Rightarrow I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2 \rightarrow \text{for n-channel}$$

$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Apply KVL to the Drain to source junction

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D$$

$$= V_{DD} - I_D R_S - I_D R_D$$

$$\therefore V_{DS} = V_{DD} - I_D(R_S + R_D)$$

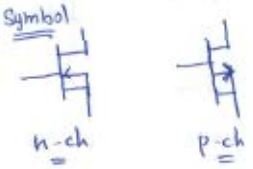
Design of Biasing for MOSFET

* MOSFET - Metal Oxide Semiconductor Field Effect Transistor

* It has a Gate, Source & Drain like the JFET.

* The Drain current (I_D) in the MOSFET is controlled by the Gate-Source Voltage V_{GS}.

* There are 2 types of MOSFETS



- Enhancement type (E-MOSFET)
- Depletion type (D-MOSFET)

* MOSFET is also referred to as an IGFET because the gate is isolated from the channel.

1. DMOSFET

* It is similar to the circuit used for JFET biasing

* The primary difference b/w the two is the fact that depletion type MOSFETs also permits operating points with positive value of V_{GS} for n-channel & negative values of V_{GS} for p-channel.

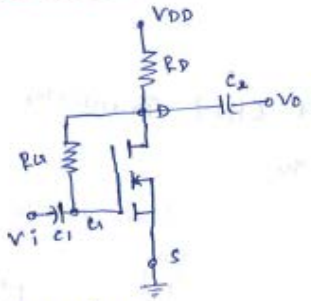
* To have positive values of V_{GS} for n-channel & negative value of V_{GS} for p-channel self bias circuit is unsuitable.

[Use only
1. Fixed bias
2. Voltage divider bias]

2. EMOSFET

* It's similar to the circuit used for JFET biasing.
* The primary difference b/w the two is the fact that Enhancement type MOSFETS also permits operating points with positive value of V_{GS} for n-channel & negative values of V_{GS} for p-channel.
* To have positive values of V_{GS} the n-channel & negative value of V_{GS} for p-channel self bias circuit is unsuitable.
* Here, we will discuss only feedback bias & voltage divider bias circuit.

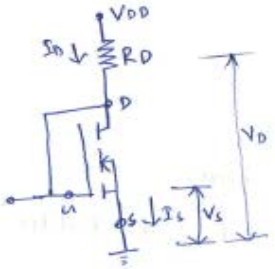
1. Feed Back Bias



Dc Analysis:

* For dc Analysis we can replace coupling capacitors by open circuit & replace the R_G by a short circuit equivalent. Since $I_G = 0$.
* The Drain & Gate Terminals are shorted.

$$V_D = V_D \quad \& \quad V_{DS} = V_{GS} \quad \because V_S = 0$$



* Apply KVL to the Drain - source junction

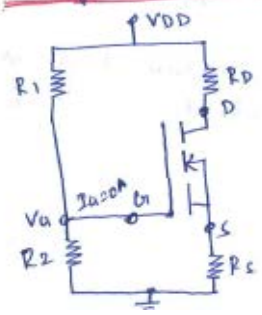
$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

(or)

$$V_{GS} = V_{DD} - I_D R_D$$

2. Voltage Divider Bias



* The biasing resistors R_1 & R_2 are designed to provide positive gate to source voltage.
* Apply KVL to the Gate - Soure junction

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S$$

$$V_{GS} = V_G - I_S R_S = V_G - I_D R_S \qquad \because I_D = I_S$$

$$\therefore V_{GS} = V_G - I_D R_S$$

* Apply KVL to Drain - Source junction

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_S R_S \qquad \because I_D = I_S$$

$$= V_{DD} - I_D R_D - I_D R_S$$

$$\therefore V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Questions:

1. Mention the different types of biasing circuits for JFET.
2. With neat diagram, explain Fixed bias of JFET.
3. Discuss Voltage Divider Biasing circuit of JFET.
4. Describe Self Bias Circuit of JFET with neat diagram.
5. Explain the biasing methods of MOSFET.