Unit-I

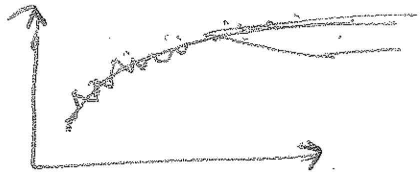
Review of semi-conductor in physics:

Open-circuited p-n junction

Diode equation:

PN diode as Rectifier (Forward and reverse bias):

Voltage Characteristics:



BJT as an amplifier and as switch:

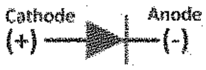
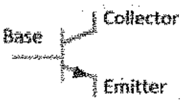
Brief idea of dc analysis:

Biasing circuits:

Small signal operation and models:

Single stage BJT amplifier:

Difference between diode and transistor:

Basis For Comparison	Diode	Transistor
Definition	A semiconductor device in which current flows only in one direction.	A semiconductor device which transfers the weak signal from low resistance circuit to high resistance circuit.
Symbol		
Uses	Rectification	Regulator, Amplification and Rectification
Terminal	Two (Anode and Cathode)	Three (Emitter, Base and Collector)
Switch	Uncontrolled	Controlled
Types	Junction diode, Light emitting diode, Photodiodes, Schottky diodes, Tunnel, Veractor and Zener diode.	Bipolar transistor and Field Effect Transistor.
Region	P-region and N-region	Emitter, Collector and Base
Depletion Region	One	Two

Date: 18.9.2023
Day: Monday

Lecture 1

Transistor:

- It was developed in the year 1947 by the three American physicists, John Bardeen, Walter Brattain and William Shockley.
- A Transistor is a three terminal semiconductor device that can be used to conduct and insulate electrical current or voltage. Generally, it is used to regulate or control the flow of electronic signals.It acts as an amplifier (e.g. radio receiver) and a switch (e.g. digital circuits).
- Transistor are inferred due to small size, light weight, no heating requirements, higher efficiency, easy to use, no warm-up period is required, lower operating voltages.

Types of transistor

- Bipolar Junction Transistor (BJT)
  - n-p-n
  - p-n-p
- Field Effect Transistor (FET) (uses EF to control the flow of current in Semiconductor)
  - JFET (Junction-FETs)
  - MOSFET
    - Depletion MOSFET
    - Enhancement MOSFET

(MOSFET: Metal-oxide-Semiconductor field effect transistor)

BJT (BipolarJunction Transistor):

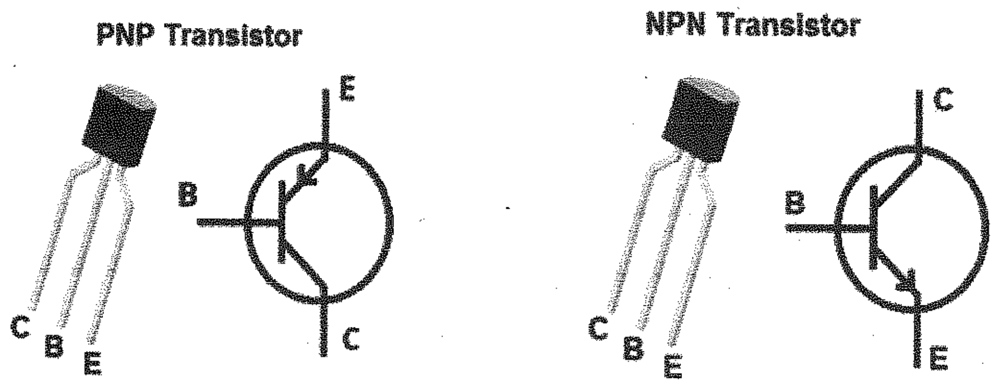
It is a three-terminal semiconductor device consisting of two p-n junctions. It is used as a switching device and for amplification of signals.It is an active device (current controlled device).

Weak signal → $\boxed{\text{BJT}}$ Strong signal →

It consist of two PN junction formed by sandwiching either P-type or N-type semiconductor between a pair of opposite types **(i) n-p-n (ii) p-n-p**

Basics parts and symbol of a Transistor:

A transistor is composed of three layers of the semiconductor materials.

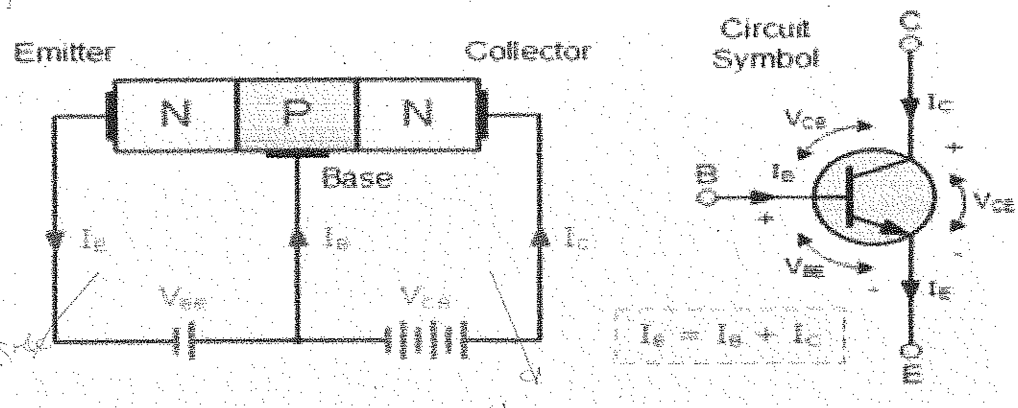


The three terminals are (Features of the terminal)

(i) **Emitter (E):** Heavily doped, Moderate size
(ii) **Base (B):** Lightly doped, Thin
(iii) **Collector (C):** Moderately doped, lager/wider

(i) n-p-n type

Working:



Forward bias causes the electron ejection to flow towards the base and constitutes emitter current I_E, base electron tends to combine with the holes since base is lightly doped and very thin very few electron combines with the holes i.e., less than 5% to constituents I_B having small value in µA. Rest of the electron i.e., more than 95% cross over the collector region to constituents collector current through diffusion and minority carriers across the junction which is the ~~because of~~ reverse bias.

Now, according to Kirchhoff law,

$$I_E = I_B + I_C$$

Thecollector current is composed of the two components (i) Minority (ii) Majority

$$I_C = I_C\,(mA) + I_{CO}\,(\mu A)$$

I_C (mA), is of majority current components. The minority current components is called the leakage current and represented by I_{CO}.

(ii) p-n-p type

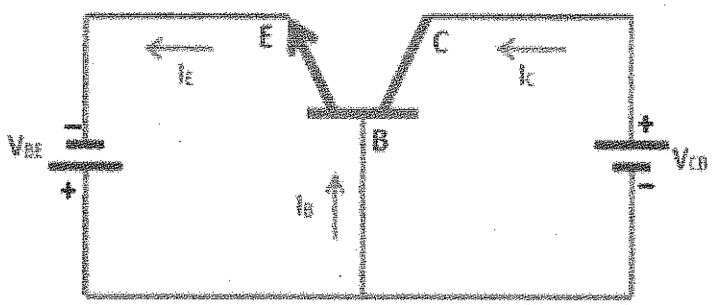
Working:

Configuration of transistor :

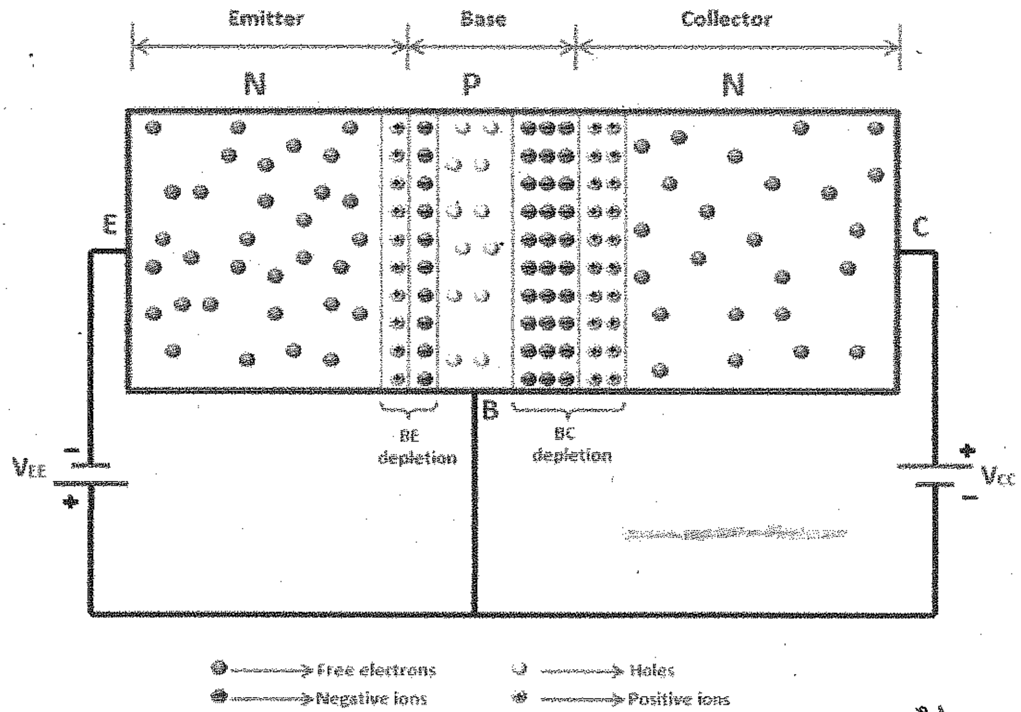
(i) Common base (CB) configuration

Common baseconfiguration is derived from the fact that the base is common to both the input and output sides of the configuration.

(a) Construction:



(b) Working:



"How I_E, I_B and I_C are generated in the transistor circuit ?

- In the figure you can see that base-emitter junction is in forward biased condition through applied voltage V_{BE} and collector-base junction is in the reverse-biased state through the voltage source V_{CB}.

- Due to forward biasing voltage V_{BE} electrons that are major carriers in emitter will bear a force of repulsion due to negative terminal of battery also holes in the base of the transistor will bear the force of repulsion from the positive side of the voltage source.
- Due to this electron move towards the base from emitter and holes moves from base to emitter.
- Due to the movement of electrons and holes current flows. The real current is due to the flow of electrons which flows from emitter to base.
- But we follow conventional current that is from base to emitter. Hence current is generated at base and emitter (I_B, I_E).
- The electrons that move from emitter toward base will combine with a hole which is majority carriers and holes moving toward the base to emitter combine with the emitter.
- In the above diagram, you can note that the area of the base is very less. So, less number of electrons coming from emitter will combine with holes in base remaining will enter to the collector.
- The electrons enter into the collector will bear the force of attraction from the positive side of the battery.
- So free electrons in collectors move to the positive side of the battery due to that current is generated at the collector region. (I_C)
- The current produced at collectors and base is due to electrons coming from the emitter. hence, emitter current is large than the collector and base current and equal to the sum of these two currents.

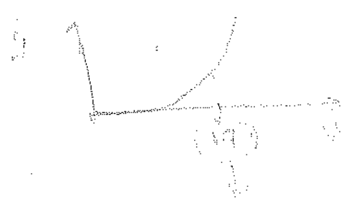
$$IE = IB + IC$$

- ~~As we discuss above emitter is input and collector is output.~~
- As output or collector current is less than the emitter current hence gain of current is less than the one. (gain = output/input)
- In simple words, a common base amplifier attenuates current ~~that~~ rather than amplification of it.
- As the base-emitter junctions at input operate as a forward-biased diode. So the impedance of a common base amplifier at the input is less.
- The collector-base junction behaves like a reverse-biased diode due to this impedance for a common base at the output is high.
- So we can conclude that input impedance for the common base is less and high at the output.
- Such a transistor that has less input impedance and large output impedance give large voltage gain.
- As the gain is large but the current is less so the power gain of this amplifier is less than other amplifiers.
- These amplifiers are used in such an application where less input is needed.
- Base amplifier configuration is mostly used in the current buffer circuit.
- This amplifier is not commonly used as a common emitter and collector is used.

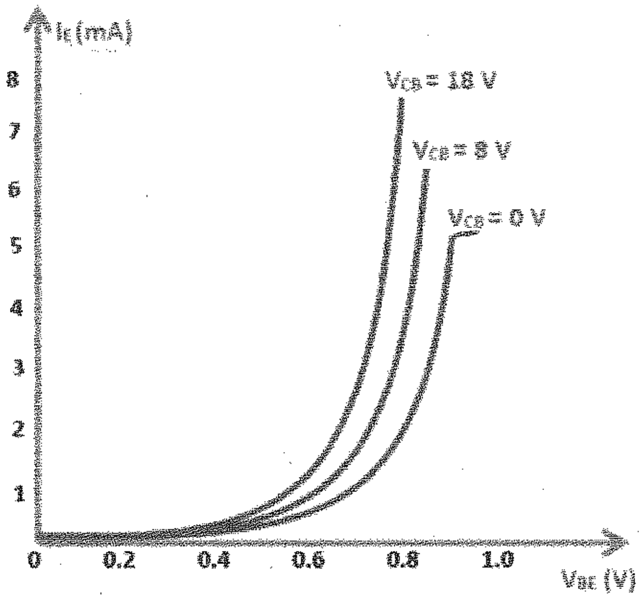
Input Characteristics: (variation of current with voltage)

Current: I_E
Voltage: V_{BE}
For various output voltage (V_{CB})

In case of simple diode



Why I_E increases with increasing V_{CB} ?



As, the V_{CB} is in the reversed bias on increasing the VCB values the reverse bias increases which results in thicker BC depletion regions and the base becomes much thinner. Thus, less recombination takes at the base and more electron moves toward the collector, resulting in higher IE.

Input resistance:

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{\text{at const. } V_{CB}}$$

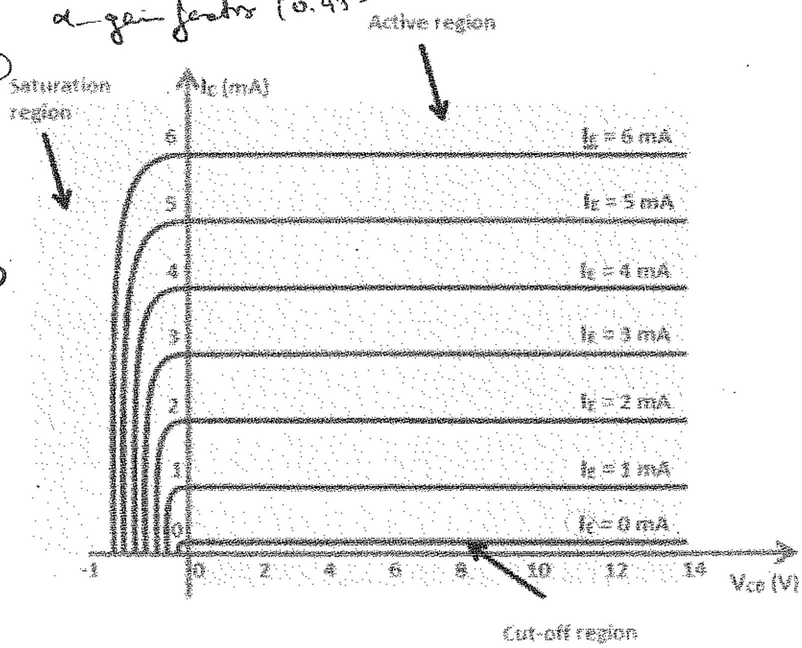
Output characteristics:
Current: I_C
Voltage: V_{CB}
For various input current (I_E)

Before the characteristics let us understand

and $\quad I_E = I_B + I_C \leftrightarrow$ ①
I_C =alpha(I_E) + I_{CBO}

$I_c = \alpha I_E$ $\quad$ α – gain factor (0.95 – 0.98 ~ 1)

$\boxed{I_c \simeq I_E} \rightarrow$ ②



Saturation region: (Both diode FB)
Both the diodes are in forward bias. So, to make the reverse bias to forward bias we change the polarity by decreasing the voltage. So, with

decrease in the V_{CB} voltage the $I_C$current decreases. Because the electron from the emitter are now restricted because of the forward bias or the positive polarity.So, I_C current decreases.

Active region: (1 FB · 1 RB)
E-B junction (Forward biased)
B-C junction (Reverse biased)
Through V_{CB} we get the current I_C, But further increasing the V_{CB}, I_C is not changing because I_C doesn't depend on V_{CB}, instead it depends on IE current. As I_C= alpha(I_E) or I_C ~ I_E

Cut-off region: (R.B) (RB)
E-B junction (open means no supply i.e., I_E=0)
B-C junction (Reverse biased)

So, ifI_E=0 then I_C is 0 (there is some leakage current which is negligible)

In the active region transistor work as an amplifier, whereas, in cut-off region it works as a switch.

- IC varies with the VCB only for few voltages less than 1V transistor is never operated in this region.
- When VCB is increased to 1 or 2 V, IC becomes constant and depends on IE only. Here almost all emitter current flows through the collector and the transistor is operated in this region.
- A very large change in VCB produces very small change in IC, this indicates that the output resistance is very high.
- Beyond the particular value of VCB, the reversed bias collector junction breaks down and the current increases rapidly. A transistor is not designed to operate in this region.

Output resistance :

$$r_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E}$$

Thus, the r_o of common base circuit is very high approx. several tens K ohms..

(C) Current amplification factor (Alpha) α (gain)

Ratio of the change in output current to change in input current at constant V_{CB} is called current amplifier factor.

$$\alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}}$$

$$I_E > I_C \Rightarrow \alpha < 1$$

α can be ↑ed by ↓ing I_B, but it can't be made 1. This is achieved by making the base thin and doping it light. Practically value of α in commercial transistors range from 0.9 to 0.99.

B) Expression for collector current:-

1. Part of emitter current that reaches collector (αI_E)
2. Leakage current ($I_{leakage}$). This current is due to the movement of minority carriers. BC junction on account of it being reverse biased.

$$I_C = \alpha I_E + \underbrace{I_{leakage}}_{I_{CBO}} \quad \text{total collector current.}$$

$$I_C = \alpha I_E + I_{CBO} \rightarrow (1)$$

We know

$$I_E = I_C + I_B$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{(1-\alpha)} I_{CBO}}$$

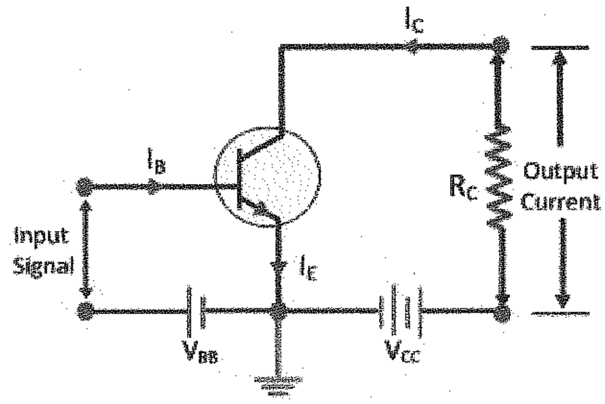
(ii) Common Emitter (CE):

Common emitter configuration is derived from the fact that the emitter is common to both the input and output sides of the configuration.

It is frequently used configuration of BJT as it does amplification of weak signal to strong signal. It does amplification of voltage, **current and power.** (Best configuration for amplification)

Discussing the n-p-n CE configuration (because the mobility of electron is higher than holes)

Construction/Working (n-p-n)

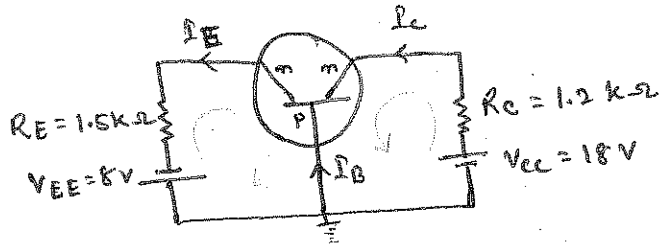


NPN Transistor

(iii) Common collector (CC)

Numerical:

①. For the common base circuit shown in fig. determine I_c and V_{CB}. Assume the transistor to be of silicon.



For Si = 0.7V
germanium = 0.3V

For Silicon. $V_{BE} = 0.7V$

Applying KVL to the emitter-side loop, we get,

$$V_{EE} = I_E R_E + V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{(8 - 0.7)V}{1.5 k\Omega}$$

$$\boxed{I_E = 4.87 mA}$$

$$\therefore I_c \simeq I_E = 4.87 mA.$$

Applying KVL to the collector-side loop, we have

$$V_{cc} = I_c R_c + V_{CB}$$

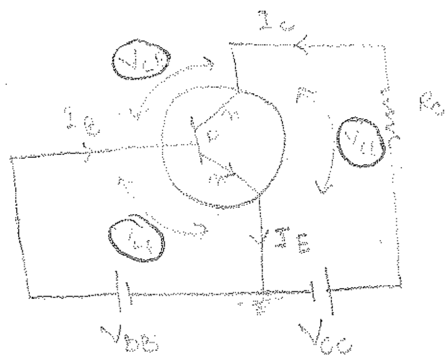
$$V_{CB} = V_{cc} - I_c R_c$$

$$= 18V - 4.87mA \times 1.2 k\Omega$$

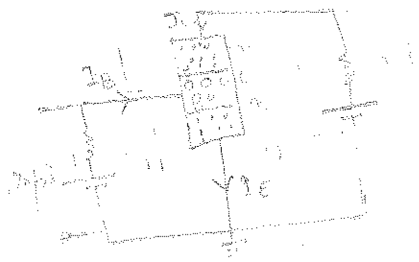
$$\boxed{V_{CB} = 12.16 V}$$

②

2. Common Emitter Configuration :-



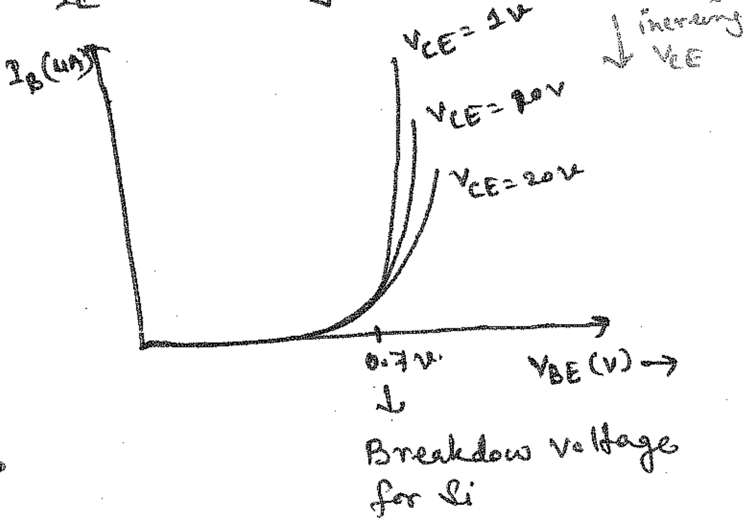
The common Emitter amplifier is a three basic Single-stage BJT and is used as a voltage Amplifier. The input of this amplifier is taken from the ~~base~~ terminal. the output is collected from the collector terminal and the emitter terminal is common for both the terminal.



Working Principle:

Input characteristics: (the characteristic is same as p-n diode)

Input current = I_B ; $I_E = I_B + I_C$
output current = I_C ; $I_C = \alpha I_E$



We have the Eqn:-

$$V_{CE} = V_{CB} + V_{BE} \rightarrow fix$$

Let fixed V_{BE}, and vary V_{CE}
(why I_B ↓es with increase in V_{CE})

V_{CE} ↑es → V_{CB} ↑es → Reverse Bias ↑es
↓
Depletion region thick
↓
no. of holes ↓es
↓
recombination ↓es. So lesser number of valance electron moves toward base.
So, I_B ↓es

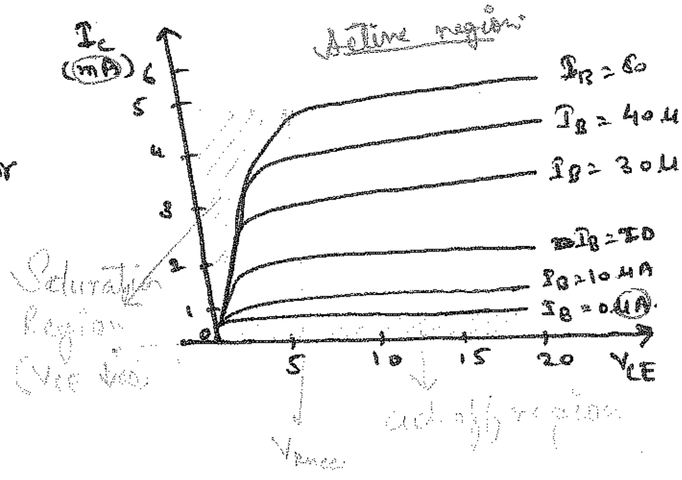
i.e.
V_{CE} ↑es → I_B ↓es.

* Input resistance:-

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}\Big|_{V_{CE}}$$

Input resistance of CE configuration is higher than the input resistance of CB configuration.

Output characteristics :- (I_C, V_{CE}) at I_B.



• Base Current Amplification factor (β) :-

The ratio of change in collector current to the change in base current is base current amplification.

i.e $\beta = \dfrac{\Delta I_C}{\Delta I_B}$

β changes from 20 to 500

$\mu A \rightarrow mA$ $\left\{ \begin{array}{l} \text{Amplification of} \\ \text{Current} \end{array} \right\}$

relation b/w α and β :-

$\beta = \dfrac{\Delta I_C}{\Delta I_B}$ (CE Configuration)

$\alpha = \dfrac{\Delta I_C}{\Delta I_E}$ (CB Configuration)

We know,

$$I_E = I_B + I_C$$

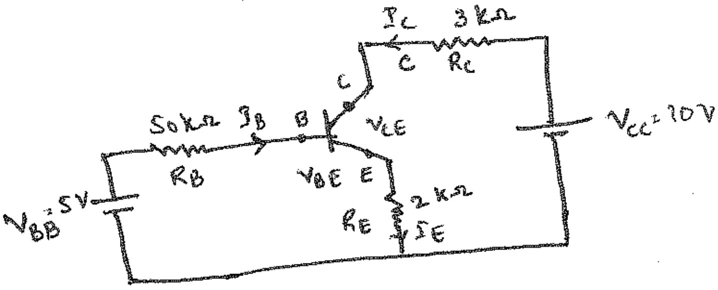
and $I_C = \alpha I_E$

$$\beta = \frac{\alpha I_E}{\Delta I_B} = \frac{\alpha \Delta I_E}{(\Delta I_E - \Delta I_C)}$$

$$= \frac{\alpha \cancel{\Delta I_E}}{\cancel{\Delta I_E}\left(1 - \frac{\Delta I_C}{\Delta I_E}\right)}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Q. The transistor in fig has $\beta = 100$ and $I_{CBO} = 20nA$. Calculate I_B, I_C, V_{CE} and hence decide in which region the transistor operates. Given $V_{BE(sat.)} = 0.8V$, $V_{CE(sat.)} = 0.2V$ and $V_{BE(active)} = 0.7V$.



At first we assume that the transistor is operating in Active Region. Now

$$I_E = I_B + I_C \simeq I_B + \beta I_B = (1+\beta) I_B$$

$$I_E = (1+\beta) I_B$$

∴ Applying KVL to the base circuit we get

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$\therefore I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$= \frac{5V - 0.7V}{50k\Omega + 101 \times 2k\Omega}$$

$$\therefore I_B = 17.06\, \mu A$$

Application of KVL to collector circuit yields

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (\because I_E \simeq I_C)$$

$$= 10 - 1.708 mA \times 5 k\Omega$$

$$V_{CE} = 1.46 V$$

Since, $V_{CE} > V_{CE(sat.)} \rightarrow 0.2V$, our assumption is correct i.e the transistor is operating in the Active Region.

Expression for Collector Current: (in CE)

$$I_E = I_B + I_C \longrightarrow (1)$$

$$I_C = \alpha I_E + I_{CBO} \longrightarrow (2)$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \rightarrow (3)$$

If $I_B = 0$ (Base is open circuit), collector current will flow to the emitter (i.e I_{CEO} → collector cut off current with base open.)

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} \rightarrow (4)$$

Substituting value of $\frac{I_{CBO}}{1-\alpha}$ in Eqn (3)

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO} \rightarrow (5)$$

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

$$\boxed{I_C = \beta I_B + (1+\beta) I_{CBO}}$$

$$\left(\begin{aligned} \beta &= \frac{\alpha}{1-\alpha} \\ (1-\alpha)\beta &= \alpha \\ 1+\beta &= \frac{1}{1-\alpha} \end{aligned} \right)$$

Current Amplification

now explain graph → as we Inc I_B, I_C becomes βI_B (i.e. Amplication of current is there)

Fig.

Leakage in transistor is due to minority carrier and is independent of temperature.

I_E in term of β:

$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$\boxed{I_E = (1+\beta) I_B}$$

*Common Emitter Configuration is mostly used configuration why?

Because it does amplification of voltage, current and power. Mostly it is used for current and power amplification.

1. High current gain

$$I_C = \beta I_B + I_{CEO}$$

β is high : $I_C >> I_B$.

$\left(\text{gain} = \frac{I_C}{I_B}\right)$

2. High voltage and power gain
3. Moderate output to input impedance ratio.

In CE configuration ratio of output impedance to input impedance is small i.e about 50, This makes CE circuit arrangement an ideal one for coupling b/w various transistor stages.

Q. The constant α of a transistor is 0.95. What would be the change in the collector current corresponding to a change of 0.4mA in the base current in the common emitter configuration.

Given $\alpha = 0.95$
$\Delta I_B = 0.4\text{mA}$
$\Delta I_C = ?$

as $\beta = \frac{\alpha}{1-\alpha}$

$\because \beta = \frac{\alpha}{1-\alpha}$

$= \frac{0.95}{1-0.95} = 19$

Also $\beta = \frac{\Delta I_C}{\Delta I_B}$

$\Delta I_C = \beta \times \Delta I_B$

$= 19 \times 0.4\text{mA}$

$\therefore \boxed{\Delta I_C = 7.6\text{mA}}$

Q. In the CE configuration, the voltage drop across a resistance of 6kΩ connected in the collector circuit is 6 volts. If the current gain in the CB configuration of a transistor is 0.995, then find the base current I_B

Given $R_L = 6k\Omega$, $V_o = 6V$, $\alpha = 0.995$

$\because \beta = \frac{\alpha}{1-\alpha} \Rightarrow \frac{0.995}{1-0.995} = 199$

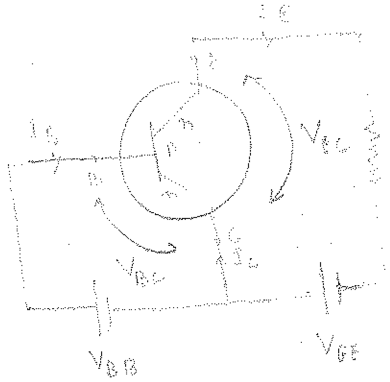
Also $\beta = I_C / I_B$

$= (V_o/R_L)/I_B$

$199 = (6V/6k\Omega)/I_B \Rightarrow I_B = 5.02\,\mu A$

3. Common Collector (CC) :-

In this configuration, the base terminal of the transistor serves as the input, the emitter terminal is the output and the collector terminal is common for both input and output.
The input is applied between the base and collector while the output is taken from the emitter and collector.

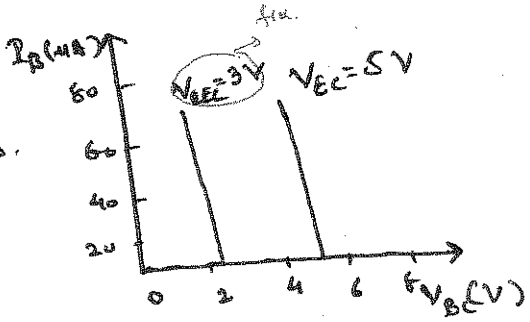


Working Principle:

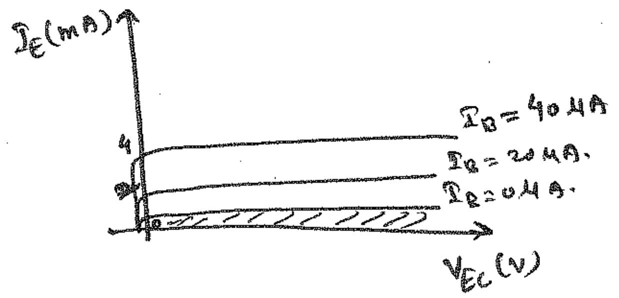
Input characteristics :-

(I_B, V_{BC})

i.e. I_B ↓es → V_{BC} ↑es.
at constant V_{EC}.



output characteristics :-



Dynamic Input resistance:

$$r_i = \frac{\Delta V_{BC}}{\Delta I_B}\Bigg|_{\text{at } V_{EC}=\text{Const.}}$$

Dynamic output resistance:

$$r_o = \frac{\Delta V_{EC}}{\Delta I_E}, \quad I_B = \text{Const.}$$

Current Amplifier factor (γ): in CC

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

as $\Delta I_E \simeq \Delta I_C$.

This configuration also provides the same current gain as in Common Emitter.

Relation b/w γ and α:

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_B}$$ (Current Amplifier gain in CB)

$$I_E = I_B + I_C$$

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

$$\gamma = \frac{1}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

v) Expression for ~~Collector~~ Emitter Current.

$$I_C = \alpha I_E + I_{CBO} \longrightarrow (1)$$

$$I_E = I_C + I_B \longrightarrow (2)$$

$$= \alpha I_E + I_{CBO} + I_B$$

$$(1-\alpha) I_E = I_B + I_{CBO}$$

$$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$\boxed{I_E = (1+\beta) I_B + (1+\beta) I_{CBO}}$$

$$\left(\because \beta = \frac{\alpha}{1-\alpha} \quad (1-\alpha)\beta = \alpha \quad 1+\beta = \frac{1}{1-\alpha} \right)$$

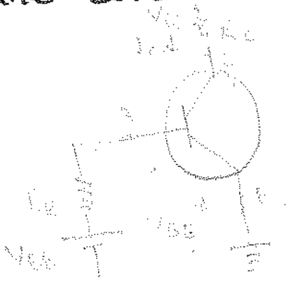
Why C-C Configuration is not used for Amplification?

This configuration has high input resistance & low output resistance hence voltage gain < 1. So ~~hence~~ CC Configuration is not used for Amplification. ~~This~~ It is generally used for impedence matching i.e. for deriving low impedence load and high impedence Source.

Q. Why CE is mostly used Configuration?

* DC Analysis & DC Load Line :-

In case of amplifier, it has two input AC & DC input. If we analyse the circuit as DC input it is called DC analysis.



What is DC Load Line?

In a graph which has all possible values of output current I_c and output voltage V_{CE}. So applying KVL to the output of CE confi. we get.

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = -V_{CE} + V_{CC}$$

$$\boxed{I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}} \rightarrow (A)$$

In Order to get a line, we required minimum two points. So, to get the points. put

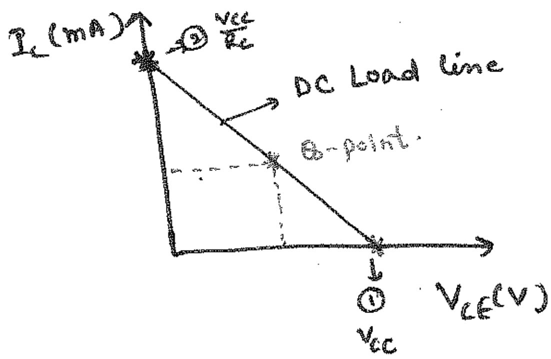
i) $I_C = 0$ in Eqn. (A)

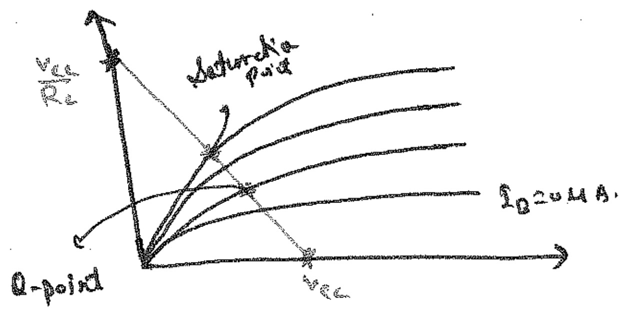
then $\boxed{V_{CE} = V_{CC}} \rightarrow (1)$

ii) $V_{CE} = 0$ in Eqn. (A)

So, $\boxed{I_C = \frac{V_{CC}}{R_C}} \rightarrow (2)$

DC Load Line in output characteristics.





Now, comes. Q-point / operating point:

- Zero Signal value of I_C and V_{CE} are known as the operating point. When a signal is applied variation of I_C + V_{CE} takes place about the line.
- For a faithful amplification we select Q-point at exactly middle of the plot.

(Numerical).

Transistor Biasing :-   BJT — ON → Saturation; OFF → cut-off; amplifier → Active region.

(4)

The proper flow of zero Signal Collector current, and the maintenance of proper collector-emitter voltage during the passage of Signal is known as Transistor Biasing.
To obtain the faithful amplification in a transistor. It is required the transistor in active region.

Biasing circuit: (Basic purpose of transistor)
In transistor biasing we want to keep BE junction FB and CB junction properly RB during the application of Signal which can be done by adjusting a bias battery in the circuit. The circuit that provide the transistor biasing is called the Biasing Circuit.

What is Stabilization: (Means to make the operating point independent of T)
Semi-Conductor show temperature dependent characteristics and hence the operating point also changes with temperature. Which is Undesirable.
→ The process of making operating point independent of Temperature changes or variation in transistor parameter is known as Stabilization.
The unstable Q-point causes the thermal runaway.

$$I_C = \beta I_B + (1+\beta) I_{CBO} \rightarrow (1)$$

I_{CBO} is the collector leakage current which is highly influenced by the temperature & ↑es of 10°C temp. doubles the I_{CBO} which is an experimentally varified fact. So, from Eqn. (1) I_C ↑es by $(1+\beta) I_{CBO}$ times, Hence ↑es in I_C.

1. Shift the operating point.
2. This high I_C current when flows produces heat within the transistor. This ↑es the transistor temp. & hence I_{CBO} further ↑es. ↑es in I_{CBO}, I_C ↑es by $(1+\beta) I_{CBO}$ → This ↑es I_C will further raised the temperature.
This effect is Cummulative and I_C in second I_C becomes too large & hence burn the transistor.

This self destruction of an unstablized transistor is known as thermal runaway.

Hence for stability of operating point I_c should kept constant irrespective of change in I_{CBO}. This implies that I_c can be contd. by using I_B.

Stability factor: (S)

The extend to which biasing circuit is capable of keeping I_c constant with variation in I_{CBO} is defined in term of stability factor

$$S = \left.\frac{dI_c}{dI_{CBO}}\right|_{\text{at const. } \beta \text{ or } I_B}.$$

→ Ideal value of $S = 1$, (not possible to attain this value).
→ performance is satisfactory for $S < 25$.

Expression for S for a transistor in CE configuration:

$$I_c = \beta I_B + (1+\beta) I_{CBO}$$

Diff. w.r.t. I_c

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \underbrace{\frac{dI_{CBO}}{dI_c}}_{1/S}$$

$$1 = \beta \frac{dI_B}{dI_c} + \frac{(1+\beta)}{S}$$

$$\boxed{S = \frac{(1+\beta)}{1-\beta\left(\frac{dI_B}{dI_c}\right)}}$$

· General Eqn. for Stability factor.
→ Lower the value of S, better is the thermal stability of the transistor.

→ How or by which changes change collector current.
→ Why stabilization of operating point is necessary.
→ What is thermal runaway.
→ How thermal runaway is avoided.

→ Why Biasing a transistor is needed? or Essential?

Transistor biasing is done to get faithful amplification; So for that the following 3-points should be proper.

i) It should ensure proper Zero Signal Current.

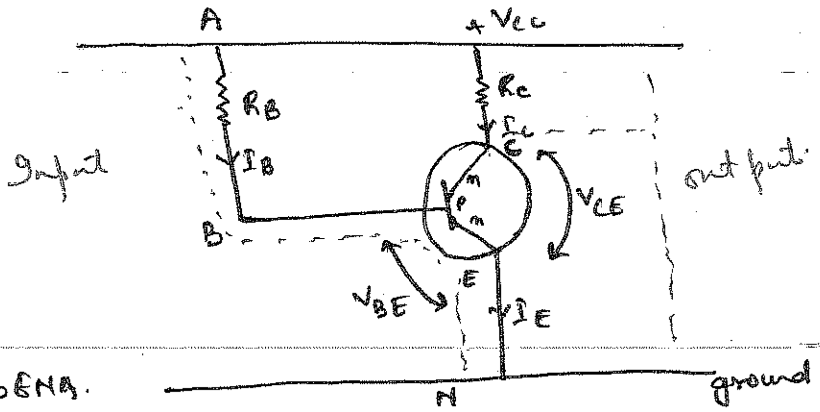
ii) It should ensure that V_{CE} does not fall below 0.5 V for Ge and 1 for Si transistor.

iii) It should ensure the stabilization of operating point.

Four Ways to Biase a Transistor:
- → Base resistor / Fixed Bias
- → Emitter base Method
- → Biasing with collector-feedback resistor
- → Voltage-divider bias / Self biasing

① Fixed Bias:

→ Input
→ output
→ Stability factor
→ Load Line
→



Applying KVL to input ABENA.

$$V_{CC} = I_B R_B + V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \rightarrow ① \quad \text{or} \quad R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

as $V_{CC} > V_{BE}$

$$\boxed{R_B \cong \frac{V_{CC}}{I_B}} \rightarrow ②$$

here, V_{CC} is fixed quantity and I_B is chosen at some suitable value, hence R_B can be found directly and for this reason. This method is called fixed Bias method.

Stability factor:

$$S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}}$$

Differentiate I_B in Eqn ① i.e I_B

$$\frac{dI_B}{dI_C} = 0$$

Hence, $S = \frac{1+\beta}{1-\beta(0)}$

$$\boxed{S = 1+\beta}$$

Comments:

$$S = 1+\beta$$

i.e $\frac{dI_C}{dI_{CBO}} = 1+\beta$

or $dI_C = (1+\beta) dI_{CBO}$

i.e I_C changes $(1+\beta)$ times as much as I_{CBO} changes.

Hence, the fixed bias circuit provides poor thermal stability.

hence, prone to thermal Runaway.

→ For output loop:

$$V_{CC} = I_C R_C + V_{CE}$$

and $I_C = \beta I_B$.

So change in R_C will not affect I_B or I_C as long as we are in active region. However R_C will determine the magnitude of V_{CE}.

Load Line Analysis:

From Eq^n. ①

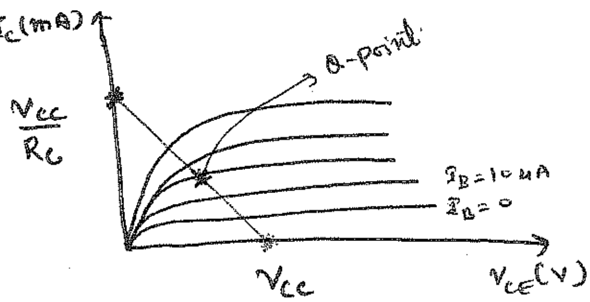
$V_{CE} = V_{CC} - I_C R_C$

case i)

$V_{CE}\big|_{I_C=0} = V_{CC}$

case ii) $V_{CE} = 0$

$I_C\big|_{V_{CE}=0} = \frac{V_{CC}}{R_C}$



i.e Q-point changes by changing the following parameters.

i) I_C can change by varying I_B

ii) if V_{CC} is fixed & R_C changes

iii) if R_C is fixed and V_{CC} is changed.

Advantage:

- Simple.
- Calculations are simple.

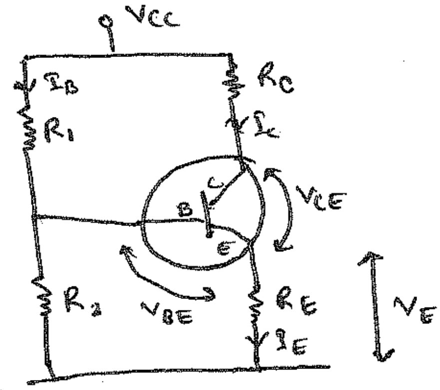
Disadvantages:

i) High S and hence strong chances of thermal runaway.

ii) Poor Stability. there is no means of stoping ↑e in I_C due to I_{CBO}, as I_B is always fixed.

Voltage Divider Bias Method / Self Bias:

This is the most commonly used method for stabilizing & biasing of a transistor.



The resistors R_1 and R_2 will divide the supply voltage and across R_2 will forward bias the Emitter-Base junction.

Approximate Analysis:

1. In this method two resistance R_1 & R_2 are connected across the supply voltage Vcc
2. R_1 & R_2 provide biasing.
3. R_E provide stabilization to the circuit.
4. Voltage drops across R_2 i.e ~~FB~~ E-B junction in FB.

→ Collector Current (I_C):

$I_B \to I_1$

{ I_1 is the current flowing throu' R_1 since I_B is very small current through R_2 is approximately I_1.

$$I_1 = \frac{V_{cc}}{R_1+R_2}$$

voltage across R_2 : $V_2 = R_2 I_1$

$$V_2 = R_2 \cdot \frac{V_{cc}}{R_1+R_2}$$

Applying KVL to the input part:

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + R_E I_E$$

$$\Rightarrow \quad I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since: $I_E \simeq I_c$ $\quad (\because I_E = \underset{\underset{\sim 0}{\downarrow}}{I_B} + I_C)$

$$\boxed{I_c = \frac{V_2 - V_{BE}}{R_E}}$$

$\Rightarrow$ I_c is independent of β.

$\rightarrow$ $V_{BE} << V_2$ i.e I_c is independent of V_{BE}

So in this circuit I_c is independent of transistor parameter and hence a good stabilization is ensured.

Hence potential divider circuit has become universal method for dividing voltage and used for stabilizing and biasing.

- Collector-emitter voltage:- (V_{CE})

Applying KVL to output.

$$V_{CC} = I_c R_c + V_{CE} + I_E R_E$$

as $I_c \sim I_E$

So,

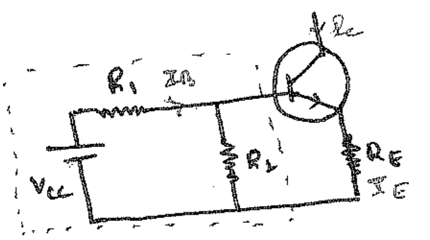
$$V_{CC} = I_c(R_c + R_E) + V_{CE}$$

$$\boxed{V_{CE} = V_{CC} - I_c(R_c + R_E)}$$

Since, I_c and V_{CE} are both independent of β, Q-point doesnot change with change in transistor parameters.

Exact Analysis / Stability factor for potential Divider Bias :-

Drawing the input part and replacing it by the thevenin Equivalent circuit



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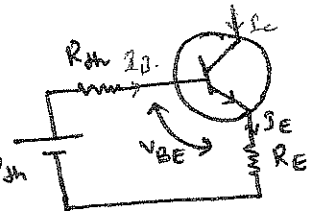


Thevenin Equivalent circuit.

as $R_1 \parallel R_2$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{th} = I_1 R_2$$

$$V_{th} = \frac{V_{CC} R_2}{R_1 + R_2}$$

Applying KVL in The input loop.

$$V_{th} = R_{th} I_B + V_{BE} + I_E R_E \rightarrow (1)$$

$$I_E = I_C + I_B$$

$$I_E = I_B + \beta I_B$$

$$I_E = (1+\beta) I_B \rightarrow (2)$$

Substituting (2) in (1)

$$\Rightarrow V_{th} = R_{th} I_B + V_{BE} + (1+\beta) I_B \cdot R_E$$

$$\boxed{I_B = \frac{V_{th} - V_{BE}}{R_{th} + R_E(1+\beta)}}$$

~~Hence~~, I_B is depending on β as Temp. ↑es β ↑es and hence I_B ↓es, which reduces I_C maintaing the stabilization and Avoid thermal runaway.

Stability factor:

$$S = \frac{(1+\beta)(R_{th}+R_E)}{(R_{th}+R_E+\beta R_E)}$$

Proof.

As,

$$V_{th} = R_{th} I_B + V_{BE} + I_E R_E$$

$$= I_B R_{th} + V_{BE} + (I_B + I_c) R_E$$

$V_{BE} \simeq 0$

Differentiating w.r.t I_c

$$\frac{dV_{th}}{dI_c} = R_{th}\frac{dI_B}{dI_c} + 0 + R_E \frac{dI_B}{dI_c} + R_E$$

or

$$0 = \frac{dI_B}{dI_c}(R_{th}+R_E) + R_E$$

$$\frac{dI_B}{dI_c} = \frac{-R_E}{(R_{th}+R_E)}$$

General expression for $S = \dfrac{1+\beta}{1-\beta\dfrac{dI_B}{dI_c}}$

$$S = \frac{(1+\beta)}{1-\beta\left(\dfrac{-R_E}{R_{th}+R_E}\right)}$$

$$\boxed{S = \frac{(1+\beta)(R_{th}+R_E)}{R_{th}+R_E+\beta R_E}}$$

$$S = \frac{(1+\beta)\left(1+\dfrac{R_{th}}{R_E}\right)}{\dfrac{R_{th}}{R_E}+1+\beta}$$

$R_{th} = \dfrac{R_1 R_2}{R_1+R_2}$

⇒ If the ratio $\dfrac{R_{th}}{R_E}$ is very small, $\dfrac{R_{th}}{R_E}$ can be neglected

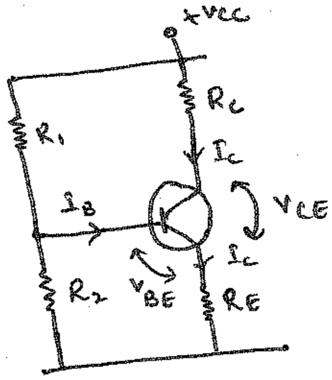
thus, $S = \dfrac{(1+\beta)}{(1+\beta)} = 1 \Rightarrow \boxed{S=1}$

Smallest possible value of S that gives maximum possible stability.

Due to design consideration $\frac{R_H}{R_E}$ has a value that can't be neglected in comparison to 1. So in actual practice the ckt may have $S = 10$.

Numericals

For the circuit given below, find I_c and V_{CE}. Given the values of $R_1 = 39 k\Omega$, $R_2 = 39 k\Omega$, $R_C = 4 k\Omega$, $R_E = 5 k\Omega$ and $\beta = 140$ and $V_{CC} = 18V$



So $I_c = \beta I_B$
and $V_{CE} = V_{CC} - I_c(R_c + R_E)$.

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = 3.55 K$$

$$V_{th} = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = 1.64V$$

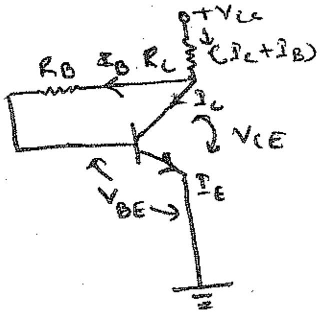
$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + R_E(1+\beta)} = 4.37 \mu A.$$

$$\boxed{I_c = \beta I_B = 0.612 mA.}$$

$$V_{CE} = V_{CC} - I_c(R_c + R_E)$$

$$\boxed{V_{CE} = 12.63V}$$

Stability factor of collector-to-Base bias circuit:



KVL to input loop:

$$V_{cc} = R_c(I_B + I_c) + I_B R_B + V_{BE}$$

$$V_{cc} = I_B(R_B + R_c) + I_c R_c + V_{BE}$$

$$I_B(R_B + R_c) = V_{cc} - V_{BE} - I_c R_c$$

$$I_B = \frac{V_{cc} - V_{BE} - I_c R_c}{R_B + R_c} \longrightarrow (1)$$

and $I_c = \beta I_B \longrightarrow (2)$

KVL to output loop:

$$V_{cc} = R_c(I_B + I_c) + V_{CE}$$

or $V_{CE} = V_{cc} - R_c(I_B + I_c) \longrightarrow (3)$

Stability factor:

$$S = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_c}}$$

$\therefore$ Differentiating eqn (1) i.e I_B w.r.t I_c we get

$$\frac{dI_B}{dI_c} = \frac{-R_c}{R_B + R_c}$$

$$\therefore \quad S = \frac{1+\beta}{1 + \beta\left(\frac{R_c}{R_B + R_c}\right)}$$

Comments:

→ If $R_B \ll \beta R_c$

$$S \simeq \frac{1+\beta}{1 + \beta\left(\frac{R_c}{R_c}\right)}$$

$$\boxed{S \simeq 1}$$

→ Provides better thermal Stability by making $R_B << \beta R_C$

→ Stability factor is very much less than that of fixed bias circuit.

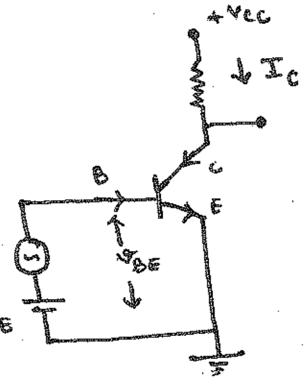
* The operating point of collector-to-Base bias circuit is given by (I_C, V_{CE}) as given by Equations ② and ③.

Small Signal Model:-

→ to find ac current & ac voltage.

In This we will be using both ac and dc signal → To operate transistor in active region. Thus find ac current and ac voltage.

Let us consider the circuit as



v_{be} → ac voltage

V_{BE} → dc voltage

v_{BE} → Total voltage

Total voltage = $\underbrace{v_{be}}_{ac} + \underbrace{V_{BE}}_{dc}$

$$\boxed{v_{BE} = v_{be} + V_{BE}} \rightarrow (1)$$

I_c → dc current

i_c → ac current

i_C → total current ⇒ $\boxed{i_C = i_c + I_C} \rightarrow (2)$

As we know Current Eqn: $I = I_s (e^{V/V_T})$

dc current:

$$I_C = I_s (e^{V_{BE}/V_T}) \rightarrow (3)$$

Total current

$$i_C = I_s (e^{v_{BE}/V_T}) \rightarrow (4)$$

$$i_C = I_s (e^{(v_{be} + V_{BE})/KT})$$

$e^{a+b} = e^a . e^b$

$$i_C = I_s (e^{v_{be}/KT} . e^{V_{BE}/KT})$$

$$i_C = e^{v_{be}/KT} . \underbrace{I_s e^{V_{BE}/KT}}_{\text{dc current (from eqn. (3))}}$$

$$i_c = I_c \, e^{v_{be}/V_T}$$

$$e^{a/b} = (1 + a/b)$$

$$i_c = I_c\left(1 + \frac{v_{be}}{V_T}\right)$$

$$\underset{\text{total current}}{i_c} = \underbrace{I_c}_{\text{dc sig.}} + \underbrace{I_c \frac{v_{be}}{V_T}}_{\text{ac signal}}$$

ac Current: $\boxed{i_c = I_c \cdot \frac{v_{be}}{V_T}}$ → ac current across the Collector.

→ Collector Current:

$$\boxed{i_c = I_c \cdot \frac{v_{be}}{V_T}}$$

here $\frac{I_c}{V_T}$ ⇒ trans conductance g_m

As resistance is inverse of Conductance

So,

$$\boxed{r_c = \frac{1}{g_m}}$$

Collector Current using g_m:

$$\boxed{i_c = g_m \cdot v_{be}}$$

→ Base current using collector current:

$$i_b = i_c/\beta$$

$$i_b = \frac{I_c}{\beta} \cdot \frac{v_{be}}{V_T}$$

$$\boxed{i_b = g_m \cdot \frac{v_{be}}{\beta}}$$

Base resistance:

$$\boxed{r_\pi = r_b = \beta/g_m}$$

$$\boxed{i_b = \frac{1}{r_\pi} \cdot v_{be}}$$

→ Emitter Current using Collector Current:

we know

$$i_e = i_c + i_b \longrightarrow i_c/\beta$$

$$= i_c\left(1 + \frac{1}{\beta}\right)$$

$$\boxed{i_e = \left(I_c \cdot \frac{v_{be}}{V_T}\right)\left(1 + \frac{1}{\beta}\right)}$$

$$i_e = g_m \cdot v_{be}\left(1 + \frac{1}{\beta}\right)$$

$$r_e = \frac{1}{g_m\left(1 + \frac{1}{\beta}\right)}$$

$$\boxed{i_e = \frac{1}{r_e} \cdot v_{be}}$$

Hybrid Parameters or h-parameter / hybrid Model:-

In order to predict the behaviour of a small-signal transistor amplifier, it is important to know its operating characteristics e.g. input impedance, output impedance, voltage gain etc.

Reasons for using h-parameter: (in describing the characteristics of a transistors).

i) It yields exact results because the inter-effects of input and output circuits are taken into account.

ii) These parameters can be measured very easily.

→ h-parameters of a Linear Circuit:

Every linear circuit having input and output terminals can be analysed by four parameters one measured in ohm, one in siemens($\mho$) and two dimensionless) called h-parameters.

Let us consider a linear circuit such that (i_1, v_1) are the input current and voltage. (v_2, i_2) are the output current and voltage.

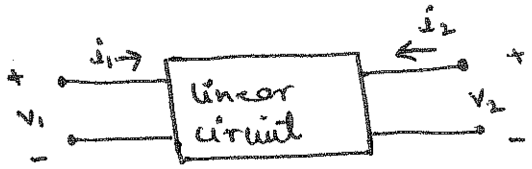


Fig. 1.

Standard Convention:-

$i_1, i_2 \rightarrow$ flow into the box
$v_1, v_2 \rightarrow$ positive from upper to lower terminal
$v_2, i_1 \rightarrow$ independent variables
$v_1, i_2 \rightarrow$ dependent variables

$$v_1 = f(i_1, v_2) \quad \text{and} \quad i_2 = f(i_1, v_2)$$

$$dv_1 = \left(\frac{\partial v_1}{\partial i_1}\right) di_1 + \left(\frac{\partial v_1}{\partial v_2}\right) dv_2 \rightarrow (1)$$

$$di_2 = \left(\frac{\partial i_2}{\partial i_1}\right) di_1 + \left(\frac{\partial i_2}{\partial v_2}\right) dv_2 \rightarrow (2)$$

can re-write ① & ② as

$$v_1 = h_{11} i_1 + h_{12} V_2 \rightarrow ③$$

$$i_2 = h_{21} i_1 + h_{22} V_2 \rightarrow ④$$

In Matrix-form:

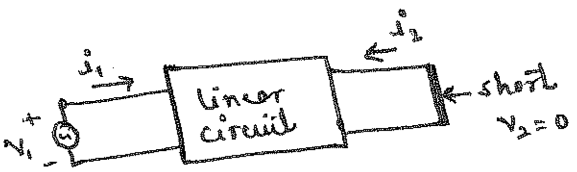
$$\begin{bmatrix} V_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ V_2 \end{bmatrix}$$

Once, the h-parameters are known eqn. ③ + ④ can be used to find out the voltages and currents in the circuit.

- <u>Determination of h parameters;</u>

The h-parameters of fig. 1 can be determined as:

i) short-circuit the output terminal (i.e $V_2 = 0$).



So,

$$V_1 = h_{11} i_1 + h_{12} \times 0$$

$$i_2 = h_{21} i_2 + h_{22} \times 0$$

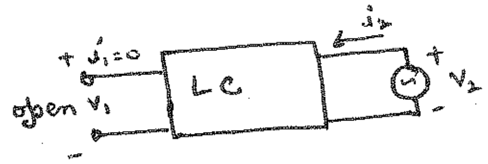
$\Rightarrow$ $h_{11} = \left.\dfrac{V_1}{i_1}\right|_{V_2 = 0}$ output shorted

$h_{21} = \left.\dfrac{i_2}{i_1}\right|_{V_2 = 0}$ output shorted

$\Rightarrow$ $h_{11} \rightarrow$ Input impedance with output shorted

$h_{21} \rightarrow$ Current gain with output shorted

ii) Input terminal open i.e $i_1 = 0$



So,

$$V_1 = h_{11} \times 0 + h_{12} V_2$$

$$i_2 = h_{21} \times 0 + h_{22} V_2$$

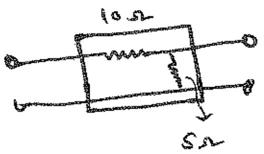
$\Rightarrow$ $h_{12} = \left.\dfrac{V_1}{V_2}\right|_{i_1 = 0}$ input open

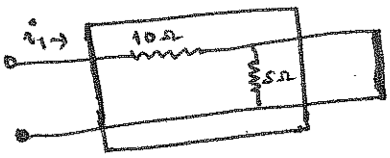
$\Rightarrow$ $h_{22} = \left.\dfrac{i_2}{V_2}\right|_{i_2 = 0}$ input open.

$\Rightarrow$ $h_{12} \rightarrow$ Reverse voltage feedback ratio with input open.

$h_{22} \rightarrow$ output conductance with input open.

Find the h parameters of the circuit:





$h_{11} = 10\,\Omega$

$h_{21} = \dfrac{i_2}{i_1} = \dfrac{-i_1}{i_1} = -1$

$h_{12} = \dfrac{V_1}{V_2}$ as $V_1 = V_2$ $\Rightarrow h_{12} = 1.$

$h_{22} = \dfrac{1}{5} = 0.2\ S$

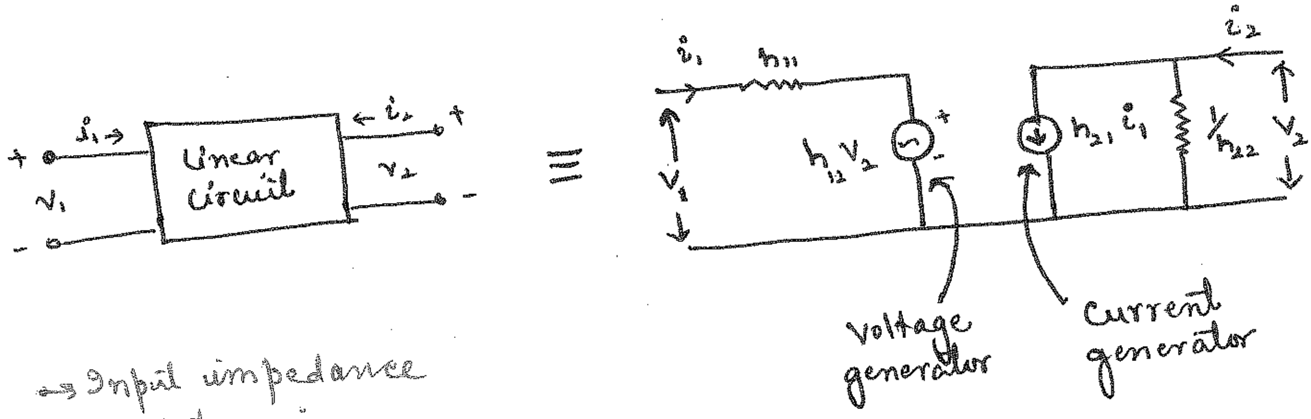
Summary table:

Parameters	Meaning	Condition
h_{11}	Input resistance	output shorted
h_{12}	Reverse voltage feedback ratio.	Input open
h_{21}	current gain	output shorted
h_{22}	output Conductance	Input open.

h-parameter Equivalent Circuit :-

$$v_1 = h_{11} i_1 + h_{12} V_2 \rightarrow (1) \text{ (input part)}$$
$$i_2 = h_{21} i_1 + h_{22} V_2 \rightarrow (2) \text{ (output part)}$$

general Eq^n.

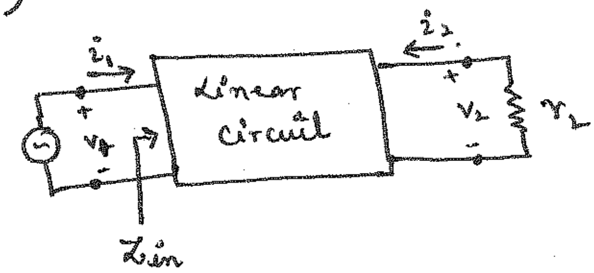


→ Input impedance
→ current gain
→ voltage gain
→ output impedance.

~~h-parameter equivalent circuit (CE configuration)~~

(1) Input impedance :- (Z_{in})

Consider a Linear Circuit with a load resistance r_L across its terminal.



$$Z_{in} = \frac{V_1}{i_1} \rightarrow (1)$$

as $\quad v_1 = h_{11} i_1 + h_{12} V_2 \rightarrow (2)$

$$Z_{in} = \frac{h_{11} i_1 + h_{12} V_2}{i_1}$$
$$= h_{11} + h_{12} \cdot \frac{V_2}{i_1} \rightarrow (3)$$

Now, $\quad i_2 = h_{21} i_1 + h_{22} V_2 \quad \Big| \quad i_2 = -V_2/r_L$

$$\frac{-V_2}{r_L} = h_{21} i_1 + h_{22} V_2$$

$$\Rightarrow \frac{V_2}{i_1} = \frac{-h_{21}}{h_{22} + \frac{1}{r_L}} \rightarrow (4)$$

-ve sign is used ∵ the actual load current is opposite to the direction of i_2.

Substituting Eqn. (4) in (3), we get.

$$\boxed{Z_{in} = h_{11} - \frac{h_{12} h_{21}}{h_{22} + \frac{1}{r_2}}}$$

<u>Comments:</u>

If either h_{12} or r_2 is very small, then second term can be neglected and

$$\boxed{Z_{in} \simeq h_{11}}$$

(ii) <u>Current gain</u> :- (A_i)

gain of a circuit is given by

$$A_i = \frac{i_2}{i_1}$$

Now $\quad i_2 = h_{21} i_1 + h_{22} V_2$

$$V_2 = -i_2 r_2$$

$$i_2 = h_{21} i_1 - h_{22} i_2 r_2$$

$$i_2 (1 + h_{22} r_2) = h_{21} i_1$$

$$A_i = \frac{i_2}{i_1} = \frac{h_{21}}{1 + h_{22} r_2}$$

$$\boxed{A_i = \frac{h_{21}}{1 + h_{22} r_2}}$$

<u>Comments:</u>

If $h_{22} r_2 << 1$, then

$$\boxed{A_i \simeq h_{21}}$$

(iii). Voltage gain :- (A_v)

Voltage gain of a circuit is given by

$$A_v = \frac{V_2}{V_1}$$

$$A_v = \frac{V_2}{i_1 Z_{in}} \qquad \left(Z_{in} = \frac{V_1}{i_1} \right)$$

From Eqn ④ (input impedance)

$$\frac{V_2}{i_1} = \frac{-h_{21}}{h_{22} + \frac{1}{r_2}}$$

Substituting $\frac{V_2}{i_1}$ in A_v, we get

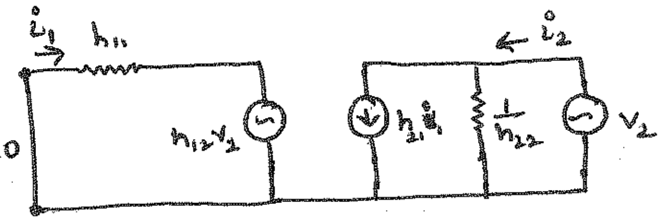
$$\boxed{A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_2}\right)}}$$

(iv) Output impedance: (Z_{out})

To get the Z_{out}, remove the load r_2. Set the signal voltage $V_1 = 0$ and connect a generator of voltage V_2 at the output terminals.

The output impedance is

$$Z_{out} = \frac{V_2}{i_2}$$



with $V_1 = 0$, and applying KVL to input circuit, we have

$$0 = i_1 h_{11} + h_{12} V_2$$

$$i_1 = \frac{-h_{12} V_2}{h_{11}} \rightarrow ①$$

$$i_2 = h_{21} i_1 + h_{22} V_2 \rightarrow ②$$

putting i_1 (①) in Eqn ②

$$i_2 = h_{21}\left(\frac{-h_{12} V_2}{h_{11}}\right) + h_{22} V_2$$

$$i_2 = -\frac{h_{21}h_{12}v_2}{h_{11}} + h_{22}v_2$$

Dividing throughout by v_2, we have

$$\frac{i_2}{v_2} = \frac{-h_{21}h_{12}}{h_{11}} + h_{22}$$

$$\boxed{Z_{out} = \frac{v_2}{i_2} = \frac{1}{h_{22} - \frac{h_{21}h_{12}}{h_{11}}}}$$

* The h Parameters of a Transistor :-

→ For small a.c. signals, a transistor behaves as a linear circuit.

∴ ac operation can be described in terms of h-parameters.

Nomenclature for transistor h parameters :

h parameters	Notation in CB	Notation in CE	Notation in CC
h_{11}	h_{ib}	h_{ie}	h_{ic}
h_{12}	h_{rb}	h_{re}	h_{rc}
h_{21}	h_{fb}	h_{fe}	h_{fc}
h_{22}	h_{ob}	h_{oe}	h_{oc}

i → Input Impedance

r → reverse voltage feedback ratio

f → forward current transfer ratio

o → output admittance.

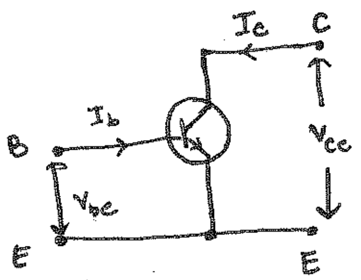
Limitations of h-parameters:

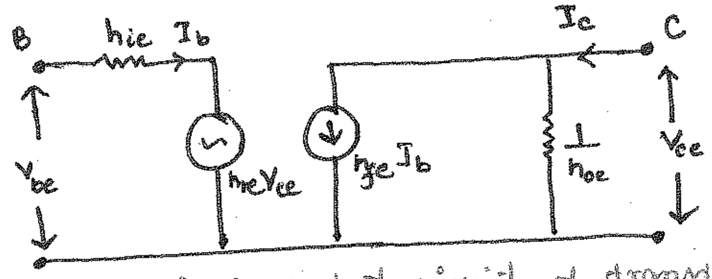
The h-parameter approach provides accurate information regarding the current gain, voltage gain, input impedance and output impedance of a transistor amplifier. However there are two limitations;

i) It is very difficult to get the exact values of h-parameters for a particular transistor.

ii) The h parameter approach gives correct answers for small a.c signals only. It is ∵ a transistor behaves as a linear device for small signals only.

Transistor h parameter Model (CE):





hybrid Equivalent circuit of transistor (CE).

The h parameter a.c equation for this circuit are:

$$V_{be} = h_{ie} I_b + h_{re} V_{ce}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce}$$

here, h_{ie}, h_{fe} → measured with $V_{ce}=0$ (output short-circuited to a.c)

h_{re}, h_{oe} → " " $I_b = 0$ (i.e input open-circuited)

- here h_{re} is very small ($\sim 5\times10^{-4}$), hence $h_{re}V_{ce}$ is very small compare to V_{be}, ∴ $h_{re}V_{ce}$ can be removed from the input side without any large error. which further produces the simplified hybrid equivalent circuit of transistor.

i) Input Impedance:

General Expression:

$$Z_{in} = h_{11} - \frac{h_{12}h_{21}}{h_{22} + \frac{1}{r_L}}$$

$$Z_{in} = h_{ie} - \frac{h_{re}h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

note: r_L is the a.c load seen by the transistor.

ii Current gain:

$$A_i = \frac{h_{21}}{1 + h_{22}r_L}$$

$$A_i = \frac{h_{fe}}{1 + h_{oe}r_L}$$

iii) Voltage gain:

$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

$$A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

iv) output impedance:-

$$Z_{out} = \frac{1}{h_{22} - \frac{h_{21}h_{12}}{h_{11}}}$$

$$Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}}}$$

Q. A transistor used in CE arrangement has the following set h parameters, when the d.c operating point is $V_{CE} = 10$ volts and $I_c = 1mA$:

$h_{ie} = 2000\,\Omega$; $h_{oe} = 10^{-4}\,S$; $h_{re} = 10^{-3}$; $h_{fe} = 50$.

Determine

i) Input impedance
ii) Current gain
iii) voltage gain

The a.c load seen by the transistor is $r_L = 600\,\Omega$.