

< U.J.T >

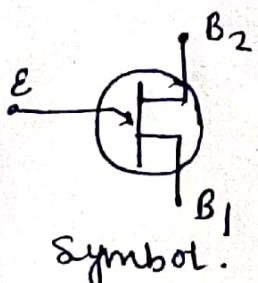
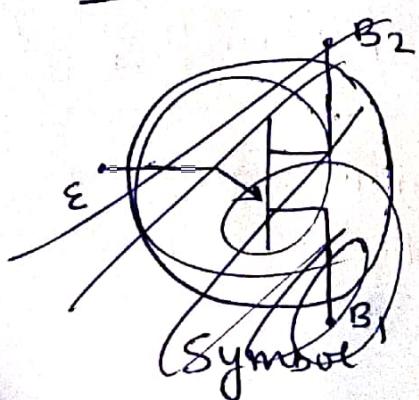
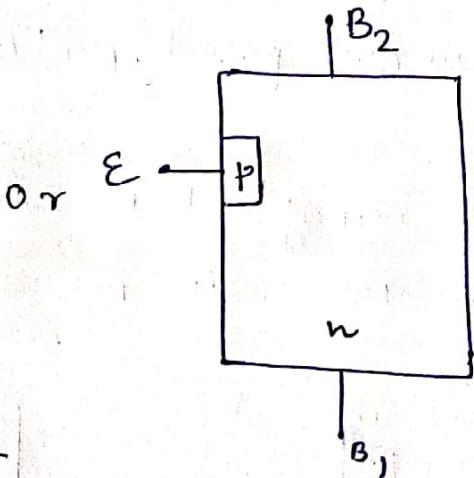
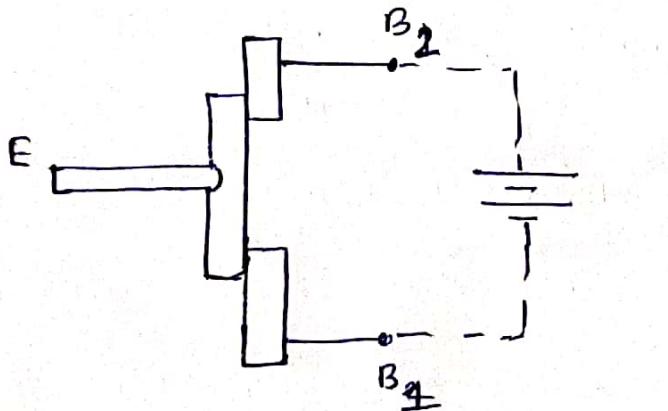
04/11/20.

A UJT is a three terminal solid state device with only one junction.

It has wide variety of application:-

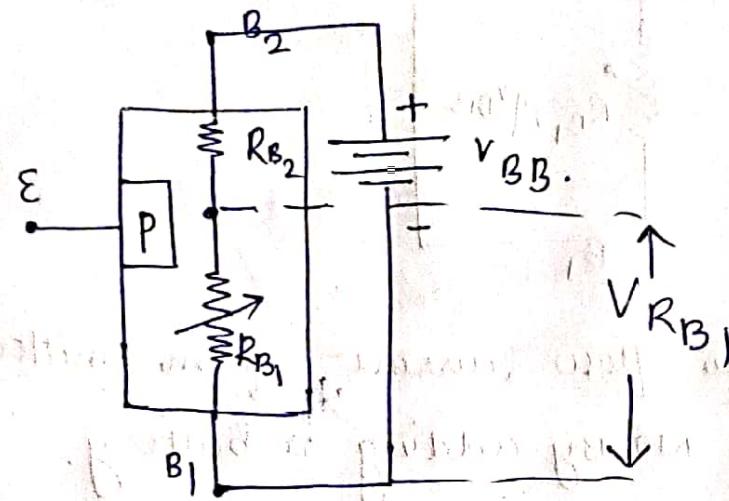
- (i) Oscillator
- (ii) trigger circuit
- (iii) sawtooth generators
- (iv) Phase control.
- (v) Timing circuit
- (vi) Bistable network
- (vii) voltage or current regulated supplies.

Basic construction :-



- UJT is a transistor which has 2 base
- n-type is lightly doped (~~not~~ charge carrier)
- p-type is heavily doped (~~not~~ charge carrier)
- Drawback
↳ do not use as a amplifier.

Working:-



- $R_{B1} > R_{B2}$
 - R_{BB} (inter base resistance) = $R_{B1} + R_{B2}$
 - When emitter diode is open then R_{BB} introduced.
- we want to find the voltage in the resistance of R_{B1} .

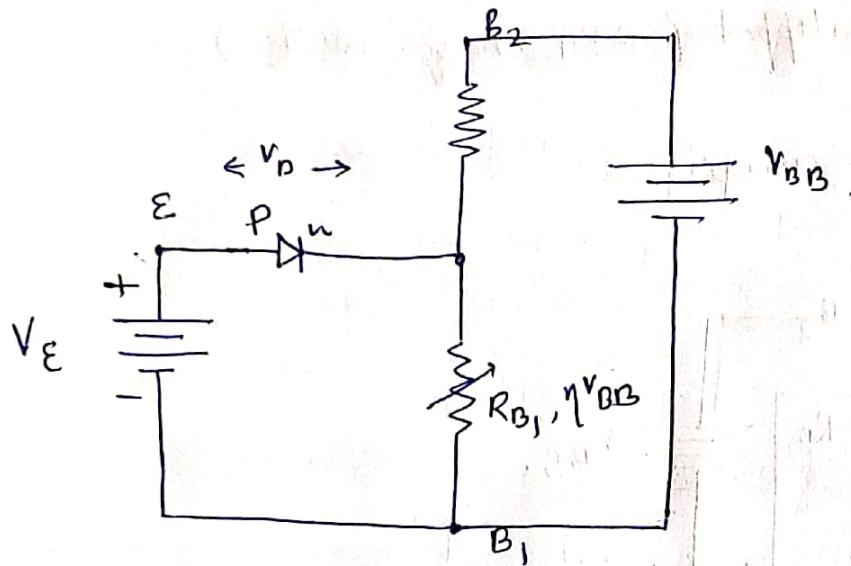
Now,
by voltage divider rule.

$$V_{R_{B1}} = \frac{R_{B1}}{(R_{B1} + R_{B2})} \times V_{BB}$$

$$V_{R_{B1}} = \eta V_{BB}$$

$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$
 η = Intrinsic stand off ratio.

Equivalent circuit



- we want to flow current from Emitter (e) to base (B1). ~~so~~ By adding a battery.

→ When there is no voltage in the emitter (e) then V_{BB} is with higher potential than positive current is entering through (n) then the diode become reverse bias and current will not flow. ($V_e < nV_{BB} + v_D$). Leaking current in reverse direction

→ If we want to make the diode forward bias then we have to get the following condition.

$$V_e \geq nV_{BB} + v_D$$

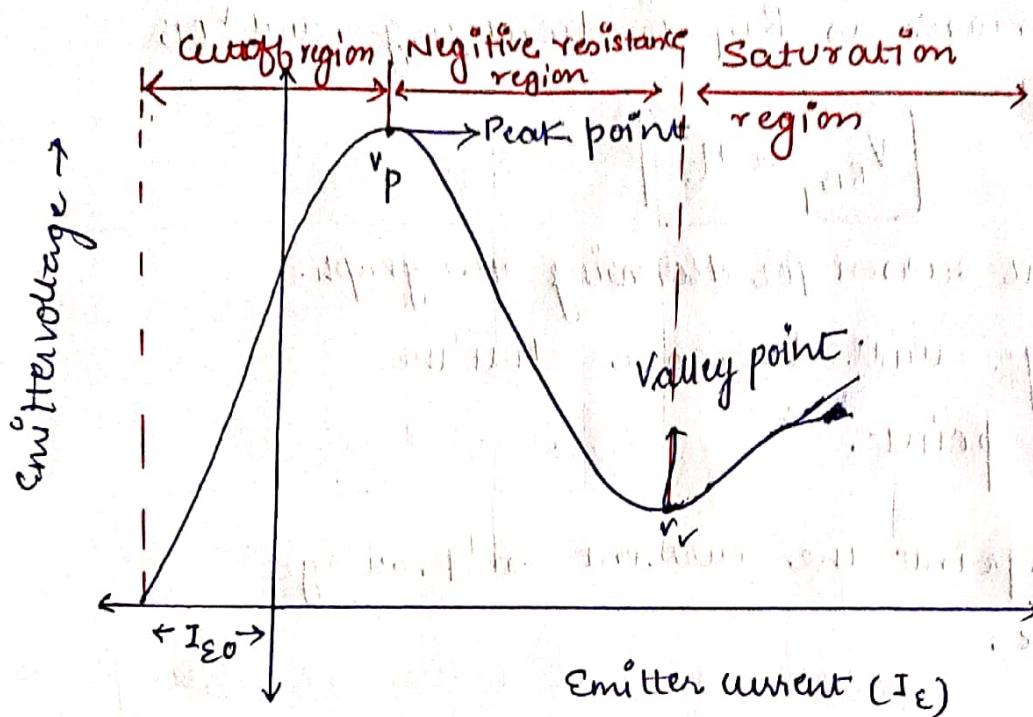
$$\left\{ \begin{array}{l} v_D = \text{diode potential} \\ \end{array} \right.$$

↓ condition when

UJT start working.

→ When we increase the (V_E) then current will increase in resistance (R_{B1}), and R_{B1} decrease and thus

→ characteristic curve.



- (i) When ($V_E = 0$) then reverse current will flow in the diode which is shown by (I_{E0}) in graph.
- (ii) Then we apply (V_E) voltage and we are increasing voltage (V_E) by which emitter current is also increasing. At some point when voltage is maximum and that point is denoted by (V_p) Peak point.
- (iii) After peak point (V_p) the current is increasing and resistance is decreasing so voltage is also decreasing in the graph by the relation.

$$V_{RB_1} = \left(\frac{RB_1}{RB_1 + RB_2} \right) V_{BB}$$

As RB_1 is decreasing now by the relation

$$V_{RB_1} = \eta V_{BB}$$

η will decrease as RB_1 is decreasing and V_{BB} is constant

$$\boxed{V_{RB_1} \propto \eta}$$

∴ This is the reason for decreasing the graph.
and the voltage will decrease till the
~~valley~~ Valley point.

(iv) After valley point the current and voltage will increase.

^{} VJT as Relaxation oscillator:-

what is oscillator?

→ oscillator are the electronic circuit which are used to generate wave form like sine wave, cosine waves, triangular waves, sawtooth wave etc.

oscillator.

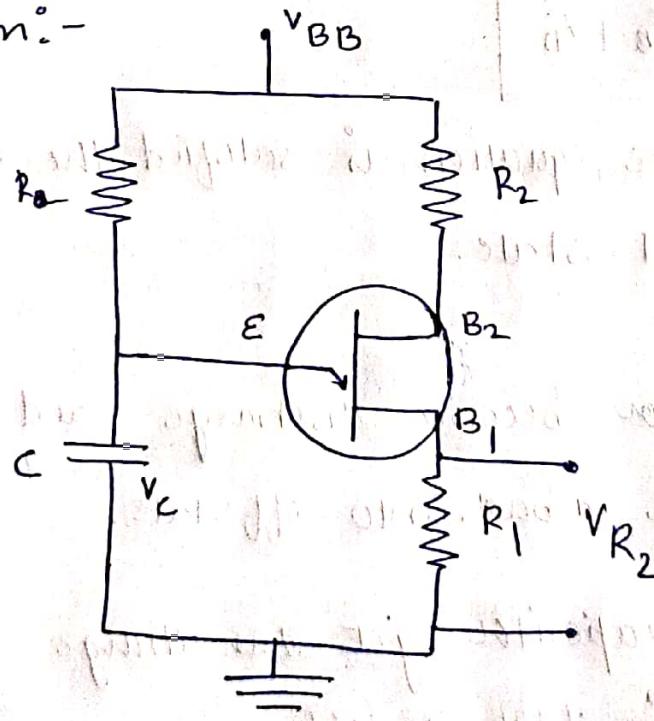
↓
linear oscillator

e.g - sinusoidal waveform

^{} Relaxation oscillator.

e.g - non-sinusoidal waveform.

Circuit diagram:-



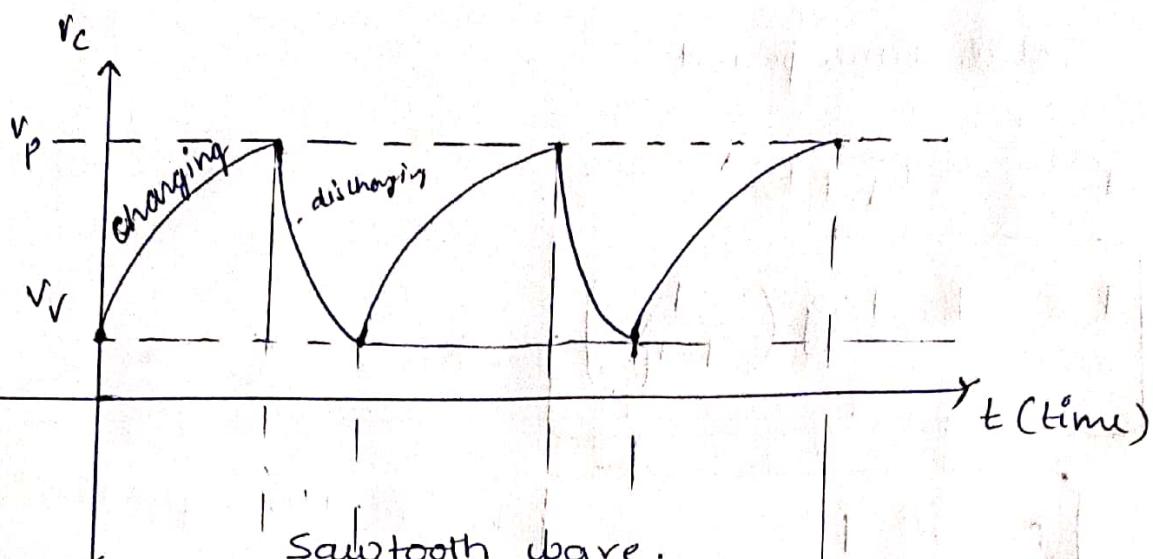
V_c = charge across capacitor.

Working of circuit:-

- (i) When we give supply (V_{BB}) to the circuit the capacitor get charged and it developed a voltage across itself and that voltage is (V_c)
- (ii) When capacitor become fully charge or V_c is maximum then a current will flow through emitter to base (B_1). But for this flow of current there is a certain condition that the (V_c) capacitor voltage have to fulfill.
- ∴
$$V_c = \eta V_B + V_D$$

When the above equation is satisfied the UJT will get into ON state.

- (iii) Then capacitor become discharge and then UJT become back into off state.
- (iv) Then again capacitor get ~~stuck~~ charge and it will again turn on UJT.

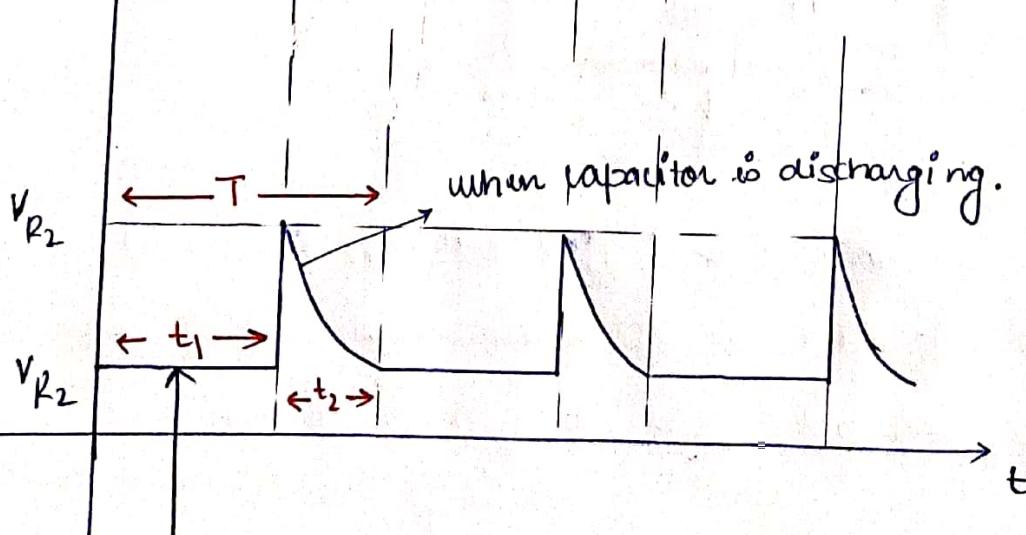


- why capacitor is discharging quickly and it is taking time to get charged?

(Ans - 1)

The resistance (R) in the circuit diagram is very high. So it will take time to get charged. And R_1 has less resistance and R_B has negative resistance, so it takes less time to get discharge!

when we want signal at output.



Relay (when capacitor is charging)

Total time period.

$$T = t_1 + t_2$$

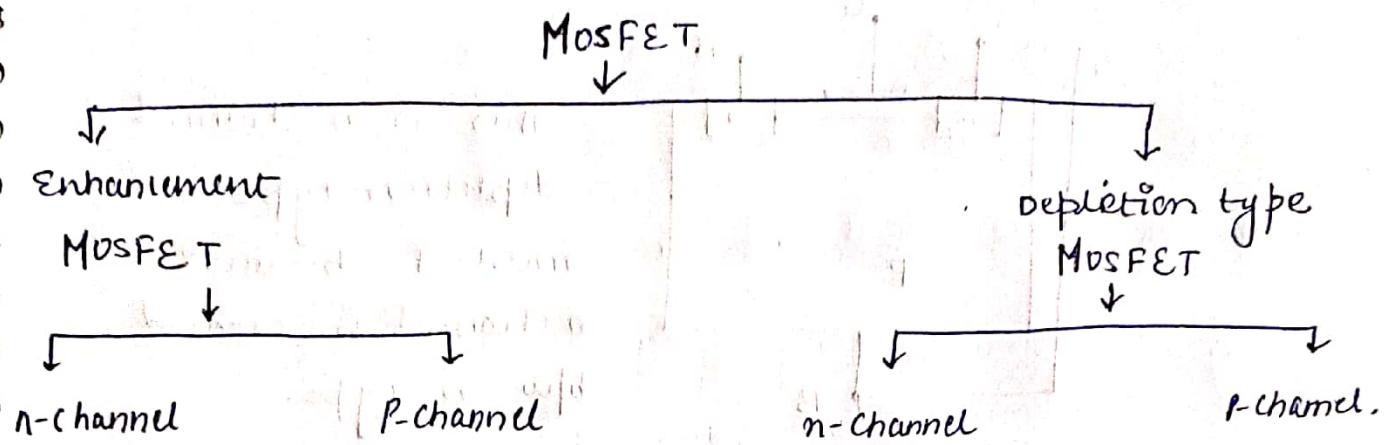
$$T = RC \log\left(\frac{1}{1-\eta}\right)$$

$$f = \frac{1}{RC \log\left(\frac{1}{1-\eta}\right)}$$

< MOSFET >

05/11/20

- ~~Mosfet~~ It stand for metal - oxide - semiconductor field effect transistor.

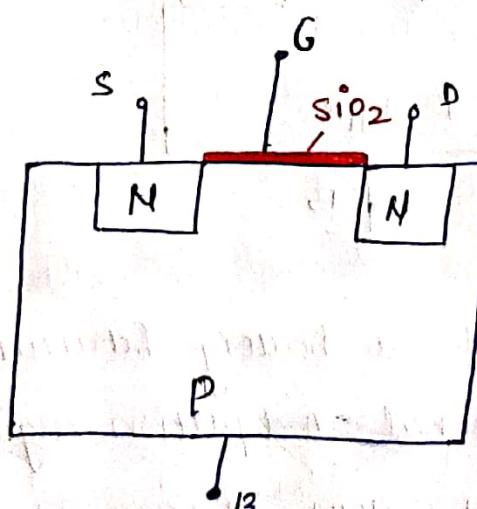


→ why we are studying MOSFET?

→ MOSFET are used in phone processor, laptop processor
eg Intel (i3, i5, i7), snapdragon 635, 666 etc)

→ In a small chip there are approx. 1 crore MOSFET.

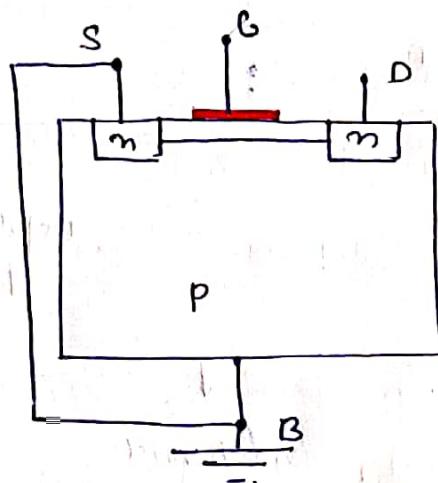
The smaller size of MOSFET increase battery life.



→ Enhancement type.

SiO_2 is insulator.

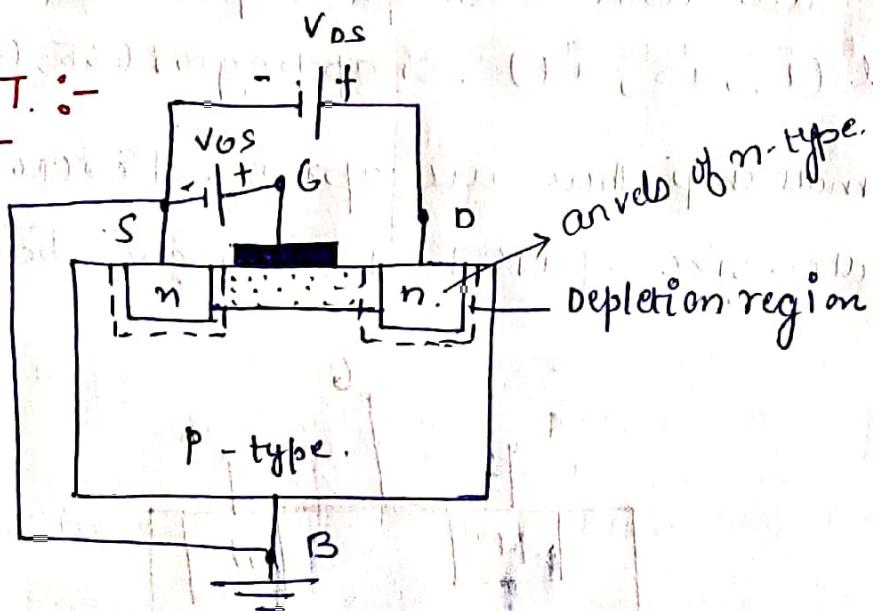
MOSFET is also known as IGFET (Insulated Gate field effect transistor)



This is n-channel depletion type mosfet because a channel is created b/w n-type.

Depletion type MOSFET.

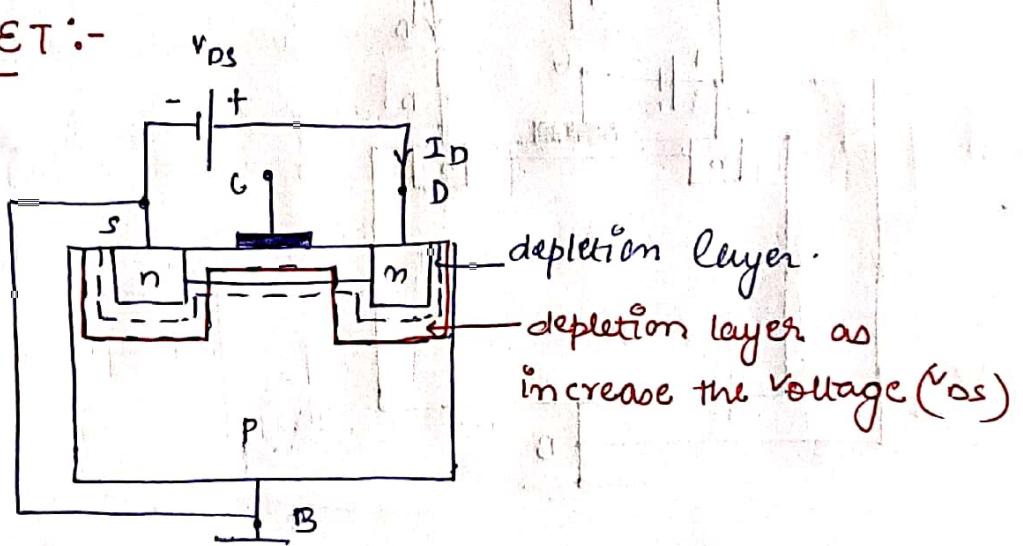
E- MOSFET :-



- When we connect a battery between source (S) and Drain (D) terminal. A depletion region is formed and charge will not flow from n to n.

- Then we will provide (V_{GS}) battery between source(s) and gate (G) terminal. Then current will flow because of the minority charge carrier electron in p-type. get attracted towards towards gate terminal. But due to SiO_2 thin layer they will not pass. Due to these electron ~~will be blocked by H-~~ a channel is created.
- E MOSFET does not have channel we create channel by providing $V_H(V_{GS})$ voltage.

D-MOSFET:-



Case-1) When $V_{GS} = 0$:

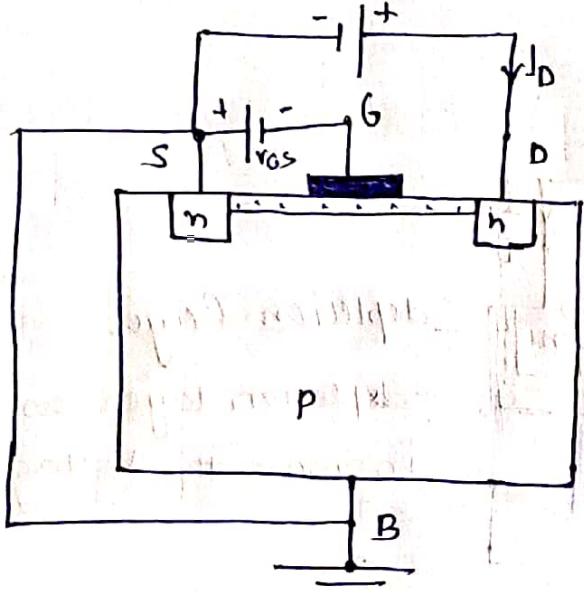
As we know V_{DS} is positive then current I_D will flow.

As we increase V_{DS} the current I_D will also increase at some point when we increase V_{DS} , I_D will not increase it become constant.

In this situation the n-type is connected to positive terminal and p-type is connected to negative terminal. Then our MOSFET is in reverse bias condition.

As we know in reverse bias the depletion region become thick and it will provide less path to flow of current.

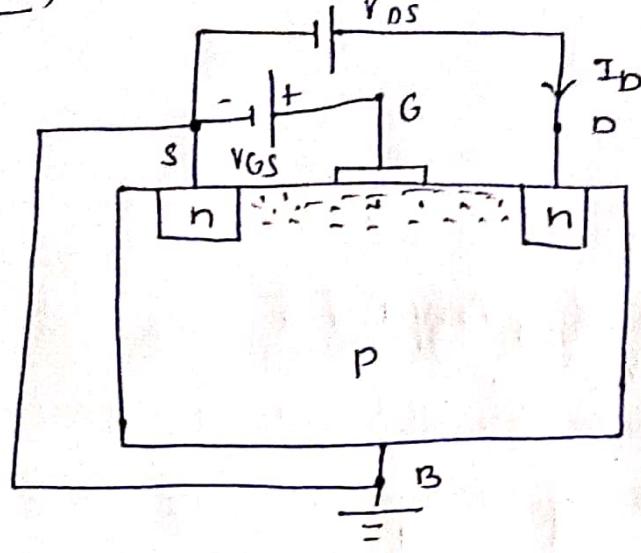
Case - II) when $V_{GS} = -ve$.



- When V_{GS} is negative, then the electron is present in the channel is repelled and thus our channel will become thin and thus current I_D will also decrease.

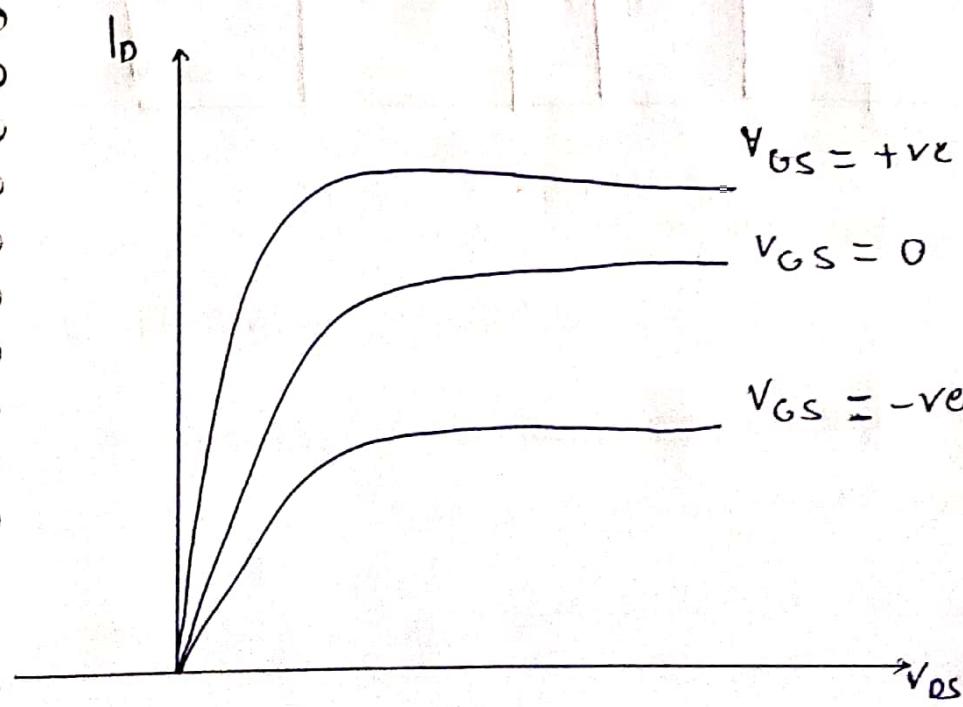
$$I_{D2} < I_{D1}$$

Case-III) when $V_{GS} = +ve.$



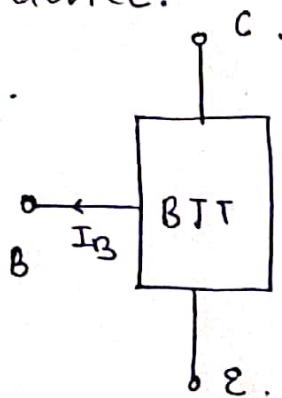
when $V_G V_{GS}$ is positive it will attract all the electron from p-type semiconductor and thus channel become thicker and the value of current (I_{D_3}) will increase very high.

$$I_{D_3} > I_{D_1} > I_{D_2}$$



B J T

- Three terminal device.



- Current control device.

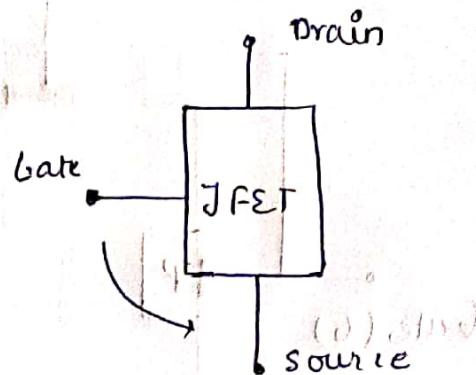
→ we use base current to control output current

- Bipolar (The current will flow due to electron and hole).

* n-p-n is better than p-n-p because current is due to electron. as the mobility of electron is greater as compared to hole.

J F E T

- Three terminal device



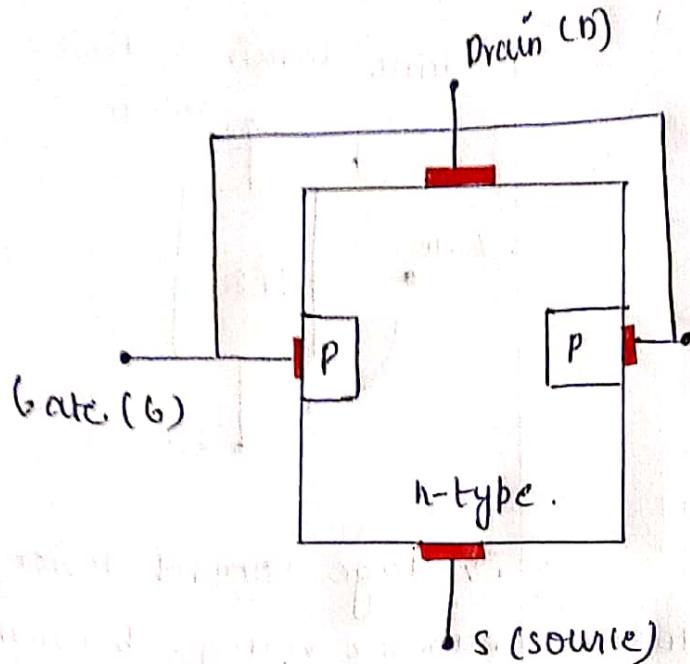
- Voltage control device.

→ The voltage between Gate and source or (V_{GS}), with the help of V_{GS} we control the output voltage.

- unipolar (The current will flow due to electron then it will called **n-channel**)

JFET. If current will flow due to hole then it will called **p-channel** JFET.

N-channel JFET:-



Source :- the path where charge carrier enters

Drain :- The path where charge carrier leaves

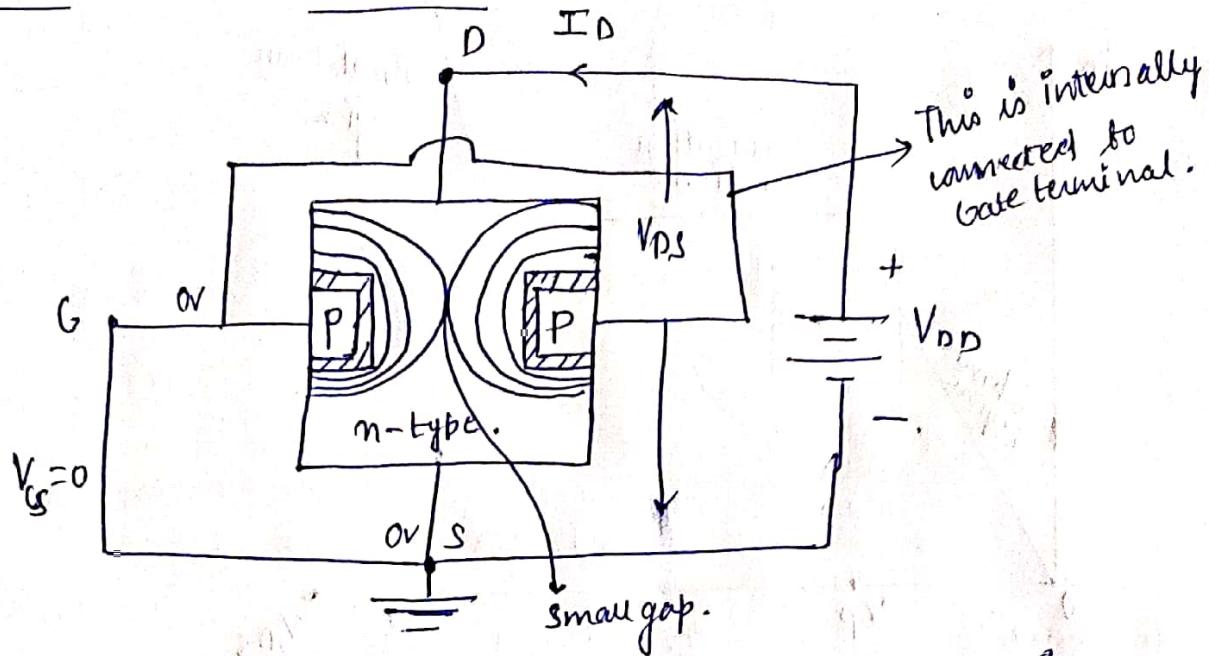
Gate :- control the conduction.

working:-

case 1) $V_{GS} = 0$; $V_{DS} > 0$, A_D

case 2) $V_{GS} < 0$; $V_{DS} > 0$

Case-1) when $V_{GS} = 0$



V_{DS} = Potential difference between source and drain

Here n-type is at higher potential and p-type is at lower potential than the. Diode is in reverse bias.

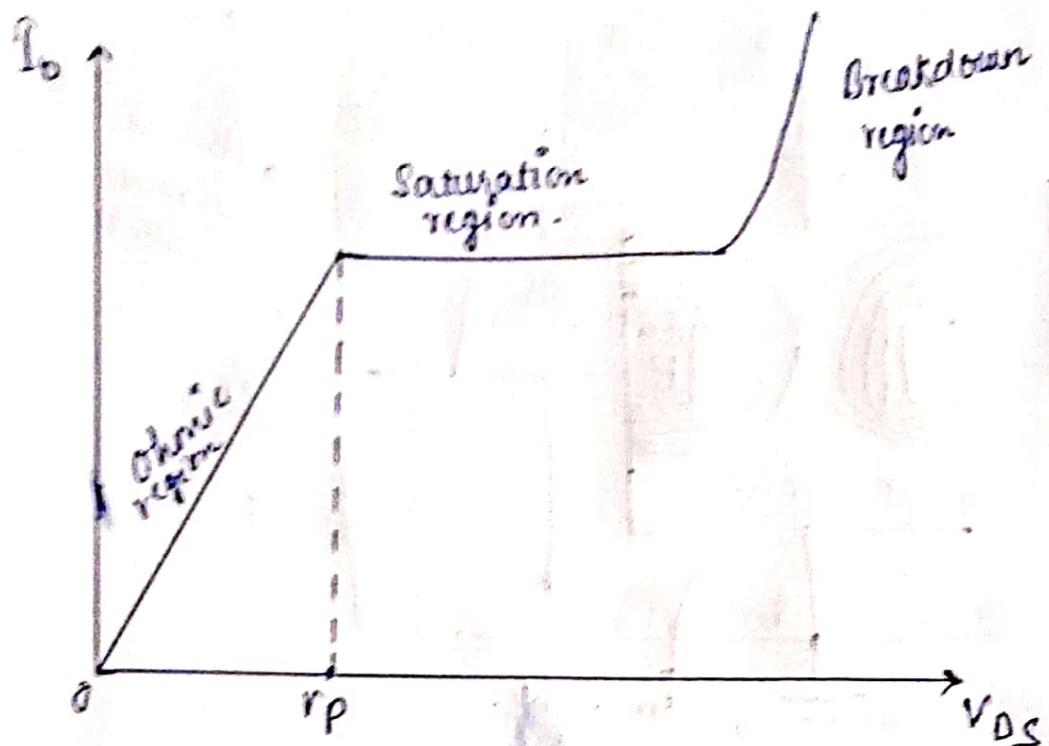
→ due to which depletion region increase. towards higher potential.

This lead to

The current will become because it will not get path due to depletion region.

But the depletion region do not meet because the reverse bias situation did not get eliminated.

At V_p = Pinch off [where current become constant]



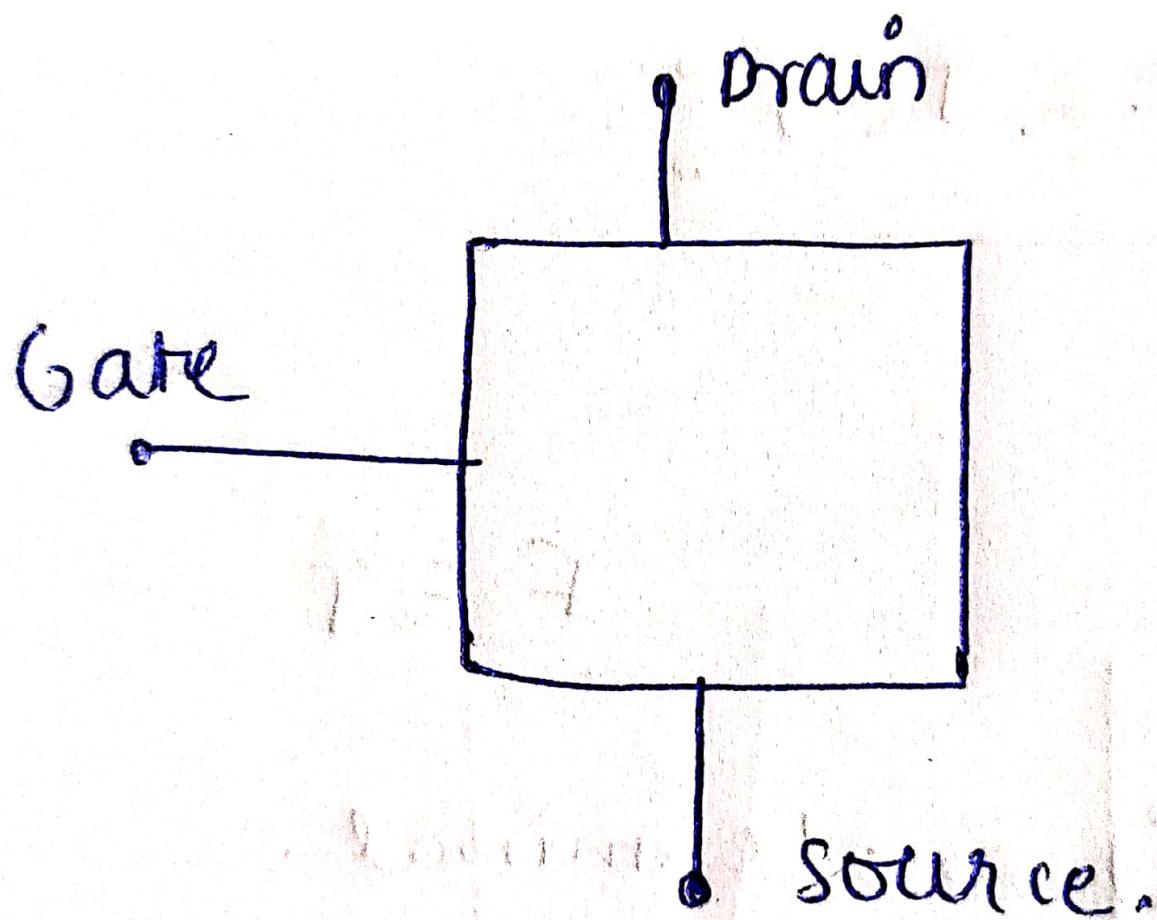
Field Effect transistor (FETs) :-

BJT

- (i) 3-terminal.
- (ii) Bipolar.
- (iii) Current control device.
- (iv) Noisy.
- (v) Large size.
- (vi) Low density.
- (vii) Low input impedance.

FET

- (i) 3-terminal.
- (ii) Unipolar.
- (iii) Voltage control device.
- (iv) Less noisy.
- (v) Small size. = $\frac{1}{5}$ th of BJT.
- (vi) High density.
- (vii) High input impedance.



FETs thru terminal.

hcl ° = Bi Th