# ANALOG CIRCUITS

## DAY-4

# TRANSISTOR BIASING

The basic function of transistor is amplification.

The process of raising the strength of weak signal without any change in its general shape is referred as faithful amplification.

For faithful amplification it is essential that :

- Emitter-Base junction is forward biased
- Collector- Base junction is reversed biased
- Proper zero signal collector current

# *DEFINITION*

**The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is called transistor biasing**

**or**

To operate the transistor in the desired region, we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is known as biasing of the transistor. Since DC voltages are used to bias the transistor, it is called as DC biasing.

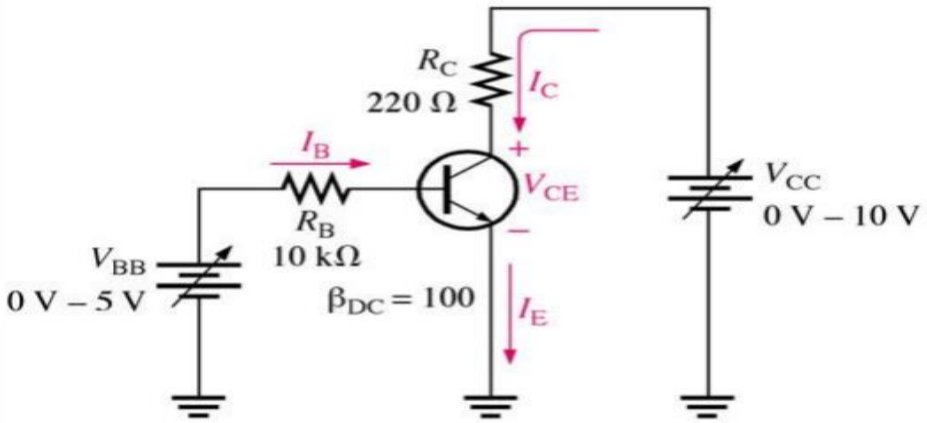
# DC OPERATING POINT :

- Application of DC voltages (bias) establishes a fixed level of current and voltage.
- For transistor amplifiers the resulting DC current and voltage establishes an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Since the operating point is a fixed point on the characteristics, it is called as Quiescent point (Q - Point).

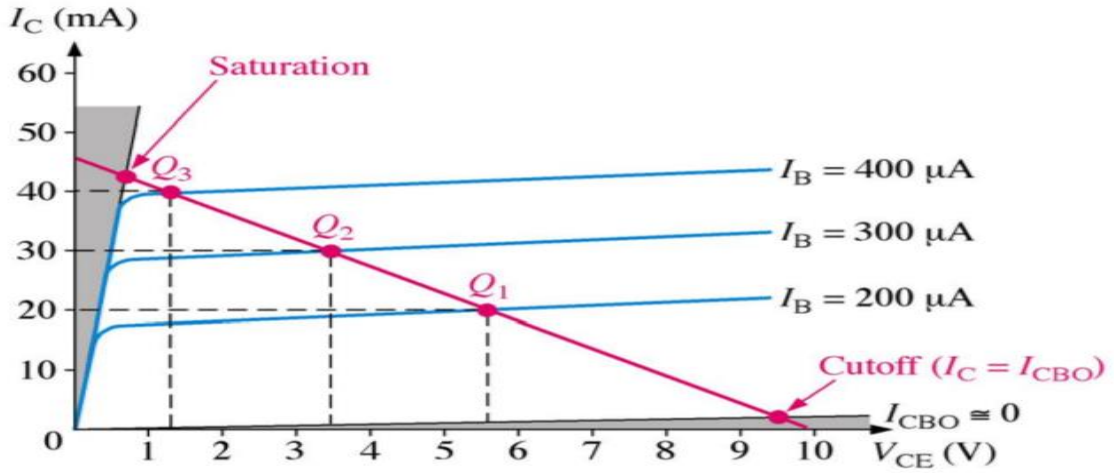
# *Figure illustrating operating point*:

## The DC Operating Point

For a transistor circuit to amplify it must be properly biased with dc voltages. The dc operating point between saturation and cutoff is called the **Q-point.** The goal is to set the Q-point such that that it does not go into saturation or cutoff when an a ac signal is applied.




(a) DC biased circuit



To find DC load line, apply KVL to the output circuit,

$-V_{cc} + I_cR_c + V_{ce} = 0$

$I_c = (V_{cc}-V_{ce})/R_c$

$I_c = (-1/R_c)V_{ce} + V_{cc}/R_c$

For AC load line, consider finite value for load resistance, $R_L$.

Then effective load resistance becomes $R_c // R_L$

# *Need for Biasing:*

- To operate the transistor in the desired region.
- The DC sources supplies the power to the transistor circuit, to get the output signal power greater than the input signal power.
- If the transistor is not biased properly, it would work inefficiently and produce distortion in output signal.

# LOAD LINE AND ITS TYPES:

## LOAD LINE:

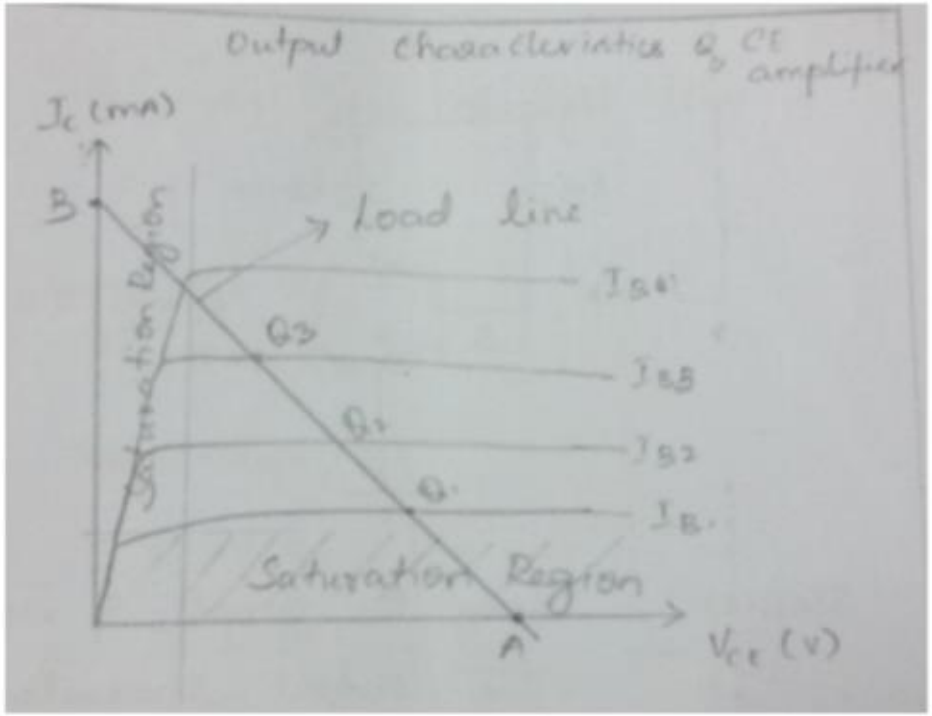
It is a straight line drawn on the characteristic curve with two end points A and B. It is used to fixed the operating point of a transistor

TYPES OF LOAD LINE:

- DC load line
- AC load line

- While drawing a load line, if only the collector resistance Rc is considered and load resistance $R_L$ is infinity , then the load line is drawn with the points [ Vcc/Rc and Vce] . It is called as Static Load Line or DC Load Line
- If the load line is drawn considering a finite load resistance $R_L$, and the resistance considered is $R_L$ in parallel with Rc, it is called AC Load Line or Dynamic Load Line, with AC Input.

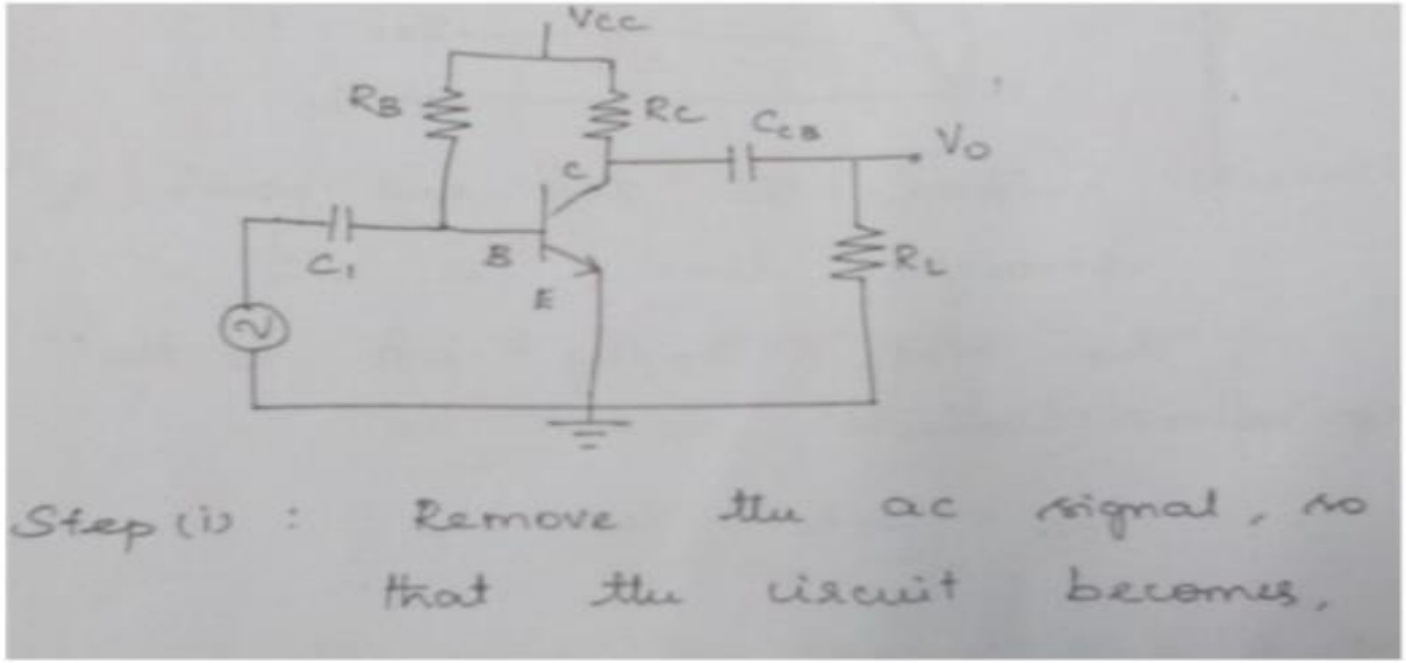
# Output characteristics of CE amplifier



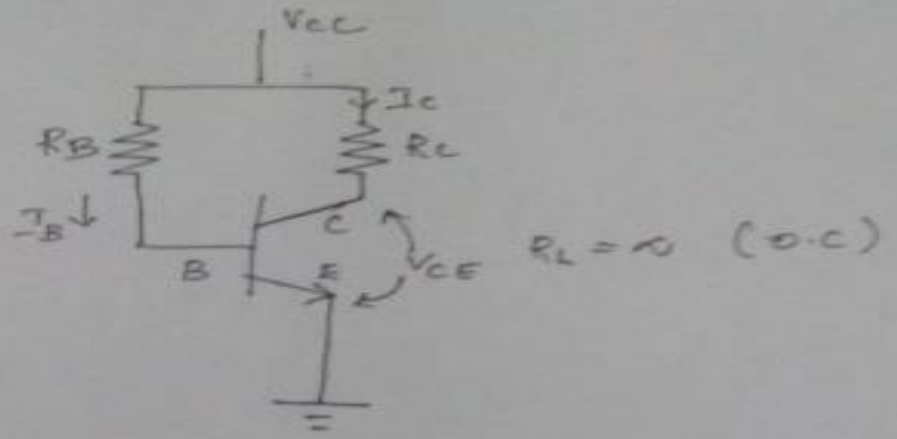
# DC LOAD LINE :

**DC LOAD LINE:**

Consider the common emitter amplifier circuit shown.

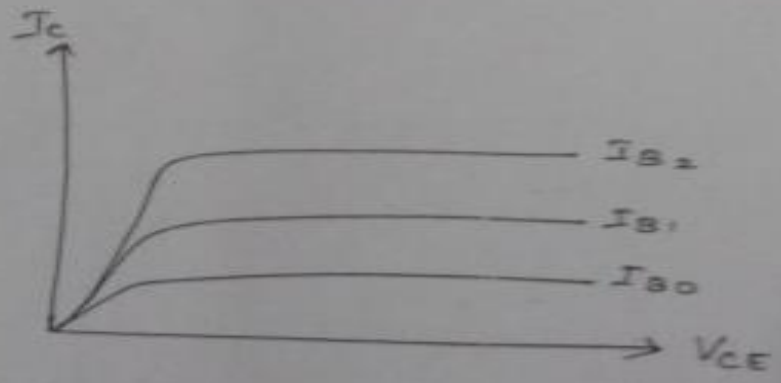



Step (i) : Remove the ac signal, so that the circuit becomes,




$R_L = 0$ (D.C)

Step:(2) : Draw the graph of $I_C$ Vs $V_{CE}$ (ie output characteristic curve)




Step:(3) : Find the two end points of the straight line.

For that, Apply KVL to the collector circuit.

$$V_{CC} = I_C R_C + V_{CE} \longrightarrow 1$$

W.k.t the equation for straight line is

$$y = mx + c$$

Here

$$y = I_C$$

$$x = V_{CE}$$

From equation (1),

$$I_C R_C = V_{CC} - V_{CE}$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \longrightarrow 2$$

**To find A:**

A is a point on X-axis

Put Y = 0 , ie $I_C = 0$ in equation 2

$$0 = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

$$V_{CE} = V_{CC} | I_{C=0mA}$$

**To find B:**

B is a point of Y – axis

Put X = 0 , ie $V_{CE} = 0$ in equation 2

$$I_C = \frac{V_{CC}}{R_C} | V_{CE=0}$$

Finally plot the points A & B on the curve.

**Step(4):**

Select the $I_B$ curve so as to find the Q – point.

**To find $I_B$:**

Apply KVL to base circuit.

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

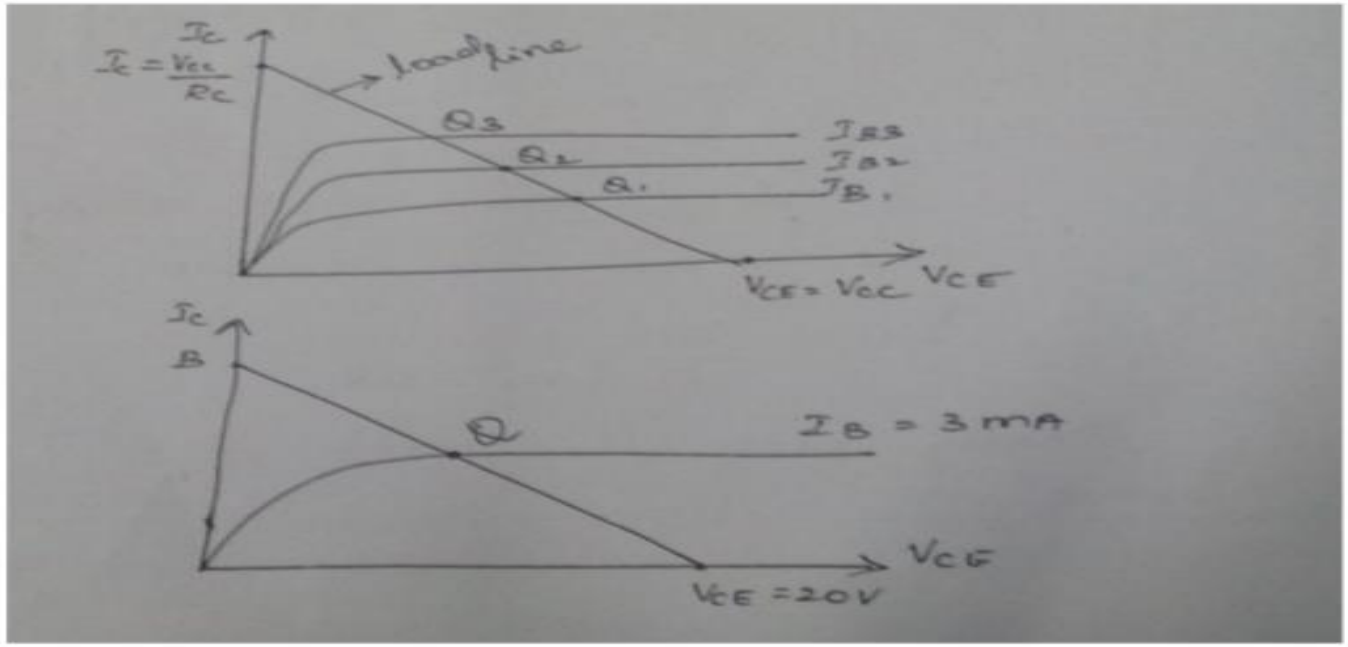
For silicon transistor $V_{BE} = 0.7V$

If $V_{CC}, R_B$ is known, the value of $I_B$ can be found.

# *EXAMPLE:*

**Example:**

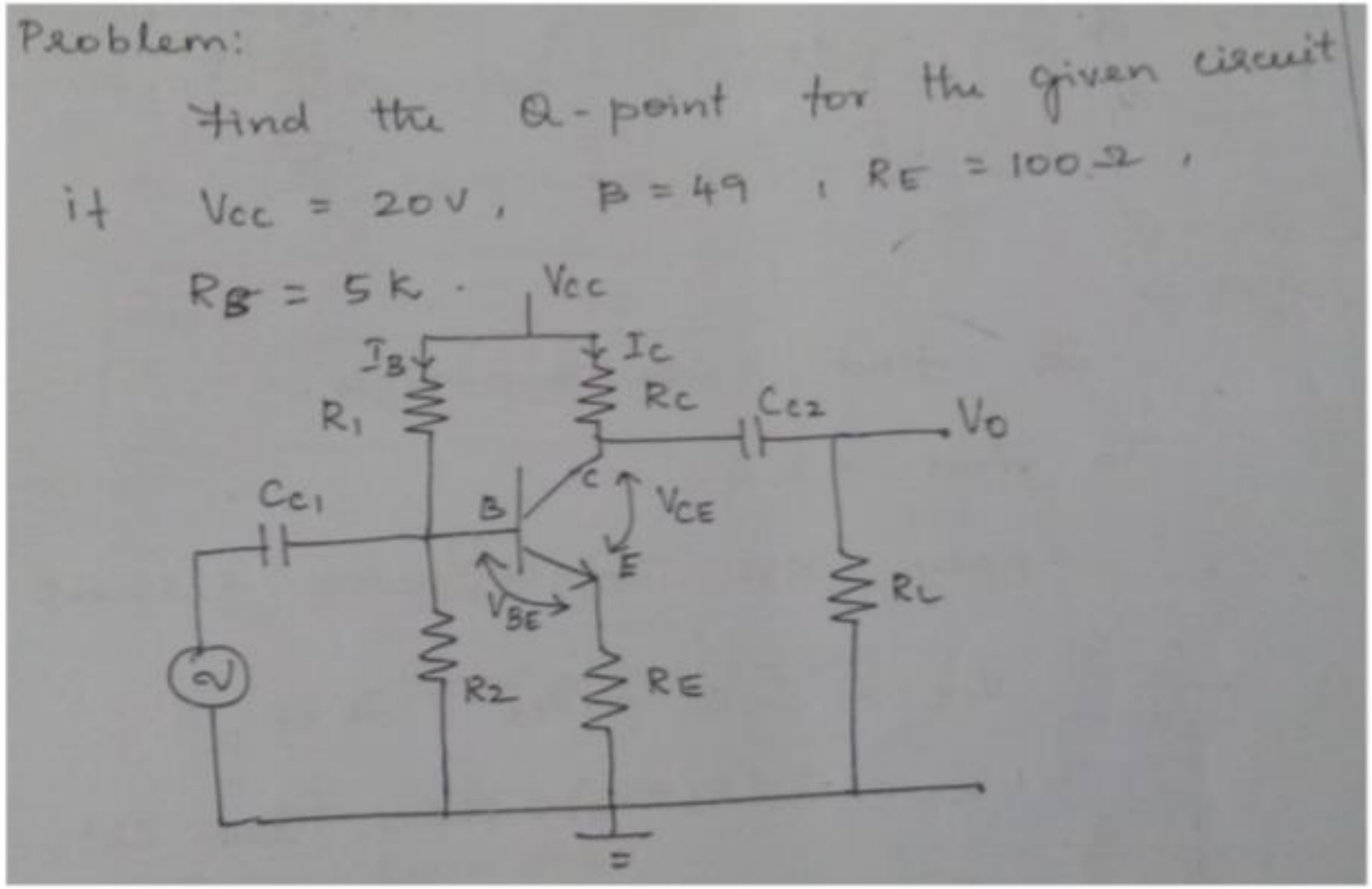
$V_{CC} = 20V, R_B = 5K, I_B = 3mA$




Conclusion:

Thus the intersection of DC load line and $I_B$ curve is called as Q – Point.

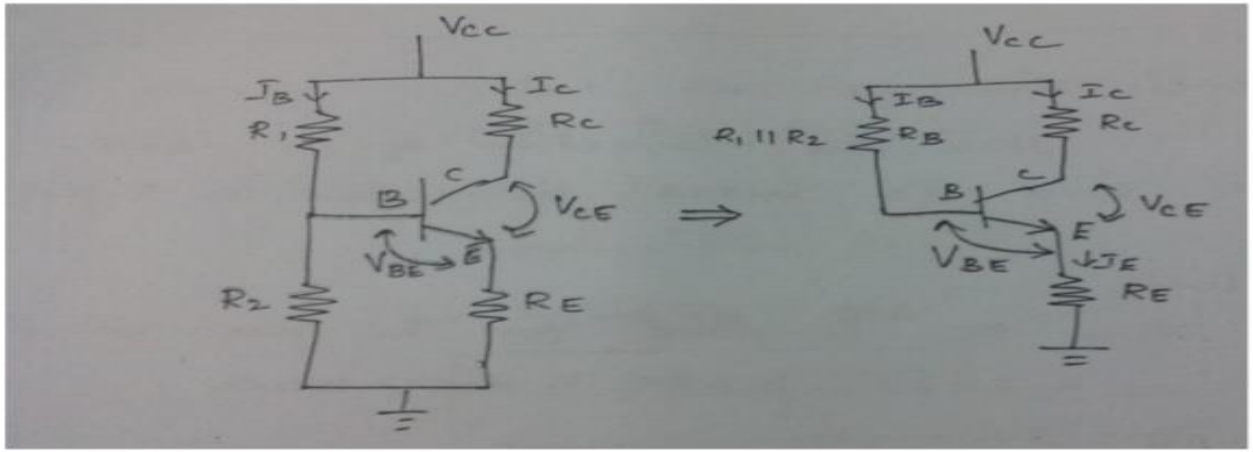
Problem:


Problem:
Find the Q-point for the given circuit
if Vcc = 20V, β = 49, RE = 100Ω,
RB = 5K.
Vcc
IB
IC
R1
RC
Cc2
Vo
C
Cc1
B
VCE
E
VBE
RL
R2
RE

Solution:

Step(i):

Remove the AC source and redraw the circuit.




Step(2):

To find A & B points:

To find A & B:

Apply KVL to collector circuit.

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

From CKT,

$$I_E = I_B + I_C$$
$$I_E = I_C$$
$$I_E \ll I_C$$

$$I_C = \frac{V_{CC}}{R_C + R_E} - \frac{V_{CE}}{R_C + R_E}$$

Since A is a point of X-axis,
$I_C = 0$

$\boxed{V_{CE} = V_{CC}|_{I_C=0}}$ (Point A)

Since B is a point of Y-axis,

$$V_{CE} = 0$$

$$I_C = \frac{V_{CC}}{R_C + R_E} \,|\, V_{CE} = 0$$ (Point B)

Step (3):

To find $I_B$ curve.

Apply KVL to base circuit.

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{CC} = I_B(R_B + (1+\beta)R_E) + V_{BE}$$

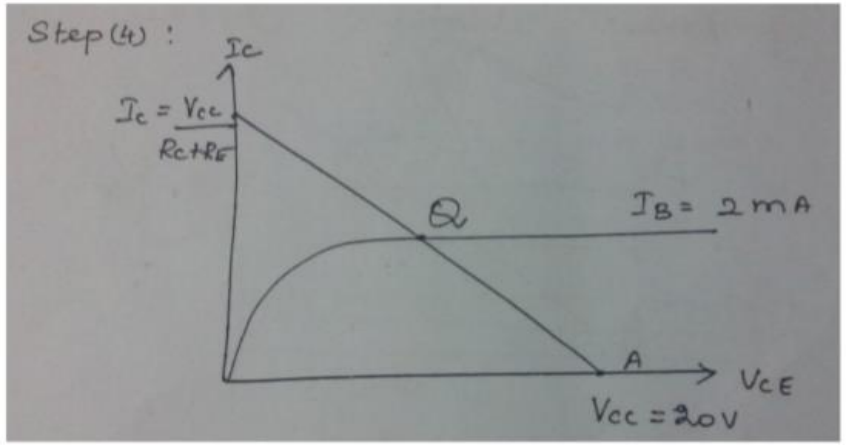
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E(1+\beta)}$$

$$I_B = \frac{20 - V_{BE}}{5 \times 10^3 + 100(1+49)}$$

$$I_B = \frac{20}{5K + 5000}$$

$$I_B = 2mA$$

Step (4):



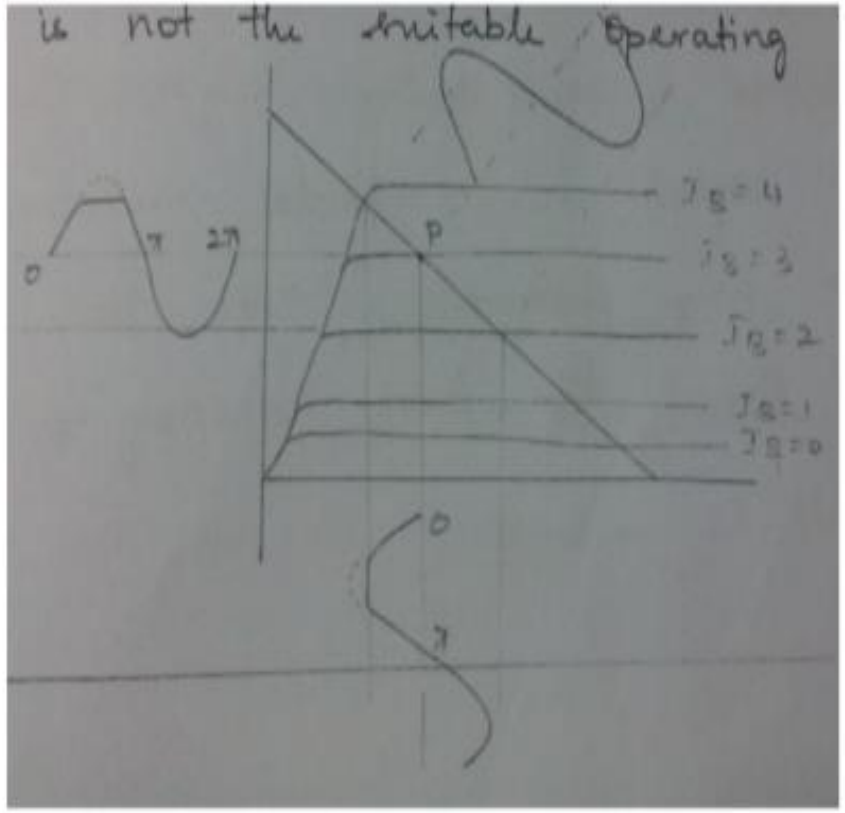
# *Selection of operating point for A C input signal:*

The operating point can be selected at three different positions on the DC load line:

- Near saturation region
- Near cut-off region
- At the centre ie. Active region

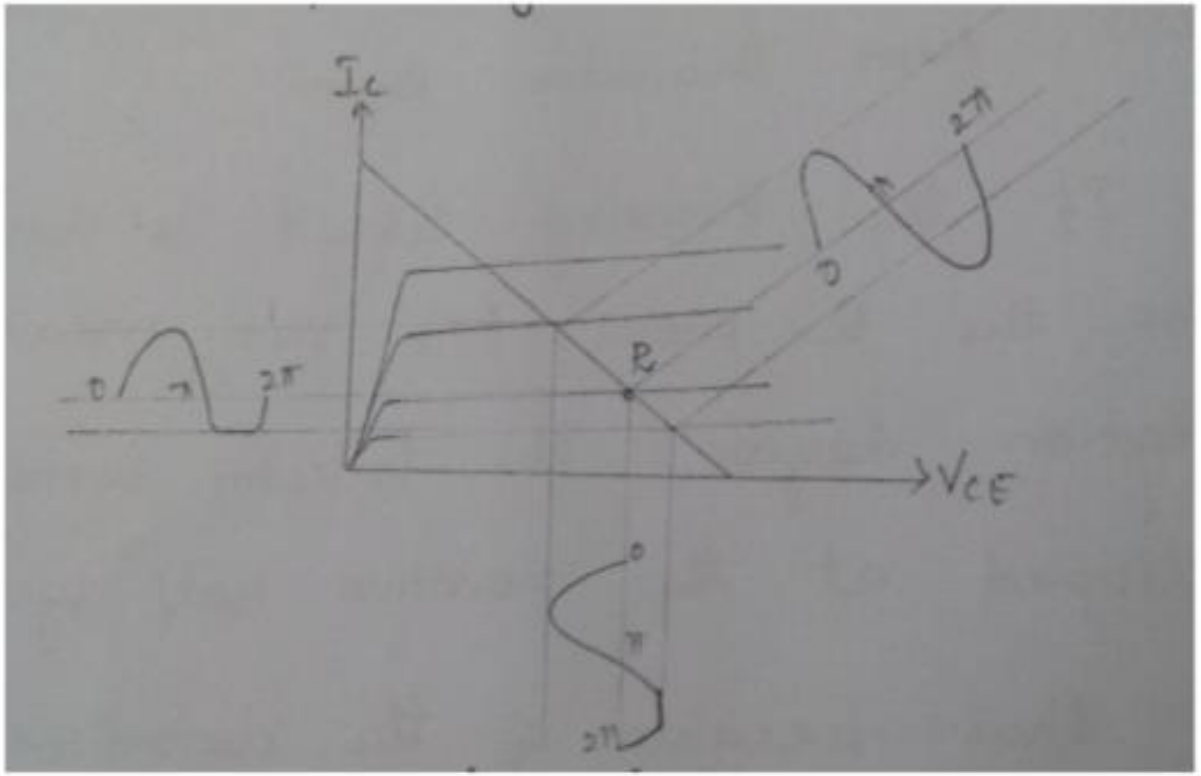
**NEAR SATURATION REGION:**

If the biasing circuit is designed to fix the Q – point (P) very near to saturation region, the collector current is clipped at the positive half cycle.
Thus because of the distortions present at the collector current, point P is not the suitable operating point.



**NEAR CUT-OFF REGION:**

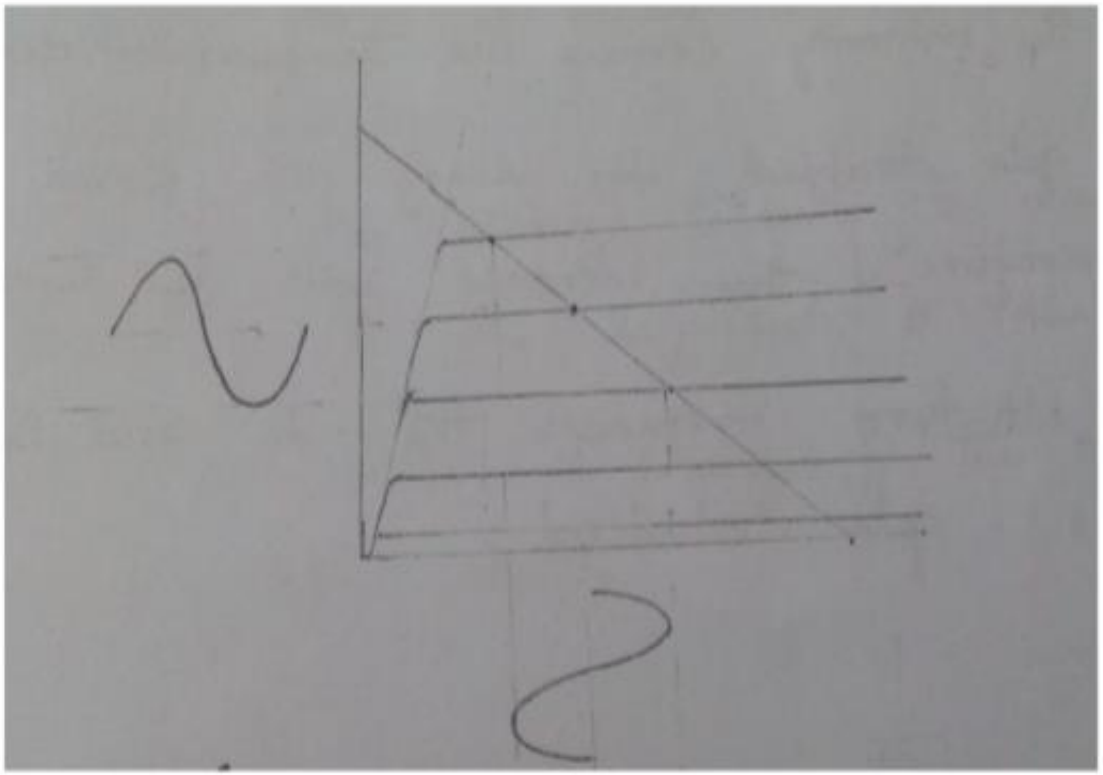
If the biasing circuit is designed to fix the Q – point (R) near cut-off region, the collector current is clipped at the negative half cycle.
Thus Q-point R is also not a suitable operating point.



Case(iii):

**AT ACTIVE REGION:**

If the Q – point is fixed at the centre of the active region, the output signal is sinusoidal waveform without any distortion. Thus the point Q is the best operating point.



# SOME QUESTIONS RELATED TO OPERATING POINT

1.The maximum peak to peak output voltage swing is obtained when Q point of a circuit is located

(a) near saturation point
(b) near cutoff point
(c) at the center of the load line
(d) at least on the load line

Solution : C

3. The ac load line of a transistor circuit is steeper than its dc line because

(a) ac signal sees less load resistance

(b) IC is higher

(c) input signal varies in magnitude

(d) none of the above

Solution : A

4. Where should be the bias point set in order to make transistor work as an amplifier?

a) Cut off
b) Active
c) Saturation
d) Cut off and Saturation

Solution : b

Explanation: To operate transistor as an amplifier, it requires more current amplification factor and in cut off and saturation, the current amplification is less, therefore active region is better to fix the Q point.

**5. It is feasible to draw DC load line of a transistor with an acquaintance of _____ points.**

a. cut-off & saturation
b. active & cut-off
c. active & saturation
d. all of the above

**ANSWER: a. cut-off & saturation**

6. The Q-point in a voltage amplifier is selected in the middle of the active region because

(a) it gives better stability

(b) the circuit needs a small power supply

(c) the biasing circuit needs less number of resistors

(d) it gives distortions less output

Solution: D

**7.Which point on the DC load line exhibit collector current and collector-emitter junction voltage in a transistor even without an application of input signal?**

a. DC operating point
b. Quiescent Point
c. Working Point
d. All of the above

**ANSWER: d. All of the above**

8. Q point can be set to work on active region requires particular conditions. What are they?
a) BE reverse biased and BC forward biased
b) BE reverse biased and BC reverse biased
c) BE forward biased and BC reverse biased
d) BE forward biased and BC forward biased

Solution : c

*Explanation:* BJT requires the forward voltage nearly equal to 0.7v and the p-junction should be more positive in BE junction and n region should be more positive in BC junction. This will make the current to flow through emitter which is the sum of current through base and emitter.

9. The negative part of the output signal in a transistor circuit starts clipping if the Q point of the circuit moves

(a) toward the saturation point

(b) toward the cutoff point

(c) toward the center of the load line

(d) none of the above

Solution: A

10. The positive part of the output signal in a transistor circuit starts clipping, if Q point of the circuit moves

(a)toward the saturation point

(b) toward the cutoff point

(c) toward the center of the load line

(d) none of the above

Solution : B

11. The Q-point of a transistor is made to shift between saturation and cut off Region, then how does the transistor behave?
a) Switch
b) Amplifier
c) Inverter
d) Bulb

*Answer: a*

Explanation: When the Q point lies in cut off, No current flows and hence it acts as a open switch. When the Q point is shifted to saturation, Current flows through the circuit creating a closed switch. Thus the current flow makes the turn on and off of switch

12. The bias point of a transistor occurs when the supply voltage exceeds the breakdown voltage of a transistor.
a) True
b) False

Answer: b

*Explanation*: Bias point can be set on the basis of DC load line that is Q point can be found out only without applying any input.

The DC load line is defined as the line drawn in response of collector current and collector to emitter voltage when no input is applied.

13.The dc load line of transistor circuit

(a) is a graph between IC and VCE

(b) is a graph between IC and IB

(c) does not contain the Q Point

(d) is a curved line

Solution : A

# BIAS STABILITY :

Bias stabilization: While designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region (i.e into cut-off or saturation region)

Factors to be considered while designing the basing circuit:

- **Ico**
- **$V_{BE}$**
- **Beta**

Factors to be considered while designing the basing circuit:

→ Temperature dependent factors ($I_{CO}, V_{BE}$)
→ $\beta | hfe$ – Transistor current gain

**$I_{CO}$:**

The flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions.

Since the minority carriers are temperature dependent ($I_{CO}$ gets doubled for energy 10°C raise in temperature), they increase with the temperature.
This in turn increase the $I_C$ and hence Q – point gets shifted

**$V_{BE}$:**

→ $V_{BE}$ changes with temperature at the rate of 2.5mv°/c
→ $I_B$ depends on $V_{BE}$

Since $\frac{I_C}{I_B} = \beta$

$I_C = \beta I_B$, increase in $I_B$

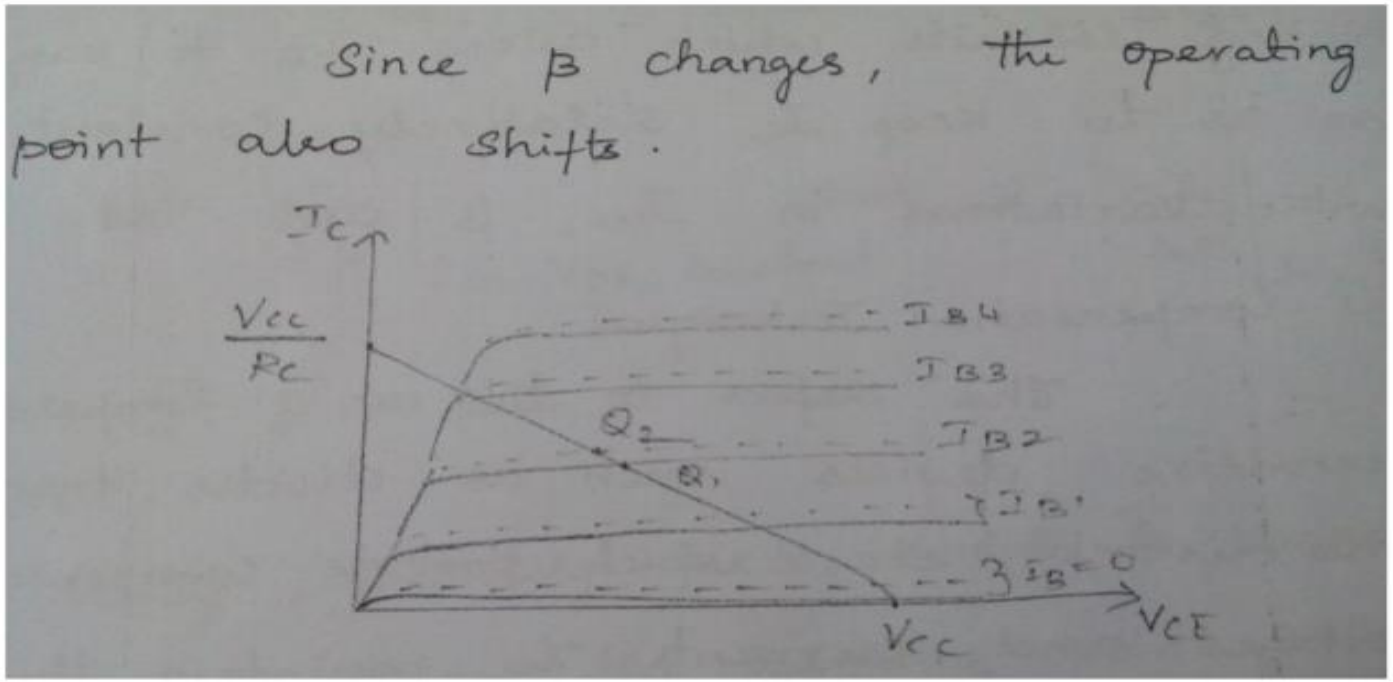
Increase $I_C$ This in turn changes the operation point.

**Transistor current gain $\beta$:**

The transistor parameters among different units of same type, same number changes. Ie. If we take two transistor units of same type (ie. Same number, construction, parameter specified etc.) and we them in the circuit, there is change in the $\beta$ value in actual practice.

The biasing circuit is designed according to the required $\beta$ value.

Since $\beta$ changes, the operating point also shifts.



# *Requirements of a biasing network*:

- The emitter-base junction must be forward biased and collector-base junction must be reversed biased. i.e. The transistors should be operated in the active region.
- The circuit design should provide a degree of temperature stability.
- The operating point should be made independent of transistor parameters (like transistor current gain)

# Techniques used to keep Q point stable:

**STABILIZATION TECHNIQUE:**

This refers to the use of resistive biasing circuits which allow $I_B$ to vary so as to keep $I_C$ Relatively constant with variations in $I_{CO}$ and $V_{BE}$ current gain(beta)

***COMPENSATION TECHNIQUE:***

This refers to the use of temperature sensitive devices such as diodes, transistors, thermistors, etc, which provide compensating voltages and current to maintain the operating point stable.

# Stability Factors :

**STABILITY FACTORS:**

- → The stability factor is a measure of stability provided by the biasing circuit.
- → Stability factor indicates the degree of change in operating point due to variation in temperature.
- → Since there are 3 temperature dependent variables, there are 3 stability factors.

$$S = \frac{\partial I_C}{\partial I_{CO}} |V_{BE,\beta\ constant} \quad \text{(or)} \quad S = \frac{\Delta I_C}{\Delta I_{CO}} |V_{BE,\beta\ constant}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} |I_{CO,\beta\ constant} \quad \text{(or)} \quad S' = \frac{\Delta I_C}{\Delta V_{BE}} |I_{CO,\beta\ constant}$$

$$S'' = \frac{\partial I_C}{\partial \beta} |V_{BE,I_{CO}\ constant} \quad \text{(or)} \quad S'' = \frac{\Delta I_C}{\Delta \beta} |V_{BE,I_{CO}\ constant}$$

**Note:**

- → Ideally, stability factor should be perfectly zero to keep the operating point stable.
- → Practically stability factor should have the value as minimum as possible.

**EXPRESSION FOR STABILITY FACTOR S:**

For a common emitter configuration collector current is given by

$$I_C = I_{C(majority)} + I_{CEO\,(majority)}$$

WKT

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

$$I_{CEO} = (1 + \beta)\, I_{CBO}$$

$$I_C = \beta I_B + (1 + \beta)\, I_{CBO}$$

When
$I_{CBO}$ changes by $\Delta I_{CBO}$
$I_B$ changes by $\Delta I_B$
$I_C$ changes by $\Delta I_C$

$$\partial I_C = \beta \partial I_B + (1 + \beta) \partial\, I_{CBO}$$

$\div$ by $\partial I_C$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial\, I_{CBO}}{\partial I_C}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} = (1 + \beta) \frac{\partial\, I_{CBO}}{\partial I_C}$$

$$\frac{\partial\, I_{CBO}}{\partial I_C} = \frac{(1 - \beta) \frac{\partial I_B}{\partial I_C}}{(1 + \beta)}$$

If $S = \frac{\partial I_C}{\partial I_{CBO}}$

$$\frac{1}{S} = \frac{(1 - \beta) \frac{\partial I_B}{\partial I_C}}{(1 + \beta)}$$

$$S = \frac{(1 + \beta)}{(1 - \beta) \frac{\partial I_B}{\partial I_C}}$$

14. There are two transistors A and B having ‘S’ as 25 and 250 respectively, on comparing the value of S, we can say B is more stable than A.

a) True

b) False

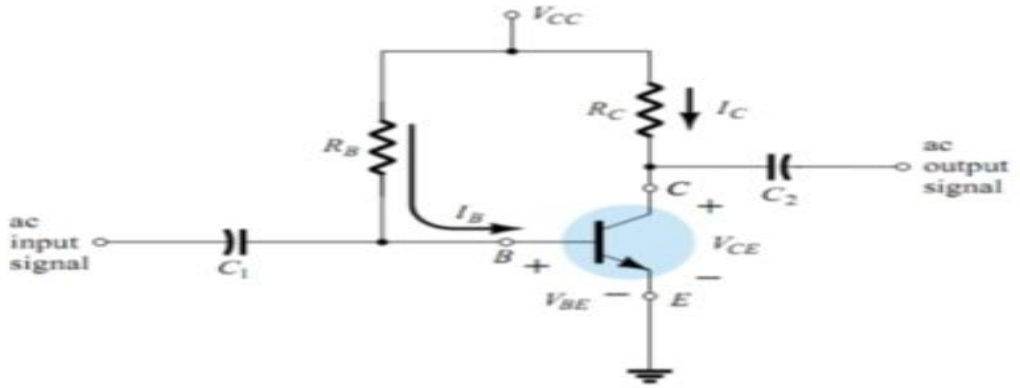
Answer: b

*Explanation:* More the value of S, lesser the stability, since A has lesser S value the change in beta does not affect much on the collector current. When S is high, even if $I_B$ changes by a small value, the $I_C$ current will drastically vary. Hence stability factor must possess lesser value for the proper working of a transistor.

# *Types of **B**iasing Circuits:*

- ***Fixed bias circuit with and without emitter resistor***
- ***Collector to base bias circuit***
- ***Voltage divider or self bias circuit***

# *Fixed bias circuit* :




**To find $I_B$:**

Apply KVL to the base circuit,

$V_{CC} = I_B R_B + V_{BE}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \longrightarrow 1$$

$$I_B = \frac{V_{CC}}{R_B}$$

$V_{BE} \ll V_{CC}$

$V_{BE} = 0.7 for\ si$

$V_{CC}$ →fixed, $R_B$ → fixed and hence $I_B$ is fixed and the circuit is called as fixed bias circuit.

**To find $V_{CE}$:**

Apply KVL to the Collector circuit,

$V_{CC} = I_C R_C + V_{CE}$

$$V_{CE} = V_{CC} + I_C R_C \longrightarrow 2$$

**To find $I_C$:**

From equation (2),

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \longrightarrow 3$$

**To find $S$:**

WKT

$$S = \frac{(1+\beta)}{(1-\beta)\frac{\partial I_B}{\partial I_C}}$$

$$\frac{\partial I_B}{\partial I_C} = 0$$

$$S = \frac{(1+\beta)}{(1-\beta)0}$$

$$S = (1+\beta) \longrightarrow 4$$

**To find $S'$:**

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

WKT,

$$I_C = I_{C(majority)} + I_{CEO\,(majority)}$$

$$I_C = \beta I_B + I_{CBO}$$

$$I_C = \beta I_B + (1+\beta)\, I_{CBO}$$

Sub $I_B$ in above equation,

$$I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (1+\beta) I_{CBO}$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CBO}$$

Diff. $I_C$ WRT to $V_{BE}$

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B}$$

$$S' = \frac{-\beta}{R_B} \longrightarrow 5$$

**To find S'':**

$$S'' = \frac{\partial I_C}{\partial \beta}$$

$$I_C = \beta I_B + (1+\beta)\, I_{CBO}$$

$$I_C = \beta I_B + I_{CBO} + \beta I_{CBO}$$

Diff $I_C$ WRT to $\beta$

$$\frac{\partial I_C}{\partial \beta} = I_B + I_{CBO}$$

$$S'' = I_B + I_{CBO}$$

$$\boxed{S'' \cong I_B}$$

$$S'' = I_B = \frac{I_C}{\beta} \longrightarrow 6$$

To find relation between s and S'

$$S = (1+\beta)$$

$$S' = \frac{-\beta}{R_B}$$

To obtain S' in terms of S
Multiply and divided by $(1+\beta), S'$

$$S' = \frac{-\beta}{R_B} \times \frac{(1+\beta)}{(1+\beta)}$$

$$S' = \frac{-\beta S}{R_B(1+\beta)} \longrightarrow 7$$

To find relation between S and S''
We have

$$S'' = \frac{I_C}{\beta}$$

$$S' = \frac{-\beta}{R_B}$$

Multiply and divided by $(1+\beta), S''$

$$S'' = \frac{I_C}{\beta} \times \frac{(1+\beta)}{(1+\beta)}$$

$$S'' = \frac{I_C S}{\beta(1+\beta)} \longrightarrow 8$$

# ADVANTAGES OF FIXED BIAS CIRCUIT:

- **It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (RB).**
- **A very small number of components are required.**

# DISADVANTAGES OF FIXED BIAS CIRCUIT:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

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# Demerits :

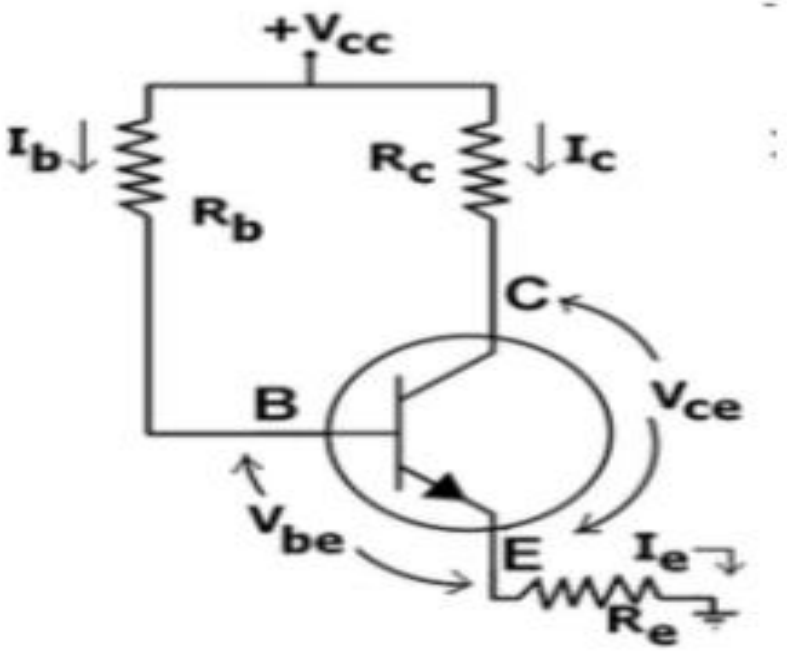
- In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately $\beta+1$.
- For small-signal transistors (e.g., not power transistors) with relatively high values of $\beta$ (i.e., between 100 and 200), this configuration will be prone to thermal runaway.
- To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

# Usage :

- Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source).
- Instead, it is often used in circuits  where transistor is used as a switch.
- However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage

# Fixed bias with emitter resistor

The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point.



# MERITS AND DEMERITS:

*Merits :*

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits :

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE very large, or making RB very low.
- If RE is of large value, high VCC is necessary. This increases cost as well as necessary precautions while handling.

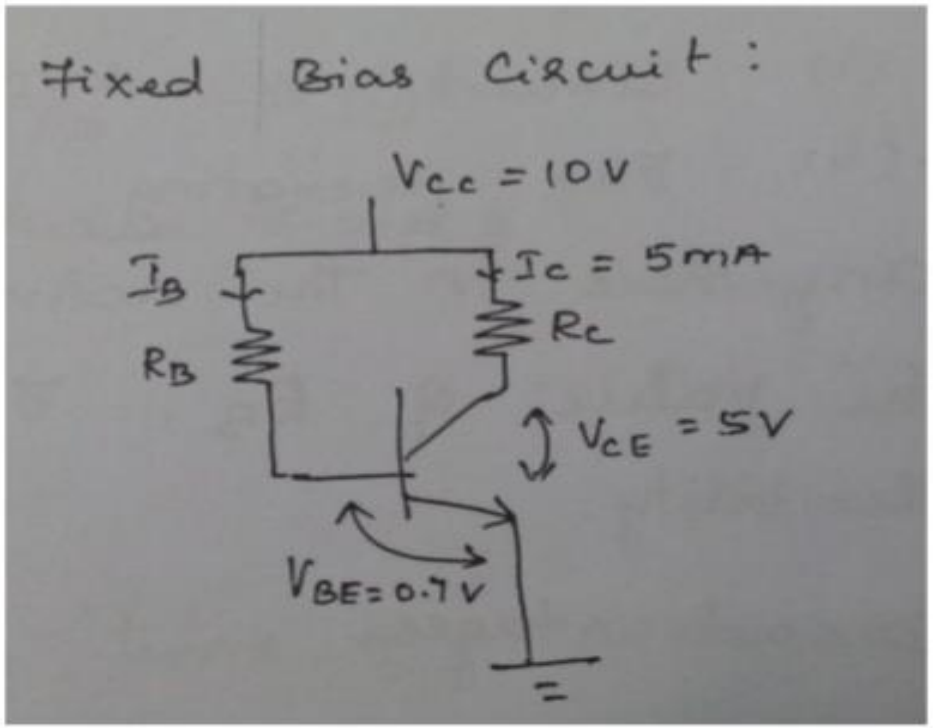
- If RB is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical
- In addition to the above, RE causes ac feedback which reduces the voltage gain of the amplifier.

# Usage :

- The feedback also increases the input impedance of the amplifier when seen from the base, which can be advantageous.
- This type of biasing circuit is used only with careful consideration of the trade-offs involved.

**Problem**

Design a fixed bias circuit using a silicon transistor having $\beta$ value of 100, $V_{CC} = 10V$ and DC bias condition are to be $V_{CE} = 5V$ and $I_C = 5mA$




**Solution:**
**Given:**
$\beta = 100$
$V_{CC} = 10V$
$V_{CE} = 5V$
$I_C = 5mA$

**To find:**
$R_B = ?$
$R_C = ?$
$I_B = ?$

**To find $R_C$:**

Applying KVL to collector circuit,

$$V_{CC} = I_C R_C + V_{CE}$$

$$10 = 5 \times 10^{-3} R_C + 5$$

$$\frac{5}{5 \times 10^{-3}} = R_C$$

$$\boxed{R_C = 1\ K\Omega}$$

**To find $I_B$:**

WKT $\frac{I_C}{I_B} = \beta$

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{5m}{100}$$

$$\boxed{I_B = 50\mu A}$$

**To find $R_B$:**

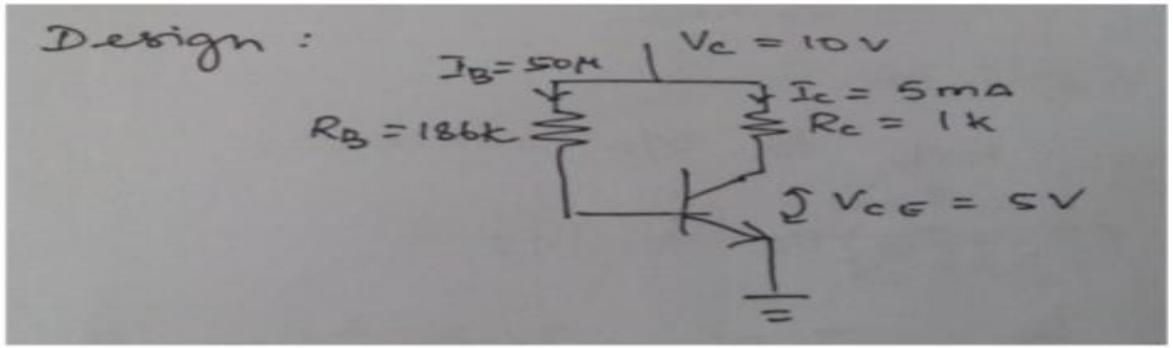
Applying KVL to input circuit,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\frac{10 - 0.7}{50\mu} = R_B$$

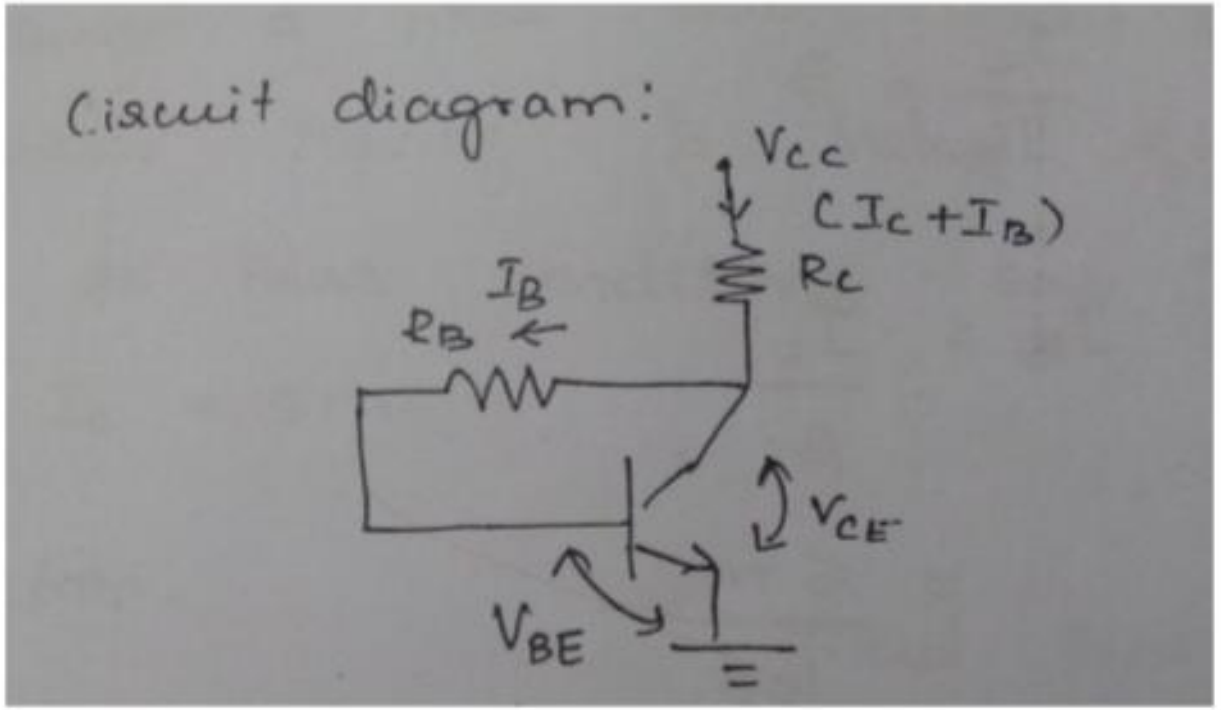
$$\boxed{R_B = 1861\ K\Omega}$$

**Design:**



# Collector to base bias circuit:

**COLLECTOR TO BASE BIAS CIRCUIT:**



Since the $R_B$ resistor is connected between the collector and base, it is called as collector to base bias circuit.

To find $I_B$:

Applying KVL to input circuit,

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_C R_C + I_B(R_C + R_B) + V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{CE}}{R_C + R_B} \longrightarrow 1$$

To find $V_{CE}$:

Applying KVL to output circuit,

$$V_{CC} = (I_C + I_B)R_C + V_{CE}$$

$$V_{CC} = V_{CC} - I_C R_C - I_B R_C \longrightarrow 2$$

To find $I_C$:

Applying KVL to collector circuit,

$$V_{CC} = (I_C + I_B)R_C + V_{CE}$$

$$V_{CC} = I_C R_C + I_B R_C + V_{CE}$$

$$I_B = \frac{V_{CC} - V_{CE} - I_B R_C}{R_C} \longrightarrow 3$$

WKT the basic equation for $I_C$ is

$$I_C = \beta I_B + I_{CBO}$$
$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$\boxed{I_C \cong \beta I_B}$$

To find S:

$$S = \frac{(1+\beta)}{(1-\beta)\frac{\partial I_B}{\partial I_C}}$$

$\frac{\partial I_B}{\partial I_C}$ is obtained by diff. $I_B$ WRT $I_S$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B} \longrightarrow 4$$

$$S = \frac{(1+\beta)}{(1-\beta)\frac{-R_C}{R_C + R_B}}$$

$$= \frac{(1+\beta)}{(1+\beta)\frac{R_C}{R_C + R_B}} \longrightarrow 5$$

$$S = \frac{(1+\beta)(R_C + R_B)}{R_C + R_B + \beta R_C}$$

$$\boxed{S = \frac{(1+\beta)(R_C + R_B)}{R_B + (\beta+1)R_C}}$$

**To find S′:**

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

$$I_B = \frac{V_{CC} - V_{CE} - I_B R_C}{R_C}$$

As there is no $V_{BE}$ term in the above equation

WKT,

$$I_C = \beta I_B$$

Sub $I_B$ in above equation,

$$I_C = \beta \left( \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \right)$$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_C + R_B} - \frac{\beta I_C R_C}{R_C + R_B}$$

$$I_C + \frac{\beta I_C R_C}{R_C + R_B} = \frac{\beta (V_{CC} - V_{BE})}{R_C + R_B}$$

$$I_C R_B + I_C R_C + \beta I_C R_C = \beta (V_{CC} - V_{BE})$$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_C + R_B + \beta R_C} \longrightarrow 5.1$$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1+\beta) R_C} \longrightarrow 6$$

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B}$$

$$S' = \frac{-\beta}{R_B + (1+\beta) R_C} \longrightarrow 7$$

**To find $S''$:**

$$S'' = \frac{\partial I_C}{\partial \beta}$$

From equation (6),

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_C + R_B + \beta R_C}$$

$$S'' = \frac{\partial I_C}{\partial \beta}$$

$$= \frac{(R_C + R_B + \beta R_C)(V_{CC} - V_{BE}) - \beta (V_{CC} - V_{BE})(R_C)}{(R_C + R_B + \beta R_C)^2}$$

$$S'' = \frac{(V_{CC} - V_{BE})(R_C + R_B)}{(R_B + (1+\beta) R_C)^2} \longrightarrow 8$$

To find relation between s and $S'$

$$S' = \frac{-\beta}{R_B + (1 + \beta) R_C}$$

Multiply and divided by $(1 + \beta)$ , $R_C + R_B$

$$S' = \frac{-\beta}{R_B+(1+\beta)R_C} \times \frac{(1+\beta)R_C+R_B}{(1+\beta)R_C+R_B} \longrightarrow 8.1$$

From equation (5),

$$S = \frac{(1+\beta)}{(1-\beta)\frac{-R_C}{R_C+R_B}}$$

$$= \frac{(1+\beta)}{(1+\beta)\frac{R_C}{R_C+R_B}}$$

$$S = \frac{(1+\beta)(R_C+R_B)}{R_C+R_B+\beta R_C}$$

$$S = \frac{(1+\beta)(R_C+R_B)}{R_B+(\beta+1)R_C} \longrightarrow 9$$

By combining equation (9) & (8.1),

$$S' = \frac{-\beta S}{(1+\beta)R_C+R_B} \longrightarrow 10$$

To find relation between S and S''

We have

$$S'' = \frac{(V_{CC}-V_{BE})(R_C+R_B)}{(R_B+(1+\beta)R_C)^2}$$

Multiply and divided by $(1+\beta)$ we have

$$S'' = \frac{(V_{CC}-V_{BE})(R_C+R_B)}{(R_B+(1+\beta)R_C)^2} \times \frac{(1+\beta)}{(1+\beta)}$$

$$S'' = \frac{(V_{CC}-V_{BE})S}{(1+\beta)(R_B+(1+\beta)R_C)}$$

$$S'' = \frac{I_C S}{\beta(1+\beta)} \longrightarrow 11$$

# *Merits and demerits :*

## Merits :

Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

## Demerits:

- As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping Rc fairly large or making Rb very low.
- If Rc is large, a high Vcc is necessary, which increases cost as well as precautions necessary while handling.

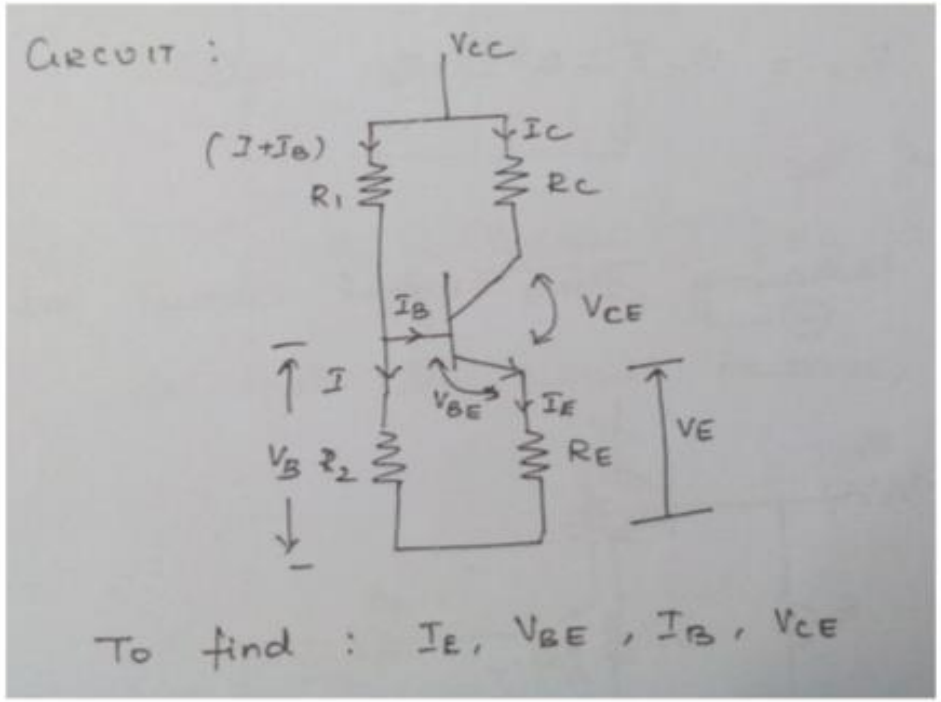
- If Rb is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor Rb causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability

# Usage :

- The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous.
- Due to the gain reduction from feedback,  this biasing form is used only when the trade-off for stability is warranted

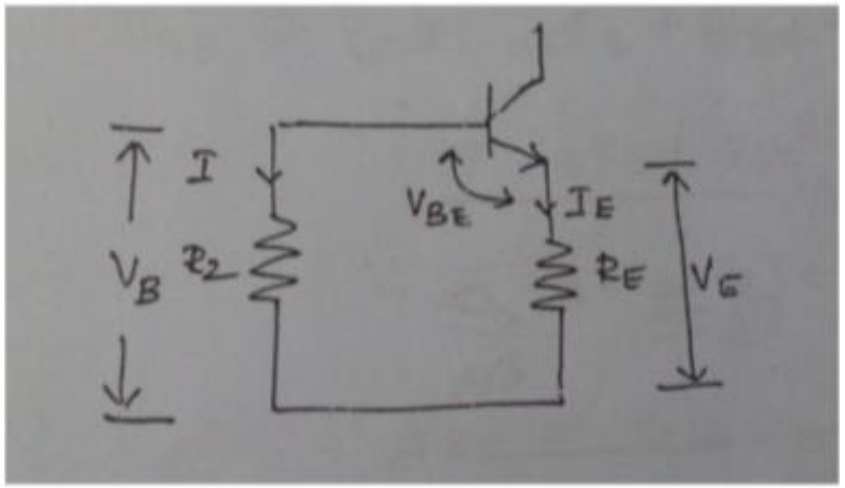
# Voltage divider bias circuit :

**VOLTAGE- DIVIDER BIAS CIRCUIT:**
**[OR]**
**SELF – BIAS (OR) EMITTER BIAS CIRCUIT.**



**To find $I_E$:**

Consider the closed loop shown in the circuit.




$$V_B = V_{BE} + V_E$$

$$V_B = V_{BE} + I_E R_E$$

$$I_E = \frac{V_B - V_{BE}}{R_E} \longrightarrow 1$$

**To find $V_{CE}$:**

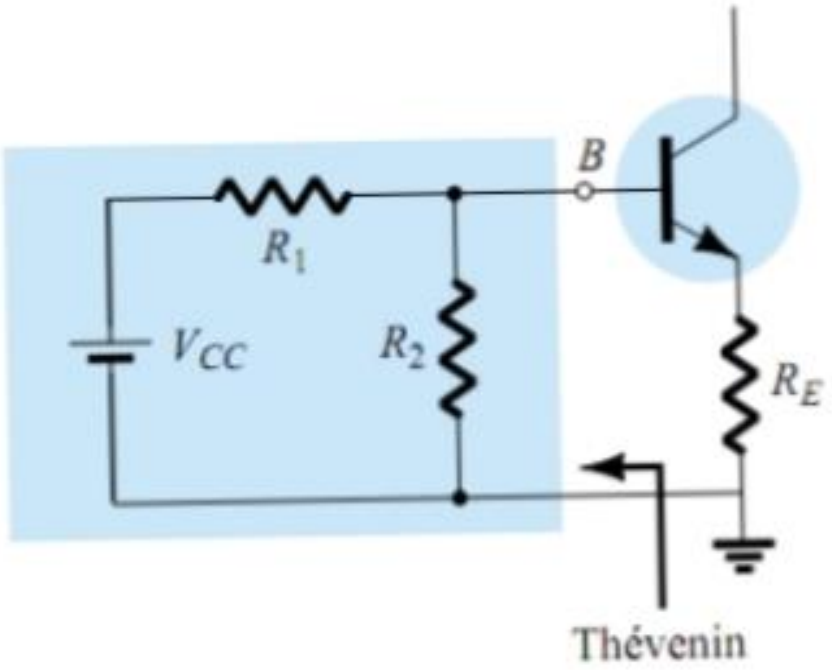
Applying KVL to the collector circuit.

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \longrightarrow 2$$

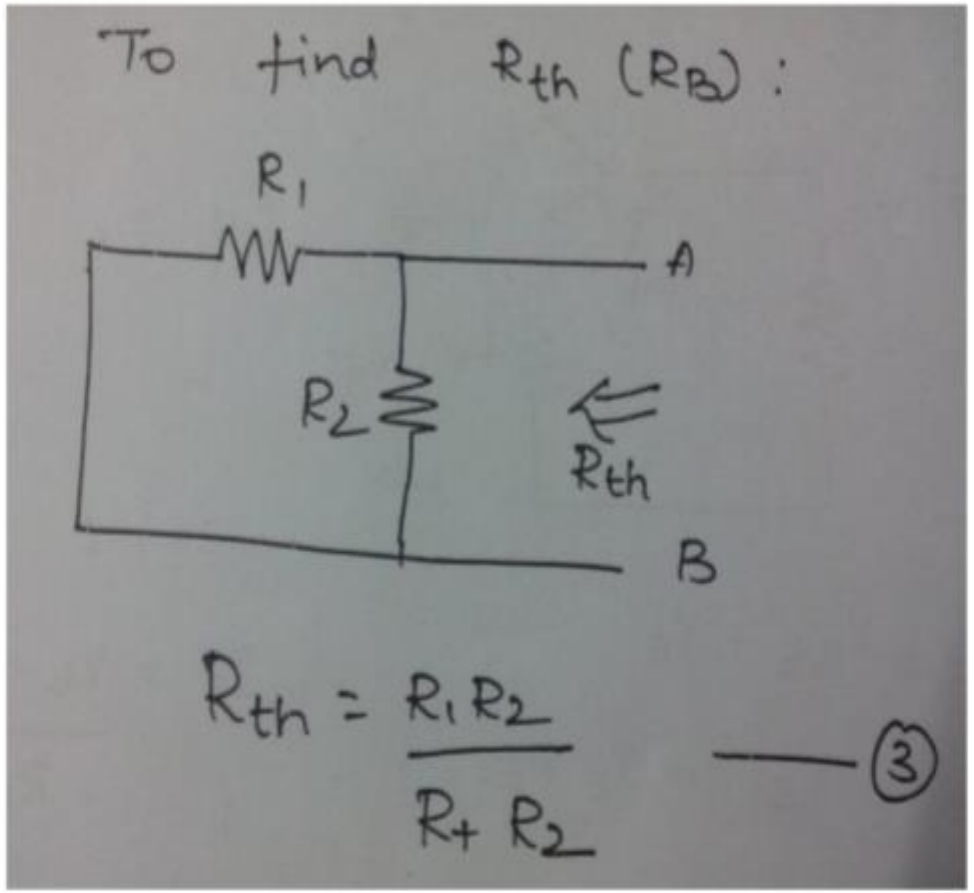
**To find $V_{BE}$:**

Redrawing the original circuit as follow,

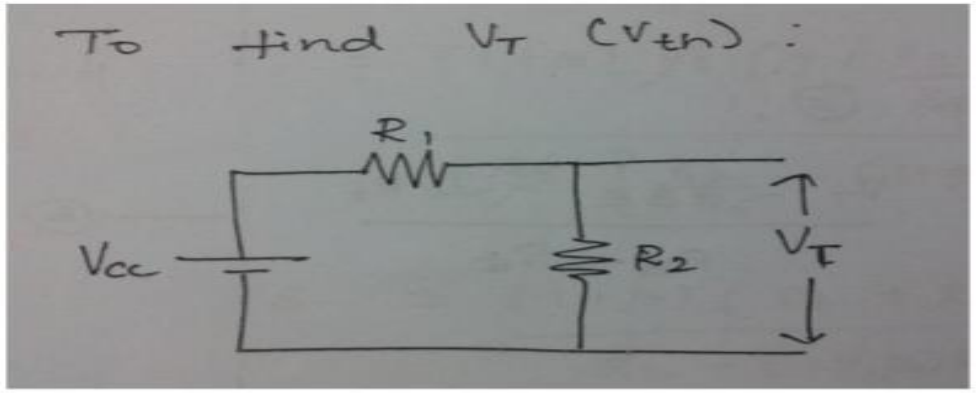


To find thevenin's equivalent circuit:-

To find $R_{th}(R_b)$:



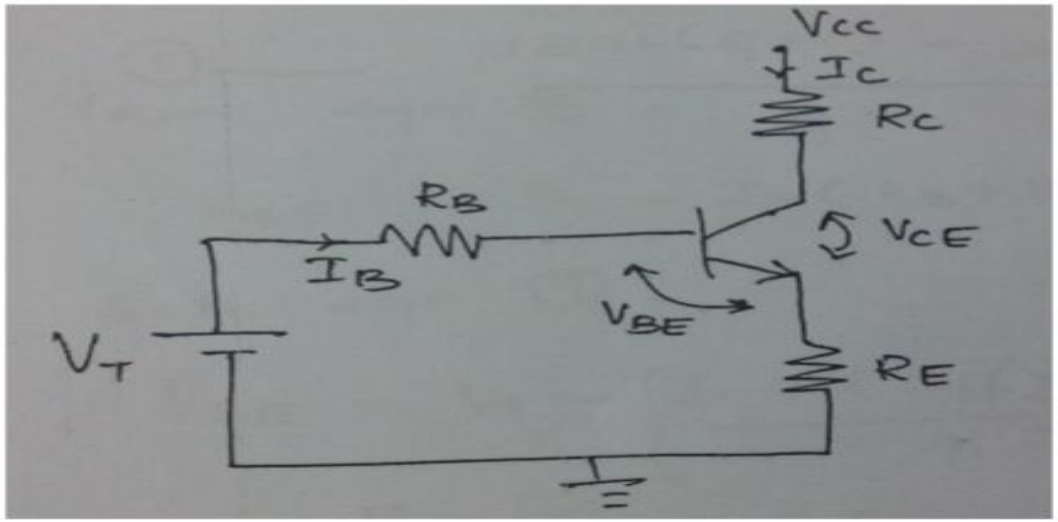
To find $V_T(V_{th})$:




$$V_T = \frac{V_{CC}R_2}{R_1+R_2} \longrightarrow 4$$

By voltage divided rule.

So that the circuit becomes,




Thus,

$$V_{BC} \rightarrow V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$I_E = I_B + I_C$$

$$V_T = I_B(R_B + R_E) + V_{BE} + I_C R_E$$

$$V_{BE} = V_T - I_B(R_B + R_E) + I_C R_E \longrightarrow 5$$

To find $I_B$:

From equation (5)

$$I_B = \frac{V_T - V_{BE} - I_C R_E}{R_B + R_E} \longrightarrow 6$$

To find $S$:

$$I_C = \beta I_B + (1 + \beta)\, I_{CBO}$$

$$I_B = \frac{I_C - (1+\beta)\, I_{CBO}}{\beta} \longrightarrow 7$$

WKT

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{(1 + \beta)}{(1 - \beta)\frac{-R_E}{R_B + R_E}}$$

$$= \frac{(1 + \beta)}{(1 - \beta)\frac{-R_E}{R_B + R_E}}$$

$$S = \frac{(1 + \beta)(R_B + R_E)}{R_B + R_E + \beta R_E}$$

$$S = \frac{(1+\beta)(R_B + R_E)}{R_B + (\beta+1)R_E} \longrightarrow 8$$

To find $S'$:

$$\frac{\partial I_C}{\partial V_{BE}}$$

From equation (7),

$$V_{BE} = V_T + I_B(R_B + R_E) - I_C R_E$$

Sub equation (7),

$$V_{BE} = V_T + \frac{I_C - (1+\beta)\, I_{CBO}}{\beta}(R_B + R_E) - I_C R_E$$

$$V_{BE} = V_T + \frac{I_C}{\beta}(R_B + R_E) + \frac{(1+\beta)\, I_{CBO}}{\beta}(R_B + R_E) - I_C R_E$$

$$V_{BE} = V_T + \frac{I_C}{\beta}(R_B + R_E) + \frac{(1+\beta)\, I_{CBO}(R_B + R_E)}{\beta} - \frac{I_C R_E \beta}{\beta}$$

$$V_{BE} = V_T + \frac{I_C(R_B + R_E(1+\beta))}{\beta} + \frac{(1+\beta)\, I_{CBO}(R_B + R_E)}{\beta}$$

Let

$$\mathrm{V}' = \frac{(1+\beta)\, I_{CBO}(R_B + R_E)}{\beta}$$

$$V_{BE} = V_T + \frac{I_C(R_B + R_E(1+\beta))}{\beta} + \mathrm{V}'$$

$$\frac{I_C(R_B + R_E(1+\beta))}{\beta} = V_T - V_{BE} + \mathrm{V}'$$

$$I_C = \frac{\beta[V_T - V_{BE} + \mathrm{V}']}{R_B + (\beta+1)R_E} \longrightarrow 9$$

$$\mathrm{s}S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (\beta+1)R_E} \longrightarrow 10$$

To find $S''$:

$$S'' = \frac{\partial I_C}{\partial \beta}$$

Differentiating equation (9), WRT $\beta$

$$S'' = \frac{R_B + R_E(1+\beta)[V_T - V_{BE} + V'] - \beta[V_T - V_{BE} + V']R_E}{[R_B + R_E(1+\beta)]^2}$$

$$S'' = \frac{(R_B + R_E)[V_T - V_{BE} + V']}{[R_B + R_E(1+\beta)]^2}$$

Now multiply and divide by $(1+\beta)$

$$S'' = \frac{(R_B + R_E)[V_T - V_{BE} + V']}{[R_B + R_E(1+\beta)]^2} \times \frac{(1+\beta)}{(1+\beta)}$$

$$S'' = \frac{S[V_T - V_{BE} + V']}{(1+\beta)R_B + R_E(1+\beta)}$$

$$S'' = \frac{I_C S}{\beta(1+\beta)} \text{ by equation (9)} \longrightarrow 11$$

# *Merits and demerits :*

## *Merits* :

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

### ***Demerits:***

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE fairly large

- If RE is of large value, high VCC is necessary .

This increases cost as well as precautions necessary while handling.

Usage : widely used in linear circuits .