

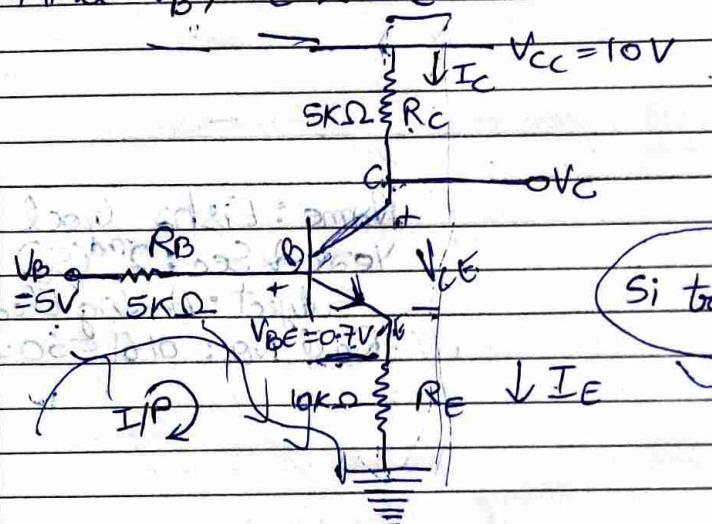
16.7.19

### Unit-I

Reference Book  
 → S. Salivahan  
 → J.B. Gupta

\* Review of BJT:

Q1. Find  $V_B$ ,  $V_C$  &  $I_C$



For input side:

$$\begin{aligned} V_B - V_{BE} &= I_B R_B + I_E R_E \quad (\text{Kirchhoff's law}) \\ &= I_B R_B + (I_B + I_C) R_E \quad (\because I_C = I_E + I_B) \\ &= I_B R_B + I_B (1 + \beta) R_E \quad (\because \beta = \frac{I_C}{I_B}) \end{aligned}$$

$$\Rightarrow V_B - 0.7V = I_B (R_B + 51 R_E)$$

$$5 - 0.7 = I_B (5 + 51 \times 10) \quad (V_B = 5V)$$

$$I_B = \frac{5 - 0.7}{515}$$

$$[I_B = 0.0083mA]$$

$$\text{As, } \beta I_B = \frac{V_{CC} - V_C}{R_C}$$

$$\Rightarrow 50 \times 0.0083 = \frac{10 - V_C}{5}$$

$$10 - V_C = 250 \times 0.0083$$

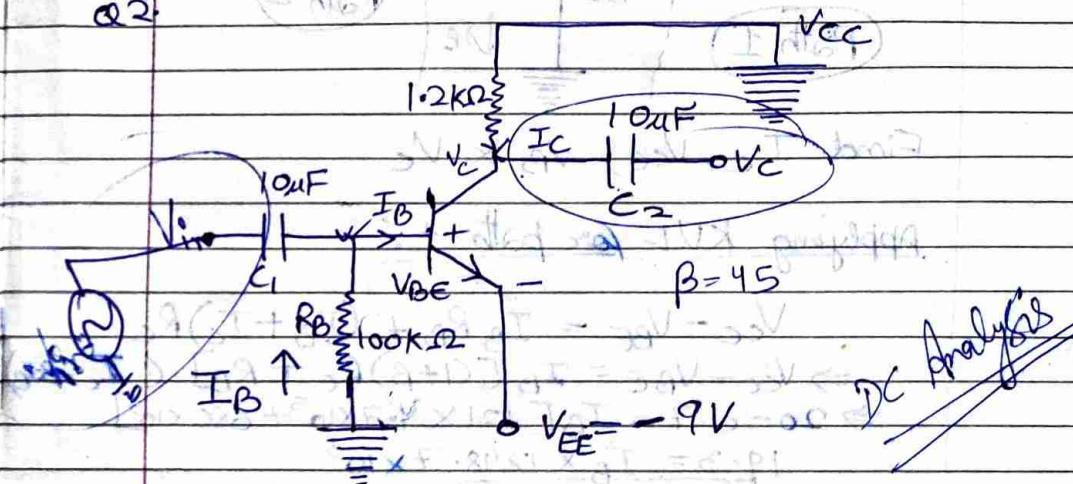
$$V_C = 10 - 2.075$$

$$V_C = 7.925V$$

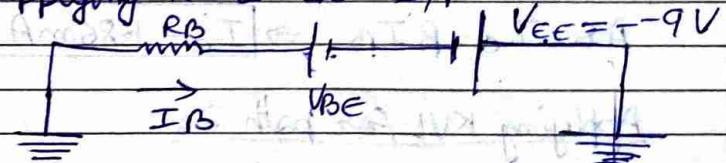
$$I_C = \frac{V_{CC} - V_C}{R_C} \Rightarrow \frac{10 - 7.925}{5}$$

$$I_C = 0.415A$$

Q2.



Applying KVL at I/P



$$+9V - V_{BE} = I_B R_B$$

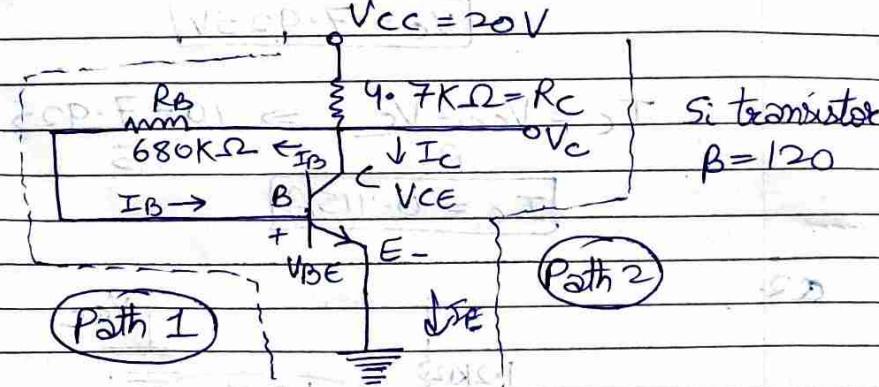
$$I_B = 9 - 0.7V$$

$$[I_B = 0.083A]$$

$$V_{BE} = V_B - V_E \\ 0.7 = V_B + 9$$

$$V_B = -8.3V$$

Q3.



Find  $I_C$ ,  $V_{CE}$ ,  $V_B$  &  $V_C$

Applying KVL for path 1:

$$V_{CC} - V_{BE} = I_B R_B + (I_B + I_C) R_C \\ \Rightarrow V_{CC} - V_{BE} = I_B [(1 + \beta) R_C + R_B] \quad (\because I_C = \beta I_B) \\ \Rightarrow 20 - 0.7 = I_B [121 \times 4.7 \times 10^3 + 680 \times 10^3] \\ 19.3 = I_B \times 1248.7 \times 10^3 \\ I_B = 15.5 \mu A$$

$$\text{As } I_C = \beta I_B \Rightarrow I_C = 1.86 \text{ mA}$$

Applying KVL for path 2:

$$V_{CC} - V_{CE} = (I_B + I_C) R_C \\ 20 - V_{CE} = (15.5 \times 10^{-6} + 1.86 \times 10^{-3}) 4.7 \times 10^3 \\ V_{CE} = 20 - 8.815 \\ V_{CE} = 11.185 V = V_C \\ \text{Also } V_{BE} = V_B - V_E = 0.7 \Rightarrow V_B = 0.7 \text{ (as } V_E = 0)$$

22-7-19

## Unit - I

1. Introduction to BJT
2. Need of biasing
3. DC/AC load line
4. Q-point
5. Biasing methods

↓      ↓      ↓  
Fixed Emitter Self  
Biasing Biasing Biasing

## 6. Compensation Techniques

- We know that the value of  $\beta$ ,  $V_{BE}$  &  $I_C$  depends on temperature.
- With the rise in Temperature, these parameters can be changed.
- The proper value of voltage & resistances stabilised a set of DC voltage & current for active region operation.
- These values of voltages & currents gives the Q-point (Quiescent point) of the transistor.
- The process of giving proper supply voltage & resistance gives the Q-point.

23.7.19

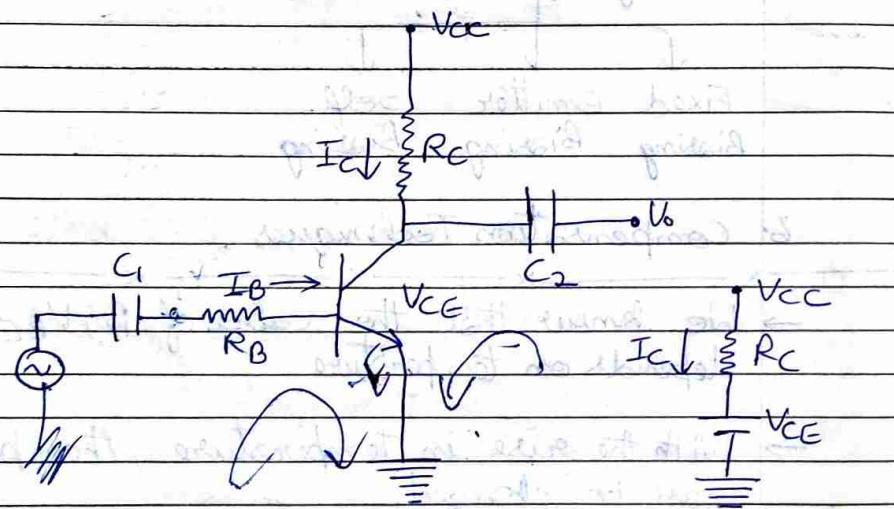
→ The  $I_C$  in CE configuration can be explained;

$$I_C = \beta I_B + I_{CEO}$$

$$I_C = \beta I_B + (\beta + 1) I_C$$

→ To stabilize Q-point biasing is needed.

# DC Load Line:



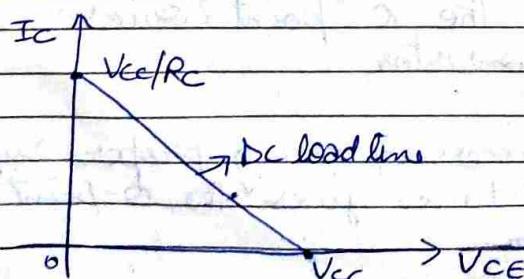
Applying KVL at O/P

$$V_{CC} - V_{CE} = I_C R_C$$

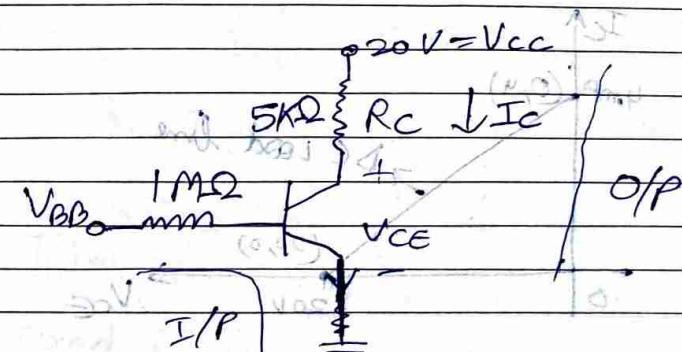
$$\text{Put } V_{CE} = 0 \Rightarrow I_C = V_{CC}/R_C$$

$$\text{Put } I_C = 0 \Rightarrow V_{CE} = V_{CC}$$

DC Load line:



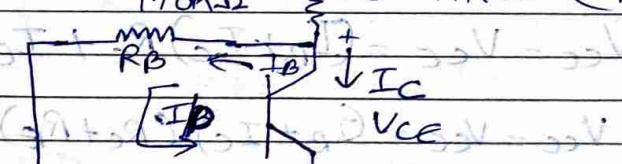
Q1. Draw the DC load line for the given circuit.



Q2. Determine the levels of  $I_C$  &  $V_{CE}$  for the given circuit.  $\beta = 90$ ,  $V_{BE} = 0.7V$

$$+20V = V_{CC}$$

$$470k\Omega \parallel R_C = 9.1k\Omega \quad (I_B + I_C)$$



$$V_{BE} = 0.7V$$

$$R_E = 2k\Omega \downarrow I_C$$

Ans. Applying KVL at O/P

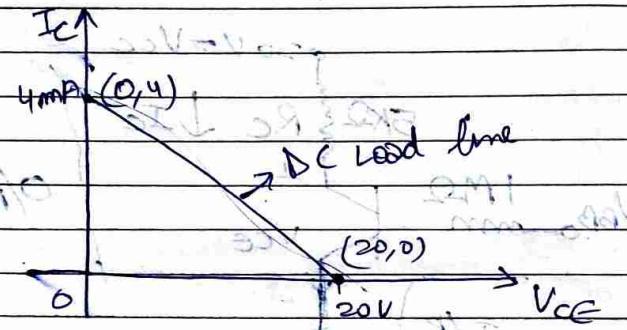
$$V_{CC} - V_{CE} = I_C R_C$$

$$\text{Put } V_{CE} = 0$$

$$\Rightarrow I_C = \frac{V_{CC}}{R_C} = \frac{20V}{5k\Omega} = 4mA$$

Put  $I_C = 0$

Then  $V_{CE} = V_{CC} = 120V$  ~~at~~ forward  $\rightarrow 10$



Ans 2. Applying KVL at I/P

$$V_{CC} - V_{BE} = I_B R_B + (I_B + I_C) R_E + I_C R_C \rightarrow ①$$

KVL at O/P

$$V_{CC} - V_{CE} = (I_B + I_C) R_E + I_C R_C \rightarrow ②$$

$$V_{CC} - V_{CE} = (I_B + I_C)(R_E + R_C) \quad (\text{because } I_C = I_B + I_E)$$

$$\Rightarrow V_{CC} - V_{CE} = (I_B + \beta I_B)(R_E + R_C)$$

$$V_{CC} - V_{CE} = 91 \times I_B (R_E + R_C) \rightarrow ③$$

From eq<sup>n</sup> ①

$$V_{CC} - V_{BE} = I_B R_B + (I_B + \beta I_B)(R_E + R_C)$$

$$20 - 0.7 = I_B [R_B + 91(R_E + R_C)]$$

$$19.3 = I_B [470 \times 10^3 + 91(2k\Omega + 9.1k\Omega)]$$

$$I_B = \frac{19.3}{1480.1 \times 10^3} = 0.013 \text{ mA}$$

Put value of  $I_B$  in eq<sup>n</sup> ③

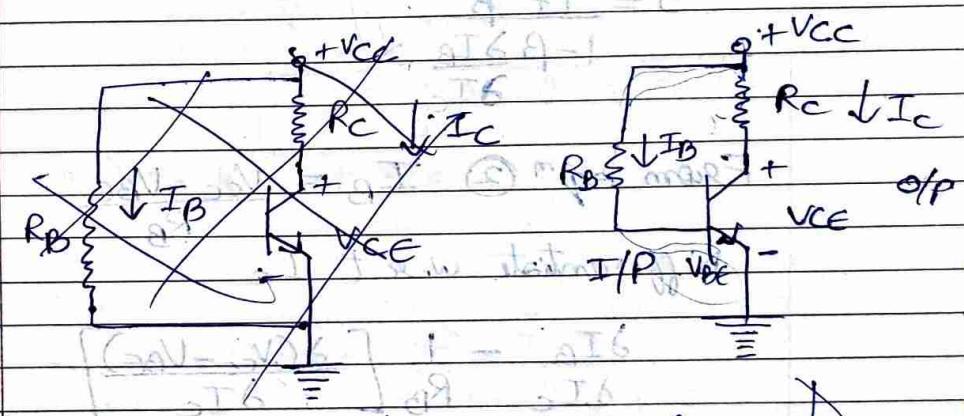
$$\Rightarrow 20 - V_{CE} = 13.17$$

$$\therefore V_{CE} = 6.82V$$

$$\& I_C = 0.62 \text{ mA} \quad (\text{from eq<sup>n</sup> ①})$$

# Types of Biasing:

I Fixed Biasing:



Applying KVL at O/P terminal

$$V_{CC} - V_{CE} = I_C R_C \rightarrow ①$$

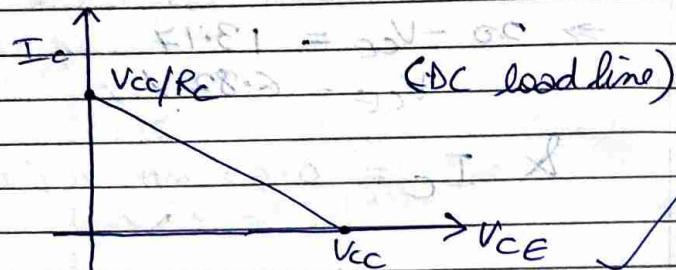
Now applying KVL at I/P terminal

$$V_{CC} - V_{BE} = I_B R_B \rightarrow ②$$

From eq<sup>n</sup> ①

$$\text{Put } V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C}$$

Put  $I_C = 0 \Rightarrow V_{CE} = V_{CC}$



Stability Factor: (in I/P terminal always)

$$S = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

$$\text{From eqn } ② \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Differentiate w.r.t  $I_C$

$$\frac{\partial I_B}{\partial I_C} = \frac{1}{R_B} \left[ \frac{\partial (V_{CC} - V_{BE})}{\partial I_C} \right]$$

$$= \frac{1}{R_B} [0] \quad (\text{because } V_{CC}, V_{BE} \text{ are constant})$$

∴

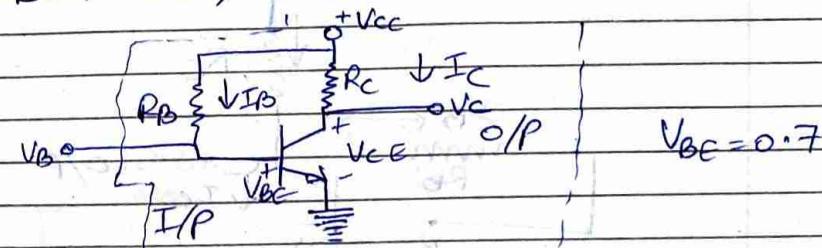
$$\frac{\partial I_B}{\partial I_C} = 0 \quad (\text{if } R_B \text{ is small})$$

$$\Rightarrow S = \frac{1 + \beta}{1 - \beta \times 0}$$

$$[S = 1 + \beta]$$

### Homework - T

- Q1. For the given circuit if  $R_B = 240k\Omega$ ,  $R_C = 2.2k\Omega$ ,  $V_{CC} = 12V$ ,  $\beta = 75$  then find the value of  $I_{BO}$ ,  $I_{CO}$ ,  $V_{CEO}$ ,  $V_B$ ,  $V_c$  &  $V_{BC}$ .



A1. Applying KVL at I/P we get,

$$V_{CC} - V_{BE} = I_B R_B \rightarrow ①$$

$$12 - 0.7 = I_B R_B$$

$$I_B = \frac{11.3}{240} \text{ mA} = 0.047 \text{ mA}$$

Applying KVL at O/P we get,

$$V_{CC} - V_{CE} = I_C R_C$$

$$V_{CE} = V_{CC} - \beta I_B R_C \quad (\text{because } I_C = \beta I_B)$$

$$V_{CE} = 12 - 75 \times 0.047 \times 2.2$$

$$V_{CEO} = 12 - 7.755$$

$$V_{CEO} = 4.245V$$

$$V_{CC} - V_{CE} = I_C R_C \Rightarrow I_C = \frac{12 - 4.245}{R_C}$$

$$[I_C = 3.525 \text{ mA}]$$

$$\text{Now } V_{BE} = V_B - V_E = 0.7$$

$$\Rightarrow V_B - 0 = 0.7 \quad (\text{as } V_E = 0V)$$

$$[V_B = 0.7V]$$

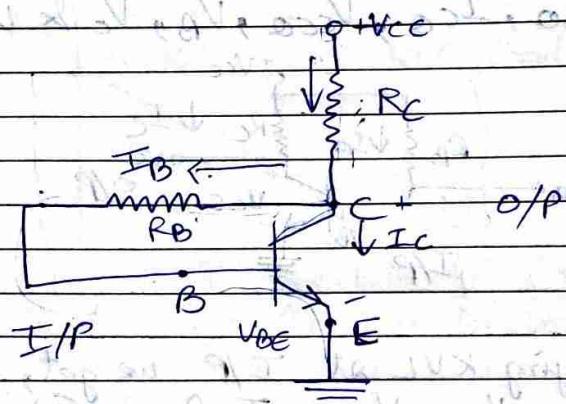
$$V_{CE} = V_C - V_E = 4.245$$

$$[V_C = 4.245V] \quad (\text{as } V_E = 0V)$$

$$\text{Also } V_{BC} = V_B - V_C = 0.7 - 4.245 = -3.545V$$

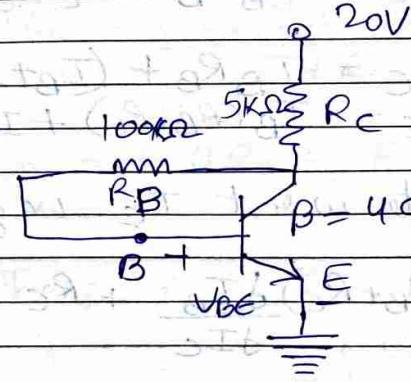
$$[V_{BC} = -3.545V]$$

## II Collector to Base Bias Circuit:



value of  $R_B$  &  $R_C$  because for every value of  $R_B$  &  $R_C$ ,  $S \leq 1 + \beta$ .

Q1.



Applying KVL for I/P

$$V_{CC} - V_{BE} = (I_B + I_C)R_C + I_B R_B$$

$$V_{CC} - V_{BE} = I_B (R_B + R_C) + I_C R_C \rightarrow ①$$

Differentiate eq "①" w.r.t  $I_C$  both side

$$0 = (R_B + R_C) \frac{dI_B}{dI_C} + R_C$$

$$\frac{dI_B}{dI_C} = -\frac{R_C}{R_B + R_C}$$

$$\text{Stability factor} = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$$

$$= \frac{1 + \beta}{1 + \beta \left( \frac{R_C}{R_B + R_C} \right)}$$

→ Here the circuit is stable for any

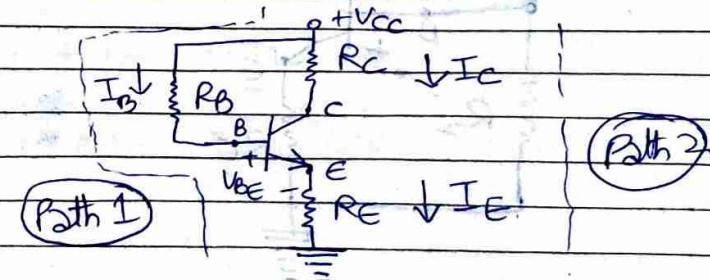
Find the value of S.

$$S = \frac{1 + \beta}{1 + \beta (R_C / R_B + R_C)}$$

$$S = \frac{50}{1 + 49 \left( \frac{50}{105} \right)}$$

$$S = \frac{50}{155}$$

## III Emitter Bias Circuit:



Applying KVL at I/P,

$$V_{CC} - V_{BE} = I_B R_B + I_E R_E$$

$$V_{CC} - V_{BE} = I_B R_B + (I_B + I_C) R_E$$

$$V_{CC} - V_{BE} = I_B (R_B + R_E) + I_C R_E$$

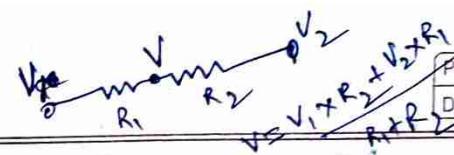
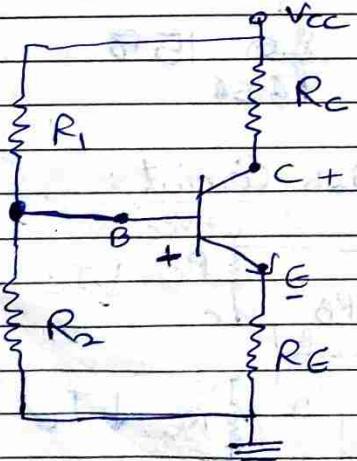
Differentiate w.r.t  $I_C$  we get,

$$0 = (R_B + R_E) \frac{dI_B}{dI_C} + R_E$$

$$\Rightarrow \frac{dI_B}{dI_C} = -\frac{R_E}{R_B + R_E}$$

$$\text{Stability Factor, } S = \frac{1 + \beta}{1 + \beta \left( \frac{R_E}{R_B + R_E} \right)}$$

#### IV Self Biasing / Voltage Divider Biasing:



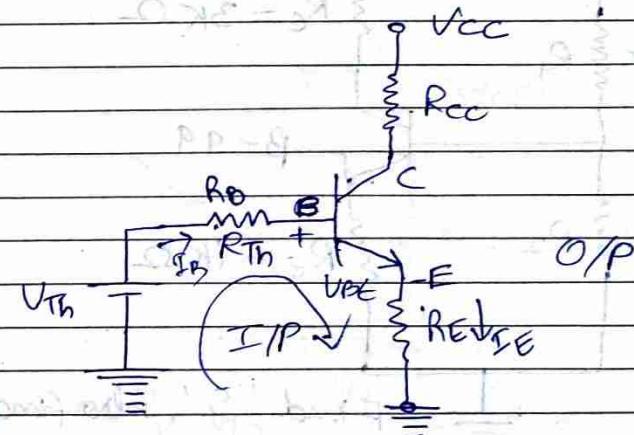
Applying

Thevenin theorem,

$$V_{TH} = \frac{V_{CC} \times R_2 + 0 \times R_1}{R_1 + R_2} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$R_{TH} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Thevenin Eq. Circuit



Applying KVL in I/P

$$V_{TH} - V_{BE} = I_B R_B (0 + R_{TH}) + I_E R_E$$

$$V_{TH} - V_{BE} = I_B (R_{TH} + R_E) + I_E R_E$$

Differentiate w.r.t  $I_C$  we get,

$$0 = \frac{dI_B}{dI_C} (R_{TH} + R_E) + R_E$$

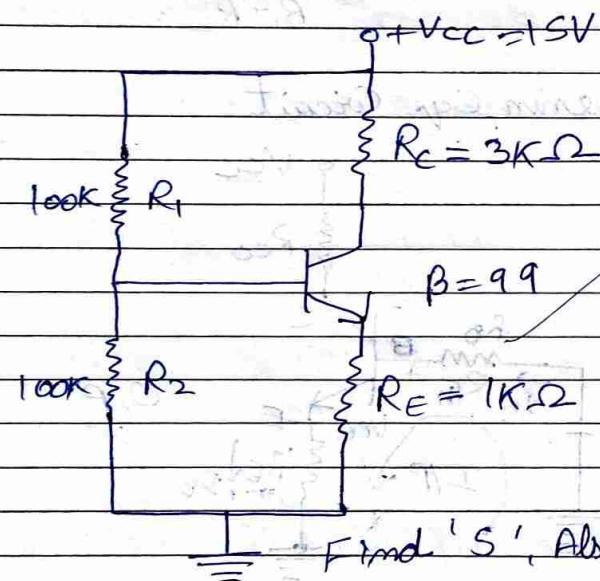
$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_{Th} + R_C}$$

Stability factor,  $S = \frac{1+\beta}{1+\beta \left( \frac{R_E}{R_{Th} + R_E} \right)}$

29-7-19

GATE:

Q1.

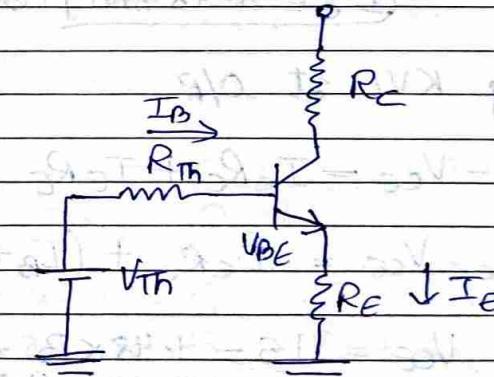


Ans.  $R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$   
 $= \frac{100 \times 100}{200}$   
 $= 50\text{k}\Omega$

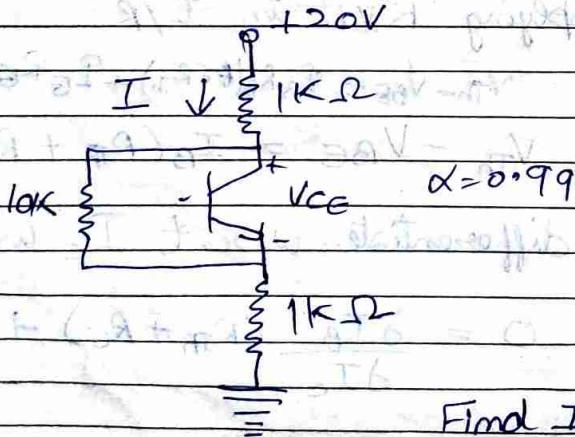
Stability factor,  $S = \frac{1+\beta}{1+\beta \left( \frac{R_E}{R_{Th} + R_E} \right)}$

$$= \frac{1+99}{1+99 \left( \frac{1}{50} \right)}$$

= 34.01 Circuit is stable



Q2.



$$V_{Th} = \frac{V_{cc} \times R_2}{R_1 + R_2}$$

$$= \frac{15 \times 100}{200}$$

$$V_{Th} = 7.5\text{V}$$

Applying KVL at T/P.

$$V_{Th} - V_{BE} = I_B R_B + I_E R_E \rightarrow ①$$

$$V_{Th} - V_{BE} = I_B R_B + I_B R_C + \beta I_B R_E$$

$$7.5 - 0.7 = I_B (R_B + R_E + \beta R_E)$$

$$I_B = \frac{6.8}{50 + 1 + 99} \text{ mA}$$

$$I_B = 45.3 \mu\text{A}$$

Put value of  $I_B$  in eq<sup>n</sup> ①

$$7.5 - 0.7 = I_B (R_B + R_E) + I_C R_E$$

$$I_C R_E = 6.8 - 0.0453 \times 51$$

$$I_C = 4.48 \text{ mA}$$

$$\boxed{I_C = 4.48 \text{ mA}} \quad \text{or} \quad I_C = \frac{\beta I_B}{9}$$

Applying KVL at O/P

$$V_{CC} - V_{CE} = I_C R_C + I_E R_E$$

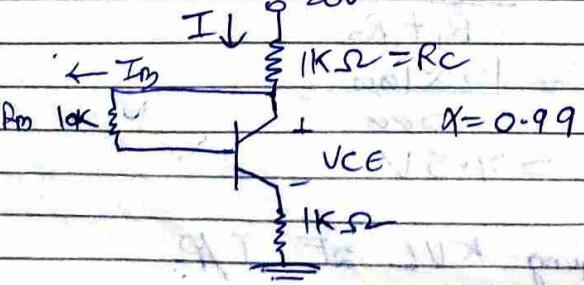
$$V_{CE} - V_{CC} = I_C R_C + (I_B + I_C) R_E$$

$$V_{CE} = 15 - 4.48 \times 3 - (4.48 + 0.0453) \times 1$$

$$= 15 - 13.44 - 4.52$$

$$= -2.96$$

$\pm 20V$



A32.

Applying KVL at I/P

$$20 - V_{BE} = I_R C + I_B R_B + I_E R_E$$

$$19.3 = I_R C + I_B R_B + I_E R_E \rightarrow ①$$

Applying KVL at O/P

$$V_{CC} - V_{CE} = I_R C + I_E R_E$$

$$V_{CC} - V_{CE} = (I_B + I_C) R_C + I_E R_E \rightarrow ②$$

From eq<sup>n</sup> ①

$$19.3 = (I_B + I_C) R_C + I_B R_B + I_E R_E$$

$$19.3 = I_B (R_C + R_B) + I_C R_C + I_E R_E$$

$$\text{Also } \beta = \frac{\alpha}{1-\alpha}$$

$$= \frac{0.99}{0.01} = 99$$

$$19.3 = I_B (R_C + R_B) + \beta I_B R_C + (I_B + I_C) R_E$$

$$19.3 = I_B [R_C + R_B + \beta R_C + (1+\beta) R_E]$$

$$I_B = \frac{19.3}{1 + 10 + 99 \times 1 + 100 \times 1} \text{ k}\Omega$$

$$I_B = \frac{19.3}{210} \text{ mA}$$

$$\boxed{I_B = 91.9 \mu\text{A}}$$

$$\text{Also } I_C = \beta I_B$$

$$\Rightarrow I_C = 99 \times 0.091 \text{ mA}$$

$$I_C = 9.09 \text{ mA}$$

$$I = I_B + I_C = 9.09 + 0.091$$

$$I = 9.18 \text{ mA}$$

Also from eqn ②

$$V_{CE} = 20 - I_B [ (1+\beta) R_C + (1+\beta) R_E ]$$

$$= 20 - 0.091 [ 100 \times 1 + 100 \times 1 ]$$

$$V_{CE} = 1.8 \text{ V}$$

## # Bias Compensation Techniques:

### (I) Thermistor:

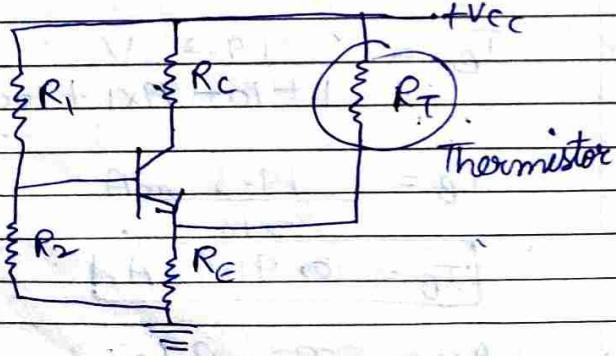
### (II) Sensistor:

### (III) Variation of $V_{BE}$ :

### (IV) Variation of $I_{CO}$ :

### (I) Thermistor Compensation Techniques:

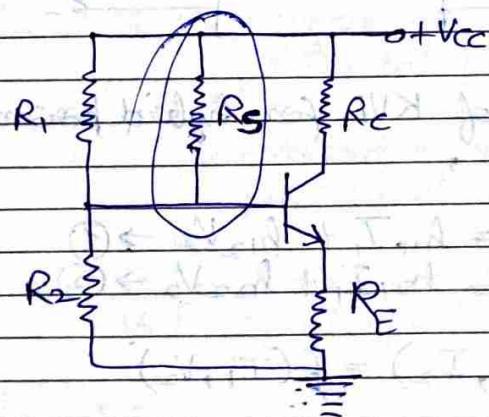
→ Thermistor is NTC (Negative Temperature Coeff.).



→ With increase in temp.  $R_T$  decreases & hence  $R_E$  decreases i.e. emitter current  $I_E$  increases.

→ With increase in  $T_E$ ,  $V_{BE}$  decreases & hence  $I_B$ . Consequently  $I_C$  reduces & maintain its original value. Hence any increase in temp. does not effect the  $I_C$  & Q-point remains unchanged.

### 30. 7.19 (II) Sensistor Compensation Technique:



→ Sensistor is positive temperature coeff. (PTC), it means  $R_s$  increases with increase in temp.

→ When temperature increases,  $R_s$  also increases causing an increase in the resultant resistance  $\frac{R_1 R_s}{R_1 + R_s}$

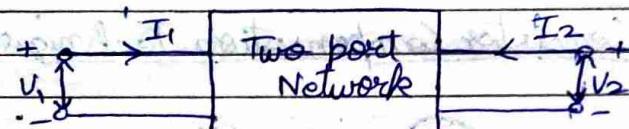
→ It decreases the voltage drop across  $R_2$ .

Hence bias voltage at the base decreases &  $I_C$  decreases.

→ Therefore, increased  $I_C$  due to temp. is compensated by transistor.

### # Small Signal Amplifier: (Hybrid Parameters)

Let us consider a two-port network



The eq<sup>n</sup> of KVL for hybrid parameter can be written as,

$$V_1 = h_{11} I_1 + h_{12} V_2 \rightarrow ①$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \rightarrow ②$$

$$(V_1, I_2) = f(I_1, V_2)$$

To find the hybrid parameters,

Case-I: When ~~V<sub>2</sub>~~ = 0 then from eq<sup>n</sup> ① & ②

$$\begin{aligned} V_1 &= h_{11} I_1 \\ I_2 &= h_{21} I_1 \end{aligned}$$

$$h_{11} = \frac{V_1}{I_1} \quad \& \quad h_{21} = \frac{I_2}{I_1}$$

(unit =  $\Omega$ ) (unit = unitless)

Case-II: Put  $I_1 = 0$  in eq<sup>n</sup> ① & ②

$$V_1 = h_{12} V_2$$

$$I_2 = h_{22} V_2$$

$$\Rightarrow h_{12} = \frac{V_1}{V_2} \quad \& \quad h_{22} = \frac{I_2}{V_2}$$

Unit = unitless

Unit = mho/dimension

$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$  = Input impedance with output port short circuited

$h_{22} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$  = Reverse voltage transfer ratio with input port open circuited

$h_{21} = \left. \frac{I_2}{I_1} \right|_{V_2=0}$  = Forward current gain with output port short circuited

$h_{12} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$  = Output admittance with input port open circuited.

Notations:

$$i = 11 = I/P, o = 22 = O/P$$

$f = 21 = \text{forward transfer}, r = 12 = \text{reverse transfer}$

### # Hybrid Model for a two-port Network:

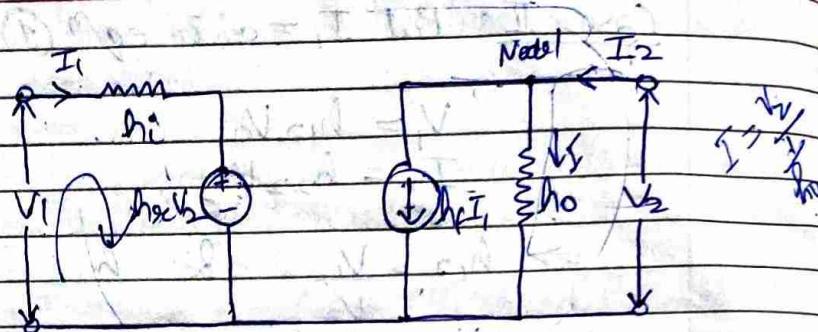
Common hybrid model for two-port network is as follows:

P.T.O.

Fig. Hybrid mode

Page No. \_\_\_\_\_  
Date \_\_\_\_\_

Page No. \_\_\_\_\_  
Date \_\_\_\_\_



For first port, (KVL)

$$V_1 - h_{21}V_2 = h_i I_1 \Rightarrow V_1 = h_i I_1 + h_{21}V_2 \rightarrow ①$$

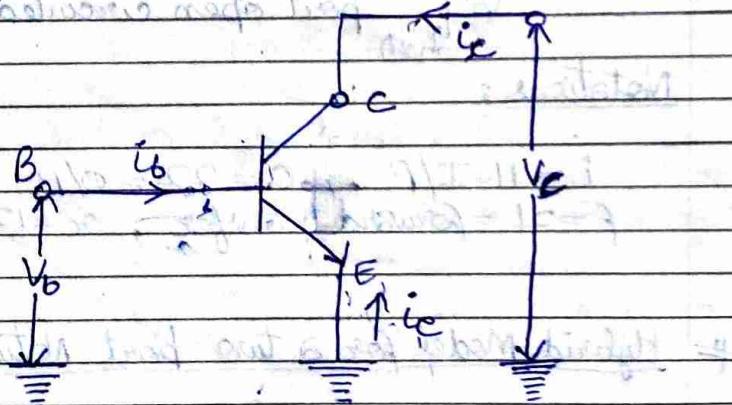
Apply KCL at Node 1, we get,

$$I_2 = h_f I_1 + V_2 \quad (\text{where } h_o \text{ is admittance})$$

$h_o$  is hence resistance =  $1/h_o$

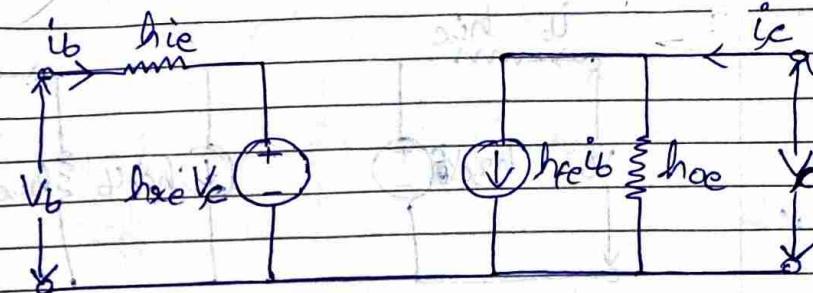
$$\Rightarrow I_2 = h_f I_1 + V_2 h_o \rightarrow ②$$

# Hybrid Model for Common-Emitter Configuration:

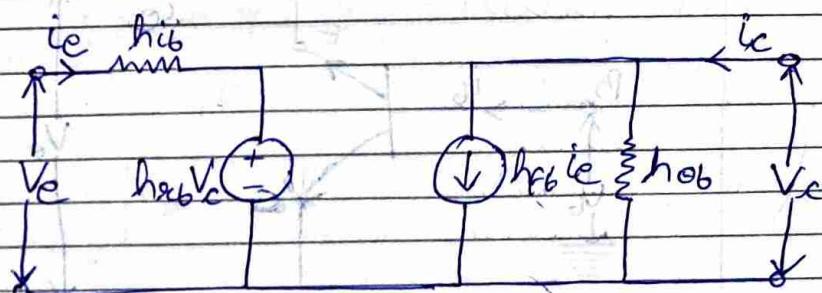


Hybrid Model:  $V_b = h_{ie} i_e + h_{ce} V_c \rightarrow ①$

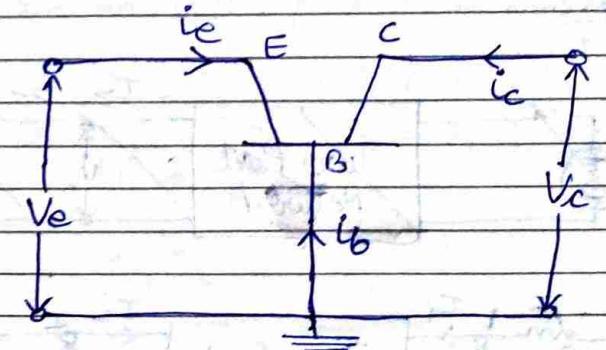
 $i_c = h_{fe} i_e + h_{oe} V_c \rightarrow ②$



# Hybrid Model for Common-Base Configuration:



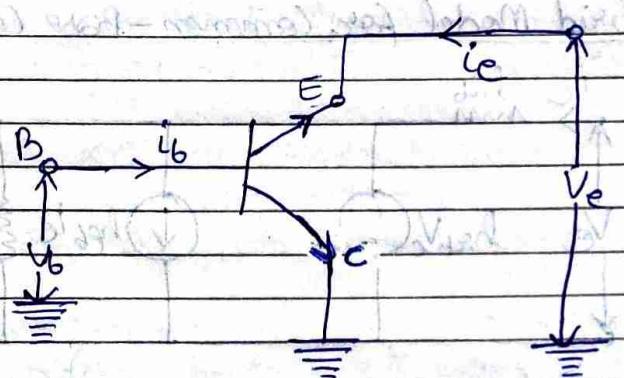
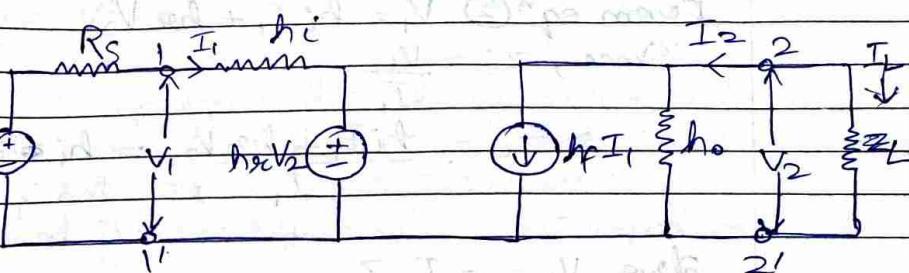
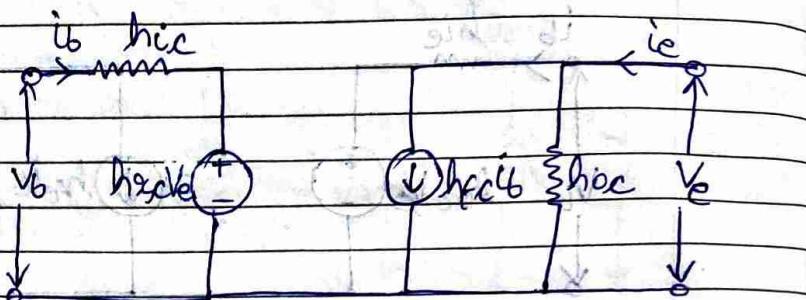
$$V_e = h_{ib} i_e + h_{cb} V_c \rightarrow ①$$
 $i_c = h_{fb} i_e + h_{ob} V_c \rightarrow ②$



# Hybrid Model for Common-Collector Configuration:

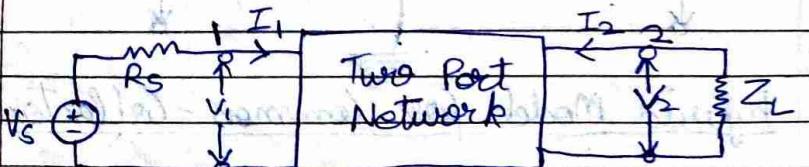
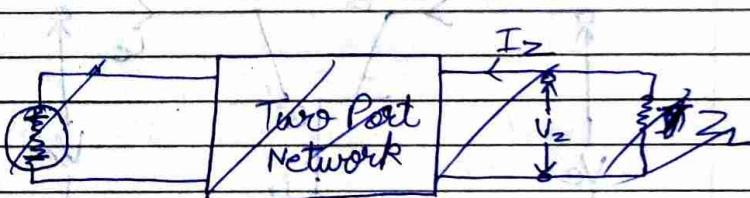
Hybrid Model:  $V_b = h_{ic} i_e + h_{ce} V_c \rightarrow ①$

 $i_e = h_{fc} i_b + h_{ac} V_c \rightarrow ②$



5.8.19

Analysis of Transistor amplifier using Hybrid-model:



1. Current Gain or Current amplification factor:  
It is the ratio of output current to input current.  
i.e.  $A_I = \frac{I_2}{I_1}$  Since  $I_2 = -I_L$ ,

$$\Rightarrow A_I = -\frac{I_2}{I_1} \rightarrow ①$$

$$V_1 = h_{iE} I_1 + h_{re} V_2 \rightarrow ②$$

$$I_2 = h_f I_1 + h_o V_2 \rightarrow ③$$

From eq. ③, putting the value of  $V_2 = -I_2 Z_L$

$$\Rightarrow I_2 = h_f I_1 + h_o (-I_2 Z_L)$$

$$\Rightarrow I_2 (1 + h_o Z_L) = h_f I_1$$

$$\Rightarrow \text{Also } A_I = -\frac{I_2}{I_1}$$

$$\Rightarrow A_I = -\frac{h_f}{1 + h_o Z_L}$$

2. Input Impedance ( $Z_i$ ): The input impedance, we looking into the amplifier input terminal (1, 1') is the amplifier input impedance  $Z_i$  or  $Z_i = \frac{V_1}{I_1}$ .

From eq<sup>n</sup> ②  $V_1 = h_i I_1 + h_{re} V_2$

Since,  $Z_i = \frac{V_1}{I_1}$

$$\Rightarrow Z_i = \frac{h_i I_1 + h_{re} V_2}{I_1} = h_i + h_{re} \frac{V_2}{I_1}$$

also  $V_2 = -I_2 Z_L$

$$V_2 = A_I I_1 Z_L \quad (\text{because } A_I = -\frac{I_2}{I_1})$$

$$\Rightarrow Z_i = h_i + h_{re} A_I Z_L \quad (\text{because } A_I = -\frac{h_f}{1+h_o Z_L})$$

$$Z_i = h_i - \frac{h_{re} h_f}{Y_L + h_o} \quad (\text{where } Y_L = \frac{1}{Z_L})$$

Admittance

3. Voltage Gain or Voltage amplification factor:  
The voltage gain can be written as the ratio of output to input voltage i.e.  $A_v = \frac{V_2}{V_1}$

$$A_v = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

4. Output Admittance  $Y_o$ :

$$Y_o = \frac{I_2}{V_2}$$

From eq<sup>n</sup> ③ we have,  $I_2 = h_f I_1 + h_o V_2$

$$\therefore Y_o = \frac{h_f I_1 + h_o V_2}{V_2}$$

$$\Rightarrow Y_o = \frac{h_f I_1 + h_o}{V_2} \quad & Z_o = \frac{V_2}{I_1}$$

Consider the source voltage is short circuited

i.e.  $V_S = 0$

6.8.4

- (i) C-E amplifier has h-parameters given by  
 $h_{ie} = 1000 \Omega$ ,  $h_{re} = 2 \times 10^{-4}$ ,  $h_{fe} = 50$  &  $h_{oe} = 25 \mu mho$   
If load & source resistance are  $1 k\Omega$ , then  
find (i) Current gain, (ii) Input impedance  $Z_i$  &  
(iii) Voltage gain.

Ans. 1.

$$h_{ie} = 1000 \Omega$$

$$h_{re} = 2 \times 10^{-4}$$

$$h_{fe} = 50$$

$$h_{oe} = 25 \mu mho$$

$$\begin{aligned} (i) A_I &= \frac{-h_{fe}}{1 + h_{oe} Z_L} \\ &= \frac{-50}{1 + 25 \times 10^{-6} \times 10^3} \\ &= -50 \\ (ii) A_v &= -\frac{1 + 0.025}{1 + 0.025} \\ &= -48.78 \end{aligned}$$

$$Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}}$$

$$\begin{aligned} &= 1000 - \frac{2 \times 10^{-4} \times 50}{10^{-3} + 25 \times 10^{-6}} \\ &= 1000 - \frac{10^2}{1.025 \times 10^3} \\ &= 1000 - 9.756 \end{aligned}$$

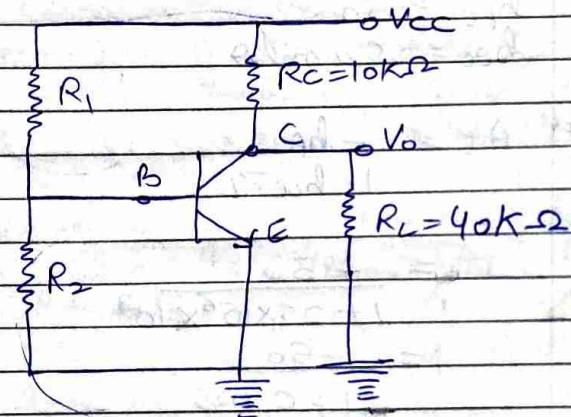
$$Z_i = 990.24 \Omega$$

$$(iii) A_v = \frac{A_I Z_L}{Z_i}$$

$$A_V = \frac{-48.78 \times 10^3}{990.24}$$

$$A_V = -49.26$$

- Q2. A transistor amplifier circuit with  $R_i = 100\text{ k}\Omega$ ,  $R_o = 50\text{ k}\Omega$ ,  $R_C = 10\text{ k}\Omega$  &  $R_L = 40\text{ k}\Omega$  has the hybrid parameters  $h_{ie} = 1100\text{ }\Omega$ ,  $h_{fe} = 100$ ,  $h_{re} = 10 \times 10^{-4}$ ,  $h_{oe} = 4 \times 10^{-4}\text{ mho}$ . Determine the input impedance & voltage gain. Find ac input impedance of the amplifier.



$$Ans 2: Z_i = h_{ie} = h_{fe} h_{re} \\ Y_L + h_{oe}$$

$$\Rightarrow Y_L = \frac{1}{Z_L} = \frac{R_C + R_L}{R_C R_L} \quad (\text{because here an extra resistance } R_C \text{ is also given which is connected in (1)}) \\ = \frac{50\text{ k}\Omega}{40\text{ k}\Omega}$$

$$Y_L = 0.125 \times 10^3 \Omega$$

$$Z_i = 1100 - \frac{100 \times 10 \times 10^{-4}}{10^3 \times 0.125 + 0.0004}$$

$$= 1100 - \frac{10^{-1}}{0.125} \times 0.525$$

$$= 1100 - 0.19 \\ Z_i = 1099.8 \Omega$$

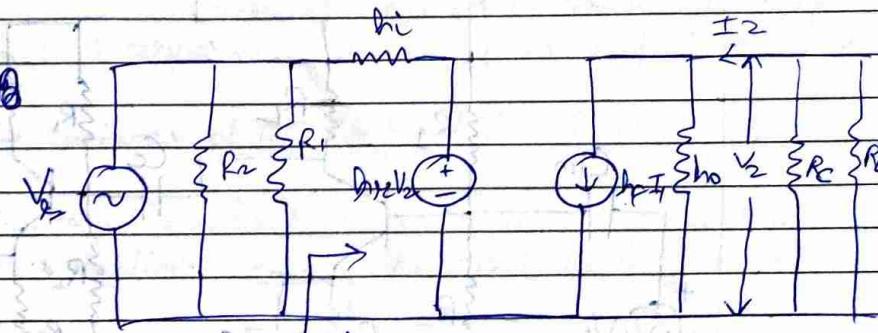
$$A_V = \frac{A_I Z_L}{Z_i}$$

$$\Rightarrow \text{Also } A_I = \frac{-h_{fe}}{1 + h_{oe} Z_L}$$

$$A_I = -23.8$$

$$A_V = -23.8 \times 8 \times 10^3 \\ 1099.8$$

$$A_V = 173.19$$



$$\text{Ac input impedance} = Z_i || R_1 || R_2 \\ - 0.222\Omega$$

$$R_1 || R_2 = 100 \times 10^3 \times 50 \times 10^3 \\ 150 \times 10^3$$

$$= \frac{500 \times 10^3}{150} \\ 150$$

$$= 3.33 \text{ k}\Omega$$

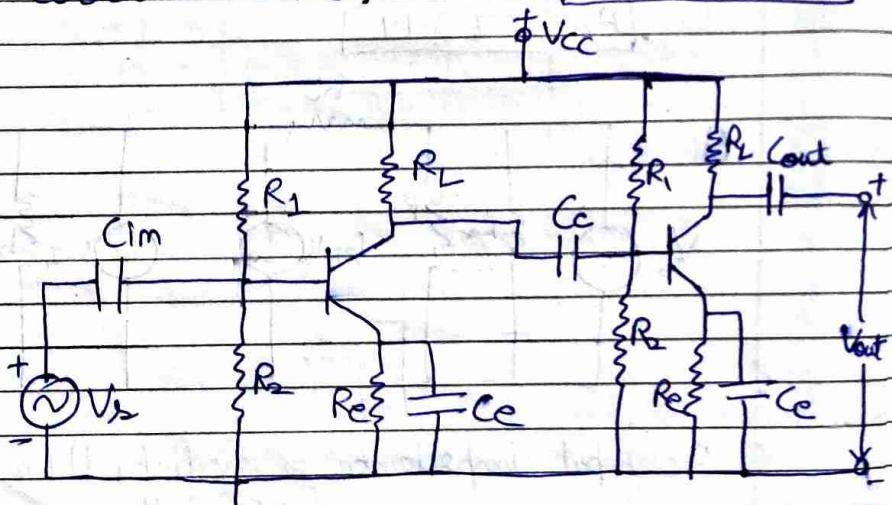
$$\text{Ac input} \Rightarrow Z_i = 11.3 \cdot 33.3 \text{ k}\Omega$$

$$\text{impedance} \Rightarrow \frac{1099.8 \times 33.3}{4433.13} \cdot 3.12$$

$$= 826.94 \Omega$$

### 19.8.19 R-C Coupled Amplifier:

01. Explain RC coupled amplifier (6 or 6.5 marks) in ET
02. What are the advantages, disadvantages, and applications of RC coupled amplifier. (2 or 3 marks in sessional & ET)
03. Derive the voltage gain & current gain in mid frequency range of RC coupled amplifier (6 or 6.5 marks). [ET → End Term]



### Construction & Working:

01. The resistors  $R_1, R_2, R_E$  for stabilization circuit & also  $R_1$  &  $R_2$  provides biasing for the circuit.

02. The emitter bypass capacitor  $C_E$  offers low reactance path to the input signal.
03. The input capacitor  $C_{in}$  couples the AC signal at the Base of the transistor.
04. In the absence of  $C_{in}$ , the signal source will be in parallel with  $R_1$  & the biasing voltage of the Base will be changed. Hence, the function of  $C_{in}$  is to provide only AC signal to the circuit.
05. The output of first stage is coupled to the input of second stage through coupling capacitor ( $C_c$ ). It allows the AC component only & blocks the DC component.
06. If the AC signal is applied to the first stage then it appears across  $R_L$  in amplified form.

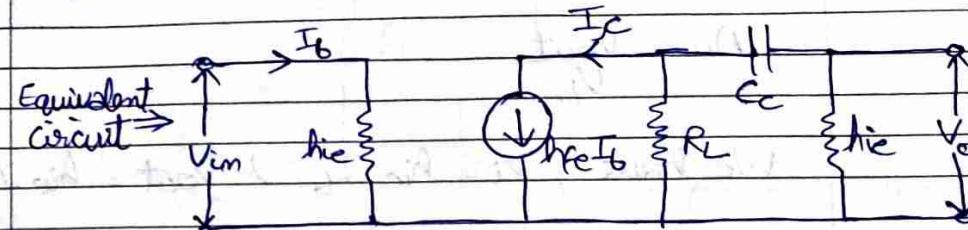
### # Advantages of RC Coupled Amplifier:

01. Since it contains resistors, capacitors & transistors. Hence, the cost is very low.
02. It provides a uniform voltage amplification over a wide range of frequencies.
03. It has minimum non-linear distortion.
04. It has higher amplification over other coupling amplifiers.

## # Disadvantages of RC Coupled Amplifier:

1. It is noisy.
2. Poor impedance matching

equivalent circuit is,



## # Applications of RC coupled Amplifier:

1. Audio fidelity is excellent over a wide range of frequency.

## # Mid Frequency Range of R-C Coupled Amplifier:

### Analysis of RC Coupled Amplifier:

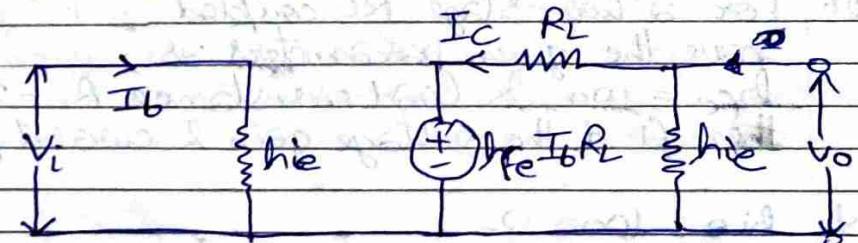
#### Assumptions:

1.  $h_{fe}$  is so small, hence the voltage source  $h_{fe}V_b$  or  $h_{fe}V_2$  can be neglected.
2. The value of  $I_b$  is large hence it can be assumed as  $h_{ie}$  an open circuit.
3. The reactance of  $C_c$  for any given input frequency is so small, hence the parallel combination of  $R_L$  &  $C_c$  can be considered as short circuit.
4. The bias resistors  $R_b$  &  $R_f$  are generally large as compared to  $h_{ie}$ .

With the help of our assumptions the simplified

~~Equivalent~~ For mid-frequency range the capacitor is short circuited & the current source is change into voltage source.

#### Equivalent Circuit:



#### Current Gain:

$$A_I = \frac{\text{Output current}}{\text{Input current}}$$

$$A_I = \frac{I_C}{I_b}$$

$$\text{where, } I_C = \frac{h_{fe}I_bR_L}{R_L + h_{ie}}$$

$$\Rightarrow A_I = \frac{h_{fe}R_L}{R_L + h_{ie}}$$

## 2. Voltage Gain:

$$A_V = \frac{V_{out}}{V_{in}}$$

We have,  $V_i = h_{ie} I_b$  &  $V_{out} = h_{fe} I_c$

$$\Rightarrow A_V = \frac{h_{fe} I_c}{h_{ie} I_b}$$

$$A_V = \frac{I_c}{I_b} = \frac{h_{fe} R_L}{R_L + h_{ie}}$$

- Q1. For a two-stage RC coupled amplifier we have the given parameters as,  $h_{ie} = 1000 \Omega$ ,  $h_{fe} = 100$ , & load resistance  $R_L = 200 \Omega$  then find the voltage gain & current gain.

Ans:  $h_{ie} = 1000 \Omega$

$h_{fe} = 100$

$R_L = 200 \Omega$

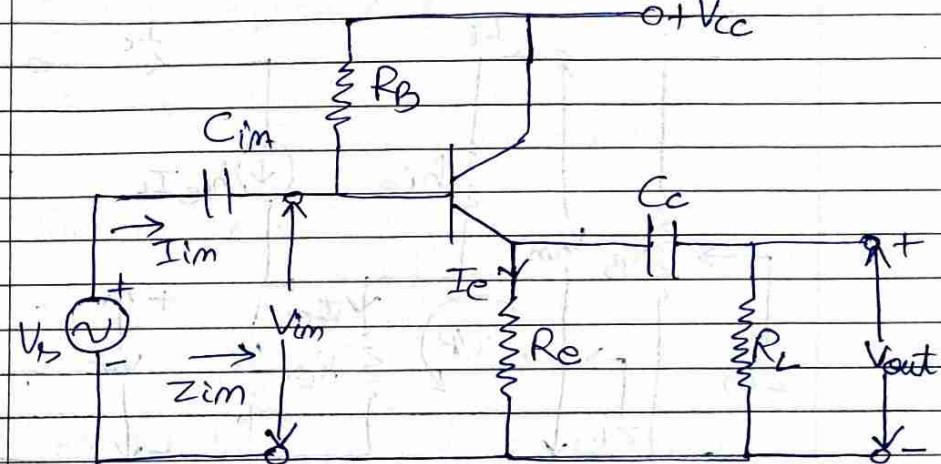
$$A_I = A_V = \frac{100 \times 200}{200 + 1000} = \frac{20000}{1200} = 16.67$$

$A_I = A_V = 16.67$

In emitter follower the input signal is applied at the base terminal & the output signal is taken from the emitter terminal.

## # Emitter Follower:

- This circuit provides a large input impedance, a small output impedance & a voltage gain



approximately equal to unity.

2. Since it has unity gain, hence the output voltage is in phase with input voltage & hence its name is emitter follower.

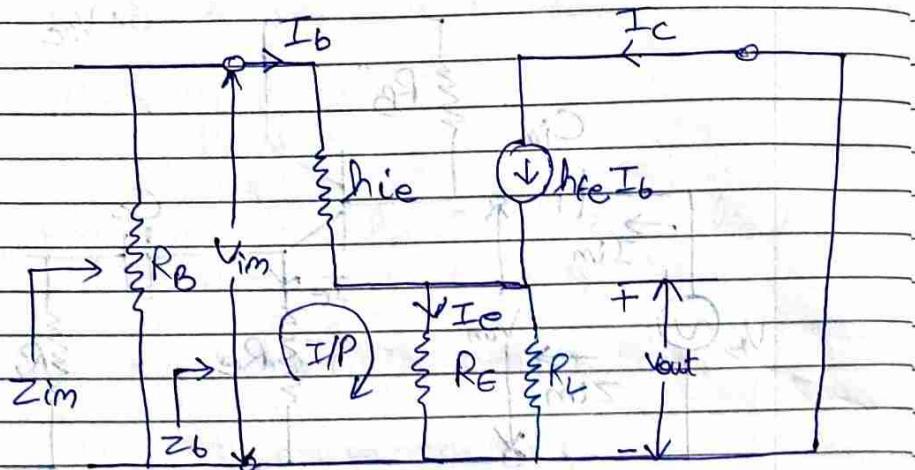
### Operation:

- When input signal  $V_i$  is applied to the base the emitter current  $I_e$  develops an output voltage  $V_{out} = I_e R_L$ .
- The output follows the input.

### Circuit Analysis of Emitter Follower Using Hybrid Parameter:

#### 1. Hybrid Model of Emitter Follower

On Next Page



### 1. Input Impedance:

Apply KVL at input terminal (Containing  $V_{in}$ ,  $h_{ie}$  &  $R_E$ )

$$V_{in} = I_B h_{ie} + I_E R_C$$

$$\Rightarrow V_{in} = I_B h_{ie} + (I_B + I_C) R_E$$

$$V_{in} = I_B h_{ie} + (I_B + \beta I_B) R_E$$

$$V_{in} = I_B [h_{ie} + (1 + \beta) R_E]$$

$$\text{Also } \beta = h_{fe}$$

$$\Rightarrow V_{in} = I_B [h_{ie} + (1 + h_{fe}) R_E]$$

$$\Rightarrow \frac{V_{in}}{I_B} = Z_B = [h_{ie} + (1 + h_{fe}) R_E]$$

Input impedance is given by  $Z_{in} = R_B || Z_B$

$$\Rightarrow Z_{in} = \frac{R_B [h_{ie} + (1 + h_{fe}) R_E]}{R_B + [h_{ie} + (1 + h_{fe}) R_E]}$$

2. Output Impedance ( $Z_{out}$ ): Since  $Z_B = \frac{V_{in}}{I_B}$

$$\text{So, } I_B = \frac{V_{in}}{Z_B} = \frac{V_{in}}{h_{ie} + (1 + h_{fe}) R_E} \rightarrow ①$$

$$\text{Since, } I_E = I_B + I_C$$

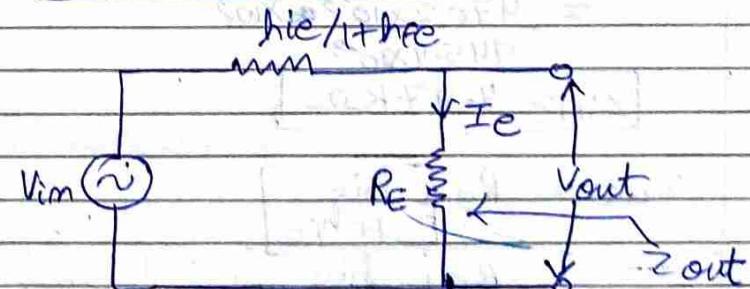
$$= I_B + \beta I_B$$

$$= (1 + \beta) I_B$$

$$I_E = I_B (1 + h_{fe}) \rightarrow ②$$

Now putting the value of  $I_B$  from eq "①" into ② we get,

$$I_E = \frac{V_{in}}{R_E + h_{ie} \frac{1}{1 + h_{fe}}}$$



$$\Rightarrow Z_{out} = R_E \parallel \frac{h_{ie}}{1 + h_{fe}}$$

### 3. Voltage gain:

$$V_o = I_E R_E$$

$$V_o = \frac{V_{in}}{R_E + h_{ie} \frac{1}{1 + h_{fe}}} \times R_E$$

$$\Rightarrow V_o = \frac{R_E}{V_{in} + R_E + h_{ie} \frac{1}{1 + h_{fe}}}$$

4. Current gain:

$$A_I = \frac{O/P \text{ current}}{I/P \text{ current}} = \frac{I_E}{I_B} \quad (\text{because } I_E = (1+hfe)I_B)$$

$$\Rightarrow \frac{R_E R_L}{R_E + h_{ie}} \quad [A_I = 1+hfe]$$

Q1. An emitter follower having the following parameters  $V_{CC} = 20 \text{ V}$ ,  $R_B = 5 \text{ k}\Omega$ ,  $R_E = 9.3 \text{ k}\Omega$ ,  $R_L = 18.6 \text{ k}\Omega$ ,  $h_{ie} = 1.1 \text{ k}\Omega$ ,  $h_{fe} = 100$ . Find value of input, output, voltage & current gain.

Ans1.

$$Z_{in} = \frac{5 \times 10^3}{(5 \times 10^3 + (1.1 \times 10^3 + (1+100)9.3 \times 10^3))} \times 10^3$$

$$= \frac{4702 \times 10^3}{945.4 \times 10^3} \times 10^3$$

$$[Z_{in} = 4.97 \text{ k}\Omega]$$

$$Z_{out} = \frac{R_E \left[ \frac{h_{ie}}{1+hfe} \right]}{R_E + \frac{h_{ie}}{1+hfe}}$$

$$= \frac{9.3 \times 10^3}{\left( \frac{9.3 \times 10^3 + 1.1 \times 10^3}{1+100} \right)} \Omega$$

$$= \frac{101.28 \times 10^3}{9.31 \times 10^3} \Omega$$

$$[Z_{out} = 10.87 \Omega]$$

$$\text{Voltage gain, } A_V = \frac{R_E}{R_E + \frac{h_{ie}}{1+hfe}}$$

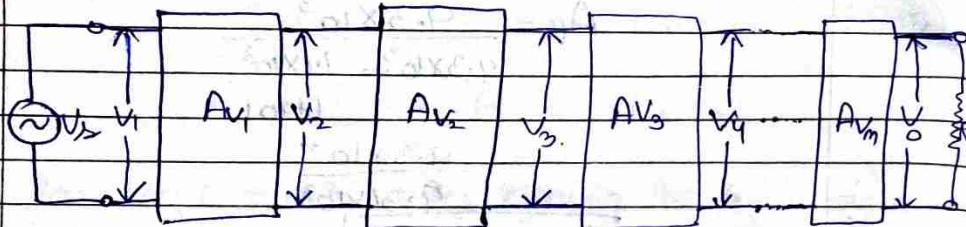
$$A_V = \frac{9.3 \times 10^3}{9.3 \times 10^3 + \frac{1.1 \times 10^3}{1+101}}$$

$$= \frac{9.3 \times 10^3}{9.31 \times 10^3}$$

$$[A_V = 0.998]$$

$$\text{Current gain, } A_I = \frac{1+hfe}{1+100}$$

$$[A_I = 101]$$

Unit - II~~Answers~~Cascade Amplifier or Multi-stage Amplifiers

(i) ~~A~~ A multistage amplifier is used to increase the amplification.

(ii) Cascading means the connection of first stage to the second stage & so on.

(iii) In multistage amplifier the input of first stage is connected to source voltage  $V_1$  & output of this stage is connected to input of second stage. Similarly, for further stages also.

(iv) The overall gain of multistage amplifier can be written as,

$$A_V = A_{V1} \times A_{V2} \times A_{V3} \times \dots \times A_{Vm-1} \times A_{Vm} \rightarrow ①$$

The overall gain in terms of dB can be expressed as,  $A_V(\text{in dB}) = 20 \log_{10} A_V$

$$= 20 \log_{10} (A_{V1} \times A_{V2} \times \dots \times A_{Vm})$$

$$A_V(\text{in dB}) = 20 \log_{10} A_{V1} + 20 \log_{10} A_{V2} + \dots + 20 \log_{10} A_{Vm}$$

Q: A multistage amplifier consists of three stages.

The voltage gains of stages are 60, 100 & 160. Find the overall voltage gain in dB.

Ans:  $A_{V1} = 60$

$A_{V2} = 100$

$A_{V3} = 160$

$A_V = A_{V1} \times A_{V2} \times A_{V3}$

$A_V = 960000$

$A_V(\text{in dB}) = 20 \log_{10} (960000)$

$[A_V(\text{in dB}) = 119.6 \text{ dB}]$

Q2. The overall voltage gain of a two-stage RC coupled amplifier is 80dB. If the voltage gain of second stage is 150, calculate the voltage gain of first stage in dB.

Ans:  $A_{V2} = 150$

$A_V = 80 \text{ dB}$

$A_V(\text{in dB}) = 20 \log_{10} A_{V1} + 20 \log_{10} (150)$

$\Rightarrow 20 \log_{10} A_{V1} = 36.47$

$\Rightarrow [A_{V1}(\text{in dB}) = 36.47 \text{ dB}]$

Q3:

In C-B configuration if  $\alpha = 0.988$  &  $I_C = 2 \text{ mA}$  then find base & emitter current.

Ans:  $\alpha = \frac{I_E}{I_C}$

$$I_E = \frac{I_C}{\alpha} = \frac{2 \times 10^{-3}}{0.988} \text{ A}$$

$I_E = 2.024 \text{ mA}$

$$I_B = I_E - I_C$$

$$I_B = (2.024 - 2) \text{ mA} = 24.2 \mu\text{A}$$

~~Unit 1~~ Q4. Find the relation b/w  $\alpha$ ,  $B$  &  $\gamma$ .

Ans 4. We know,  $\alpha = \frac{I_C}{I_E} \rightarrow ①$

$$B = \frac{I_C}{I_B} \rightarrow ②$$

$$\gamma = \frac{I_E}{I_B} \rightarrow ③$$

$$\Rightarrow \gamma = \frac{I_C + I_B}{I_B} \quad (\text{because } I_E = I_C + I_B)$$

$$\Rightarrow \gamma = \frac{I_C}{I_B} + 1$$

$$\Rightarrow \boxed{\gamma = B + 1} \quad (\text{because } B = \frac{I_C}{I_B})$$

Also  $\alpha = \frac{I_C}{I_E}$

$$\Rightarrow I_E \alpha = I_C$$

divide both sides by  $I_B$

$$\Rightarrow \frac{I_E}{I_B} \alpha = \frac{I_C}{I_B}$$

$$\Rightarrow \gamma \alpha = B$$

$$\text{or } \boxed{\gamma = \frac{B}{\alpha}}$$

& also  $I_E \alpha = I_C$

$$(I_C + I_B) \alpha = I_C \quad (\text{because } I_E = I_C + I_B)$$

$$\Rightarrow 1 + \frac{I_B}{I_C} \alpha = 1 \Rightarrow \boxed{\alpha = \frac{B}{B+1}}$$

Q5(a) Explain Cascode - Amplifier or CE-CB configuration of amplifier.

(b) Find the voltage gain, overall input impedance, overall voltage gain & overall current gain.

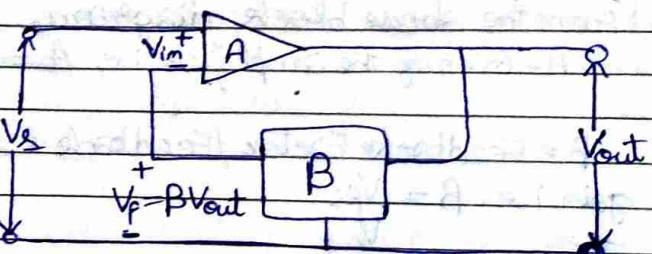
Ans 5(i) (a) Cascode - Amplifier is a composite amplifier having a large bandwidth which is used for RF applications & as a video amplifier.  
 (radio frequency) (88-108 MHz)

(ii) It consists of a common emitter amplifier followed by common base stage & ~~are~~ directly coupled to each other, that why it is called CE-CB configuration.

(iii) For high frequency applications, CB configuration has the most desirable characteristics but it suffers from low input impedance.

(iv) ~~in~~ the connection, ~~GE~~ with CB configuration provides good isolation b/w input & output.

# Feedback Amplifier : An amplifier with two input terminals & one output terminal is shown below,



From the given diagram,

$A$  = Amplifier Gain

$B$  = Feedback Factor / Feedback gain

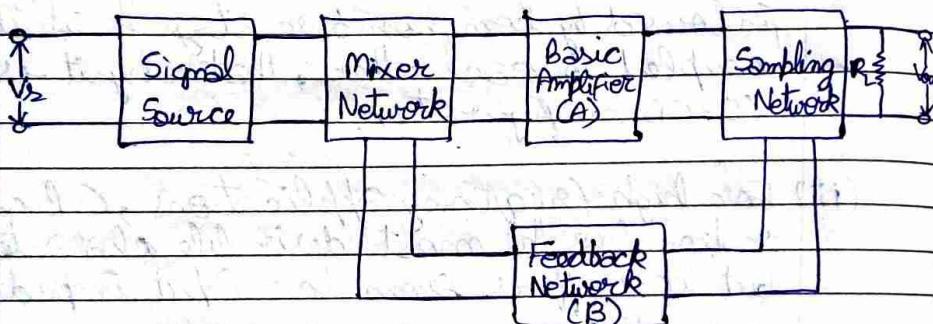
$V_f$  = Feedback voltage

Now apply KVL at input terminal we have,

$$V_s - V_{in} - V_f = 0$$

$$\Rightarrow V_s = V_{in} + V_f$$

### # Concept of Feedback (Positive or Negative):



1. Mixer Network provides the connections b/w signal source & feedback network either in series or in parallel.

2. Sampling Network provides voltage or current.

From the above block diagram,

$A$  = Gain of the amplifier i.e.  $A = \frac{V_{out}}{V_{in}}$

$B$  = Feedback Factor / Feedback ratio / Feedback gain i.e.  $B = \frac{V_f}{V_{out}}$

$A_f$  = Gain of Feedback amplifier i.e.  $A_f = \frac{V_{out}}{V_s}$

### # Positive Feedback:

1. If feedback voltage  $V_f$  is in phase with source signal  $V_s$ , then  $V_{in}$  can be written as,

$$V_{in} = V_s + V_f \rightarrow ①$$

2. Now the Feedback gain,  $A_f = \frac{V_{out}}{V_s}$

Put value of  $V_s$  in above eq<sup>n</sup> from eq<sup>n</sup> ①

$$\begin{aligned} \Rightarrow A_f &= \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{in} + V_f} \\ &= \frac{1}{\frac{V_{in}}{V_{out}} + \frac{V_f}{V_{out}}} = \frac{1}{\frac{V_{in}}{V_{out}} + \frac{1}{A}} \\ &= \frac{1}{\frac{V_{in}}{V_{out}}} - \frac{1}{\frac{1}{A}} \end{aligned}$$

$$\Rightarrow A_f = \frac{A}{1 - BA}$$

### 2/9/19 # Negative Feedback:

1. If feedback voltage  $V_f$  is out of phase with source signal  $V_s$ , then input voltage  $V_{in}$  can be written as,

$$\begin{aligned} V_{in} &= V_s - V_f \\ \text{i.e. } V_s &= V_{in} + V_f \end{aligned}$$

2. Now the gain with feedback can be written as,

$$A_f = \frac{V_{out}}{V_s}$$

$$= \frac{V_{out}}{V_{in} + V_f}$$

$$= \frac{\frac{V_m + V_f}{V_{out}}}{\frac{V_{out}}{V_{in}}} = \frac{V_m + V_f}{V_{in}}$$

$$= \frac{1}{1 + \beta}$$

$$\Rightarrow A_f = \frac{A}{1 + \beta A}$$

Q1. The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain with feedback if -ve feedback is applied. And also find the loop gain. Given that feedback fraction is 0.001.

$$A = 3000$$

$$\beta = 0.001$$

$$A_f = \frac{A}{1 + \beta A}$$

$$= \frac{3000}{1 + 3000 \times 0.001}$$

$$= \frac{3000}{4}$$

$$A_f = 750$$

$$\text{Loop gain} = AB$$

$$= 3000 \times 0.001$$

$$= 3$$

Q2. An amplifier has a voltage gain of 40. The amplifier is now modified to provide 10% -ve feedback with input. Calculate (i) Voltage gain with feedback ( $A_f$ ), (ii) Amount of Feedback in dB, (iii) Loop gain.

$$\text{Ans 2. } A = 40$$

$$\beta = 0.1$$

$$\begin{aligned} \text{(i) } A_f &= \frac{A}{1 + \beta A} \\ &= \frac{40}{1 + 40 \times 0.1} \\ &= \frac{40}{5} = 8 \end{aligned}$$

$$\begin{aligned} \text{(ii) } A_f (\text{in dB}) &= 20 \log_{10}(A_f) \\ &= 20 \log_{10}(8) \\ A_f (\text{in dB}) &= 18.06 \text{ dB} \end{aligned}$$

$$\begin{aligned} \text{(iii) Loop gain} &= \beta A \\ &= 0.1 \times 40 \\ &= 4 \end{aligned}$$

### Advantages of Negative Feedback:

1.) Gain Stability: The gain with negative feedback can be written as  $A_f = \frac{A}{1 + \beta A}$ . If the loop gain ( $\beta A$ ) is much greater than 1, then  $A_f = 1$ .

It means it is independent of amplifier parameters like resistors, capacitors etc.

Explanation of point (b):

With rise in temperature the variation in transistor parameters occurs and due to this gain can be changed. However, with negative feedback it is independent of these variations. If  $A_B$  is much greater than 1 then  $A_f = 1$ .

\* Note: We know that the feedback gain can be written as  $A_f = \frac{A}{1 + BA}$  → ①

Now differentiate eq^n ① w.r.t A.

$$\frac{dA_f}{dA} = \frac{(1+BA) - AB}{(1+BA)^2}$$

$$\frac{dA_f}{dA} = \frac{1}{(1+BA)^2} \rightarrow ②$$

Now eq^n ② can be written as,

$$dA_f = \frac{dA}{(1+BA)^2} \rightarrow ③$$

Now divide eq^n ③ by ① we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+BA)^2} \times \frac{(1+BA)}{A}$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{1}{1+BA} \times \frac{dA}{A} \rightarrow ④$$

The sensitivity of an amplifier is defined as the ratio of percentage change in transfer

gain with feedback to the percentage change in transfer gain without feedback i.e. sensitivity,  $S = \frac{dA_f}{A_f}$

$$\frac{dA_f}{A_f} = \frac{1}{1+BA} \quad (\text{from eq^n ④})$$

Q1 An amplifier having a close loop gain of 100 is required & this gain should not vary more than 1%, when the inherent gain of amplifier without feedback varies by 20%. Find the sensitivity of the amplifier.

(Inherent  $\rightarrow$  open loop)

Ans 1. Given, close loop gain  $A_f = 100$

$$\frac{dA_f}{A_f} = 1\% \quad (\text{close loop})$$

$$\frac{dA}{A}$$

$$\frac{dA}{A} = 20\% \quad (\text{open loop})$$

$$\Rightarrow S = \frac{\frac{dA_f}{A_f}}{\frac{dA}{A}} = \frac{\frac{1\%}{100}}{\frac{20\%}{2}} = \frac{0.01}{0.2} = 0.05$$

We have given that  $\frac{dA_f}{A_f} = 1\% = 0.01$

$$\frac{dA}{A} = 20\% = 0.2$$

(b) Calculate the feedback factor of loop gain i.e.

$$\text{Ans 1(b)} \quad S = \frac{1}{1+BA} \Rightarrow 0.05 = \frac{1}{1+BA}$$

$$1 + \beta A = 100$$

$$\beta A = 0.95$$

$$\beta A = 20 - 1$$

$$\boxed{\beta A = 19}$$

(I) Q1. Q2.

The open loop gain of an amplifier changes by 5%, if 10 dB -ve feedback is applied. Calculate the percentage change in the close loop gain.

Ans: Given,  $\frac{dA}{A} = 5\% = 0.05$

Ans: Q1.

If -ve feedback is given  
then gain =  $1 + \beta A$

$$dA_f = ?$$

$$A_f$$

$$\Rightarrow \text{gain (in dB)} = 10 \text{ dB}$$

$$\text{antilog}(10 \text{ dB}) = 3.1623$$

$$\Rightarrow 1 + \beta A = 3.1623$$

$$\beta A = 2.1623$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{1}{3.1623} \times 0.05$$

$$= 0.0158 \text{ or } 1.58\%$$

2) Reduced Non-linear Distortion: A large signal stage produces maximum distortion at the output. With -ve feedback it can be reduced by a factor  $1 + \beta A$ .

Explanation of point 2):

(i) Distortion occurs when transistor operates beyond its range of linear operation.

(ii) When -ve feedback is applied the input is increased by the same factor by which the gain is reduced.

(iii) Let the amplifier with open loop gain  $A$  & distortion  $D$  in the output signal without feedback. Now -ve feedback is applied, then close loop gain becomes  $A_f$  & distortion becomes  $D_f$ . Hence net distortion can be written as  $D_f = D - \beta A D_f$  or  $D_f = \frac{D}{1 + \beta A}$

Q3: The gain & distortion of an amplifier are 150 & 5% respectively without feedback. If 10% of its output applied as -ve feedback find the distortion of the amplifier with feedback.

Ans:  $A = 150$

$$D = 5\% = 0.05$$

$$\beta = 0.1$$

$$\rightarrow D_f = \frac{D}{1 + \beta A}$$

$$= 0.05$$

$$1 + 0.1 \times 150$$

$$D_f = 0.003125 = 0.31\%$$

3) Reduced Noise: With -ve feedback noise is also reduced by a factor  $1 + \beta A$ .

4) Increased Bandwidth: If  $A$  is the gain, then gain-bandwidth product can be written as

$A \times B.W = \text{constant}$   
↓ Bandwidth

With -ve feedback the amplifier gain is reduced, so obviously the bandwidth will increase to compensate the reduction in gain by the same factor.

5.) Increased input impedance: With -ve feedback the input impedance is increased. ( $R_{if} = R_i(1 + \beta A)$ )

6.) Decreased output impedance: With -ve feedback the output impedance is decreased,  $R_{of} = R_o(1 + \beta A)$ .

(IPU 2010, 2013)  
Q1. The output resistance of a voltage series feedback is  $10\Omega$ . If the gain of the basic amplifier is 100 & the feedback fraction is 0.01. What is the output resistance.

Ans.  $R_{of} = 10\Omega$   
 $\beta = 0.01$   
 $A = 100$

$$\Rightarrow R_{of} = R_o(1 + \beta A)$$

$$10 = R_o(1 + 0.01 \times 100)$$

$$\therefore R_o = \frac{10}{(1 + 0.01)} = 5\Omega$$

## # Classification of Feedback Amplifier:

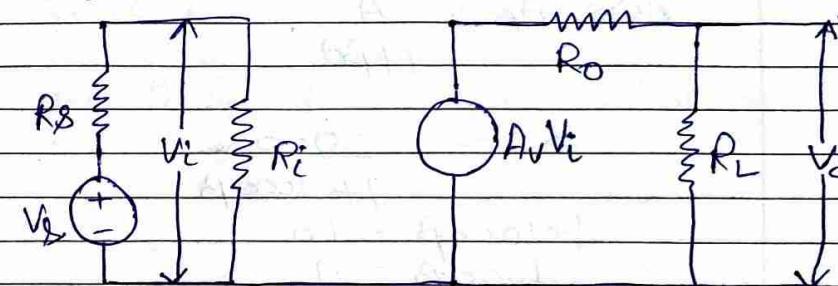
1) Voltage Amplifier

2) Current Amplifier

3) Trans Resistance Amplifier

## 4) Transconductance Amplifier

### 1.) Voltage Amplifier:



Voltage amplifier provides output in terms of voltage which is proportional to input voltage & this proportionality is independent of impedances of the given circuit.

Let  $R_i$  is much greater than  $R_g$  i.e.  $R_i \gg R_g$  then  $V_i \approx V_s$  & let  $R_L \gg R_o$  then  $V_o = A V_i$   
So, the voltage gain  $A_v = \frac{V_o}{V_i}$

$$\Rightarrow A_v = \frac{V_o}{V_i} \quad (\because V_i = V_s)$$

Q2. Voltage gain of an amplifier without feedback is ~~6dB~~ 6db if decreases to 40db with ~~loop~~ feedback. Find the feedback factor. Also find loop gain.

Ans.  $A = 60\text{db}$   
 $A_f = 40\text{db}$

Also  $A(\text{db}) = 20 \log_{10}(A)$   
 $\Rightarrow 60 = 20 \log_{10} A$   
 $A = 10^3$

$A_f(\text{dB}) = 20 \log_{10}(A_f)$

$$A_f^2 = 20 \log_{10} A_f$$

$$A_f = 10^2$$

Also  $A_f = \frac{A}{1 + \beta A}$

$$100 = \frac{1000}{1 + 1000\beta}$$

$$1 + 1000\beta = 10$$

$$1000\beta = 9$$

Feedback factor,  $B = 0.009$

Loop gain,  $\beta A = 9$

Q2. In a C-B configuration of a pnp transistor the current amplification factor is 0.988. Find the base current if emitter current is 1.2 mA.

$I_E = 1.2 \text{ mA}$

$$\beta = 0.988$$

$$\beta = I_C$$

$$I_E$$

$$I_C = \beta I_E$$

$$I_C = 1.18 \text{ mA}$$

Also  $I_B = I_E - I_C$

$$I_B = 1.2 - 1.18 \text{ mA}$$

$$I_B = 0.02 \text{ mA}$$

Q3. Explain the limitations of a fixed-biased circuit.

Ans 3(i) Fixed biased circuit provides poor stability

(ii) With replacement of transistor, the Q-point can be vary.

Q4. Compare the imp. characteristics of CE, CB & CC amplifier.

Ans 4. Typical Value

	CE	CB	CC
Voltage gain, $A_v$	High (-13)	High (13)	Low (-1)
Current gain, $A_i$	High (-46.5)	Low (1)	High (47.5) (Learn it)
Input impedance $Z_i$	Medium ( $10K\Omega$ )	Low ( $2.5K\Omega$ )	High ( $14.4K\Omega$ )
Output impedance $Z_o$	Medium ( $155K\Omega$ )	High ( $10K\Omega$ )	Low ( $80.5K\Omega$ )
	$K\Omega$	$K\Omega$	$K\Omega$
			$(450K\Omega)$

Q5. The overall gain of a 2-stage RC coupled amplifier is 80 dB. If the voltage gain of second stage is 150. Find the voltage gain of first stage in dB.

Ans 5.  $A_V = A_{V1} + A_{V2}$

Given,  $A_V = 80 \text{ dB} \Rightarrow 10000$

$$A_{V2} = 150 = 43.52 \text{ dB}$$

$$\Rightarrow A_{V1} = A_V - A_{V2} \text{ (in dB)}$$

~~$$A_{V1} = 80 - 43.52$$~~

$$A_{V1} (\text{dB}) = 20 \log (9850) [A_{V1} = 36.47 \text{ dB}]$$

$$A_{V1} (\text{dB}) = 79.86 \text{ dB}$$

Q6. Name of Region in which a transistor is used when used as (a) Amplifier, (b) Switch.

Ans 6(a) Active region

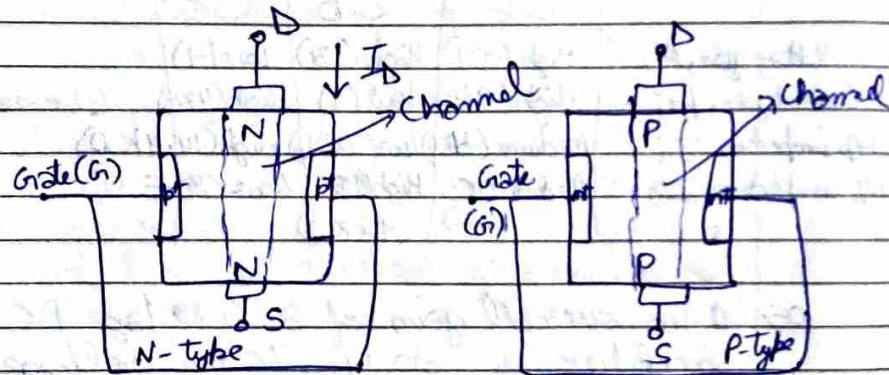
(b) Saturation or Cut off region

X X X

### Unit - III

#### # Field Effect Transistor (FET):

1. Unipolar Device (Either electrons or holes are responsible for conduction):



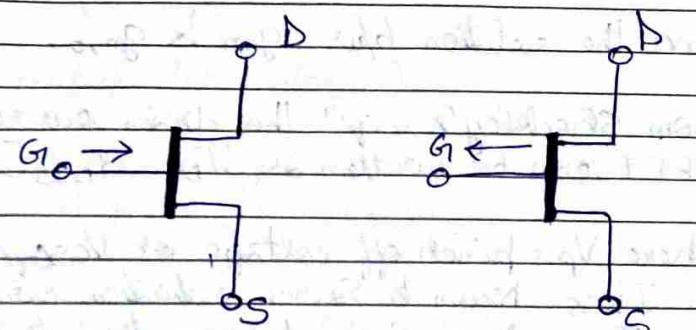
(a) Drain (D): The terminal through which the majority charge carriers leave the channel is called drain terminal.

(b) Gate (G): There are 2 internally connected heavily doped impurity regions formed by alloying or diffusion to create 2 p-n junctions.

(c) Source (S): The terminal through which majority charge carriers enter into the channel is called source.

FET → The FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence its name is Field Effect Transistor. Current conduction is only due to majority carriers. FET is said to be a unipolar device.

Circuit Symbol of FET:



N-type JFET

p-type JFET

Note: The shaded portion means that the junction is already b/w the majority carriers.

16/10/19

Parameters of FET:

(i) AC Drain Resistance:

It is defined as the ratio of change in drain to source voltage ( $V_{ds}$ ) to the change in drain current at constant Gate to source voltage ( $V_{gs}$ )

$$\therefore r_{ac} = \frac{\Delta V_{ds}}{\Delta I_D} \Big|_{V_{gs}=\text{const.}}$$

(ii) Transconductance ( $g_m$ ):

It is defined as the ratio of change in drain current to the change in gate to source voltage ( $V_{gs}$ ) at constant  $V_{ds}$  i.e.  $g_m = \frac{\Delta I_D}{\Delta V_{gs}} \Big|_{V_{ds}=\text{const.}}$

### Expression for Transconductance:

Imp

Q1. Find the relation b/w  $g_m$  &  $g_{m,0}$ .

Ans1. From Shockley's Eq<sup>m</sup> the drain current of a FET can be written as  $I_{DS} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$

where  $V_p$  = pinch off voltage or  $V_{GSOFF}$

$I_{DSS}$  = Drain to Source saturation current

$I_{DS}$  = Drain Current from drain to source

Differentiate eq<sup>m</sup> ① from both sides w.r.t  $V_{GS}$ .

$$\frac{dI_{DS}}{dV_{GS}} = 2 I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right] \left[ -\frac{1}{V_p} \right]$$

$$\frac{dI_{DS}}{dV_{GS}} = -2 \frac{I_{DSS}}{V_p} \left[ 1 - \frac{V_{GS}}{V_p} \right] \rightarrow ②$$

We know that  $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

$$\Rightarrow g_m = -2 \frac{I_{DSS}}{V_p} \left[ 1 - \frac{V_{GS}}{V_p} \right] \quad (\text{from eq } ②) \rightarrow ③$$

Putting the value of  $V_{GS} = 0$  in eq<sup>m</sup> ③ we have,

$$g_{m,0} = -2 \frac{I_{DSS}}{V_p} \rightarrow ④$$

when we short drain to source

From eq<sup>m</sup> ③ & ④ we get,

$$g_m = g_{m,0} \left[ 1 - \frac{V_{GS}}{V_p} \right]$$

### (iii) Amplification Factor ( $\mu$ ):

It is defined as the ratio of change in drain to source voltage to change in gate to source voltage i.e.  $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = g_d \times g_m \quad (\text{Here } g_d = g_{m,0})$$

### (iv) DC drain Resistance ( $R_D$ ):

$$R_D = \frac{V_D}{I_D}$$

Q2. A JFET has  $V_p = -4.5V$ ,  $I_{DSS} = 10mA$ , &  $I_{DS} = 2.5mA$ . Find transconductance  $g_m$ .

Ans2.  $\Rightarrow V_p = -4.5V$

$$I_{DSS} = 10mA$$

$$I_{DS} = 2.5mA$$

$$I_{DS} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$$

$$\Rightarrow 2.5 \times 10^{-3} = 10 \times 10^{-3} \left[ 1 + \frac{V_{GS}}{4.5} \right]^2$$

$$\Rightarrow 0.5 = 1 + \frac{V_{GS}}{4.5}$$

$$V_{GS} = -2.25V$$

$$g_m = \frac{2.5 \times 10^{-3}}{-2.25}$$

$$g_m = -0.0011 \text{ S/mA}$$

$$g_m = \frac{2 \times 10 \times 10^{-3}}{+4.5} \left[ 1 - \frac{2.25}{4.5} \right]$$

$$g_m = 2.22 \text{ mA/V}$$

Q2. An N-channel JFET has a pinch off voltage of  $-4.5V$  &  $I_{DSS} = 9\text{mA}$ . At what value of  $V_{GS}$  will  $I_{DS}$  be equal to  $3\text{mA}$ . What is the value of  $g_m$  at this  $I_{DS}$ ?

Ans.  $V_p = -4.5V$   
 $I_{DSS} = 9\text{mA}$   
 $I_{DS} = 3\text{mA}$   
 $V_{GS} = ?$

$$I_{DS} = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$$

$$\Rightarrow 3 \times 10^{-3} = 9 \times 10^{-3} \left[ 1 + \frac{V_{GS}}{4.5} \right]^2$$

$$\Rightarrow V_{GS} = -1.9V$$

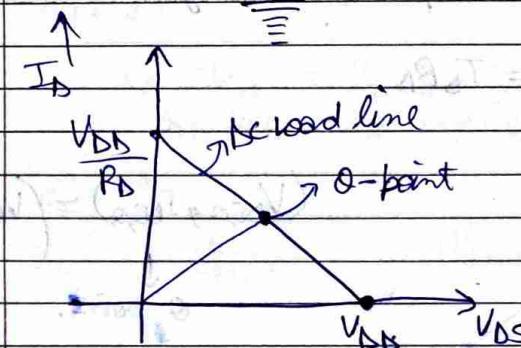
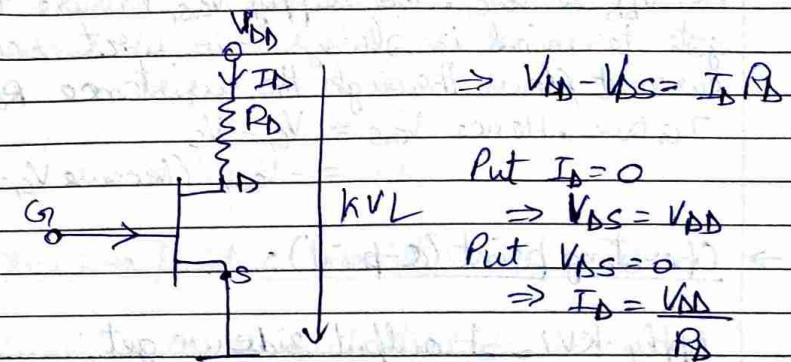
$$g_m = \frac{-2I_{DSS}}{V_p} \left[ 1 - \frac{V_{GS}}{V_p} \right]$$

$$= \frac{-2 \times 9 \times 10^{-3}}{-4.5} \left[ 1 + \frac{(-1.9)}{4.5} \right]$$

$$g_m = 2.3 \times 10^{-3} \text{ A/V}$$

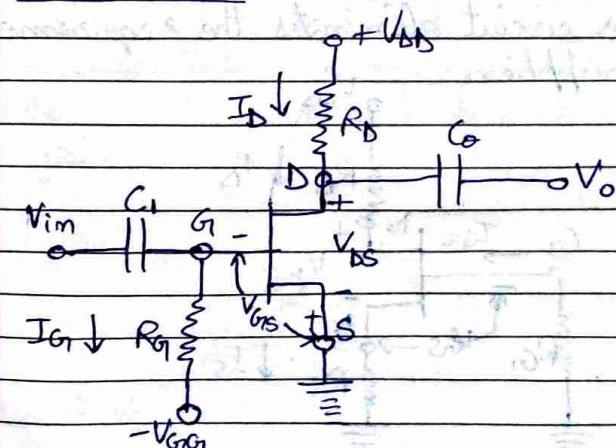
or  $2.31 \text{ mA/V}$

## # DC Load Line & Bias Point:



## 18-10-19 Types of Biasing:

### (I) Fixed Bias:

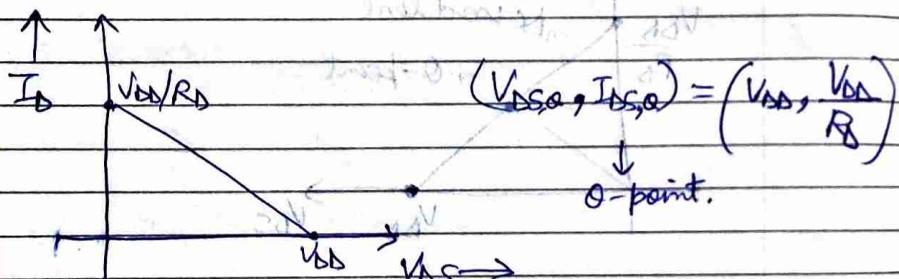


→ Fixed bias circuit uses 2 different power supplies i.e.  $V_{DD}$  &  $V_{SS}$ . The supply  $V_{G,G}$  ensure that the gate terminal is always -ve w.r.t. source & no current flows through the resistance  $R_G$  & hence  $I_G \approx 0$ . Hence  $V_{GS} = V_G - V_S$   
 $= -V_{G,G}$  (because  $V_G = -V_{G,S}$  &  $V_S = 0$ )

→ Operating point ( $\alpha$ -point):

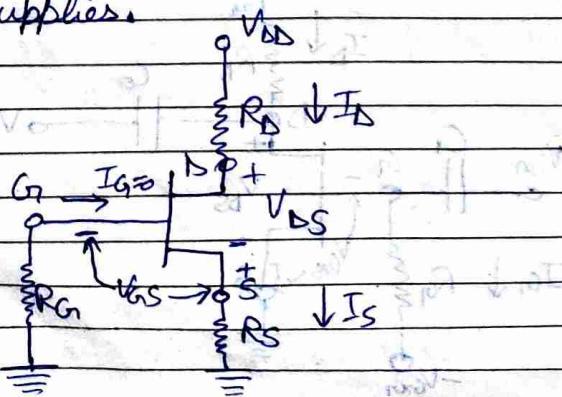
Apply KVL at output side we get

$$V_{DD} - V_{DS} = I_D R_D$$



## (II) Self Bias:

Self Bias circuit eliminates the requirement of 2 dc supplies.



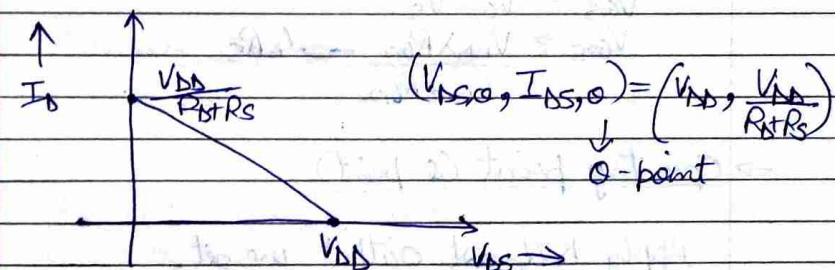
→ Since gate terminal is -ve w.r.t. source & hence no current flows through  $R_G$  due to reverse bias gate. So,  $V_{GS} = V_G - V_S$   
 $V_{GS} = 0 - I_D R_S$  (because  $I_S = I_D$  as  $I_G \approx 0$ )  
 $\Rightarrow V_{GS} = -I_D R_S$

→ Operating point ( $\alpha$ -point):

Apply KVL at output side we get,

$$V_{DD} - V_{DS} = I_D R_D + I_D R_S$$

$$V_{DD} - V_{DS} = I_D (R_D + R_S)$$

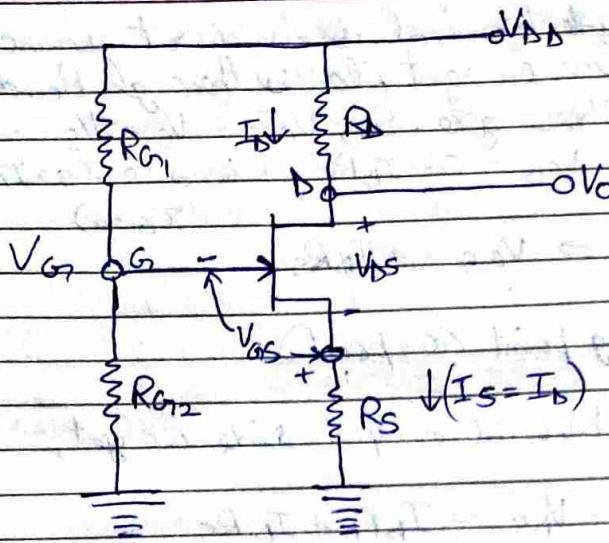


→ The voltage drop across  $R_S$  i.e.  $I_D R_S$  provides the voltage across gate to source terminal, ~~from gate to source terminal~~ & provided there is no need of extra power supply at gate terminal

## III Potential Divider Bias:

$$\rightarrow V_{GS} = \frac{V_{DD} \times R_{S2}}{R_{G1} + R_{S2}}$$

$$\& V_S = I_D R_S$$



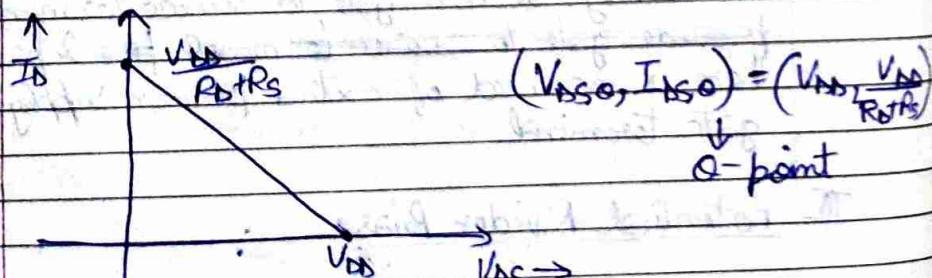
$$V_{GS} = V_G - V_S$$

$$V_{GS} = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}} - I_D R_S$$

→ Operating point (Q-point):

Apply KVL at output we get,

$$V_{DD} - V_{DS} = I_D (R_D + R_S)$$



- Q1. For a given N-channel JFET,  $I_{DSs} = 10\text{mA}$ ,  $V_p = -4\text{V}$ , &  $V_{GSs} = -1.5\text{V}$ . Find the Q-point and

draw the DC load line.

Ans1.

Applying KVL at output side,

$$V_{DD} - V_{DS} = I_D R_D$$

$$\Rightarrow 16 - V_{DS} = I_D (6\text{k}\Omega) \quad \text{①}$$

Also  $I_{DSs} = I_{DSs} \left[ 1 - \frac{V_{GSs}}{V_p} \right]$

$$\Rightarrow I_{DSs} = 10 \times 10^{-3} \left[ 1 - \frac{-1.5}{-4} \right]^2$$

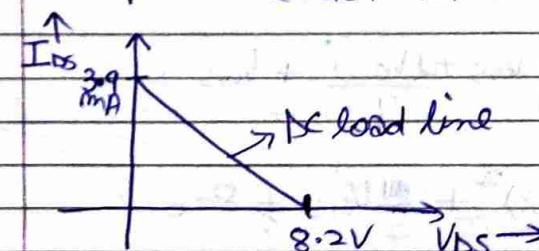
$$I_{DSs} = 3.9 \text{mA}$$

Put value of  $I_{DSs}$  in eqn ①

$$\rightarrow V_{DSs} = 16 - 3.9 \times 10^{-3} \times 2 \times 10^3$$

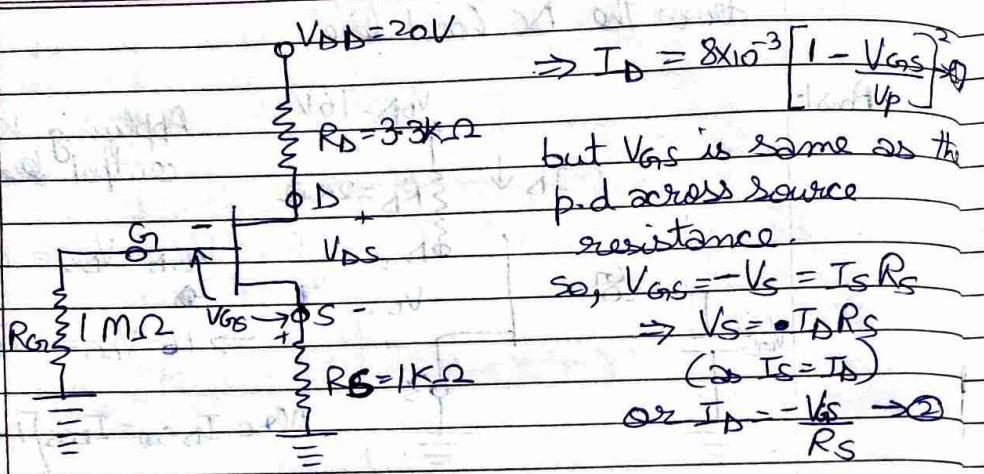
$$V_{DSs} = 8.2 \text{V}$$

$$\text{Q-point} = (V_{DSs}, I_{DSs}) = (8.2 \text{V}, 3.9 \text{mA})$$



- Q2. Find value of  $V_{GSs}$ ,  $I_D$ ,  $V_{DS}$ ,  $V_D$ ,  $V_G$ , and  $V_S$  for the following circuit. Given  $I_{DSs} = 8\text{mA}$  &  $V_p = -6\text{V}$ .

Ans2: We know  $I_{DS} = I_{DSs} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$



Comparing eq<sup>n</sup> ① & ② we get,

$$8 \times 10^{-3} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2 = -\frac{V_{GS}}{R_S}$$

③

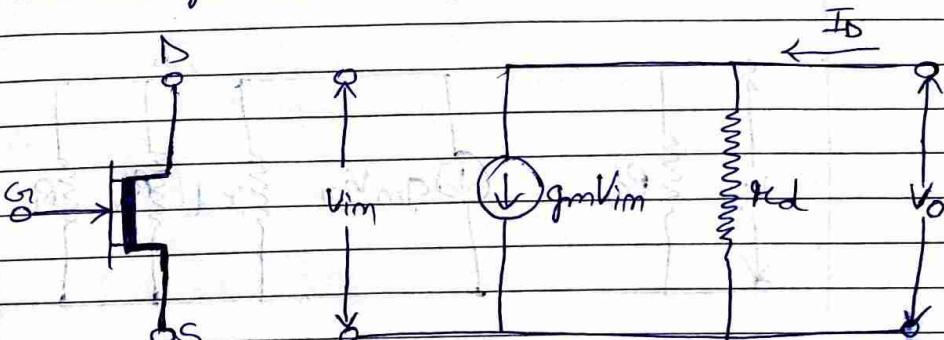
$$1 + \frac{2V_{GS}}{V_p} + \frac{(V_{GS})^2}{V_p^2} = -\frac{V_{GS}}{R_S}$$

$$\Rightarrow 8 + \frac{8}{3} V_{GS} + \frac{(V_{GS})^2}{9} + V_{GS} = 0$$

$$\Rightarrow \frac{2}{9} (V_{GS})^2 + \frac{11}{3} V_{GS} + 8 = 0$$

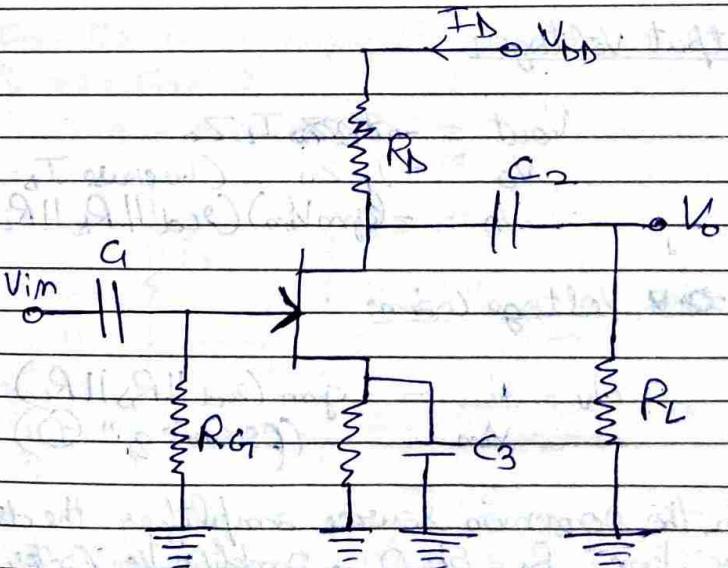
$$\Rightarrow V_{GS} = -2.58V$$

### # Small Signal Model of JFET:



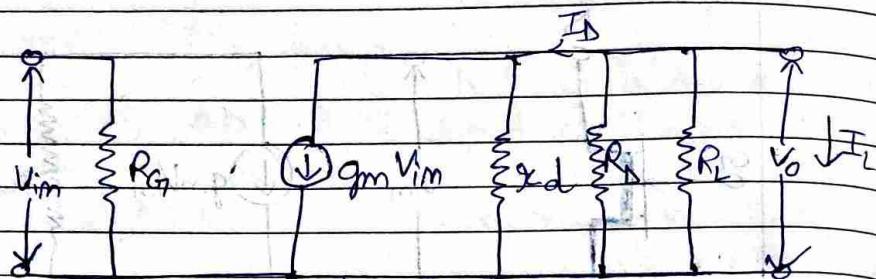
where  $g_m$  = Transconductance  
 $r_d$  = Ac resistance  
 $I_d$  = drain current

### # Small Signal model of Common Source JFET Amplifier:



The equivalent small signal model of common

source JFET amplifier is shown below;



1. Input Impedance:

$$Z_{in} = R_G$$

2. Output Impedance:

$$Z_{out} = r_d \parallel R_D \parallel R_o$$

3. Output Voltage:

$$V_{out} = -I_o Z_o$$

$$V_o = -I_o Z_o \quad (\text{because } I_o = -I_D)$$

$$V_o = -(g_m V_m) (r_d \parallel R_D \parallel R_o) \quad (1)$$

4. Voltage Gain:

$$A_v = \frac{V_o}{V_m} = -g_m (r_d \parallel R_D \parallel R_o)$$

(from eqn 1)

Q1. In the common source amplifier the drain resistance  $R_o = 5k\Omega$ , amplification factor  $u = 50$  &  $r_d = 35k\Omega$ . Find the voltage gain & o/p resistance.

$$R_o = 5k\Omega$$

$$u = 50$$

$$r_d = 35k\Omega$$

$$u = r_d \times g_m$$

$$\Rightarrow g_m = \frac{50}{35 \times 10^3}$$

$$g_m = 0.00142 S$$

$$A_v = -g_m (r_d \parallel R_o)$$

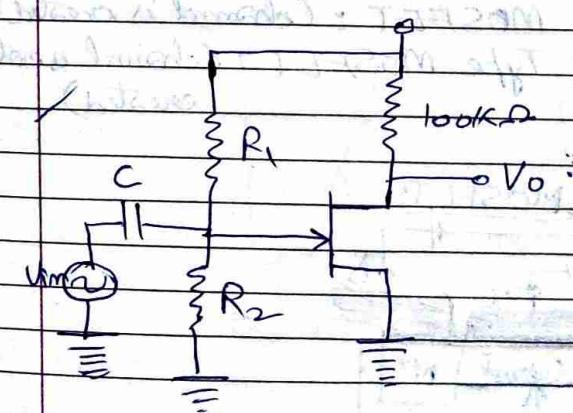
$$A_v = -0.00142 \left[ \frac{35 \times 10^3 \times 5 \times 10^3}{40 \times 10^3} \right]$$

$$A_v = -6.2$$

o/p resistance,  $R_o = r_d \parallel R_o$

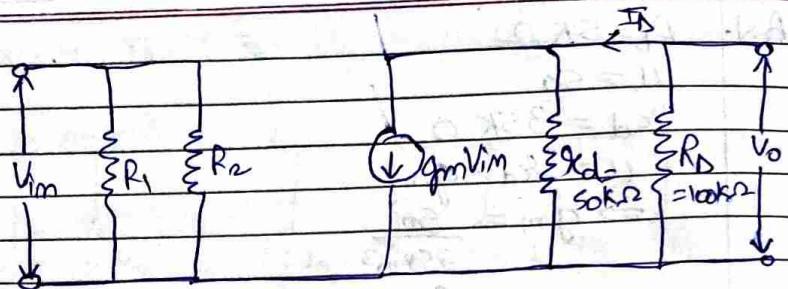
$$R_o = 4.375 k\Omega$$

Q2. For the JFET amplifier shown in figure  $u=100$ ,  $r_d = 50k\Omega$



- (a) Draw the equivalent circuit  
(b) Find the voltage gain of the amplifier.

Ans 2(a)



Ans 2(b)

$$A = \mu = g_d \times g_m$$

$$g_m = \frac{1}{2} \frac{1}{R_D} \frac{1}{k_B T}$$

$$g_m = 2 \times 10^{-3} S$$

$$A_V = -g_m (R_D \parallel R_L) \\ = -2 \times 10^3 \left[ \frac{500 \Omega \times 10 \Omega}{150 \Omega} \right]$$

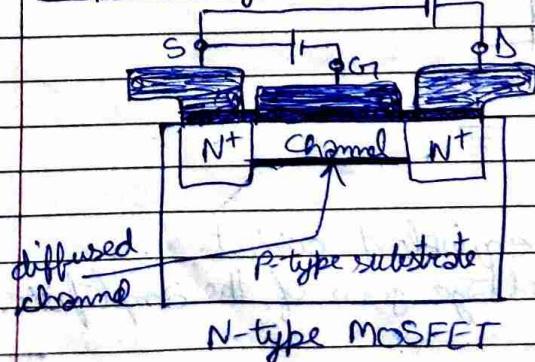
$$A_V = -66.67$$

### Types of MOSFET:

1. Depletion Type MOSFET : (channel is created)
2. Enhancement Type MOSFET : (channel is not created)

22-10-19

### Depletion Type MOSFET:

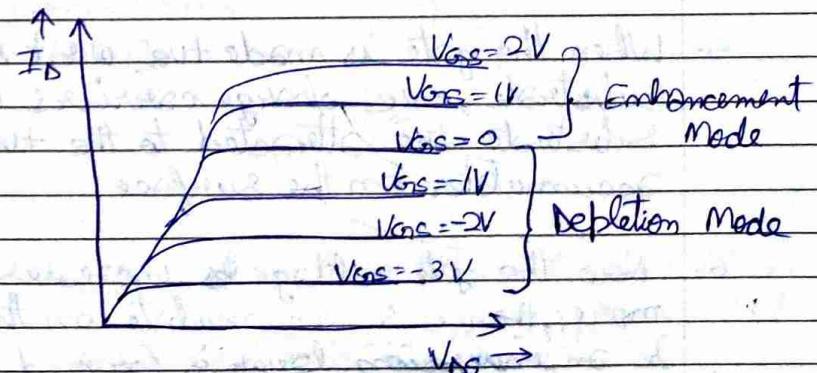


### Operation:

1. When drain is +ve w.r.t source, a drain current will flow.
2. ~~With this biasing~~ The drain current will flow with 0 gate potential.
3. When gate is -ve w.r.t source or substrate, the gate terminal repels the -ve charge carriers out of the N-channel. It creates a depletion region in the channel as shown in figure & hence increases the channel resistance & reduces the drain current.

### Drain characteristics:

Graph b/w  $V_{DS}$  &  $I_D$  when  $V_G$  is constant.



### Enhancement Type MOSFET:

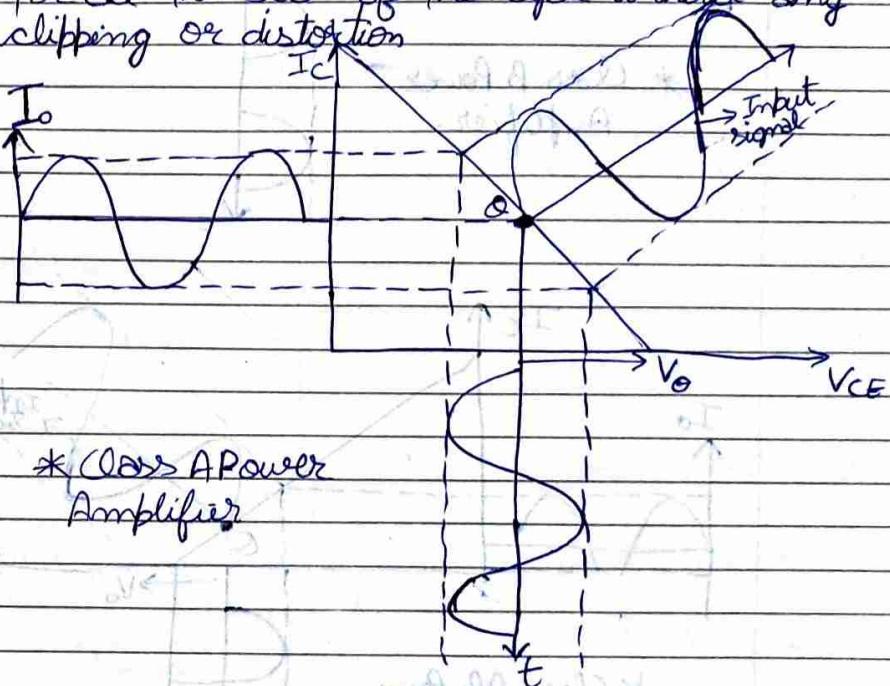
The biasing of drain terminal is +ve w.r.t source & the biasing of gate terminal is also +ve w.r.t source. (Same fig. as N-I-T MOSFET except gate is +ve)

### Operations:

1. In enhancement mode channel is not created between drain to source, hence it doesn't conduct with  $V_{GS} = 0$ .
2. It requires large +ve gate voltage.
3. When drain is +ve w.r.t source, & no gate voltage is applied, then 2 N-regions & 1 P-substrate forms two p-n junctions connected back to back.
4. No 2 p-n junctions can be forward biased at the same time, hence there is only small drain current will flow approximately about the order of micro ampere. It is approximately equal to leakage current.
5. When the gate is made +ve w.r.t source & substrate, -ve charge carriers within the substrate are attracted to the +ve gate & accumulates on the surface.
6. Now the gate voltage increases more & more, then e-s accumulate on the surface & an inversion layer is formed.

- Q1- Write down the classification of a power amplifier. Draw circuit diagram & their characteristics also.

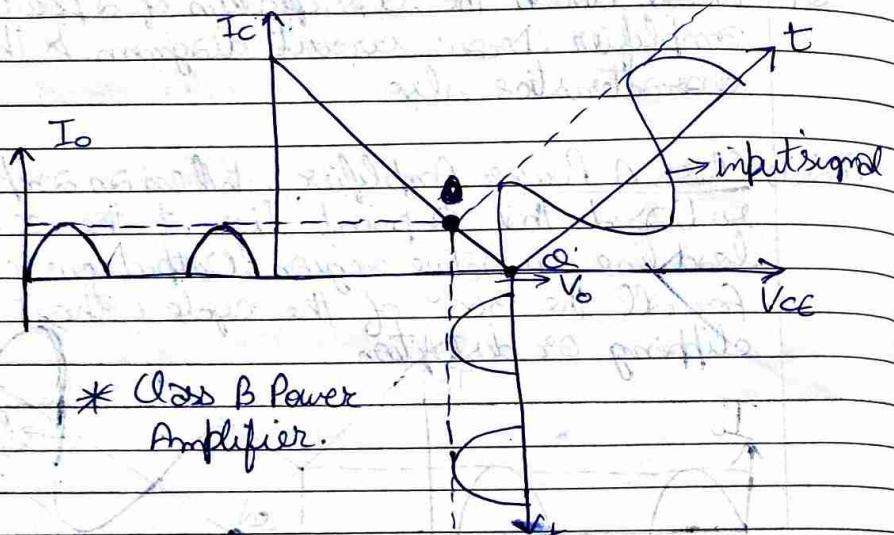
Ans: Class A Power Amplifier: When an amplifier is so biased that O point lies at the centre of load line in active regions. Output current flows for all the  $360^\circ$  of the cycle without any clipping or distortion.



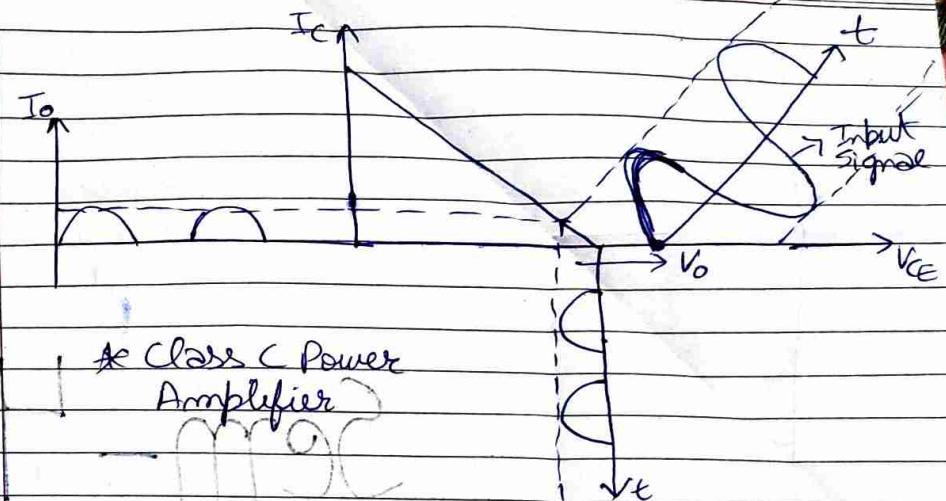
\* Class A Power Amplifier

(ii) Class B Power Amplifier: When O point of an amplifier is fixed at cut off & o/p current flows only for  $180^\circ$  (half cycle).

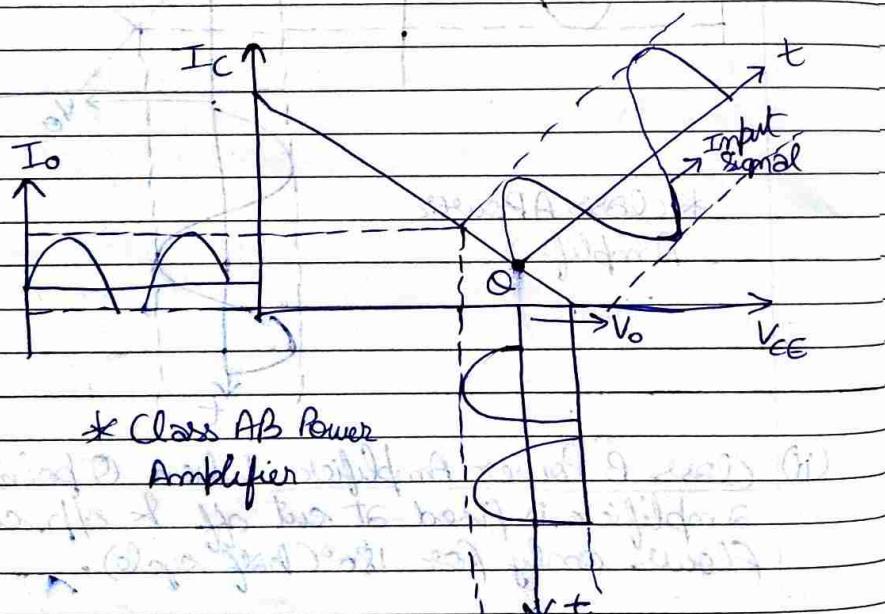
(iii) Class AB Power Amplifier: When O point lies just above the cut off on the load line but below the centre point of the load line. Output current flows more than  $180^\circ$  & less than  $360^\circ$ .



\* Class B Power Amplifier.



\* Class C Power Amplifier



\* Class AB Power Amplifier

\* Advantage of using Class B amplifier over Class A:

1. In Class B operation the transistor is so biased that zero signal collector current is zero. Hence Class B operation does not need any biasing system.

\* Push-Pull Amplifier: Push-Pull Amplifier makes use of 2 identical transistors in a single stage. It consists of 2 loops in which the transistor collector current flows in opposite direction but add in the load.

(iv) Class C Power Amplifier: When the Q point is fixed below the cut off point then some positive part is lost and q/p current flows only for less than  $180^\circ$ .