The output characteristics are plotted between emitter current I_E and collector-emitter voltage V_{CE}. The common collector gain characteristics are plotted between emitter-current and base current. Fig. 5.30 depicts the output and current gain characteristics.

The common collector (CC) arrangement gives very high input impedance and very low output impedance and, therefore, its voltage gain is always less than unity. Hence this configuration is seldom used for amplification. However, owing to relatively high input impedance and low output impedance, this configuration is primarily used for impedance matching *i.e.* for driving low impedance from a high impedance source. This configuration is also called *emitter follower.*

5.16. COMPARISON OF CHARACTERISTICS OF TRANSISTORS IN DIFFERENT CONFIGURATIONS

The essential characteristics of each of basic configurations are tabulated below :

Configuration / *Characteristics*	*Common Base*	*Common Emitter*	*Common Collector*
Input impedance	Low (about 100 Ω)	Medium (about 800 Ω)	Very high (about 750 kΩ)
Output impedance	Very high (about 500 kΩ)	High (about 50 kΩ)	Low (about 50 Ω)
Current gain	Less than unity but usually more than 0.9 (about 0.98)	High (about 80)	High (about 100)
Voltage gain	About 150	About 500	Less than unity
Leakage current	Very small (5 μA for Ge and 1 μA for Si)	Very large (500 μA for Ge and 20 μA for Si)	Very large
Output Signal phase	In phase with input	Reverse	In phase with input
Applications	For high frequency applications	For AF applications	For impedance matching

5.17. TRANSISTOR AS AN AMPLIFIER

The main utility of a transistor lies in its ability of amplifying weak signals. The weak signal is applied at the input terminals and the amplified output is obtained across the output terminals.

A transistor alone cannot perform the function of amplification and some passive components such as resistors and capacitors and a biasing battery is to be connected. Common emitter (CE) configuration, because of its high current, voltage and power gains, is much suited for most of the amplifier circuits. A common emitter N-P-N transistor amplifier circuit is given in Fig. 5.31.

The weak signal is applied between emitter-base junction and output is taken across a load resistor R_L connected in series with collector supply voltage V_{CC} (Fig. 5.31). In order to obtain faithful amplification, it is necessary that the input circuit remains always forward biased regardless the polarity of the ac input signal. So a battery V_{BB} is inserted in the circuit with the polarity indicated in addition to the signal voltage. This dc voltage is called the *bias voltage* and its magnitude is such as to keep the input circuit always forward biased regardless the polarity of the input signal.

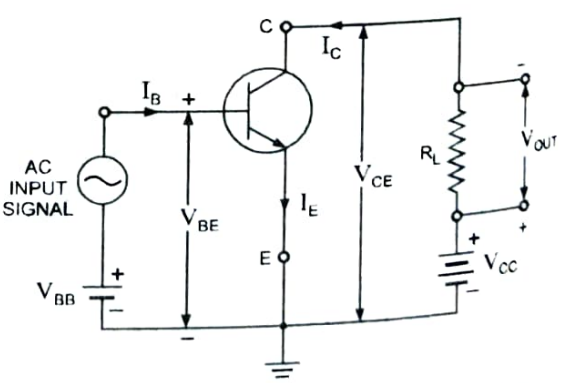

Fig. 5.31. ***Common Emitter NPN Transistor Amplifier Circuit***

The input circuit being forward biased has low resistance and a small change ΔV_{in} in input signal voltage

causes a relatively large change ΔI_E in emitter current. This causes almost the same change in collector current because of transistor action. The collector current flowing through a high load resistance R_L develops a large voltage across it. The change in output voltage across load resistance R_L may be many times the change in input signal voltage. Thus voltage amplification $A = \frac{\Delta V_{out}}{\Delta V_{in}}$ will be greater than unity, and the transistor acts as an amplifier. This is further illustrated below by considering typical circuit values.

Let the load resistance R_L be of 10 kΩ and a change of 0.1 V in input signal voltage cause a change of 0.5 mA in emitter current. This change of 0.5 mA in emitter current will also change collector current I_C by approximately 0.5 mA. This change of 0.5 mA in collector current will produce a change of $0.5 \times 10^{-3} \times 10 \times 10^3$ *i.e.* 5 V in output voltage appearing across the load resistor R_L of 10 kΩ. Thus the change of 0.1 V in input signal voltage causes a change of 5 V in the output voltage giving a voltage amplification of $\frac{5}{0.1} = 50$.

Necessity of Biasing. For most of the applications, transistors are required to operate as *linear amplifiers* (*i.e.* to amplify output voltage as a linear function of the input voltage). To achieve this, it is necessary to operate the transistor over region of its characteristic curves which are linear, parallel and equi-spaced for equal increments of the parameters. Such an operation can be ensured by proper selection of zero signal operating point and limiting the operation of the transistor over the linear portion of the characteristics. For proper selection of zero signal operating point, proper biasing *i.e.* application of dc voltages at emitter-to-base junction and collector-to-base junction is required.

If the transistor is not biased properly, it would work inefficiently and produce distortion in the output signal.

5.18. TRANSISTOR LOAD LINES

The concept of load line is very important in understanding the working of a transistor. It is defined as the locus of operating point on the output characteristic of the transistor. It is the line on which the operating point moves when ac signal is applied to the transistor.

5.18.1. DC Load Line

In the circuit shown in Fig. 5.31, V_{CC} is the supply voltage to collector, R_C (or R_L) is the collector resistance (or load resistance) and V_{CE} is the collector-to-emitter voltage. Applying Kirchhoff's second law to the output or collector circuit we have,

$$V_{CC} = V_{CE} + I_C R_C \qquad ...(5.38)$$

$$\text{or} \quad I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\text{or} \quad I_C = \frac{-V_{CE}}{R_C} + \frac{V_{CC}}{R_C} \qquad ...(5.39)$$

This equation is to be plotted on the output characteristic of the transistor, V_{CE} and I_C are variables.

Identify this equation as $y = mx + c$ where $m = \frac{-1}{R_C}$ as the slope of the line and $I_C = \frac{V_{CC}}{R_C}$ as intercept of the line on vertical current axis (Fig. 5.32).

Consider the following two particular situations :

(*i*) When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$ ...saturation point A

(*ii*) When $I_C = 0$, $V_{CE} = V_{CC}$ ...cutoff point B

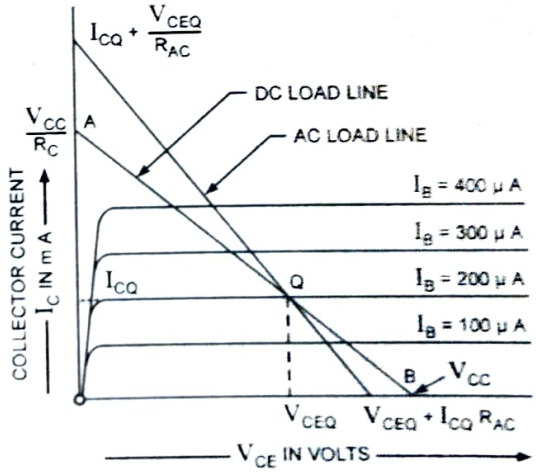

Fig. 5.32. ***Common Emitter Transistor Output Characteristics With DC and AC Load Lines***

By joining these two points A and B, *dc load line* is obtained. The dc load line represents the dynamic characteristic of the device. The dc load line gives the values of collector current I_C and collector-emitter voltage V_{CE} corresponding to zero signal conditions.

5.18.2. Quiescent Point

It is a point on the dc load line which represents dc collector-emitter voltage V_{CE} and collector current I_C in the absence of ac signal. It is also called the *operating point* because the variations in V_{CE} and I_C take place at about this point when signal is applied. The best position for this point is midway between cutoff and saturation points where $V_{CE} = \frac{1}{2} V_{CC}$. Point Q is quiescent point marked on the output characteristics shown in Fig. 5.32. Selection of the operating point is done as per application for which the device is to be used. For example in case of a small signal amplifier, in which power is conserved, operating point is selected so as to give lowest quiescent value of I_C, while for an amplifier operated to deliver small amount of power, operating point is selected so that available quiescent current is about one-half of the maximum permissible collector current I_C.

5.18.3. AC Load Line

When an ac signal is applied, the transistor voltage V_{CE} and collector current I_C vary above and below the quiescent point Q. So point Q is common to both dc and ac load lines. The *ac load line* gives the values of V_{CE} and I_C when an ac signal is applied. For drawing ac load line, take a convenient collector current change ΔI_C and compute the corresponding collector-emitter voltage change $\Delta V_{CE} = -\Delta I_C . R_C$ to obtain another point lying on the ac load line. Now the ac load can be drawn by joining this point and point Q. AC load is steeper than dc load line but the two lines intersect at the quiescent point Q determined by the biasing dc voltages and currents. AC load line takes into account the ac load resistance while the dc load line considers only the dc load resistance.

Example 5.17. In CE configuration (Fig. 5.31) collector supply voltage V_{CC} = 10 V, load resistance R_C is 8 kΩ. Draw dc load line. Determine the operating point Q for zero signal if base current is 15 μA and β is 40.

Solution :

Collector supply voltage, V_{CC} = 10 V
Load resistance, R_C = 8 kΩ
Zero signal base current, I_B = 15 μA
Current gain factor, β = 40

Collector-emitter voltage V_{CE} is given as

$$V_{CE} = V_{CC} - I_C R_C$$

For $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_C} = \frac{10\ V}{8\ k\Omega} = 1.25\ mA$$

This gives point A on the load line.

For $I_C = 0$, $V_{CE} = V_{CC} = 10$ V

This gives point B on the load line. AB is the required dc load line.

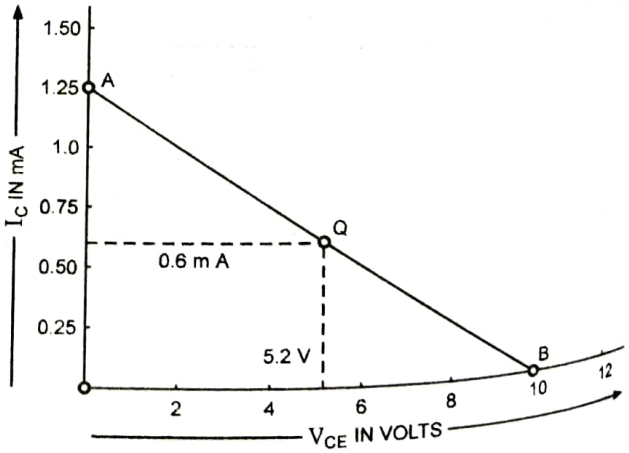

Fig. 5.33

Zero signal collector current,

$$I_C = \beta I_B = 40 \times 15 \times 10^{-6} = 0.6\ mA$$

Zero signal collector-emitter voltage,

$$V_{CE} = V_{CC} - I_C R_C = 10 - 0.6\ mA \times 8\ k\Omega = 5.2\ V$$

∴ Operating point Q is (5.2 V, 0.6 mA) **Ans.**

Example 5.18. Draw the load line for the following figure (Fig. 5.34). What is I_C at saturation point ? Find V_{CE} at cutoff point.

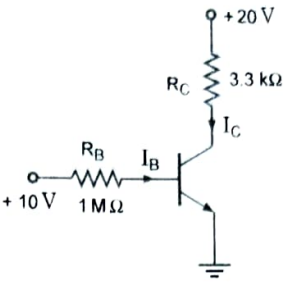

Fig. 5.34

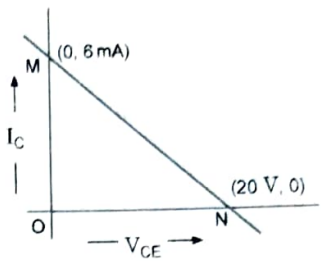

Fig. 5.35

Solution : (*i*) Applying Kirchhoff's voltage law to the output loop we have

$$V_{CC} = I_C R_C + V_{CE}$$

For cutoff point, $I_C = 0$

and, therefore, $V_{CE} = V_{CC}$

$= 20$ V **Ans.**

$\therefore$ For saturation point, $V_{CE} = 0$

$$\text{So } I_C = \frac{V_{CC}}{R_C} = \frac{20}{3.3 \times 10^3} = 6 \text{ mA } \textbf{Ans.}$$

Therefore, load line coordinates are given as (20 V, 0 mA) and (0 V, 6 mA) as shown in Fig. 5.35.

Example 5.19. Determine V_C and V_B for the network given below (Fig. 5.36) with $\beta = 45$ and $V_{BE} = 0.7$ volt.

Solution : $\beta = 45$ and $V_{BE} = 0.7$ volt

Applying Kirchhoff's voltage law in input loop we have

$$I_B R_B + V_{BE} + V_{EE} = 0$$

Putting values in above equation we have

$$I_B \times 100 \times 10^3 + 0.7 - 9 = 0$$

$$\text{or } I_B = \frac{9 - 0.7}{10^5} = 83 \text{ μA}$$

$$I_C = \beta \times I_B = 45 \times 83 \times 10^{-6} \text{ A} = 3.735 \text{ mA}$$

Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 0 - 3.735 \times 10^{-3} \times 1.2 \times 10^3$

$= -4.482$ V **Ans.**

$V_B = V_{BE} + V_{EE} = 0.7 - 9 = -8.3$ volts **Ans.**

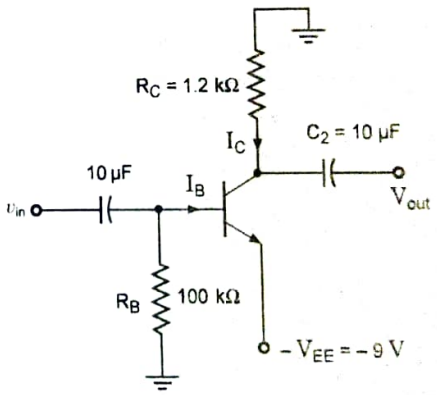

Fig. 5.36

Example 5.20. In the circuit shown in Fig. 5.37, what should be the minimum value of β such that the transistor is in saturation ? Assume $V_{CE\ Sat} = 0.2$ V.

Solution : In the given circuit,

Base current, $I_B = 0.1$ mA

Base resistance, $R_B = 10$ kΩ

Collector resistance, $R_C = 1$ kΩ

Supply voltage, $V_{CC} = 5$ V

Saturation collector-emitter voltage,

$$V_{CE\,(sat)} = 0.2 \text{ V}$$

Applying Kirchhoff's voltage law to the output loop, we have

$$V_{CC} - I_{C\,(sat)} R_C - V_{CE\,(sat)} = 0$$

$$\text{or } I_{C\,(sat)} = \frac{V_{CC} - V_{CE\,(sat)}}{R_C} = \frac{5 - 0.2}{1 \times 10^3} = 4.8 \text{ mA}$$

For transistor to be in saturation

$$\text{Base current, } I_B \geq \frac{I_{C\,(sat)}}{\beta}$$

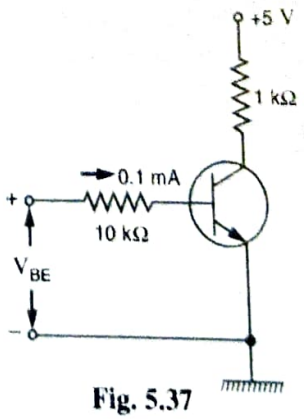

Fig. 5.37

$$\text{or} \quad \beta \geq \frac{I_{C(sat)}}{I_B} \geq \frac{4.8}{0.1} \geq 48$$

Hence, minimum value of $\beta = 48$ **Ans.**

5.19. STANDARD NOTATIONS FOR VOLTAGES AND CURRENTS

Standard notations or symbols are usually used for voltages and currents in transistor circuit analysis and applications.

1. Subscripts E (or *e*), B (or *b*) and C (or *c*) usually refer to emitter, base and collector quantities respectively.
2. Upper case (capital) letters with capital subscripts of the proper electrode symbol are used for dc or average values of voltages and currents.
3. Upper case (capital) letters with lower subscripts of the proper electrode symbol are used for rms values of ac voltages and currents.
4. Lower case (small) letters with lower subscripts of proper electrode symbol are used for instantaneous values of ac voltages and currents.

Notations used for various quantities (voltages and currents) in transistor circuit analysis and applications are given below in tabular form.

S.No.	*Particular*	*DC or average*	*RMS ac*	*Instantaneous ac*
1.	Emitter current	I_E	I_e	i_e
2.	Base current	I_B	I_b	i_b
3.	Collector current	I_C	I_c	i_c
4.	Collector-emitter voltage	V_{CE}	V_{ce}	v_{ce}
5.	Emitter-base voltage	V_{EB}	V_{eb}	v_{eb}
6.	Collector-base voltage	V_{CB}	V_{cb}	v_{cb}
7.	Emitter supply voltage	V_{EE}	—	—
8.	Base supply voltage	V_{BB}	—	—
9.	Collector supply voltage	V_{CC}	—	—
10.	Emitter voltage to ground	V_E	V_e	v_e
11.	Base voltage to ground	V_B	V_b	v_b
12.	Collector voltage to ground	V_C	V_c	v_c