UNIT-II:

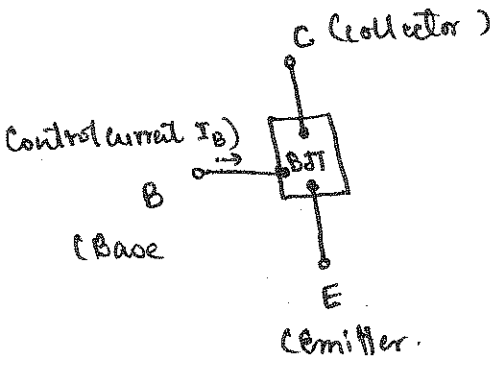
MOSFET Circuit:

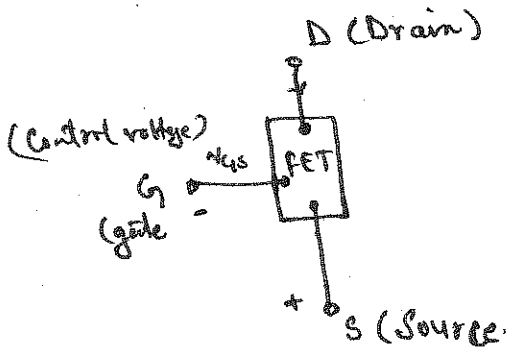
→ Metal oxide Semiconductor field effect transistor

Limitation of BJT:

1. It has low input impedance because of forward biased emitter-base junction.
2. It has considerable noise level.

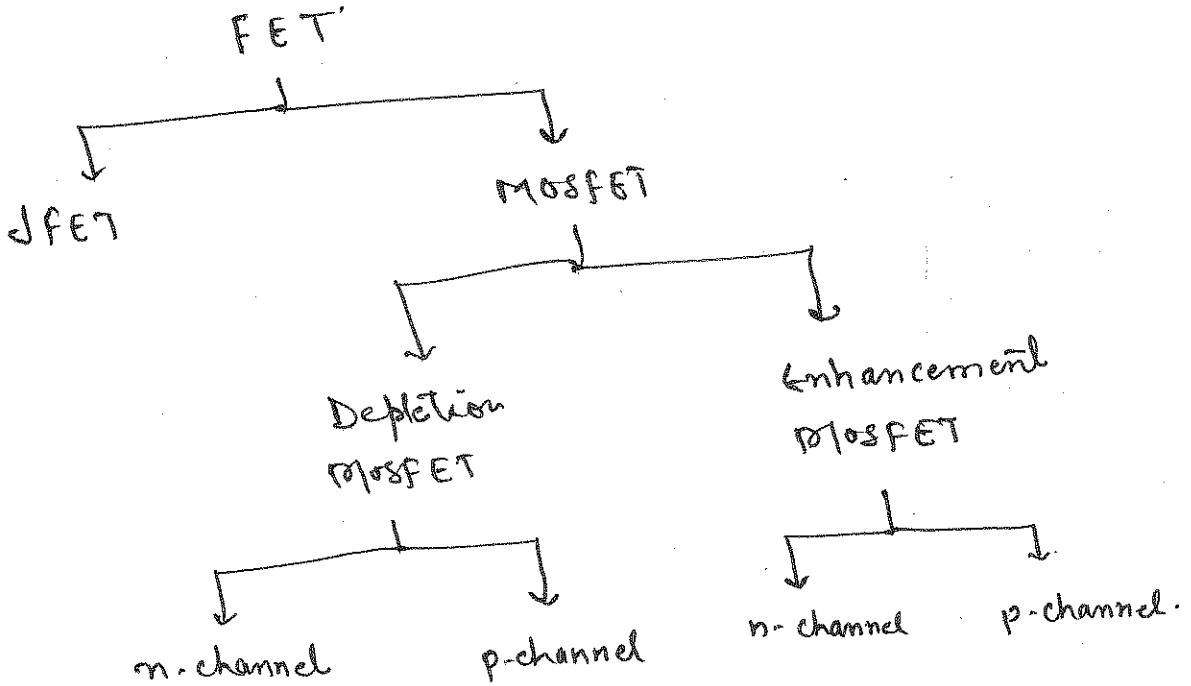
BJT	FET
→ Current-controlled device i.e I_B controls the output current I_C	→ It is a three-terminal, voltage-controlled semi-conductor device in which current conduction is due to the flow of only one of the two kinds of charge carriers i.e electron or holes. i.e input V_{GS} controls the output current I_D.
→ Three terminal collector, Base, Emitter	→ Three terminal Drain (D) Source (S) gate (G)
	→ FET can perform better amplification and switching operation.
→ Current conduction is due to both $\bar{e}$ and holes. So bipolar transistor.	→ Current conduction is due to only one of the two type charge carriers. $\bar{e}$ or hole. So FET is called Unipolar transistor.





→ The operation of the device depends on electric field intensity in the channel
→ High o/p resistance
→ Power dissipation is small
→ Majority carrier device
→ No minority carriers.
→ No leakage current and ∴ temperature effect on the device is very less and ∴ excellent thermal stability.
→ FET is small in size and easy to fabricate.

Disadvantage:
→ Small gain
→ Smaller gain bandwidth product.



Regions of FET:-

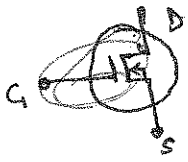
Source: It is the source of majority carrier. i.e. It is the terminal by which majority carrier will be entering into device.

Drain: It drains the majority carrier. It is the terminal by which majority carrier will be leaving the device.

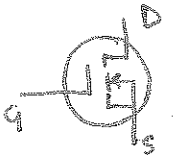
gate: It is the terminal which control majority carriers moving from source to drain.

Channel: It is the region b/w two gates.

...ship of MOSFETs



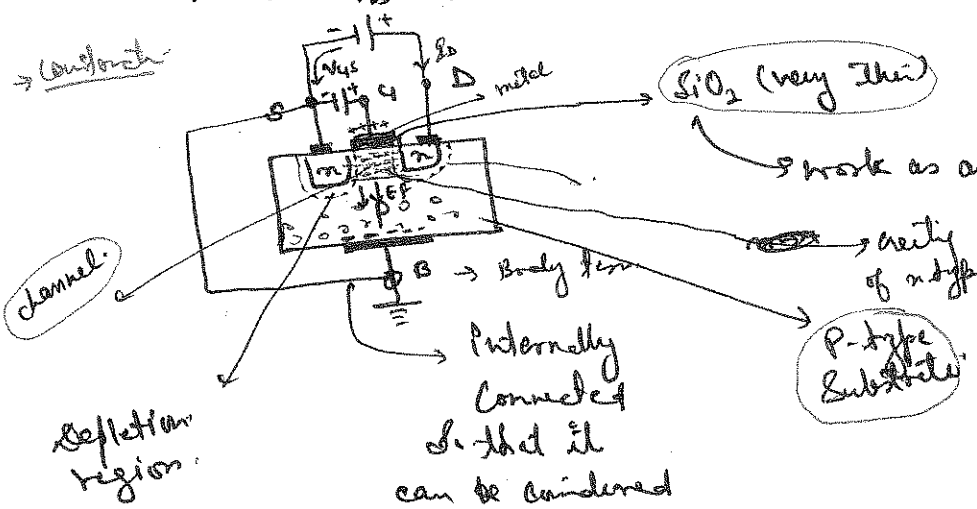
Symbol.



n-channel E MOSFET

n-channel Enhancement MOSFET.

→ take p-type substrate body and diffuse two n-type semiconductor as in fig.



V_{GS} & I_D.
to generate current I_D.

creating thin layer of n-type

E-F (+ to -ve)

I_D → how I_D is created?

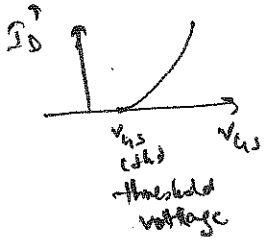
Current flows from drain to source:

V_{GS} → +ve

→ Depletion region
n → +ve (high potential) } Reverse Bias.
P → low potential)

↓
So depletion region ↑es. means. charges can't flow from drain to source.
↓
i.e. Application of a battery b/w Drain and Source no current flows. So next is to attached a battery b/w gate & source.

- V_{DS} → no current ($I_D = 0$)
- $V_{GS} = 0$, no channel connecting Source & drain i.e $I_D = 0$ (EMOSFET generally OFF)



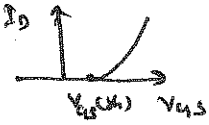
Capacitor

collects charge. → restrict flow of charge.
If a dielectric is place (insulator)

→ V_{GS} Induced n-channel.

→ characteristics → Transfer characteristics
→ Drain characteristics.

Transfer characteristics:
It is the plot b/w drain current (I_D) and gate-source voltage.



- If $V_{GS} < V_{GS(th)}$, there is no induced channel and $I_D = 0$.
- $V_{GS} = V_{GS(th)}$
  EMOSFET → ON and induced channel
- $V_{GS} > V_{GS(th)}$
  width of induced channel increases hence I_D ↑es.

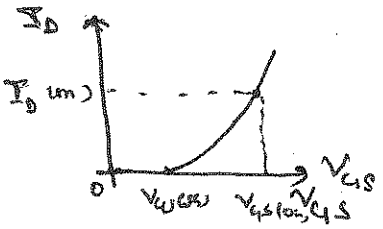
Eqⁿ for transconductance:

↳ o/p. (current / voltage)

for $V_{GS} > V_{GS(th)}$

$$I_D = K (V_{GS} - V_{GS(th)})^2$$

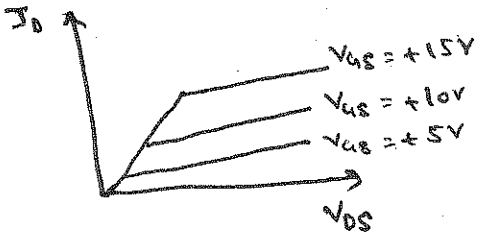
$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$



* Drain characteristics:

The drain characteristics is the graph b/w drain current (I_D) and drain-source voltage (V_{DS}).

From the graph, it can be seen that most of the part of the curve is horizontal, showing constant drain current. Hence in this part of curve the EMOSFET behaves as a constant current source.



Q. The data sheet for an E-MOSFET gives $I_{D(on)} = 500mA$ at $V_{GS} = 10V$ and $V_{GS(th)} = 1V$. Determine the drain current for $V_{GS} = 5V$.

Here $V_{GS(on)} = 10V$

$$I_D = K(V_{GS} - V_{GS(th)})^2 \rightarrow (1)$$

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2} = \frac{500\,mA}{(10V - 1V)^2} = 6.17\,mA/V^2$$

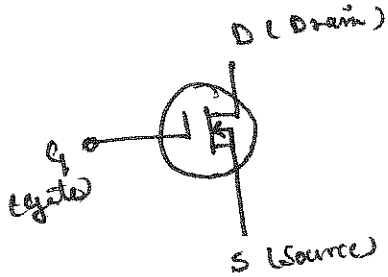
put values in Eqⁿ (1)

$$I_D = 6.17 (5V - 1V)^2$$

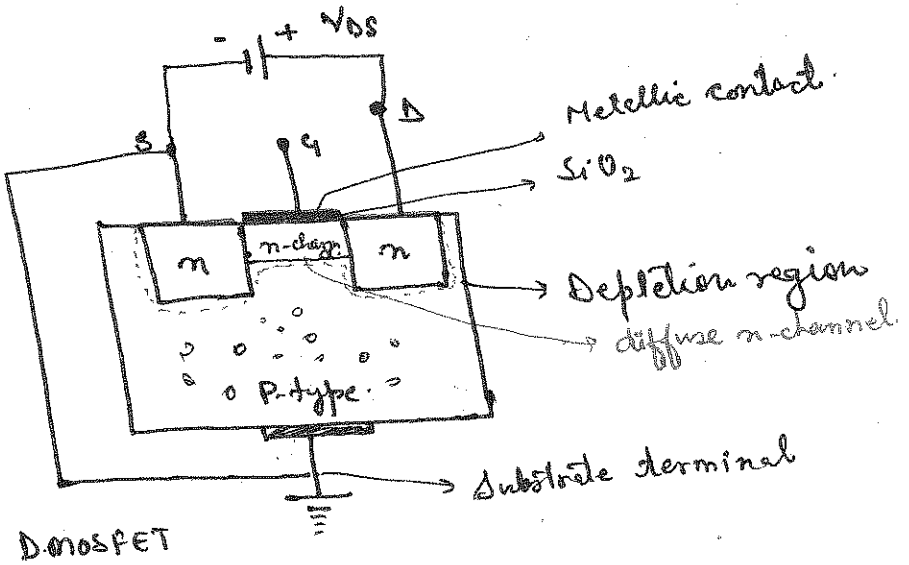
$$\boxed{I_D = 98.7mA.}$$

n-channel Depletion MOSFET:

Symbol:



Construction/working:



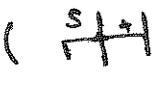
3-ways to operate: DMOSFET

1. i) $V_{GS} = 0$ (I_{D_1})

$V_{DS} \rightarrow +V \longrightarrow I_D$ flows.

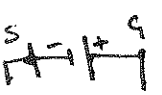
as V_{DS} ↑es I_D ↑es, at certain point ↑ing V_{DS} I_D doesn't change i.e I_D becomes constant.

∵ of the reverse biasing depletion region becomes wider and wider. and channel becomes thinner

ii) $V_{GS} = -ve$ (I_{D_2}) ()

In this case. The -ve terminal at the gate pushes $\bar{e}$ towards the substrate p. where the $\bar{e}$ recombines $\bar{c}$ the holes. which results in thinner diffuse channel i.e I_D ↓es.

$\Rightarrow V_{GS} \rightarrow -ve \Rightarrow I_D$ ↓es.

iii) $V_{GS} = +ve$ () (I_{D_3})

In this case. the +ve terminal at gate attracts the $\bar{e}$, resulting in thicker diffuse channel.

$V_{GS} = +ve \Rightarrow I_D$ ↑es

Conclusion:- $\Rightarrow I_{D_2} > I_{D_1} > I_{D_3}$

Q. For a certain D-MOSFET, $I_{DSS} = 10\,mA$ and $V_{GS(off)} = -8V$

i) Is this an n-channel or a p-channel

ii) Calculate I_D at $V_{GS} = -3V$.

iii) " " " $V_{GS} = +3V$.

i) The device has a negative $V_{GS(off)}$ ∴ n-channel D MOSFET.

ii) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 10\,mA\left(1 - \frac{-3}{-8}\right)^2 = 3.91\,mA$$

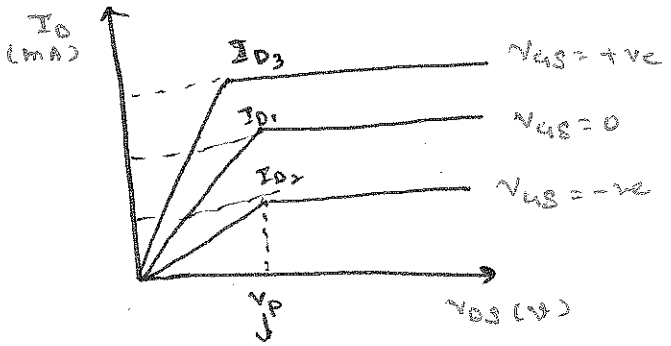
iii) $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 10\,mA\left(1 - \frac{+3V}{-8V}\right)^2 = 18.9\,mA.$$

MOSFET characteristics:

- Transfer char.
- Drain charac.

i) Drain characteristics: (I_D Vs V_{DS})

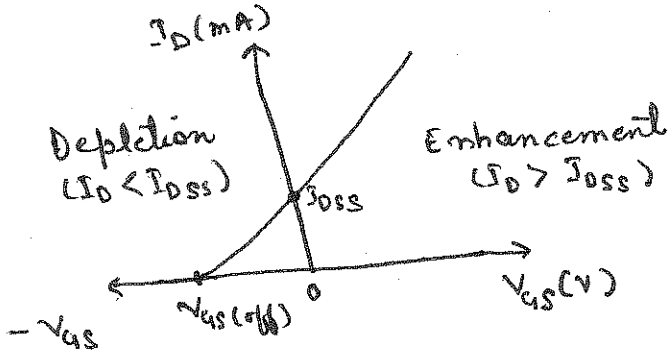


$I_{D_3} > I_{D_1} > I_{D_2}$

Pinch off voltage.

It is the minimum drain-source voltage at which the drain current becomes constant.

ii) Transfer characteristics: (I_D Vs V_{GS}).



i) $V_{GS} = 0$, $I_D = I_{DSS}$

i.e I_{DSS} is the value of I_D when gate and source terminal are shorted. i.e $V_{GS} = 0$

ii) $V_{GS} \to -ve$.
When V_{GS} is -ve, I_D ves below the value of I_{DSS} till I_D reaches zero i.e $V_{GS} = V_{GS(off)}$.

iii) $V_{GS} \to +ve$
When V_{GS} is +ve, I_D ves above the value of I_{DSS}.

Transfer Drain Current:

control variable (input voltage)

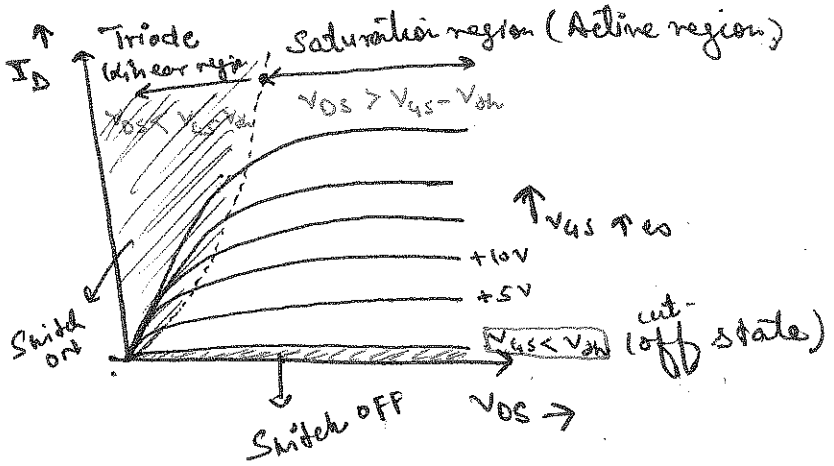
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$ → Shockley's Eq^n.

I_D ↙ output current

I_{DSS} → constant

MOSFET as a Switch:

Drain characteristics of E-MOSFET: (I_D vs V_{DS}) for a given V_{GS}



→ Cut-off Region ($V_{GS} < V_{th}$)

In this region, the MOSFET is in OFF state, as there is no induced channel b/w drain & Source

→ In both Linear and Saturation region, the MOSFET is in ON state. difference is that in Linear region, the channel is continuous and I_D α to the resistance of the channel.

→ In Saturation region, as $V_{DS} > V_{GS} - V_{th}$, the channel pinch off. i.e broadens resulting in a constant drain current i.e I_D.

To understand the operation of a MOSFET as a Switch, we consider the simple circuit as fig. 1.

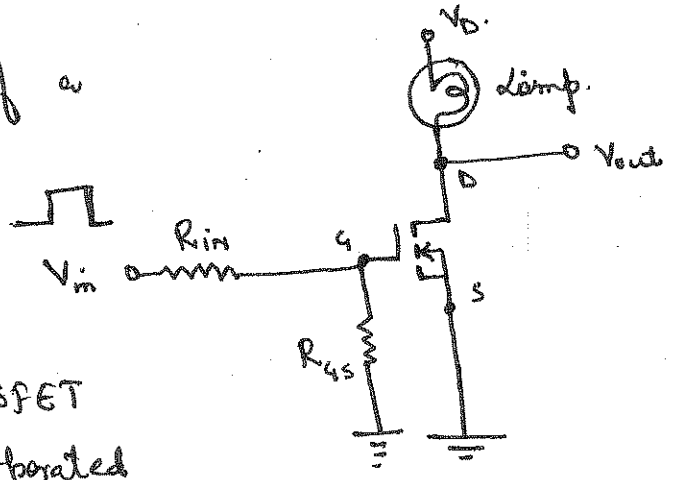


Fig. 1.

→ In order to operate a MOSFET as a Switch, it must be operated in Cut-off and linear region.

- Assume the device is initially OFF.

i) $V_{GS} > V_{th}$ (Switch ON).

V_{GS} is made positive, the MOSFET enters in the linear region and the Switch is ON. This makes the light to turn ON.

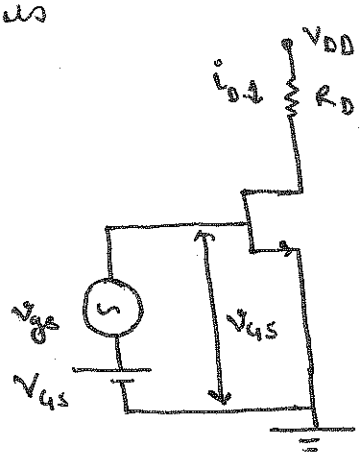
ii) $V_{GS} < V_{th}$ (or = 0). (Switch off):

If the input V_{GS} is 0 or $< V_{th}$, the MOSFET enters in cut-off state and turns OFF. This in turn will make the light to

Small Signal operating model of MOSFET:

To main purpose of Small signal is to find the ac current and ac voltage.

So let us consider a circuit which consist of both ac and dc source.



Voltages: (3-Types)

v_{gs} → ac voltage

V_{GS} → DC voltage

v_{GS} → $v_{gs} + V_{GS}$ → (1)

↑ Total voltage

Similarly Current:

i_d → ac current

I_D → dc current

i_D → total current

$i_D = i_d + I_D$ → (2)

i_D Current is:

Now:

$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2 \rightarrow (3)$$

(k_n: constant; V_t: threshold voltage; $\frac{W}{L}$: transistor aspect ratio i.e. width/length)

i.e. (in Saturation region)

So,

$$i_D = \frac{1}{2} k_n \frac{W}{L} (v_{GS} - V_t)^2$$

(v_{GS}: total voltage; i_D: total current)

$$= \frac{1}{2} k_n \frac{W}{L} ((v_{gs} + V_{GS}) - V_t)^2 \quad \text{or} \quad \frac{1}{2} k_n \frac{W}{L} ((V_{GS} + v_{gs}) - V_t)^2 \rightarrow (4)$$

$$(a+b-c)^2 = a^2 + b^2 + c^2 + 2ab - 2bc - 2ca$$

$$i_D = \frac{1}{2} k_n \frac{W}{L} \left[V_{GS}^2 + v_{gs}^2 + V_t^2 + 2 V_{GS} \cdot v_{gs} - 2 v_{gs} V_t - 2 V_t V_{GS} \right]$$

Considering the ac component,

$$i_d = \frac{1}{2} k_n \frac{W}{L} \left[2 V_{GS} \cdot v_{gs} - 2 v_{gs} V_t \right]$$

$$i_d = \frac{1}{2} k_n \frac{W}{L} \left[2 v_{gs} (V_{GS} - V_t) \right]$$

$$\boxed{i_d = k_n \frac{W}{L} \left[v_{gs} (V_{GS} - V_t) \right]}$$

i_d ac current in a small signal of MOSFET

* Trans Conductance: (g_m)

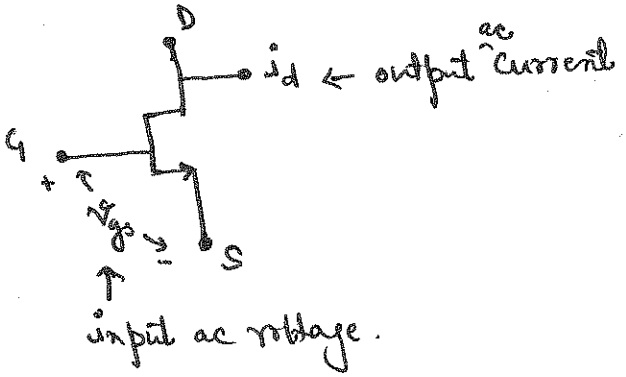
Trans → $\frac{o/p}{i/p}$

Conductance → current/voltage.

So

trans conductance (g_m) = i_d / v_{gs}.

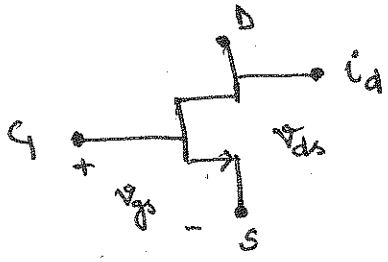
$$\therefore \boxed{g_m = \frac{i_d}{v_{gs}}}$$



for small signal $i_d = k_n \frac{W}{L} \left[v_{gs} (V_{GS} - V_t) \right]$

$$\therefore \boxed{g_m = k_n \frac{W}{L} \left[V_{GS} - V_t \right]}$$

Voltage gain: (A_v)



Voltage gain = $\frac{\text{output voltage}}{\text{input voltage}}$

$$A_v = \frac{v_{ds}}{v_{gs}}$$

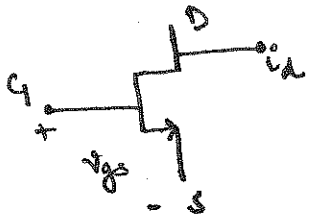
$$A_v = \frac{i_d \cdot R_D}{v_{gs}}$$

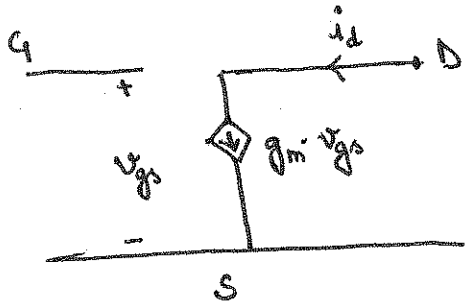
$$\boxed{A_v = g_m \cdot R_D}$$

voltage gain

Small Signal Equivalent Model:-

MOSFET



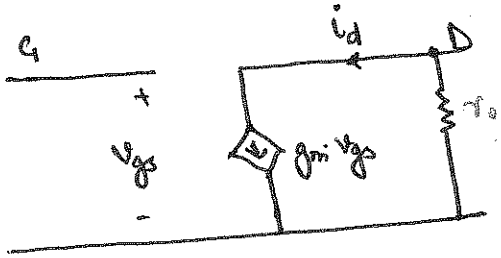


$i_d = g_m \cdot v_{gs}$

$g_m = i_d / v_{gs}$

$A_v = g_m \cdot R_D$

Without internal Resistance r_o



$r_o = \frac{v_o}{i_d}$

$A_v = g_m \cdot (R_D \| r_o)$

With internal resistance r_o

Procedure for Small Signal Model:

i) Consider 3 terminals G, D, S.

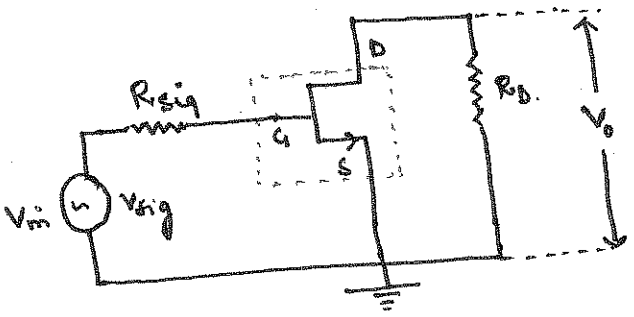
ii) There is no Connection b/w Gate and Source and there is no Current (input) flowing b/w Gate and Source.

iii) But there is a Current flow b/w Drain and Source terminals. that is the constant current. why ? in the saturation region current is constant, so we can represent it with constant small signal current Source $g_m v_{gs}$ i.e i_d.
↳ ac. current.

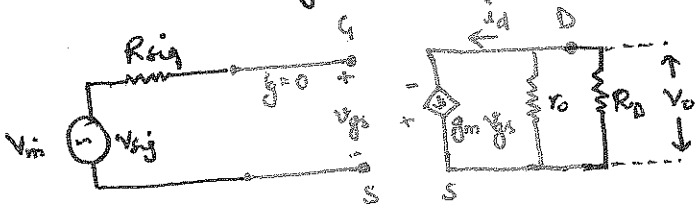
MOSFET Amplifier Configurations:-

• (A)

i) Common Source Configuration :- → Without R_S
→ With R_S :



is Small Signal model:



ii Input resistance: (R_{in})

$$\boxed{R_{in} = R_{sig} = \infty}$$

Any Configuration with gate (G) as input have $R_{in}=\infty$, ∵ i_g current is zero.

$$\because R = \frac{v}{i} = \frac{V}{0} = \infty$$

iii Output resistance (R_{out}):

$$R_{out} = r_o \parallel R_D$$

$$r_o >> R_D$$

$$R_{out} = \frac{r_o R_D}{r_o + R_D}$$

$$= \frac{r_o R_D}{r_o}$$

$$\boxed{R_{out} = R_D}$$

iv Voltage Gain (A_v):

$$A_v = \frac{V_o}{V_i}$$

$$= \frac{-i_d (R_D \parallel r_o)}{V_{gs}}$$

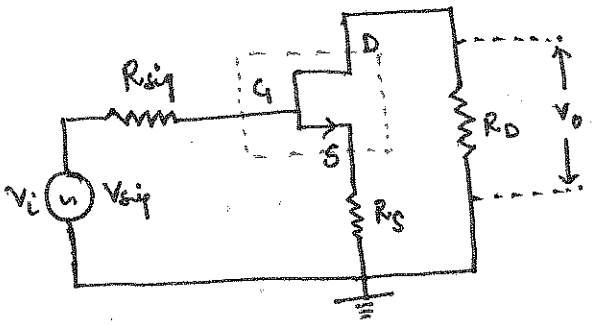
$$\boxed{A_v = -g_m (R_D \parallel r_o)} \quad (\because i_d/V_{gs} = g_m)$$

Overall gain :- (G_v)

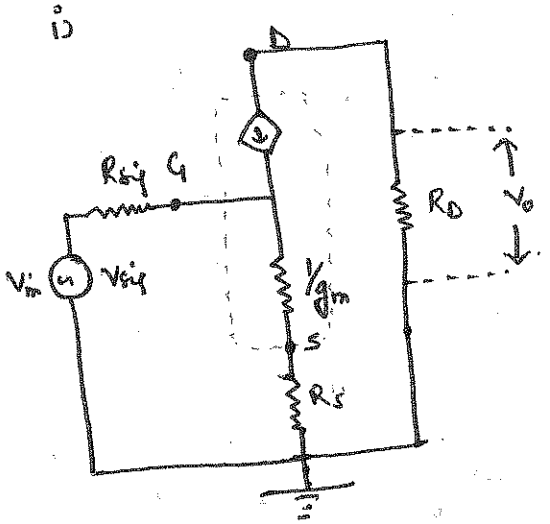
$$G_v = \frac{V_o}{V_{sig}} = \frac{V_o}{V_{in}} = \frac{-i_d (R_D \parallel r_o)}{V_{gs}} = -g_m (R_D \parallel r_o)$$

; $\boxed{G_v = -g_m (R_D \parallel r_o)}$

Common Source Configuration: (with R_S)



i)



ii) Input resistance: (R_{in})

$$\boxed{R_{in} = R_{sig} = \infty}$$

iii) output resistance: (R_o):

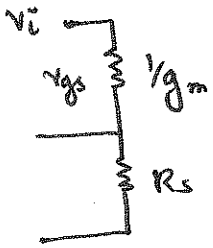
$$\boxed{R_o = R_D}$$

iv) Voltage gain (A_v):

$$A_v = \frac{V_o}{V_i}$$

$$A_v = -i_d R_D$$

To get v_{input} consider the input part: as



$$v_{gs} = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} \cdot v_i$$

We have used voltage divider formula, which states that resistance in that branch divided by the sum of the resistance multiplied with source voltage.

$$v_{gs} = \frac{1}{1 + g_m R_S} \cdot V_i$$

$$V_i = v_{gs}(1 + g_m R_S).$$

Conclusion / Remarks:

→ The CS amplifiers has infinite input impedance and a moderately high output resistance, and a high voltage gain

→ Reducing R_D reduces the output resistances of a CS amplifier - but unfortunately, the voltage gain is also reduced. Alternate design can be employed to reduce the output resistance.

→ A CS amplifier suffers from poor high frequency performances as most transistor amplifiers do.

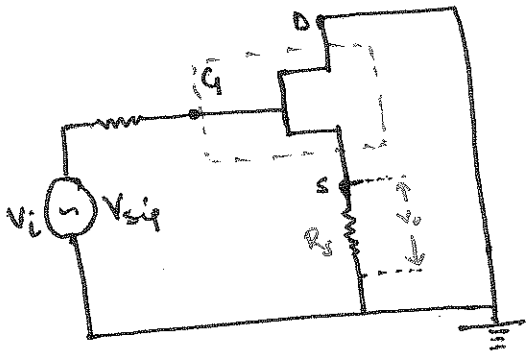
$$A_v = \frac{-i_d \cdot R_D}{V_{gs}(1+g_m R_s)}$$

$$\boxed{A_v = \frac{-g_m R_D}{(1+g_m R_s)}} \quad \left(\text{as } \frac{i_d}{V_{gs}} = g_m\right)$$

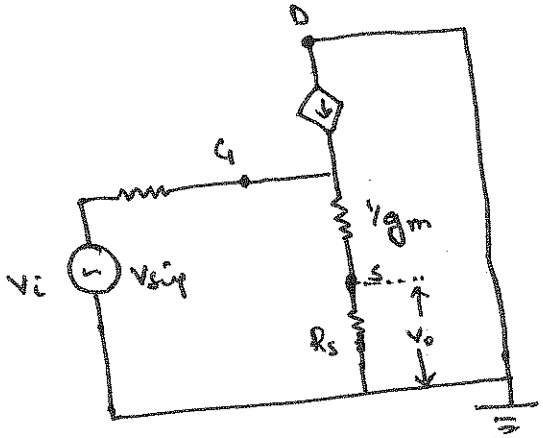
② Common drain Configuration :-

In Common drain Configuration the drain terminal is common between input and output. So Drain terminal connected to ground Source as output and Gate as input.

* If there is a resistance connected to Source terminal, then hybrid T-model is considered for the MOSFET.



is



i) Input resistance: R_{in}

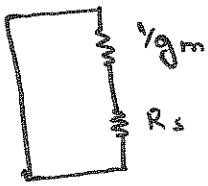
$$\boxed{R_{in} = R_{sig} = \infty} \quad i_g = 0$$

ii) output resistance: R_o

$$R_o = \frac{1}{g_m} \parallel R_s$$

$\because R_s >>> \frac{1}{g_m}$

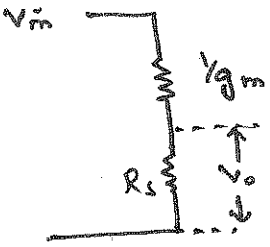
$$\boxed{R_o \simeq \frac{1}{g_m}} \quad \left(R_o = \frac{\frac{1}{g_m} \cdot R_s}{\frac{1}{g_m} + R_s}\right)$$



($V_{in} = 0$

Voltage gain (A_v):

Considering the output part.



using the voltage divider formula

$$V_o = \frac{R_s}{R_s + \frac{1}{g_m}} \cdot V_i$$

$$A_v = \frac{\frac{R_s}{R_s + \frac{1}{g_m}} \cdot V_i}{V_i} \quad \left(\text{as } A_v = \frac{V_o}{V_{in}}\right)$$

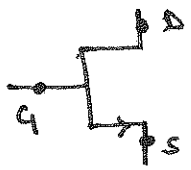
$$\therefore \boxed{A_v = \frac{R_s}{R_s + \frac{1}{g_m}}}$$

Total/overall gain: G_v

$$G_v = \frac{V_o}{V_i}$$

$$\boxed{G_v = \frac{R_s}{R_s + \frac{1}{g_m}}}$$

FET Amplifier Configuration:

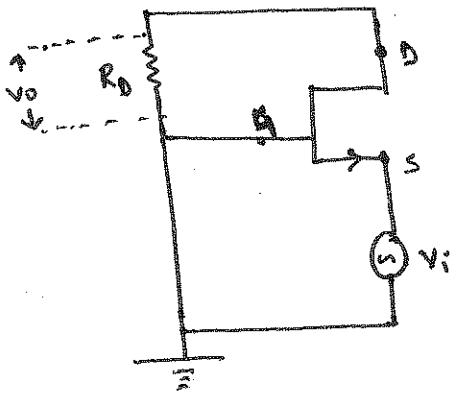


↳ i) Common Source
ii) Common Gate
iii) Common drain

Concept:

Configuration	G	S	D
CS	i/p	GND	o/p
CG	GND	i/p	o/p
CD	i/p	o/p	GND

In general
G → i/p.
D → o/p.



Steps:

i) Amplifier circuit is converted to Small Signal model
ii) Get expression from R_{in}, R_o.
iii) Get gain, A_v, V_i, V_o.