

Project: OROBOROS (snake eating own tail)

- python makes it easy to see byte code
  - use `dis` (for disassembly)

- `def foo(n):`  
    `return 42`      may think: if I see `foo`, just replace w/ 42

But Can't!

it's a very dynamic language

- best effort approach: try to write compiler optimizations not to find everyone, but to find some w/out destroying everything
- other dynamics: can change operators (can't change what `+` does, `-` does, etc)
  - C++ called operator overloading
- IR = low level representation (usually looks like control flow graph)
  - may want to do `src`  $\rightarrow$  `AST`  $\rightarrow$  `IR`, but actually want hybrid
  - widely used IR: static single assignment (SSA)
    - $\hookrightarrow$  introduce new variables (`x`  $\rightarrow$  `x-prime`)
    - $\hookrightarrow$  <sup>essentially</sup> turning imperative lang into functional
    - $\phi$  nodes: too complicated to explain :)
- we will build a `src-to-src` compiler

python code  $\rightarrow$  do something  $\rightarrow$  python code

- visitor pattern:

`ast-FunctionDef` (      )

- have a class, by default does nothing for nodes
- then have a class that's special, visitor visits it
- we have to use to process ASTs (or could write function that walks the tree)
- 1<sup>st</sup> step: write simple visitors just to get feel for code (start small + get accustomed to this way of programming)
- straight forward sounding but lots of gotchas!
- +100 tests by Juan - so make / share 100 of tests

Last time talked about CISC v RISC, etc;

terms used in literature:

- superscalar architectures: multiple execution units
- super pipelining: multiple ins in exec execution; Fetch, decod, execute

## FDIV Bug

- divide float in certain range w/ another float in another range (substantial error)

unit pipeline as full as possible or get bubbles  
emptying pipeline = flushing

asynchronous

- error baked into chip!
- there are known errors in processors all the time, but not this bad
- led to recall of intel processor
- led to verification

32 bits / 32 bits  $\rightarrow$  need  $2^{64}$  tests

(1 bit / 1 bit  $\rightarrow$  4 tests)

64 / 64  $\rightarrow$  need  $2^{128}$  tests

side note:  
earth will be swallowed by sun ahhh

exhaustive testing doesn't work for large state space

- Formal verification (prove w/ math)
  - some dudes PhD dissertation
- model checking: inbetween formal ver + exh testing
  - automatic testing up to size n
  - collapses a bunch of "identical" states
  - standard approach

"Testing can only reveal the presence of bugs but not their absence!"

- justify formal verification
- but not exactly true
- what does Tictok do? what is formal spec? hard to specify things so formal verification is hard
- what does it mean to be correct?
  - correct w/ respect to its specs
  - is the spec correct?
  - is the meta spec correct?



- qSort:

- needs to terminate
- if multiset input  $\rightarrow$  output sequence

$\forall i, j : i \leq j : \text{output}[i] \leq \text{output}[j]$

$i \geq 0$   
 $i < n$   
 $j \geq 0$   
 $j < n$

if tried to prove  
 about all to  
 left, it would  
 fail

Fairly simple spec

what if strings? what  
 does  $\leq$  mean? what is  
 empty string? lower v. upper?  
 spec becomes long  
 once spec is long, it's  
 an "identical prog" that's  
 hard to read

Berger's Opinion:  
 why not high-level PL?  
 - enrich w/  
 - post/pre conditions  
 - invariants

No oracle! No truth!  
 specs could be wrong

The Spec Problem  
 (spec not useful -  
 not "clearly" correct)

total correctness:  $\text{prog} = \text{spec}$   
 partial correctness: prog properties  
 are subset of spec  
 (ex: prog never % by 0)

The Oracle Problem  
 (where's the truth)

Intel + HP  
 org name: VLIW  
 very long instr word

explicitly parallel instruction computing (EPIC)

VLIW:  
 ADD  
 ADD [ADD ADD MULT SUB]  
 MULT  
 SUB

EPIC:  
 ← if all inst, can run in parallel

only make big chunk of know can run in parallel  
 shift to the compiler the responsibility  
 of identifying parallelism

↓ problem?

can't be done  
 (can 18 lane ex w/ ideal conditions)

plan:  
 new chip Itanium using EPIC

nickname: Itanic

unbelievable failure

- totally diff inst set (causes major compatibility problems)

- in C, this is impossible

- problem: aliasing (b/c of ptrs)

p and q can point to same object

combinatorial / state space explosion