OBJECTIVE:

The main objective of this project is to design a falling-edge D Flip-Flop using the Cadence Virtuoso design tool and to perform timing analysis using HSPICE. An additional design constraint is to minimize the usage of the M2 layer. This constraint is important because, when connecting multiple cells in future designs, excessive vertical M2 usage for interconnections can complicate placement and routing. Minimizing M2 usage also helps optimize cell density for a smaller area, improves signal integrity, and reduces parasitic capacitance and resistance, leading to better overall performance.

D-FLIP FLOP DESIGN AS MENTIONED IN CLASS:

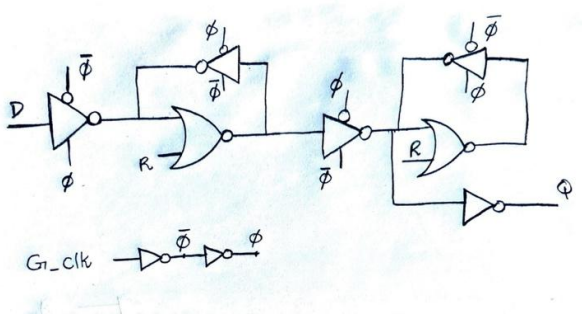
The figure below depicts the design of a D Flip-Flop. The circuit consists of two latches connected in a cascaded configuration each containing a feedback loop. The tristate inverter is part of the feedback path to maintain the latched value.

The input **D** serves as the data signal that will be stored or propagated to the output depending on the clock state. The circuit uses two clock signals: Φ and $\overline{\Phi}$. During the falling edge, $\overline{\Phi}$ becomes active as Φ transitions to low.

The tristate inverters selectively enable certain sections of the circuit to drive outputs, preventing unwanted interference when disabled. The feedback loop stabilizes the data value between clock cycles.

Each latch has a NOR gate, with one input labeled **R**. A global clock is implemented using two cascaded inverters to synchronize circuit operation. The outputs of these inverters, **clk** and **~clk**, are used as control signals for the tristate inverters to prevent glitches.

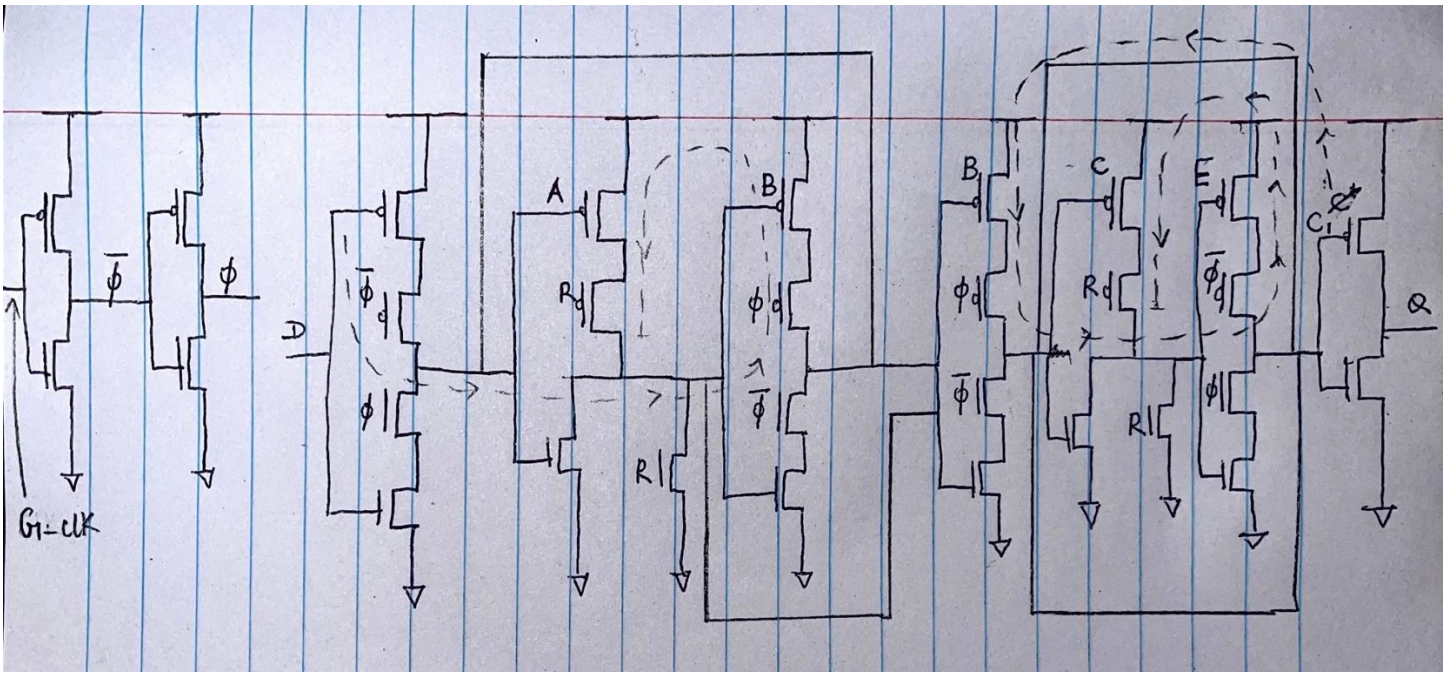
An additional inverter is connected at the common point between the second latch and its feedback loop output to reduce noise, resulting in the final output **Q**.



Gate level view of d flip-flop

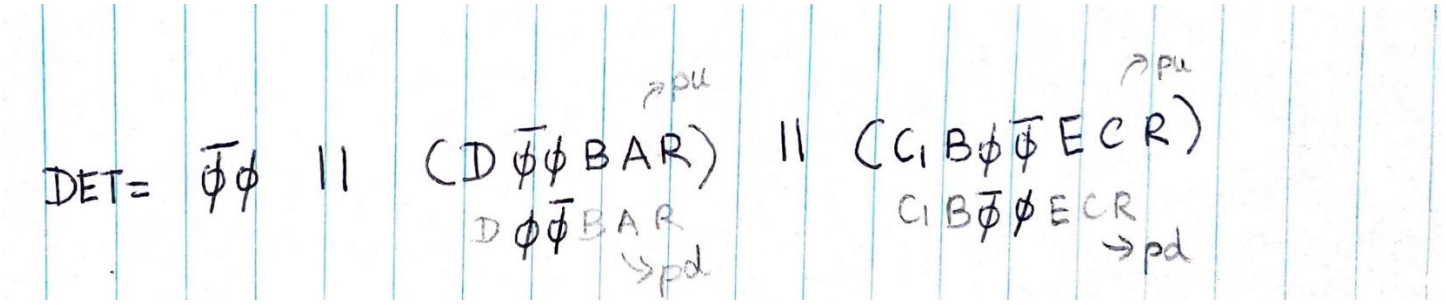
EULER PATH:

The main objective in determining the Euler path is to minimize the number of diffusion breaks. The final Euler path is selected based on this criterion, resulting in a configuration with only two diffusion breaks.



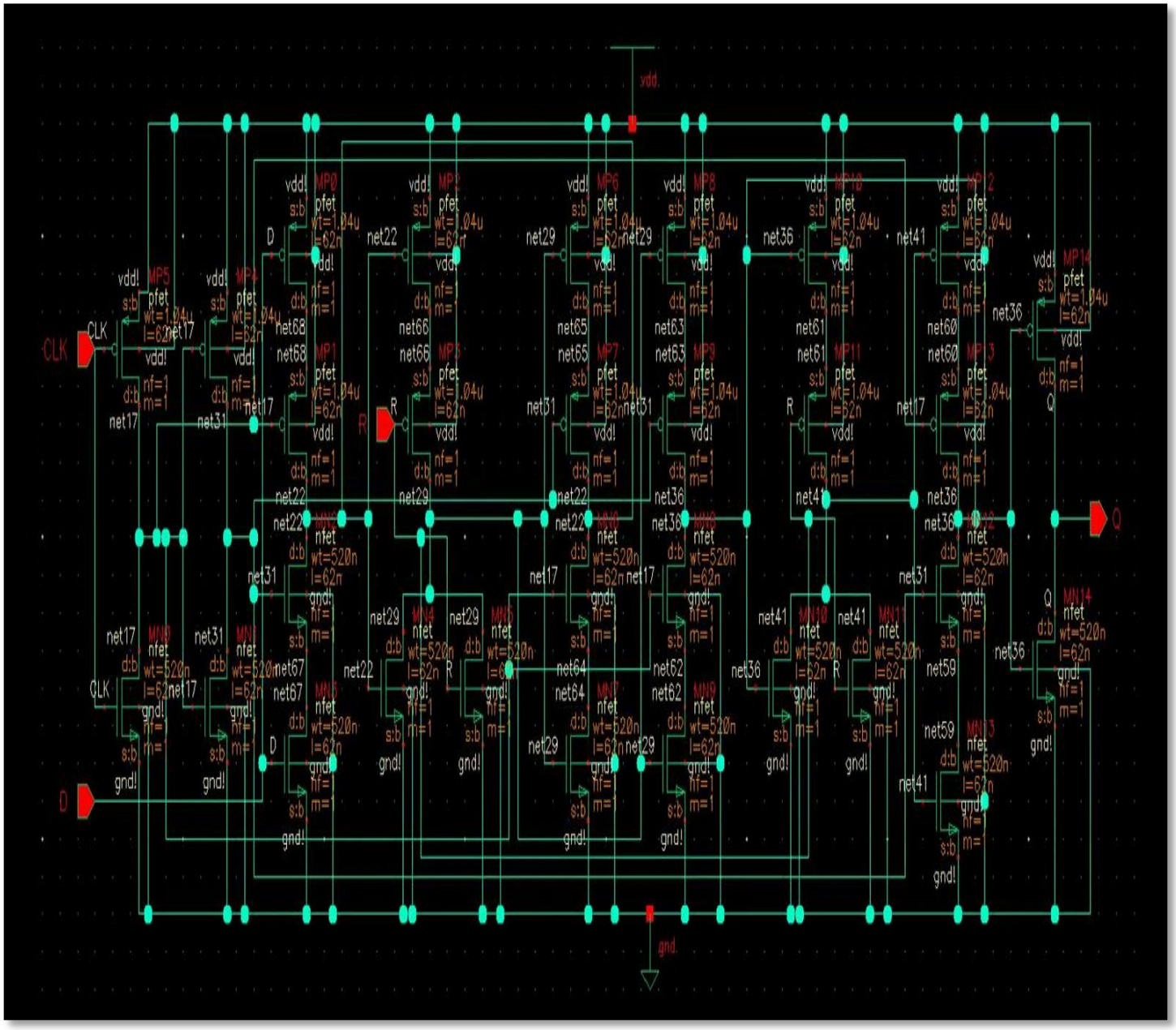
Rough Snippet of Euler Trail

Final Euler Trail:

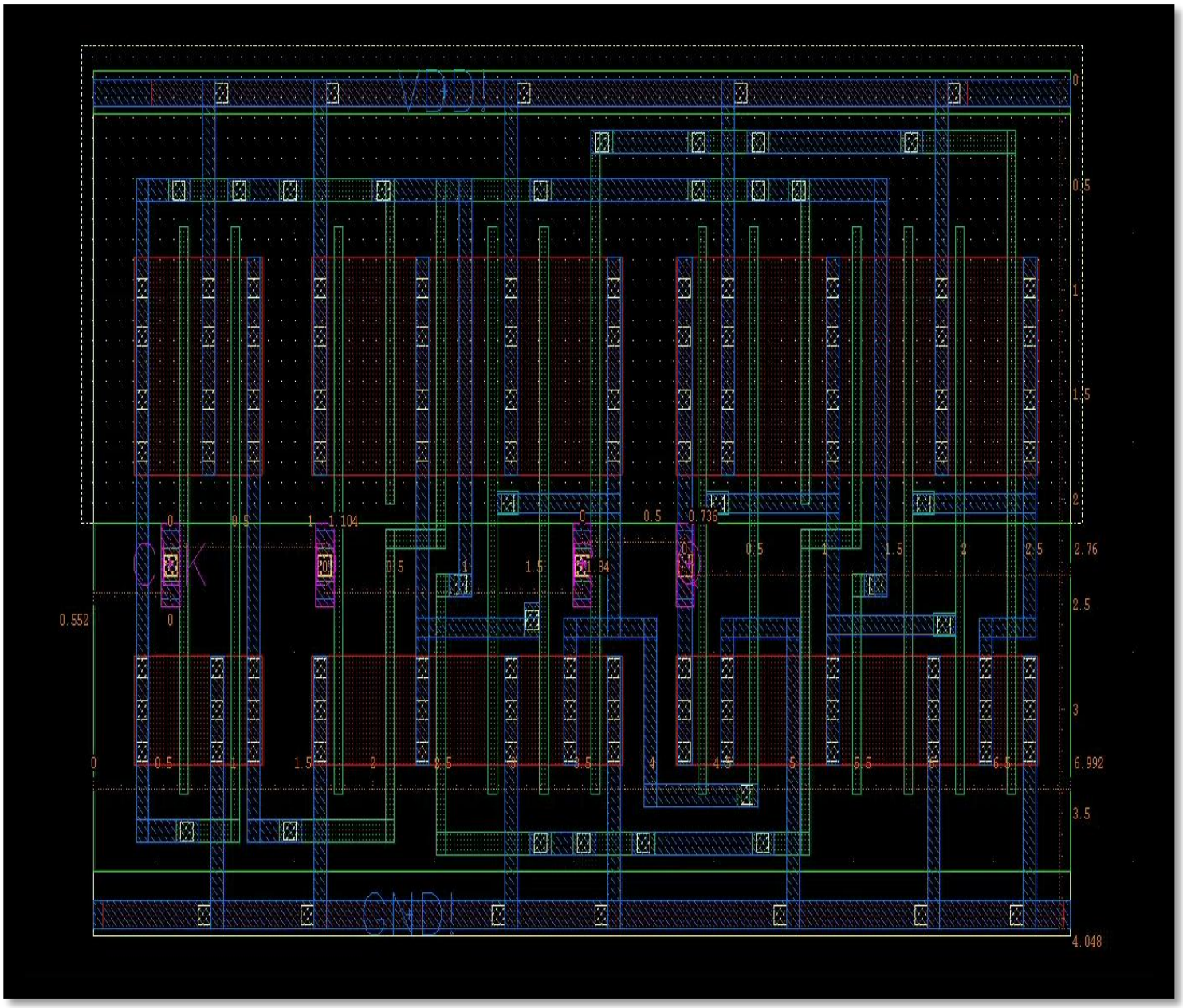


Final Euler Trail with 2 diffusion breaks

SCHEMATIC


vdd!
gnd!
CLK
D
R
Q
net17
net22
net29
net31
net36
net41
net59
net60
net62
net63
net64
net65
net66
net67
net68
MP0
MP1
MP2
MP3
MP4
MP5
MP6
MP7
MP8
MP9
MP10
MP11
MP12
MP13
MP14
MN0
MN1
MN2
MN3
MN4
MN5
MN6
MN7
MN8
MN9
MN10
MN11
MN12
MN13
MN14
pfet
nfet
wt=1.04u
wt=520n
l=62n
nf=1
m=1
d:b
s:b

LAYOUT

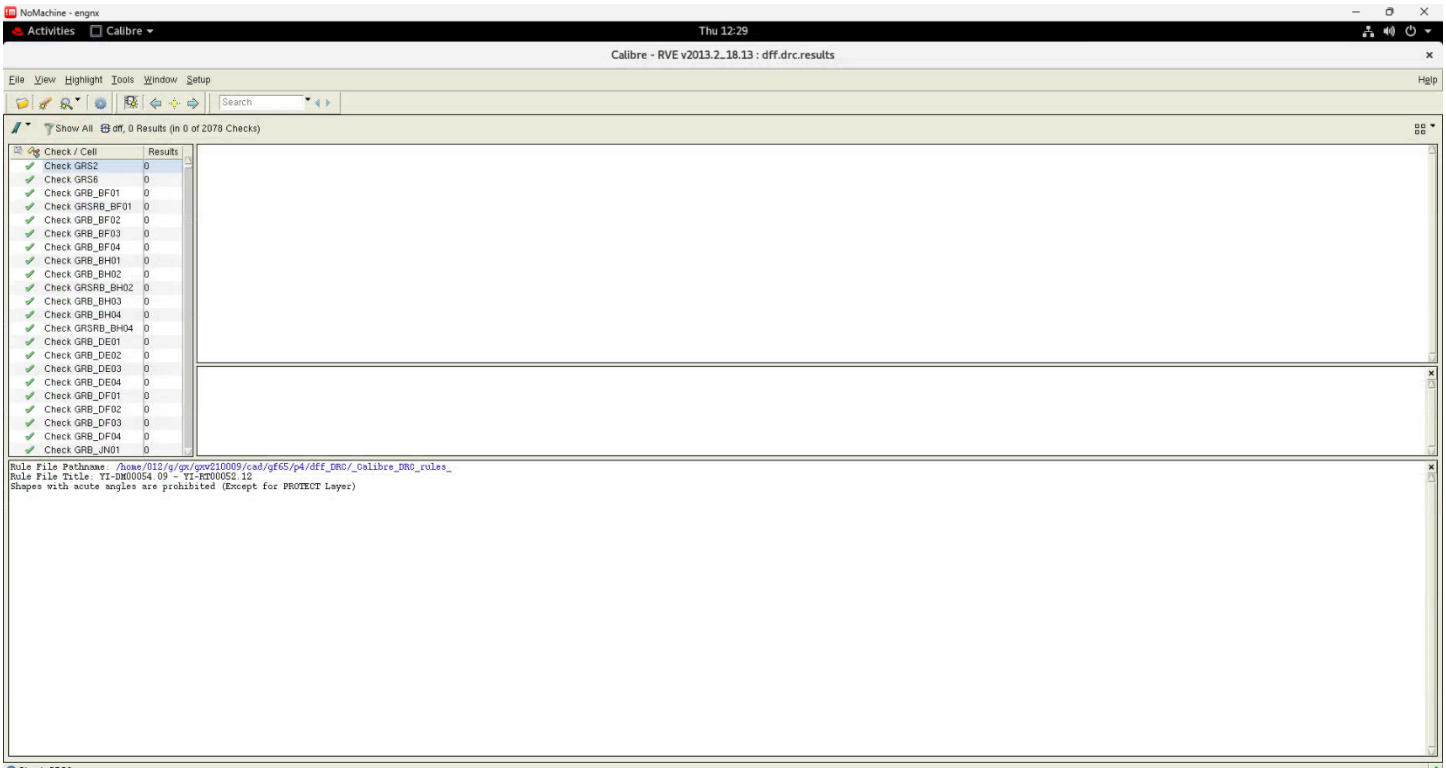


Height: 4.048 um.

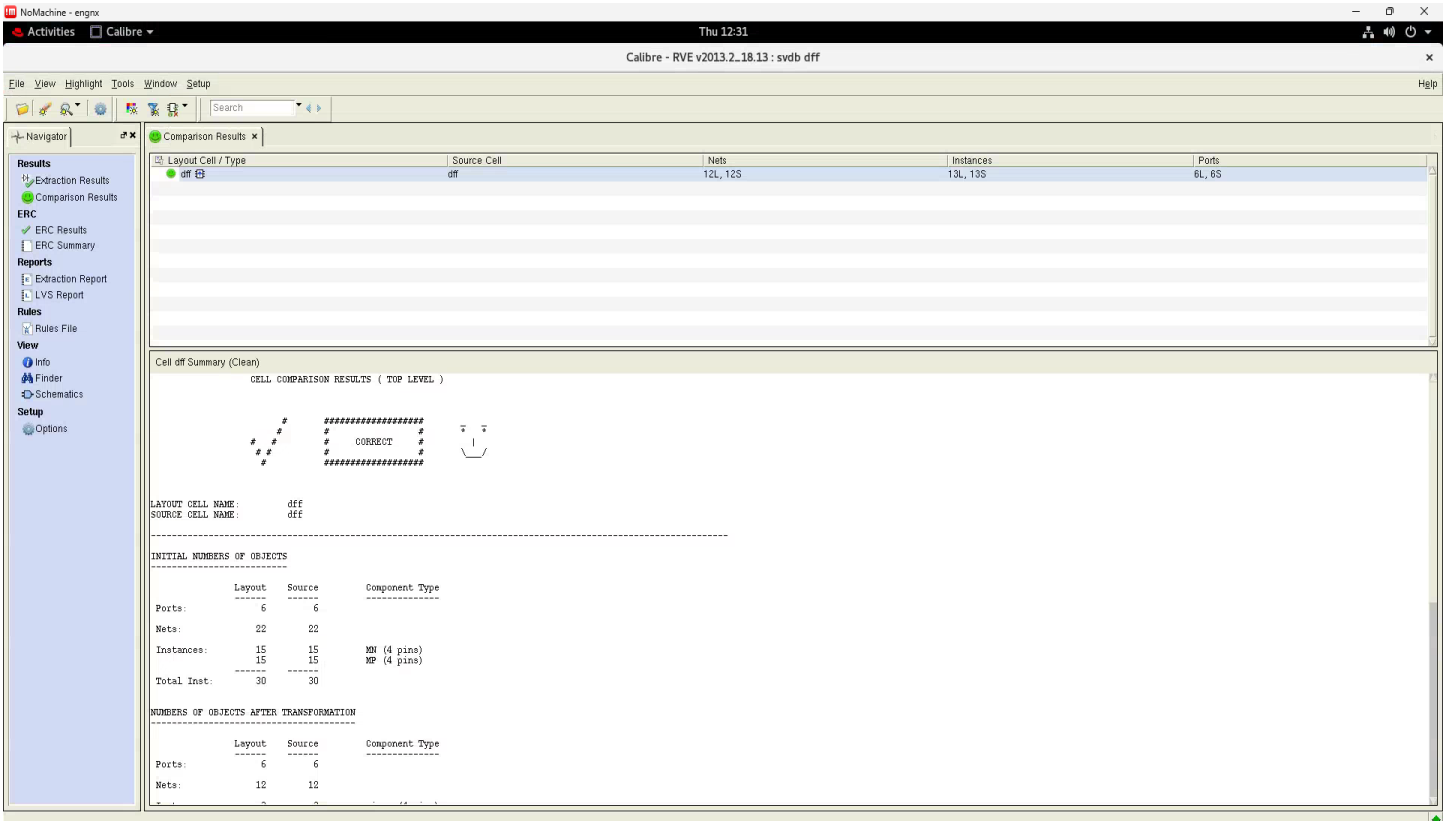
Width: 6.992 um.

Area: 4.048 * 6.992 = 28.3036 um^2

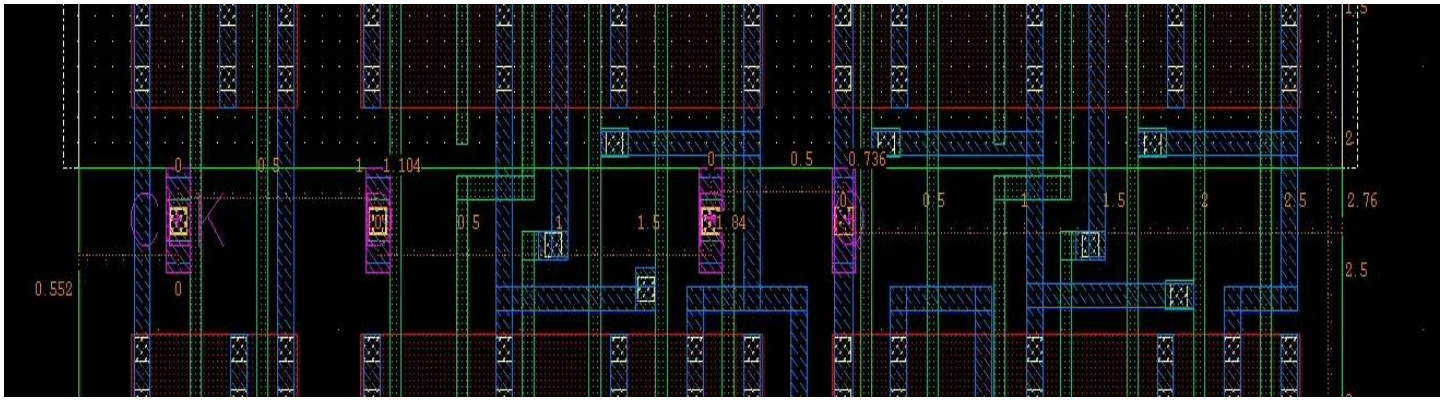
DRC


NoMachine - engnx
Activities
Calibre
Thu 12:29
Calibre - RVE v2013.2_18.13 : dff.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
dff, 0 Results (in 0 of 2078 Checks)
Check / Cell
Results
Check GRS2 0
Check GRS6 0
Check GRB_BF01 0
Check GRSRB_BF01 0
Check GRB_BF02 0
Check GRB_BF03 0
Check GRB_BF04 0
Check GRB_BH01 0
Check GRB_BH02 0
Check GRSRB_BH02 0
Check GRB_BH03 0
Check GRB_BH04 0
Check GRSRB_BH04 0
Check GRB_DE01 0
Check GRB_DE02 0
Check GRB_DE03 0
Check GRB_DE04 0
Check GRB_DF01 0
Check GRB_DF02 0
Check GRB_DF03 0
Check GRB_DF04 0
Check GRB_JN01 0
Rule File Pathname: /home/012/g/gx/gxv210009/cad/gf65/p4/dff_DRC/_Calibre_DRC_rules_
Rule File Title: YI-DM00054.09 - YI-RT00052.12
Shapes with acute angles are prohibited (Except for PROTECT Layer)

LVS


NoMachine - engnx
Activities
Calibre
Thu 12:31
Calibre - RVE v2013.2_18.13 : svdb dff
File View Highlight Tools Window Setup
Help
Search
Navigator
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
dff
dff
12L, 12S
13L, 13S
6L, 6S
Cell dff Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: dff
SOURCE CELL NAME: dff
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 6 6
Nets: 22 22
Instances: 15 15 MN (4 pins)
15 15 MP (4 pins)
Total Inst: 30 30
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 6 6
Nets: 12 12

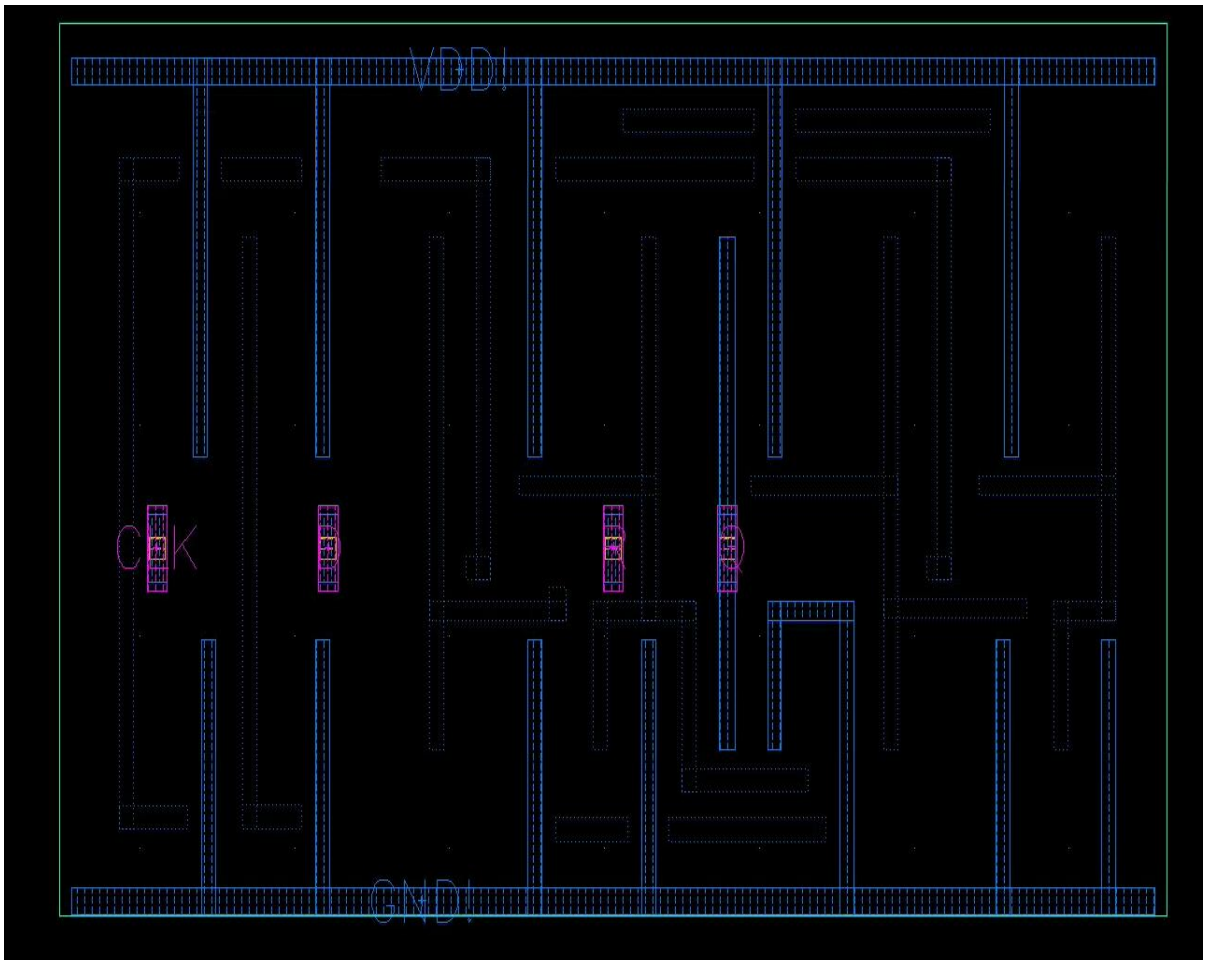
Pin Pitch:



Zoomed view Pin Pitch

The offset is maintained as the standard cells which is 0.552 and the pin-pitch values were assigned as multiples of 0.368.

Abstract View



TIMING CALCULATIONS:

Setup time refers to how early the data signal **D** must arrive and remain stable before the clock signal captures it, ensuring reliable operation. In this case, two types of setup times are considered:

a) **Drop Dead Setup Time(t_{su_dd}):** This represents the minimum preparation time required for a stable output. It is the absolute minimum duration that **D** must be stable before the clock edge to prevent incorrect data propagation to the output.

b) **Optimum Setup Time(t_{su_opt}):** This ensures the fastest and smoothest response. It minimizes the delay from the clock edge to the output, also known as the **Clock-to-Q delay**.

c) **Hold Time(t_{hold}):** Defined as the minimum duration for which the input signal must remain stable after the clock edge to avoid data corruption. It is characterized by the relationship:

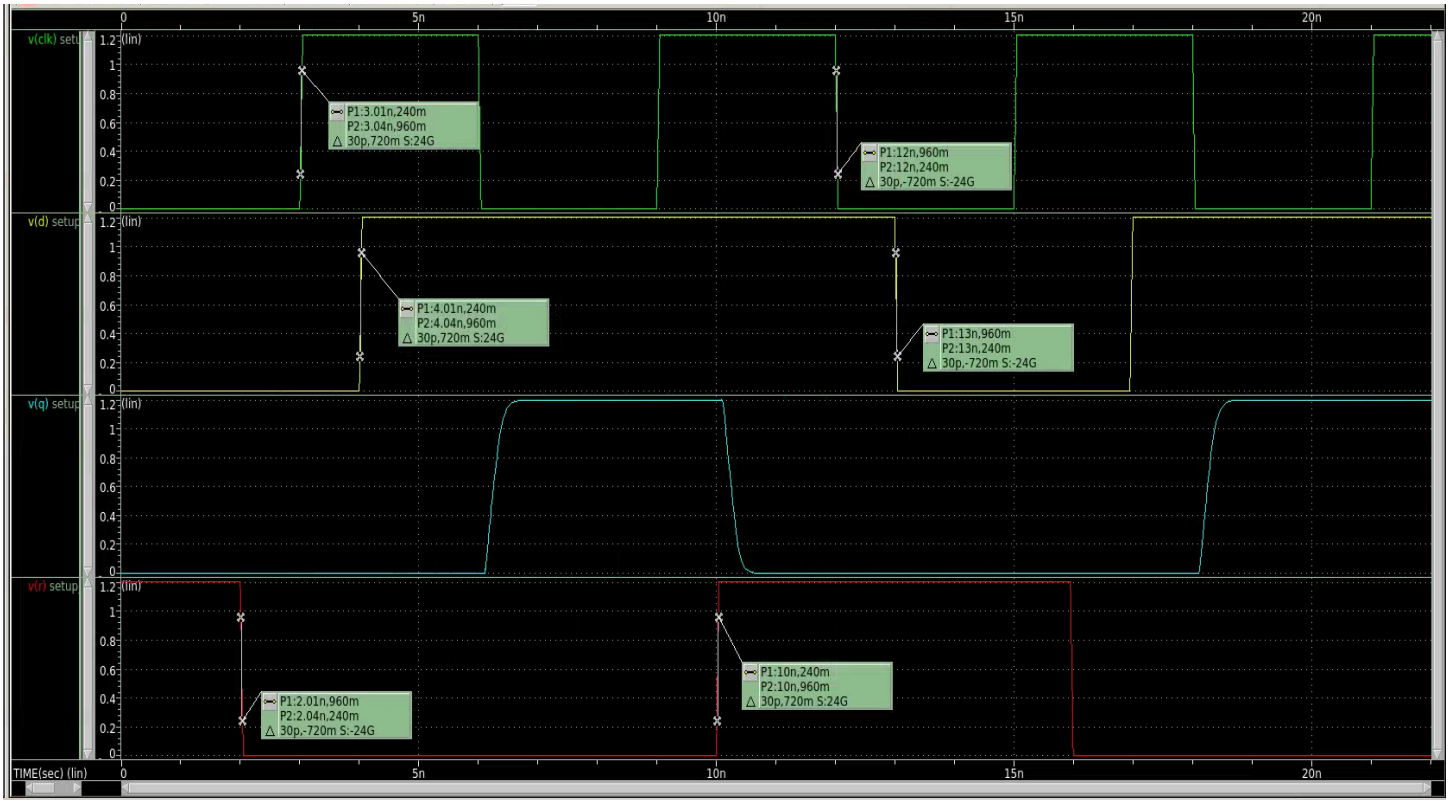
- $t_{su\_dd(0)} = t_{hold(1)}$
- $t_{su\_dd(1)} = t_{hold(0)}$

d) **$t_{clk \rightarrow Q}$:** This is the delay between the clock edge and the moment when the output **Q** updates and stabilizes to the new value based on the input **D**. It represents the propagation delay from the active clock edge (rising or falling) to the output.

e) **Total delay(t_D)**: This is the total delay, defined as the sum of the optimum setup time and the clock-to-Q delay:

$$t_D = t_{su\_opt} + t_{clk \rightarrow Q)}.$$

Waveform Simulation:



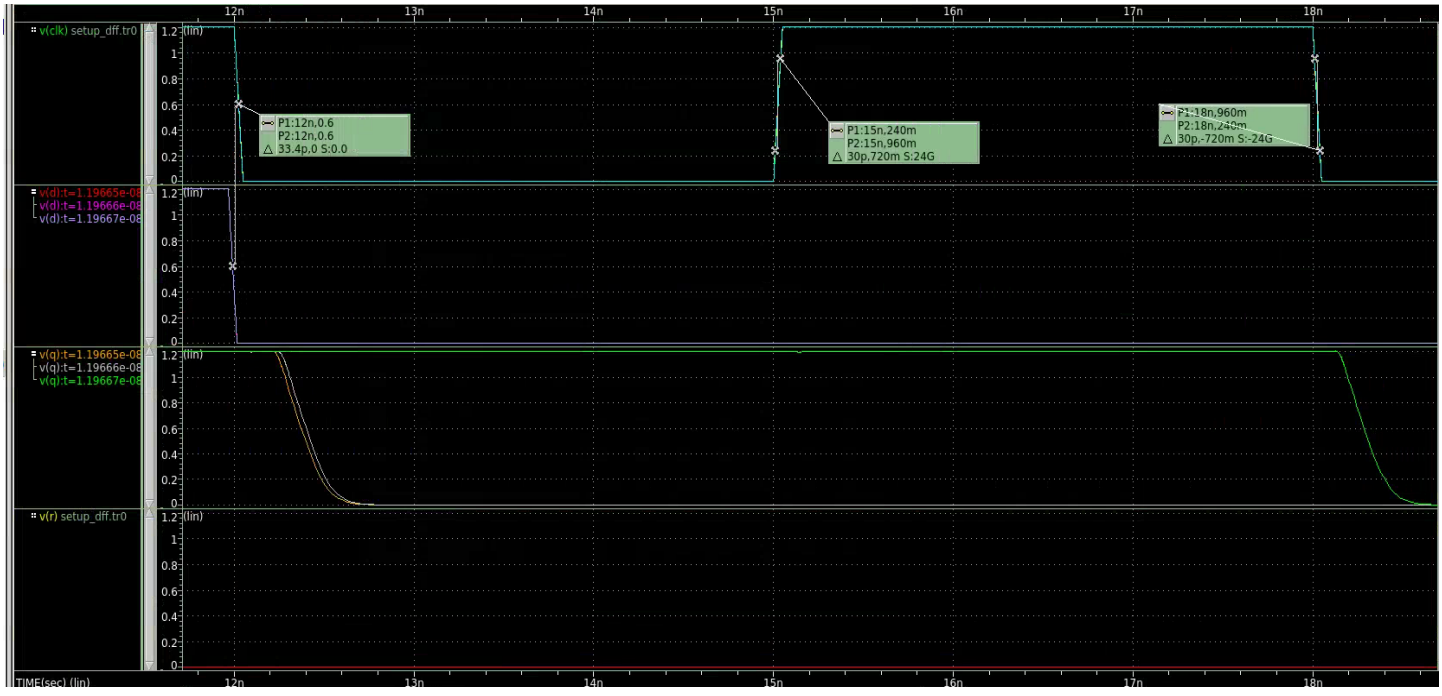
HSpice Setup File

```
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "dff.pex.sp"
.option post runlvl=5

xi GND! Q VDD! CLK D R dff

vdd VDD! GND! 1.2v

vin1 CLK GND! pwl(0ns 0v 3ns 0v 3.05ns 1.2v 6ns 1.2v 6.05ns 0v 9ns 0v 9.05ns 1.2v 12ns 1.2v 12.05ns 0v 15ns 0v 15.05ns 1.2v 18ns
1.2v 18.05ns 0v 21ns 0v 21.05ns 1.2v)
vin2 D GND! pwl(0ns 0v 4ns 0v 4.05ns 1.2v 13ns 1.2v 13.05ns 0v 16.95ns 0v 17ns 1.2v)
vin3 R GND! pwl(0ns 1.2v 2ns 1.2v 2.05ns 0v 10ns 0v 10.05ns 1.2v 15.95ns 1.2v 16ns 0v)

cout Q GND! 55f

$transient analysis
.tr 100ps 22ns

.end
```

Case 1 - : While Passing 0 -> D = 0

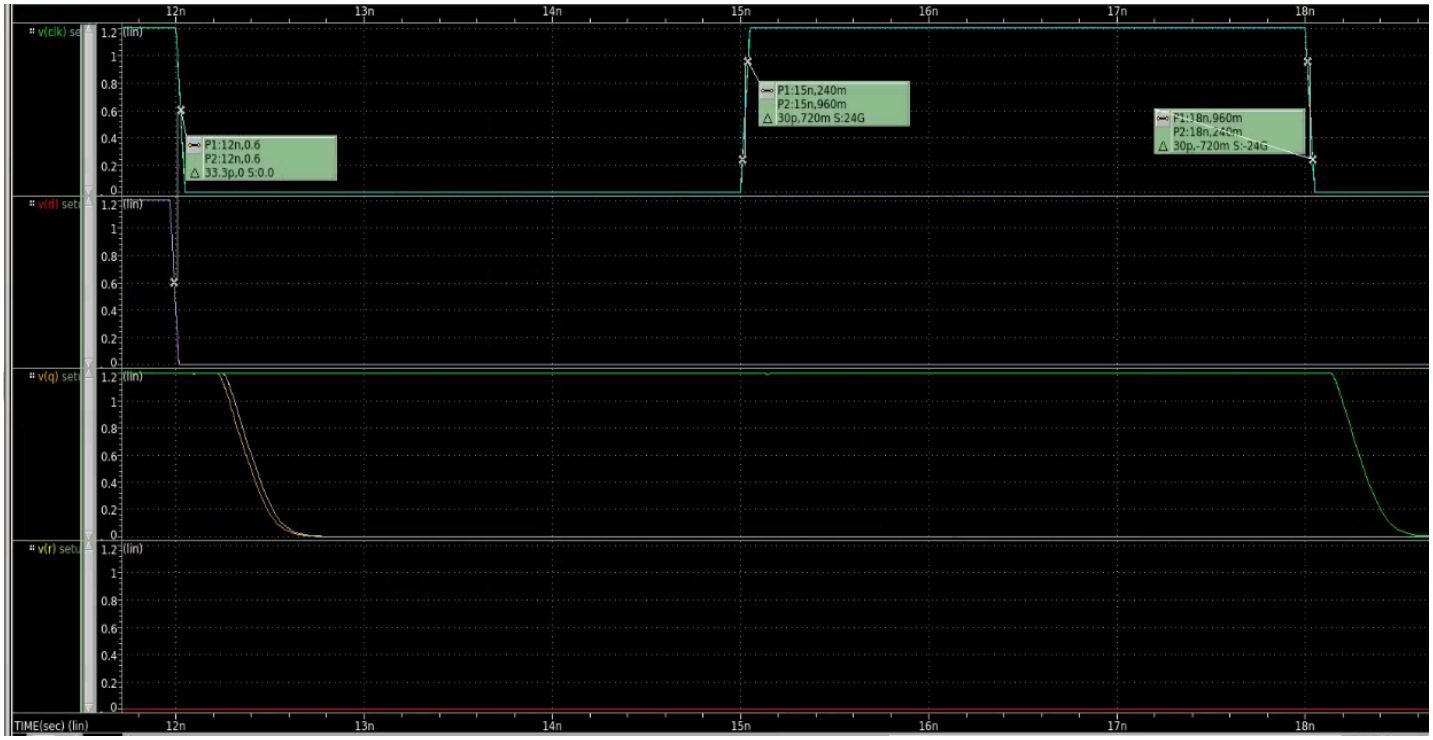
HSPICE setup file

```
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "dff.pex.sp"
.option post runlvl=5

xi GND! Q VDD! CLK D R dff

vdd VDD! GND! 1.2v

vin1 CLK GND! pwl(0ns 0v 3ns 0v 3.05ns 1.2v 6ns 1.2v 6.05ns 0v 9ns 0v 9.05ns 1.2v 12ns 1.2v 12.05ns 0v 15ns 0v 15.05ns 1.2v 18ns
1.2v 18.05ns 0v 21ns 0v 21.05ns 1.2v)
vin2 D GND! pwl(0ns 0v 't' 0v 't+0.05ns' 1.2v)
vin3 R GND! pwl(0ns 1.2v 5ns 1.2v 5.05ns 0v)

cout Q GND! 55f

$transient analysis
.tr 1ps 20ns sweep t 11995.9ps 11996.1ps 0.1ps

.end
```



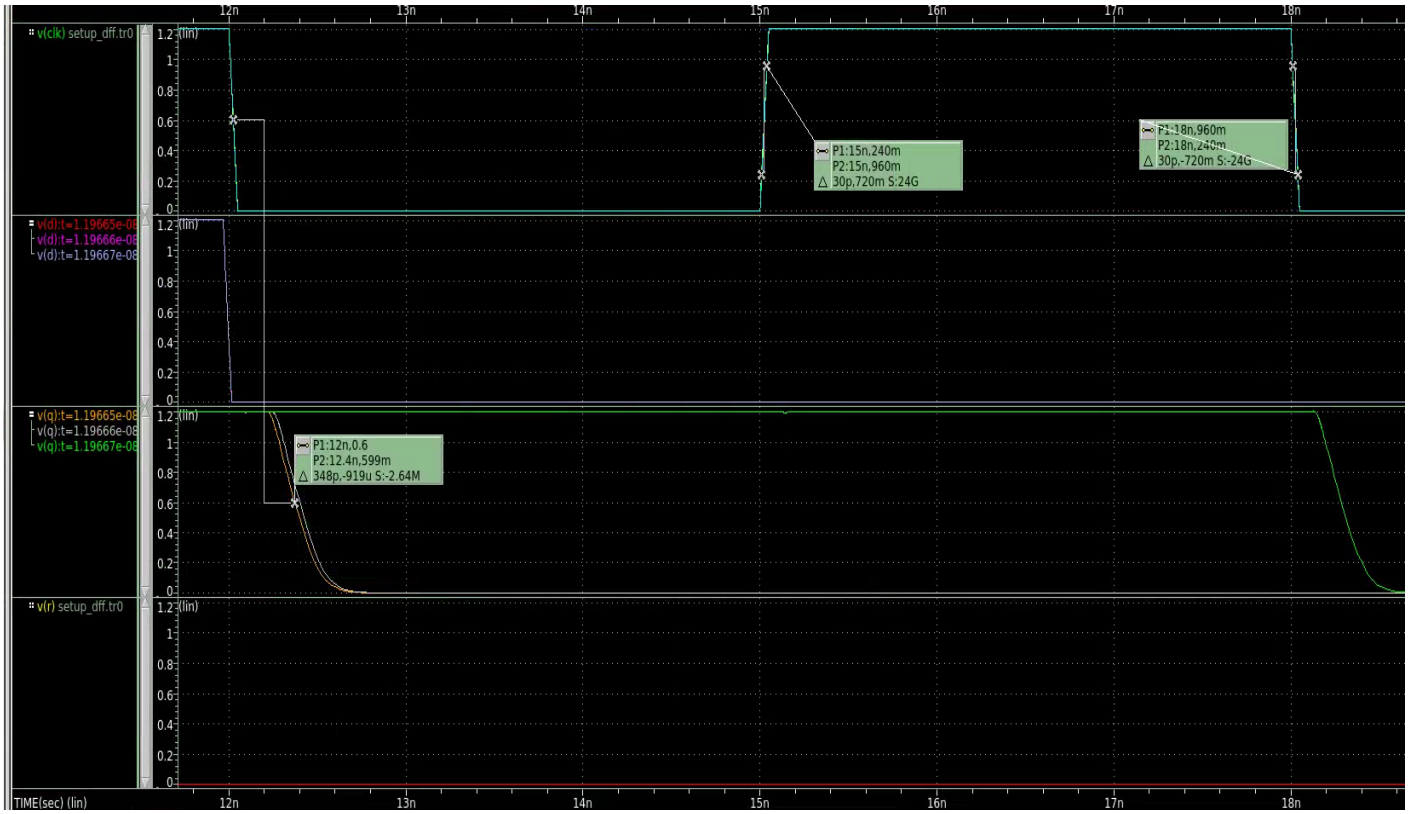
$T_{su\text{-}dd}$ – Drop dead setup time while passing 0

T_{su_dd} = 33.4ps



$T_{su\text{-}opt}$ – Optimum setup time while passing 0

T_{su_opt} = 33.3ps



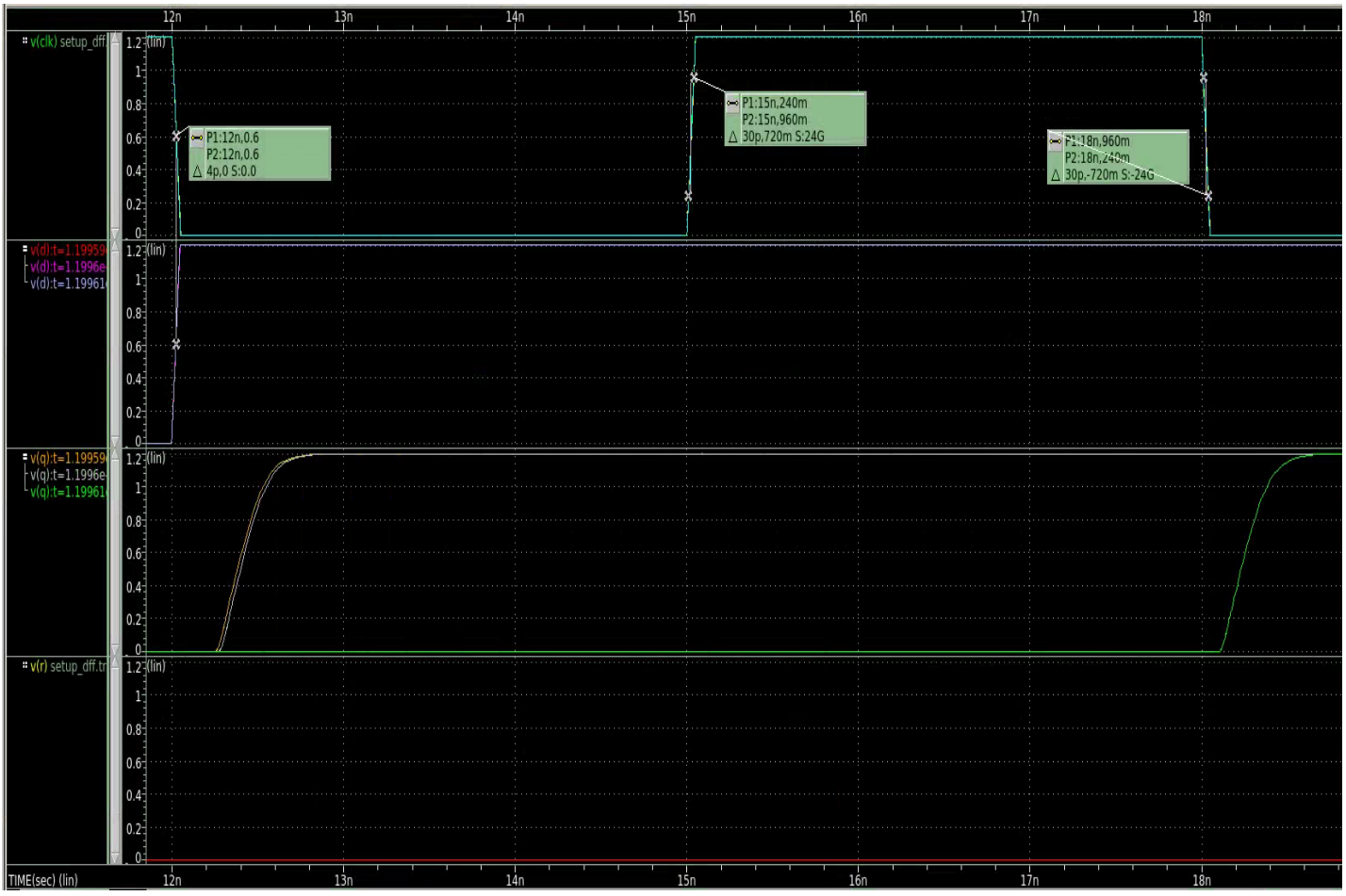
$T_{clk \rightarrow Q}$ – Clock-to-Q time while passing 0

$T_{clk \rightarrow Q}$ = 348ps

Case 2 - : While Passing 1 -> D = 1

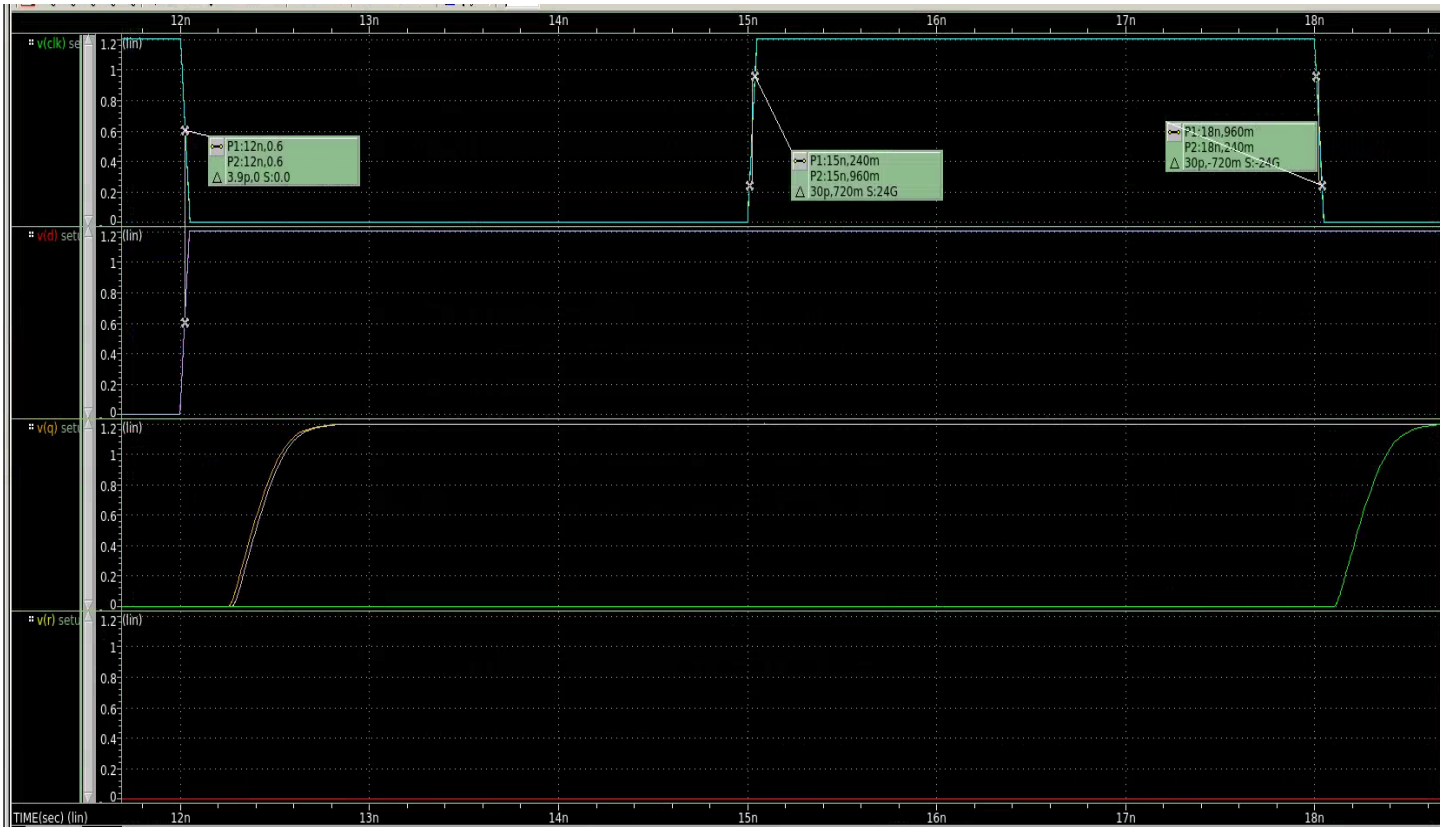
HSPICE setup file

```
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "dff.pex.sp"
.option post runlvl=5

xi GND! Q VDD! CLK D R dff

vdd VDD! GND! 1.2v

vin1 CLK GND! pwl(0ns 0v 3ns 0v 3.05ns 1.2v 6ns 1.2v 6.05ns 0v 9ns 0v 9.05ns 1.2v 12ns 1.2v 12.05ns 0v 15ns 0v 15.05ns 1.2v 18ns
1.2v 18.05ns 0v 21ns 0v 21.05ns 1.2v)
vin2 D GND! pwl(0ns 0v 4ns 0v 4.05ns 1.2v 't' 1.2v 't+0.05ns' 0v)
vin3 R GND! pwl(0ns 1.2v 5ns 1.2v 5.05ns 0v)

cout Q GND! 55f

$transient analysis
.tr 1ps 20ns sweep t 11966.5ps 11966.7ps 0.1ps

.end
```



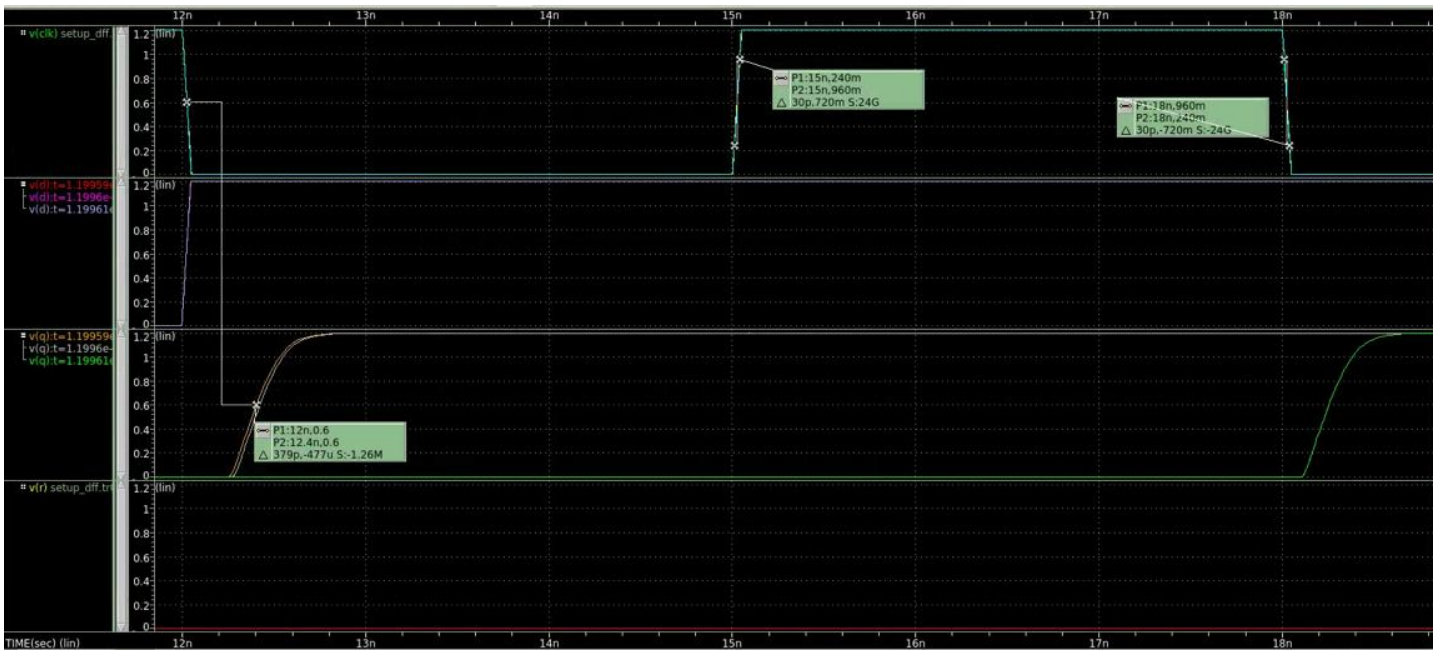
$T_{su\text{-}dd}$ – Drop dead setup time while passing 1

T_{su_dd} = 4ps



$T_{su\text{-}opt}$ – Optimum setup time while passing 1

T_{su_opt} = 3.9ps



$T_{clk \rightarrow Q}$ – Clock-to-Q time while passing 1

$T_{clk \rightarrow Q}$ = 379ps

Parameters	Transition from 1 to 0	Transition from 0 to 1
t_{su_dd}	3.9 ps	33.3 ps
t_{su_opt}	4 ps	33.4 ps
t_{hold}	33.3 ps	3.9 ps
$t_{clk\text{-}Q}$	379 ps	348 ps
t_D	383 ps	381.4 ps