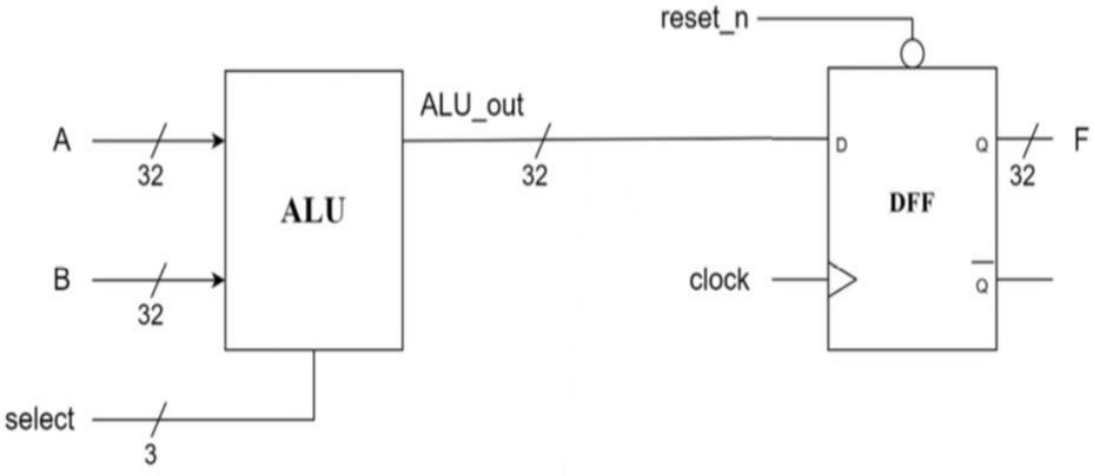
## Introduction

The Arithmetic Logic Unit (ALU) is a fundamental component of a CPU, responsible for performing various arithmetic and logical operations. A 32-bit ALU is designed to execute the following operations: addition, subtraction (using 2's complement), bitwise NOT of input **A**, bitwise NOT of input **B**, comparison, and multiplication.

The operations are selected using a 3-bit select line, and a clock signal is used to synchronize all operations, thereby incorporating both combinational and sequential logic within the module. Inputs **A** and **B** are 32-bit operands, and **reset_n** is an active-low reset signal. When **reset_n** is high, the output or the stored value in the D flip-flop is cleared. When **reset_n** is low, the output is captured on the rising edge of the clock signal.

The first always block is sequential logic, triggered by the rising edge of the clock, and can be classified as edge-triggered. The second block represents combinational logic and performs the defined arithmetic and logical operations.

# Block Diagram



# Design Flow

Project 1: Developed behavioral Verilog code and a testbench for a 16-bit ALU and implemented it using Xilinx Vivado.

Project 2 : A 16-bit ALU design was scaled up to a 32-bit ALU to reduce latency and enhance performance. Verilog code for the 32-bit ALU was successfully implemented. A netlist was generated, and a report displaying the total number of cells used in the design was produced using Synopsys Design Vision.
**Result: No. of cells obtained = 4164 cells**

Project 3: Used the GF65nm process and Cadence design tools to design and characterize the layout of an inverter.

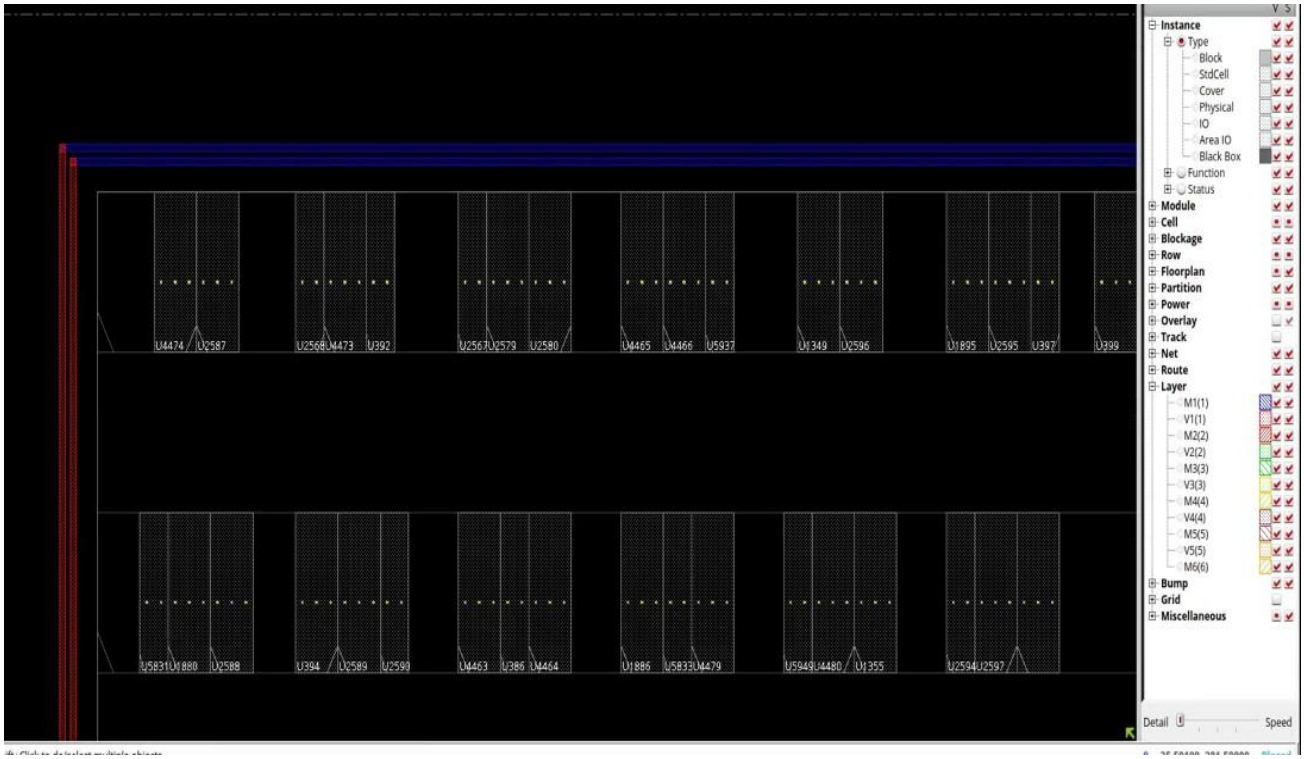
Project 4: Designed a custom cell library containing eight combinational standard cells: inverter, NAND2, NOR2, AOI332, NAND3, OAI4331, an 11-input logic circuit, and NOR3.
**Height of all cells: 3.312 um.**

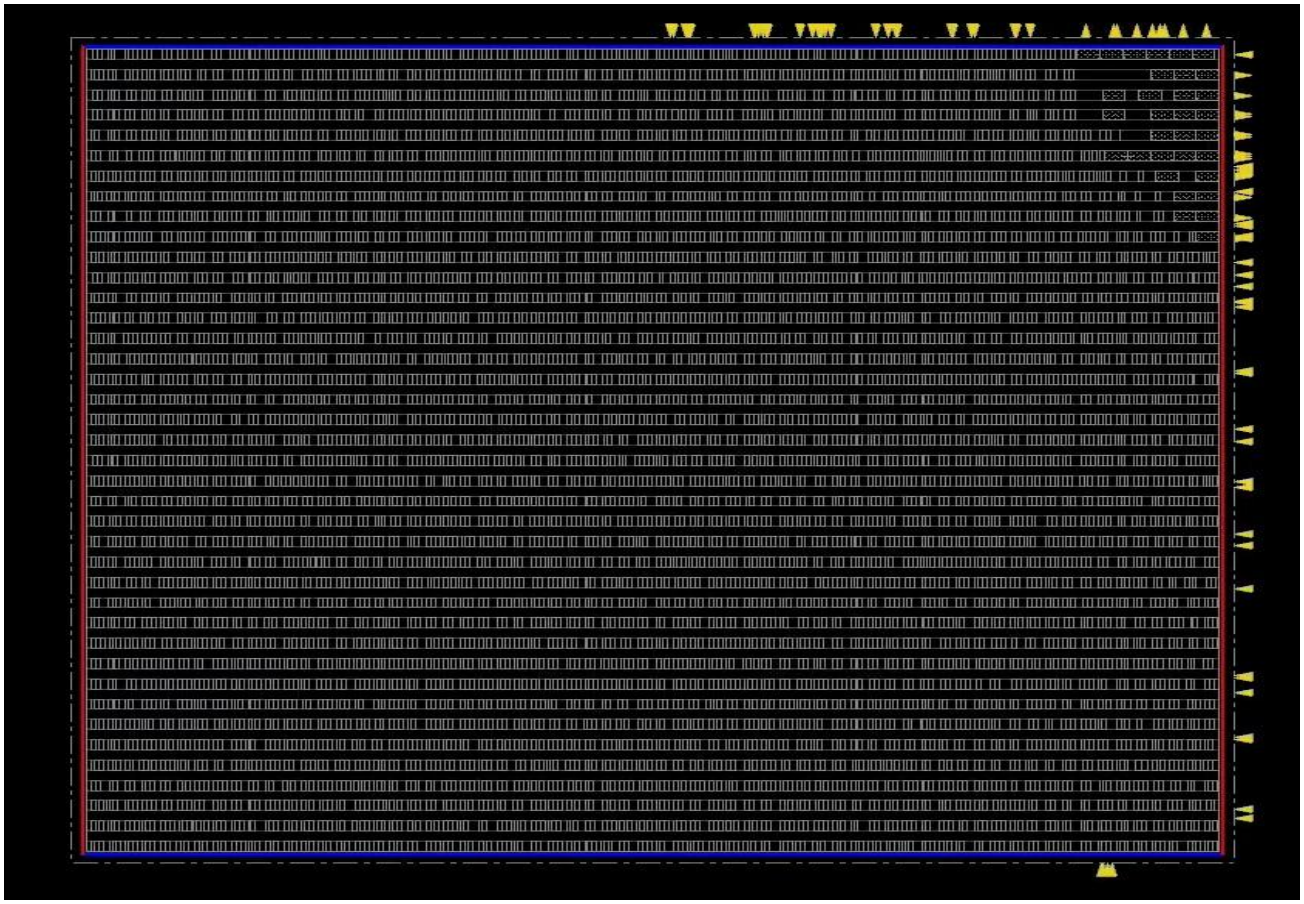
Project 5: Designed a falling-edge D Flip-Flop using the Cadence Virtuoso design tool and performed timing analysis using HSPICE.
**Height of the d flip-flop : 4.048 um.**

Project 6: Cells designed in Projects 3–5 were used to generate the complete layout of a 32-bit ALU. Characterization of each cell was done using PrimeLib. A LEF file was generated using Virtuoso. LibraryCompiler was then used to convert the combined library file into a database (.db) file. Synopsys Design Vision synthesized a Verilog file using the .db file, and a netlist was generated showing the total number of cells used: 7,402. Placement and routing were handled by Innovus. After completion, the design was imported into Virtuoso for DRC, LVS, and PEX checks. Static Timing Analysis (STA) was performed using PrimeTime to calculate clock delay and power consumption

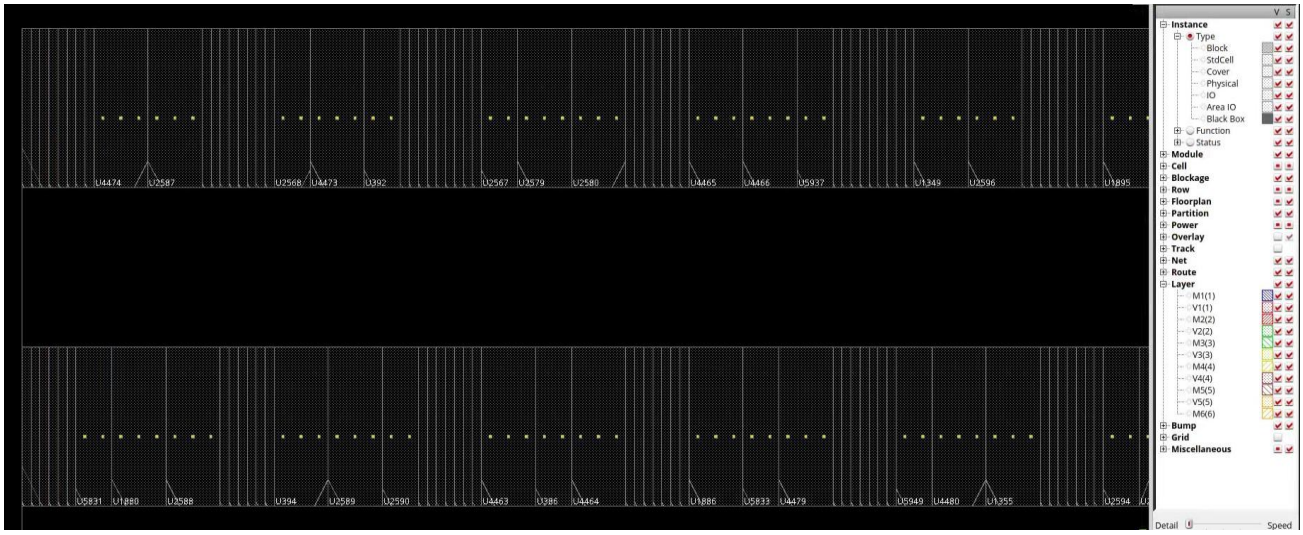
# Cell Placement and Routing in Innovus

## Without filler cells:

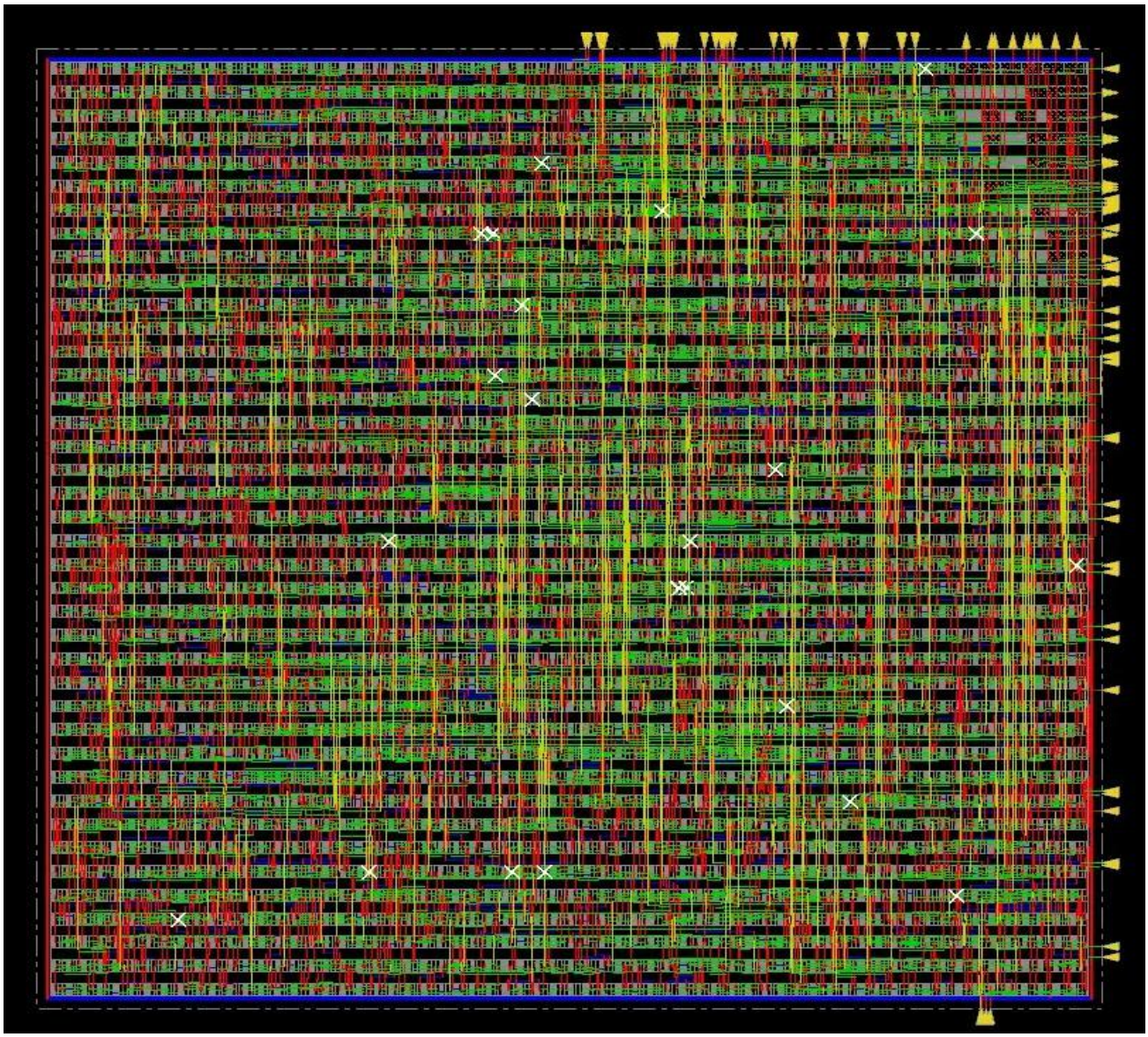


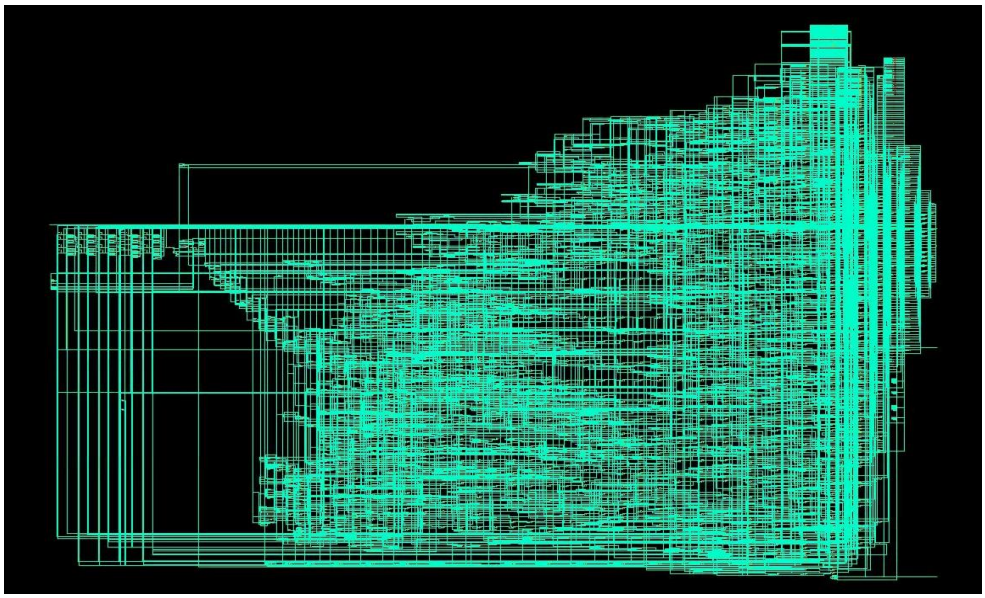
# With filler cells:



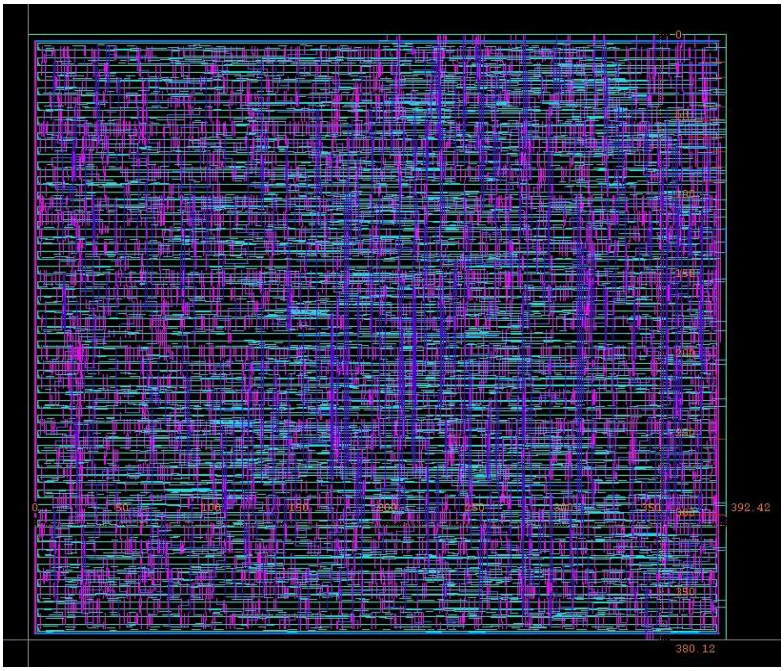

## Routing



## Schematic



# Layout

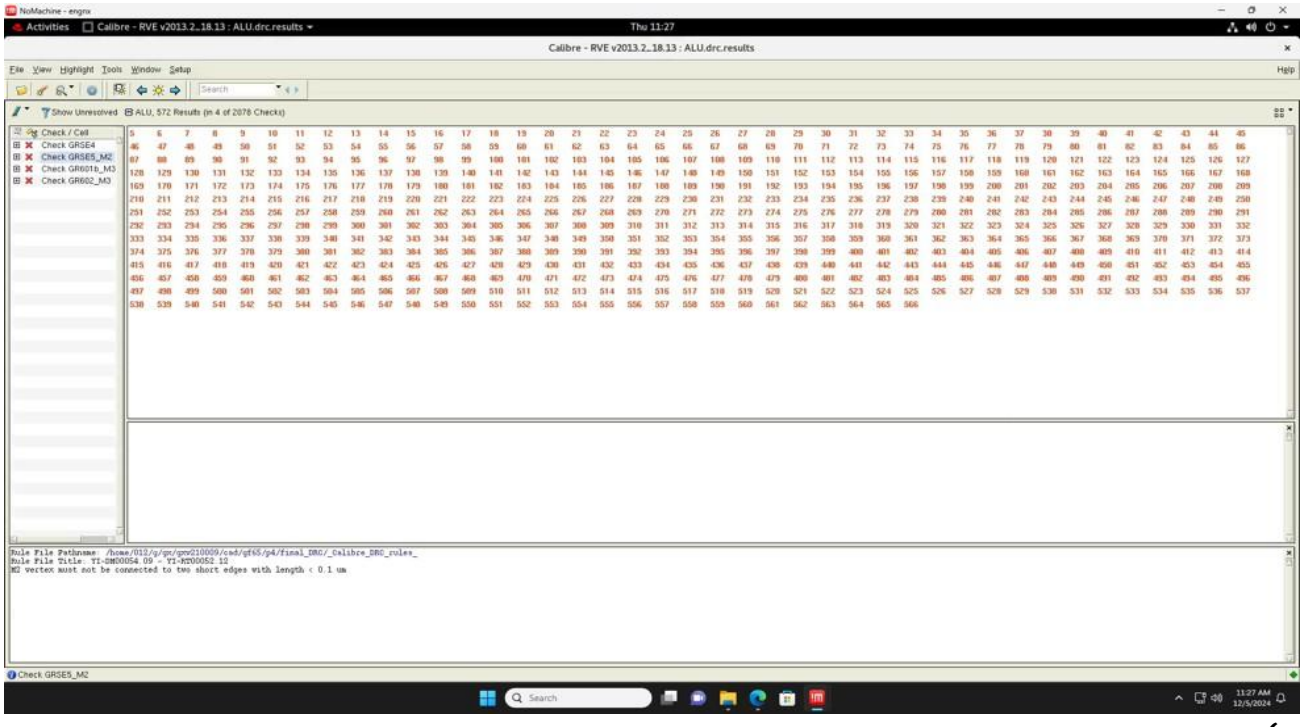



**Final cell height = 380.12 um**

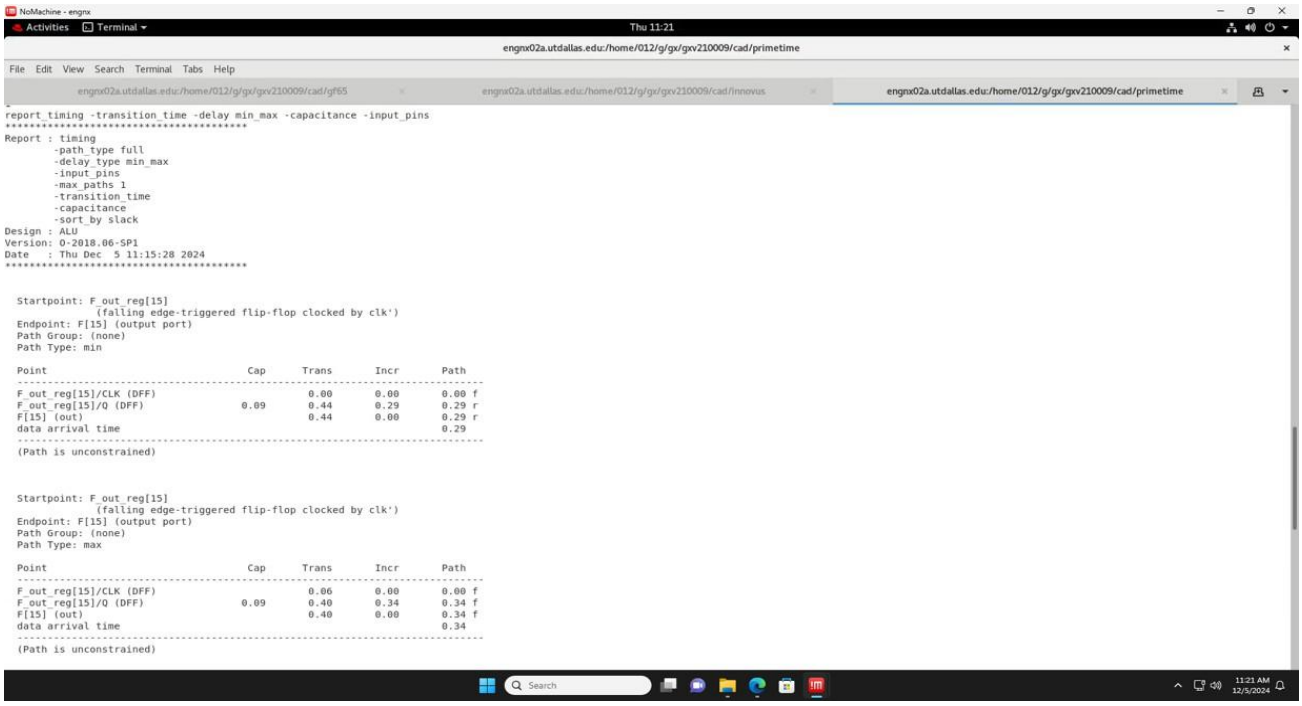
**Final cell width = 392.42 um**

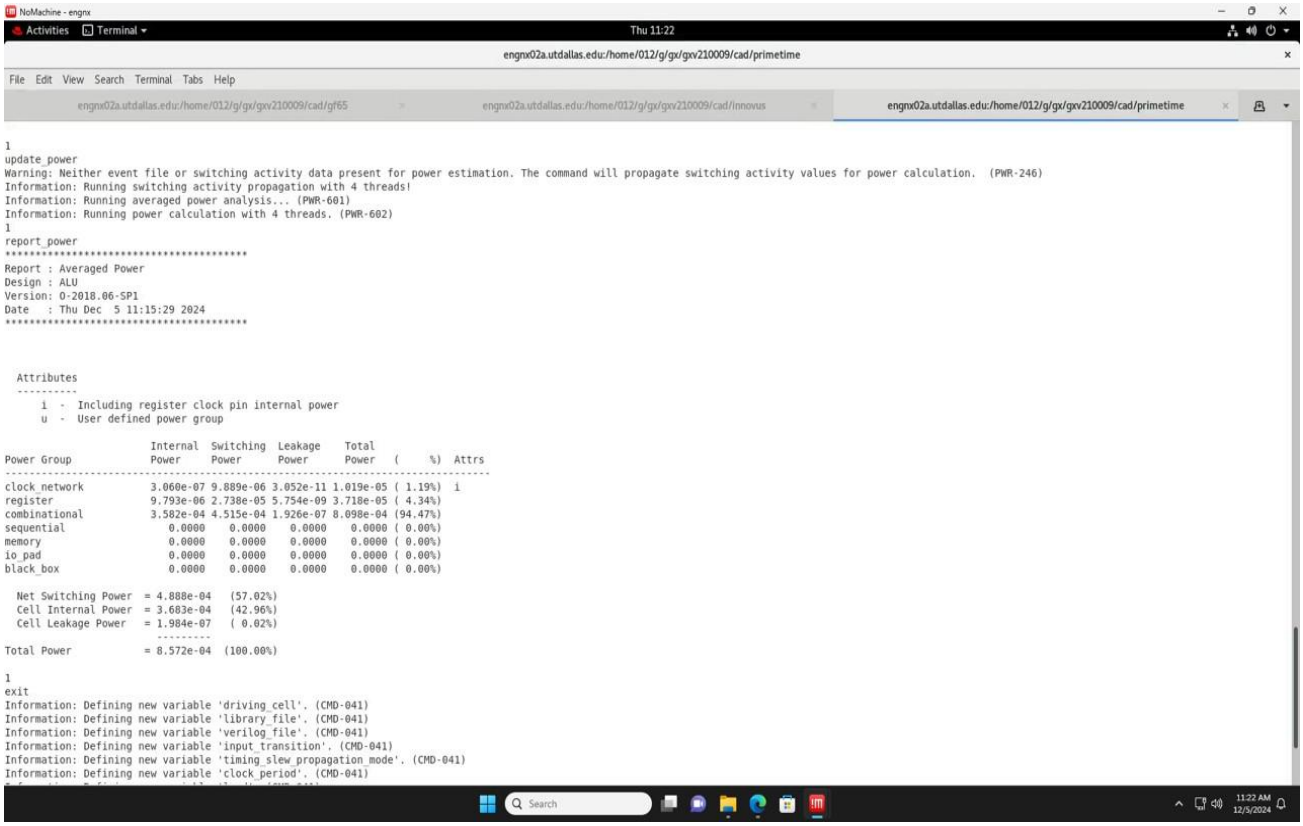
# DRC Results

Initial DRC violations were around 2000 but it was brought down to around 500 by doing few changes .



# Primetime


NoMachine - engnx
Activities
Terminal
Thu 11:21
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/primetime
File Edit View Search Terminal Tabs Help
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/gf65
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/innovus
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/primetime
report_timing -transition_time -delay min_max -capacitance -input_pins
****************************************
Report : timing
-path_type full
-delay_type min_max
-input_pins
-max_paths 1
-transition_time
-capacitance
-sort_by slack
Design : ALU
Version: O-2018.06-SP1
Date : Thu Dec 5 11:15:28 2024
****************************************
Startpoint: F_out_reg[15]
(falling edge-triggered flip-flop clocked by clk')
Endpoint: F[15] (output port)
Path Group: (none)
Path Type: min
Point Cap Trans Incr Path
F_out_reg[15]/CLK (DFF) 0.00 0.00 0.00 f
F_out_reg[15]/Q (DFF) 0.09 0.44 0.29 0.29 r
F[15] (out) 0.44 0.00 0.29 r
data arrival time 0.29
(Path is unconstrained)
Startpoint: F_out_reg[15]
(falling edge-triggered flip-flop clocked by clk')
Endpoint: F[15] (output port)
Path Group: (none)
Path Type: max
Point Cap Trans Incr Path
F_out_reg[15]/CLK (DFF) 0.06 0.00 0.00 f
F_out_reg[15]/Q (DFF) 0.09 0.40 0.34 0.34 f
F[15] (out) 0.40 0.00 0.34 f
data arrival time 0.34
(Path is unconstrained)
Search
11:21 AM
12/5/2024


NoMachine - engnx
Activities
Terminal
Thu 11:22
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/primetime
File Edit View Search Terminal Tabs Help
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/gf65
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/innovus
engnx02a.utdallas.edu:/home/012/g/gx/gxv210009/cad/primetime
1
update_power
Warning: Neither event file or switching activity data present for power estimation. The command will propagate switching activity values for power calculation. (PWR-246)
Information: Running switching activity propagation with 4 threads!
Information: Running averaged power analysis... (PWR-601)
Information: Running power calculation with 4 threads. (PWR-602)
1
report_power
****************************************
Report : Averaged Power
Design : ALU
Version: O-2018.06-SP1
Date : Thu Dec 5 11:15:29 2024
****************************************
Attributes
i - Including register clock pin internal power
u - User defined power group
Power Group Internal Power Switching Power Leakage Power Total Power ( %) Attrs
clock_network 3.060e-07 9.889e-06 3.052e-11 1.019e-05 ( 1.19%) i
register 9.793e-06 2.738e-05 5.754e-09 3.718e-05 ( 4.34%)
combinational 3.582e-04 4.515e-04 1.926e-07 8.098e-04 (94.47%)
sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
io_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
black_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
Net Switching Power = 4.888e-04 (57.02%)
Cell Internal Power = 3.683e-04 (42.96%)
Cell Leakage Power = 1.984e-07 ( 0.02%)
---------
Total Power = 8.572e-04 (100.00%)
1
exit
Information: Defining new variable 'driving_cell'. (CMD-041)
Information: Defining new variable 'library_file'. (CMD-041)
Information: Defining new variable 'verilog_file'. (CMD-041)
Information: Defining new variable 'input_transition'. (CMD-041)
Information: Defining new variable 'timing_slew_propagation_mode'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
Search
11:22 AM
12/5/2024

# Symbol


# Trade-offs g challenges faced while designing

- The height of all other cells was scaled up to match the height of the D Flip-Flop (DFF). The pin pitch was adjusted to 0.52 µm due to significant empty spaces remaining between cells, even after the insertion of filler cells. The offset was modified to 0.26 µm to accommodate and minimize these gaps.
- During the initial simulation, approximately 2,000 DRC errors were observed, primarily due to the height of the M2 layer. These errors were later reduced to 572 by resizing the M2 layer.
- Initially, the filler cells were designed with a width of 0.52 µm; however, this led to excessive spacing. The design was later updated with a reduced filler cell width of 0.26 µm to effectively minimize unused space.