

OBJECTIVE:

This project uses the GF65nm process and Cadence design tools to design the layout and characterize an inverter. The power and ground pins in the layout are named VDD! and GND!. Likewise, the input and output pins are capitalized and named IN and OUT in both schematic and layout. The VDD value is assigned as 1.2V and the ground as 0V. The CMOS inverter is designed with specific values: the width of the PMOS (W_p) is $1.9\text{ }\mu\text{m}$, the width of the NMOS (W_n) is $1.5\text{ }\mu\text{m}$, and the load capacitance (C_{load}) is 20 fF. **The channel length is 65 nm. The main design objective of the project is to minimize the bounding area (height \times width) of the inverter layout.**

ABSTRACT:

Various drawing layers in the LSW pane were used to create the layout in the Virtuoso Layout Editing Window, including NW, RX, JZ, JX, PC, CA, M1, V1, and M2. The layout was designed according to specific metric values, with the pin pitch being a multiple of 0.26 and the offset value defined as $(0.13 + 0.26 \times n)$. The poly gates of the transistors were also aligned vertically in the design.

After designing the layout, the DRC (Design Rule Check) is run. A DRC result with 0 errors indicates that the layout is ready for fabrication; however, this does not guarantee functional correctness. Therefore, an LVS (Layout Versus Schematic) check is performed to ensure that the layout matches the schematic.

Once these checks are completed, parasitic capacitance and resistance values are extracted using PEX. HSPICE is then used to generate the SPICE netlist file. The output log from HSPICE is examined to determine whether the simulation completed successfully; otherwise, errors are indicated.

Finally, the HSPICE setup file is run, and with the help of WaveView, the waveforms of the desired signals are analyzed.

LAYOUT:

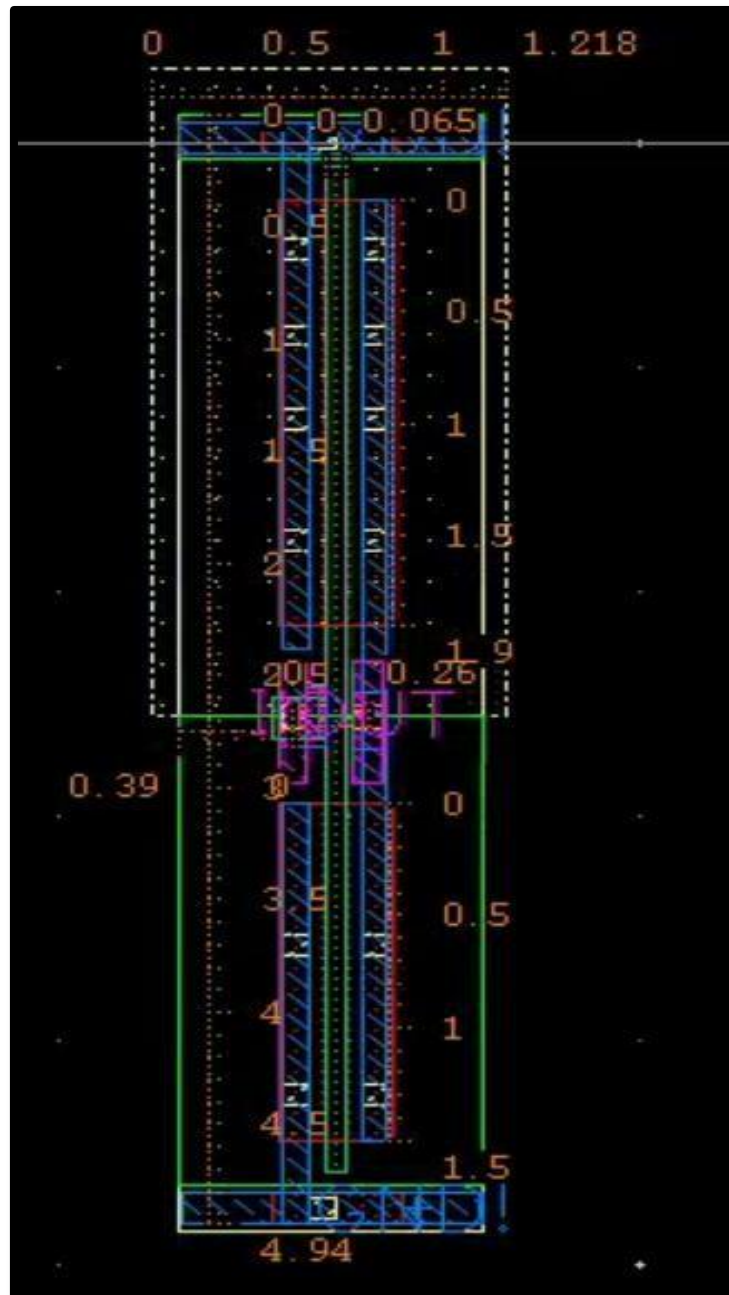


Figure 1. Inverter Layout

DIMENSIONS OF THE LAYOUT:

Height = 4.94um

Width = 1.218um

Width of PMOS = 1.9um

Width of NMOS = 1.5um

Cell ratio = Width of PMOS/ Width of NMOS = 1.266

Length = 0.065um

Area = 4.94 * 1.218 = 6.016 um²

EDP = 1.728 * 10⁻²⁴ Js

SCHEMATIC:

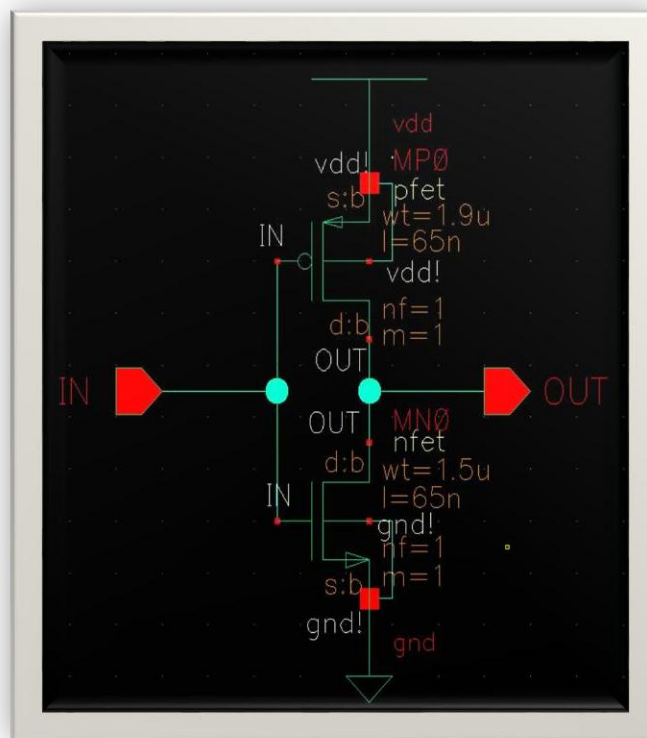


Figure 2. Schematic view of Inverter

DRC CHECK (Design Rule Check):

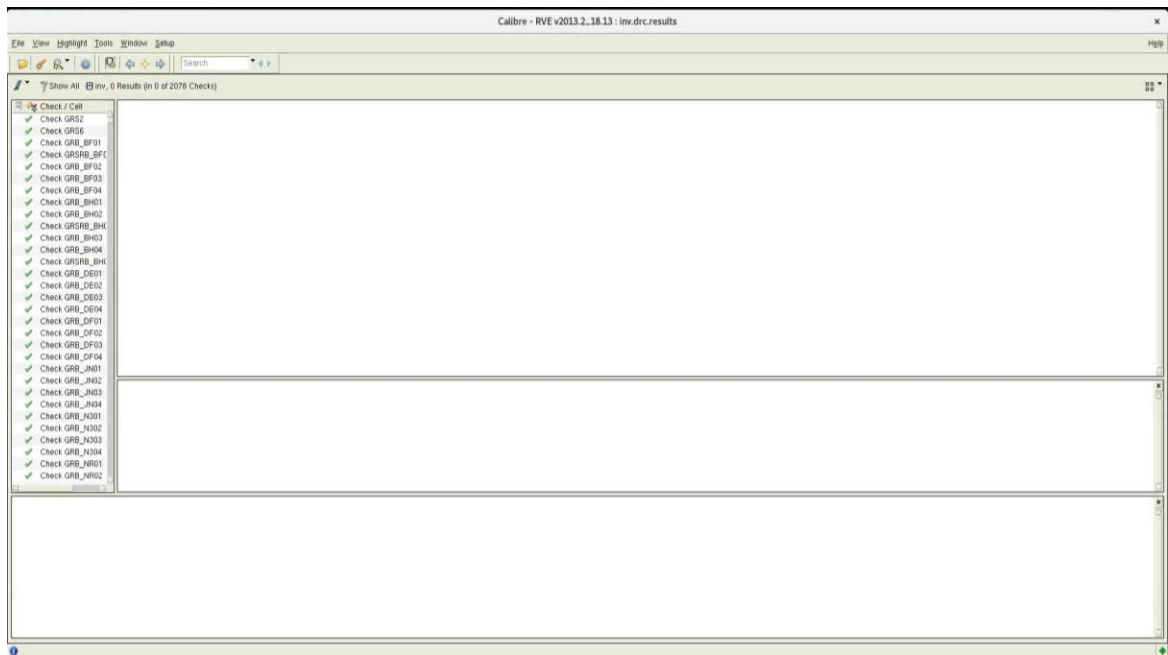


Figure 3. DRC Check Results

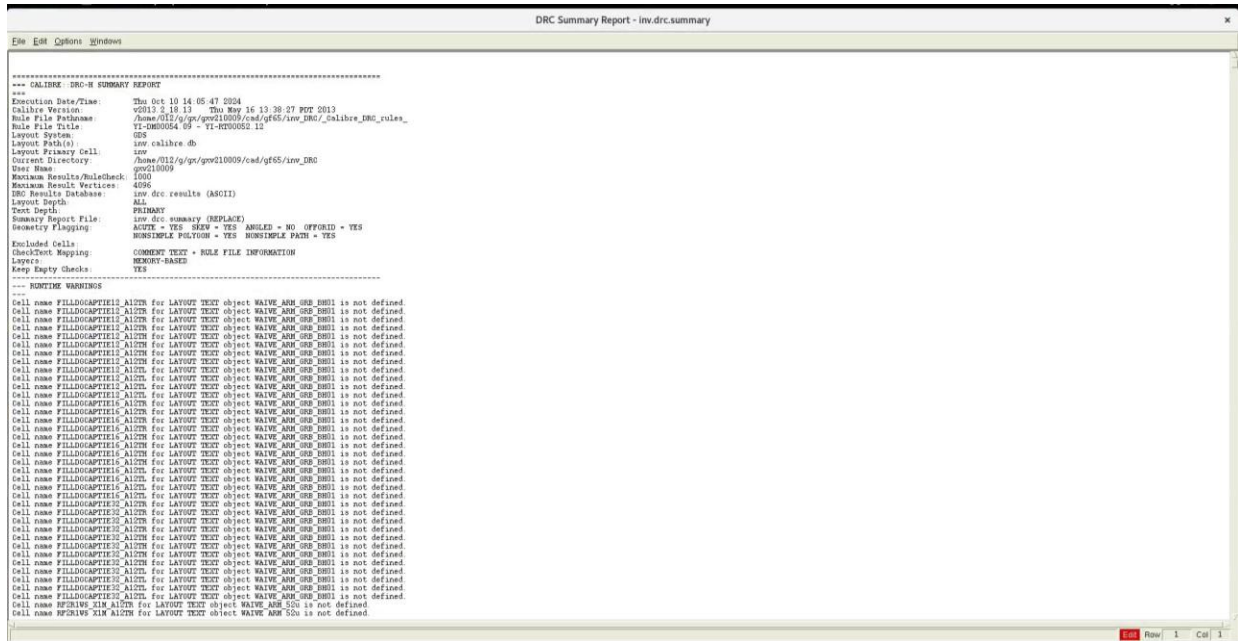


Figure 4. DRC Summary Report

LVS CHECK (LAYOUT VERSUS SCHEMATIC CHECK):

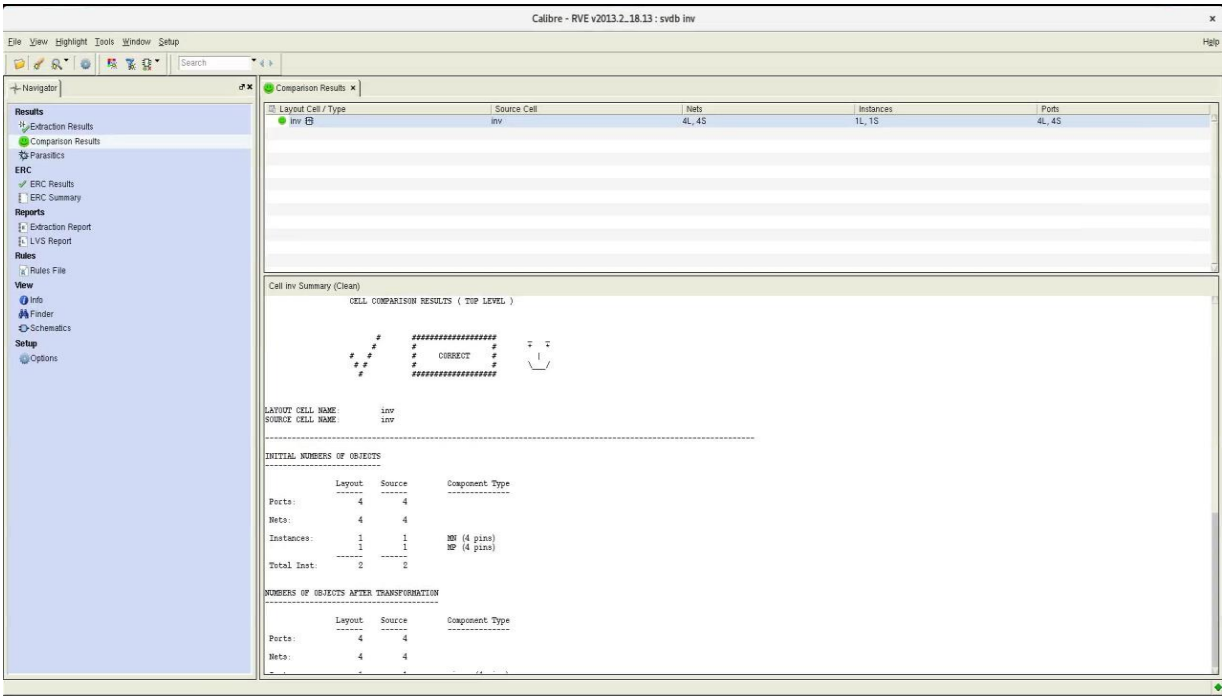


Figure 5. Layout VS Schematic Check

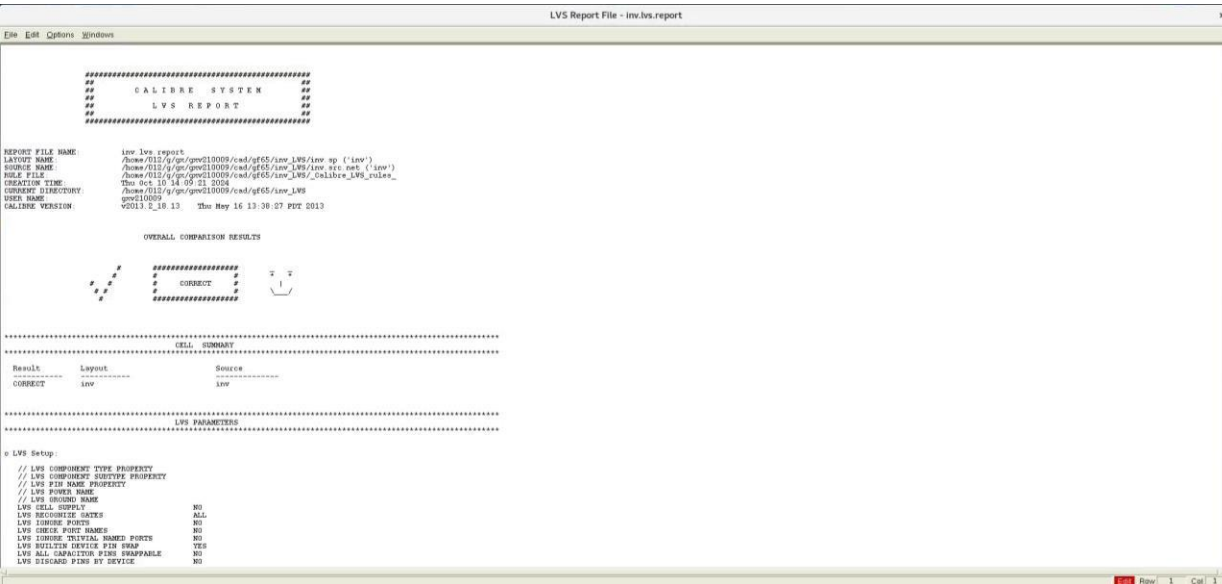
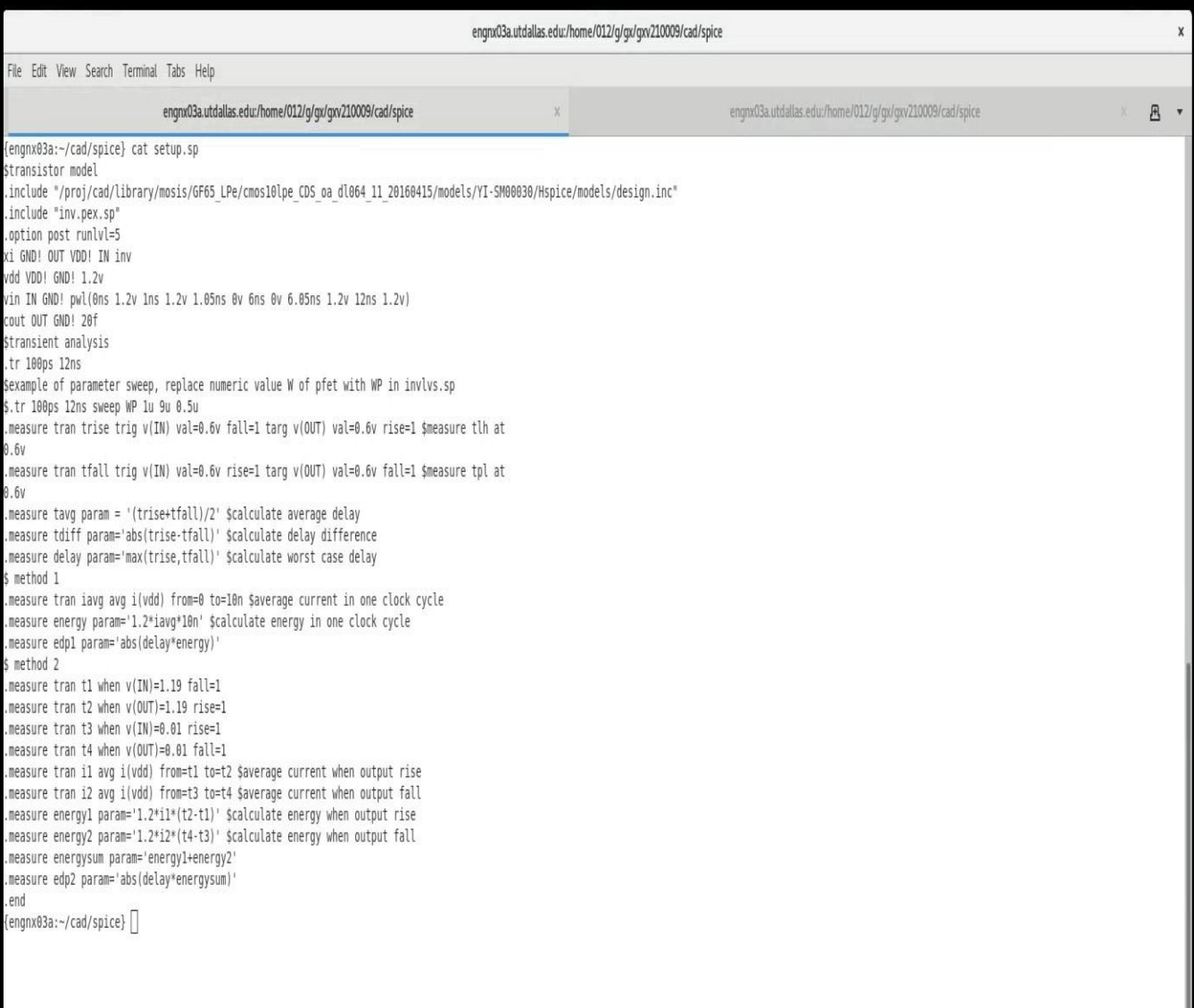


Figure 6. LVS Report

SPICE TEST SETUP FILE:



```
{engnx03a:~/cad/spice} cat setup.sp
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_d1064_11_20160415/models/Y1-SM00830/Hspice/models/design.inc"
.include "inv.pex.sp"
.option post runlvl=5
xi GND! OUT VDD! IN inv
vdd VDD! GND! 1.2v
vin IN GND! pwl(0ns 1.2v 1ns 1.2v 1.05ns 0v 6ns 0v 6.05ns 1.2v 12ns 1.2v)
cout OUT GND! 20f
$transient analysis
.tr 100ps 12ns
$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
$.tr 100ps 12ns sweep WP 1u 9u 0.5u
.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $measure t1h at
0.6v
.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 $measure t1l at
0.6v
.measure tavg param = '(trise+tfall)/2' $calculate average delay
.measure tdiff param='abs(trise-tfall)' $calculate delay difference
.measure delay param='max(trise,tfall)' $calculate worst case delay
$ method 1
.measure tran iavg avg i(vdd) from=0 to=10n $average current in one clock cycle
.measure energy param='1.2*iavg*10n' $calculate energy in one clock cycle
.measure edp1 param='abs(delay*energy)'
$ method 2
.measure tran t1 when v(IN)=1.19 fall=1
.measure tran t2 when v(OUT)=1.19 rise=1
.measure tran t3 when v(IN)=0.01 rise=1
.measure tran t4 when v(OUT)=0.01 fall=1
.measure tran i1 avg i(vdd) from=t1 to=t2 $average current when output rise
.measure tran i2 avg i(vdd) from=t3 to=t4 $average current when output fall
.measure energy1 param='1.2*i1*(t2-t1)' $calculate energy when output rise
.measure energy2 param='1.2*i2*(t4-t3)' $calculate energy when output fall
.measure energysum param='energy1+energy2'
.measure edp2 param='abs(delay*energysum)'
.end
{engnx03a:~/cad/spice} □
```

Figure 7. Inverter SPICE Test Setup File

INPUT AND OUTPUT WAVEFORMS:

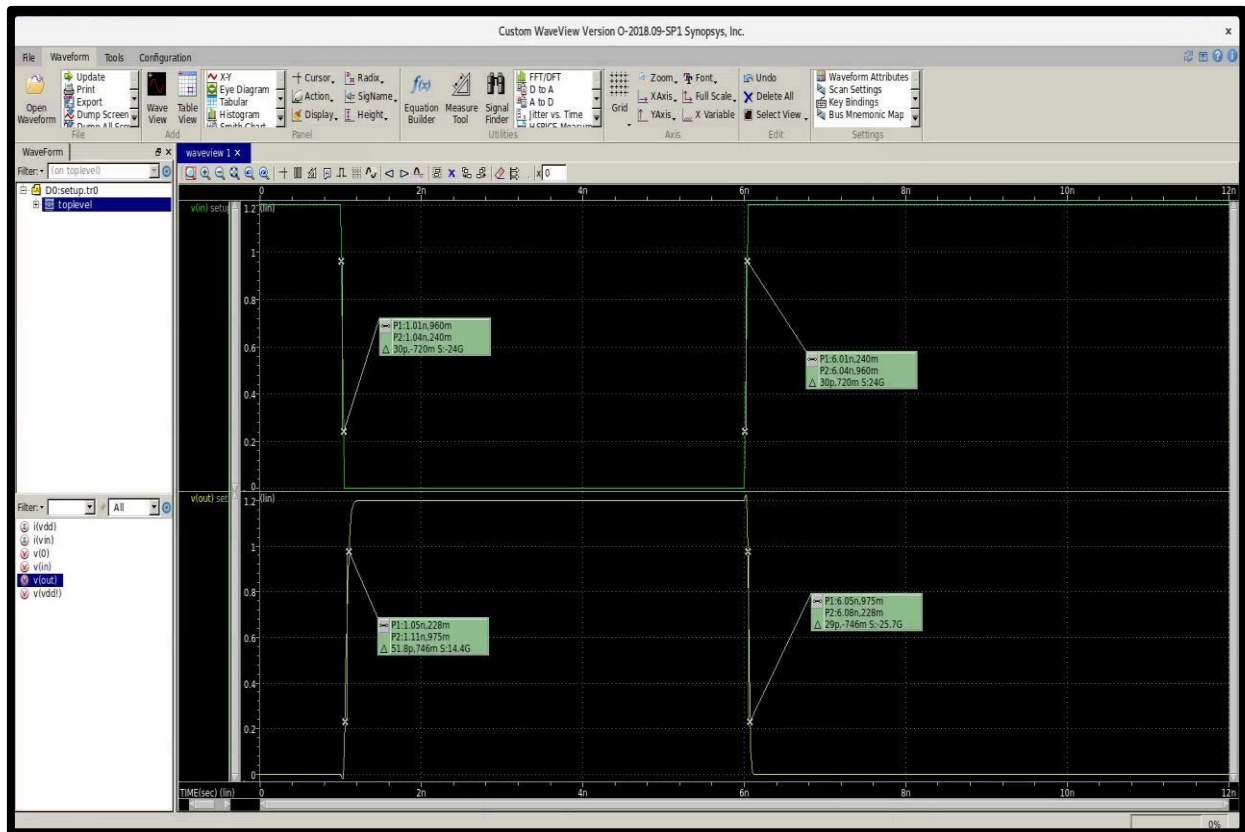


Figure 8. Waveforms representing the Slew Rate for both Input and Output

The slew rate for the input waveform is 30 ps. Slew rate is defined as the time it takes for the input signal to transition from low ($0.2 \times VDD$) to high ($0.8 \times VDD$) and vice versa.

For the output waveform:

- The rising edge slew is 51.8 ps.
- The falling edge slew is 29 ps.

Calculations:

- Output rising edge rate = $(P2 - P1) / 51.8 \text{ ps} = (975 \text{ mV} - 228 \text{ mV}) / 51.8 \text{ ps} = 14.42 \text{ mV/ps}$
- Output falling edge rate = $(P1 - P2) / 29 \text{ ps} = (975 \text{ mV} - 228 \text{ mV}) / 29 \text{ ps} = 25.75 \text{ mV/ps}$

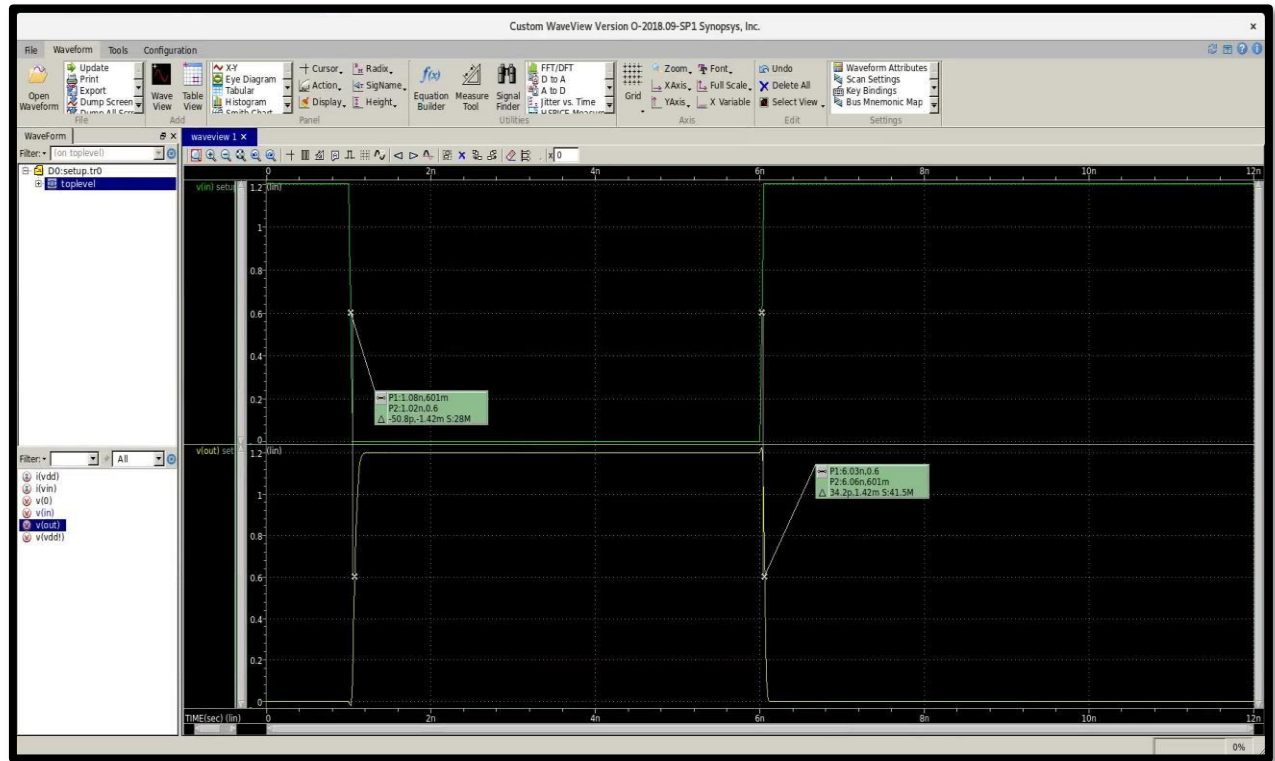


Figure 9. t_{LH} and t_{HL} Waveforms

OUTPUT METRICES:

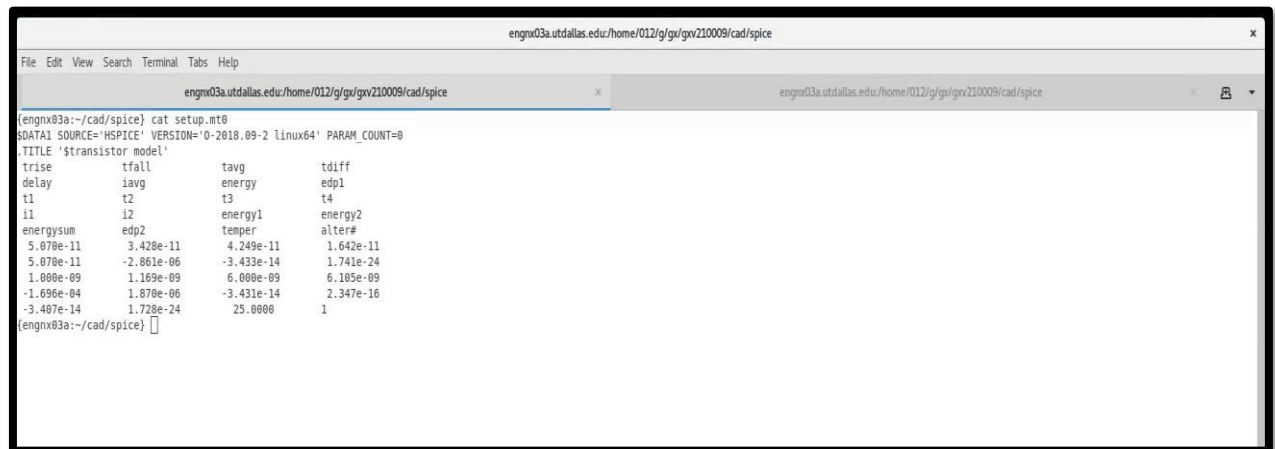


Figure 10. Parameters and their corresponding values

EXTRACTED SPICE NETLIST:

```
PEX Netlist File - /home/012/g/gx/gxv210009/cad/gf65/inv_LVS/inv.pex.sp
File Edit Options Windows
* File: /home/012/g/gx/gxv210009/cad/gf65/inv_LVS/inv.pex.sp
* Created: Thu Oct 10 13:41:39 2024
* Program: Calibre xRC
* Version: v2013.2_18.13
*
* include "/home/012/g/gx/gxv210009/cad/gf65/inv_LVS/inv.pex.sp.pex"
* subckt inv GND! OUT VDD! IN
*
* IN IN
* VDD! VDD!
* OUT OUT
* GND! GND!
XDD_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=3.52002e-12
* PEXIM=3 215e-06
XGND0 N_OUT_M0P0_d N_IN_M0P0_g N_GND!_M0P0_s N_GND!_D0_noxref_pos NFET L=6.5e-08
* V=1.5e-06 AD=2.475e-13 AS=2.415e-13 PD=3.33e-06 PS=3.322e-06 NRQ=0.0673333
* NRS=0.0673333 N=1 NF=1 CNR_SWITCH=0 PCORIT=0 PAR=1 PTWELL=0 SA=1.61e-07
* SE=1.65e-07 SD=0 PANW1=0 PANW2=0 PANW3=7.15e-16 PANW4=3.85e-15 PANW5=3.25e-15
* PANW6=6.5e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=2.6e-14 PANW10=3.1785e-14
XGND0 N_OUT_M0P0_d N_IN_M0P0_g N_VDD!_M0P0_s N_VDD!_D0_noxref_neg PFET L=6.5e-08
* V=1.9e-06 AD=3.135e-13 AS=3.059e-13 PD=4.13e-06 PS=4.122e-06 NRQ=0.0531579
* NRS=0.0531579 N=1 NF=1 CNR_SWITCH=0 PCORIT=0 PAR=1 PTWELL=1 SA=1.61e-07
* SE=1.65e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=2.795e-15 PANW5=3.25e-15
* PANW6=1.02605e-13 PANW7=1.78e-13 PANW8=2.6e-14 PANW9=5.2e-14 PANW10=7.8e-14
*
* include "/home/012/g/gx/gxv210009/cad/gf65/inv_LVS/inv.pex.sp.INV.pxi"
*
ends
*
*
```

Figure 11. Inverter Parasitic Capacitance and Resistance Values Extraction File