

## OBJECTIVE

The objective of this project is to design a custom cell library containing at least eight different combinational standard cells. Schematics, layouts, and waveform simulations, along with abstract views of these cells, were created using tools such as Cadence Virtuoso and HSPICE. The cells included in this project are: INV, NAND2, NOR2, NAND3, NOR3, AOI332, OAI4331, and a complex 11-input circuit with the functionality defined as:

$$F = \text{NOT}[(B | H) \& (E | J) D] | [(A | (C \& K)) \& (F | G | I)]$$

All cells were designed and optimized with a height that is nine times the pitch, resulting in a final cell height of 3.312  $\mu\text{m}$ . The layout was designed to minimize the overall area. The channel length for this design is set to 62 nm. The offset and pin pitch are 0.552  $\mu\text{m}$  and 0.368  $\mu\text{m}$ , respectively, while the width of the PMOS ( $W_p$ ) is 0.72  $\mu\text{m}$  and the width of the NMOS ( $W_n$ ) is 0.52  $\mu\text{m}$ . The height of the PMOS diffusion accommodates four contacts, and the NMOS diffusion accommodates three contacts, satisfying the project requirements.

As specified in the project guidelines, all inputs of the cells maintain a slew rate of 30 ps, verified for both rising and falling edges in the HSPICE waveform simulations. A load capacitance of 55 fF was assumed during these simulations. There were no errors during the Design Rule Check (DRC), Layout vs. Schematic (LVS), and Parasitic Extraction (PEX) for each individual cell. Furthermore, when the cells are placed adjacent to one another in a horizontal row, they successfully pass the DRC. A separate .lib file was generated for this project using PrimeLib by Synopsys.

# INVERTER

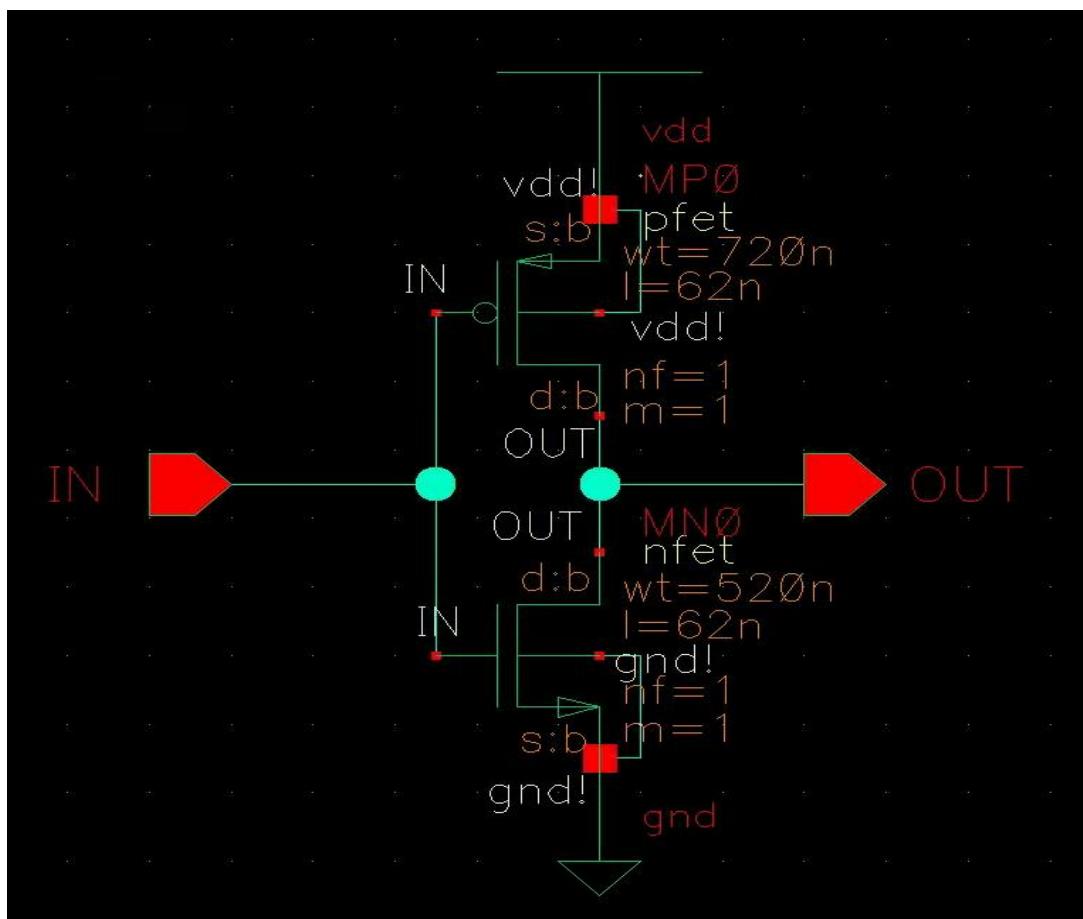
## Function

$$\text{OUT} = \text{NOT } (\text{A})$$

## Truth Table

INPUT (A)	OUTPUT
1	0
0	1

## Schematic

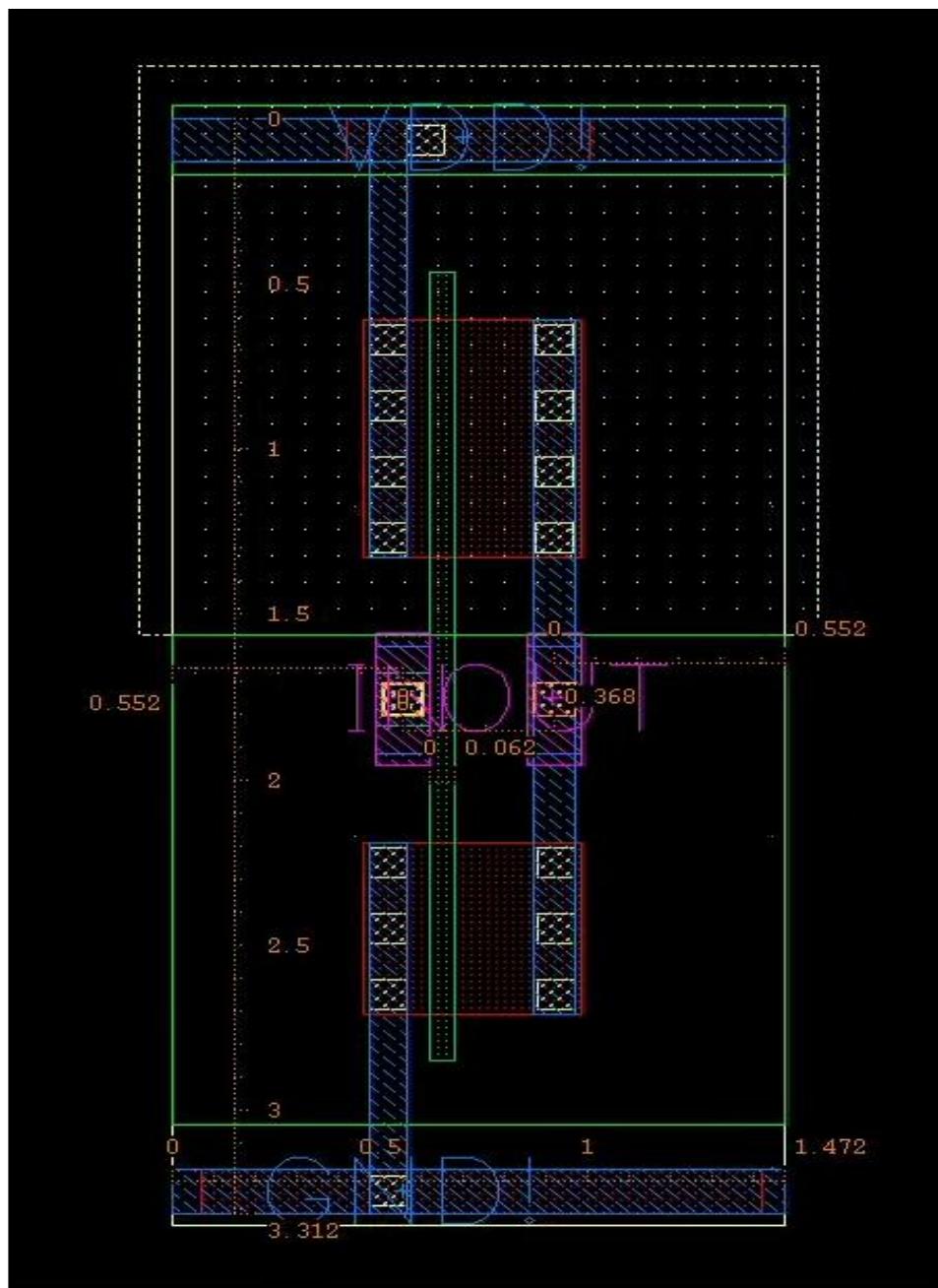


## Layout

Cell Height = 3.312 um

Cell Width = 1.472 um

Total Cell Area = 4.875 um<sup>2</sup>



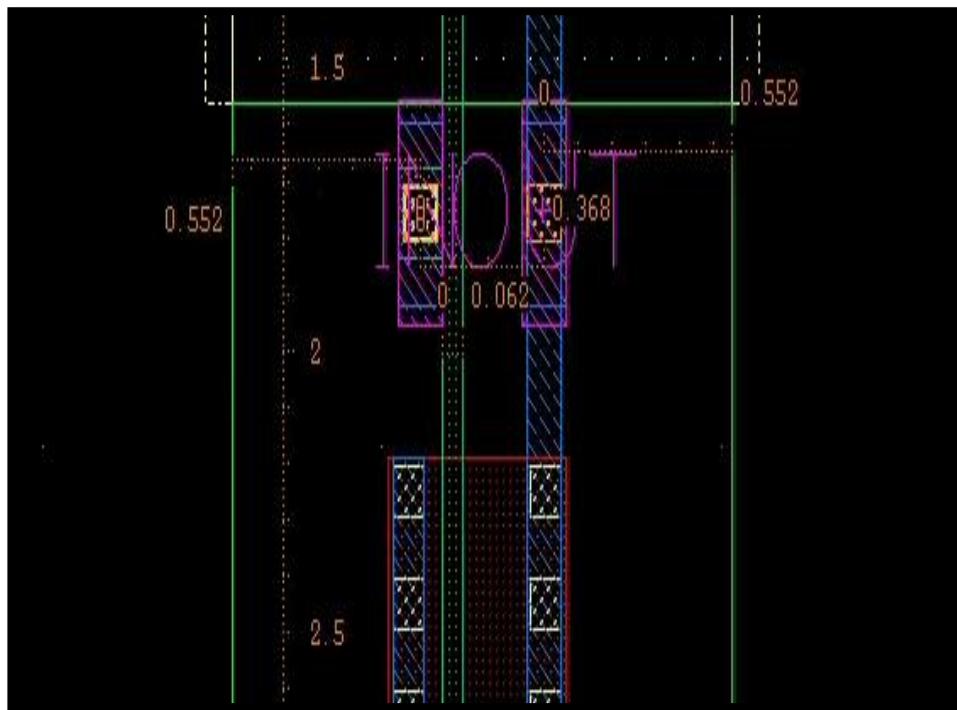
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um

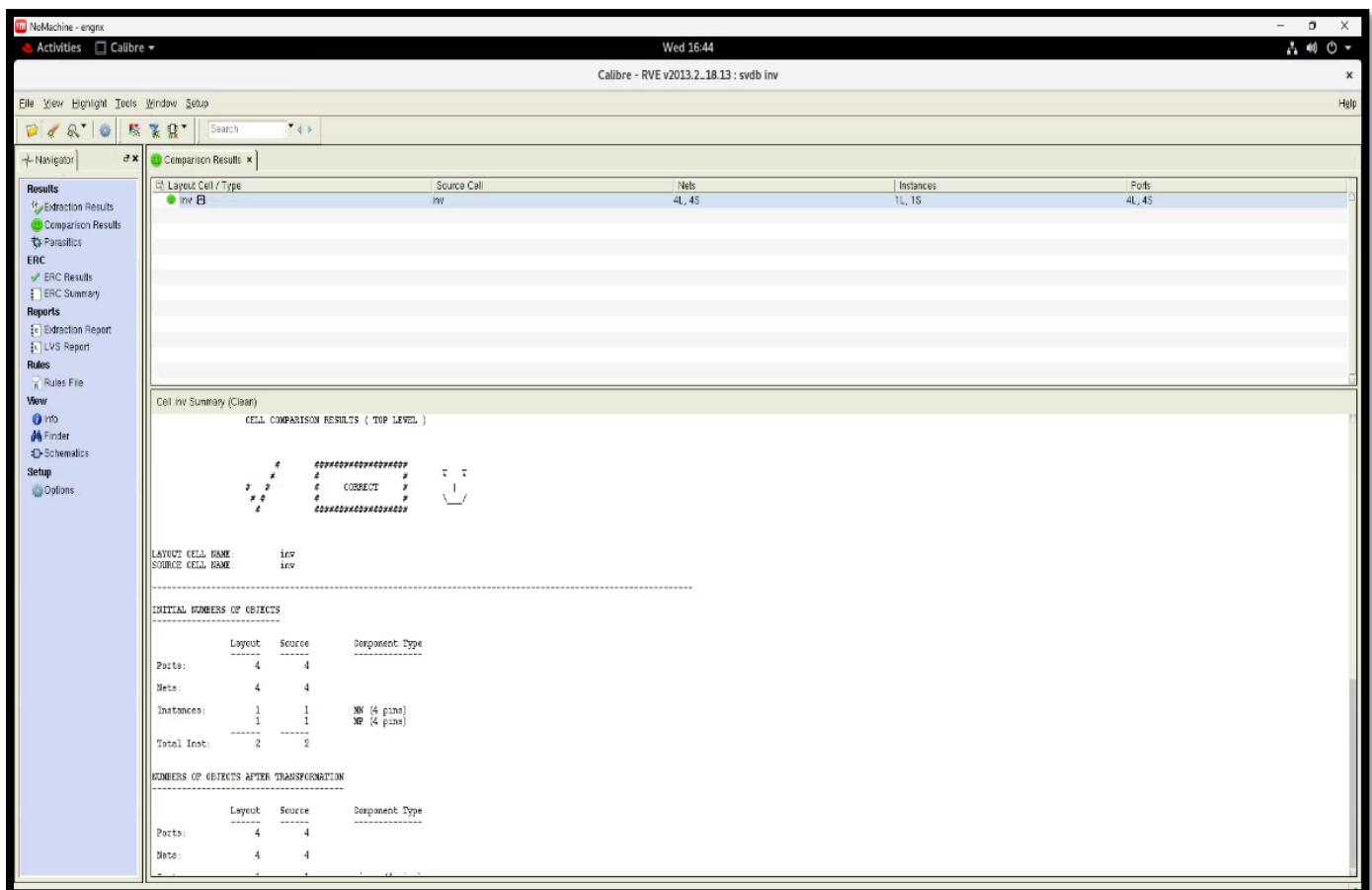


## DRC

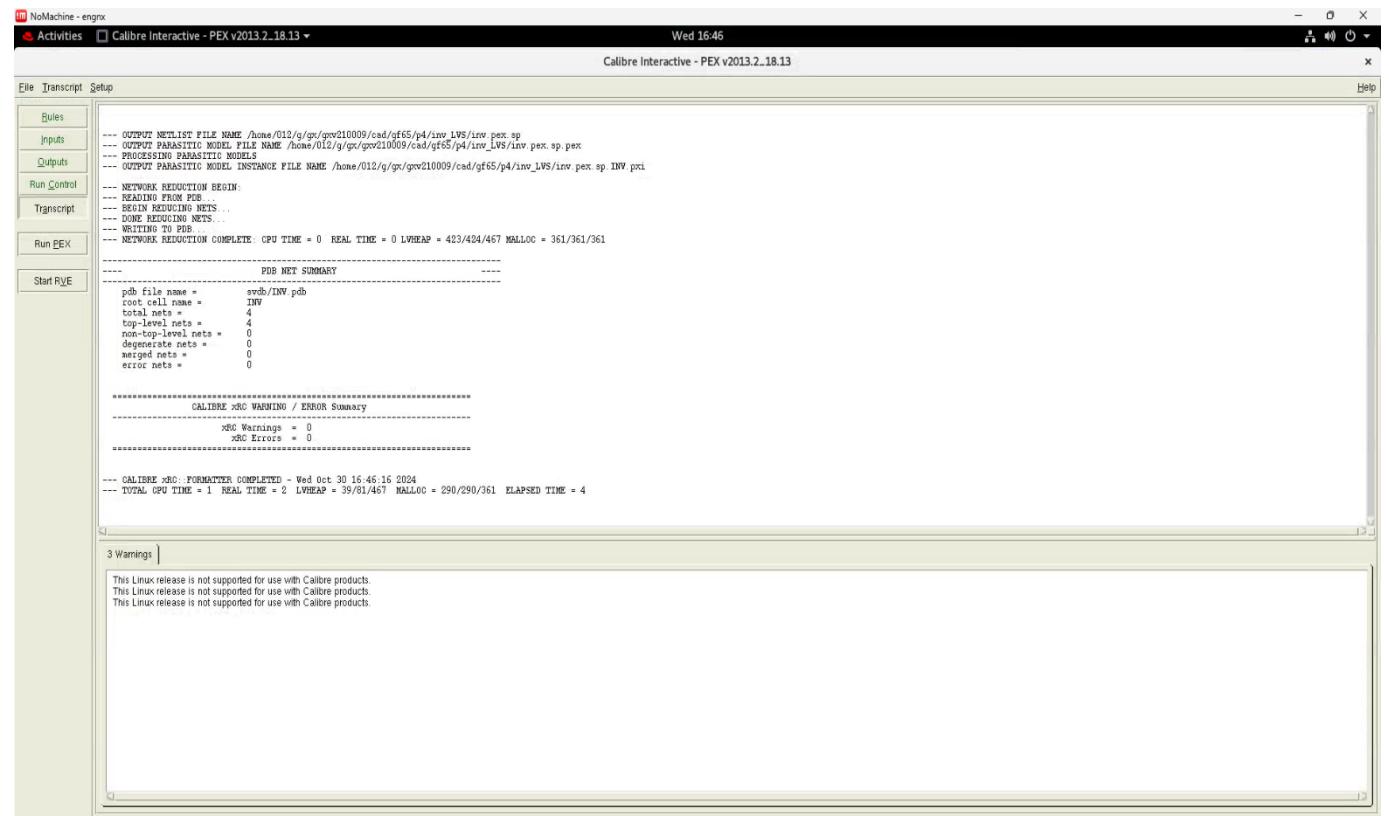
The screenshot shows the Calibre DRC tool interface. The title bar reads "Calibre - RVE v2013.2..18.13 : inv.drc.results" and the status bar shows "Wed 16:43". The menu bar includes File, View, Highlight, Tools, Window, Setup, and Help. The toolbar contains icons for opening files, saving, zooming, and search. The main window displays a tree view of checks under "Check / Cell" and a table titled "Results" showing 0 results for 2070 checks. The table has columns for "Check" and "Results". A message at the bottom states: "Rule File Pathname: /home/012/g/grc210009/cad/gf65/p4/inv\_DRC/\_Calibre\_DRC\_rules\_ Rule File Title: YI-RDN0054\_09 - YI-RDN0052\_12 Shapes with acute angles are prohibited (Except for PROTECT Layer)".

Check	Results
Check GR52	0
Check GR58	0
Check GRB_BF01	0
Check GRSRB_BF01	0
Check GRB_BF02	0
Check GRB_BF03	0
Check GRB_BF04	0
Check GRB_BH01	0
Check GRB_BH02	0
Check GRSRB_BH02	0
Check GRB_BH03	0
Check GRB_BH04	0
Check GRSRB_BH04	0
Check GRB_DE01	0
Check GRB_DE02	0
Check GRB_DE03	0
Check GRB_DE04	0
Check GRB_DF01	0
Check GRB_DF02	0
Check GRB_DF03	0
Check GRB_DF04	0
Check GRB_JN01	0

# LVS



# PEX



# PEX Netlist

```
* File: /home/012/g/gx/gxv210009/cad/gf65/p4/inv_LVS/inv.pex.sp
* Created: Tue Oct 29 11:13:44 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "/home/012/g/gx/gxv210009/cad/gf65/p4/inv_LVS/inv.pex.sp.pex"
.subckt inv GND! OUT VDD! IN
*
* IN     IN
* VDD!   VDD!
* OUT    OUT
* GND!   GND!
XDO_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=2.17408e-12
+ PERIM=5.968e-06
XMMN0 N OUT MMN0 d N IN MMN0 g N_GND! MMN0_s N_GND! D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=1.5912e-13 AS=8.32e-14 PD=1.652e-06 PS=1.36e-06 NRD=0.465385
+ NRS=0.192308 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=3.06e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMP0 N OUT MMP0 d N IN MMP0 g N_VDD! MMP0_s N_GND! D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=2.2032e-13 AS=1.152e-13 PD=2.052e-06 PS=1.76e-06 NRD=0.334722
+ NRS=0.138889 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07
+ SB=3.06e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=5.9148e-14 PANW8=2.1948e-14 PANW9=2.48e-14
+ PANW10=5.332e-15
*
.include "/home/012/g/gx/gxv210009/cad/gf65/p4/inv_LVS/inv.pex.sp.INV.pxi"
*
.ends
*
*
```

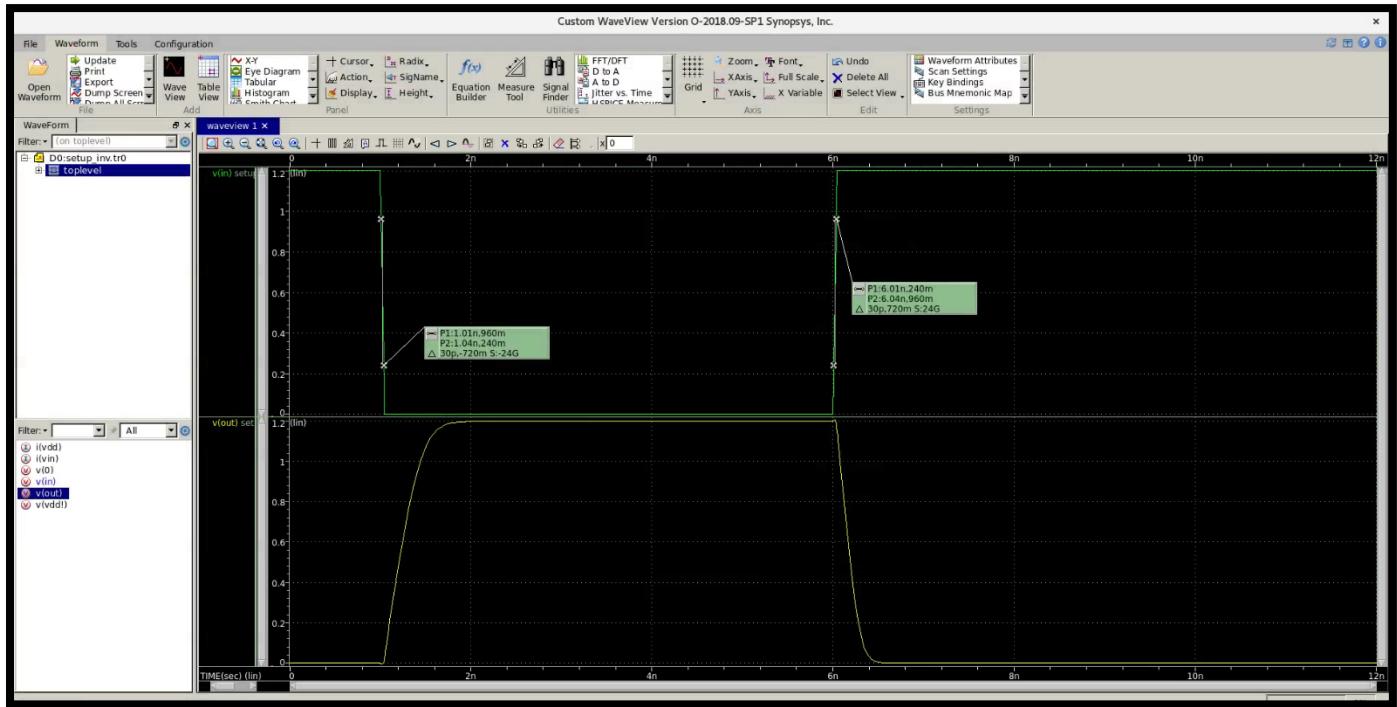
Plain Text ▾ Tab Width: 8 ▾ Ln 1, Col 1 ▾ INS

# HSpice setup file

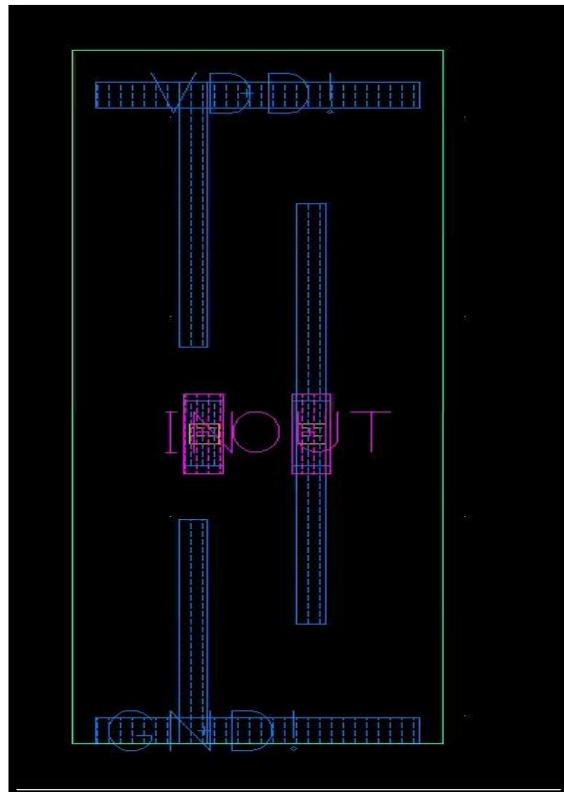
```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "inv.pex.sp"
.option post runlvl=5
xi GND! OUT VDD! IN inv
vdd VDD! GND! 1.2v
vin IN GND! pwl(0ns 1.2v 1ns 1.2v 1.05ns 0v 6ns 0v 6.05ns 1.2v 12ns 1.2v)
cout OUT GND! 55f
$transient analysis
.tr 100ps 12ns
$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
$.tr 100ps 12ns sweep WP 1u 9u 0.5u
.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $measure tlh at 0.6v
.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 $measure tpl at 0.6v
.measure tavg param = '(trise+tfall)/2' $calculate average delay
.measure tdiff param='abs(trise-tfall)' $calculate delay difference
.measure delay param='max(trise,tfall)' $calculate worst case delay
$ method 1
.measure tran iavg avg i(vdd) from=0 to=10n $average current in one clock cycle
.measure energy param='1.2*iavg*10n' $calculate energy in one clock cycle
.measure edpi param='abs(delay*energy)'
$ method 2
.measure tran t1 when v(IN)=1.19 fall=1
.measure tran t2 when v(OUT)=1.19 rise=1
.measure tran t3 when v(IN)=0.01 rise=1
.measure tran t4 when v(OUT)=0.01 fall=1
.measure tran i1 avg i(vdd) from=t1 to=t2 $average current when output rise
.measure tran i2 avg i(vdd) from=t3 to=t4 $average current when output fall
.measure energyl param='1.2*i1*(t2-t1)' $calculate energy when output rise
.measure energy2 param='1.2*i2*(t4-t3)' $calculate energy when output fall
.measure energysum param='energyl+energy2'
.measure edp2 param='abs(delay*energysum)'
.end
```

Plain Text ▾ Tab Width: 8 ▾ Ln 9, Col 17 ▾ INS

## Simulation Waveform



## Abstract View



## NAND2

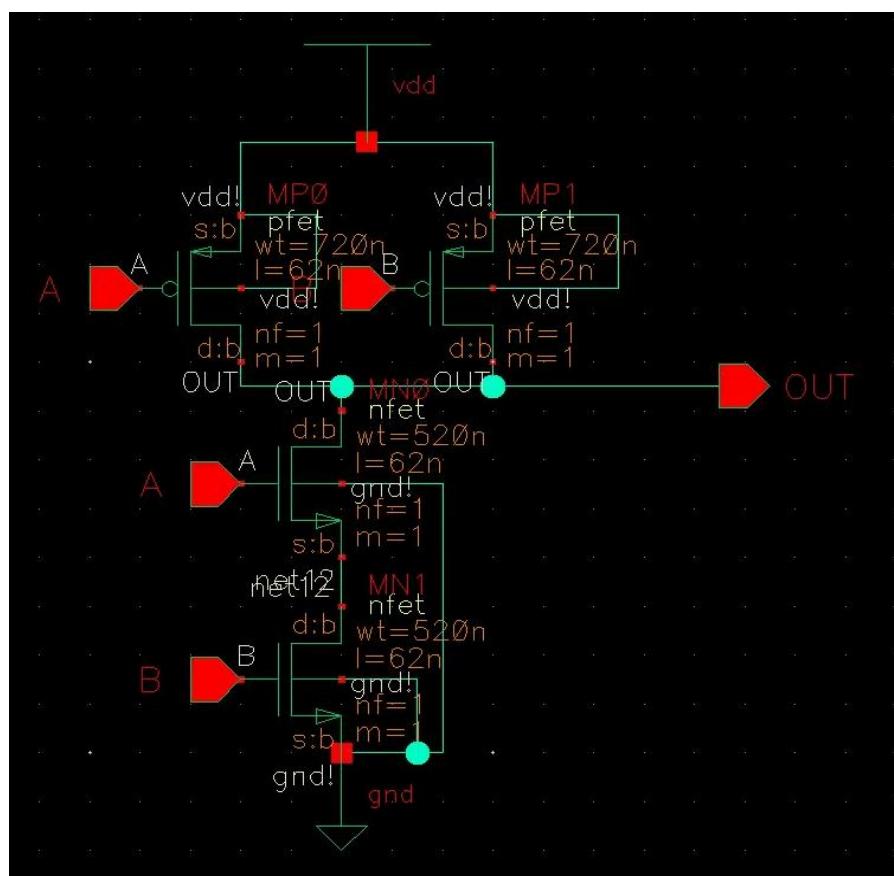
### Function

$$\text{OUT} = \text{NOT } (\text{AB})$$

### Truth Table

INPUT (A)	INPUT (B)	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

### Schematic

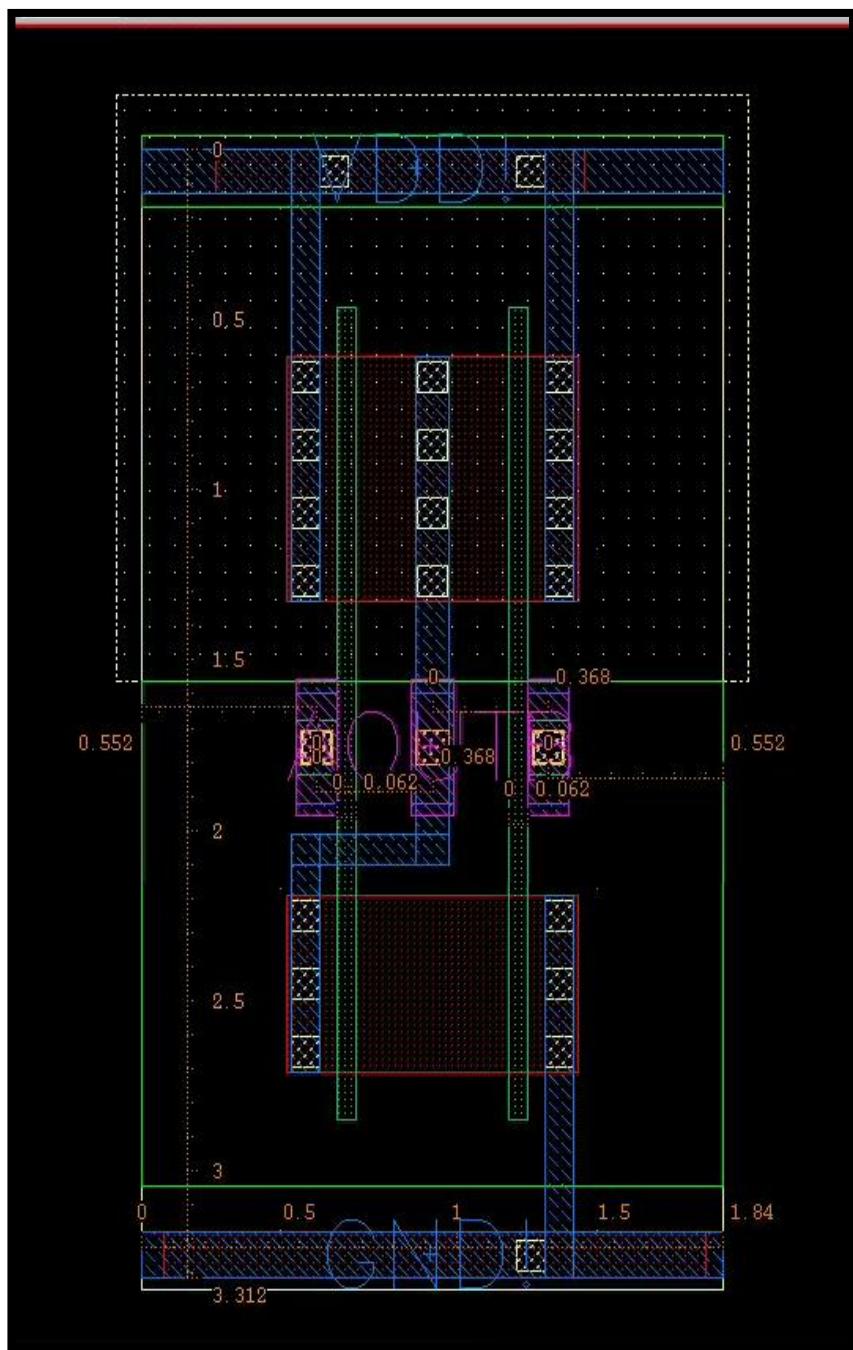


## Layout

Cell Height = 3.312 um

Cell Width = 1.84 um

Total Cell Area = 6.094 um<sup>2</sup>



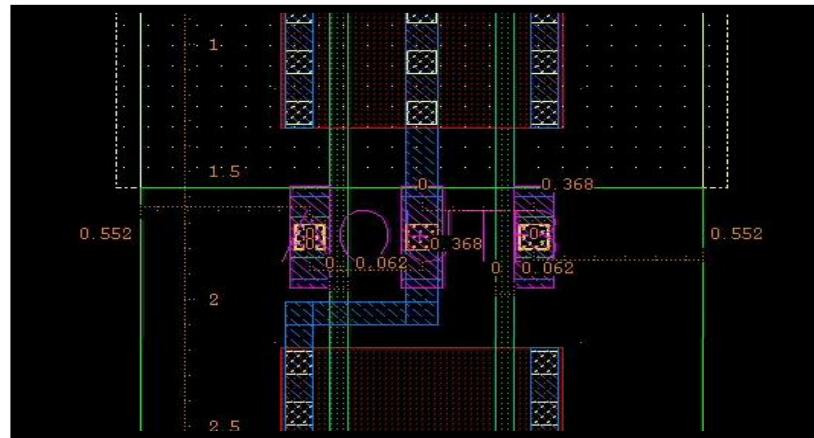
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um



## DRC

NoMachine - engnx

Activities Calibre

Wed 16:50

Calibre - RVE v2013.2\_18.13 : nand2.drc.results

File View Highlight Tools Window Setup Help

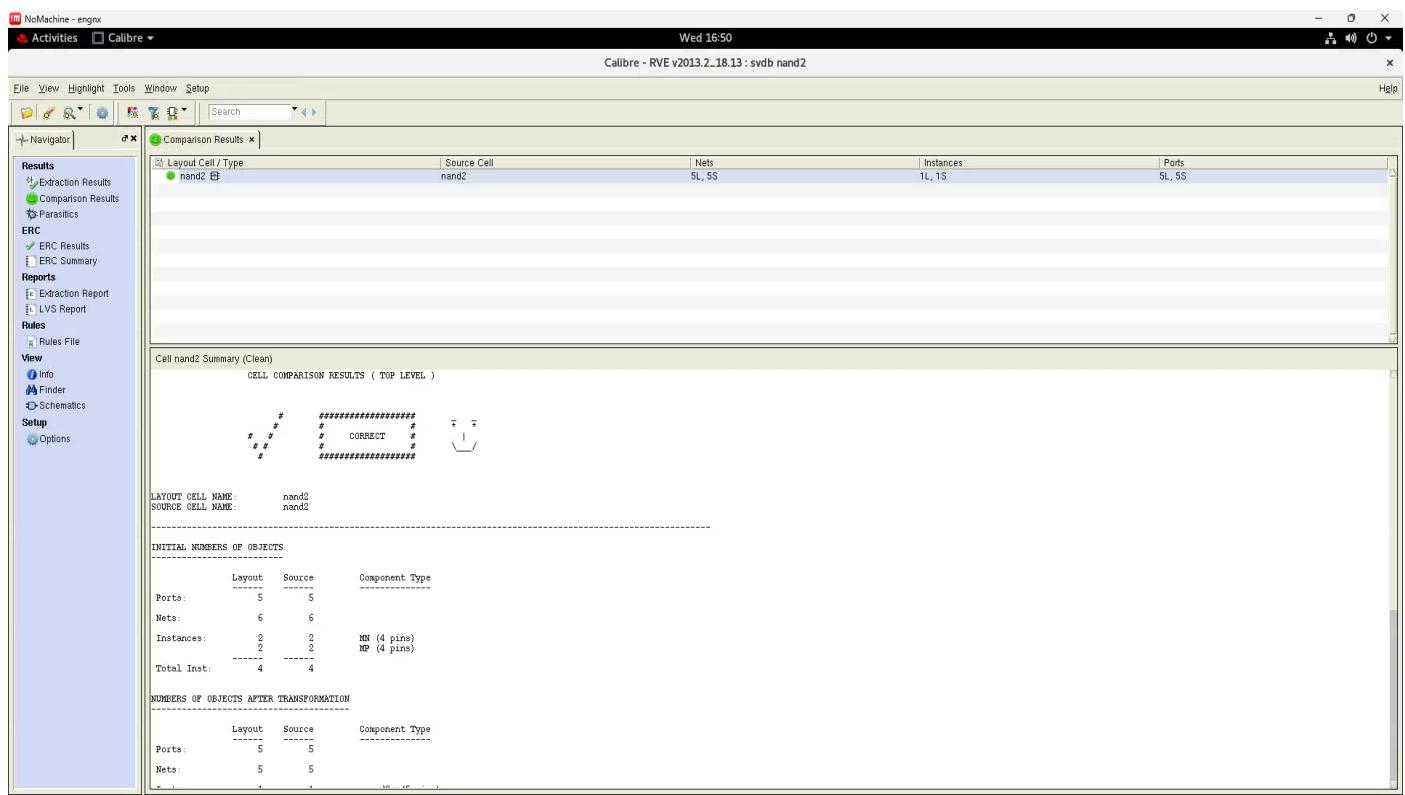
Show All nand2, 0 Results (0 of 2078 Checks)

Check / Cell	Results
✓ Check GRS2	0
✓ Check GR58	0
✓ Check GRB_BF01	0
✓ Check GRSRB_BF01	0
✓ Check GRB_BF02	0
✓ Check GRB_BF03	0
✓ Check GRB_BF04	0
✓ Check GRB_BH01	0
✓ Check GRB_BH02	0
✓ Check GRSRB_BH02	0
✓ Check GRB_BH03	0
✓ Check GRB_BH04	0
✓ Check GRSRB_BH04	0
✓ Check GRB_DE01	0
✓ Check GRB_DE02	0
✓ Check GRB_DE03	0
✓ Check GRB_DE04	0
✓ Check GRB_DF01	0
✓ Check GRB_DF02	0
✓ Check GRB_DF03	0
✓ Check GRB_DF04	0
✓ Check GRB_JN01	0

Rule File Pathname: /home/012/gx/gcv210009/cad/gf65/p4/nand2\_DRC/\_Calibre\_DRC\_rules\_.yml  
Shape File Title: YI-DNU054\_09 - YI-KT0052\_12  
Shapes with acute angles are prohibited (Except for PROTECT Layer)

Check GRS2

## LVS



## PEX



## PEX Netlist

The screenshot shows a terminal window titled "Text Editor" with the file "nand2.pex.sp" open. The file content is a PEX (Post-Extraction) netlist for a NAND2 gate. It includes header information like file creation date (Tue Oct 29 11:15:54 2024), program version ("Calibre xRC" v2013.2\_18.13), and a list of components and their connections. The netlist uses abbreviations like "N\_GND!" for ground and "VDD!" for power. The code is heavily commented with asterisks (\*).

```
* File: /home/012/g/gxv210009/cad/gf65/p4/nand2_LVS/nand2.pex.sp
* Created: Tue Oct 29 11:15:54 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.included "/home/012/g/gxv210009/cad/gf65/p4/nand2_LVS/nand2.pex.sp.pex"
.subckt nand2 OUT GND! VDD! A B
*
* B     B
* A     A
* VDD!  VDD!
* GND!  GND!
* OUT   OUT
XDB_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=2.80704e-12
+ PERIM=6.704e-06
XMMNO N_OUT MMNO_d N_A MMNO_g NET12 N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=8.32e-14 AS=1.2532e-13 PD=1.36e-06 PS=1.002e-06 NRD=0.192308
+ NR5=0.463462 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=7.04e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN1 NET12 N_B MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=1.2532e-13 AS=8.32e-14 PD=1.002e-06 PS=1.36e-06 NRD=0.463462
+ NR5=0.192308 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=7.04e-07
+ SB=1.6e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMP0_N_OUT_MMPO_d N_A MMPO_g N_VDD!_MMPO_s N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.7352e-13 AS=1.152e-13 PD=1.202e-06 PS=1.76e-06 NRD=0.334722
+ NR5=0.138889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07
+ SB=7.04e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=1.4508e-14 PANW8=2.1948e-14
+ PANW9=6.944e-14 PANW10=5.332e-15
XMMP1_N_OUT_MMPO_d N_B MMPO_g N_VDD!_MMPO_s N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.7352e-13 AS=1.152e-13 PD=1.202e-06 PS=1.76e-06 NRD=0.334722
+ NR5=0.138889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=7.04e-07
+ SB=1.6e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=1.4508e-14 PANW8=2.1948e-14
+ PANW9=6.944e-14 PANW10=5.332e-15
```

## HSpice Setup File

The screenshot shows a terminal window titled "Text Editor" with the file "setup.nand2.sp" open. The file content is an HSpice setup script for a NAND2 gate. It includes directives for the transistor model, component inclusion, simulation parameters, and transient analysis. The code uses dollar signs (\$) to denote HSpice commands.

```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "nand2.pex.sp"

.option post runlvl=5

xi OUT GND! VDD! A B nand2

vdd VDD! GND! 1.2v

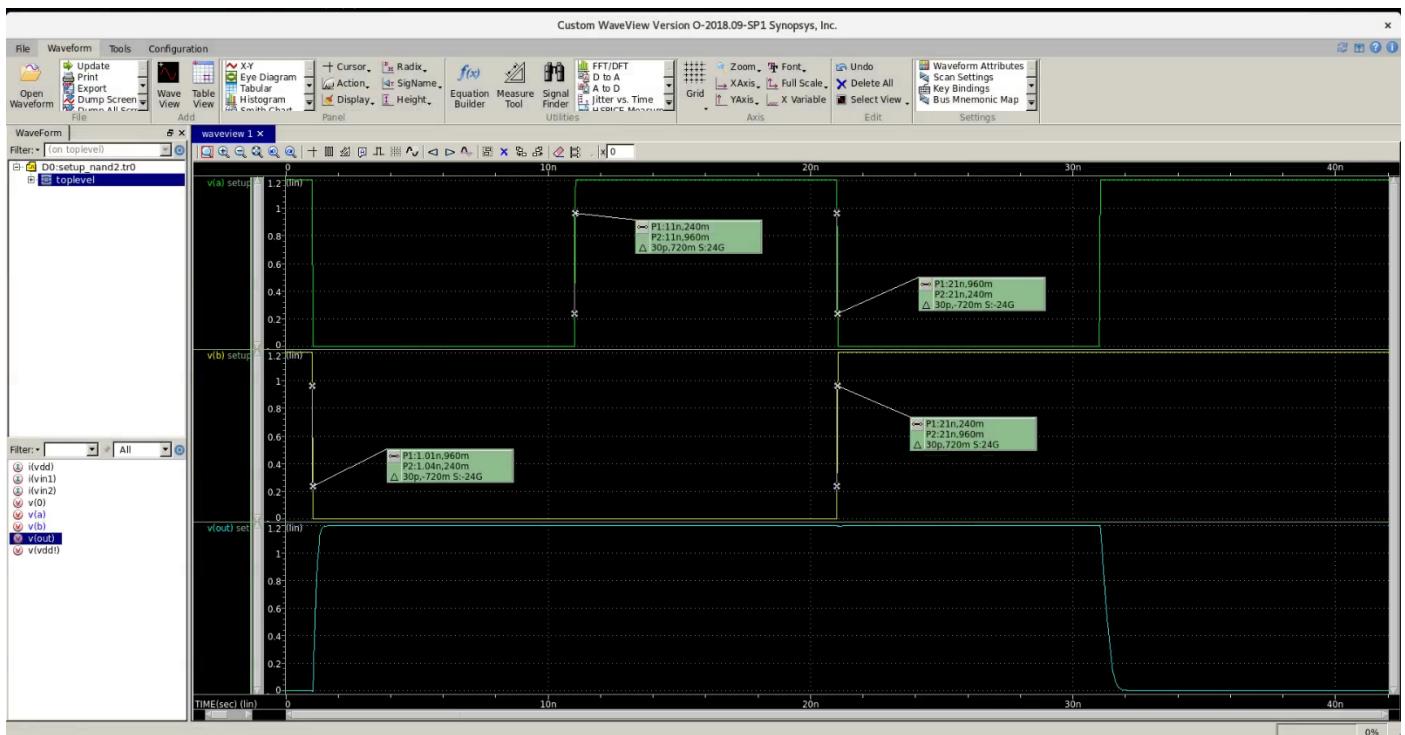
vin1 A GND! pwl(0ns 1.2v 1ns 1.2v 1.05ns 0v 11ns 0v 11.05ns 1.2v 21ns 1.2v 21.05ns 0v 31ns 0v 31.05ns 1.2v 41ns 1.2v)
vin2 B GND! pwl(0ns 1.2v 1ns 1.2v 1.05ns 0v 21ns 1.2v 21.05ns 1.2v 41ns 1.2v)

cout OUT GND! 55f

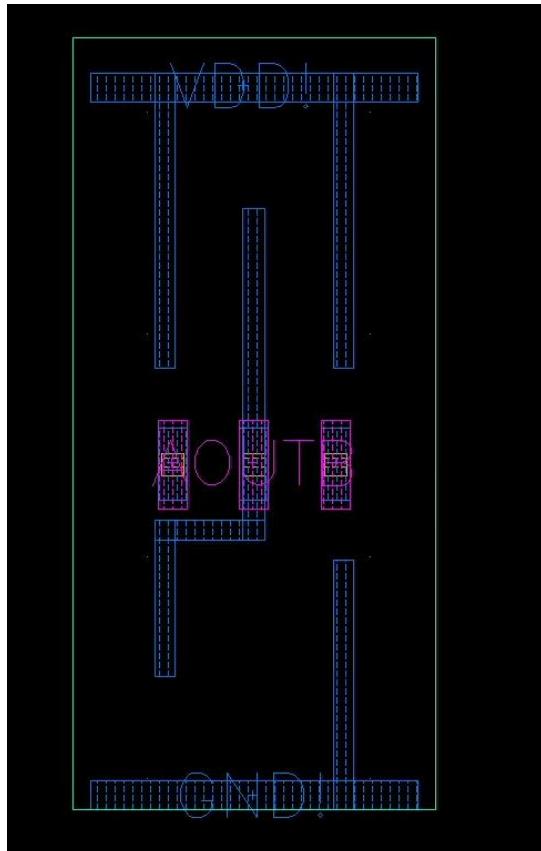
$transient analysis
.tr 100ps 42ns

.end
```

## Simulation Waveform



## Abstract View



## NOR2

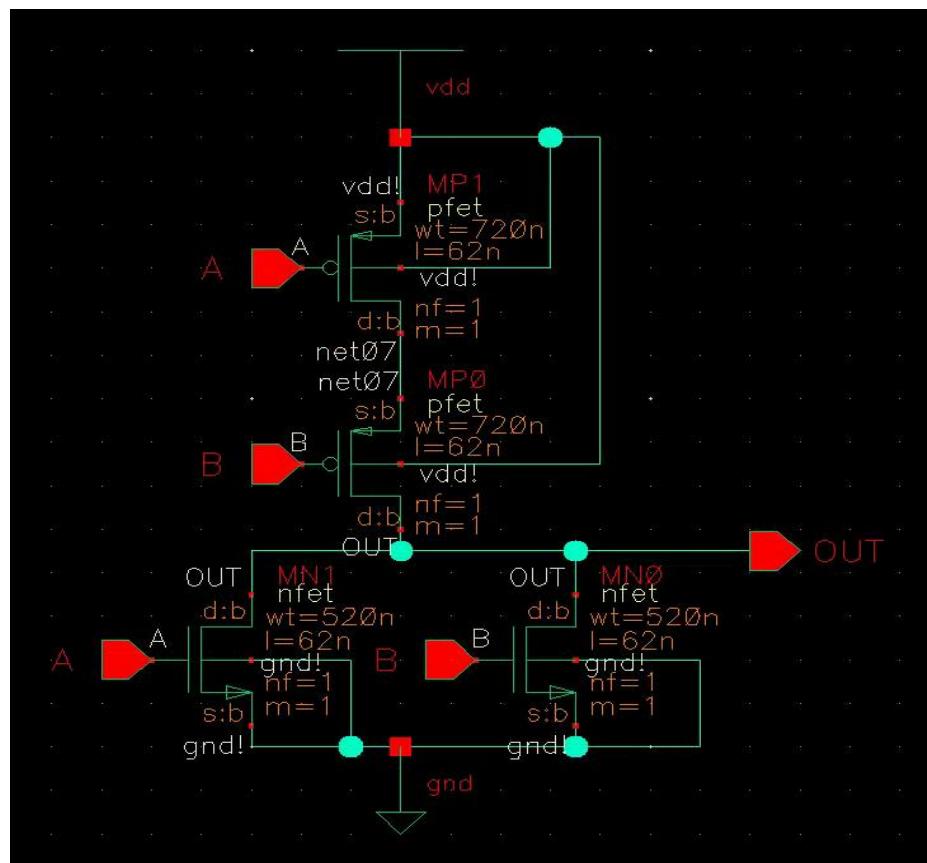
### Function

$$\text{OUT} = \text{NOT } (\text{A} \mid \text{B})$$

### Truth Table

INPUT (A)	INPUT (B)	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

### Schematic

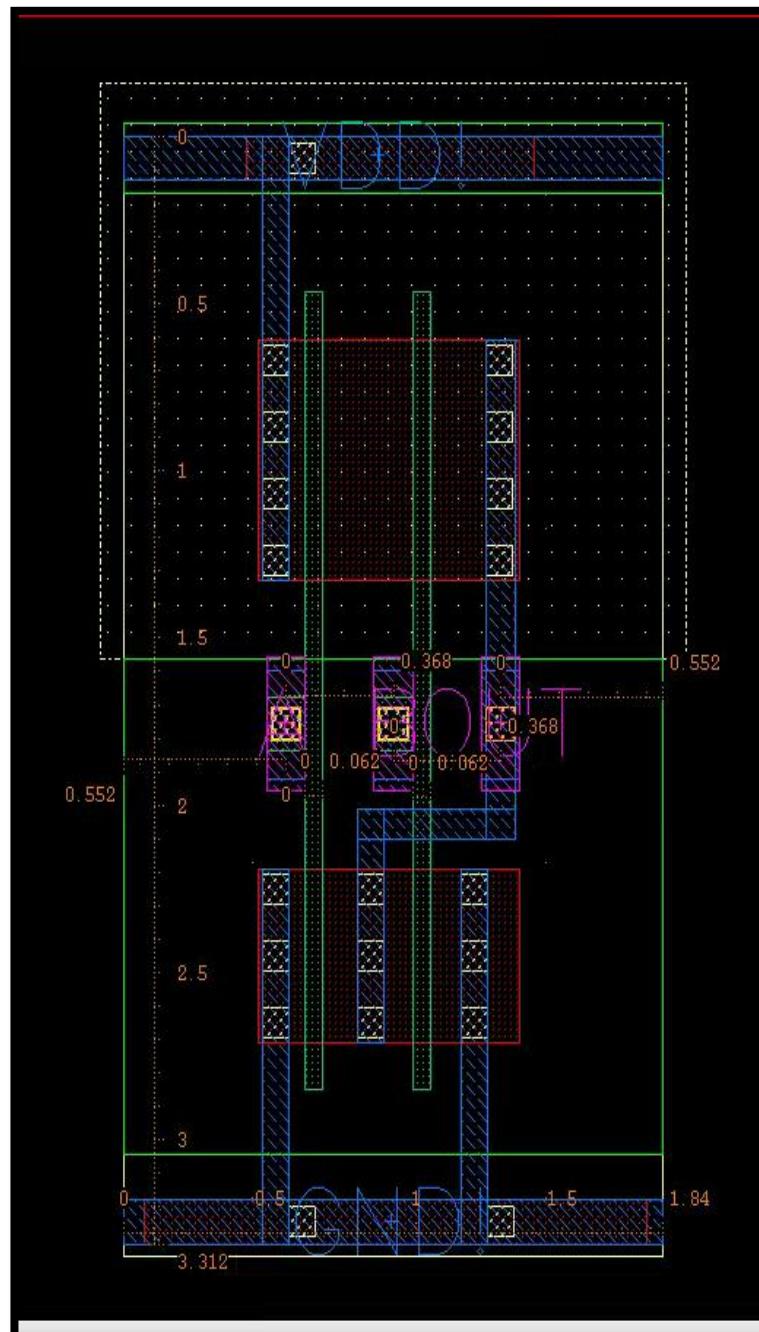


## Layout

Cell Height = 3.312 um

Cell Width = 1.84 um

Total Cell Area = 6.094 um<sup>2</sup>



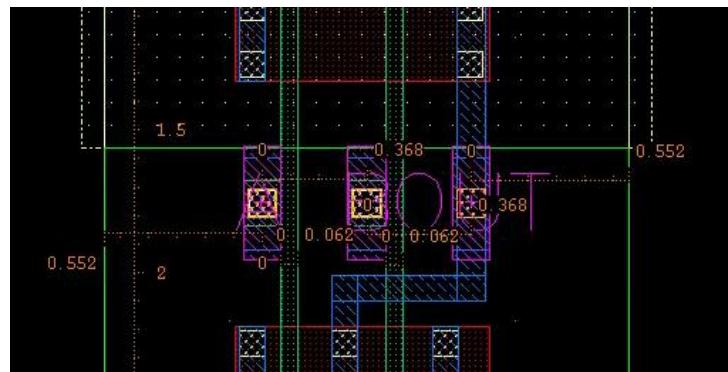
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um



## DRC

Activities Calibre ▾ Wed 19:03  
Calibre - RVE v2013.2\_18.13 : nor2.drc.results

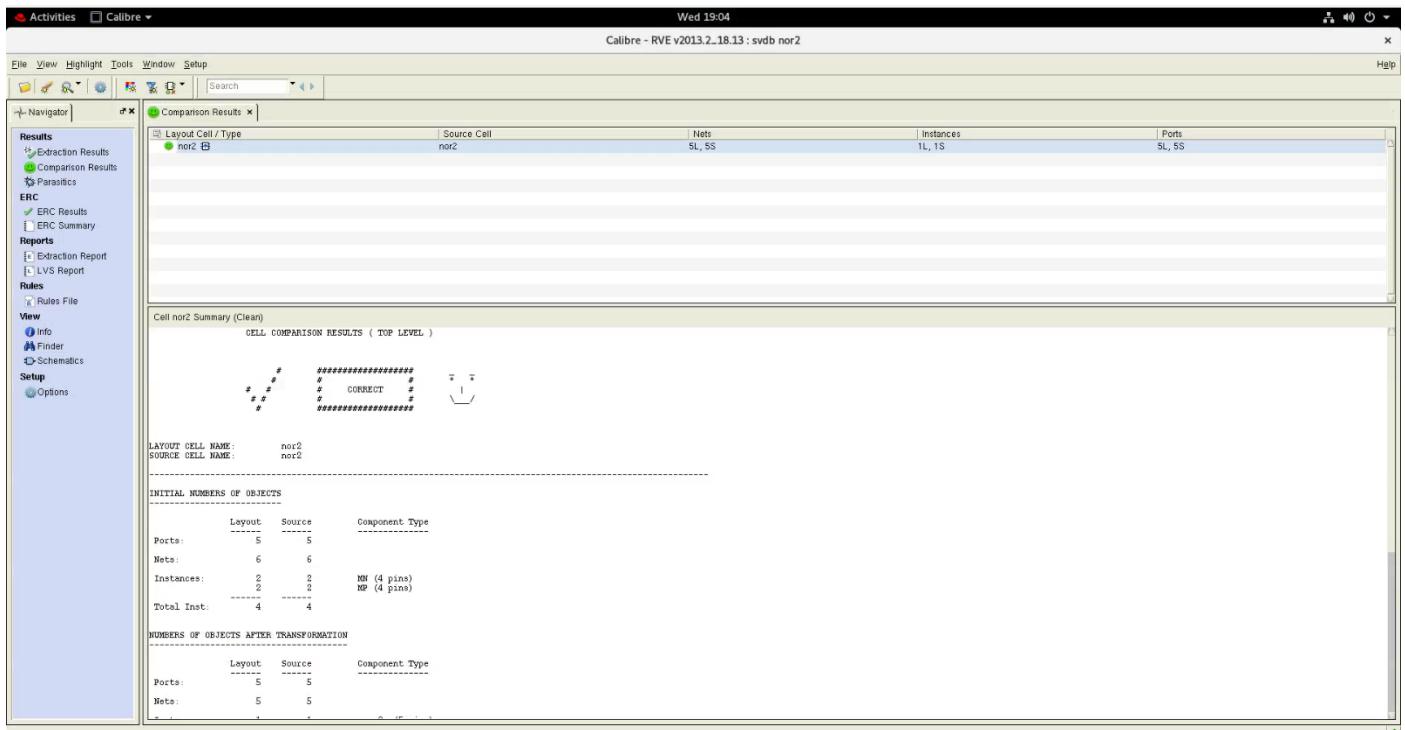
File View Highlight Tools Window Setup Help

Show All: nor2, 0 Results (in 0 of 2078 Checks)

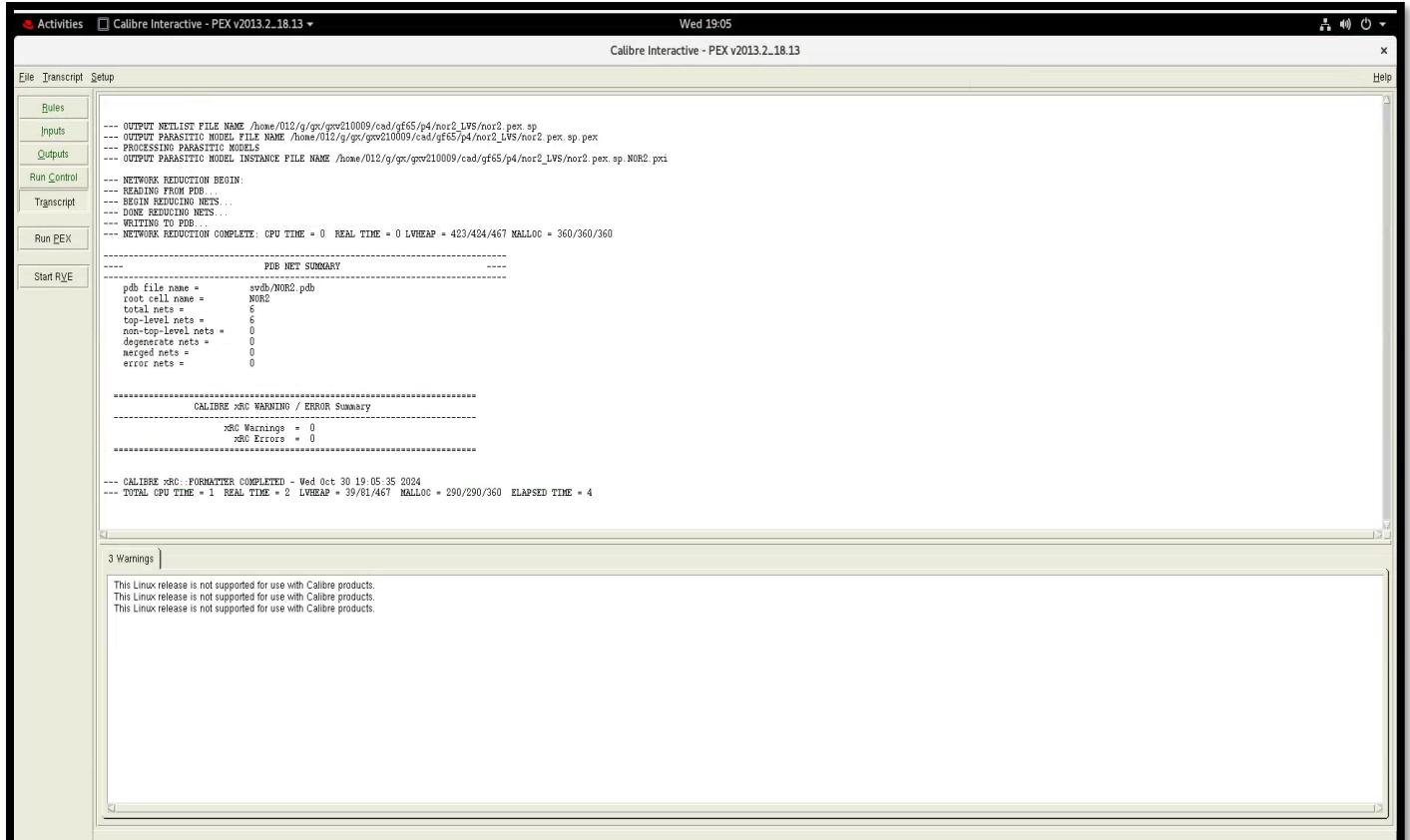
Check / Cell	Results
✓ Check GRS2	0
✓ Check GRS6	0
✓ Check GRB_BF01	0
✓ Check GRBSRB_BF01	0
✓ Check GRB_BF02	0
✓ Check GRB_BF03	0
✓ Check GRB_BF04	0
✓ Check GRB_BH01	0
✓ Check GRB_BH02	0
✓ Check GRSRB_BH02	0
✓ Check GRB_BH03	0
✓ Check GRB_BH04	0
✓ Check GRSRB_BH04	0
✓ Check GRB_DE01	0
✓ Check GRB_DE02	0
✓ Check GRB_DE03	0
✓ Check GRB_DE04	0
✓ Check GRB_DF01	0
✓ Check GRB_DF02	0
✓ Check GRB_DF03	0
✓ Check GRB_DF04	0
✓ Check GRB_JN01	0

Rule File Pathname: /home/012/gx/gcv210009/cad/gf65/p4/nor2\_DRC/\_Calibre\_DRC\_rules\_.rule  
Rule File Title: YI-RD00054.09 - YI-RD00052.12  
Shapes with acute angles are prohibited (Except for PROTECT Layer)

LVS



PEX



## PEX Netlist



```
NoMachine - gdcbm
Fri 13:02
nor2.pex.sp
~/cad/spice/nor2

*.include "/home/012/g/gx/gxv210009/cad/gf65/p4/nor2_LVS/nor2.pex.sp.pex"
.subckt nor2 GND! OUT VDD! A B
*
* B     B
* A     A
* VDD!  VDD!
* OUT   OUT
* GND!  GND!
X00_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=2.80704e-12
+ PERIM=6.704e-06
XMMN1 N_OUT MMN1_d N_A MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=8.32e-14 PD=8.26e-07 PS=1.36e-06 NRD=0.315385
+ NRS=0.192308 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=6.74e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN0 N_OUT MMN0_d N_B MMN0_g N_GND!_MMN0_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=1.5912e-13 PD=8.26e-07 PS=1.652e-06 NRD=0.273077
+ NRS=0.288462 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.28e-07
+ SB=3.06e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMP1 NET07 N_A MMP1_d N_B MMP1_g NET07_N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.1016e-13 AS=1.152e-13 PD=1.026e-06 PS=1.76e-06 NRD=0.2125
+ NRS=0.138889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07
+ SB=6.74e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=1.4508e-14 PANW8=2.1948e-14
+ PANW9=6.944e-14 PANW10=5.332e-15
XMMP0 N_OUT MMP0_d N_B MMP0_g NET07_N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=2.2032e-13 AS=1.1016e-13 PD=2.052e-06 PS=1.026e-06 NRD=0.327778
+ NRS=0.2125 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=5.28e-07
+ SB=3.06e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=6.2e-15 PANW7=5.9148e-14 PANW8=6.6588e-14 PANW9=2.48e-14
+ PANW10=5.332e-15
*
*.include "/home/012/g/gx/gxv210009/cad/gf65/p4/nor2_LVS/nor2.pex.sp.NOR2.pxi"
*
.ends
```

## HSpice Setup File



```
NoMachine - gdcbm
Fri 13:02
setup_nor2.sp
~/cad/spice/nor2

$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "nor2.pex.sp"

.option post runlvl=5

xi GND! OUT|VDD! A B nor2

vdd VDD! GND! 1.2v

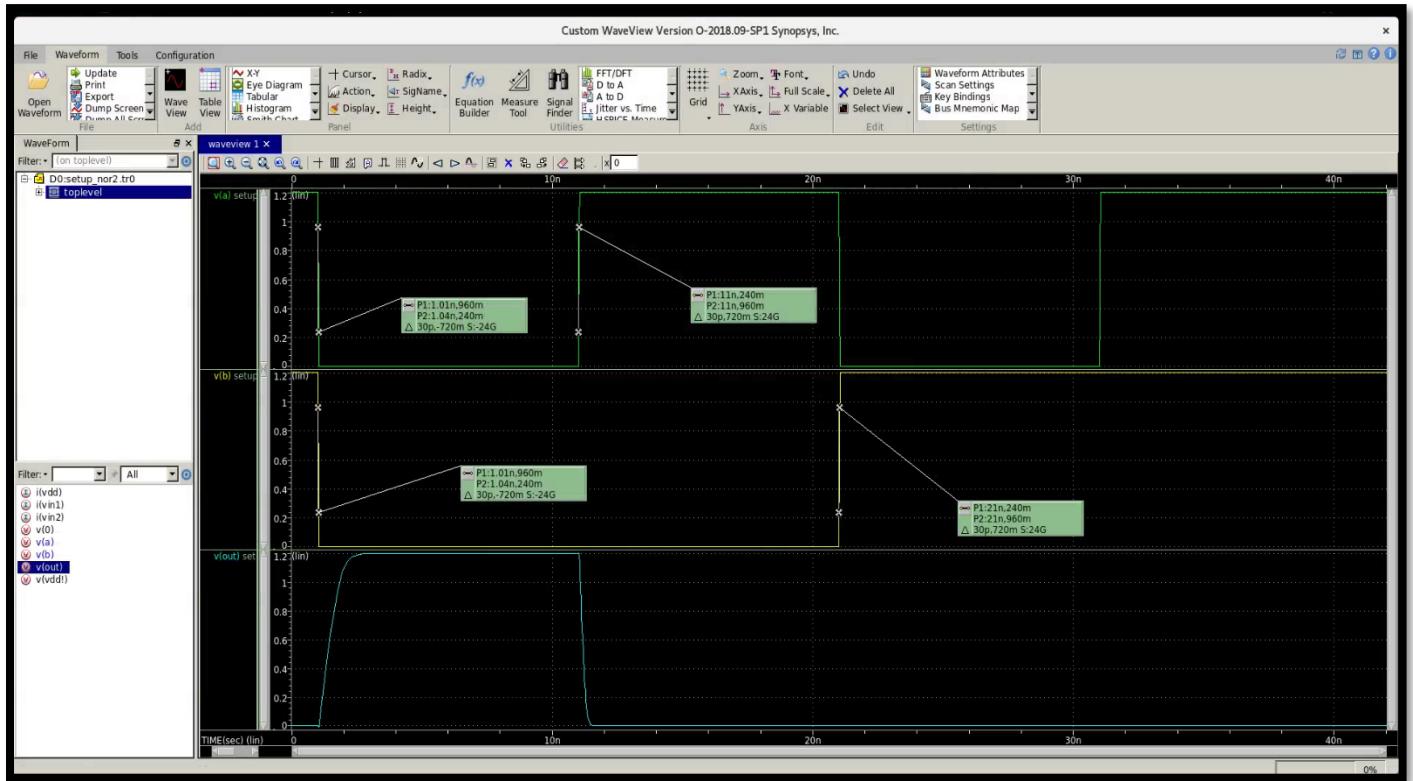
vin1 A GND! pw1(0ns 1.2v 1ns 1.2v 1.05ns 0v 11ns 0v 11.05ns 1.2v 21ns 1.2v 21.05ns 0v 31ns 0v 31.05ns 1.2v 41ns 1.2v)
vin2 B GND! pw1(0ns 1.2v 1ns 1.2v 1.05ns 0v 21ns 0v 21.05ns 1.2v 41ns 1.2v)

cout OUT GND! 55f

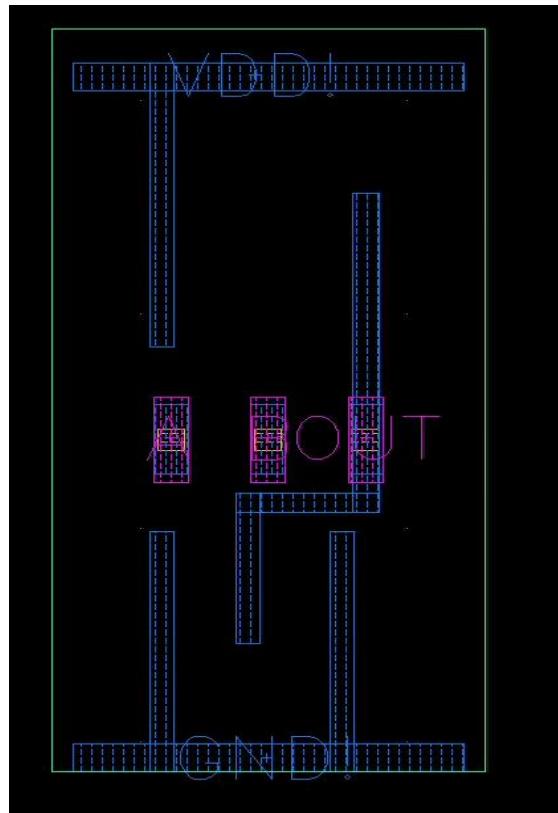
$transient analysis
.tr 100ps 42ns

.end
```

## Simulation Waveform



## Abstract View

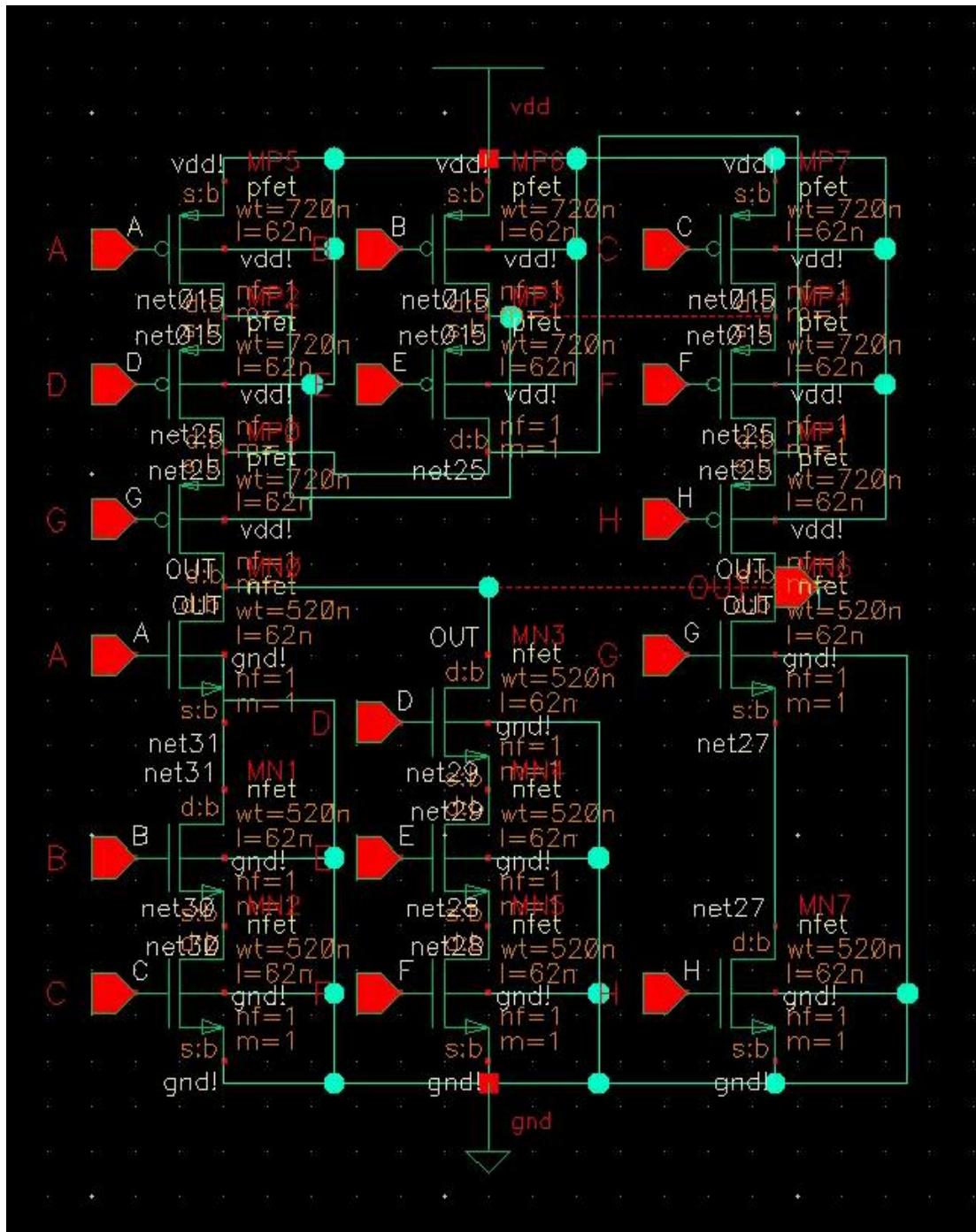


# AOI332

## Function

$$\text{OUT} = \text{NOT}(\text{ABC} \mid \text{DEF} \mid \text{GH})$$

## Schematic

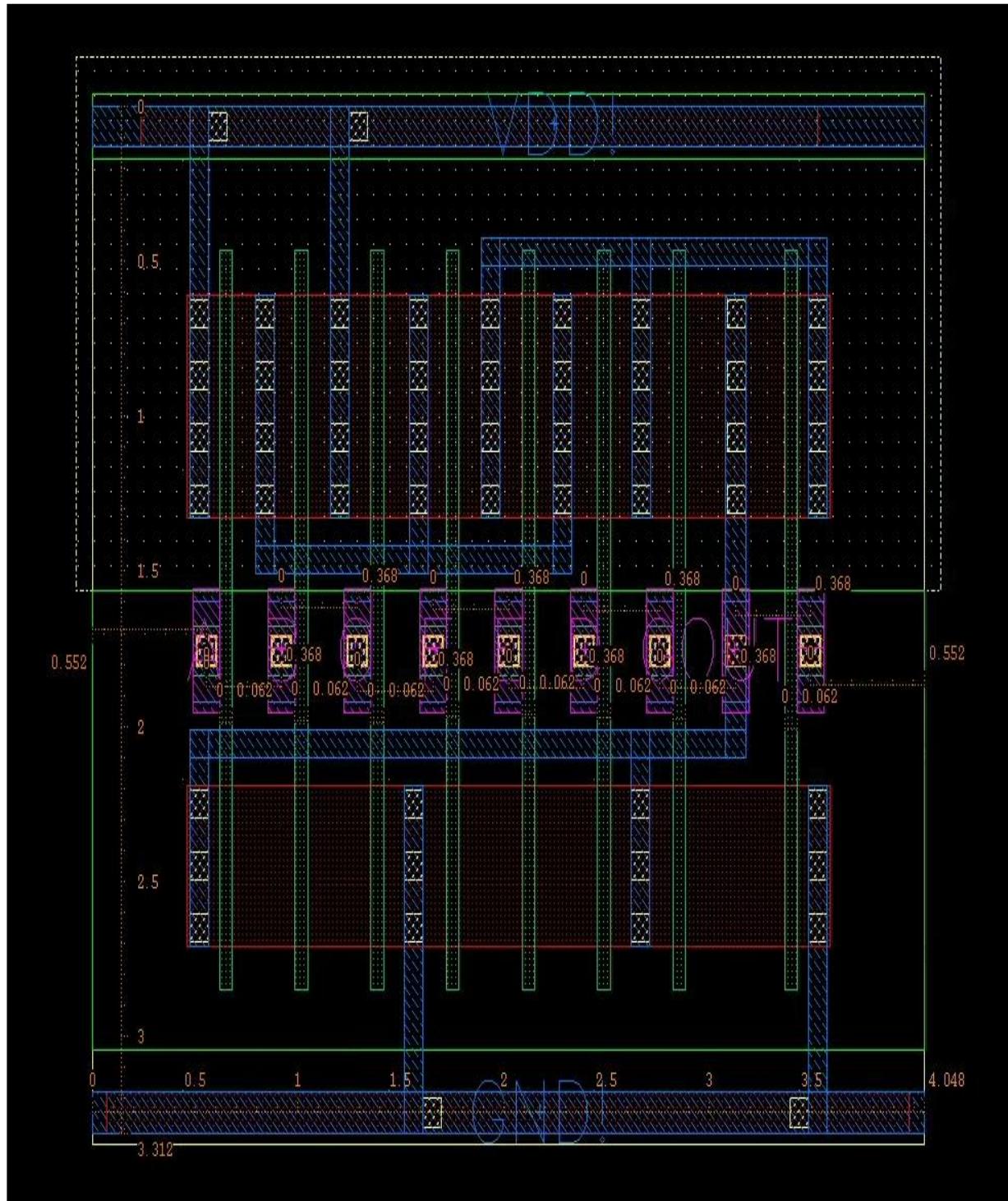


## Layout

Cell Height = 3.312 um

Cell Width = 4.048 um

Total Cell Area = 13.406 um<sup>2</sup>



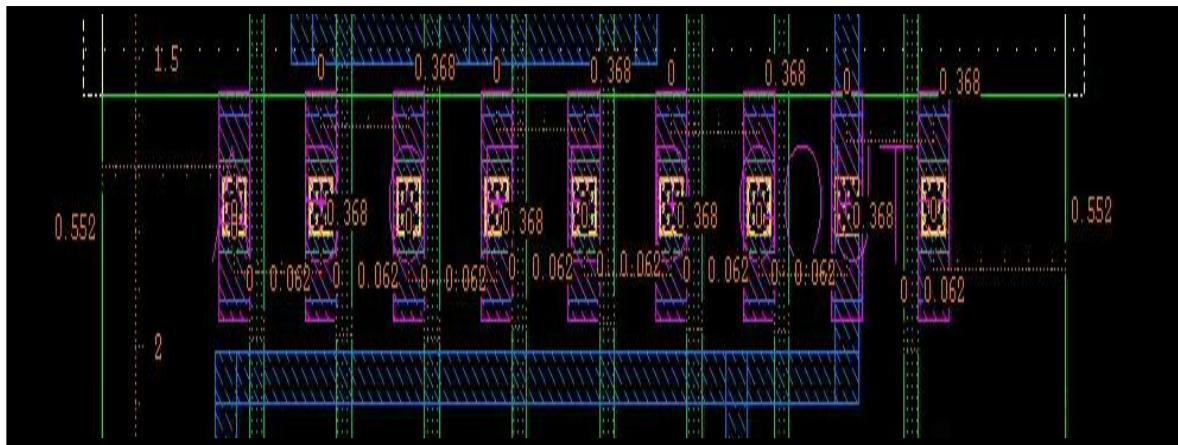
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um



## DRC

NoMachine - engnx

Activities Calibre

Wed 16:31

Calibre - RVE v2013.2\_18.13 : aoi332.drc.results

File View Highlight Tools Window Setup Help

Show All aoi332, 0 Results (in 0 of 2078 Checks)

Check / Cell	Results
✓ Check GRS2	0
✓ Check GRS6	0
✓ Check GRB_BF01	0
✓ Check GRSRB_BF01	0
✓ Check GRB_BF02	0
✓ Check GRB_BF03	0
✓ Check GRB_BH04	0
✓ Check GRB_BH01	0
✓ Check GRB_BH02	0
✓ Check GRSRB_BH02	0
✓ Check GRB_BH03	0
✓ Check GRB_BH04	0
✓ Check GRSRB_BH04	0
✓ Check GRB_DE01	0
✓ Check GRB_DE02	0

Rule File Pathname: /home/312/gc/gcv210009/cad/gf65/p4/aoi332\_DRC/\_Calibre\_DRC\_rules\_09  
Rule File Title: VI-M00054.09 - VI-MT0052.12  
Shapes with acute angles are prohibited (Except for PROTECT Layer)

# LVS

The screenshot shows the Calibre LVS interface. The main window displays a table of comparison results for the cell `ao332`. The table includes columns for `Layout Cell / Type`, `Source Cell`, `Nets`, `Instances`, and `Ports`. The results show 11L, 11S nets, 4L, 4S instances, and 11L, 11S ports.

Below the table, a detailed summary for cell `ao332` is provided:

- CELL ao332 Summary (Clean)**
- CELL COMPARISON RESULTS ( TOP LEVEL )**
- LAYOUT CELL NAME:** ao332  
**SOURCE CELL NAME:** ao332
- INITIAL NUMBERS OF OBJECTS**

	Layout	Source	Component Type
Ports:	11	11	
Nets:	18	18	
Instances:	8	8	MN (4 pins) NP (4 pins)
Total Inst:	16	16	

- NUMBERS OF OBJECTS AFTER TRANSFORMATION**

	Layout	Source	Component Type
Ports:	11	11	
Nets:	11	11	

# PEX

The screenshot shows the Calibre Interactive PEX interface. The main window displays a transcript of the command-line session:

```

--- Activities Calibre Interactive - PEX v2013.2..18.13 -
Wed 16:35
Calibre Interactive - PEX v2013.2..18.13
File Transcript Setup Help
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE
---- OUTPUT NEILIST FILE NAME /home/012/g/gx/gxv210009/cad/gf65/p4/aoi332_LVS/aoi332.pex.sp
---- OUTPUT PARASITIC MODEL FILE NAME /home/012/g/gx/gxv210009/cad/gf65/p4/aoi332_LVS/aoi332.pex.sp.pex
---- PROCESSING PARASITIC MODELS
---- OUTPUT PARASITIC MODEL INSTANCE FILE NAME /home/012/g/gx/gxv210009/cad/gf65/p4/aoi332_LVS/aoi332.pex.sp.Aoi332.pci
---- NETWORK REDUCTION BEGIN:
---- READING FROM PDB...
---- BEGIN REDUCING NETS...
---- DONE REDUCING NETS...
---- WRITING TO PDB...
---- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 423/424/467 MALLOC = 360/360/360
---- PDB NET SUMMARY
---- pdb file name = svdb/Aoi332.pdb
root cell name = Aoi332
total nets = 18
top-level nets = 18
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0
---- CALIBRE xRC: WARNING / ERROR Summary
---- xRC Warnings = 0
---- xRC Errors = 0
---- CALIBRE xRC: FORMATTER COMPLETED - Wed Oct 30 16:35:30 2024
---- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 290/290/360 ELAPSED TIME = 4
3 Warnings

```

The transcript also includes a note about unsupported Linux releases:

This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.

# PEX Netlist

```

* File: /home/012/g/gxv210009/cad/gf65/p4/aoi332_LVS/aoi332.pex.sp
* Created: Tue Oct 29 11:09:07 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
*.include "/home/012/g/gxv210009/cad/gf65/p4/aoi332_LVS/aoi332.pex.sp.pex"
.subckt aoi332 OUT GND! VDD! A B C F E D G H
*
* H     H
* G     G
* D     D
* E     E
* F     F
* C     C
* B     B
* A     A
* VDD!  VDD!
* GND!  GND!
* OUT   OUT
X00_noxref N_GND! _D0_noxref_pos N_VDD! _D0_noxref_neg DIODENWX AREA=6.30208e-12
+ PERIM=1.0768e-05
XMMN0_N_OUT_MMN0_d N_A_MMN0_g NET31 N_GND! _D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=8.32e-14 AS=-7.956e-14 PD=1.36e-06 PS=8.26e-07 NRD=0.192308
+ NRS=0.294231 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=2.736e-06 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN1_NET31_N_B_MMN1_g NET30 N_GND! _D0_noxref_pos NFET L=6.2e-08 W=5.2e-07
+ AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07 NRD=0.294231 NRS=0.294231
+ M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.28e-07 SB=2.368e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.054e-14 PANW8=1.24e-14
+ PANW9=9.3e-15 PANW10=0
XMMN2_NET30_N_C_MMN2_g N_GND! _MMN2_s N_GND! _D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07 NRD=0.294231
+ NRS=0.286538 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=8.96e-07
+ SB=2e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.054e-14
+ PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN5_NET28_N_F_MMN5_g N_GND! _MMN2_s N_GND! _D0_noxref_pos NFET L=6.2e-08

```

```

+ PANW9=6.944e-14 PANW10=5.332e-15
XMMP4_N_NET25_MMP4_d N_F_MMP4_g N_NET015_MMP7_d N_VDD! _D0_noxref_neg PFET
+ L=6.2e-08 W=7.2e-07 AD=1.1016e-13 AS=1.1016e-13 PD=1.026e-06 PS=1.026e-06
+ NRD=0.2125 NRS=0.188889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.264e-06 SB=1.632e-06 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15
+ PANW4=3.1e-15 PANW5=3.1e-15 PANW6=6.2e-15 PANW7=1.4508e-14 PANW8=2.1948e-14
+ PANW9=2.48e-14 PANW10=6.0772e-14
XMMP3_N_NET25_MMP4_d N_E_MMP3_g N_NET015_MMP3_s N_VDD! _D0_noxref_neg PFET
+ L=6.2e-08 W=7.2e-07 AD=1.1016e-13 AS=1.1016e-13 PD=1.026e-06 PS=1.026e-06
+ NRD=0.2125 NRS=0.190278 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.632e-06 SB=1.264e-06 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15
+ PANW4=3.1e-15 PANW5=3.1e-15 PANW6=6.2e-15 PANW7=1.4508e-14 PANW8=2.1948e-14
+ PANW9=2.48e-14 PANW10=6.0772e-14
XMMP2_NET25_MMP2_d N_D_MMP2_g N_NET015_MMP3_s N_VDD! _D0_noxref_neg PFET
+ L=6.2e-08 W=7.2e-07 AD=1.1016e-13 AS=1.1016e-13 PD=1.026e-06 PS=1.026e-06
+ NRD=0.208333 NRS=0.234722 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1
+ SA=2e-06 SB=8.96e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15
+ PANW4=3.1e-15 PANW5=3.1e-15 PANW6=6.2e-15 PANW7=1.4508e-14 PANW8=2.1948e-14
+ PANW9=2.48e-14 PANW10=6.0772e-15
XMMP0_N_OUT_MMPO_d N_N_G_MMPO_g NET25_MMPO_d N_VDD! _D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.1016e-13 AS=1.1016e-13 PD=1.026e-06 PS=1.026e-06 NRD=0.222222
+ NRS=0.216667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=2.368e-06
+ SB=5.28e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=6.2e-15 PANW7=1.4508e-14 PANW8=6.6588e-14 PANW9=2.48e-14
+ PANW10=5.332e-15
XMP11_OUT_MMPO_d N_H_MMMP1_g N_NET25_MMMP1_s N_VDD! _D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.1016e-13 AS=1.152e-13 PD=1.026e-06 PS=1.76e-06 NRD=0.202778
+ NRS=0.138889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=2.736e-06
+ SB=1.6e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=1.4508e-14 PANW8=2.1948e-14 PANW9=2.48e-14
+ PANW10=5.332e-15
*
.included "/home/012/g/gxv210009/cad/gf65/p4/aoi332_LVS/aoi332.pex.sp.A0I332.pxi"
*
.ends
*
*
```

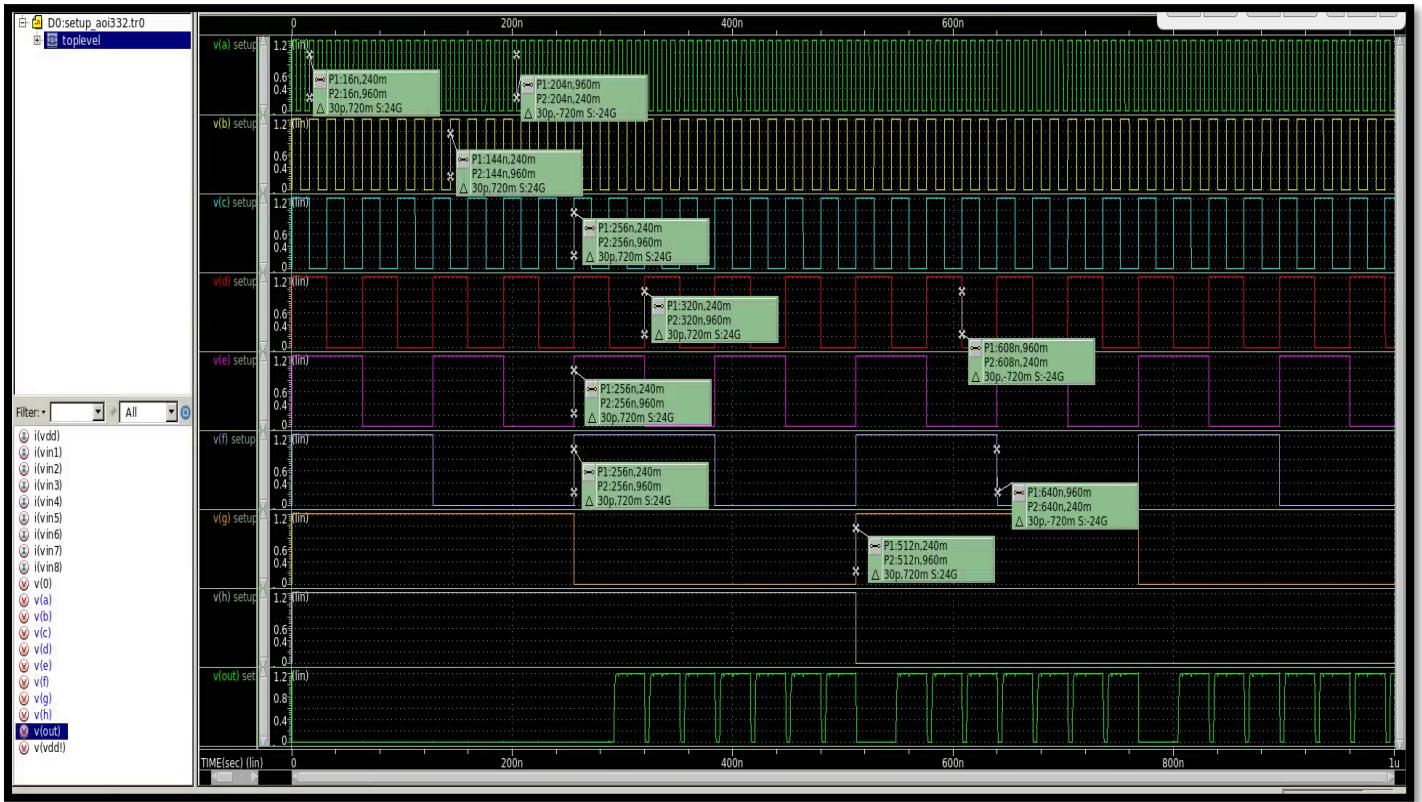
## HSpice Setup File

The screenshot shows a terminal or text editor window titled "NoMachine - gdcbm". The file being edited is named "setup.aoi332.sp" located at "/cad/spice/aoi332". The content of the file is a HSPICE script for a transistor model. It includes include statements for a library and a design model, defines input voltages (xi, vdd) and output voltage (cout), and specifies transient analysis parameters. The script ends with an .end command.

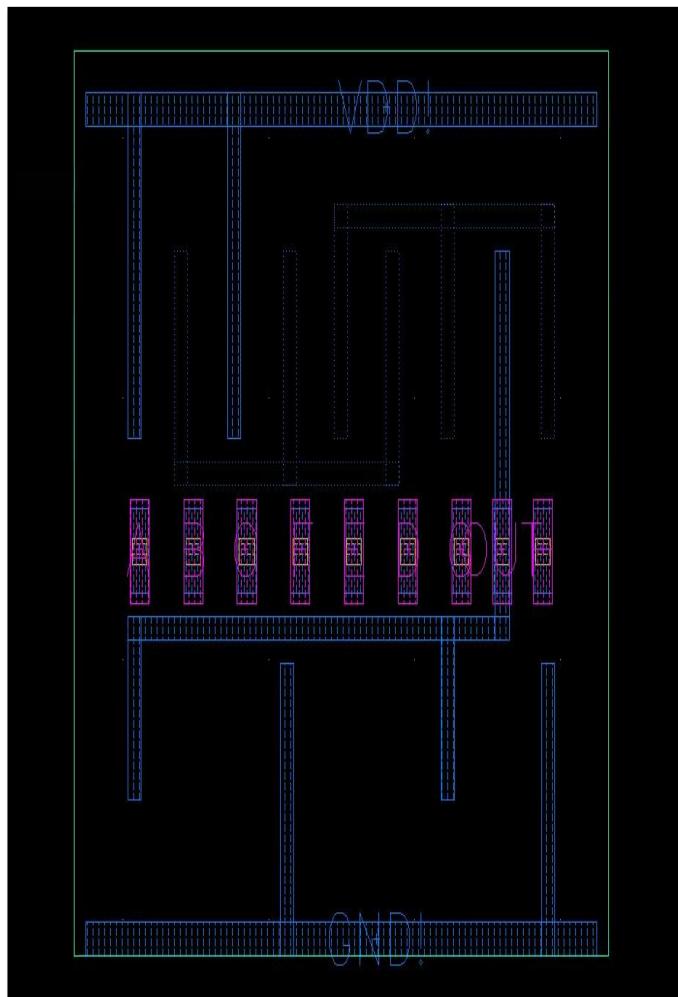
```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "aoi332.pex.sp"
.option post runlvl=5
xi OUT GND! VDD! A B C F E D G H aoi332
vdd VDD! GND! 1.2v
vin1 A GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 4ns 8ns)
vin2 B GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 8ns 16ns)
vin3 C GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 16ns 32ns)
vin4 D GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 32ns 64ns)
vin5 E GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 64ns 128ns)
vin6 F GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 128ns 256ns)
vin7 G GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 256ns 512ns)
vin8 H GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 512ns 1024ns)
cout OUT GND! 55f
$transient analysis
.tr 100ps 1000ns
.end
```

Plain Text ▾ Tab Width: 8 ▾ Ln 27, Col 7 ▾ INS

## Simulation Waveform



## Abstract View



# NAND3

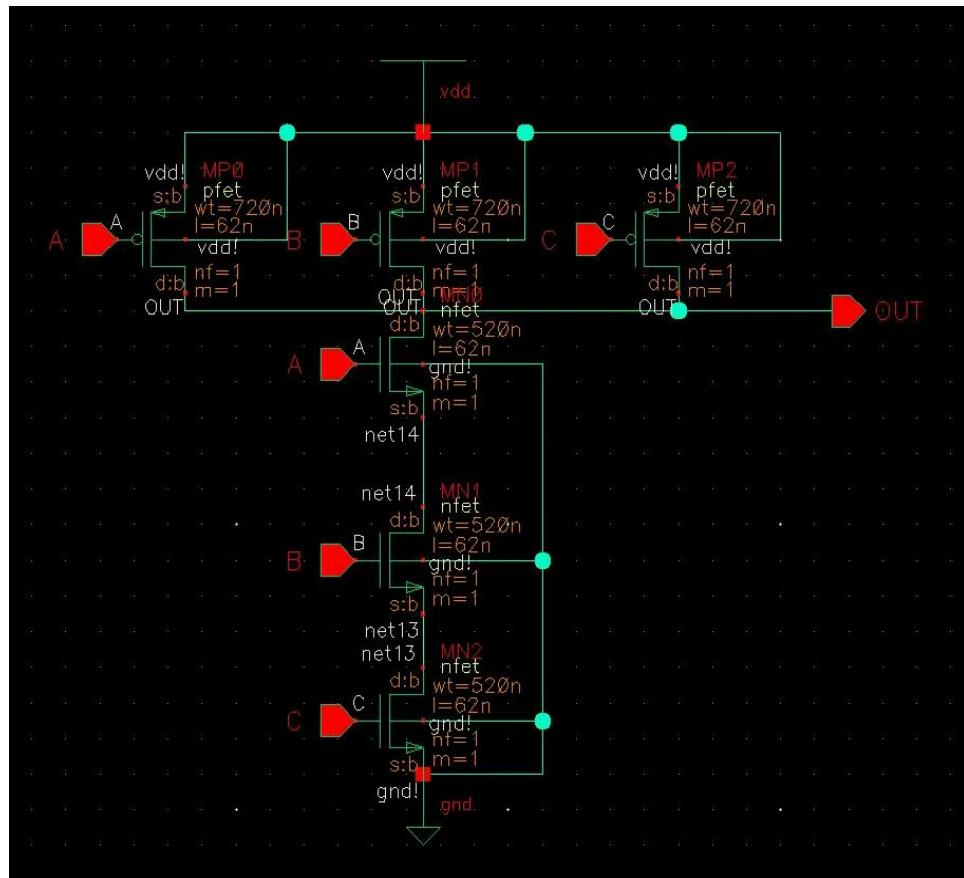
## Function

$$OUT = (\text{NOT}(A \& B \& C))$$

## Truth Table

A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

## Schematic

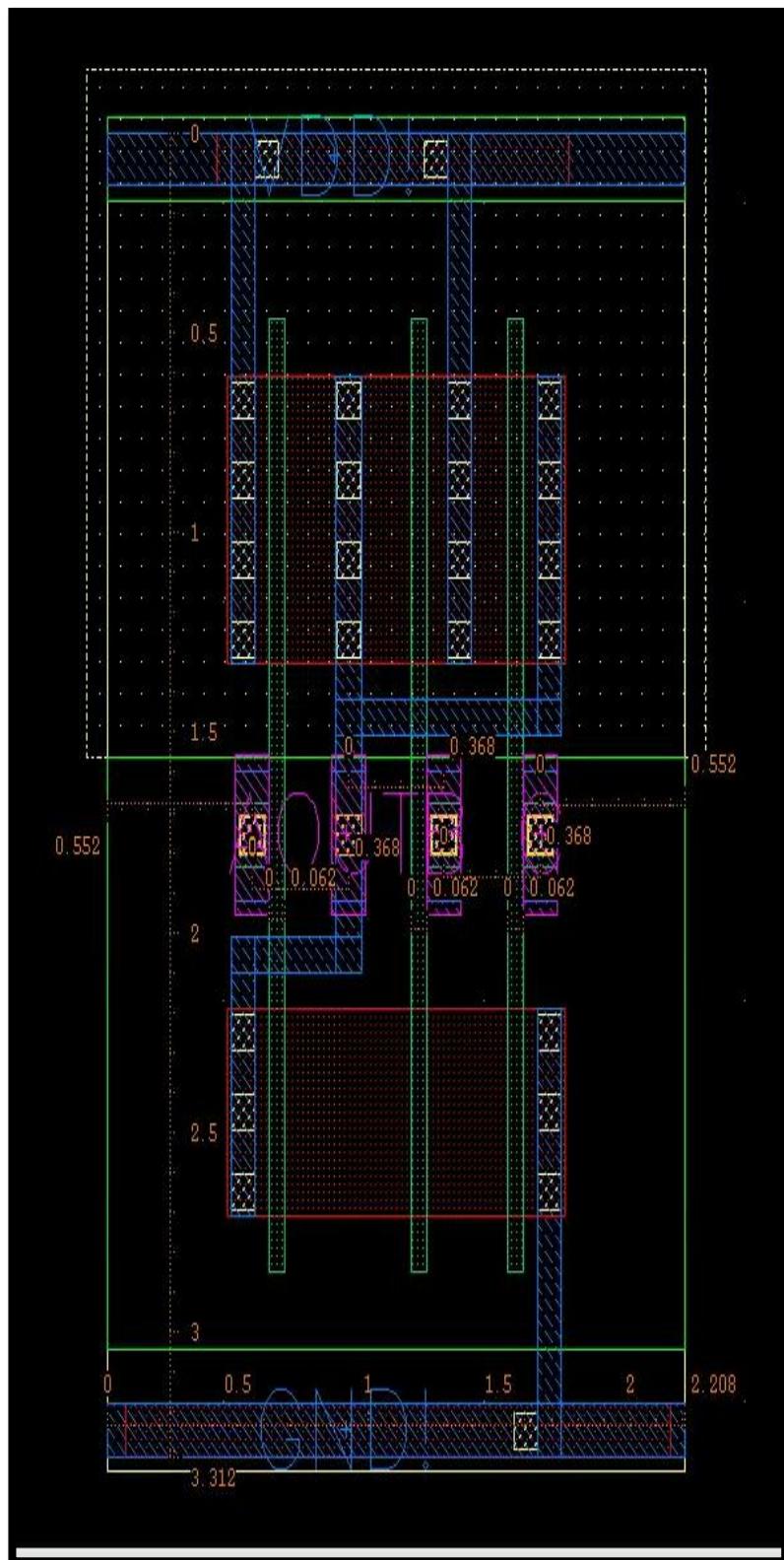


## Layout

Cell Height = 3.312 um

Cell Width = 2.208 um

Total Cell Area = 7.312 um<sup>2</sup>



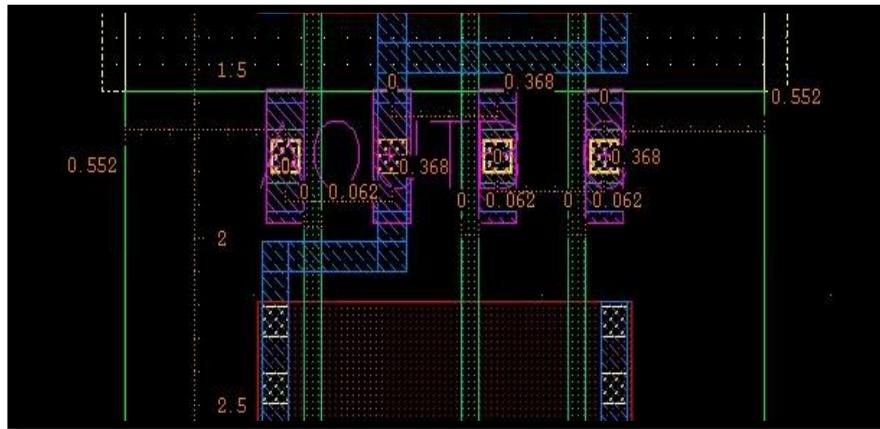
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

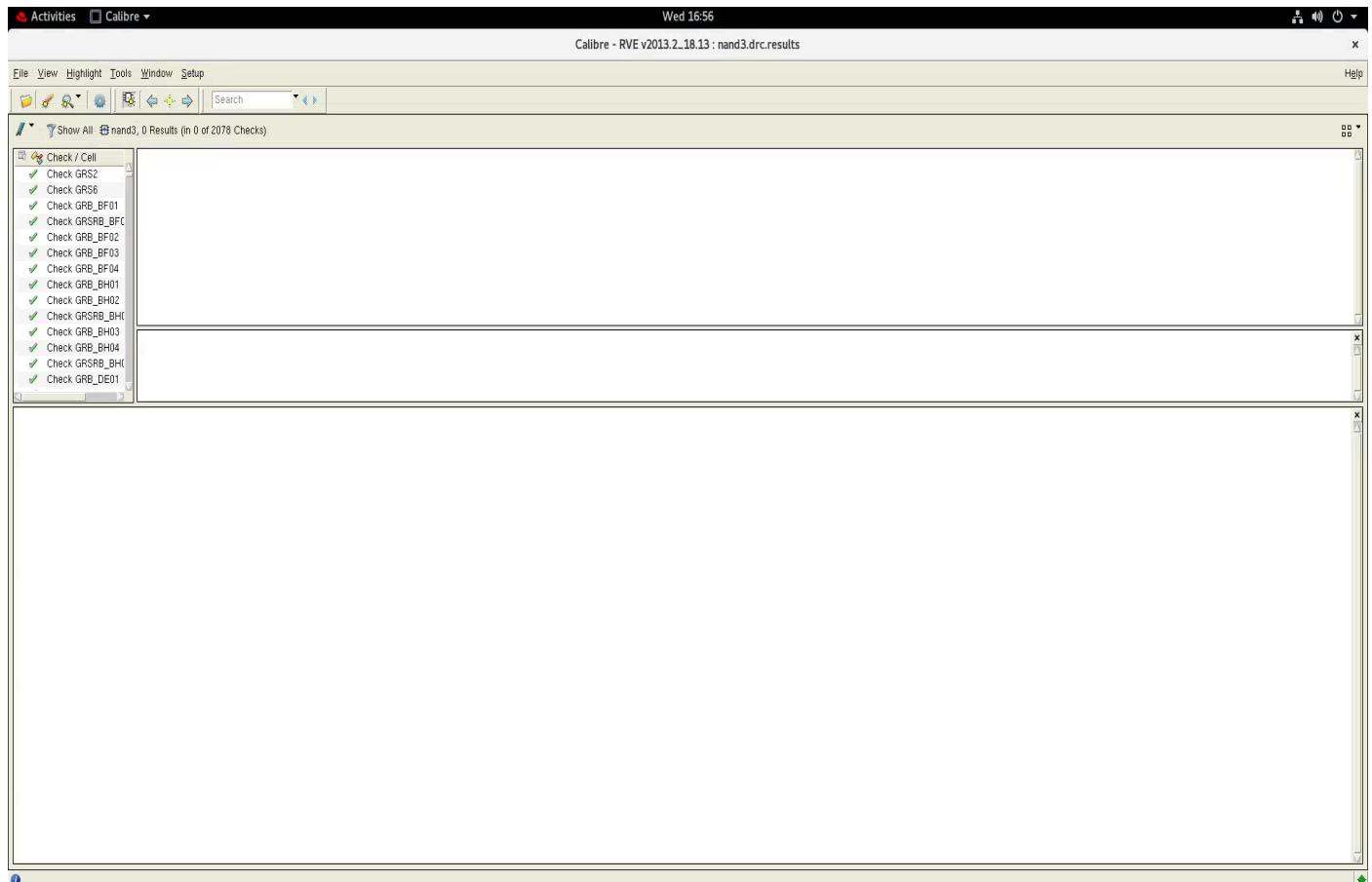
Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um



## DRC



## LVS

The screenshot shows the Calibre LVS interface. The top menu bar includes 'Activities' (selected), 'Calibre', 'File', 'View', 'Highlight', 'Tools', 'Window', 'Setup', 'Search', and 'Help'. The title bar indicates 'Calibre - RVE v2013.2..18.13 : svdb nand3' and the time 'Wed 16:57'. The left sidebar contains navigation links for Extraction Results, Comparison Results, Parasitics, ERC (ERC Results, ERC Summary), Reports (Extraction Report, LVS Report), Rules, View (Info, Finder, Schematics), Setup (Rules File), and Options. The main window displays 'Comparison Results' for the 'nand3' cell. A table provides summary information:

Layout Cell / Type	Source Cell	Nets	Instances	Ports
nand3	nand3	6L, 6S	1L, 1S	6L, 6S

The bottom pane shows the 'Cell nand3 Summary (Clean)' report, which includes the following sections:

- CELL COMPARISON RESULTS ( TOP LEVEL )**
- LAYOUT CELL NAME:** nand3  
**SOURCE CELL NAME:** nand3
- INITIAL NUMBERS OF OBJECTS**

	Layout	Source	Component Type
Ports:	6	6	
Nets:	8	8	
Instances:	3	3	MN (4 pins)
	3	3	MP (4 pins)
Total Inst:	6	6	

- NUMBERS OF OBJECTS AFTER TRANSFORMATION**

	Layout	Source	Component Type
Ports:	6	6	
Nets:	6	6	

## PEX

The screenshot shows the Calibre Interactive PEX interface. The top menu bar includes 'Activities' (selected), 'Calibre Interactive - PEX v2013.2..18.13', 'File', 'Transcript', 'Setup', 'Help', and a toolbar with icons for Rules, Inputs, Outputs, Run Control, Transcript, Run PEX, and Start RVE. The title bar indicates 'Calibre Interactive - PEX v2013.2..18.13' and the time 'Wed 16:58'. The left sidebar contains links for Rules, Inputs, Outputs, Run Control, Transcript, Run PEX, and Start RVE. The main window displays a processing log and a warning summary.

**Processing Log:**

```

--- OUTPUT NETLIST FILE NAME /home/012/g/gx/gxv210009/cad/gf65/p4/nand3_LVS/nand3.pex.sp
--- OUTPUT PARASITIC MODEL FILE NAME /home/012/g/gx/gxv210009/cad/gf65/p4/nand3_LVS/nand3.pex.sp.pex
--- PROCESSING PARASITIC MODELS
--- OUTPUT PARASITIC MODEL INSTANCE FILE NAME /home/012/g/gx/gxv210009/cad/gf65/p4/nand3_LVS/nand3.pex.sp.NAND3.pxi

--- NETWORK REDUCTION BEGIN:
--- READING FROM PDB...
--- BEGIN REDUCING NETS...
--- END REDUCING NETS...
--- WAITING TO PDB
--- NETWORK REDUCTION COMPLETE: GPU TIME = 0 REAL TIME = 0 LVHEAP = 423/424/467 MALLOC = 360/360/360

```

**NET SUMMARY:**

```

PDB NET SUMMARY
=====
pdbs file name = svdb/NAND3.pdb
root cell name = NAND3
total nets = 8
top level nets = 8
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
errored nets = 0

```

**CALIBRE xRC WARNING / ERROR Summary:**

```

CALIBRE xRC WARNING / ERROR Summary
-----
xRC Warnings = 0
xRC Errors = 0

```

**Completion Summary:**

```

--- CALIBRE xRC FORMATTER COMPLETED - Wed Oct 30 16:58:22 2004
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 290/290/360 ELAPSED TIME = 4

```

**Warnings:**

This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.

## PEX Netlist



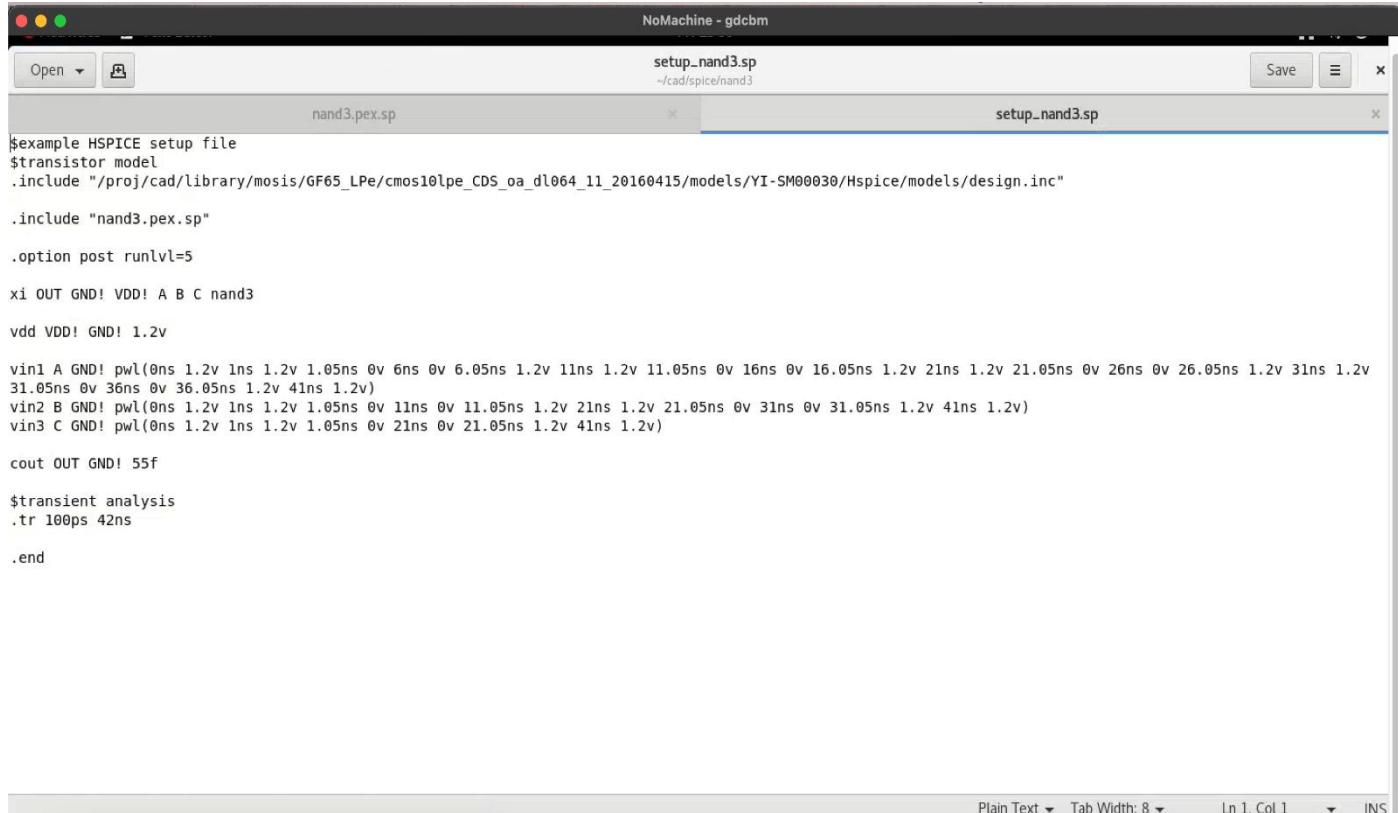
```

nand3.pex.sp
~/cad/spice/nand3

*.include "/home/012/g/gx/gxv210009/cad/gf65/p4/nand3_LVS/nand3.pex.sp.pex"
*.subckt nand3 OUT GND! VDD! A B C
*
* C      C
* B      B
* A      A
* VDD!   VDD!
* GND!   GND!
* OUT    OUT
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=3.44e-12
+ PERIM=7.44e-06
XMMN0_N_OUT MMN0_d N_A MMN0_g NET14_N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=8.32e-14 AS=1.2532e-13 PD=1.36e-06 PS=1.002e-06 NRD=0.192308
+ NRS=0.463462 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=1.072e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN1 NET14_N_B MMN1_g NET13_N_GND!_D0_noxref_pos NFET L=6.2e-08 W=5.2e-07
+ AD=1.2532e-13 AS=7.956e-14 PD=1.002e-06 PS=8.26e-07 NRD=0.463462 NRS=0.294231
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=7.04e-07 SB=5.28e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.054e-14 PANW8=1.24e-14
+ PANW9=9.3e-15 PANW10=0
XMMN2 NET13_N_C_MMN2_g N_GND!_MMN2_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=8.32e-14 PD=8.26e-07 PS=1.36e-06 NRD=0.294231
+ NRS=0.192308 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.072e-06
+ SB=1.6e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMP0_N_OUT MMP0_d N_A MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.7352e-13 AS=1.152e-13 PD=1.202e-06 PS=1.76e-06 NRD=0.334722
+ NRS=0.138889 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07
+ SB=1.072e-06 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=1.4508e-14 PANW8=2.1948e-14 PANW9=2.48e-14
+ PANW10=4.9972e-14
XMMP1_N_OUT MMP0_d N_B_MMP1_g N_VDD!_MMP1_s N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.7352e-13 AS=1.1016e-13 PD=1.202e-06 PS=1.026e-06 NRD=0.334722
+ NRS=0.172222 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=7.04e-07
+ SR=5.28e-07 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15

```

## HSpice Setup File



```

NoMachine - gdcbm

Open Save
setup.nand3.sp
~/cad/spice/nand3

nand3.pex.sp
setup_nand3.sp

$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "nand3.pex.sp"

.option post runlvl=5

xi OUT GND! VDD! A B C nand3
vdd VDD! GND! 1.2V

vin1 A GND! pw1(0ns 1.2V 1ns 1.2V 1.05ns 0V 6ns 0V 6.05ns 1.2V 11ns 1.2V 11.05ns 0V 16ns 0V 16.05ns 1.2V 21ns 1.2V 21.05ns 0V 26ns 0V 26.05ns 1.2V 31ns 1.2V
31.05ns 0V 36ns 0V 36.05ns 1.2V 41ns 1.2V)
vin2 B GND! pw1(0ns 1.2V 1ns 1.2V 1.05ns 0V 11ns 0V 11.05ns 1.2V 21ns 1.2V 21.05ns 0V 31ns 0V 31.05ns 1.2V 41ns 1.2V)

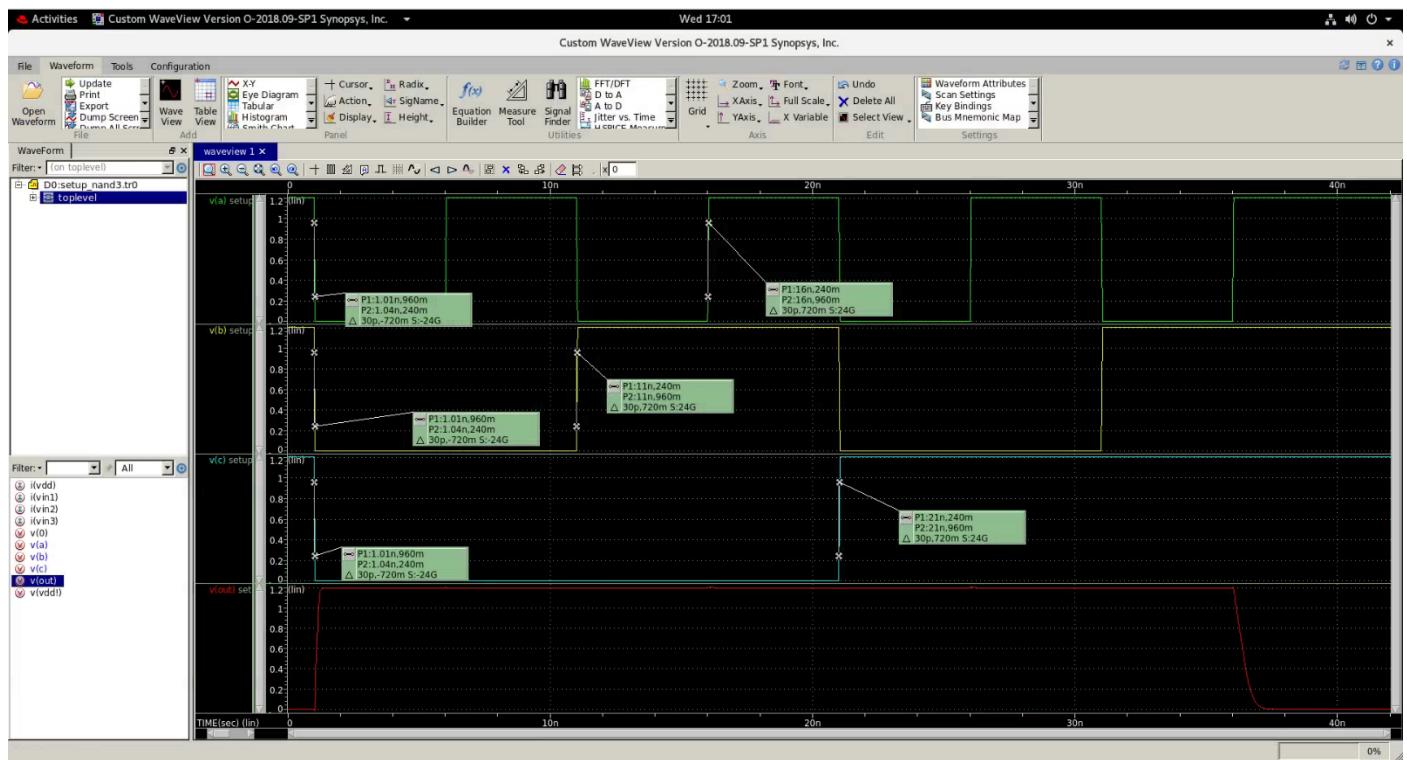
vin3 C GND! pw1(0ns 1.2V 1ns 1.2V 1.05ns 0V 21ns 0V 21.05ns 1.2V 41ns 1.2V)

cout OUT GND! 55f
$transient analysis
.tr 100ps 42ns

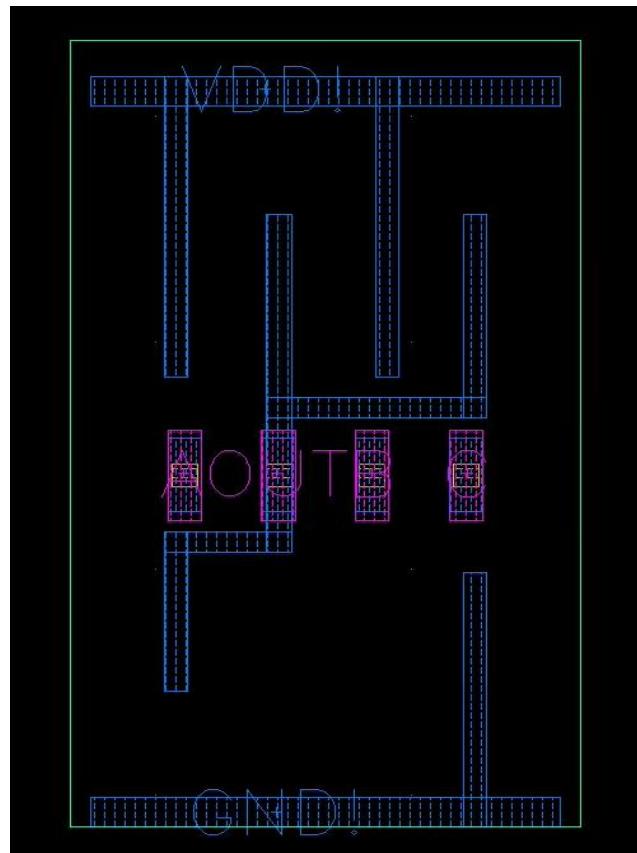
.end

```

# Simulation Waveform



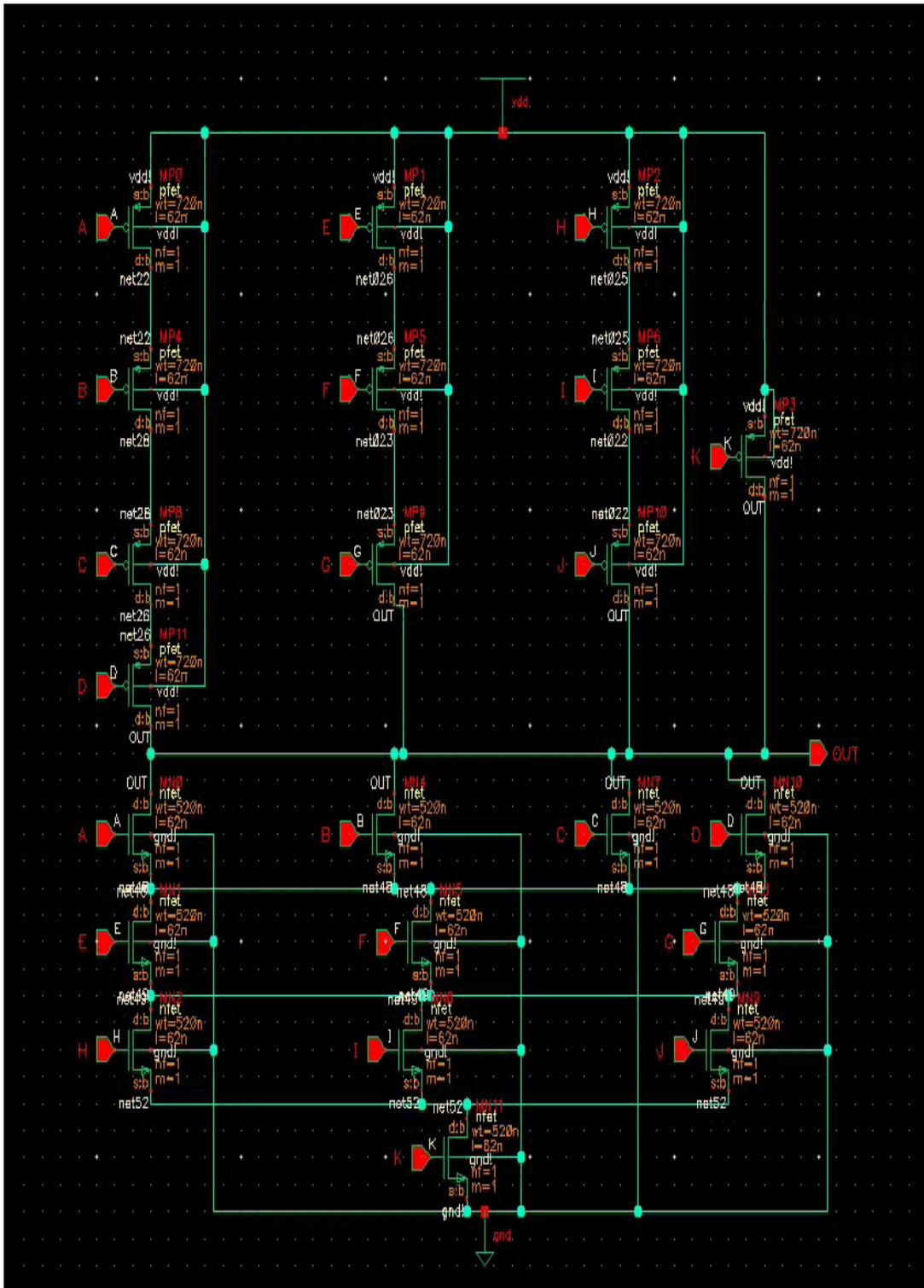
# Abstract View



## Function

$$\text{OUT} = \text{NOT}((\text{A}+\text{B}+\text{C}+\text{D})(\text{E}+\text{F}+\text{G})(\text{H}+\text{I}+\text{J})\text{K})$$

## Schematic

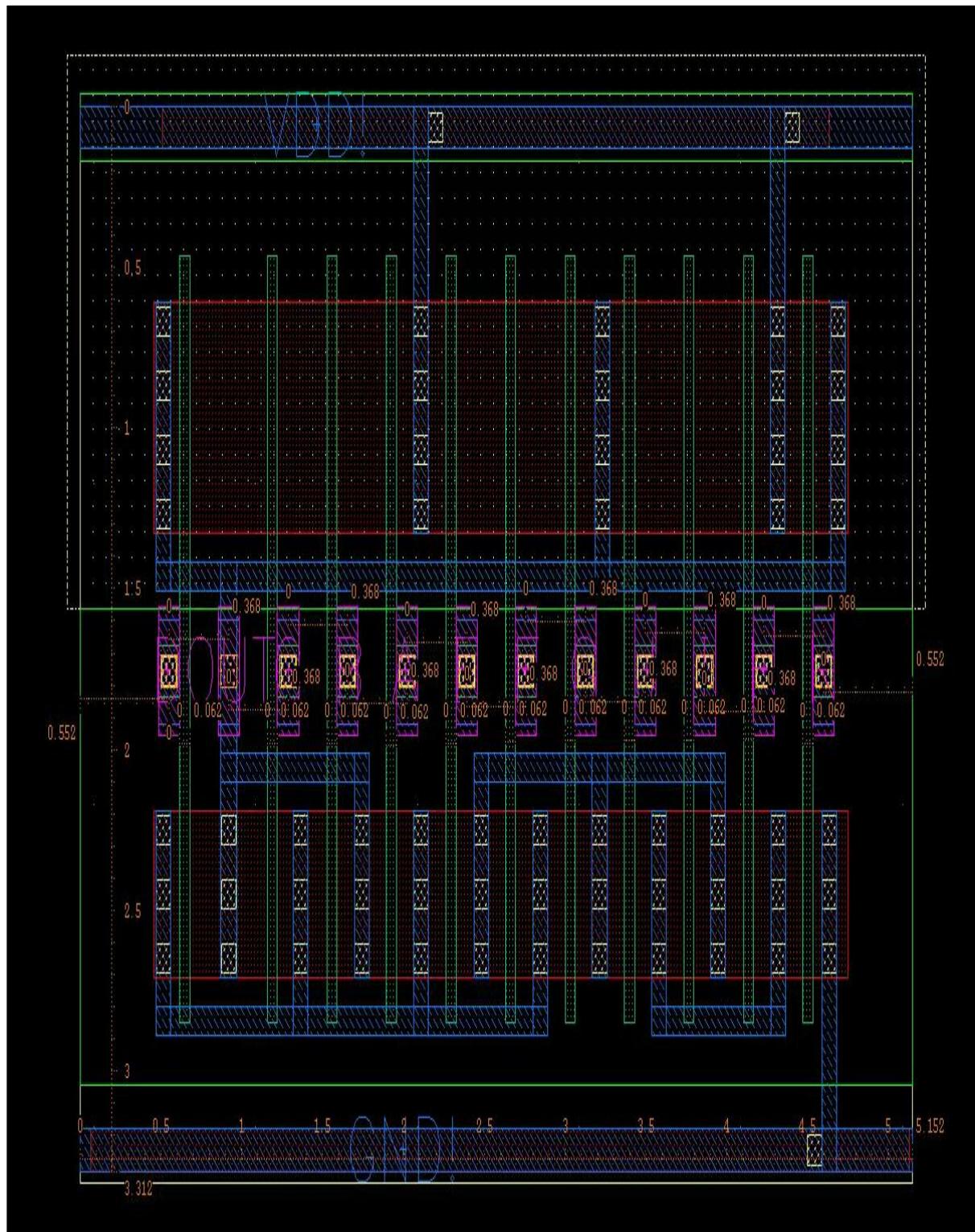


## Layout

Cell Height = 3.312 um

Cell Width = 2.208 um

Total Cell Area = 7.312 um<sup>2</sup>



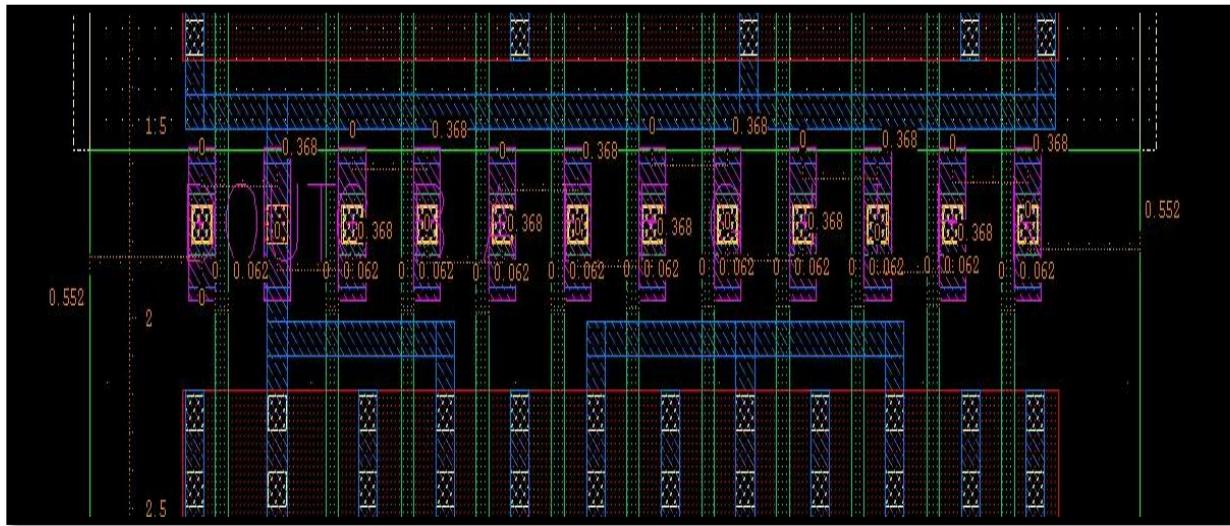
# Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

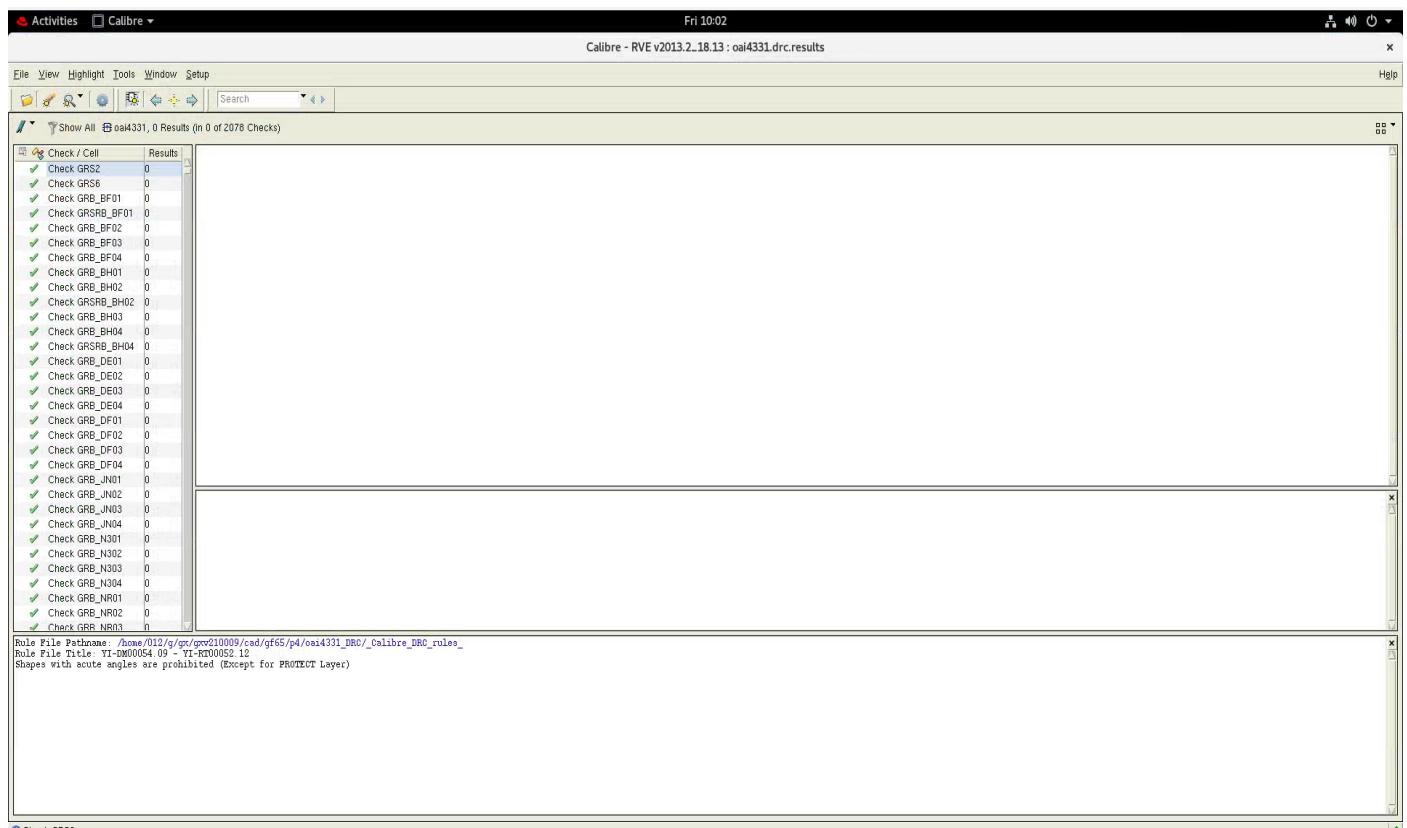
Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um



## DRC



# LVS

Calibre - RVE v2013.2\_18.13 : svdb oai4331

File View Highlight Tools Window Setup

Navigator Comparison Results

**Results**

- Extraction Results
- Comparison Results
- Parasitics
- ERC
- ERC Results
- ERC Summary
- Reports
- Extraction Report
- LVS Report
- Rules
- Rules File
- View
- Info
- Finder
- Schematics
- Setup
- Options

**Comparison Results**

Layout Cell / Type	Source Cell	Nets	Instances	Ports
oai4331	oai4331	14L, 14S	5L, 5S	14L, 14S

**Cell oai4331 Summary (Clean)**

CELL COMPARISON RESULTS ( TOP LEVEL )

```

# # ##### #
# # # CORRECT # |
# # # # \_/
# #####

```

LAYOUT CELL NAME: oai4331  
SOURCE CELL NAME: oai4331

---

**INITIAL NUMBERS OF OBJECTS**

	Layout	Source	Component Type
Ports:	14	14	
Nets:	24	24	
Instances:	11 11	MN (4 pins) NP (4 pins)	
Total Inst:	22	22	

---

**NUMBERS OF OBJECTS AFTER TRANSFORMATION**

	Layout	Source	Component Type
Ports:	14	14	
Nets:	14	14	

# PEX

Activities Calibre Interactive - PEX v2013.2\_18.13 Fri 10:05

File Transcript Setup

**Output**

```

---- OUTPUT NETLIST FILE NAME /home/012/g/grv210009/csd/gf65/p/oai4331_LW/oai4331.pex.sp
---- OUTPUT PARASTIC MODEL FILE NAME /home/012/g/grv210009/csd/gf65/p/oai4331_LW/oai4331.pex.sp.pex
---- PROCESSING PARASTIC MODELS
---- OUTPUT PARASTIC MODEL INSTANCE FILE NAME /home/012/g/grv210009/csd/gf65/p4/oai4331_LW5/oai4331.pex.sp.oai4331.pxi

```

**Run Control**

```

---- NETWORK REDUCTION BEGIN.
---- REDUCING NETS...
---- BEGIN REDUCING NETS...
---- DONE REDUCING NETS...
---- WRITING TO PEX
---- NETWORK REDUCTION COMPLETE. CPU TIME = 0 REAL TIME = 0 LVMEM = 423/424/467 MALLOC = 361/361/361

```

**Run PEX**

**Start RVE**

**PDB NET SUMMARY**

```

pbd file name = svdb/oai4331.pdb
root nets = 0A14331
total nets = 24
top-level nets = 24
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

```

**-----**

**----- CALIBRE RVE:WARNING / ERROR Summary -----**

```

#500 Warnings = 0
#260 Errors = 0

```

**-----**

**----- CALIBRE RVE:FORMATTER COMPLETED - Fri Nov 10 04:46:2014 -----**

This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.

**3 Warnings**

# PEX Netlist

```
.include "/home/012/g/gx/gxv210009/cad/gf65/p4/oai4331_LVS/oai4331.pex.sp.pex"
.subckt oai4331 OUT GND! VDD! D C B A E F G J I H K
*
* K      K
* H      H
* I      I
* J      J
* G      G
* F      F
* E      E
* A      A
* B      B
* C      C
* D      D
* VDD!   VDD!
* GND!   GND!
* OUT    OUT
X00_noxref_N_GND!_D0_noxref_pos_N_VDD!_D0_noxref_neg DIODENWX AREA=9.13664e-12
+ PERIM=1.4064e-05
XMMN10_N_OUT_MMN10_d N_D_MMN10_g N_NET48_MMN10_s N_GND!_D0_noxref_pos NFET
+ L=6.2e-08 W=5.2e-07 AD=1.2532e-13 AS=8.32e-14 PD=1.002e-06 PS=1.36e-06
+ NRD=0.465385 NRS=0.192308 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=1.6e-07 SB=4.069e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN7_N_OUT_MMN10_d N_C_MMN7_g N_NET48_MMN7_s N_GND!_D0_noxref_pos NFET
+ L=6.2e-08 W=5.2e-07 AD=1.2532e-13 AS=7.956e-14 PD=1.002e-06 PS=8.26e-07
+ NRD=0.461538 NRS=0.276923 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=7.04e-07 SB=3.525e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN4_OUT_MMN4_d N_B_MMN4_g N_NET48_MMN7_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07 NRD=0.292308
+ NRS=0.311538 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.072e-06
+ SB=3.157e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN0_OUT_MMN0_d N_A_MMN0_g N_NET48_MMN0_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07 NRD=0.296154
```

# HSpice Setup File

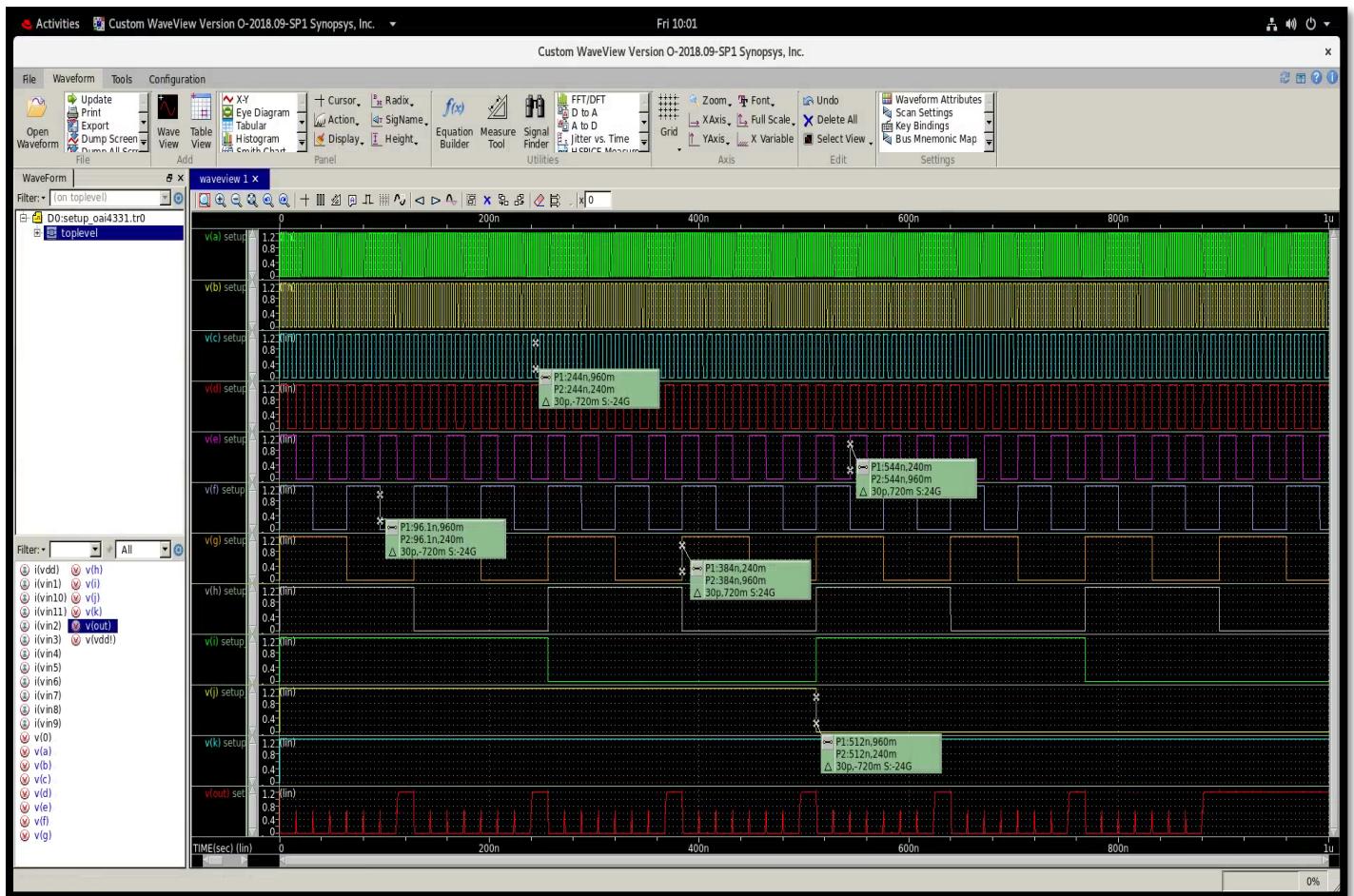
```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lp_e_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "oai4331.pex.sp"

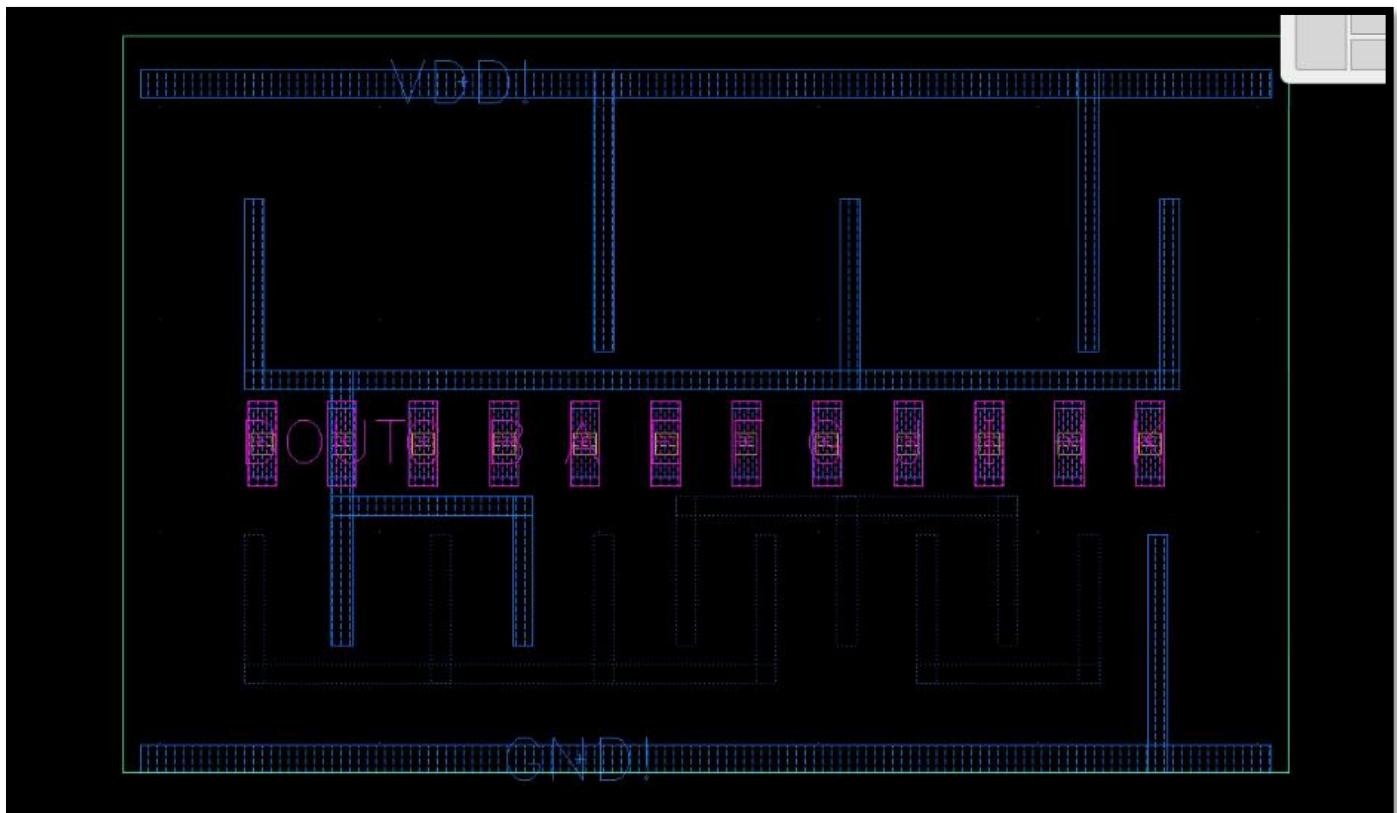
.option post runlvl=5

xi OUT GND! VDD! D C B A E F G J I H K oai4331|
vdd VDD! GND! 1.2v
vin1 A GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 1ns 2ns)
vin2 B GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 2ns 4ns)
vin3 C GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 4ns 8ns)
vin4 D GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 8ns 16ns)
vin5 E GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 16ns 32ns)
vin6 F GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 32ns 64ns)
vin7 G GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 64ns 128ns)
vin8 H GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 128ns 256ns)
vin9 I GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 256ns 512ns)
vin10 J GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 512ns 1024ns)
vin11 K GND! PULSE (0V 1.2V 0ns 0.05ns 0.05ns 1024ns 2048ns)
cout OUT GND! 55f
$transient analysis
```

## Simulation Waveform



## Abstract View

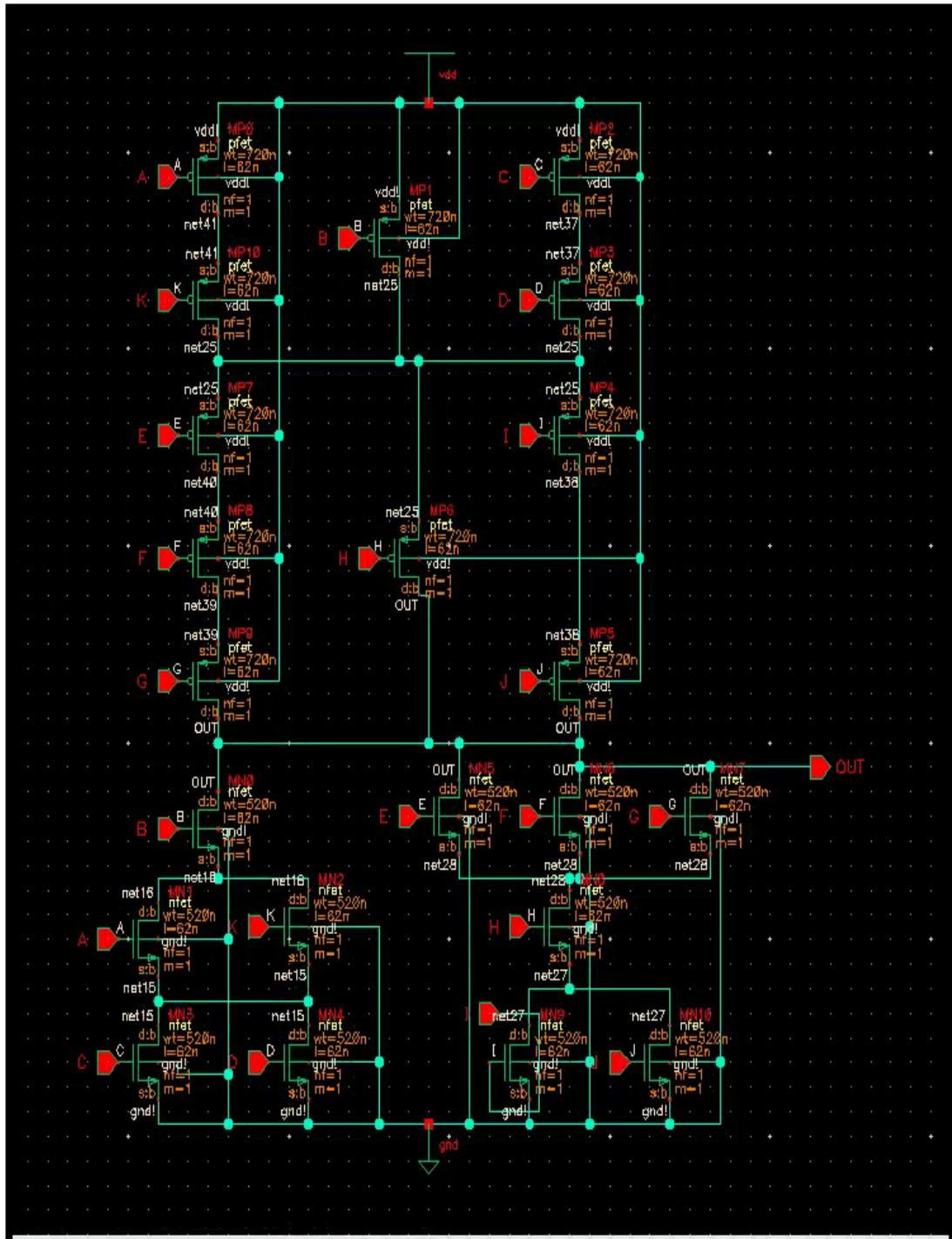


# 11 Input Circuit

## Function

$$\text{OUT} = \text{NOT } [(\text{A|K}) \& \text{B} \& (\text{C|D})] \mid [(\text{E|F|G}) \& \text{H} \& (\text{I|J})]$$

## Schematic

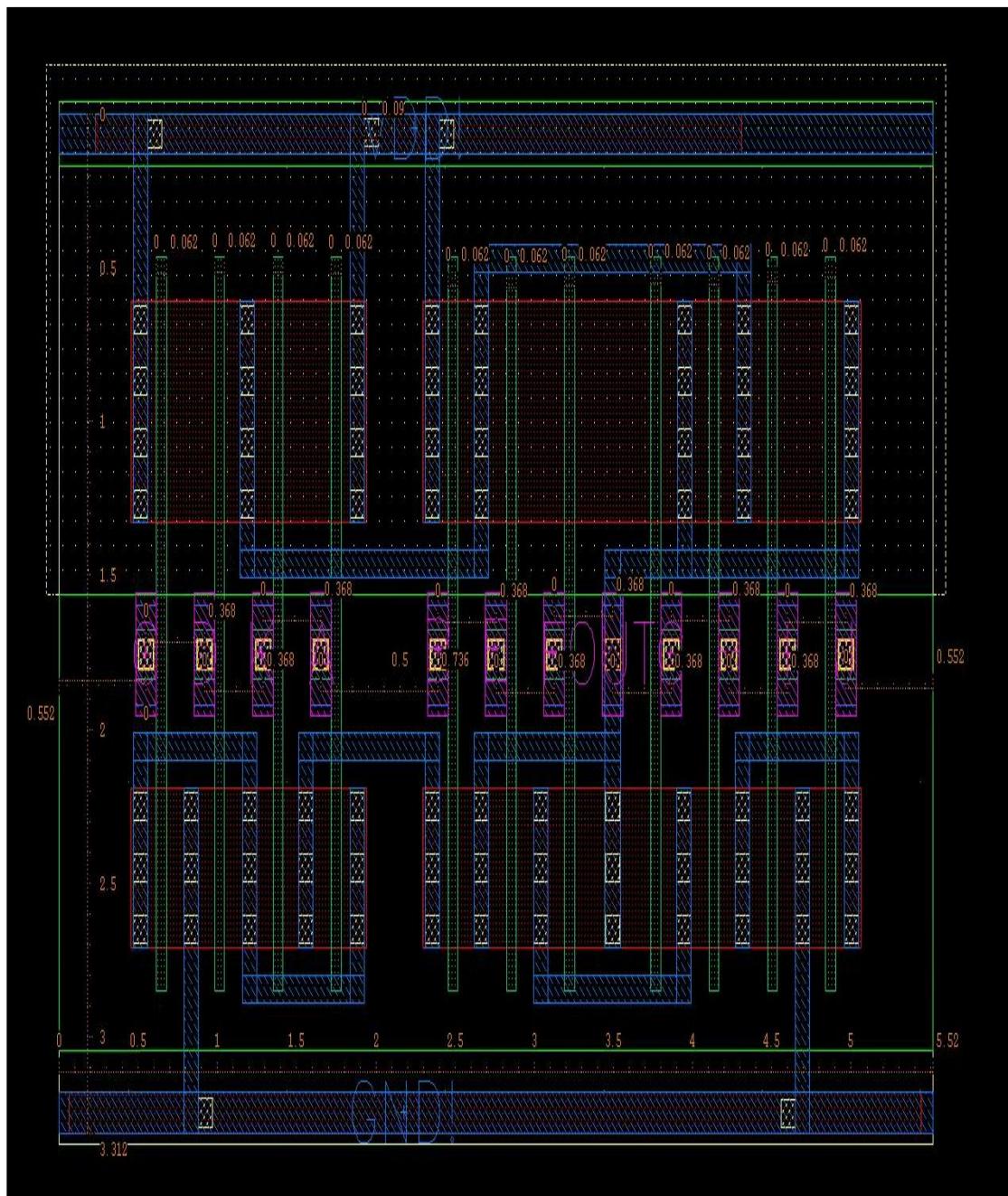


## Layout

Cell Height = 3.312 um

Cell Width = 5.52 um

Total Cell Area = 18.282  $\mu\text{m}^2$



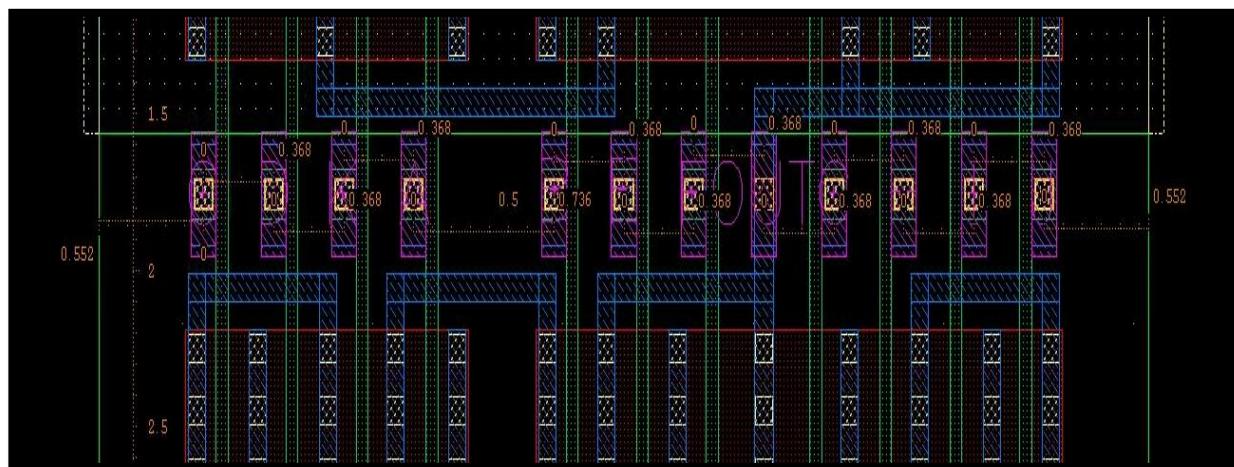
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

Pin Pitch = 0.368um

Offset (left side) = 0.552um

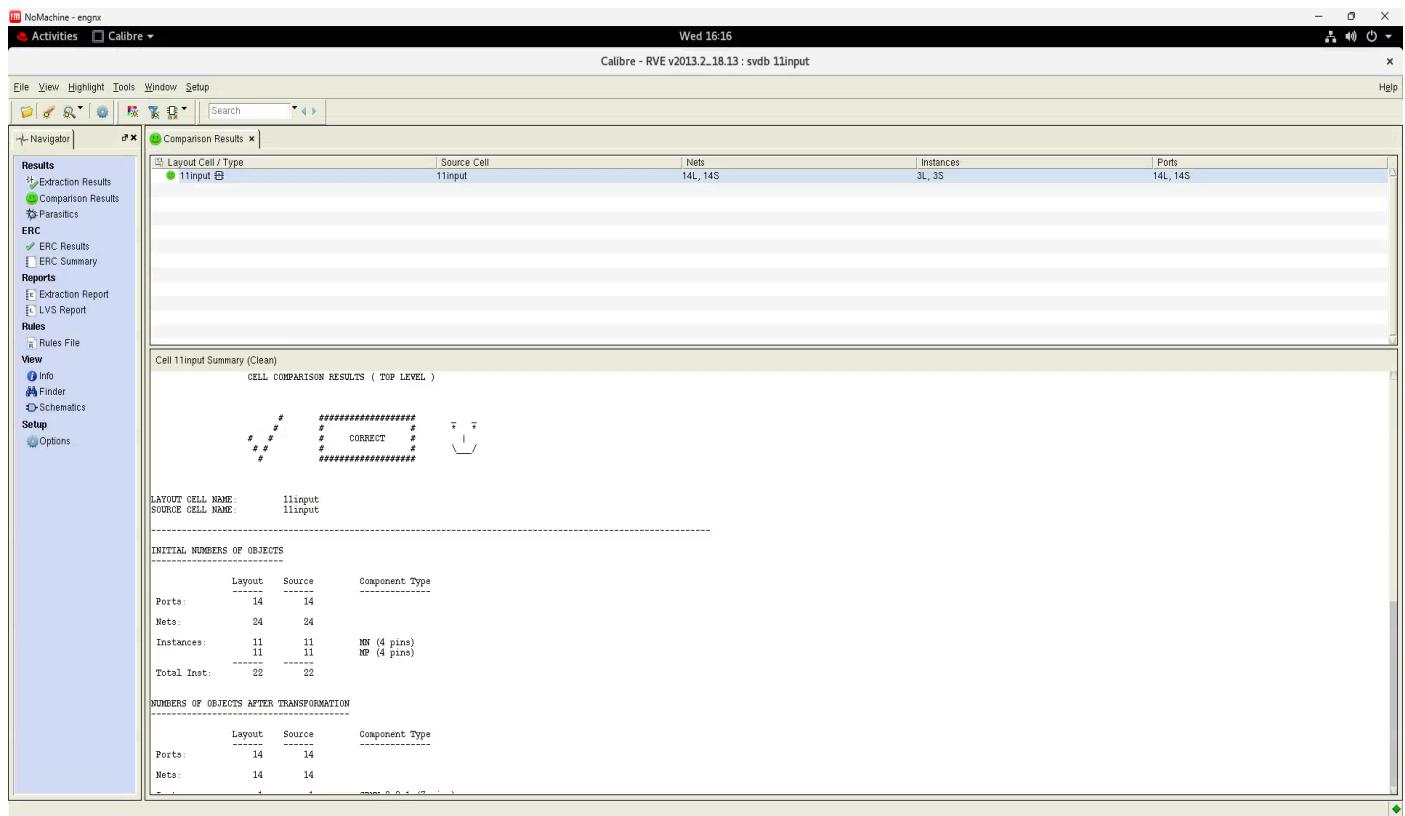
Offset (right side) = 0.552um



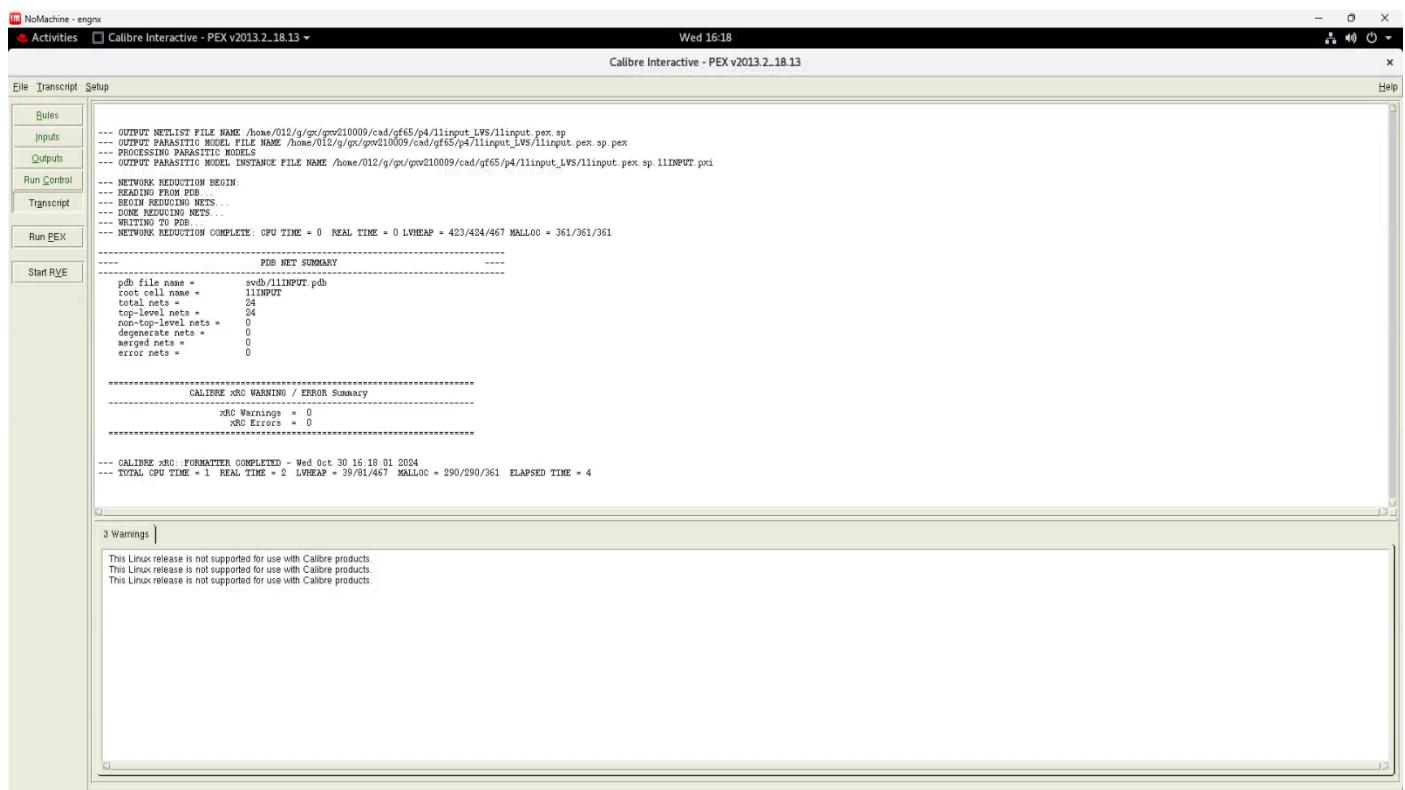
## DRC



LVS



PEX



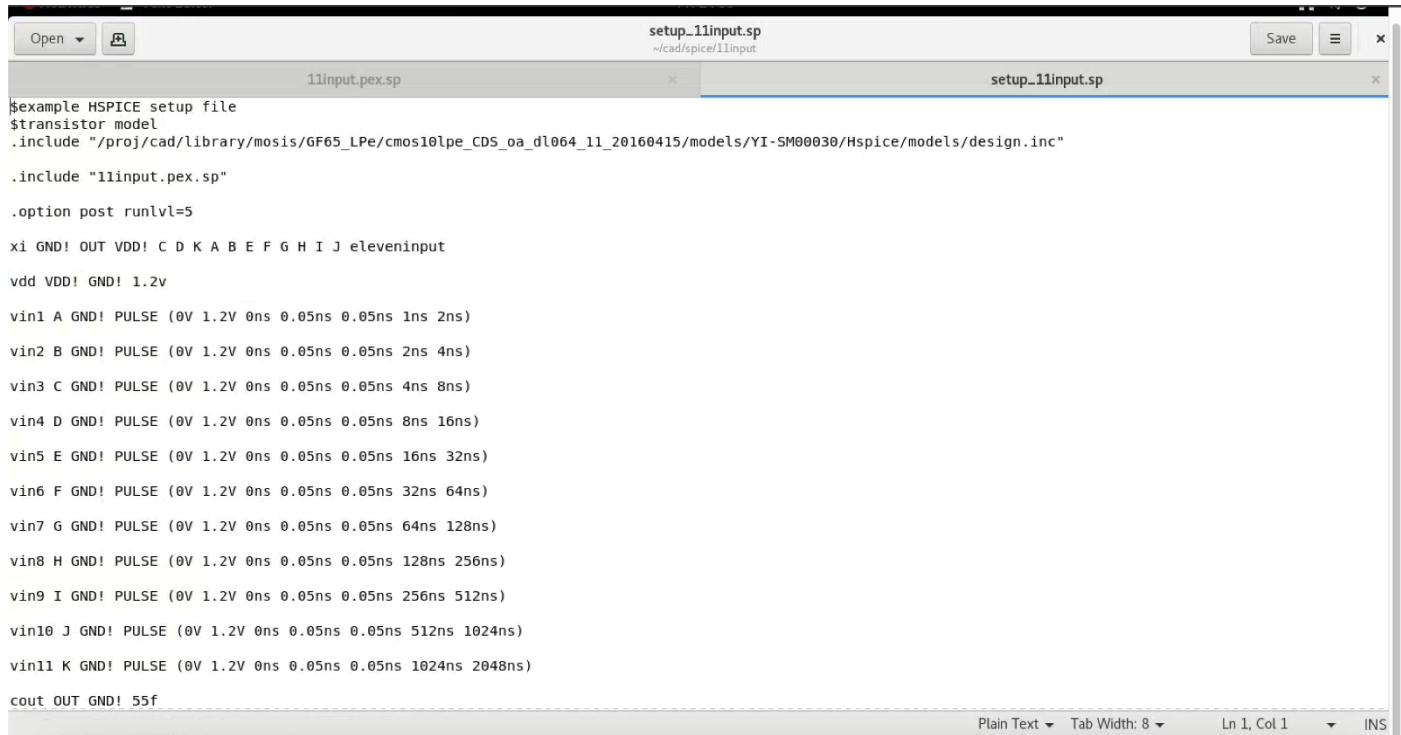
## PEX Netlist



The screenshot shows a software interface for editing a PEX netlist. The title bar reads "11input.pex.sp" and "cad/spice/11input". The main window contains a large amount of technical text representing the circuit's connections and components. The text includes various symbols like J, I, H, G, F, E, B, A, K, D, C, VDD!, OUT, GND!, and numerous labels such as MMN3, MMN4, PANW1, PANW2, PANW3, PANW4, PANW5, PANW6, and PANW7. It also includes parameters like L, W, AD, AS, PD, PS, and NRD. At the bottom right of the editor window, there are buttons for "Plain Text", "Tab Width: 8", "Ln 7, Col 15", and "INS".

```
* File: /home/012/g/gxv210009/cad/gf65/p4/11input_LVS/11input.pex.sp
* Created: Tue Oct 29 16:20:52 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "/home/012/g/gxv210009/cad/gf65/p4/11input_LVS/11input.pex.sp.pex"
.subckt eleveninput GND! OUT VDD! C D K A B E F G H I J
*
* J      J
* I      I
* H      H
* G      G
* F      F
* E      E
* B      B
* A      A
* K      K
* D      D
* C      C
* VDD!   VDD!
* OUT    OUT
* GND!   GND!
X00_noxref N_GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=8.75136e-12
+ PERIM=1.3616e-05
XMMN3_N_NET15_MMN3_d N_C_MMN3_g N_GND! MMN3_s N_GND! D0_noxref_pos NFET
+ L=6.2e-08 W=5.2e-07 AD=8.32e-14 AS=7.956e-14 PD=1.36e-06 PS=8.26e-07
+ NRD=0.192308 NRS=0.3 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=1.264e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN4_N_NET15_MMN4_d N_D_MMN4_g N_GND! MMN3_s N_GND! D0_noxref_pos NFET
+ L=6.2e-08 W=5.2e-07 AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07
+ NRD=0.307692 NRS=0.288462 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=5.28e-07 SB=8.96e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN2_N_NET16_MMN2_d N_K_MMN2_g N_NET15_MMN4_d N_GND! D0_noxref_pos NFET
+ L=6.2e-08 W=5.2e-07 AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07
+ NRD=0.276923 NRS=0.280769 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
```

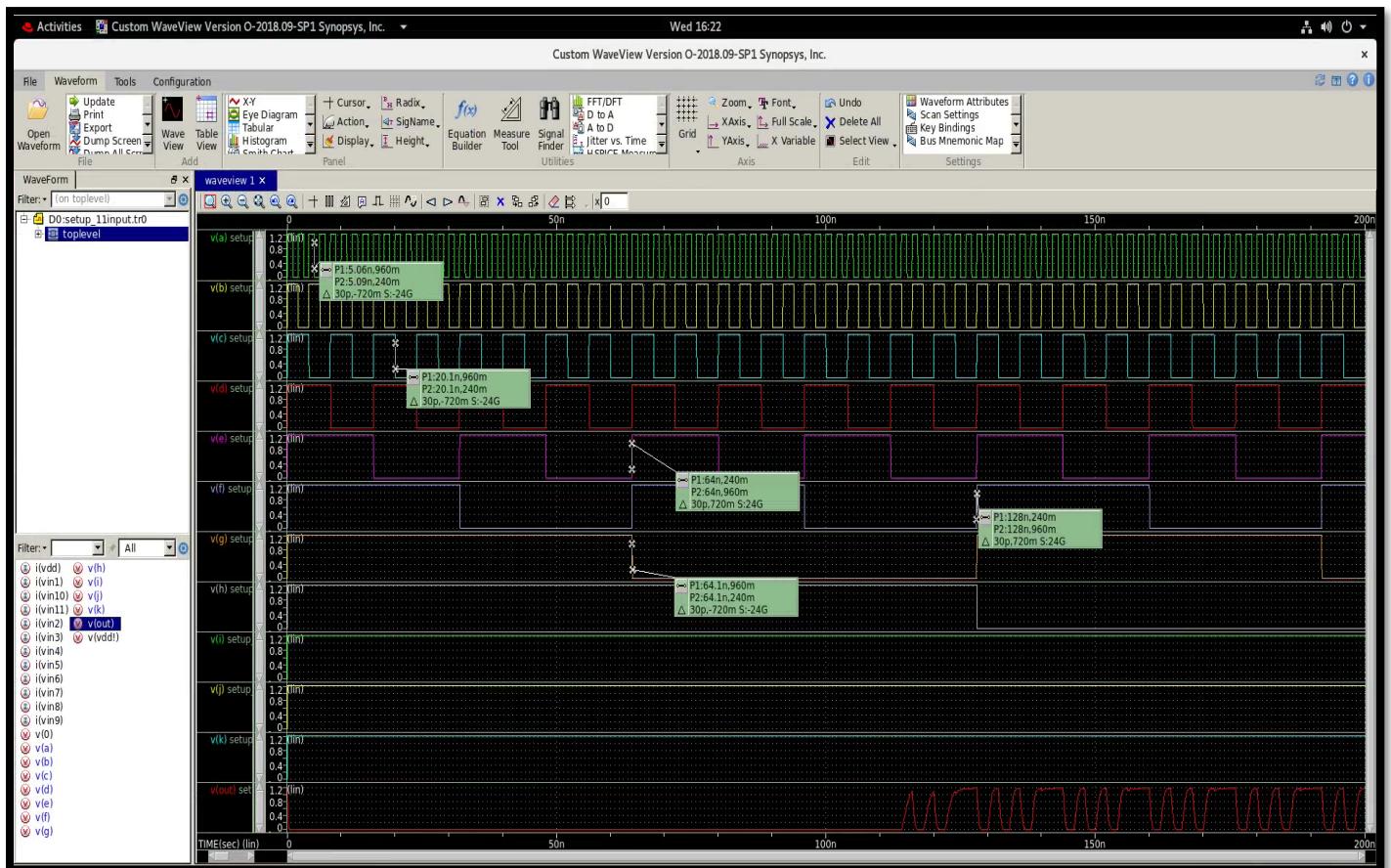
## HSpice Setup File



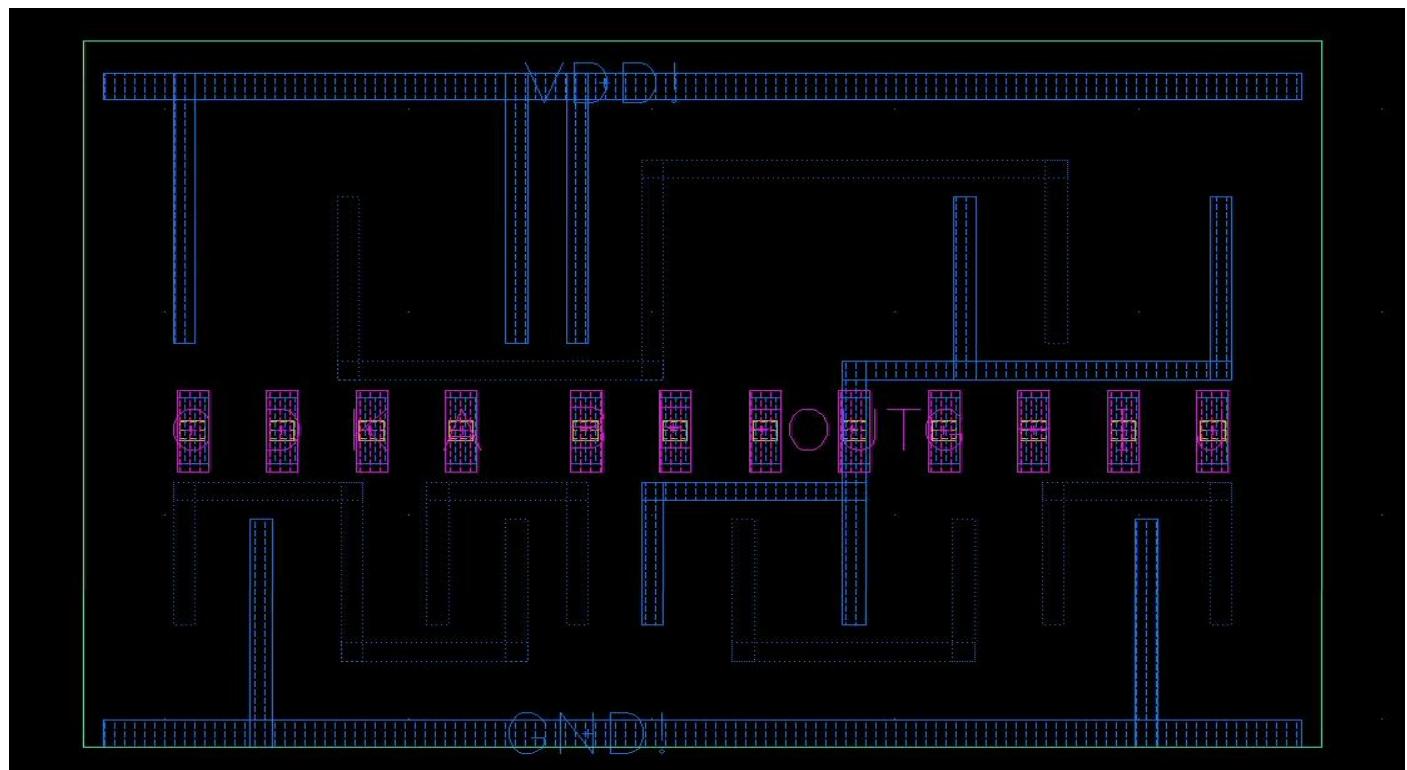
The screenshot shows a software interface for editing an HSpice setup file. There are two tabs visible: "11input.pex.sp" and "setup\_11input.sp". The "11input.pex.sp" tab is active and contains a script for setting up the simulation. It includes commands like \$example, \$transistor, .include, .option, .post, .runlvl, .model, .subckt, .param, .voltage, .current, .noise, .plot, .print, .end, and .quit. The "setup\_11input.sp" tab is also present but its content is not visible in the screenshot. At the bottom right of the editor window, there are buttons for "Plain Text", "Tab Width: 8", "Ln 1, Col 1", and "INS".

```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.option post runlvl=5
.model transistor model
.model diode diode
.model capacitor capacitor
.model inductor inductor
.model voltage voltage
.model current current
.noise
.plot
.print
.end
.quit
```

# Simulation Waveform



# Abstract View



# NOR3

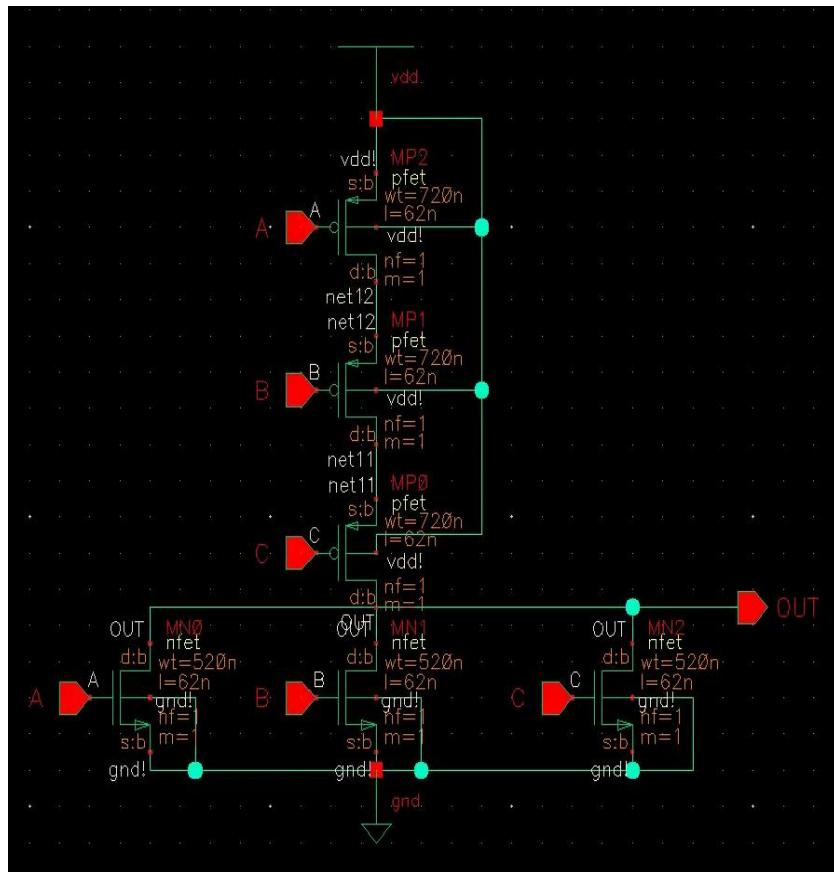
## Function

$$\text{OUT} = \text{NOT}(A|B|C)$$

## Truth Table

A	B	C	OUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

## Schematic

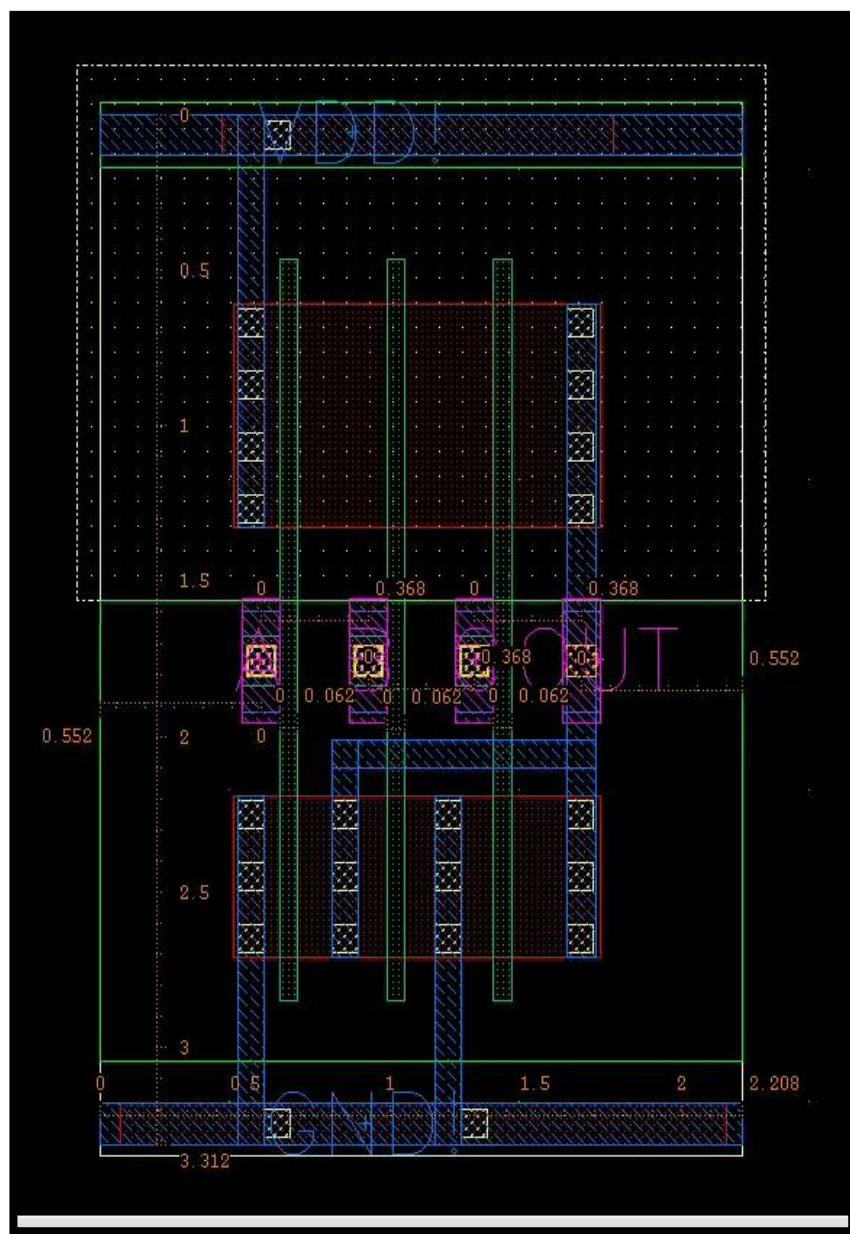


## Layout

Cell Height = 3.312 um

Cell Width = 2.208 um

Total Cell Area = 7.312 um<sup>2</sup>



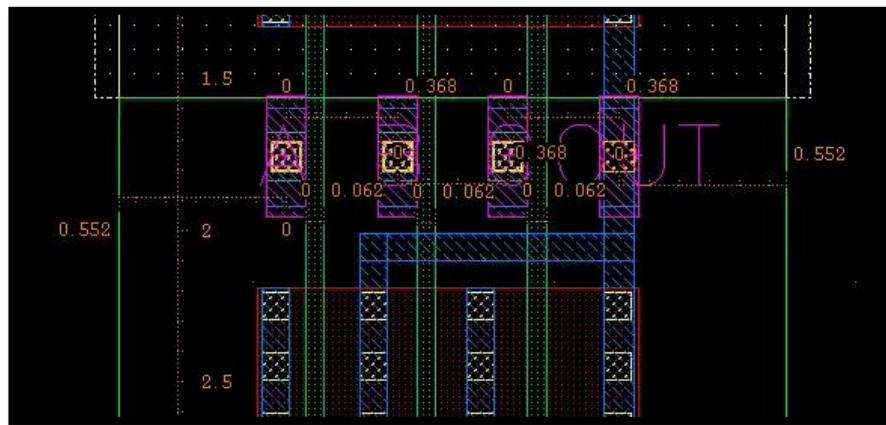
## Offset, Pin Pitch and Channel Length

Channel Length = 0.062um

Pin Pitch = 0.368um

Offset (left side) = 0.552um

Offset (right side) = 0.552um



## DRC

NoMachine - engnx

Activities Calibre Wed 19:10

Calibre - RVE v2013.2\_18.13 : nor3.drc.results

File View Highlight Tools Window Setup Help

Show All nor3, 0 Results (in 0 of 2078 Checks)

Check / Cell	Results
✓ Check_GRS2	0
✓ Check_GRS6	0
✓ Check_GRB_F01	0
✓ Check_GRSRB_BF01	0
✓ Check_GRB_BF02	0
✓ Check_GRB_BF03	0
✓ Check_GRB_BF04	0
✓ Check_GRB_BH01	0
✓ Check_GRB_BH02	0
✓ Check_GRSRB_BH02	0
✓ Check_GRB_BH03	0
✓ Check_GRB_BH04	0
✓ Check_GRSRB_BH04	0
✓ Check_GRB_DE01	0
✓ Check_GRB_DE02	0

Rule File Pathname: /home/012/g/px/gr210009/cad/gf65/p4/nor3.DRS/\_Calibre\_DRC\_rules\_.rule  
Rule File Title: YI-R70054.09 - YI-R70052.12  
Shapes with acute angles are prohibited (Except for PROTECT Layer)

## LVS

The screenshot shows the Calibre LVS interface. The top menu bar includes 'File', 'View', 'Highlight', 'Tools', 'Window', 'Setup', 'Activities' (selected), and 'Calibre'. The title bar displays 'Calibre - RVE v2013.2..18.13 : svdb nor3' and the date 'Wed 19:11'. The main window has a 'Navigator' sidebar on the left containing 'Results' (Extraction Results, Comparison Results, ERC Results, ERC Summary, Reports, Extraction Report, LVS Report), 'Rules' (Rules File), 'View' (Info, Finder, Schematics), and 'Setup' (Options). The central area shows 'Comparison Results' for 'Layout Cell / Type' 'nor3'. Below this is a 'Cell nor3 Summary (Clean)' section with 'CELL COMPARISON RESULTS (TOP LEVEL)' and a detailed report. The report includes:  
 - LAYOUT CELL NAME: nor3  
 - SOURCE CELL NAME: nor3  
 - INITIAL NUMBERS OF OBJECTS:  

	Layout	Source	Component Type
Ports:	6	6	
Nets:	8	8	
Instances:	3	3	MN (4 pins) MP (4 pins)
Total Inst:	6	6	

  
 - NUMBERS OF OBJECTS AFTER TRANSFORMATION:  

	Layout	Source	Component Type
Ports:	6	6	
Nets:	6	6	

## PEX

The screenshot shows the Calibre Interactive PEX interface. The top menu bar includes 'File', 'Transcript' (selected), 'Setup', 'Activities' (selected), and 'Calibre'. The title bar displays 'Calibre Interactive - PEX v2013.2..18.13' and the date 'Wed 19:12'. The main window has a 'Run Control' sidebar with tabs for 'Rules', 'Inputs', 'Outputs', 'Run Control' (selected), 'Transcript' (selected), 'Run PEX', and 'Start RVE'. The central area shows a transcript of the PEX run:  

```

    --- OUTPUT NETLIST FILE NAME /home/012/g/gx/gxxv210009/cad/qf65/p4/nor3_LVS/nor3.pex.sp
    --- OUTPUT PARASTATIC MODEL FILE NAME /home/012/g/gx/gxxv210009/cad/qf65/p4/nor3_LVS/nor3.pex.sp.pex
    --- PROCESSING PARASTATIC MODELS
    --- OUTPUT PARASTATIC MODEL INSTANCE FILE NAME /home/012/g/gx/gxxv210009/cad/qf65/p4/nor3_LVS/nor3.pex.sp.NOR3.pxi
    --- NETWORK REDUCTION BEGIN
    --- READING FROM PDB
    --- FINDING ALL THE NETS ...
    --- DONE REDUCING NETS ...
    --- WRITING TO PDB ...
    --- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 423/424/467 MALLOC = 360/360/360
    -----
    ----- PDB NET SUMMARY -----
    pdb file name = svdb/NOR3.pdb
    root cell name = NOR3
    total nets = 8
    top level nets = 0
    non-top-level nets = 0
    degenerate nets = 0
    merged nets = 0
    error nets = 0

    -----
    ----- CALIBRE XRC WARNING / ERROR Summary -----
    XRC Warnings = 0
    XRC Errors = 0
    -----
    --- CALIBRE XRC FORMATTER COMPLETED - Wed Oct 30 19:12:34 2004
    --- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 290/290/360 ELAPSED TIME = 5
  
```

The bottom right corner of the transcript window shows a message: '3 Warnings'.

## PEX Netlist

The screenshot shows a terminal window titled "NoMachine - gdcbm" with the file "nor3.pex.sp" open. The content of the file is a detailed PEX (Parameter Extraction) netlist for a NOR3 gate. It includes header information, component definitions, and various parameters such as NFET, PFET, and PTWELL values. The netlist is extensive, listing multiple nodes and their connections.

```
* File: /home/012/g/gx/gxv210009/cad/gf65/p4/nor3_LVS/nor3.pex.sp
* Created: Tue Oct 29 11:26:39 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "/home/012/g/gx/gxv210009/cad/gf65/p4/nor3_LVS/nor3.pex.sp.pex"
.subckt nor3 GND! OUT VDD! A B C
*
* C      C
* B      B
* A      A
* VDD!   VDD!
* OUT    OUT
* GND!   GND!
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=3.44e-12
+ PERIM=7.44e-06
XMMN0 N OUT MMN0_d N_A MMN0_g N_GND!_MMN0_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=8.32e-14 PD=8.26e-07 PS=1.36e-06 NRD=0.315385
+ NRS=0.192308 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.6e-07
+ SB=1.042e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN1 N OUT MMN1_d N_B MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=7.956e-14 AS=7.956e-14 PD=8.26e-07 PS=8.26e-07 NRD=0.273077
+ NRS=0.288462 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.28e-07
+ SB=6.74e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0
+ PANW7=1.054e-14 PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMMN2 N_OUT_MMN2_d N_C_MMN2_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6.2e-08
+ W=5.2e-07 AD=1.5912e-13 AS=7.956e-14 PD=1.652e-06 PS=8.26e-07 NRD=0.453846
+ NRS=0.3 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=8.96e-07 SB=3.06e-07
+ SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=1.054e-14
+ PANW8=1.24e-14 PANW9=9.3e-15 PANW10=0
XMP2_NET12 N_A MMP2_g N_VDD!_MMP2_s N_VDD!_D0_noxref_neg PFET L=6.2e-08
+ W=7.2e-07 AD=1.1016e-13 AS=1.152e-13 PD=1.026e-06 PS=1.76e-06 NRD=0.2125
+ NRS=0.138889 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07
+ SB=1.042e-06 SD=0 PANW1=4.092e-15 PANW2=3.1e-15 PANW3=3.1e-15 PANW4=3.1e-15
+ PANW5=3.1e-15 PANW6=5.084e-14 PANW7=1.4508e-14 PANW8=2.1948e-14 PANW9=2.48e-14
+ PANW10=4.9972e-14
```

## HSpice Setup File

The screenshot shows a terminal window titled "Text Editor" with the file "setup\_nor3.sp" open. The content is an HSpice setup script for a NOR3 gate. It includes directives like \$example, \$transistor, .include, .option, .model, .param, .param, .vin, .vdd, .cout, .transient, and .end. The script defines the NOR3 model, sets simulation parameters, and specifies voltage levels for the inputs and output.

```
$example HSPICE setup file
$transistor model
.include "/proj/cad/library/mosis/GF65_LPe_cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "nor3.pex.sp"

.option post runlvl=5

xi GND! OUT| VDD! A B C nor3

vdd VDD! GND! 1.2V

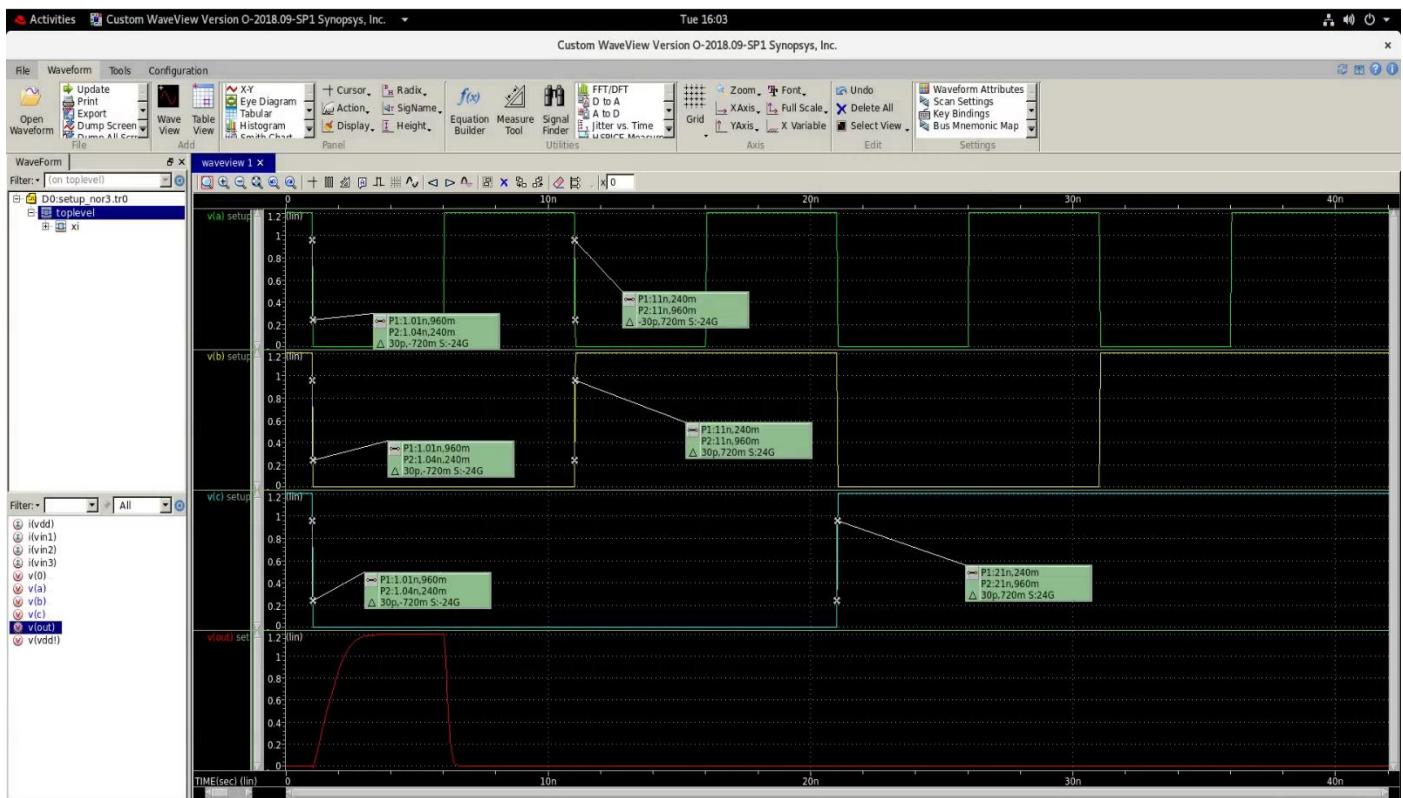
vin1 A GND! pwl(0ns 1.2V 1ns 1.2V 1.05ns 0V 6ns 0V 6.05ns 1.2V 11ns 1.2V 11.05ns 0V 16ns 0V 16.05ns 1.2V 21ns 1.2V 21.05ns 0V 26ns 0V 26.05ns 1.2V 31ns 1.2V
31.05ns 0V 36ns 0V 36.05ns 1.2V 41ns 1.2V)
vin2 B GND! pwl(0ns 1.2V 1ns 1.2V 1.05ns 0V 11ns 0V 11.05ns 1.2V 21ns 1.2V 21.05ns 0V 31ns 0V 31.05ns 1.2V 41ns 1.2V)
vin3 C GND! pwl(0ns 1.2V 1ns 1.2V 1.05ns 0V 21ns 0V 21.05ns 1.2V 41ns 1.2V)

cout OUT GND! 55f

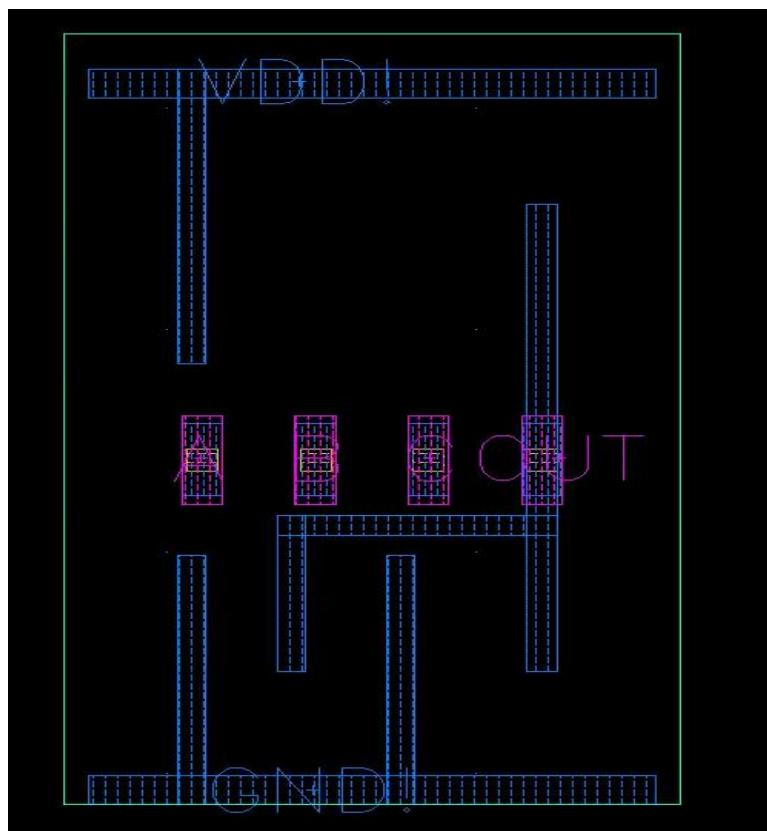
$transient analysis
.tr 100ps 42ns

.end
```

# Simulation Waveforms



# Abstract View

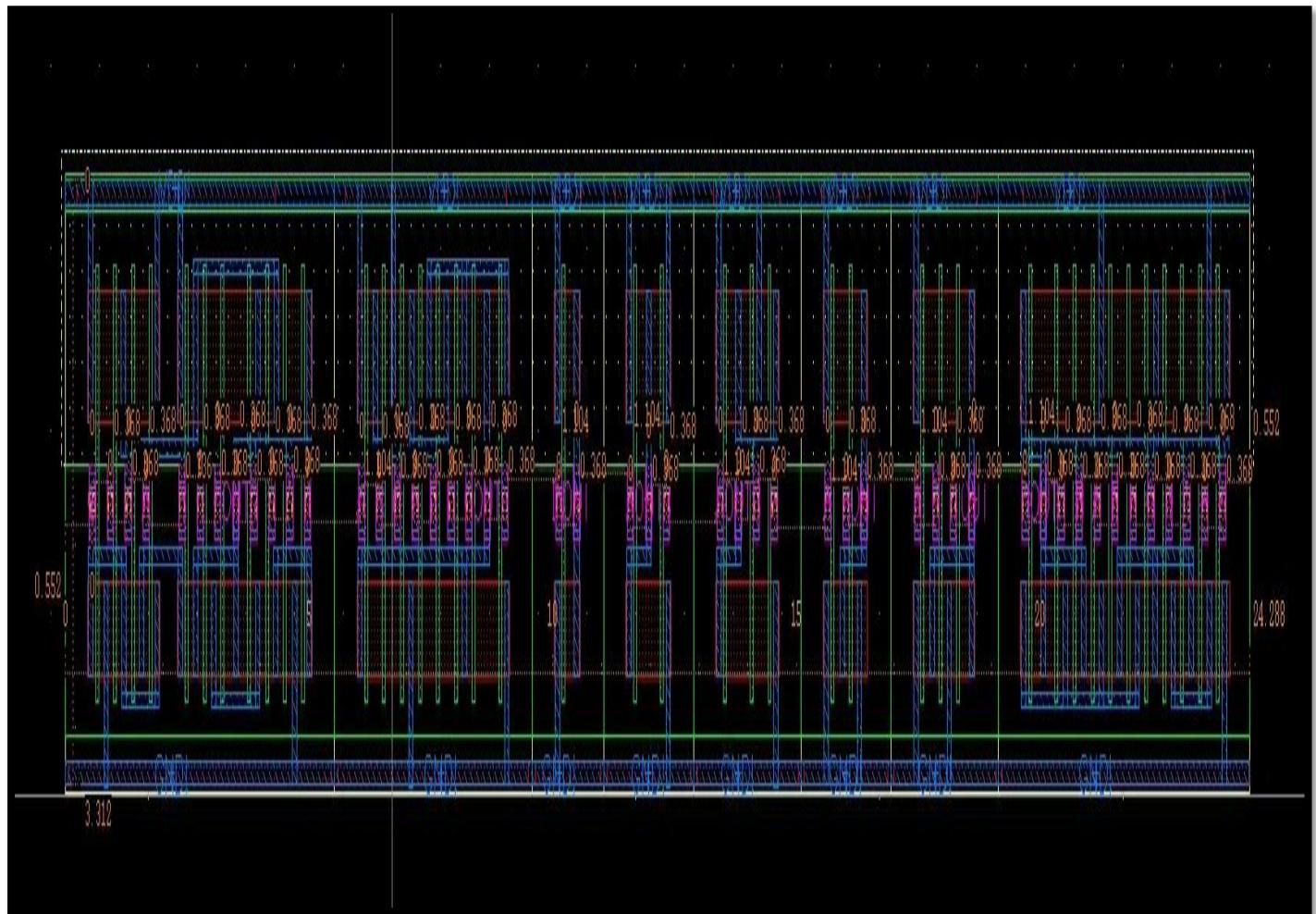


## Layout of all cells together

Cell Height = 3.312 um

Cell Width = 24.288um

Total Cell Area = 80.44 um<sup>2</sup>



# DRC Results of all the cells combined in a layout

The screenshot shows the Calibre DRC interface with the following details:

- Title Bar:** NoMachine - engnx, Activities, Calibre, Fri 10:15, Calibre - RVE v2013.2\_18.13 : combined.drc.results
- Menu Bar:** File, View, Highlight, Tools, Window, Setup, Help.
- Toolbar:** Includes icons for Open, Save, Print, Undo, Redo, Cut, Copy, Paste, Find, Replace, and Search.
- Search Bar:** Search [Search] [Find] [Replace]
- Results List:** A table titled "Check / Cell" showing 2078 checks. All checks are marked as successful (green checkmark) and have a result of 0. The columns are "Check / Cell" and "Results".
- Message Bar:** Rule File Pathname: /home/012/gx/grv210003/cad/qf65/p4/combined\_DRC/\_Calibre\_DRC\_rules\_. Rule File Title: YI-DM00054.09 - YI-RT00052.12. Shapes with outer angles are prohibited (Except for PROTECT Layer).
- Status Bar:** Check GR52