OBJECTIVE:

This project uses the GF65nm process and Cadence design tools to design the layout and characterize an inverter. The power and ground pins in the layout are named VDD! and GND!. Likewise, the input and output pins are capitalized and named IN and OUT in both schematic and layout. The VDD value is assigned as 1.2V and the ground as 0V. The CMOS inverter is designed with specific values: the width of the PMOS (Wp) is 1.9 µm, the width of the NMOS (Wn) is 1.5 µm, and the load capacitance (Cload) is 20 fF. **The channel length is 65 nm. The main design objective of the project is to minimize the bounding area (height × width) of the inverter layout.**

ABSTRACT:

Various drawing layers in the LSW pane were used to create the layout in the Virtuoso Layout Editing Window, including NW, RX, JZ, JX, PC, CA, M1, V1, and M2. The layout was designed according to specific metric values, with the pin pitch being a multiple of 0.26 and the offset value defined as (0.13 + 0.26 × n). The poly gates of the transistors were also aligned vertically in the design.

After designing the layout, the DRC (Design Rule Check) is run. A DRC result with 0 errors indicates that the layout is ready for fabrication; however, this does not guarantee functional correctness. Therefore, an LVS (Layout Versus Schematic) check is performed to ensure that the layout matches the schematic.

Once these checks are completed, parasitic capacitance and resistance values are extracted using PEX. HSPICE is then used to generate the SPICE netlist file. The output log from HSPICE is examined to determine whether the simulation completed successfully; otherwise, errors are indicated.

Finally, the HSPICE setup file is run, and with the help of WaveView, the waveforms of the desired signals are analyzed.

LAYOUT:

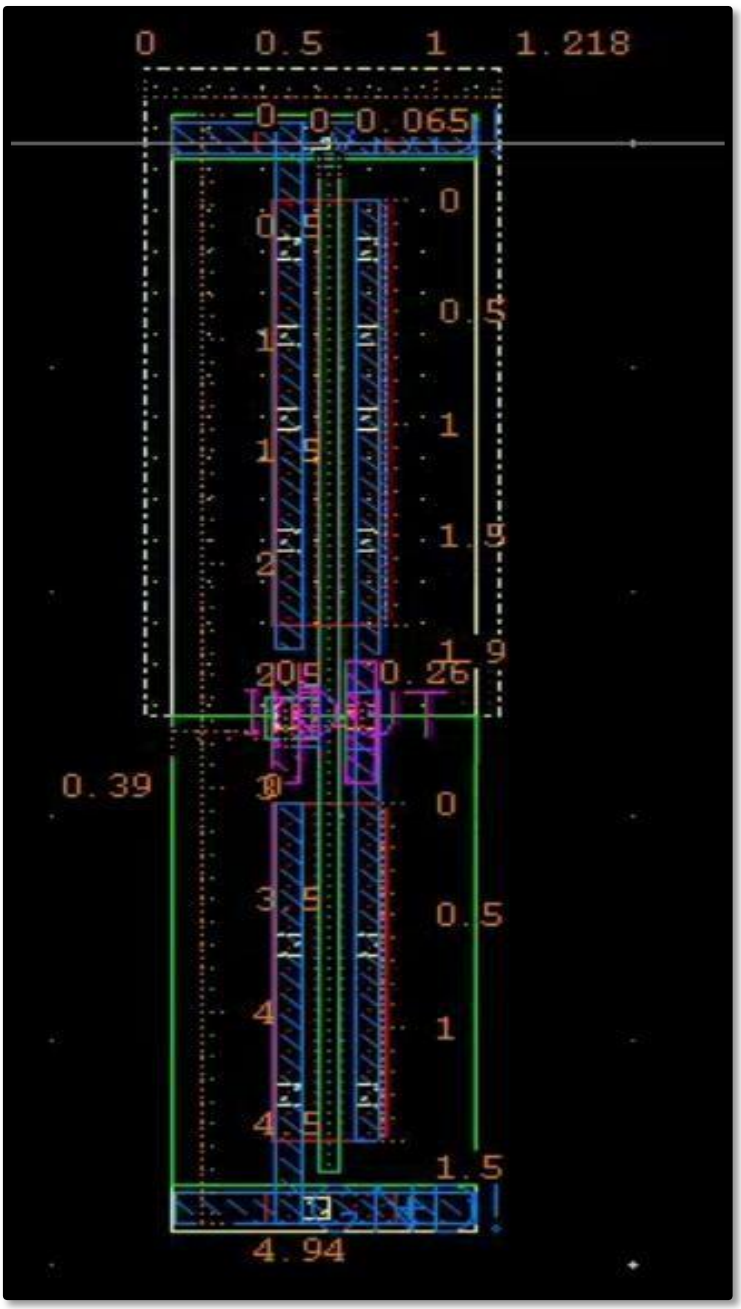

Figure 1. Inverter Layout

DIMENSIONS OF THE LAYOUT:

Height = 4.94um
Width = 1.218um
Width of PMOS = 1.9um
Width of NMOS = 1.5um
Cell ratio = Width of PMOS/ Width of NMOS = 1.266
Length = 0.065um
Area = 4.94 * 1.218 = 6.016 um^2
EDP = 1.728 * 10^-24 Js

SCHEMATIC:

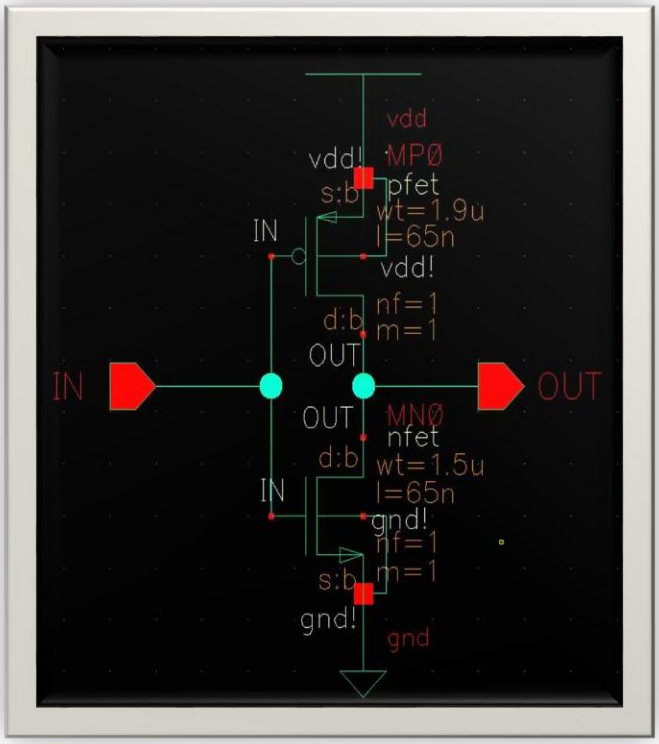

Figure 2. Schematic view of Inverter

DRC CHECK (Design Rule Check):

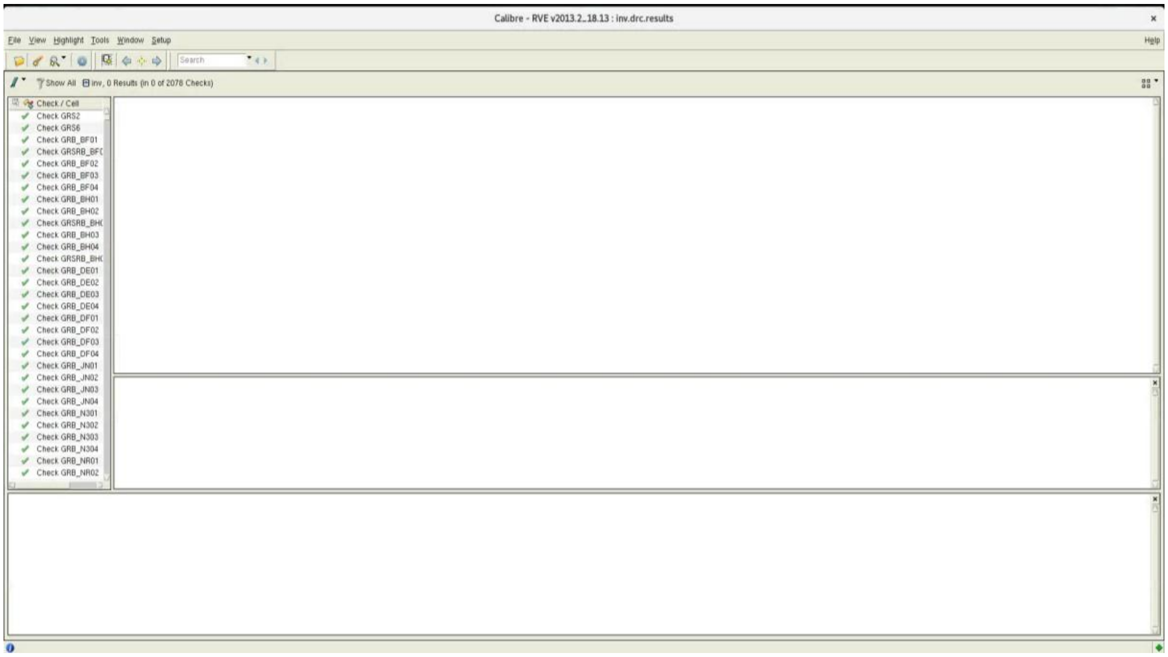

Figure 3. DRC Check Results

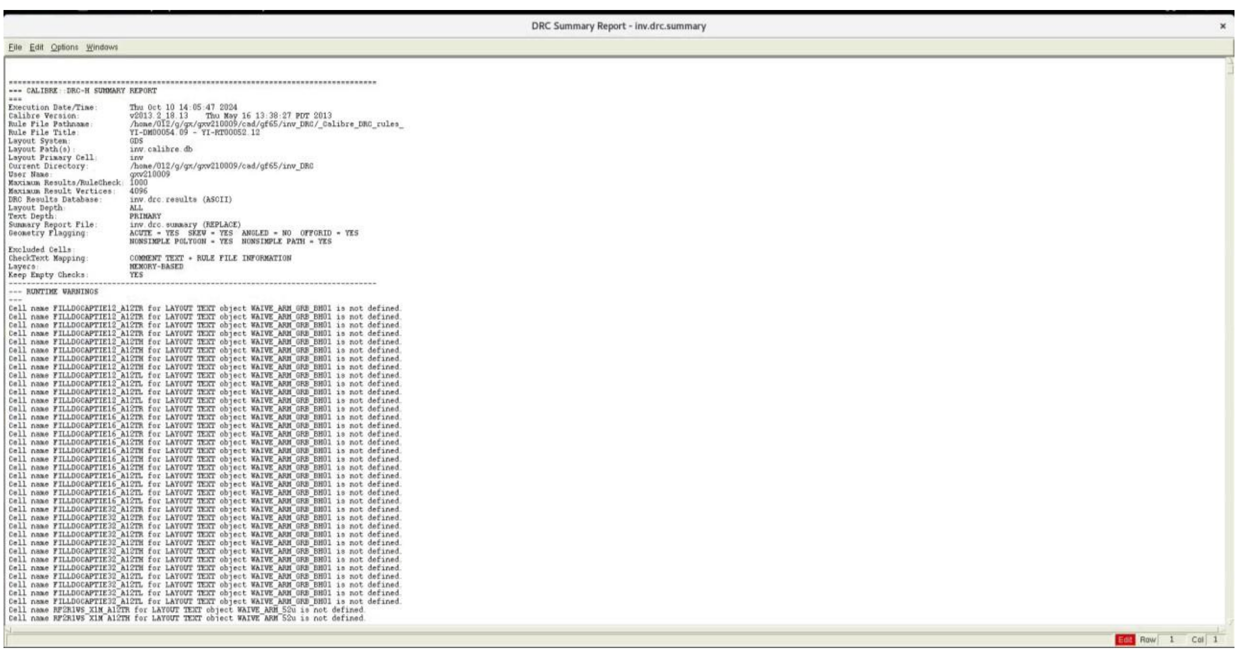

Figure 4. DRC Summary Report

LVS CHECK (LAYOUT VERSUS SCHEMATIC CHECK):

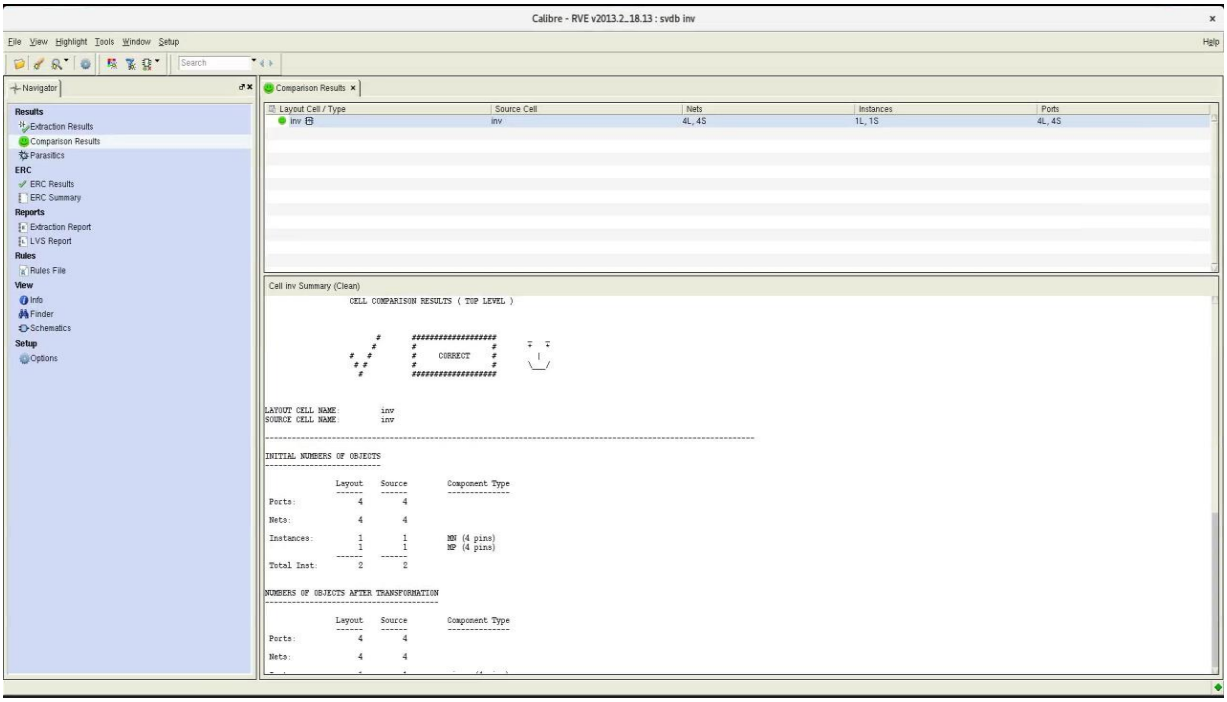

Figure 5. Layout VS Schematic Check

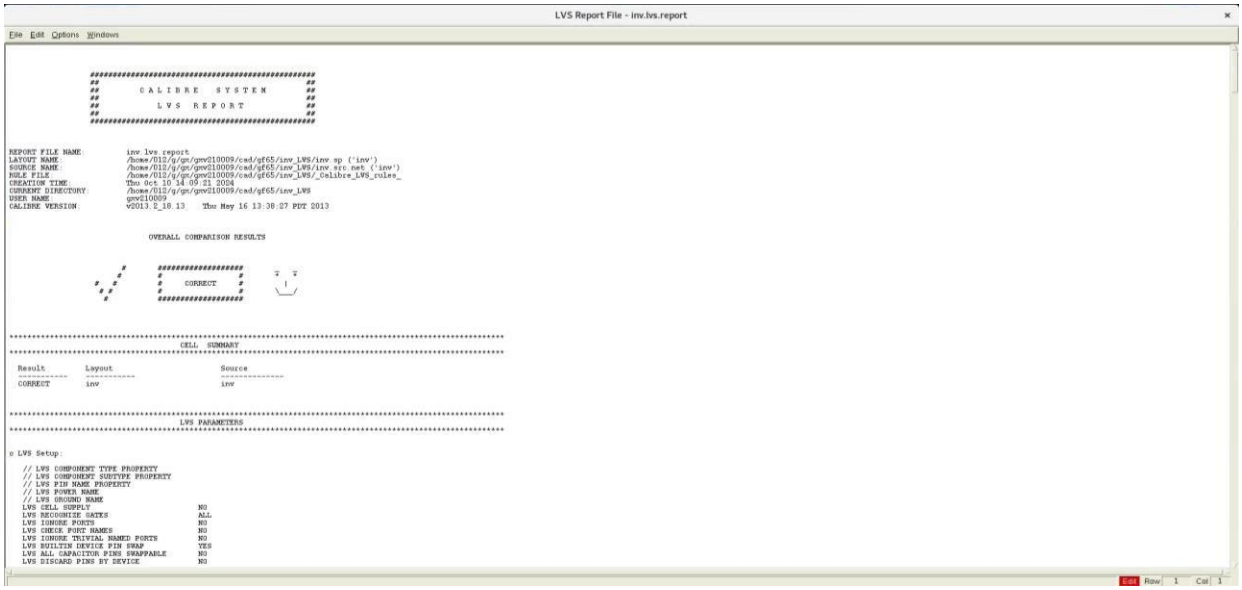

Figure 6. LVS Report

SPICE TEST SETUP FILE:

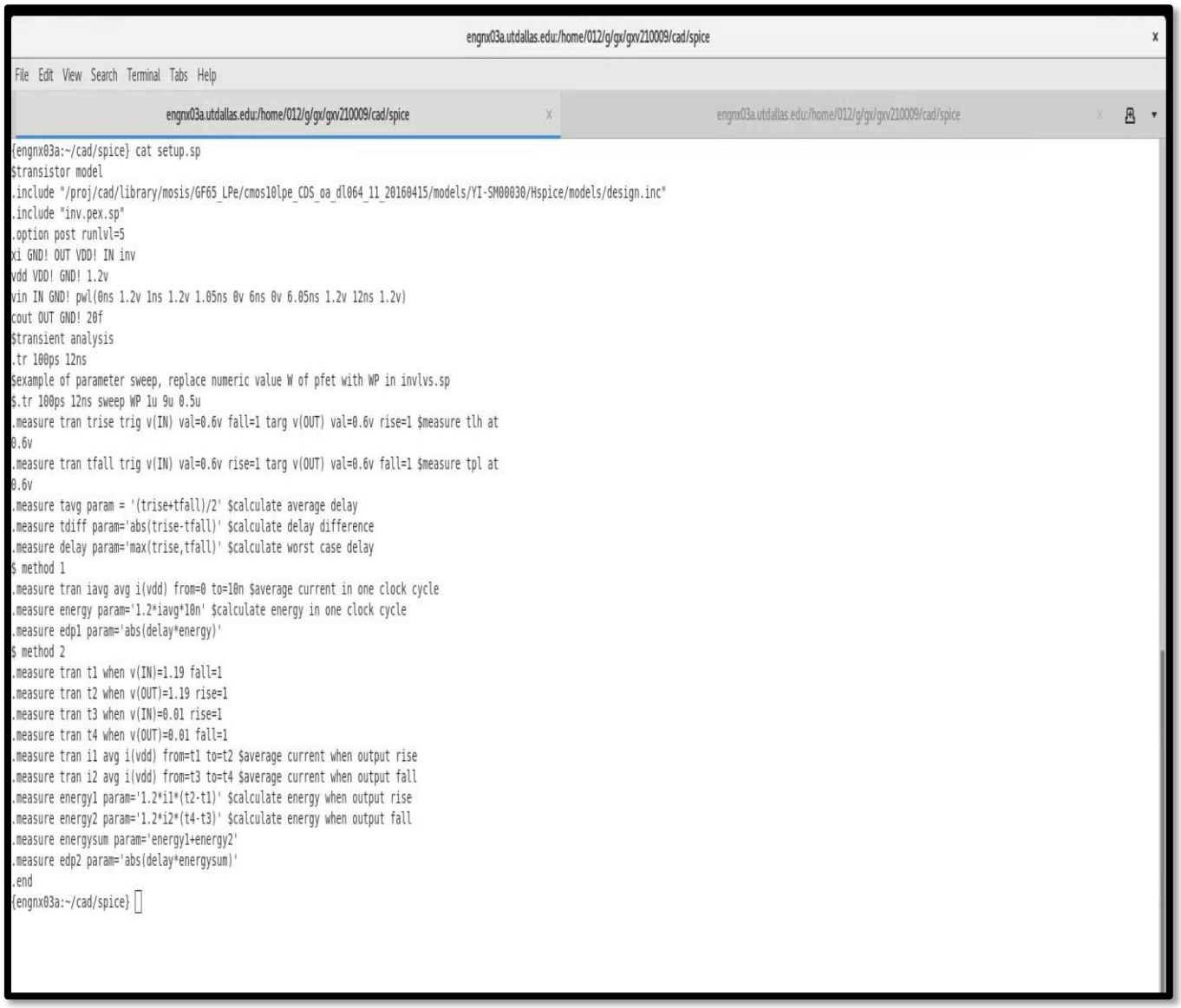

Figure 7. Inverter SPICE Test Setup File

INPUT AND OUTPUT WAVEFORMS:

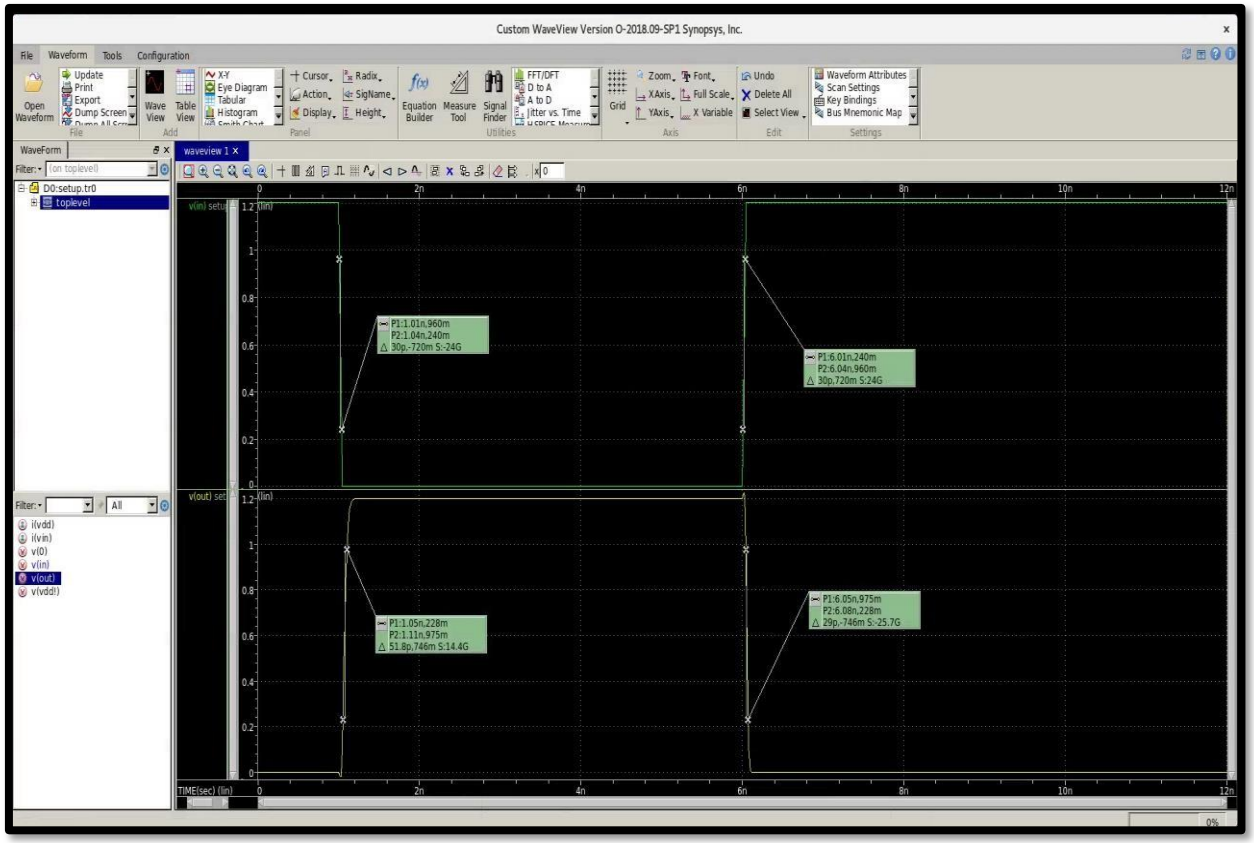

Figure 8. Waveforms representing the Slew Rate for both Input and Output

The slew rate for the input waveform is 30 ps. Slew rate is defined as the time it takes for the input signal to transition from low (0.2 × VDD) to high (0.8 × VDD) and vice versa.

For the output waveform:

- The rising edge slew is 51.8 ps.
- The falling edge slew is 29 ps.

Calculations:

- Output rising edge rate = (P2 – P1) / 51.8 ps = (975 mV – 228 mV) / 51.8 ps = **14.42 mV/ps**
- Output falling edge rate = (P1 – P2) / 29 ps = (975 mV – 228 mV) / 29 ps = **25.75 mV/ps**

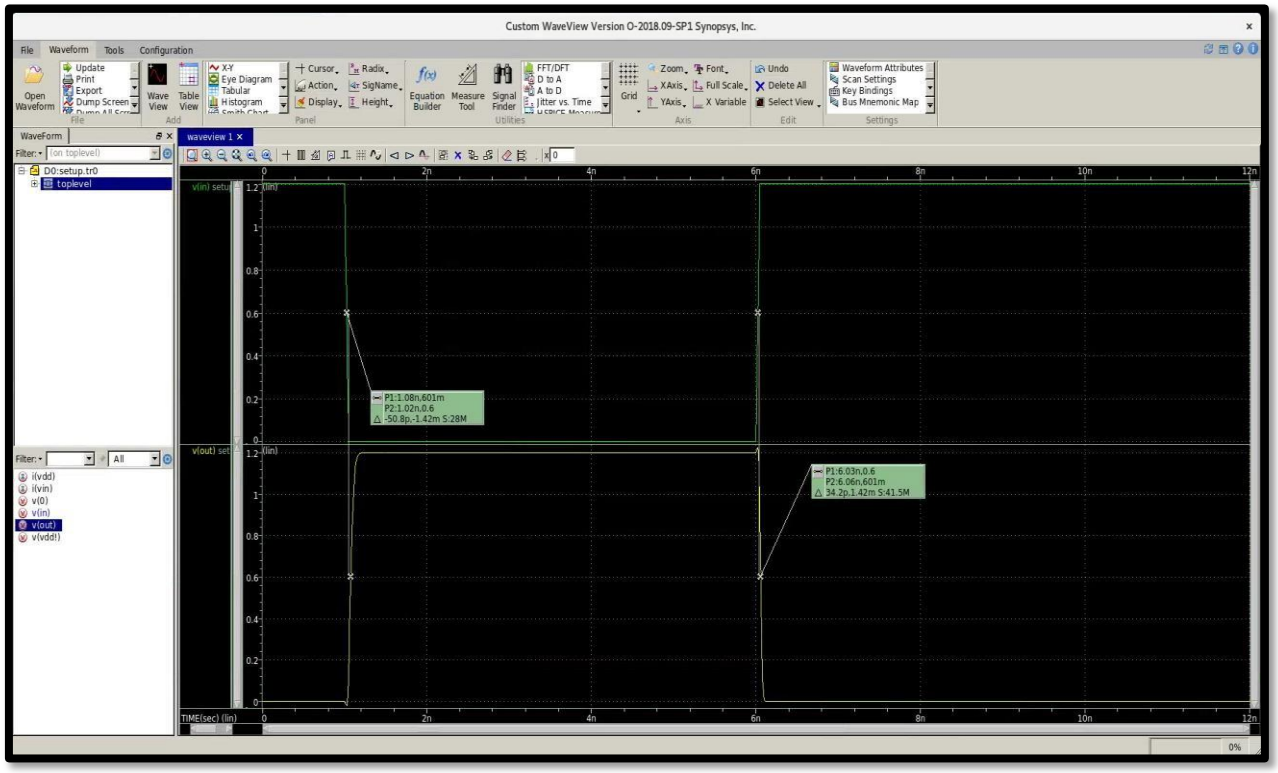

Figure 9. t_{LH} and t_{HL} Waveforms

OUTPUT METRICES:

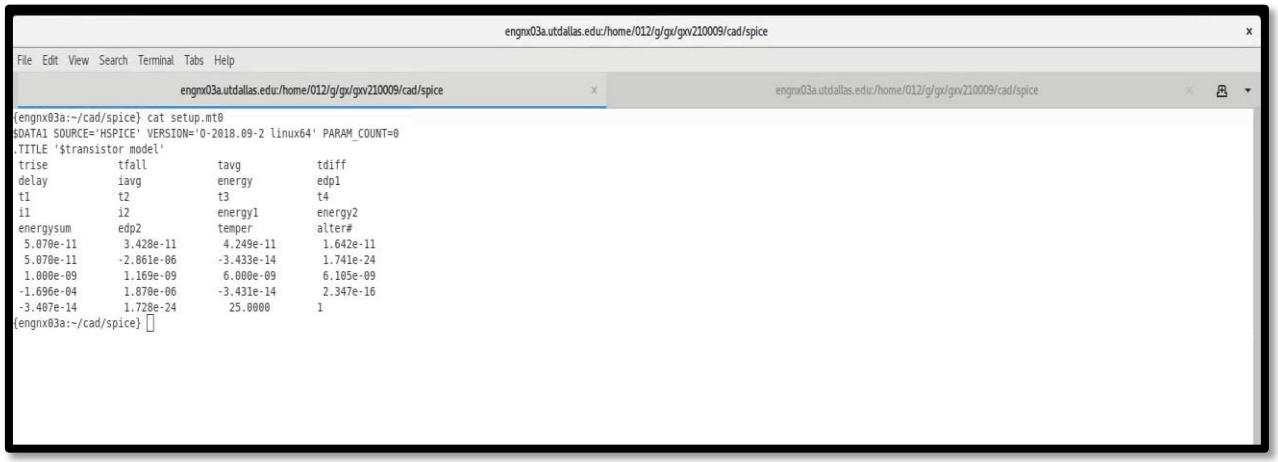

Figure 10. Parameters and their corresponding values

EXTRACTED SPICE NETLIST:

Figure 11. Inverter Parasitic Capacitance and Resistance Values Extraction File