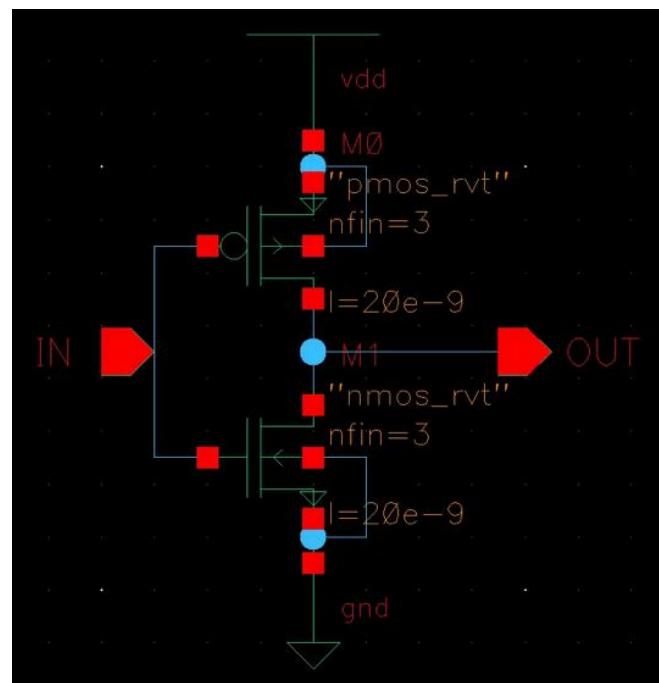
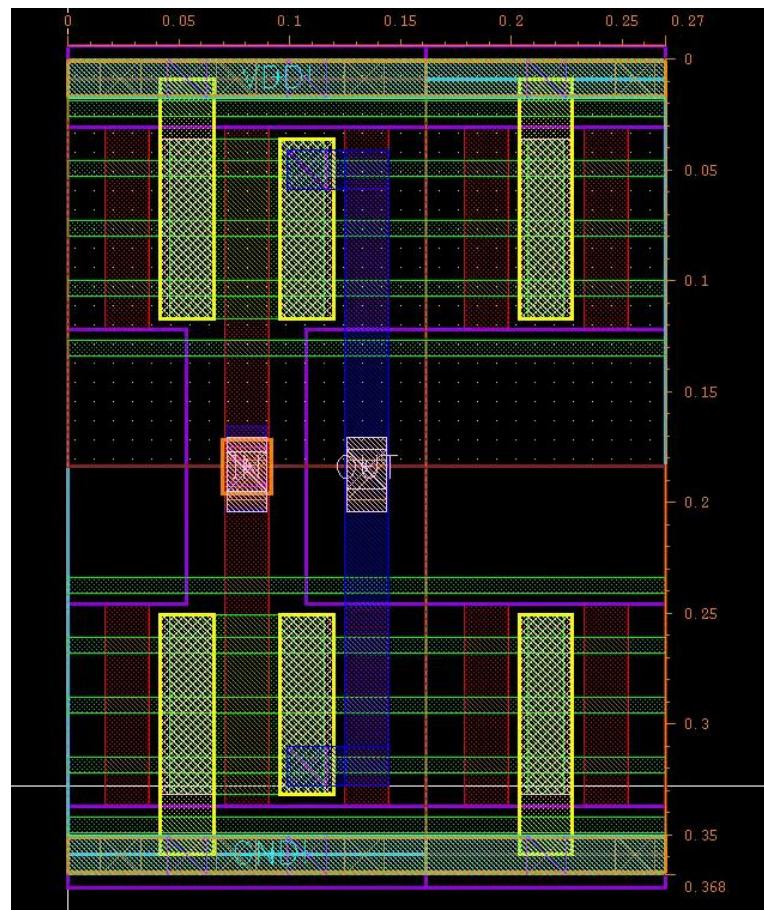


CELL#1: INVERTER:

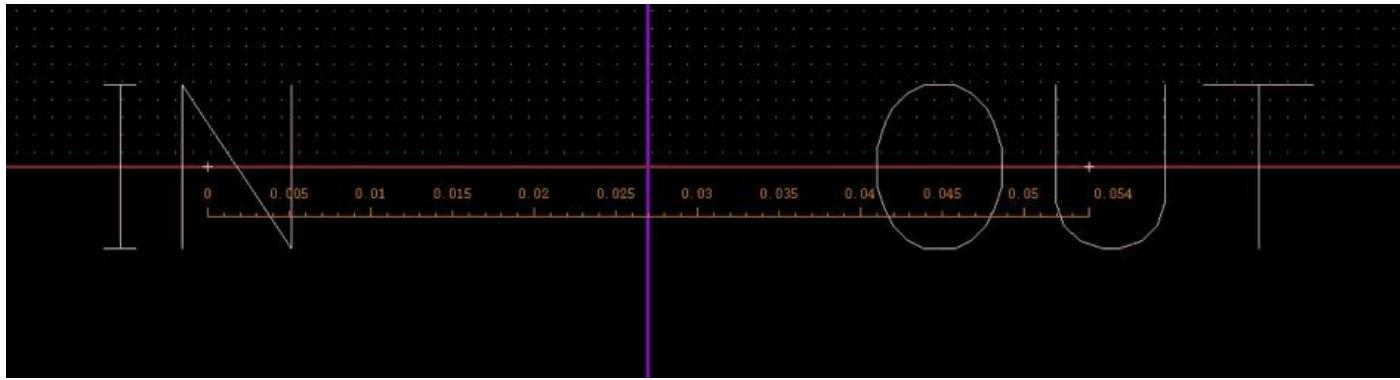
SCHEMATIC:



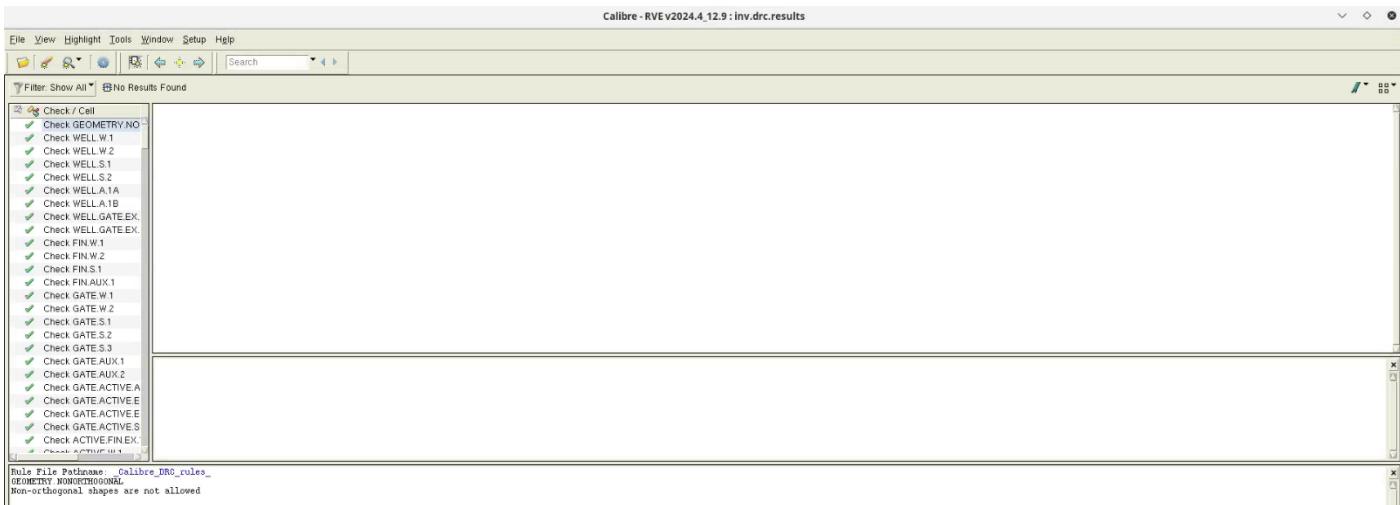
LAYOUT:



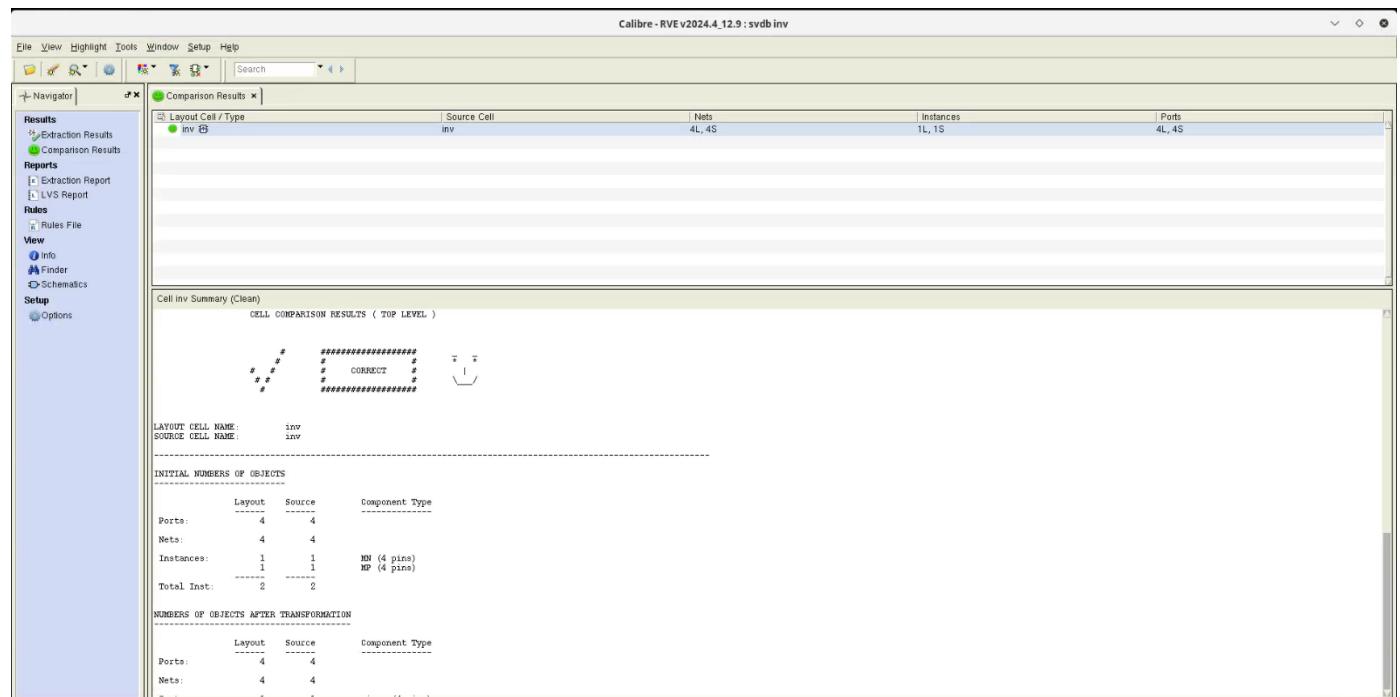
PIN_SPACING:



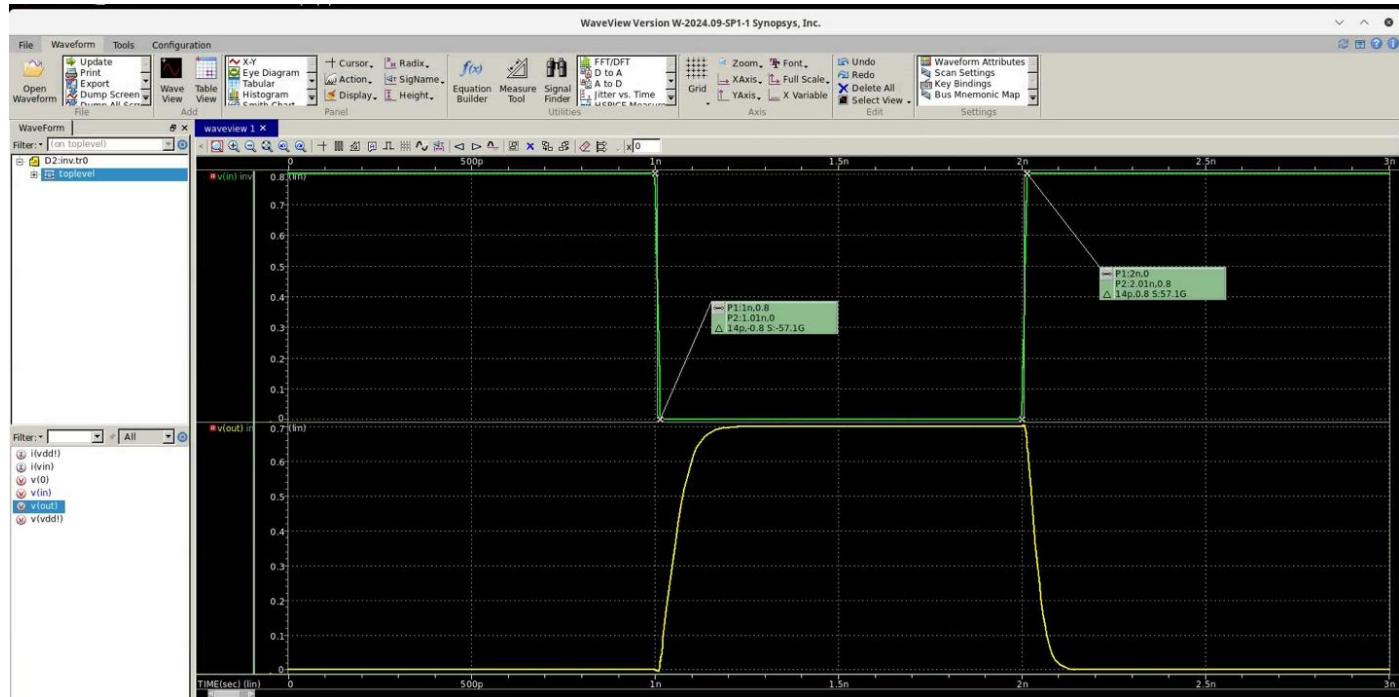
DRC CHECK:



LVS CHECK:



WAVEFORM:



Hspice file:

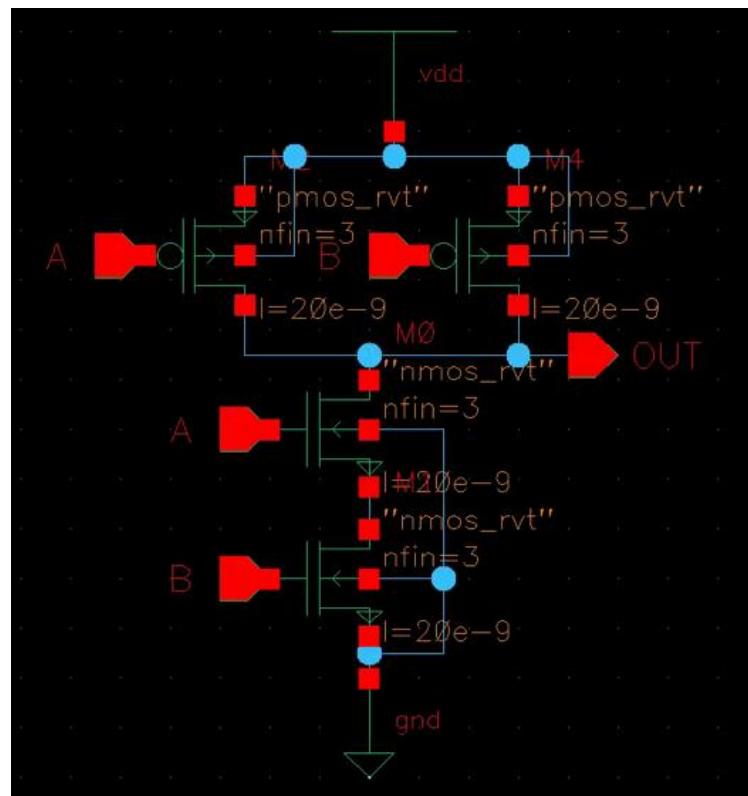
```
.include "~/asap7/7nm_TT.pm"
.include inv.pex.netlist
.option post runlvl=5
xi IN OUT inv
VDD! VDD! GND! 0.7v
vin IN GND! pwl(0ps 0.8v 1000ps 0.8v 1014ps 0v 2000ps 0v 2014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 3000ps
.end
```

LIB FILE:

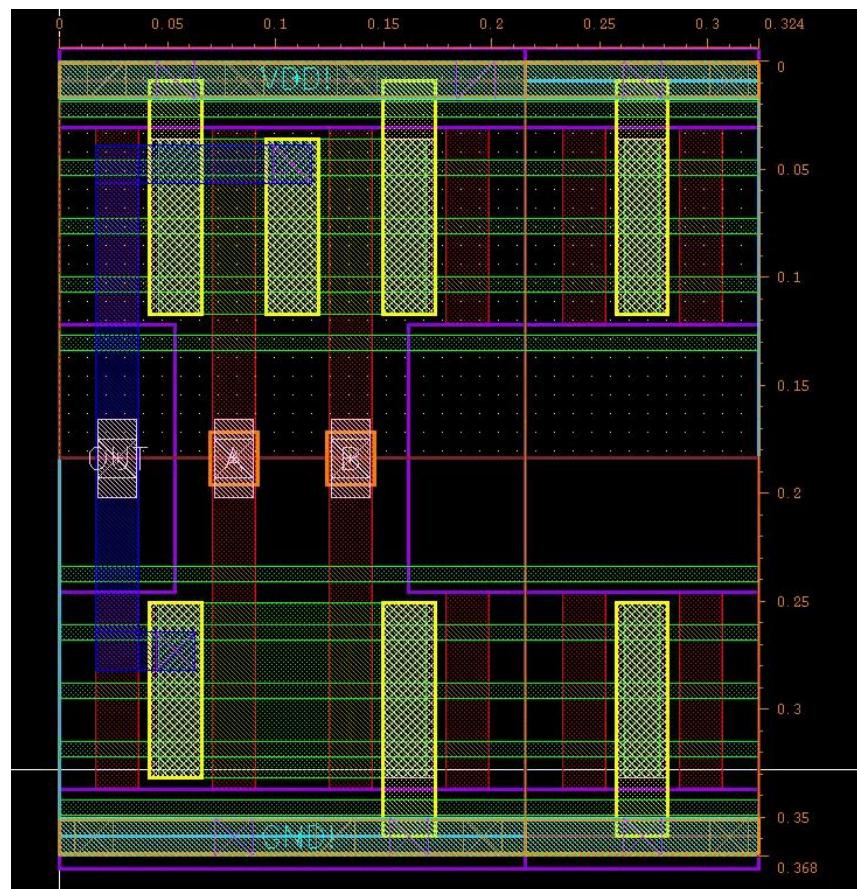
```
Cell INV configured for characterization.
Fri Mar 21 20:28:41 CDT 2025: Done configure stage (Elapsed: 0 seconds | 0.00 hours Memory: 792.92MB)
=====
pl_cci> characterize
=====
Fri Mar 21 20:29:08 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 20:29:08 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 20:29:08 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 20:29:08 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 20:29:08 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Library has standard-cells
INV: generated 7 tasks (7 total)
Using 1 standalone slots
[CDPL] Tasks: 0/7, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 7/7, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: INV::leakage_power_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Fri Mar 21 20:30:08 2025: Released license FEATURE PrimeLib_CORE(all)
Fri Mar 21 20:30:08 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 20:30:08 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1080.94MB)
=====
```

CELL#2: NAND2:

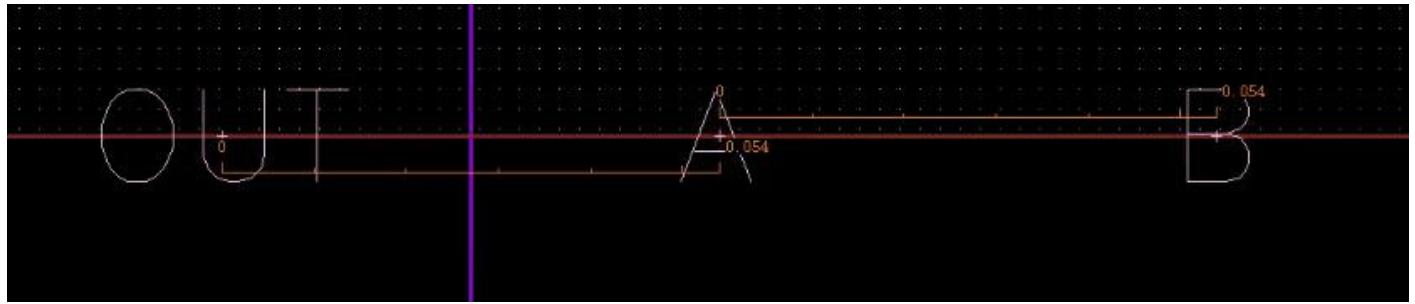
SCHEMATIC:



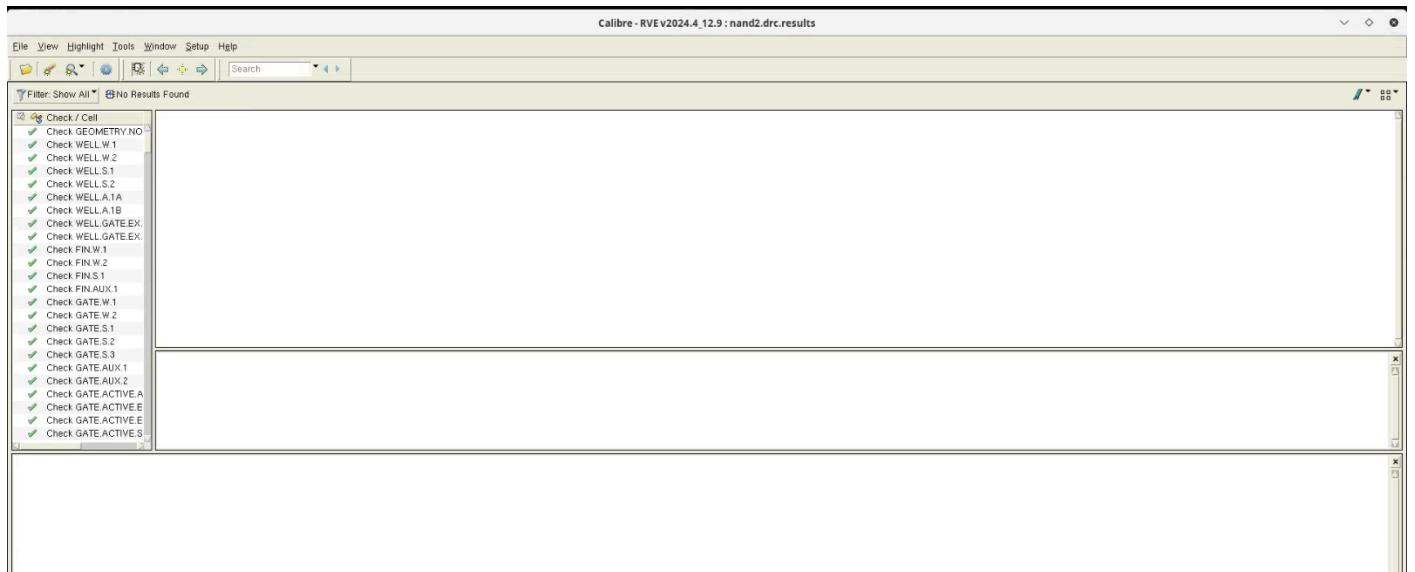
LAYOUT:



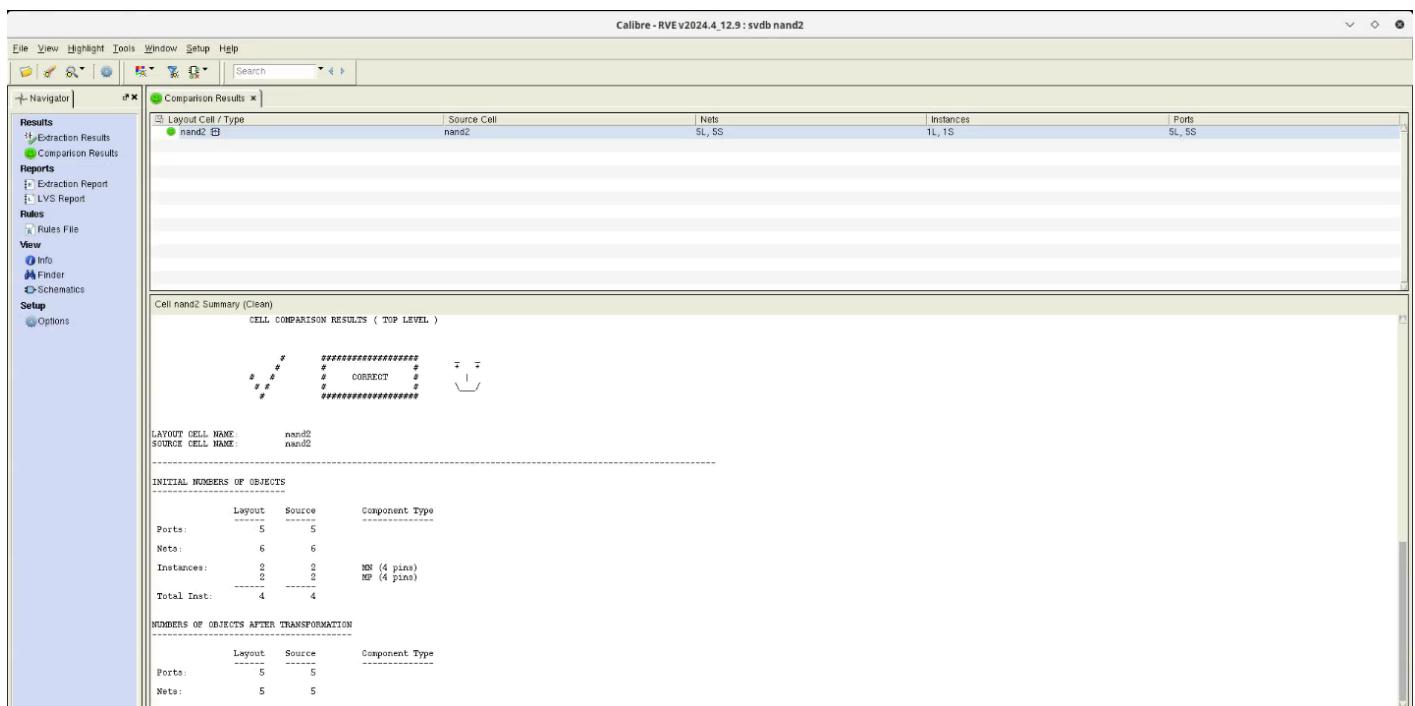
PIN_SPACING:



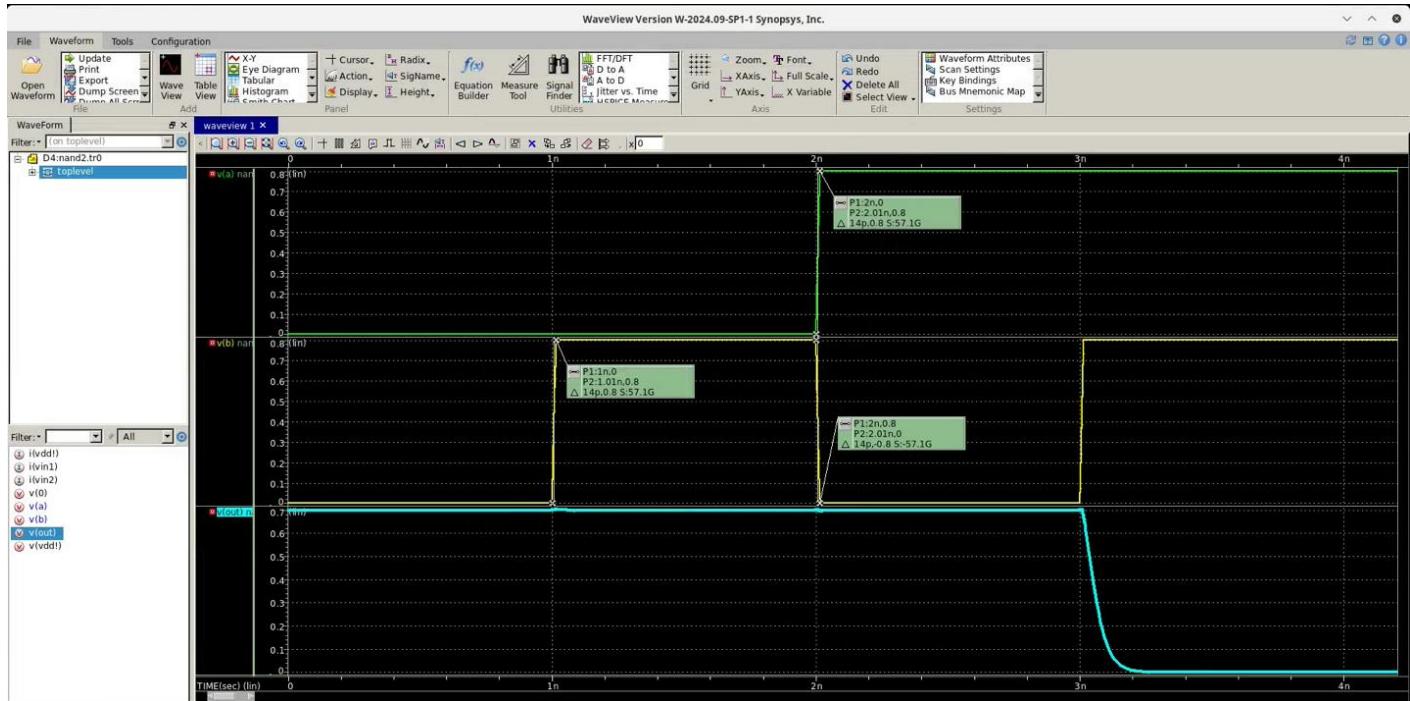
DRC CHECK:



LVS CHECK:



WAVEFORM:



Hspice file:

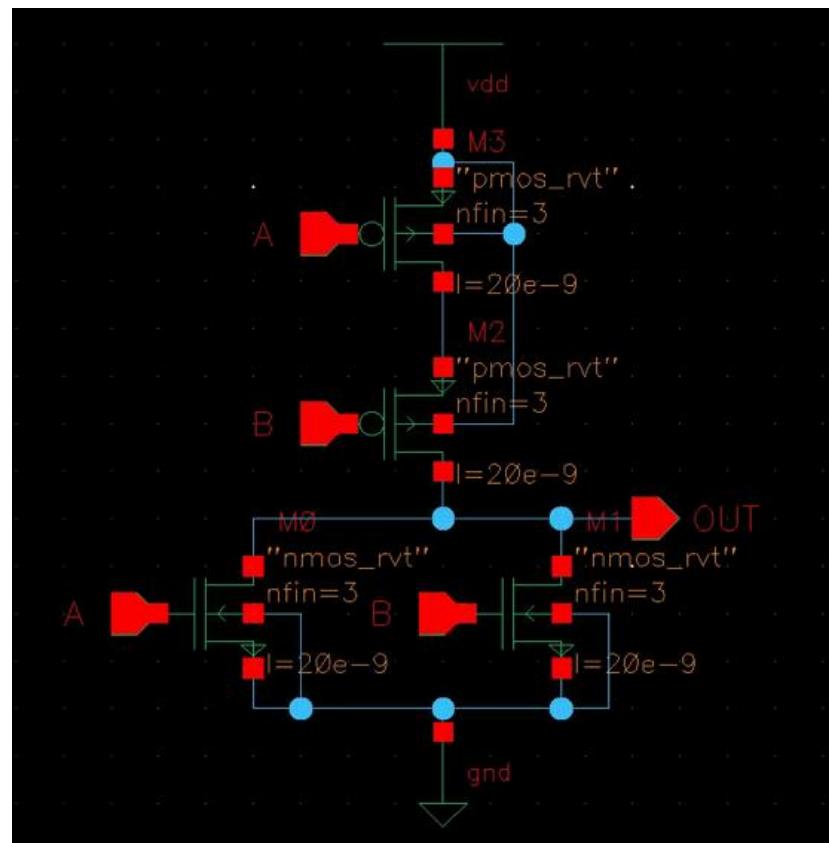
```
.include "~/asap7/7nm_TT.pm"
.include nand2.pex.netlist
.option post runlvl=5
xi A B OUT nand2
VDD! VDD! GND! 0.7v
vin1 A GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v)
vin2 B GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 4200ps
.end
```

LIB FILE :

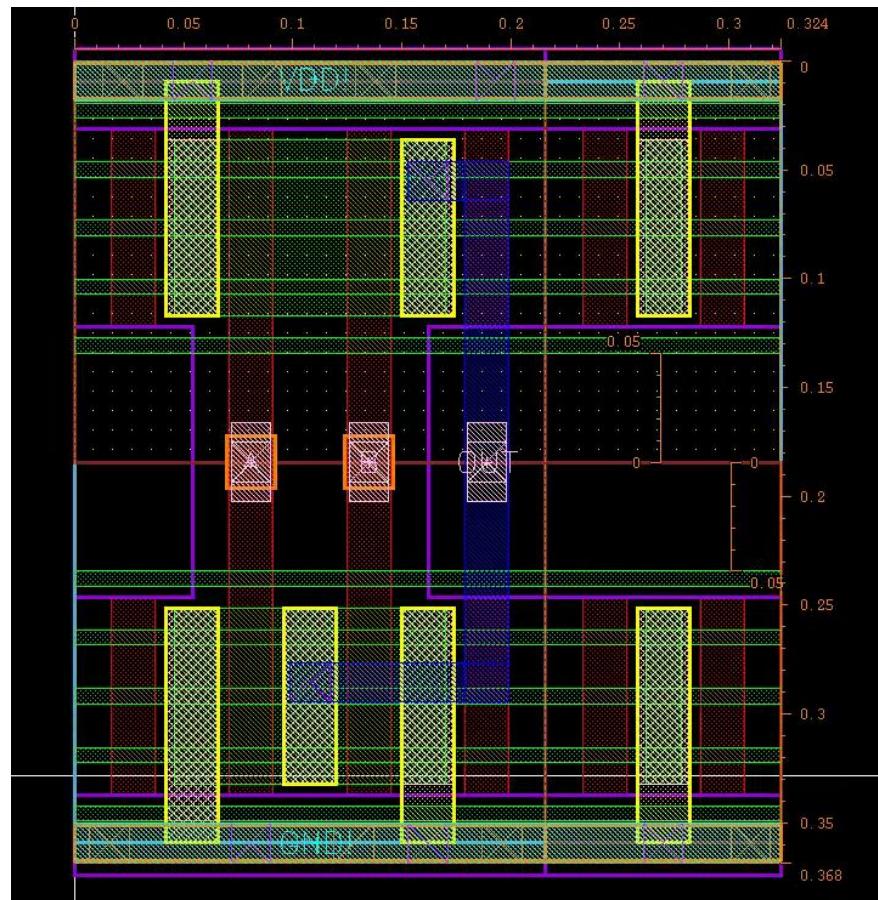
```
Generating power tests.
Generating template at Fri Mar 21 20:40:13 2025
Done generating template at Fri Mar 21 20:40:13 2025
Generate Templates: Maximum virtual memory size: 1081.17 MB
Cell NAND2 configured for characterization.
Fri Mar 21 20:40:13 CDT 2025: Done configure stage (Elapsed: 0 seconds | 0.00 hours Memory: 1081.17MB)
=====
pl_cci> characterize
=====
Fri Mar 21 20:40:35 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 20:40:36 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 20:40:36 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 20:40:36 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 20:40:36 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
NAND2: generated 9 tasks (9 total)
Using 1 standalone slots
[CDPL] Tasks: 0/9, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 9/9, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: NAND2::delay_B_lh_OUT_hl_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Fri Mar 21 20:41:36 2025: Released license FEATURE PrimeLib_CORE(all)
Fri Mar 21 20:41:36 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 20:41:36 CDT 2025: Done characterize stage (Elapsed: 61 seconds | 0.02 hours Memory: 1081.17MB)
=====
0
pl_cci> 
```

CELL#3: NOR2:

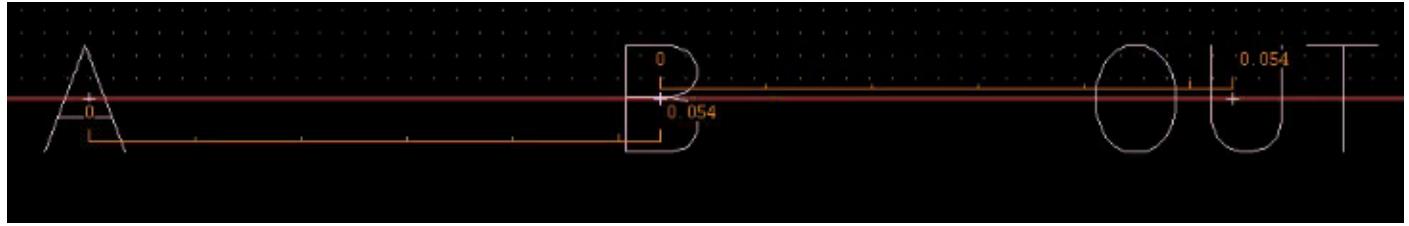
SCHEMATIC:



LAYOUT:



PIN_SPACING:



DRC CHECK:

Calibre - RVE v2024.4.12.9 : nor2.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All | No Results Found

Check / Cell

- ✓ Check GEOMETRY_N0
- ✓ Check WELL_W1
- ✓ Check WELL_W2
- ✓ Check WELL_S1
- ✓ Check WELL_S2
- ✓ Check WELL_A1A
- ✓ Check WELL_A1B
- ✓ Check WELL_GATE_EX
- ✓ Check WELL_GATE_EX.
- ✓ Check FIN_W1
- ✓ Check FIN_W2
- ✓ Check FIN_S1
- ✓ Check FIN_AUX_1
- ✓ Check GATE_W1
- ✓ Check GATE_W2
- ✓ Check GATE_S1
- ✓ Check GATE_S2
- ✓ Check GATE_S3
- ✓ Check GATE_AUX_1
- ✓ Check GATE_AUX_2
- ✓ Check GATE_ACTIVE_A
- ✓ Check GATE_ACTIVE_E
- ✓ Check GATE_ACTIVE_E
- ✓ Check GATE_ACTIVE_S

Rule File Pathname: Calibre_DRC_rules_GEOMETRY_NONORTHONGAL

Non-orthogonal shapes are not allowed

LVS CHECK:

Calibre - RVE v2024.4.12.9 : svdb nor2

File View Highlight Tools Window Setup Help

Navigator | Comparison Results x

Results
Extraction Results
Comparison Results

Reports
Extraction Report
LVS Report

Rules
Rules File

View
Info
Finder
Schematics

Setup
Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
nor2	nor2	SL, SS	1L, 1S	SL, SS

Cell nor2 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: nor2
SOURCE CELL NAME: nor2

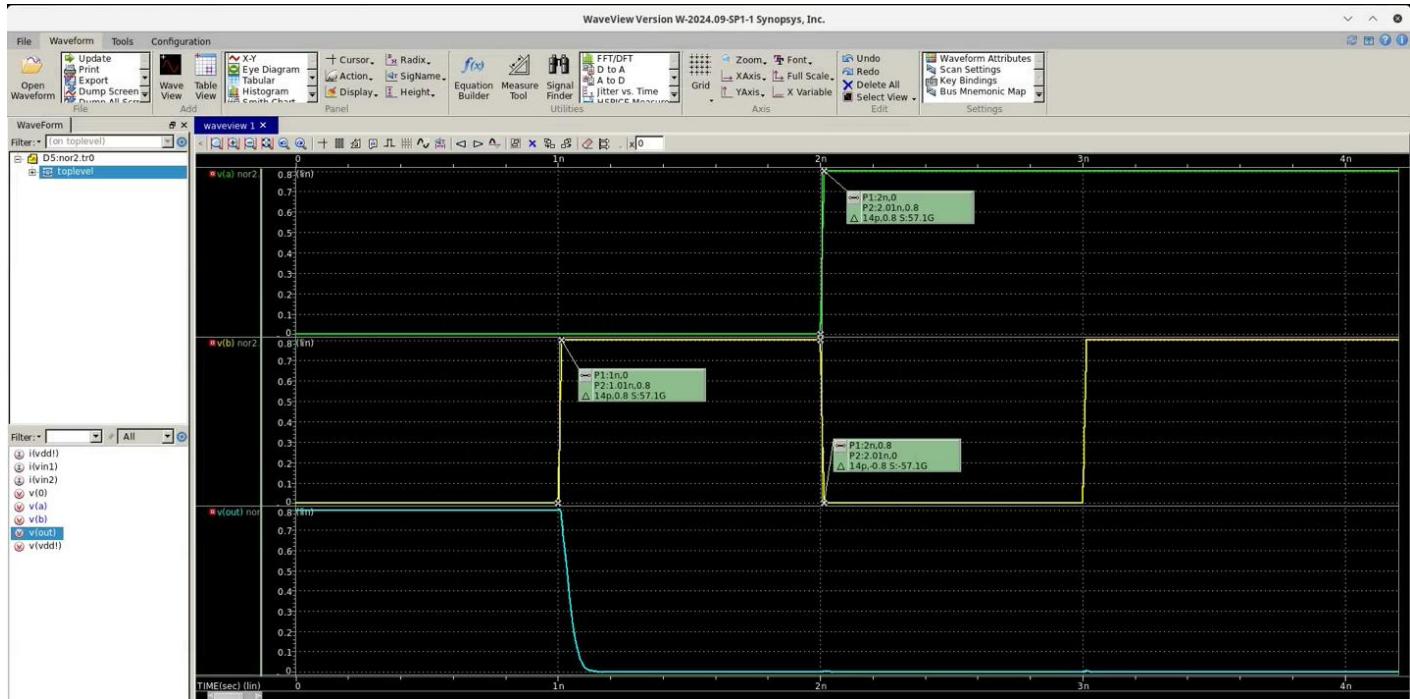
INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	5	5	
Nets:	6	6	
Instances:	2	2	NN (4 pins)
Total Inst:	4	4	NP (4 pins)

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	5	5	
Nets:	5	5	

WAVEFORM:



Hspice file:

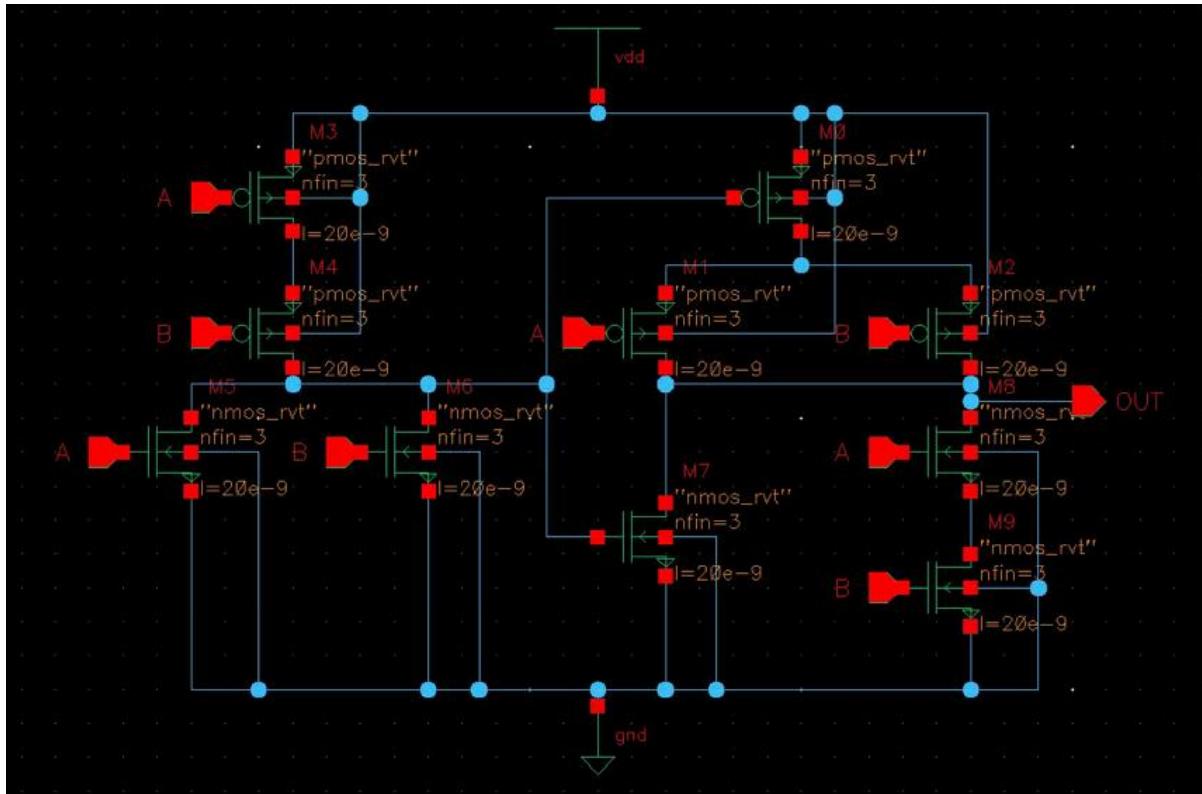
```
.include "~/asap7/7nm_TT.pm"
.include nor2.pex.netlist
.option post runlvl=5
xi A B OUT nor2
VDD! VDD! GND! 0.8v
vin1 A GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v)
vin2 B GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 4200ps
.end
```

LIB FILE :

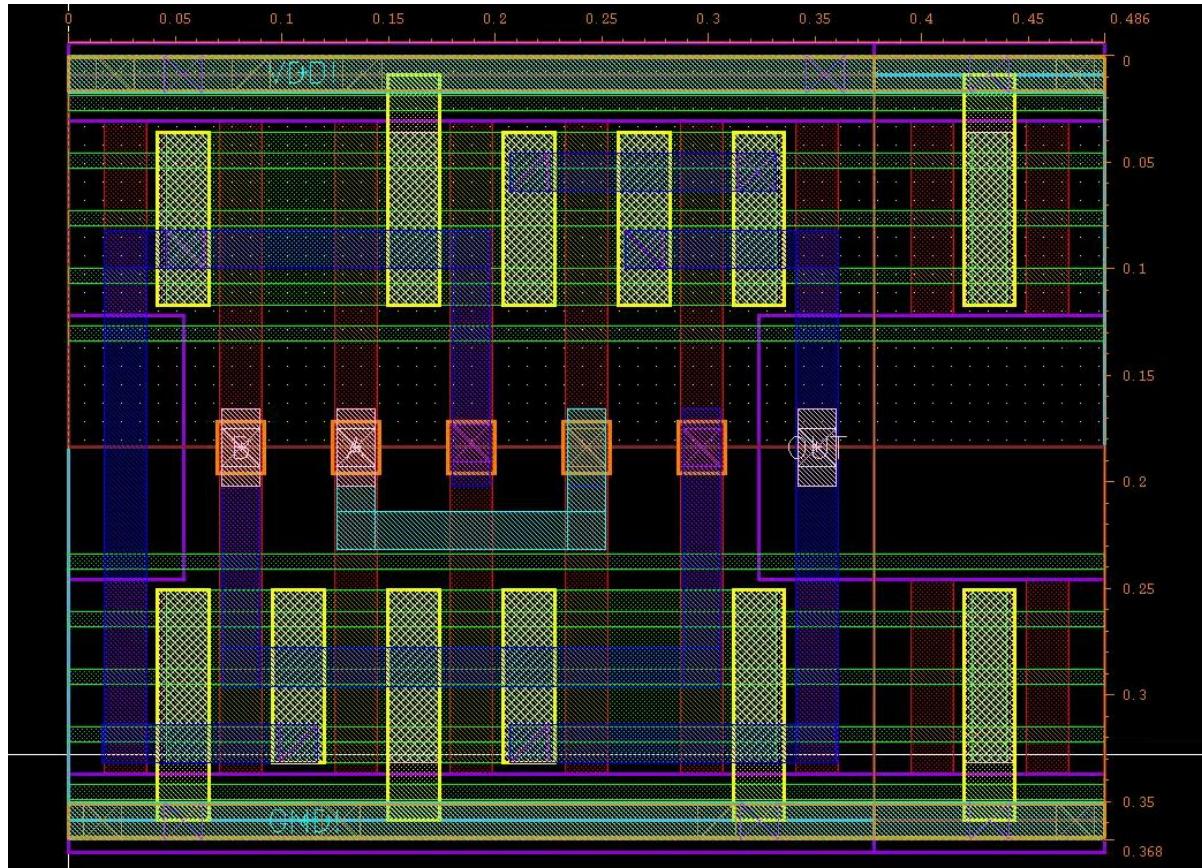
```
Generating power tests.
Generating template at Fri Mar 21 20:47:08 2025
Done generating template at Fri Mar 21 20:47:08 2025
Generate Templates: Maximum virtual memory size: 1081.17 MB
Cell NOR2 configured for characterization.
Fri Mar 21 20:47:08 CDT 2025: Done configure stage (Elapsed: 0 seconds | 0.00 hours Memory: 1081.17MB)
=====
pl_cci> characterize
=====
Fri Mar 21 20:47:12 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 20:47:12 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 20:47:12 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 20:47:12 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 20:47:12 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
NOR2: generated 9 tasks (9 total)
Using 1 standalone slots
[CDPL] Tasks: 0/9, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 9/9, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: NOR2::delay_B_lh_OUT_hl_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Fri Mar 21 20:48:12 2025: Released license FEATURE PrimeLib_CORE(all)
Fri Mar 21 20:48:12 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 20:48:12 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1081.17MB)
=====
```

CELL#4: XOR2:

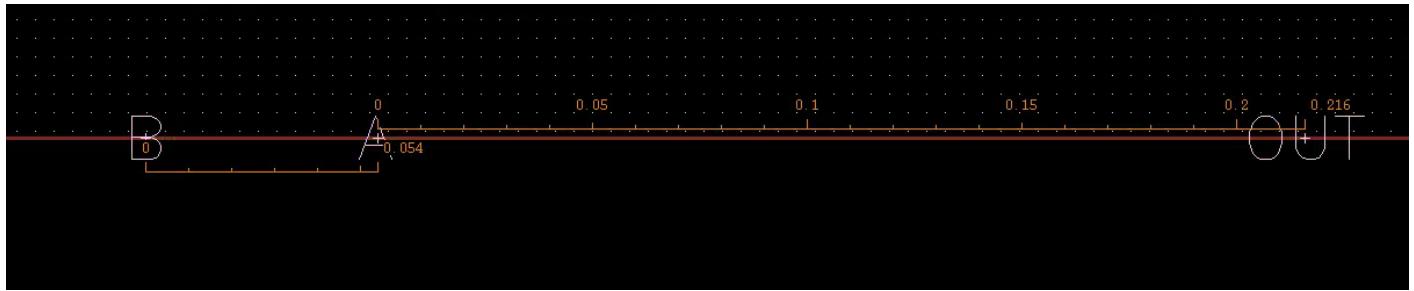
SCHEMATIC:



LAYOUT:



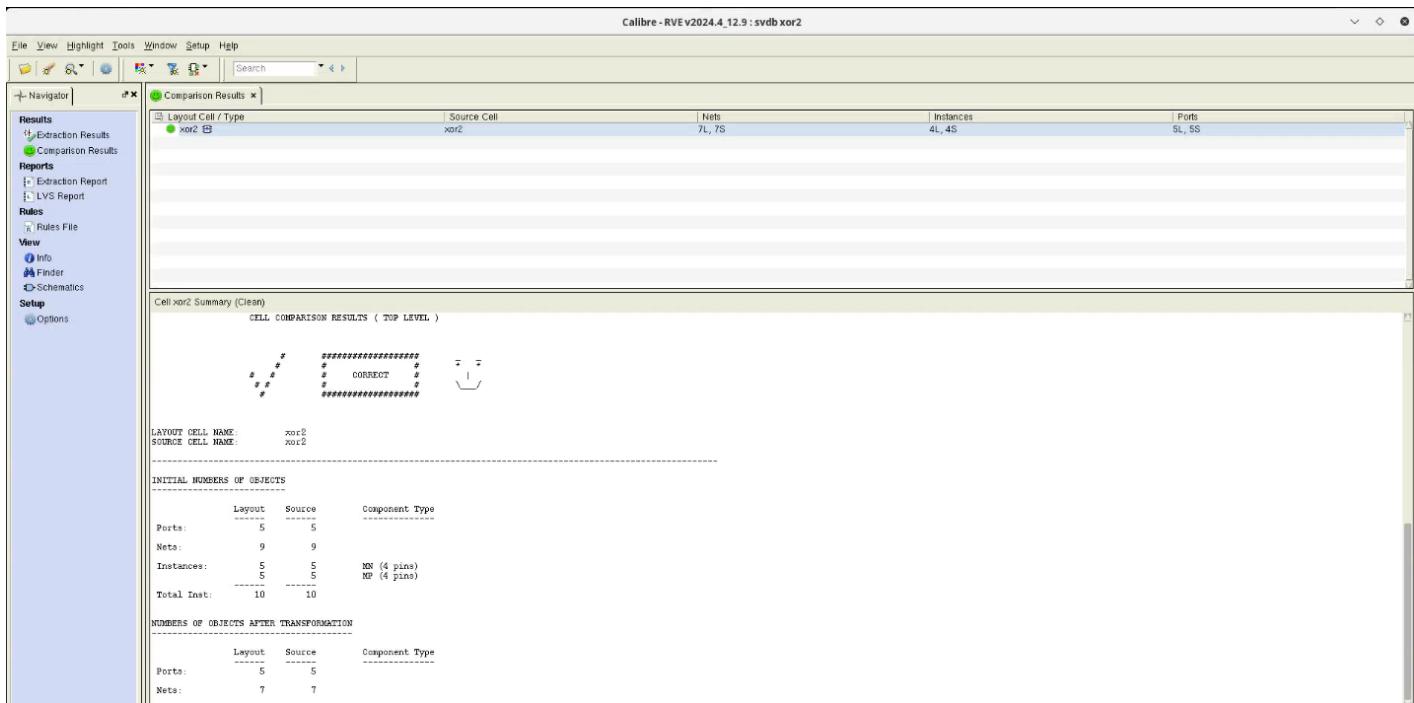
PIN_SPACING:



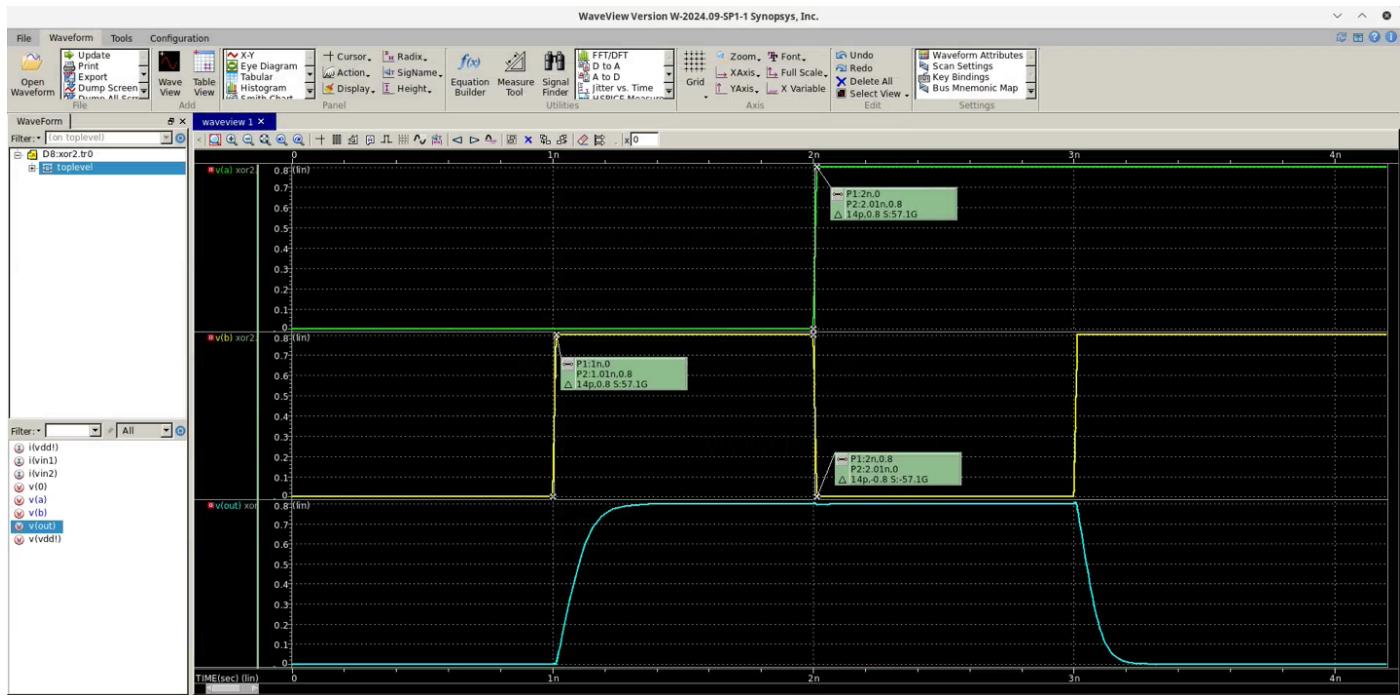
DRC CHECK:



LVS CHECK:



WAVEFORM:



Hspice file:

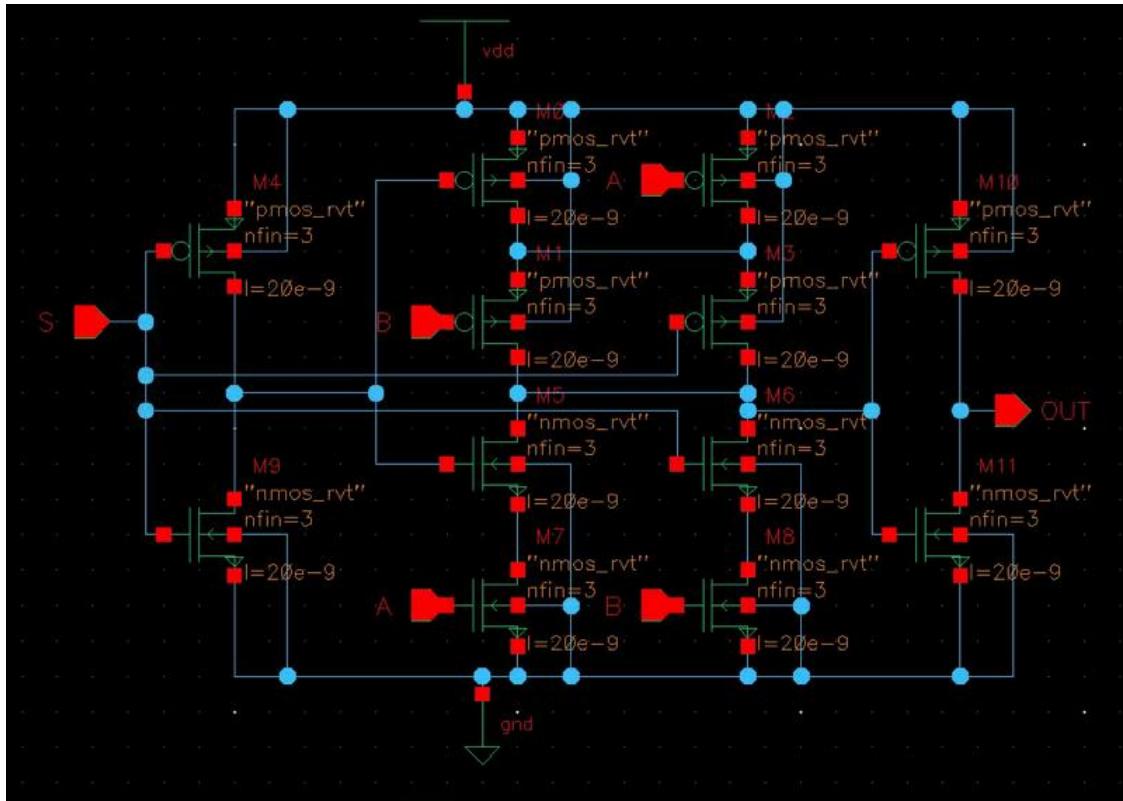
```
.include "~/asap7/7nm_TT.pm"
.include xor2.pex.netlist
.option post runlvl=5
xi A B OUT xor2
VDD! VDD! GND! 0.8v
vin1 A GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v)
vin2 B GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 4200ps
.end
```

LIB FILE :

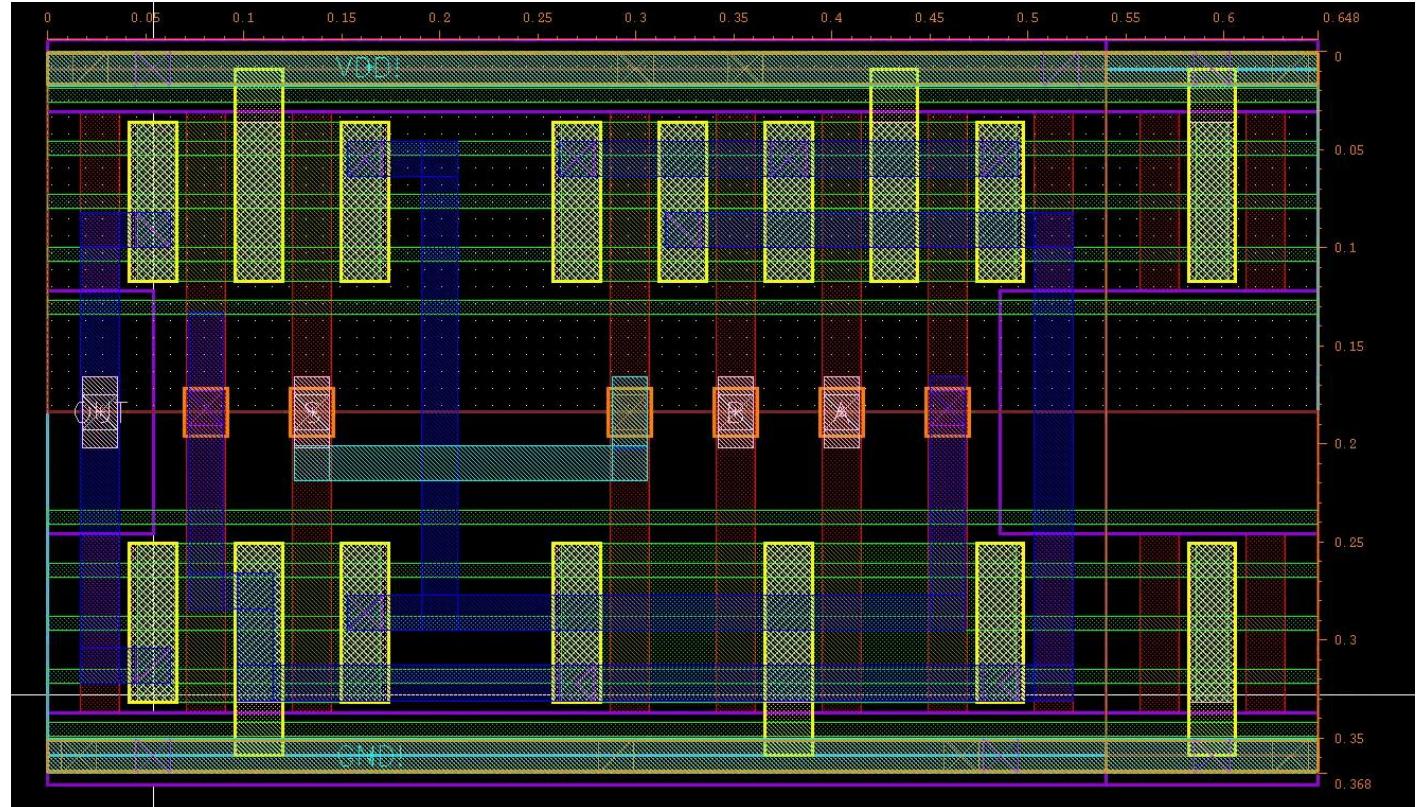
```
pl_cci> characterize
=====
Wed Mar 26 21:21:39 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
Start generating characterization tasks
XOR2: generated 13 tasks (13 total)
Using 1 standalone slots
Wed Mar 26 21:21:39 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Wed Mar 26 21:21:39 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Wed Mar 26 21:21:39 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Wed Mar 26 21:21:39 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
[CDPL] Tasks: 0/13, (0.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m00s
[CDPL] Tasks: 13/13, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: XOR2::leakage_power_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Wed Mar 26 21:22:39 2025: Released license FEATURE PrimeLib_CORE(all)
Wed Mar 26 21:22:39 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Wed Mar 26 21:22:39 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1084.81MB)
```

CELL#5: MUX2:1:

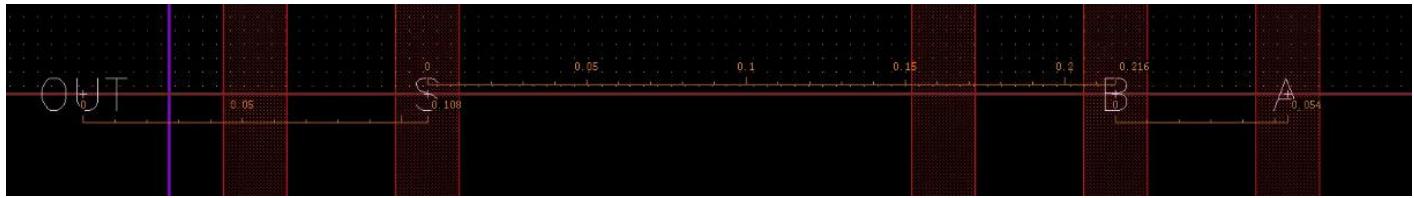
SCHEMATIC:



LAYOUT:



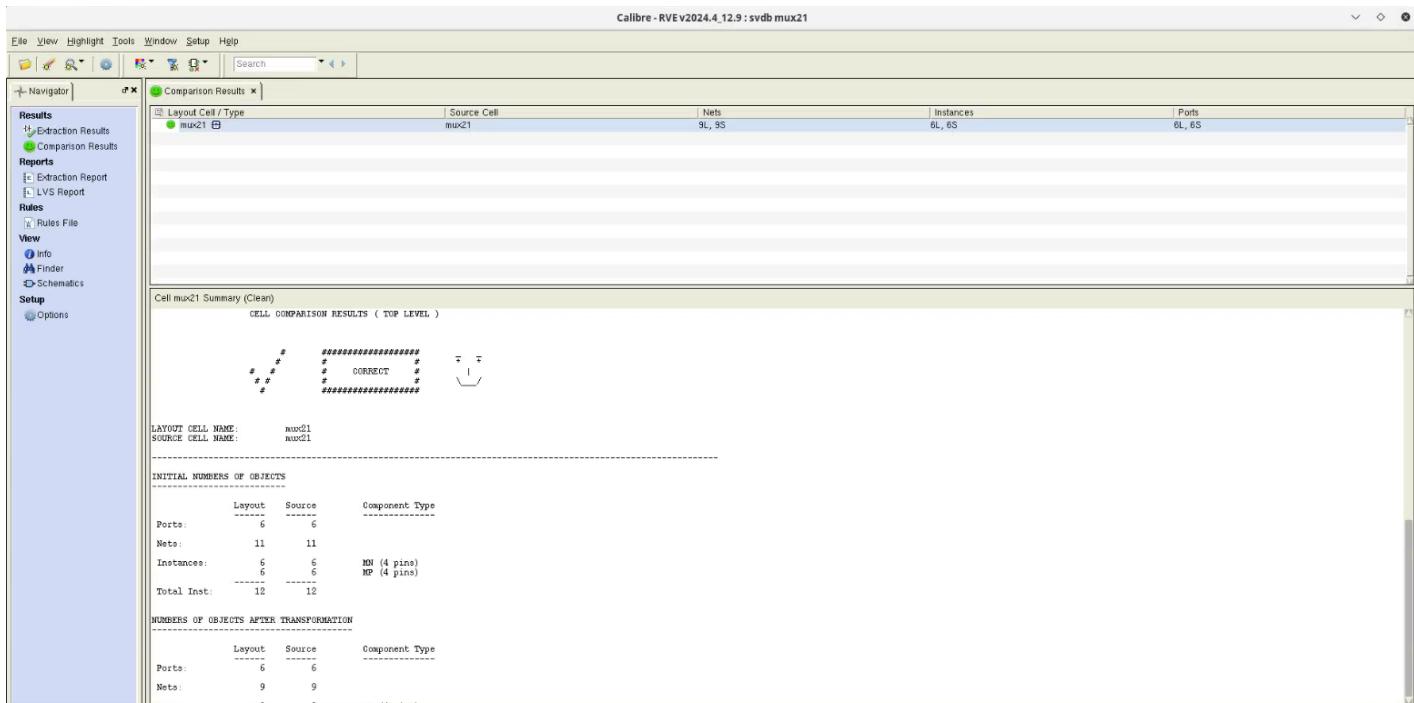
PIN_SPACING:



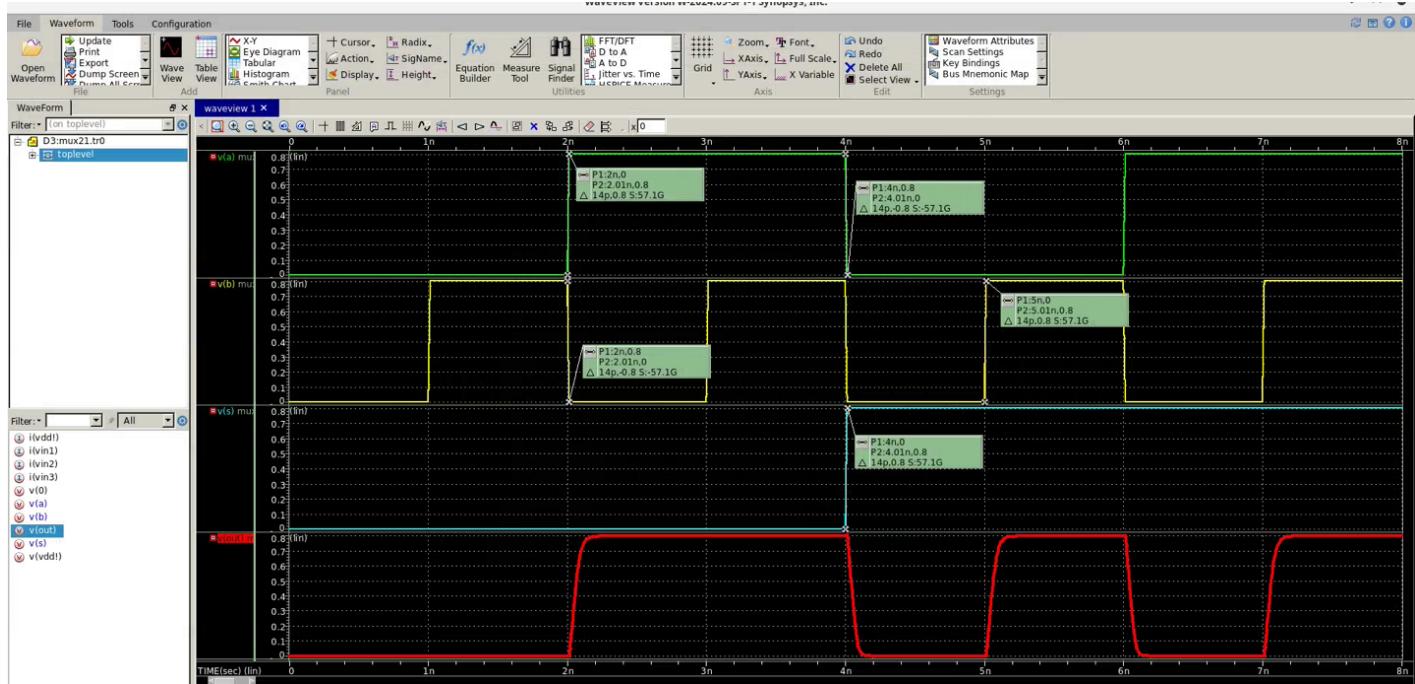
DRC CHECK:



LVS CHECK:



WAVEFORM:



Hspice file:

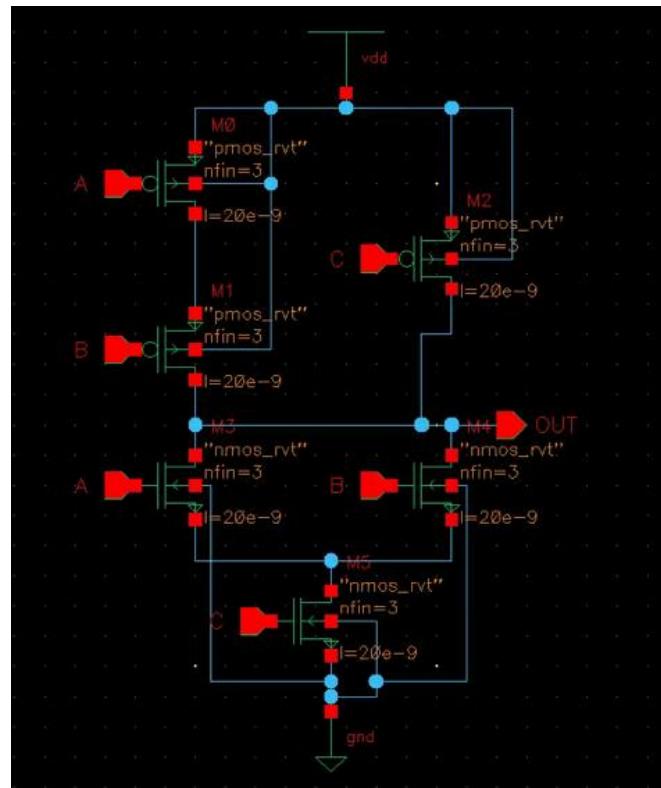
```
.include "~/asap7/7nm_TT.pm"
.include mux21.pex.netlist
.option post runlvl=5
xi A B OUT S mux21
VDD! VDD! GND! 0.8v
vin1 S GND! pwl(0ps 0v 4000ps 0v 4014ps 0.8v)
vin2 A GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v 4000ps 0.8v 4014ps 0v 6000ps 0v 6014ps 0.8v)
vin3 B GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v 4000ps 0.8v
4014ps 0v 5000ps 0v 5014ps 0.8v 6000ps 0.8v 6014ps 0v 7000ps 0v 7014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 8000ps
.end
```

LIB FILE :

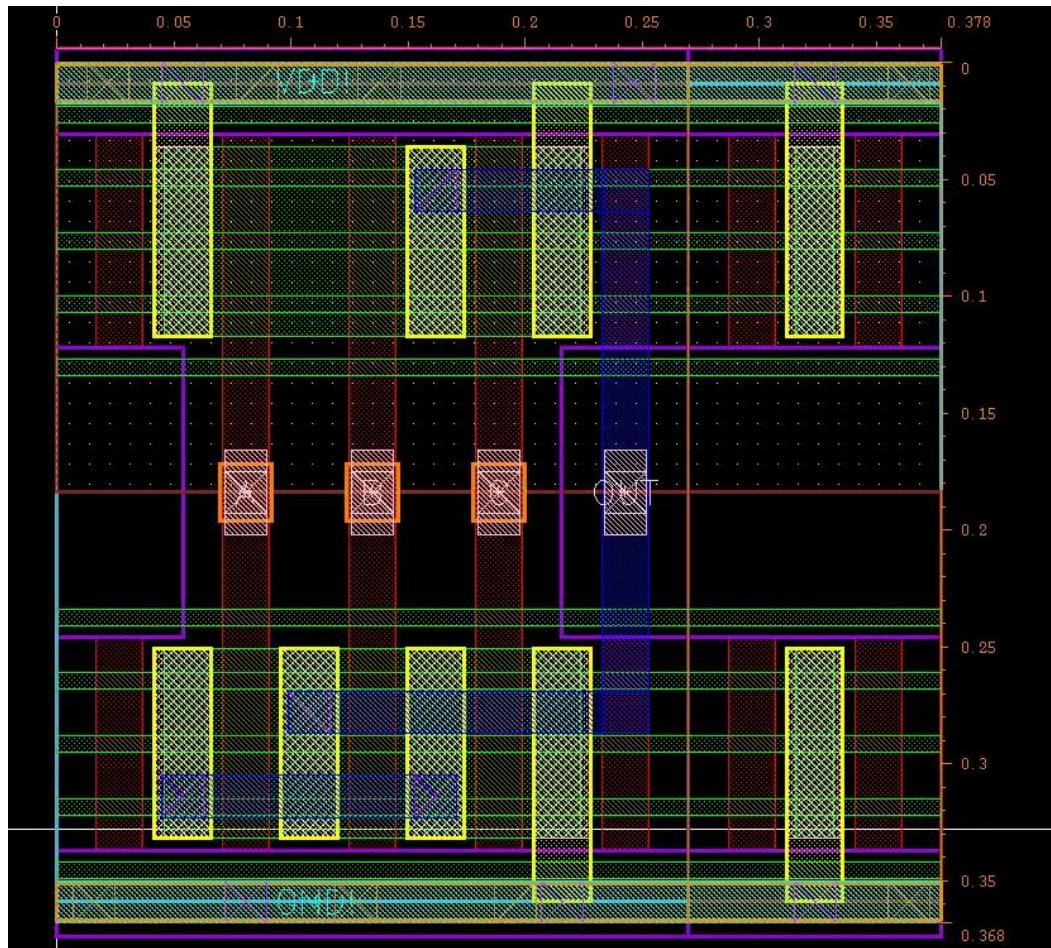
```
pl_cci> characterize
=====
Wed Mar 26 21:18:43 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Wed Mar 26 21:18:43 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Wed Mar 26 21:18:43 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Wed Mar 26 21:18:43 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Wed Mar 26 21:18:43 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Library has standard-cells
MUX21: generated 13 tasks (13 total)
Using 1 standalone slots
[CDPL] Tasks: 0/13, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 13/13, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: MUX21::leakage_power_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Wed Mar 26 21:19:43 2025: Released license FEATURE PrimeLib_CORE(all)
Wed Mar 26 21:19:43 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Wed Mar 26 21:19:43 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1081.11MB)
=====
0
pl_cci> model
```

CELL#6: OAI21:

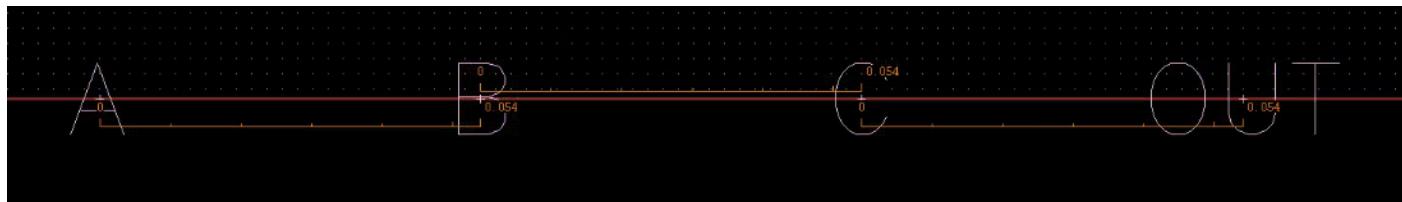
SCHEMATIC:



LAYOUT:



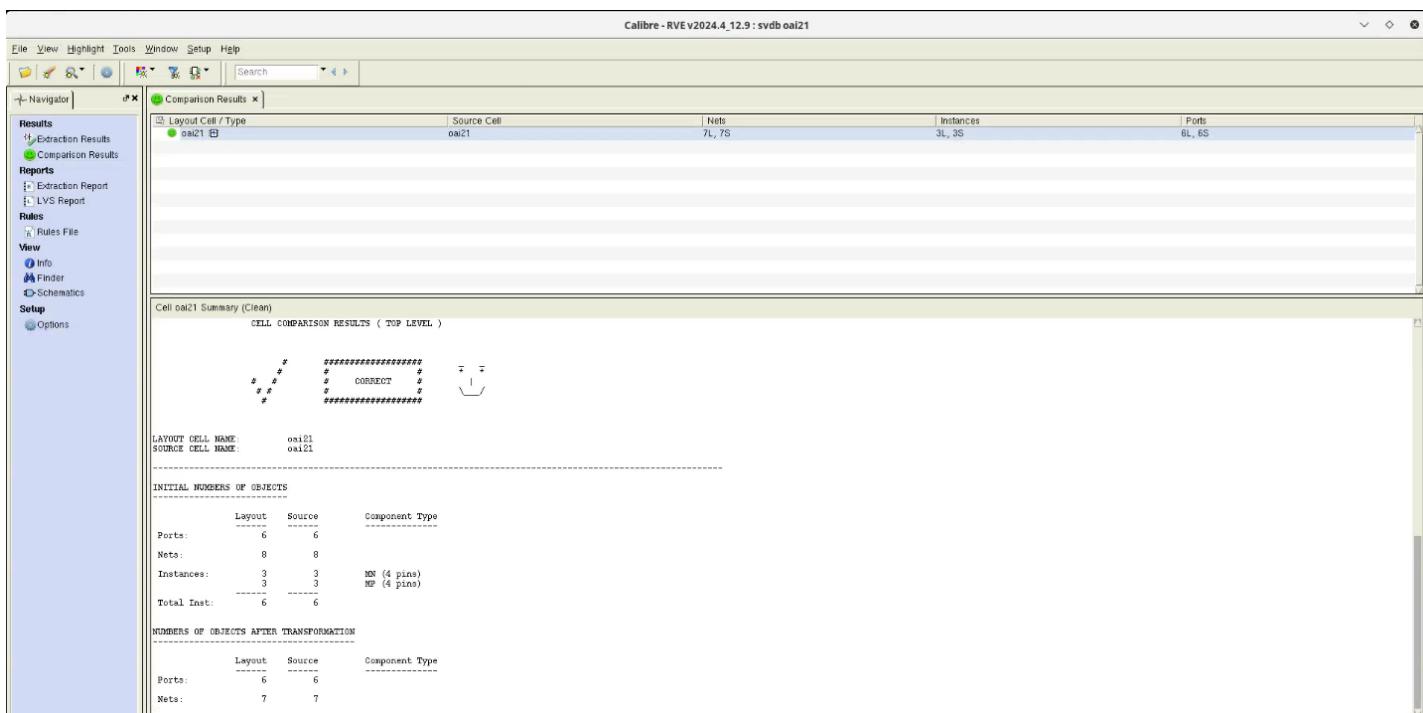
PIN_SPACING:



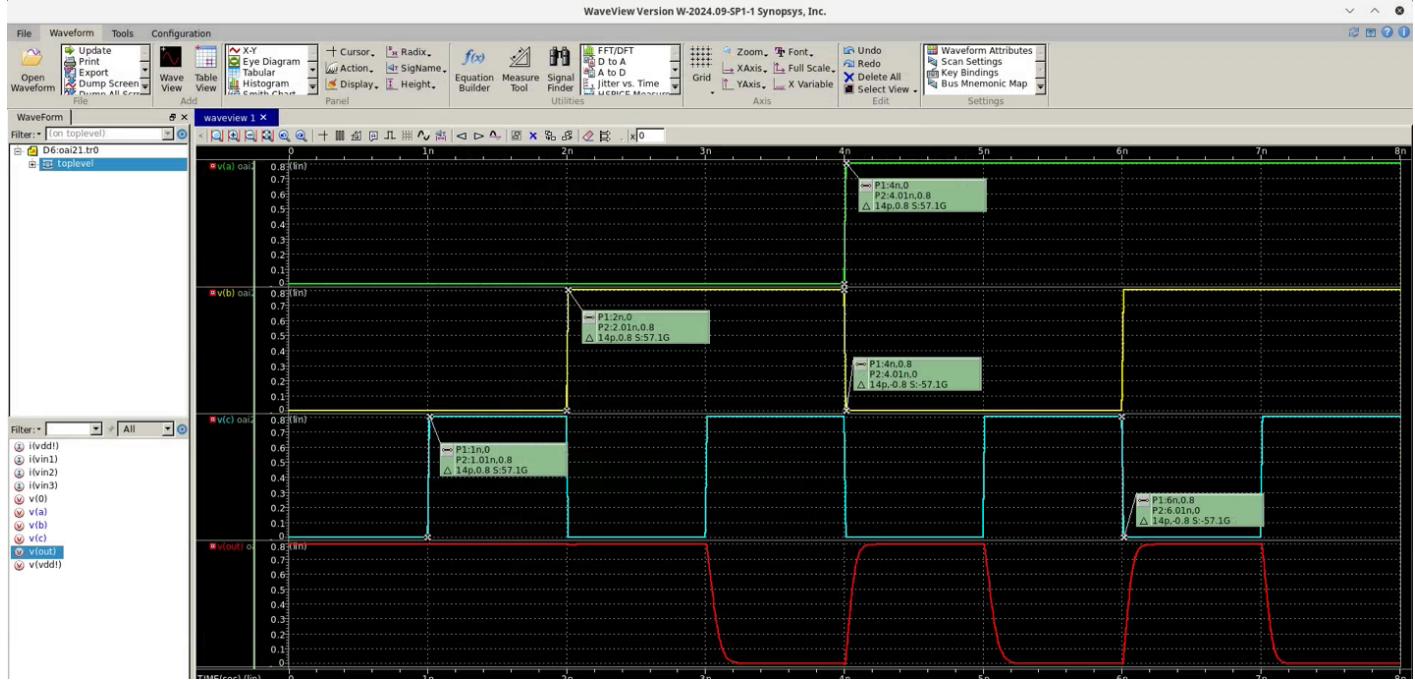
DRC CHECK:



LVS CHECK:



WAVEFORM:



Hspice file:

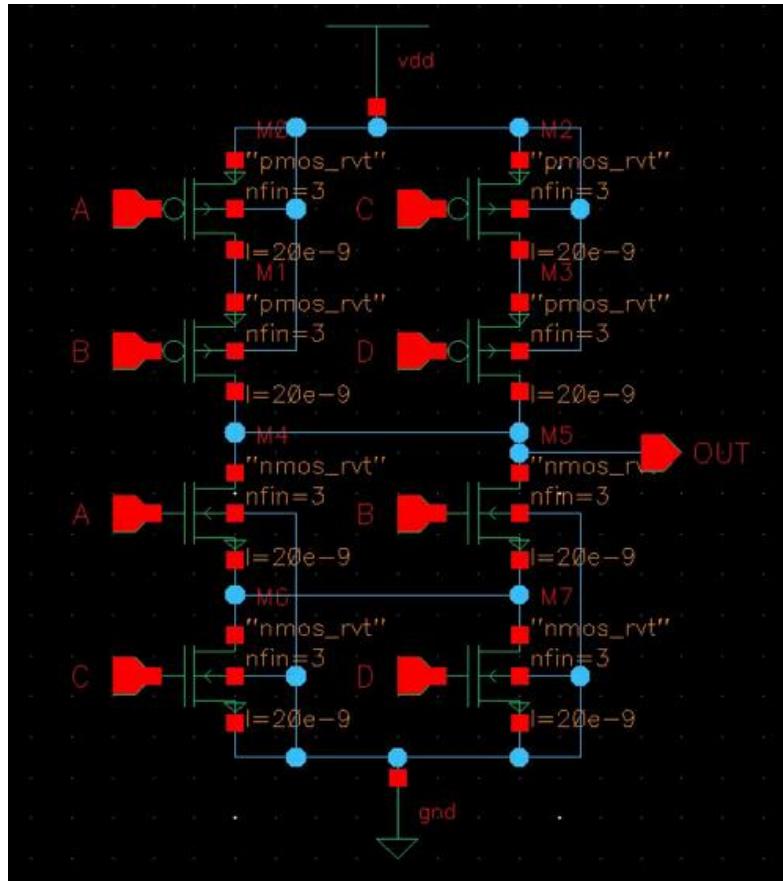
```
.include "~/asap7/7nm_TT.pm"
.include oai21.pex.netlist
.option post runlvl=5
xi A B C OUT oai21
VDD! VDD! GND! 0.8v
vin1 A GND! pwl(0ps 0v 4000ps 0v 4014ps 0.8v)
vin2 B GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v 4000ps 0.8v 4014ps 0v 6000ps 0v 6014ps 0.8v)
vin3 C GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v 4000ps 0.8v
4014ps 0v 5000ps 0v 5014ps 0.8v 6000ps 0.8v 6014ps 0v 7000ps 0v 7014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 8000ps
.end
```

LIB FILE :

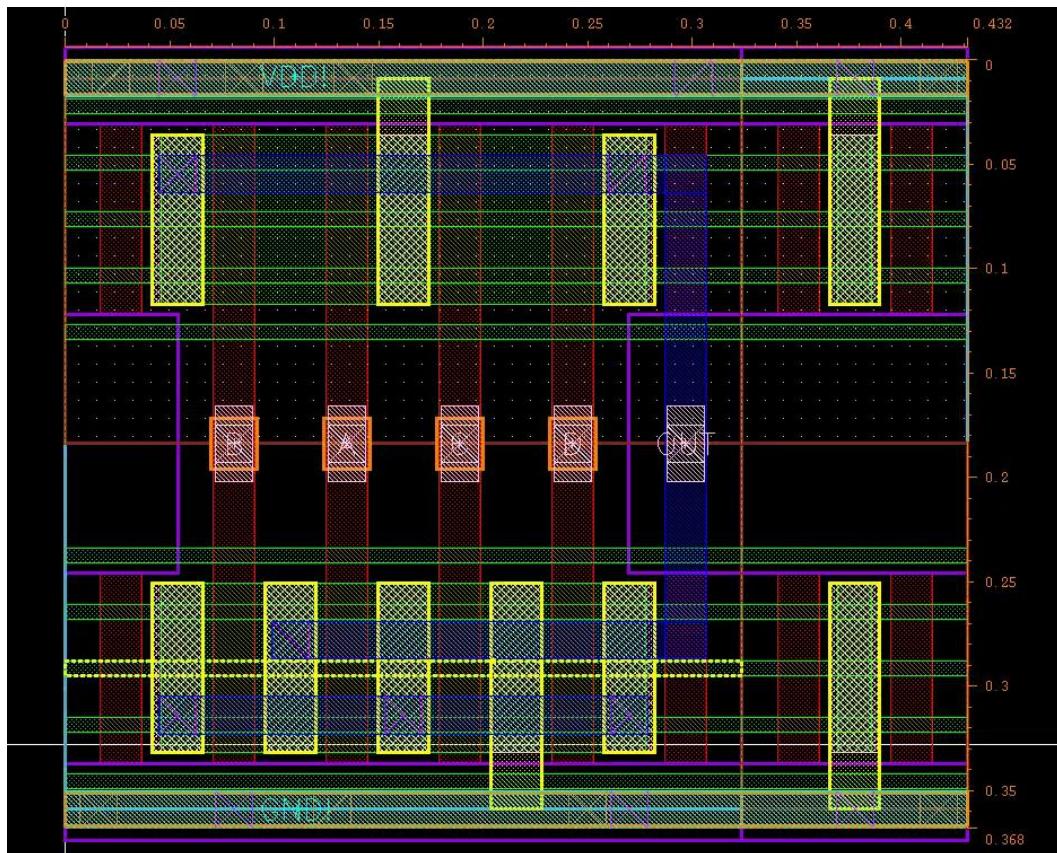
```
Generating power tests.
Generating template at Fri Mar 21 22:54:36 2025
Done generating template at Fri Mar 21 22:54:36 2025
Generate Templates: Maximum virtual memory size: 1111.68 MB
Cell OAI21 configured for characterization.
Fri Mar 21 22:54:36 CDT 2025: Done configure stage (Elapsed: 0 seconds | 0.00 hours Memory: 1111.68MB)
=====
pl_cci> characterize
=====
Fri Mar 21 22:54:41 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 22:54:41 2025: Checked out license FEATURE PrimeLib CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 22:54:41 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 22:54:41 2025: Checked out license FEATURE PrimeLib SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 22:54:41 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
OAI21: generated 11 tasks (11 total)
Using 1 standalone slots
[CDPL] Tasks: 0/11, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 11/11, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: OAI21::delay_B_lh_OUT_hl_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Fri Mar 21 22:55:41 2025: Released license FEATURE PrimeLib_CORE(all)
Fri Mar 21 22:55:41 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 22:55:41 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1111.68MB)
```

CELL#7: OAI22:

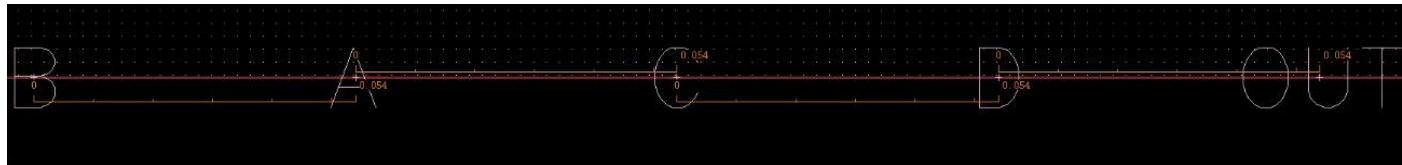
SCHEMATIC:



LAYOUT:



PIN_SPACING:



DRC CHECK:

Calibre - RVEv2024.4_12.9 : oai22.drc.results

File View Highlight Tools Window Setup Help

Filter Show All No Results Found

Check FIN.W.1
Check FIN.W.2
Check FIN.S.1
Check FIN.AUX.1
Check GATE.W.1
Check GATE.W.2
Check GATE.S.1
Check GATE.S.2
Check GATE.S.3
Check GATE.AUX.1
Check GATE.AUX.2
Check GATE.ACTIVE.A
Check GATE.ACTIVE.E
Check GATE.ACTIVE.S

Rule File Pathname: Calibre_DRC_rules.
GEOMETRY NONORTHOGONAL
Non-orthogonal shapes are not allowed

Calibre Run Completed Successfully -- Results are Valid

LVS CHECK:

Calibre - RVEv2024.4_12.9 : svdb oai22

File View Highlight Tools Window Setup Help

Navigator Comparison Results

Results Extraction Results Comparison Results Reports Extraction Report LVS Report Rules Rules File View Info Finder Schematics Setup Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
oai22	oai22	8L, 8S	4L, 4S	7L, 7S

Cell oai22 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

***** CONFLICT *****

LAYOUT CELL NAME: oai22
SOURCE CELL NAME: oai22

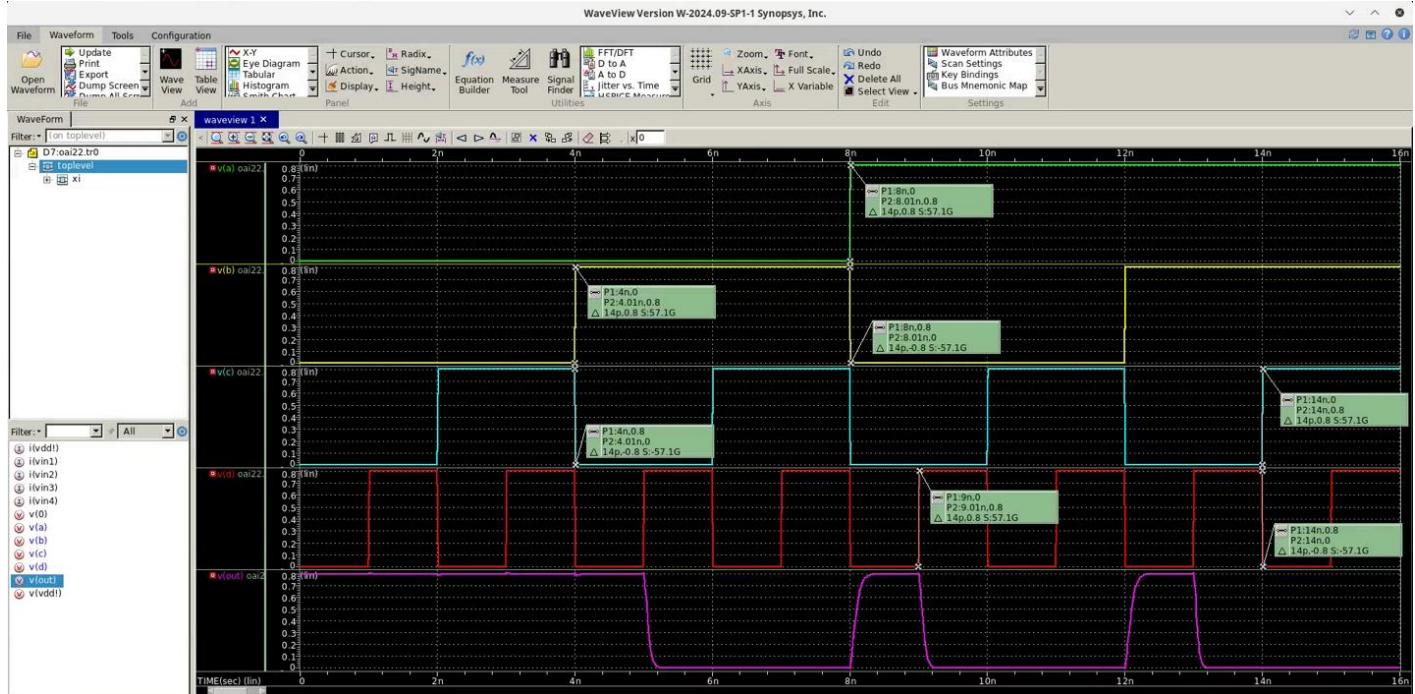
INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	7	7	
Nets:	10	10	
Instances:	4	4	NN (4 pins)
Total Inst:	8	8	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	7	7	
Nets:	8	8	

WAVEFORM:



Hspice file:

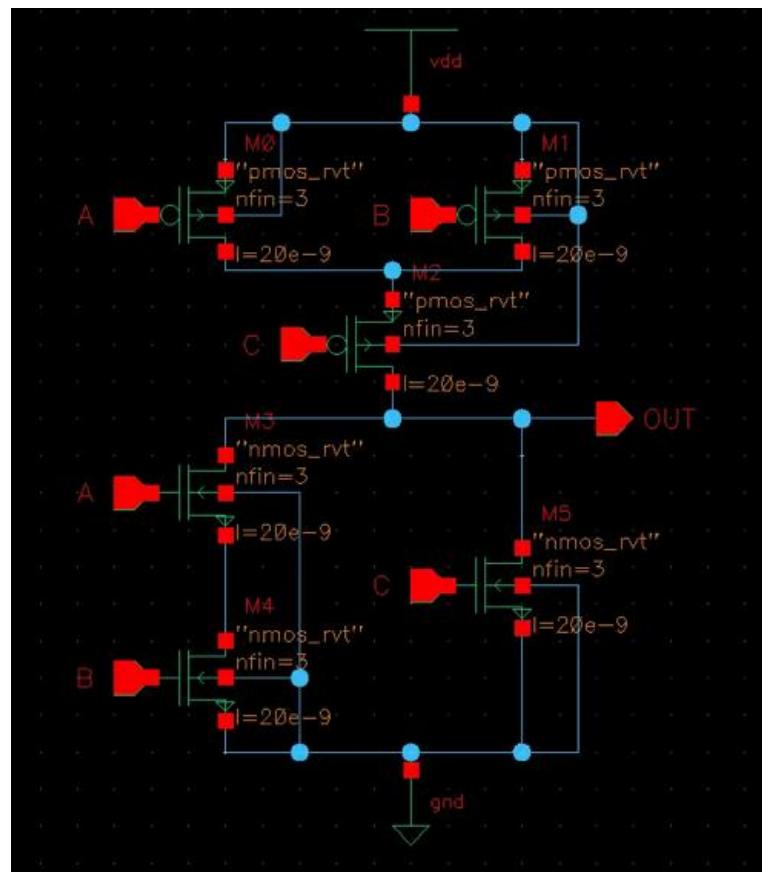
```
.include "~/asap7/7nm_TT.pm"
.include oai22.pex.netlist
.option post runlvl=5
xi A B C D OUT oai22
VDD! VDD! GND! 0.8v
vin1 A GND! pwl(0ps 0v 8000ps 0v 8014ps 0.8v)
vin2 B GND! pwl(0ps 0v 4000ps 0v 4014ps 0.8v 8000ps 0.8v 8014ps 0v 12000ps 0v 12014ps 0.8v)
vin3 C GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v 4000ps 0.8v 4014ps 0v 6000ps 0v 6014ps 0.8v 8000ps
0.8v 8014ps 0v 10000ps 0v 10014ps 0.8v 12000ps 0.8v 12014ps 0v 14000ps 0v 14014ps 0.8v )
vin4 D GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v 4000ps
0.8v 4014ps 0v 5000ps 0v 5014ps 0.8v 6000ps 0.8v 6014ps 0v 7000ps 0v 7014ps 0.8v 8000ps 0.8v
8014ps 0v 9000ps 0v 9014ps 0.8v 10000ps 0.8v 10014ps 0v 11000ps 0v 11014ps 0.8v 12000ps 0.8v
12014ps 0v 13000ps 0v 13014ps 0.8v 14000ps 0.8v 14014ps 0v 15000ps 0v 15014ps 0.8v)
cout OUT GND! 10fF
.tr 1ps 16000ps
.end
```

LIB FILE :

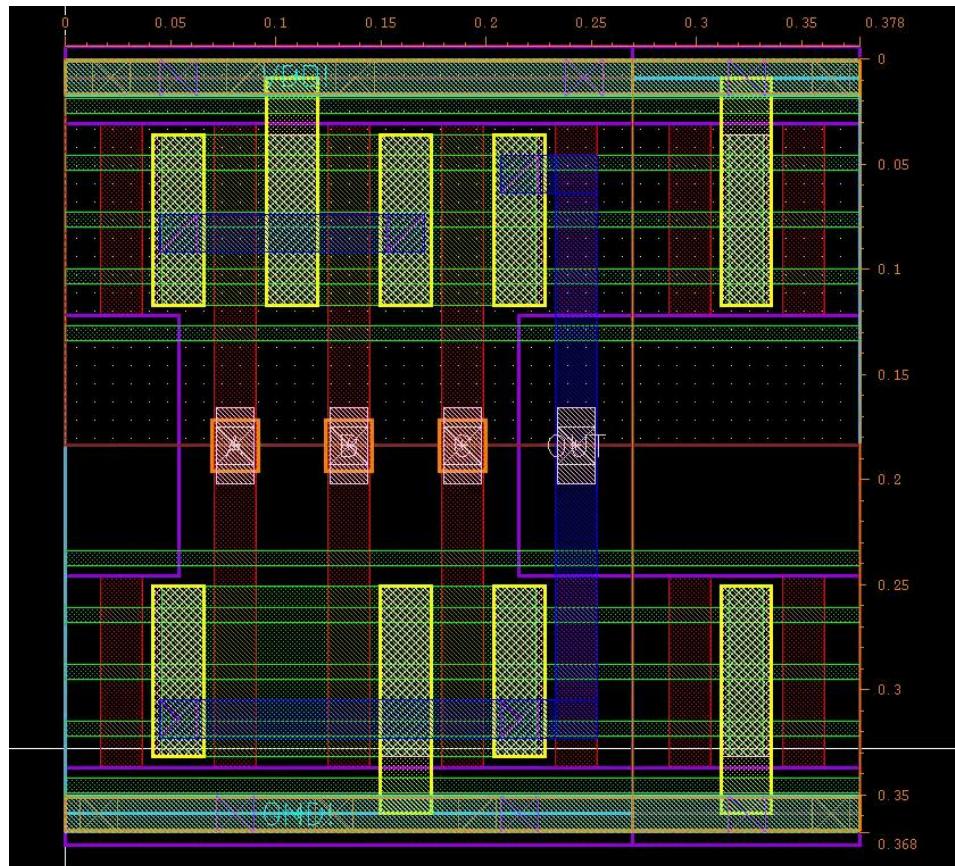
```
Generating power tests.
Generating template at Fri Mar 21 21:20:10 2025
Done generating template at Fri Mar 21 21:20:11 2025
Generate Templates: Maximum virtual memory size: 1109.9 MB
Cell OAII22 configured for characterization.
Fri Mar 21 21:20:11 CDT 2025: Done configure stage (Elapsed: 1 seconds | 0.00 hours Memory: 1109.90MB)
=====
pl_cci> characterize
=====
Fri Mar 21 21:20:18 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 21:20:18 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 21:20:18 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 21:20:18 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 21:20:18 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
OAII22: generated 13 tasks (13 total)
Using 1 standalone slots
[CDPL] Tasks: 0/13, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 13/13, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: OAII22::leakage_power_ACQ_1 30.00 seconds
[CDPL] Summary:
    All tasks finished successfully.
Fri Mar 21 21:21:18 2025: Released license FEATURE PrimeLib_CORE(all)
Fri Mar 21 21:21:18 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 21:21:18 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1111.37MB)
```

CELL#8: AIO21:

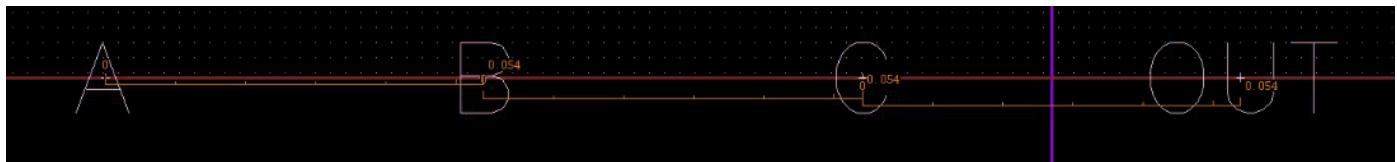
SCHEMATIC:



LAYOUT:



PIN_SPACING:



DRC CHECK:

Calibre - RVE v2024.4 12.9 : aoi21.drc.results

File View Highlight Tools Window Setup Help

Filter: Show All | No Results Found

Check / Cell

- ✓ Check GEOMETRY.NO.
- ✓ Check WELL.W.1
- ✓ Check WELL.W.2
- ✓ Check WELL.W.3
- ✓ Check WELL.S.1
- ✓ Check WELL.A.1A
- ✓ Check WELL.A.1B
- ✓ Check WELL.GATE.EX
- ✓ Check WELL.GATE.E
- ✓ Check FIN.W.1
- ✓ Check FIN.W.2
- ✓ Check FIN.S.1
- ✓ Check FIN.AUX.1
- ✓ Check GATE.W.1
- ✓ Check GATE.W.2
- ✓ Check GATE.S.1
- ✓ Check GATE.S.2
- ✓ Check GATE.S.3
- ✓ Check GATE.A.1A
- ✓ Check GATE.A.1Z
- ✓ Check GATE.ACTIVE.A
- ✓ Check GATE.ACTIVE.E
- ✓ Check GATE.ACTIVE.E
- ✓ Check GATE.ACTIVE.S
- ✓ Check ACTIVE.FINE.X
- ✓ Check ACTIVE.W.1
- ✓ Check ACTIVE.W.2
- ✓ Check ACTIVE.W.3
- ✓ Check ACTIVE.S.1
- ✓ Check ACTIVE.S.2A
- ✓ Check ACTIVE.S.2B
- ✓ Check ACTIVE.WELLS
- ✓ Check SRAM.ACTIVE.V
- ✓ Check ACTIVE.WELL.E
- ✓ Check SRAM.ACTIVE.V
- ✓ Check ACTIVE.A.1A
- ✓ Check ACTIVE.A.1B
- ✓ Check SRAM.ACTIVE.A

Rule File Pathname: Calibre_DRC_rules_.
GEOMETRY.NONORTHORIGONAL
Non-orthogonal shapes are not allowed

Calibre Run Completed Successfully -- Results are Valid

LVS CHECK:

Calibre - RVE v2024.4_12.9 : svdb aoi21

File View Highlight Tools Window Setup Help

Navigator Comparison Results

Results Extraction Results Comparison Results

Reports Extraction Report LVS Report

Rules Rules File

View Info Finder Schematics

Setup Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
aoi21	aoi21	7L, 7S	4L, 4S	6L, 6S

Cell aoi21 Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

```

    #####
    #   #
    # CORRECT #
    #   #
    #####
  
```

LAYOUT CELL NAME: aoi21
SOURCE CELL NAME: aoi21

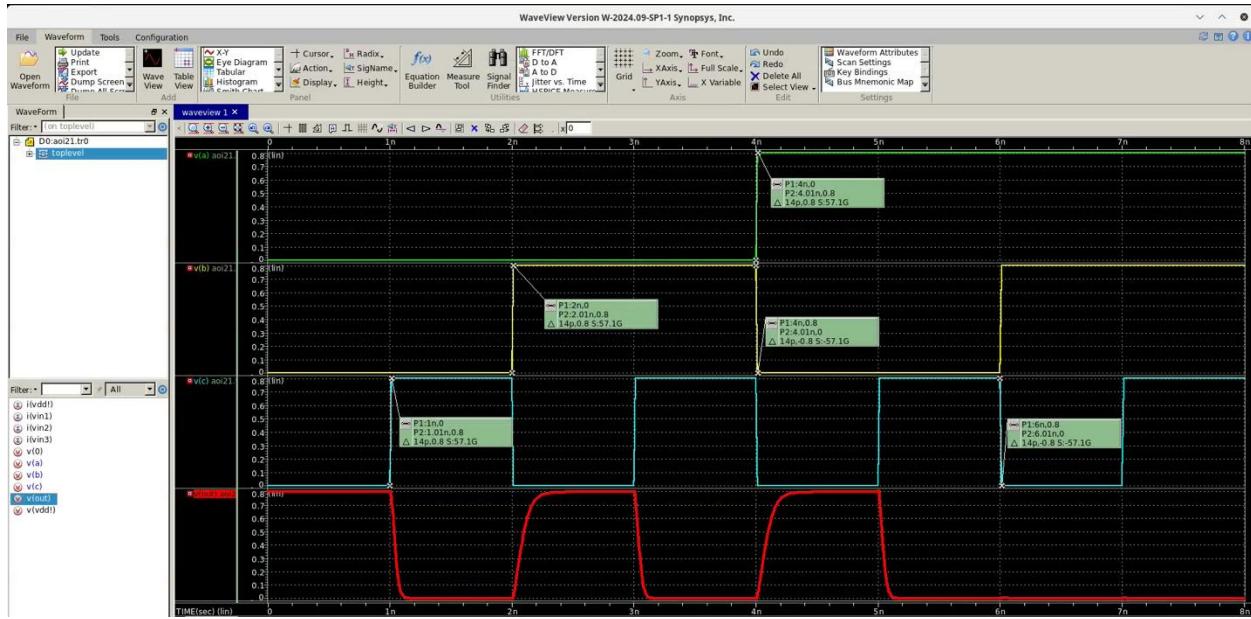
INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	6	6	
Nets:	8	8	
Instances:	3	3	NN (4 pins)
	3	3	NP (4 pins)
Total Inst:	6	6	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	6	6	
Nets:	7	7	
	7	7	

WAVEFORM:



Hspice file:

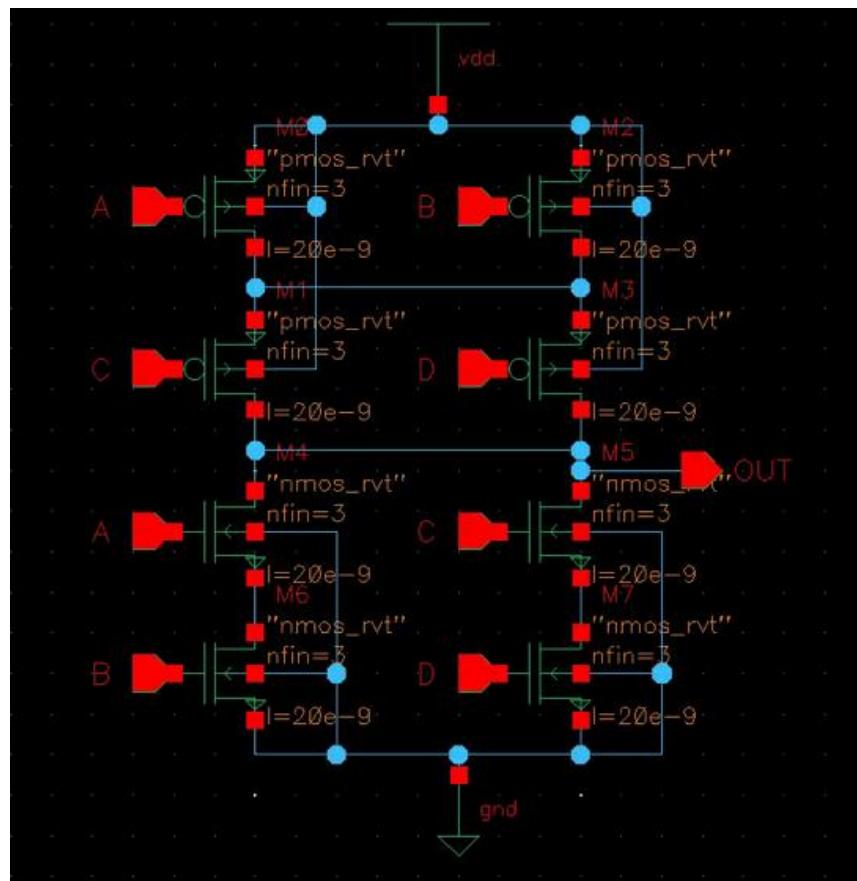
```
.include "~/asap7/7nm_TT.pm"
.include aoi21.pex.netlist
.option post runlvl=5
xi A B C OUT aoi21
VDD! VDD! GND! 0.8v
vin1 A GND! pwl(0ps 0v 4000ps 0v 4014ps 0.8v)
vin2 B GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v 4000ps 0.8v 4014ps 0v 6000ps 0v 6014ps 0.8v)
vin3 C GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v 4000ps 0.8v
4014ps 0v 5000ps 0v 5014ps 0.8v 6000ps 0.8v 6014ps 0v 7000ps 0v 7014ps 0.8v)
cout OUT GND! 10fF
.tr 1ps 8000ps
.end
```

LIB FILE :

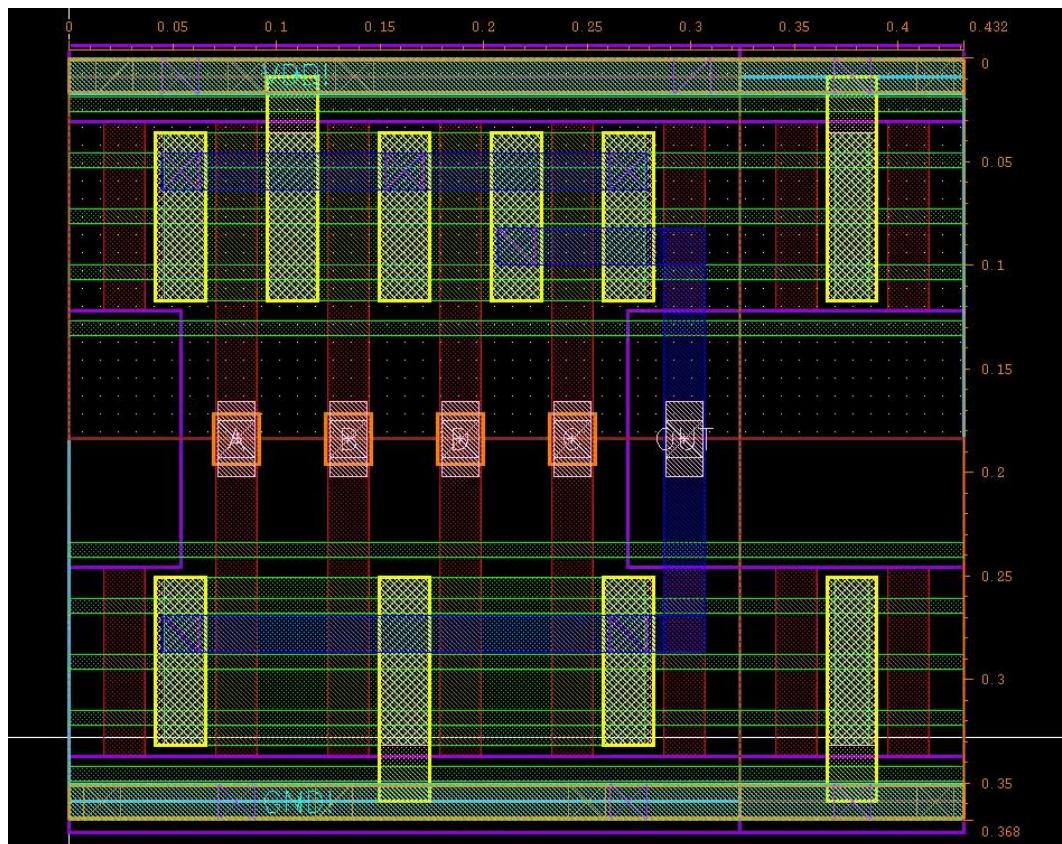
```
Generating power tests.
Generating template at Fri Mar 21 21:12:51 2025
Done generating template at Fri Mar 21 21:12:51 2025
Generate Templates: Maximum virtual memory size: 1104.34 MB
Cell AOI21 configured for characterization.
Fri Mar 21 21:12:51 CDT 2025: Done configure stage (Elapsed: 0 seconds | 0.00 hours Memory: 1104.34MB)
=====
pl_cci> characterize
=====
Fri Mar 21 21:12:54 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 21:12:54 2025: Checked out license FEATURE PrimeLib CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 21:12:54 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 21:12:54 2025: Checked out license FEATURE PrimeLib SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 21:12:54 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
AOI21: generated 11 tasks (11 total)
Using 1 standalone slots
[CDPL] Tasks: 0/11, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 1/11, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: AOI21::delay_B_lh_OUT_hl_ACQ_1 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Fri Mar 21 21:13:54 2025: Released license FEATURE PrimeLib CORE(all)
Fri Mar 21 21:13:54 2025: Released license FEATURE PrimeLib SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 21:13:54 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1105.80MB)
```

CELL#9: AIO22:

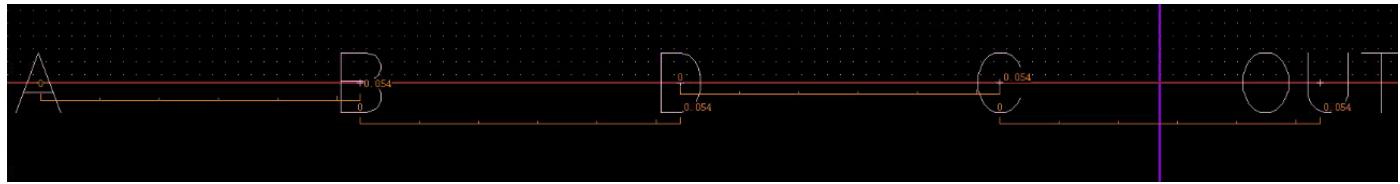
SCHEMATIC:



LAYOUT:



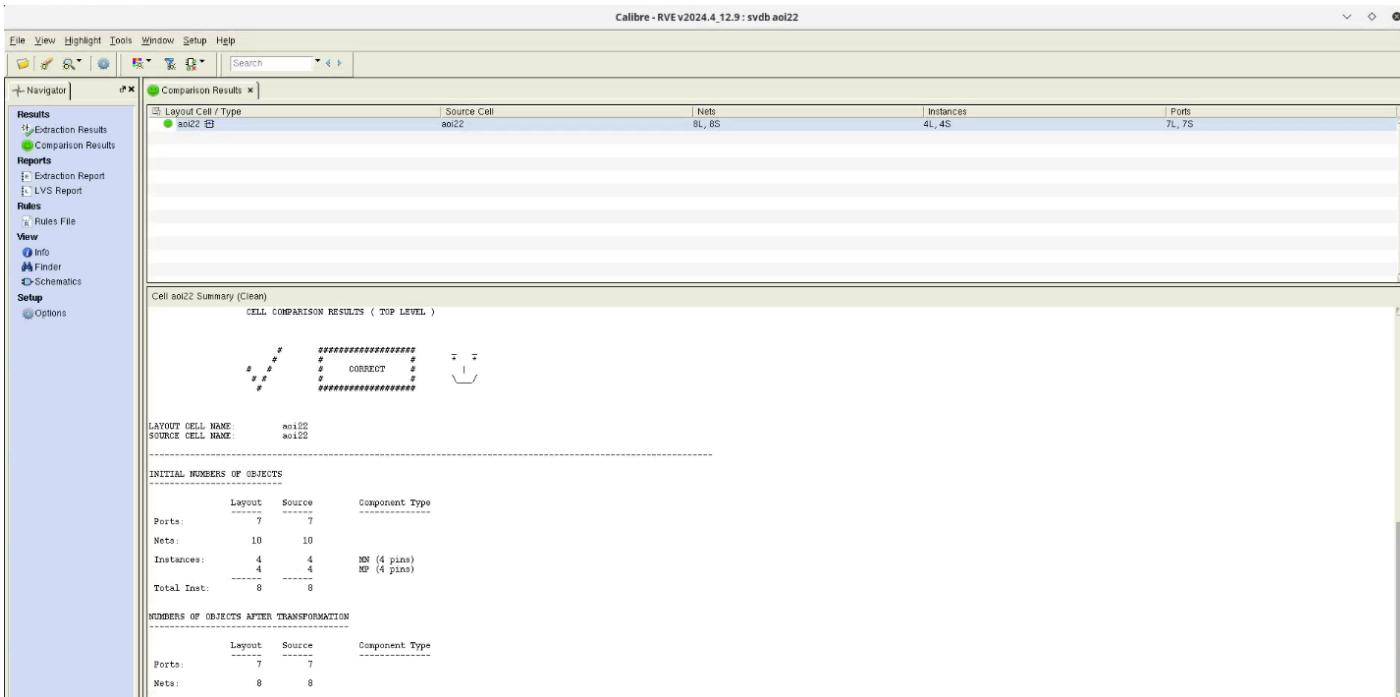
PIN_SPACING:



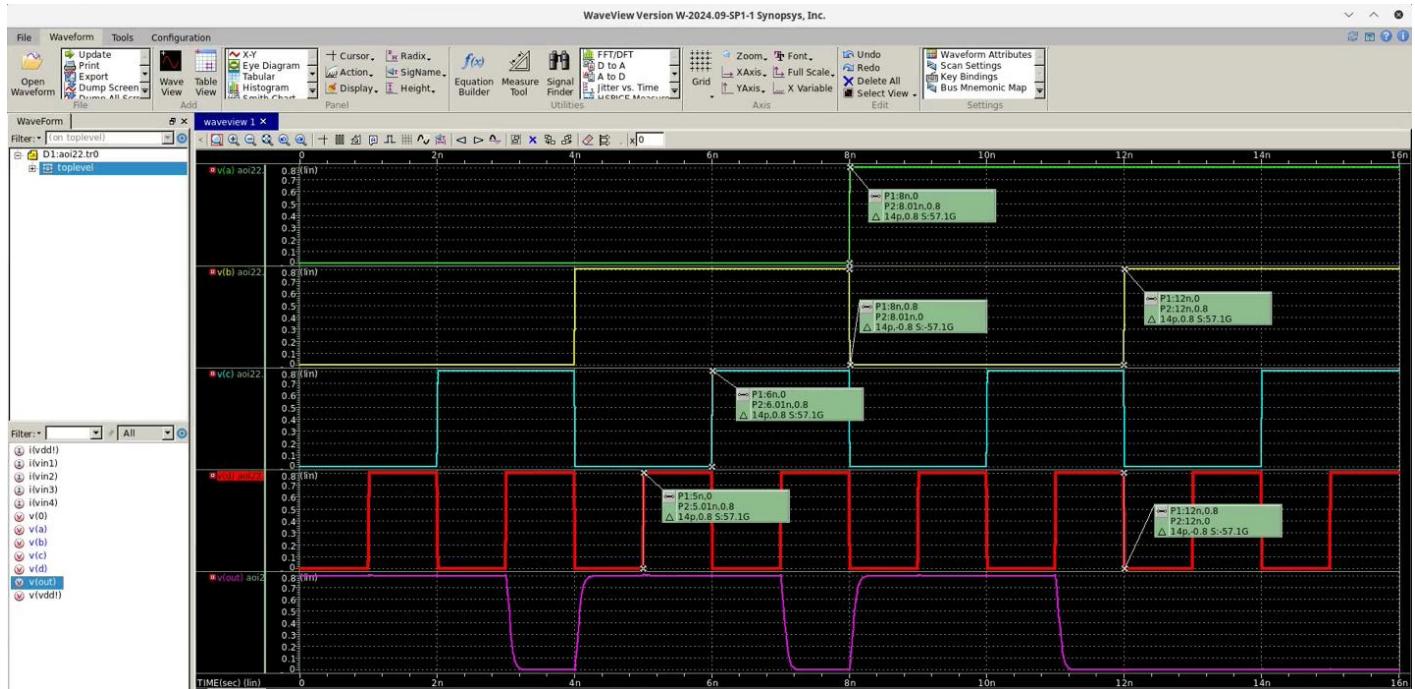
DRC CHECK:



LVS CHECK:



WAVEFORM:



Hspice file:

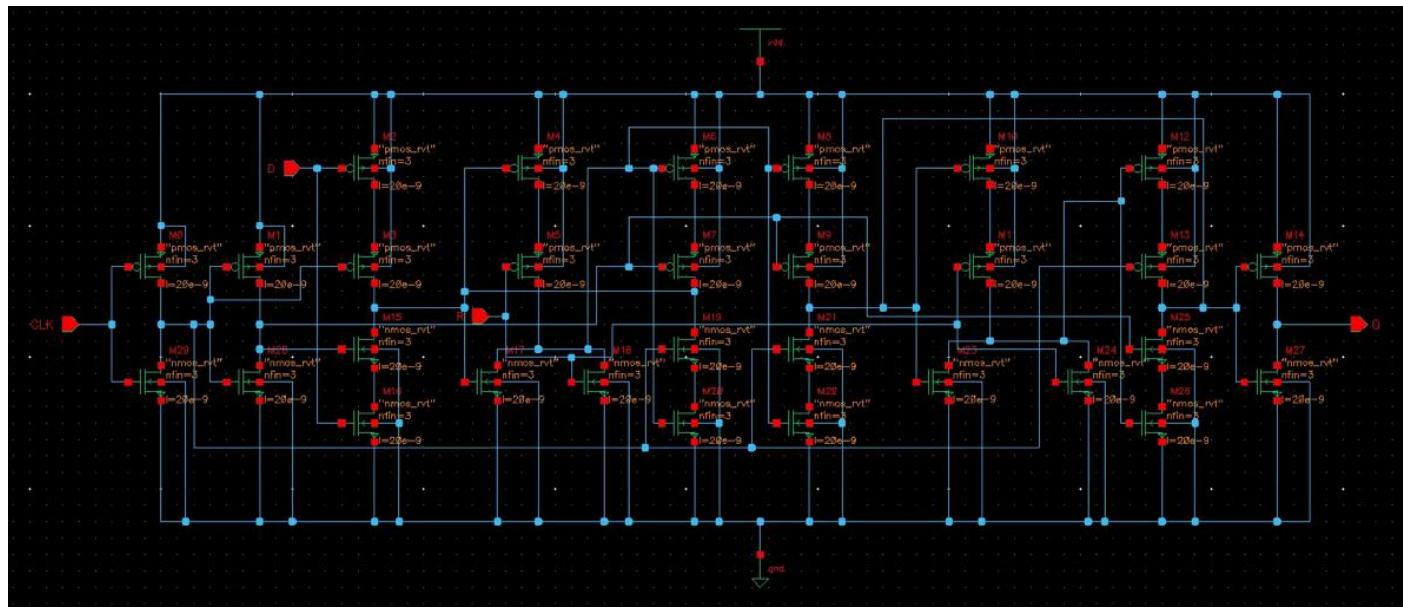
```
.include "~/asap7/7nm_TT.pm"
.include aoi22.pex.netlist
.option post runlvl=5
xi A B C D OUT aoi22
VDD! VDD! GND! 0.8v
vin1 A GND! pwl(0ps 0v 8000ps 0v 8014ps 0.8v)
vin2 B GND! pwl(0ps 0v 4000ps 0v 4014ps 0.8v 8000ps 0.8v 8014ps 0v 12000ps 0v 12014ps 0.8v)
vin3 C GND! pwl(0ps 0v 2000ps 0v 2014ps 0.8v 4000ps 0.8v 4014ps 0v 6000ps 0v 6014ps 0.8v 8000ps 0.8v
8014ps 0v 10000ps 0v 10014ps 0.8v 12000ps 0.8v 12014ps 0v 14000ps 0v 14014ps 0.8v )
vin4 D GND! pwl(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v 4000ps 0.8v
4014ps 0v 5000ps 0v 5014ps 0.8v 6000ps 0.8v 6014ps 0v 7000ps 0v 7014ps 0.8v 8000ps 0.8v 8014ps 0v
9000ps 0v 9014ps 0.8v 10000ps 0.8v 10014ps 0v 11000ps 0v 11014ps 0.8v 12000ps 0.8v 12014ps 0v
13000ps 0v 13014ps 0.8v 14000ps 0.8v 14014ps 0v 15000ps 0v 15014ps 0.8v)
cout OUT GND! 10ff
.tr 1ps 16000ps
.end
```

LIB FILE :

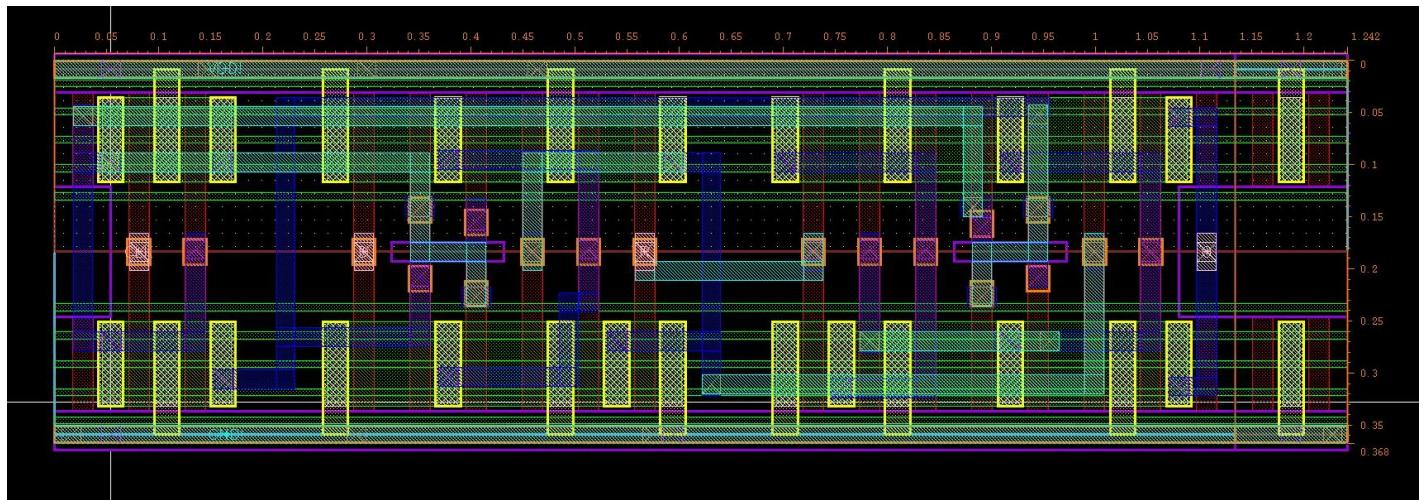
```
Generating power tests.
Generating template at Fri Mar 21 23:03:25 2025
Done generating template at Fri Mar 21 23:03:25 2025
Generate Templates: Maximum virtual memory size: 1111.76 MB
Cell AOI22 configured for characterization.
Fri Mar 21 23:03:25 CDT 2025: Done configure stage (Elapsed: 0 seconds | 0.00 hours Memory: 1111.76MB)
=====
pl_cci> characterize
=====
Fri Mar 21 23:03:28 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Fri Mar 21 23:03:29 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 23:03:29 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Fri Mar 21 23:03:29 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Fri Mar 21 23:03:29 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
AOI22: generated 13 tasks (13 total)
Using 1 standalone slots
[CDPL] Tasks: 0/13, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 13/13, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: AOI22::leakage_power_ACQ_1 30.00 seconds
[CDPL] Summary:
    All tasks finished successfully.
Fri Mar 21 23:04:29 2025: Released license FEATURE PrimeLib_CORE(all)
Fri Mar 21 23:04:29 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Fri Mar 21 23:04:29 CDT 2025: Done characterize stage (Elapsed: 61 seconds | 0.02 hours Memory: 1113.26MB)
```

CELL#10: DFF(negative edge triggered and active high reset):

SCHEMATIC:



LAYOUT:



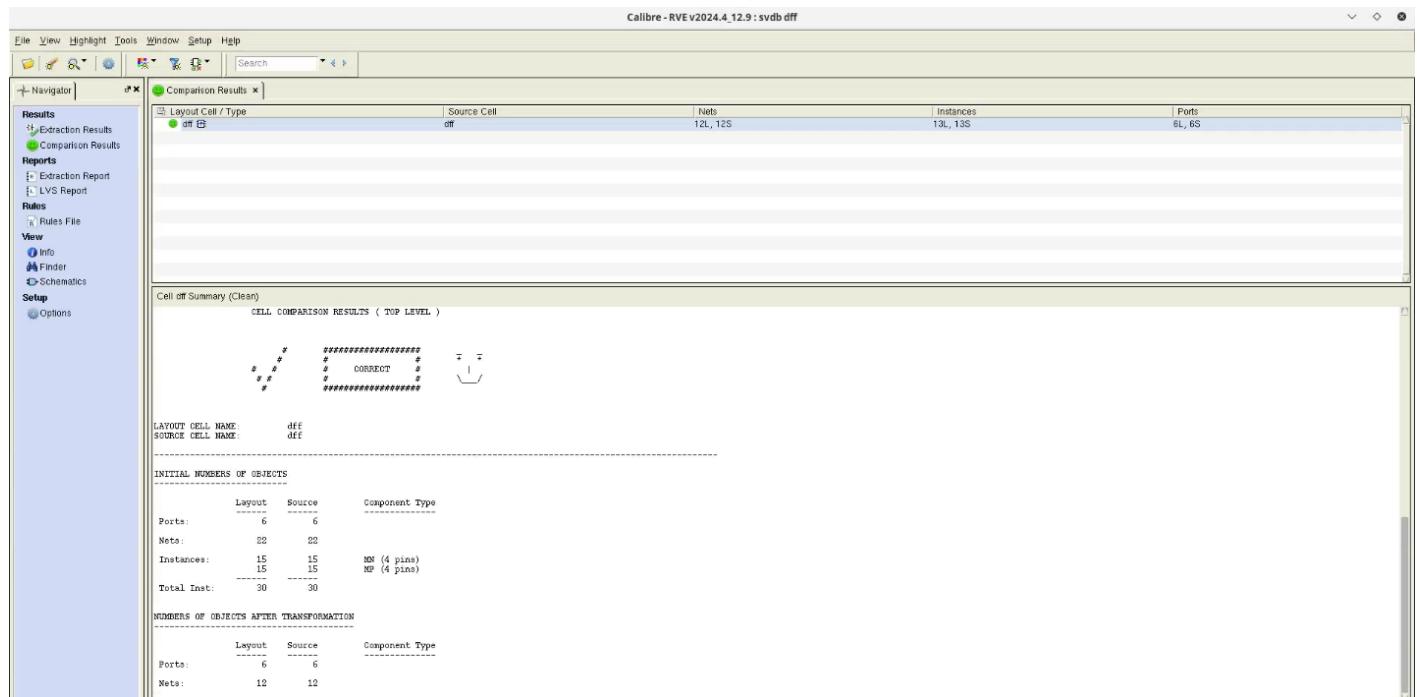
PIN_SPACING:



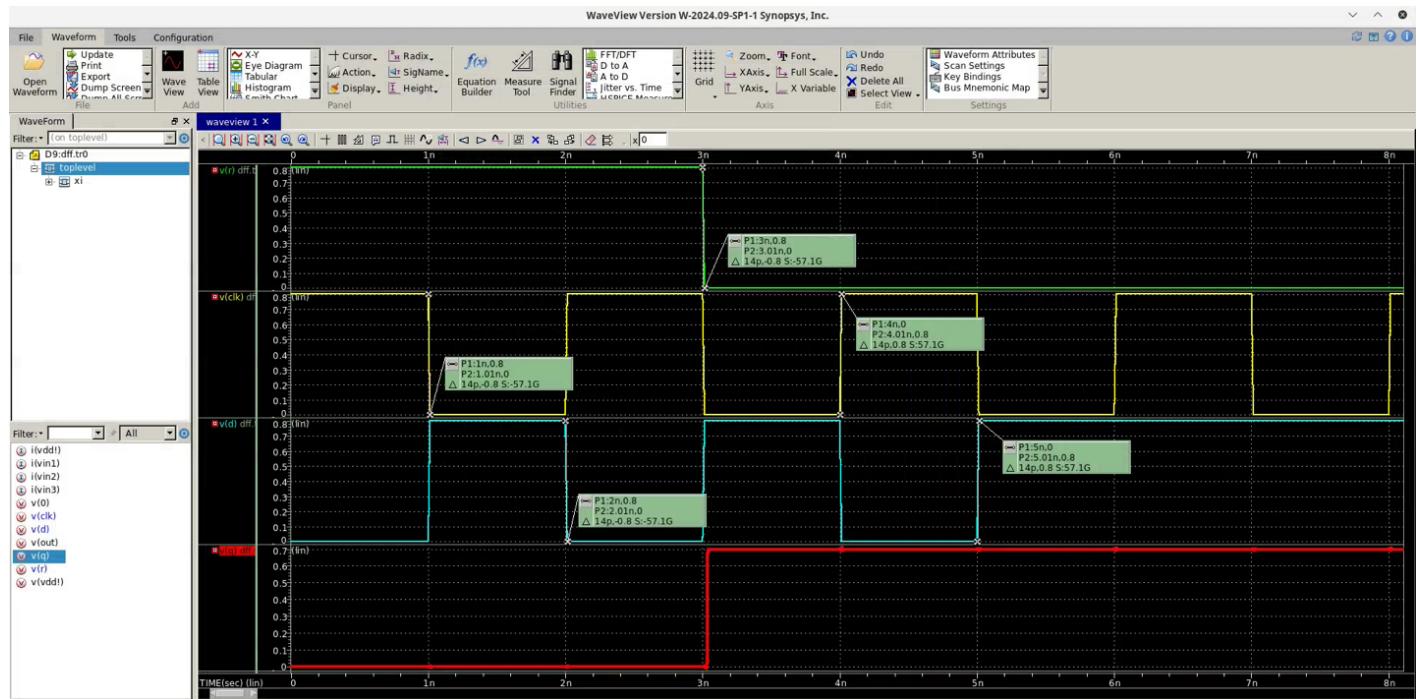
DRC CHECK:



LVS CHECK:



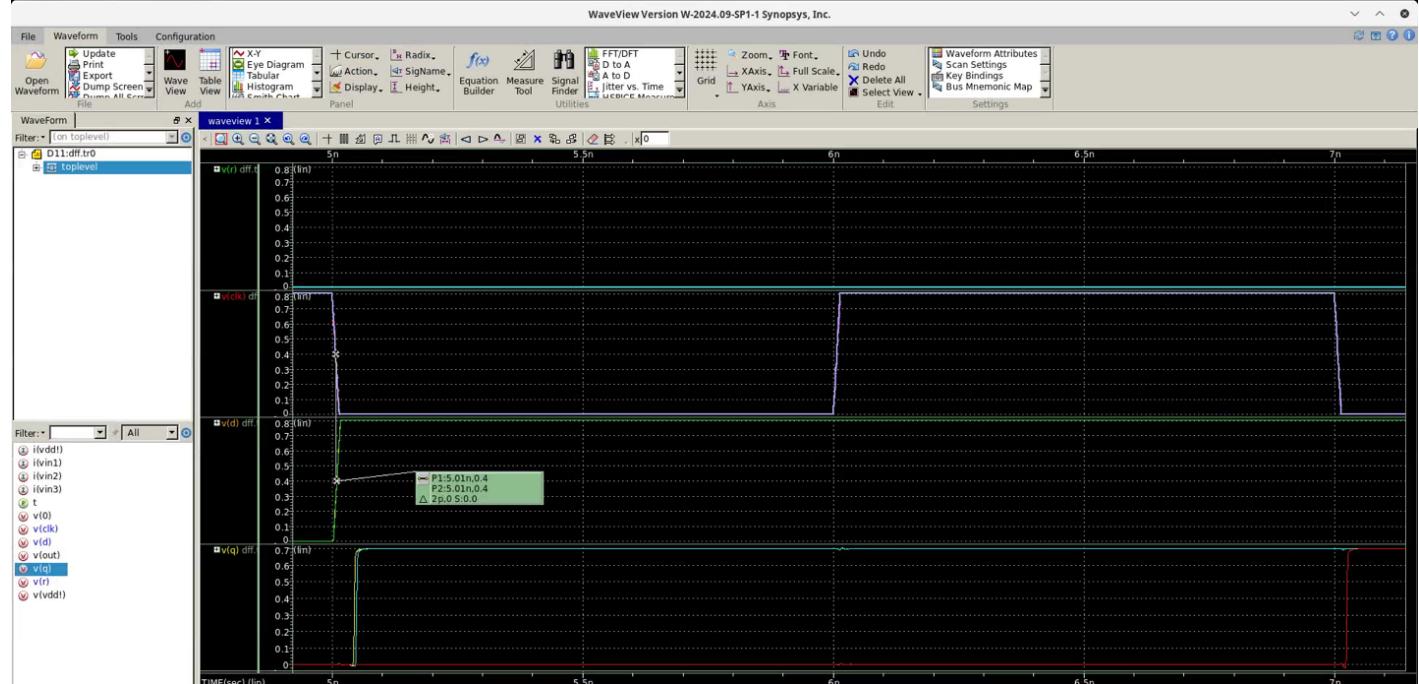
WAVEFORM:



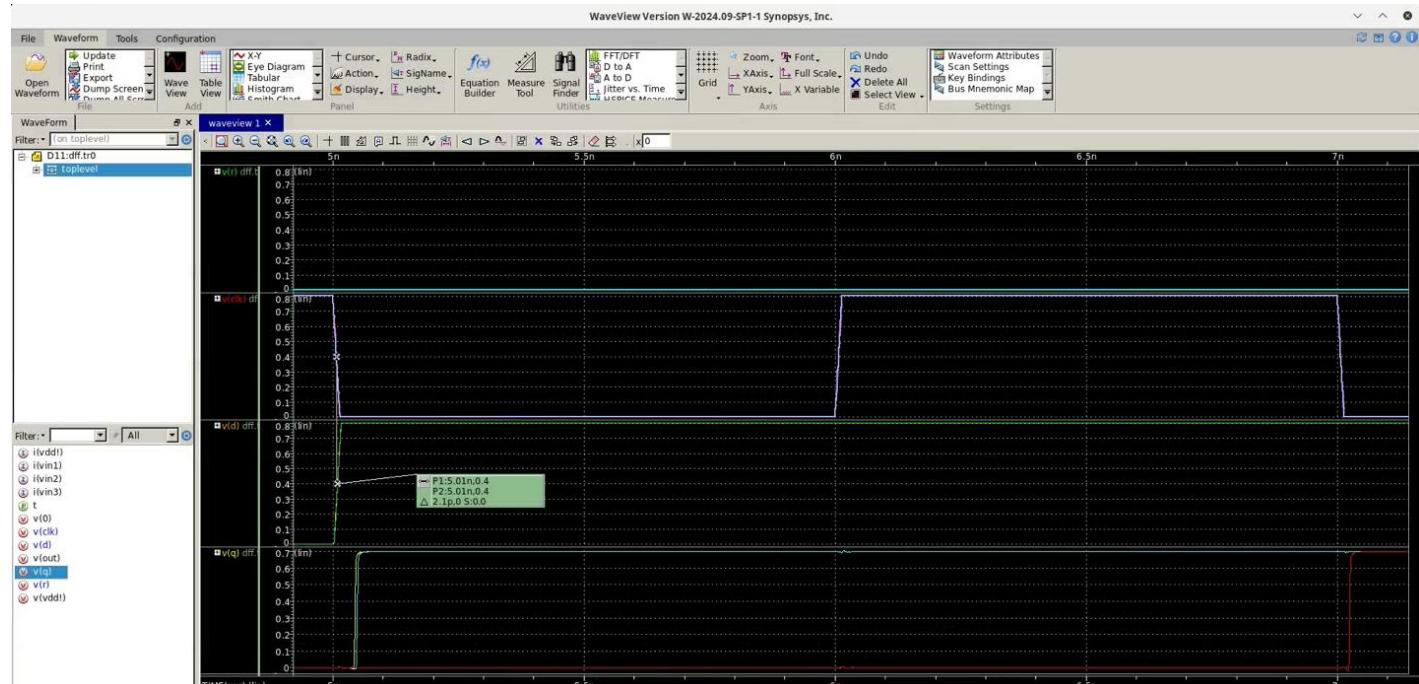
Hspice file:

```
.include " ~/asap7/7nm_TT.pm"
.include dff.pex.netlist
.option post runlvl=5
xi CLK D Q R dff
VDD! VDD! GND! 0.7v
vin1 CLK GND! pw1(0ps 0.8v 1000ps 0.8v 1014ps 0v 2000ps 0v 2014ps 0.8v 3000ps 0.8v 3014ps 0v 4000ps
0v 4014ps 0.8v 5000ps 0.8v 5014ps 0v 6000ps 0v 6014ps 0.8v 7000ps 0.8v 7014ps 0v 8000ps 0v 8014ps
0.8v)
vin2 D GND! pw1(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 3000ps 0v 3014ps 0.8v 4000ps 0.8v
4014ps 0v 5000ps 0v 5014ps 0.8v)
vin3 R GND! pw1(0ps 0.8v 3000ps 0.8v 3014ps 0v)
cout OUT GND! 10ff
.tr 1ps 8100ps
.end
```

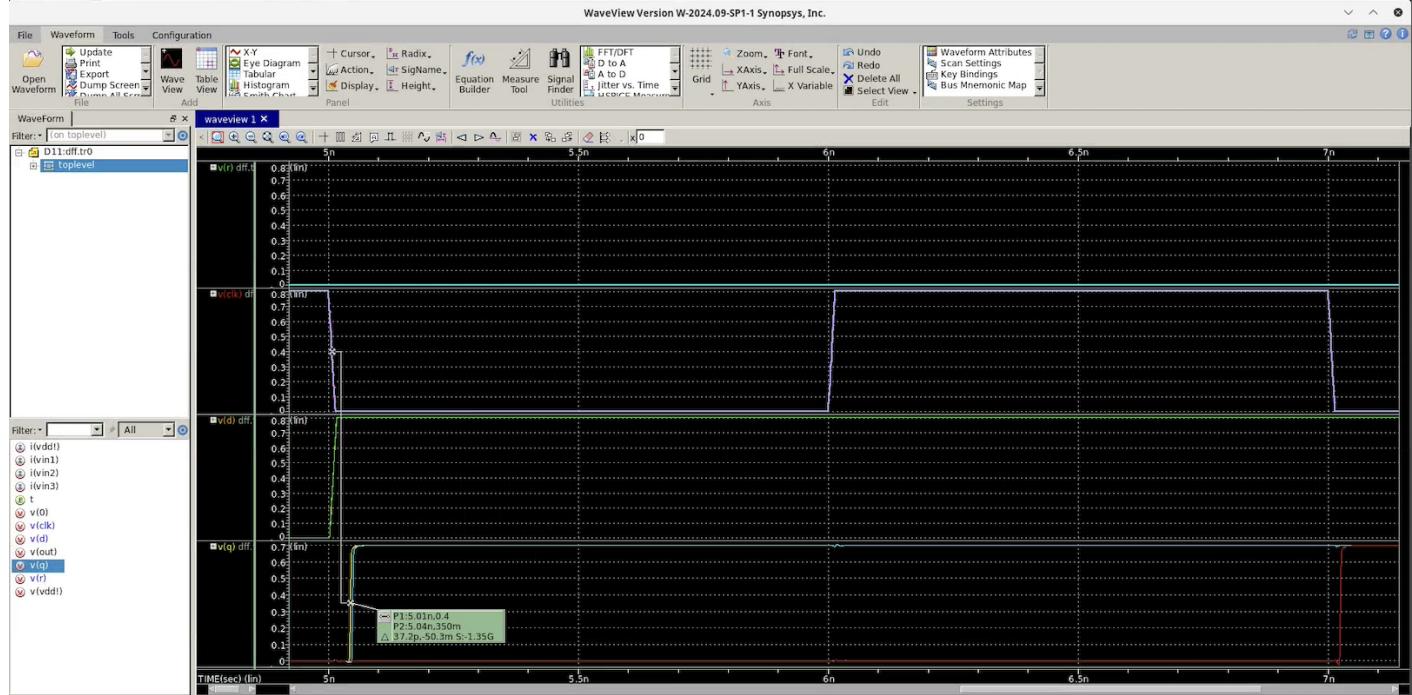
T_{su_dd}(1):



T_{su_opt}(1):



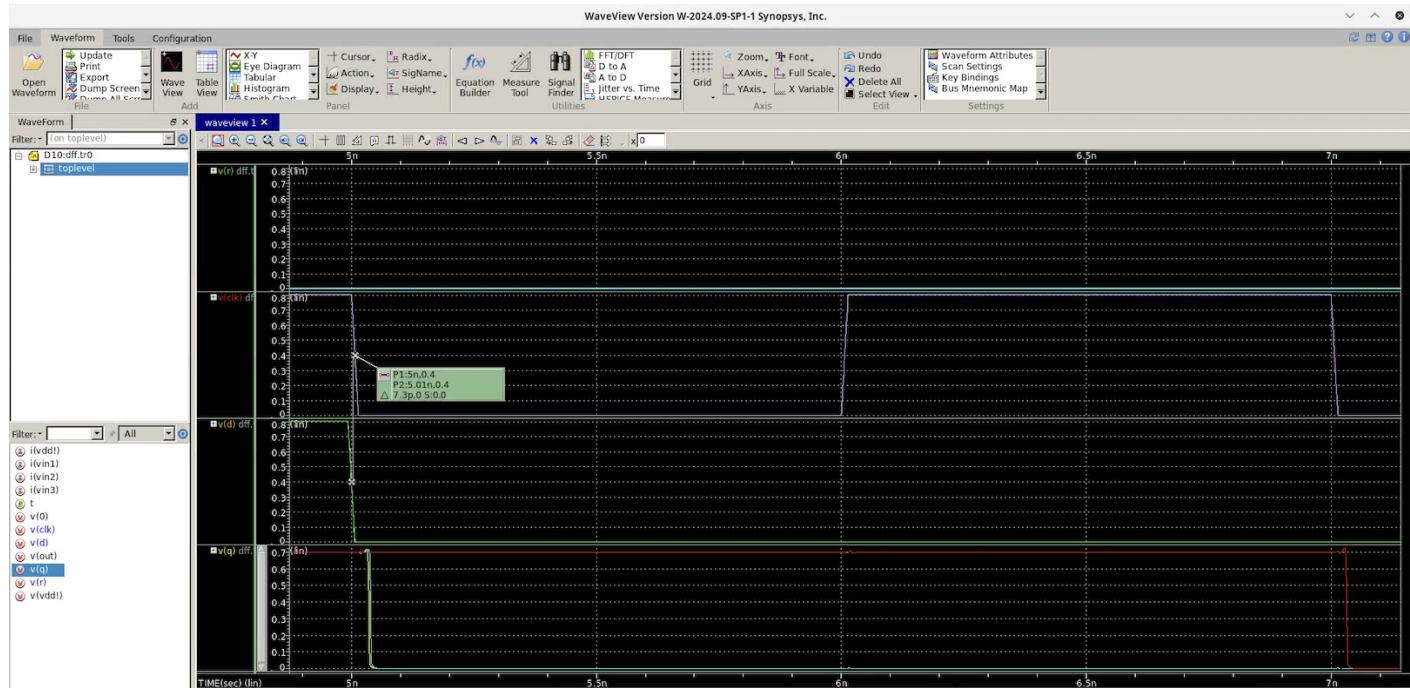
T_{clk->Q(1)}:



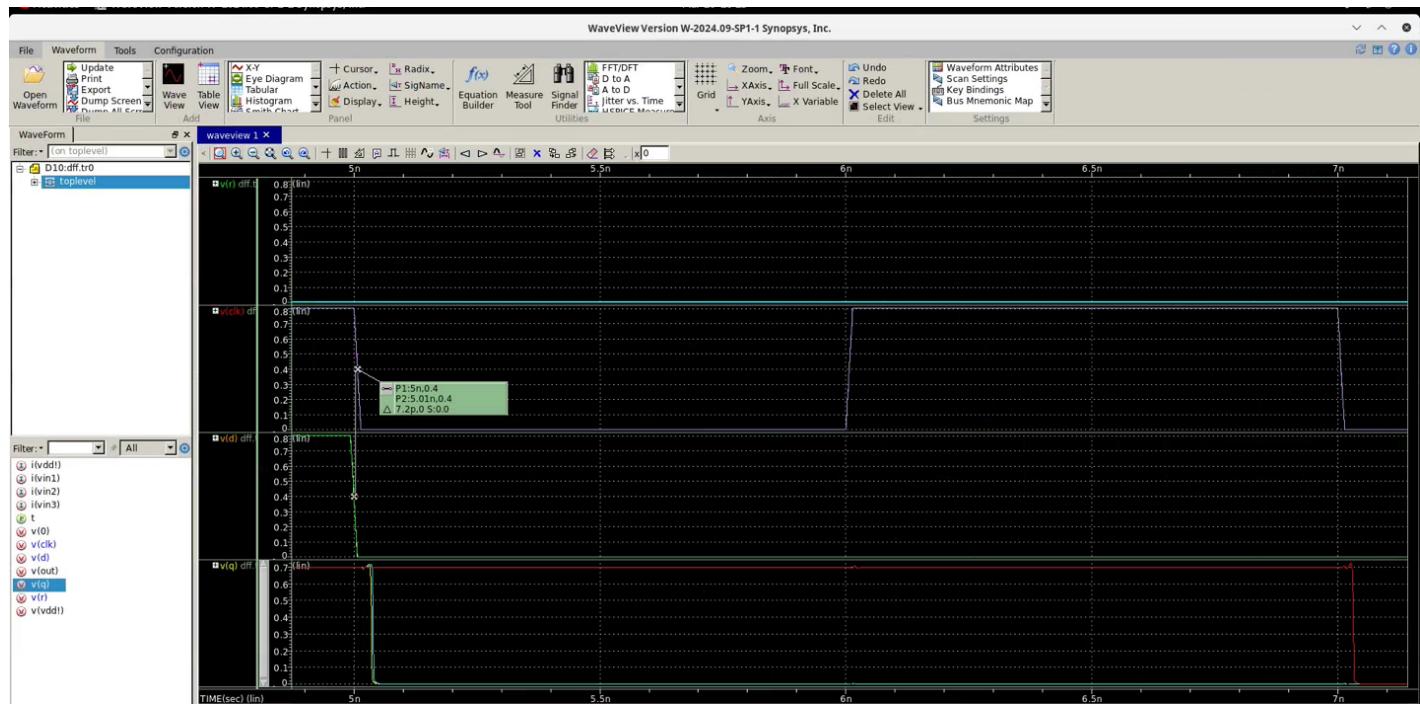
Hspice file:

```
.include "~/asap7/7nm_TT.pm"
.include dff.pex.netlist
.option post runlvl=5
xi CLK D Q R dff
VDD! VDD! GND! 0.7v
vin1 CLK GND! pw1(0ps 0.8v 1000ps 0.8v 1014ps 0v 2000ps 0v 2014ps 0.8v 3000ps 0.8v 3014ps 0v 4000ps
0v 4014ps 0.8v 5000ps 0.8v 5014ps 0v 6000ps 0v 6014ps 0.8v 7000ps 0.8v 7014ps 0v 8000ps 0v 8014ps
0.8v)
vin2 D GND! pw1(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 2014ps 0v 't' 0v 't+14ps' 0.8v)
vin3 R GND! pw1(0ps 0.8v 3000ps 0.8v 3014ps 0v)
cout OUT GND! 10fF
.tr 1ps 8100ps sweep t 5002ps 5002.2ps 0.1ps
.end
```

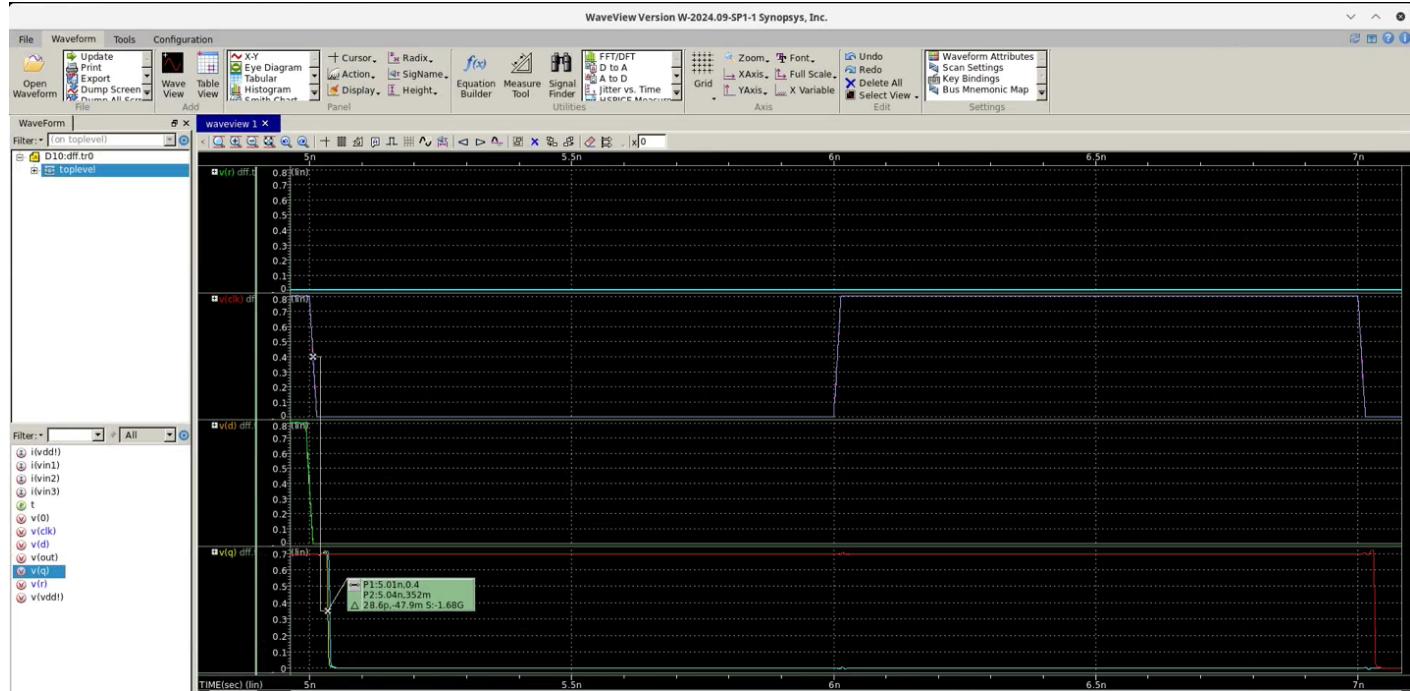
T_{su_dd}(0):



T_{su_opt}(0):



$T_{clk \rightarrow Q(0)}$:



Parameters	Transition from 0 to 1	Transition from 1 to 0
$T_{su_dd}(0)$:	2 ps	7.3ps
$T_{su_opt}(0)$:	2.1 ps	7.2ps
$T_{clk \rightarrow Q(0)}$:	37.2 ps	28.6ps
T_{hold}	7.3 ps	2 ps
T_D	39.3 ps	35.8 ps

Hspice file:

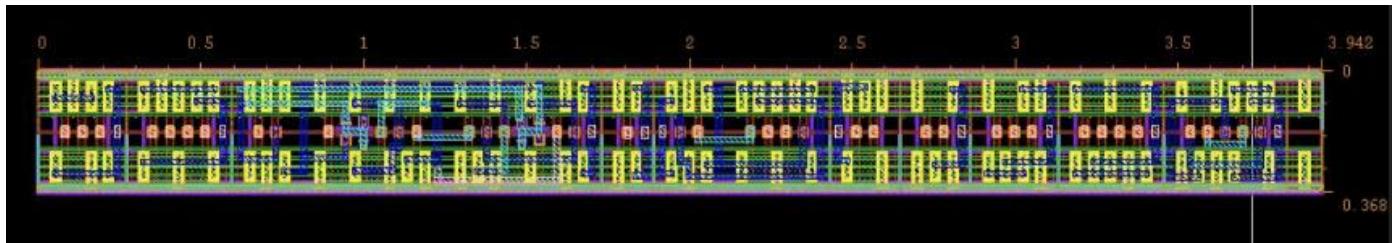
```
.include "~/asap7/7nm_TT.pm"
.include dff.pex.netlist
.option post runlvl=5
xi CLK D Q Rdff
VDD! VDD! GND! 0.7v
vin1 CLK GND! pw1(0ps 0.8v 1000ps 0.8v 1014ps 0v 2000ps 0v 2014ps 0.8v 3000ps 0.8v 3014ps 0v 4000ps
0v 4014ps 0.8v 5000ps 0.8v 5014ps 0v 6000ps 0v 6014ps 0.8v 7000ps 0.8v 7014ps 0v 8000ps 0v 8014ps
0.8v)
vin2 D GND! pw1(0ps 0v 1000ps 0v 1014ps 0.8v 2000ps 0.8v 't' 0.8v 't+14ps' 0v)
vin3 R GND! pw1(0ps 0.8v 3000ps 0.8v 3014ps 0v)
cout OUT GND! 10fF
.tr 1ps 8100ps sweep t 4992.7ps 4992.9ps 0.1ps
.end
```

LIB FILE :

```
pl_cci> characterize
=====
Wed Mar 26 21:25:13 CDT 2025: Begin characterize stage
Simulator used is hspice HSPICE 0-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_v0-2018.09-2/hspice/bin/hspice
Start generating characterization tasks
DFF: generated 28 tasks (28 total)
Using 1 standalone slots
Wed Mar 26 21:25:13 2025: Checked out license FEATURE PrimeLib_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Wed Mar 26 21:25:13 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Wed Mar 26 21:25:13 2025: Checked out license FEATURE PrimeLib_SIM_CORE v2023.12(1) on PORT 1700@engdmv.utdallas.edu
Wed Mar 26 21:25:13 2025: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
[CDPL] Tasks: 0/28, (0.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m00s
[CDPL] Tasks: 28/28, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
Long task: DFF::initialization_ACQ_7 30.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Wed Mar 26 21:26:13 2025: Released license FEATURE PrimeLib_CORE(all)
Wed Mar 26 21:26:13 2025: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Wed Mar 26 21:26:13 CDT 2025: Done characterize stage (Elapsed: 60 seconds | 0.02 hours Memory: 1091.70MB)
=====
```

COMBINED CELLS:

LAYOUT:



DRC CHECK:

