# PRACTICAL-3

AIM:

Theory:

Design of Carry Lookahead Adders :

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be **Carry Propagator** and **Carry Generator**. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below -
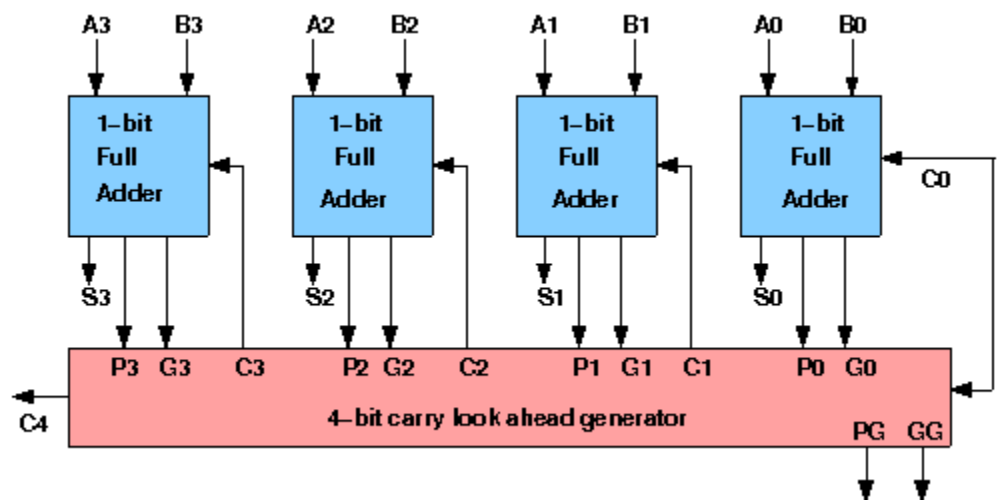
The number of gate levels for the carry propagation can be found from the circuit of full adder. The signal from input carry C_{in} to output carry C_{out} requires an AND gate and an OR gate, which constitutes two gate levels. So if there are four full adders in the parallel adder, the output carry C_5 would have 2 X 4 = 8 gate levels from C_1 to C_5. For an n-bit parallel adder, there are 2n gate levels to propagate through.

Design Issues :

The corresponding boolean expressions are given here to construct a carry lookahead adder. In the carry-lookahead circuit we ned to generate the two signals carry propagator(P) and carry generator(G),

$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i$

The output sum and carry can be expressed as

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$$\text{Sum}_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + (P_i \cdot C_i)$$

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

$$C_1 = G_0 + P_0 \cdot C_0$$

$$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$$

$$C_3 = G_2 + P_2 \cdot C_2 = G_2 P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

$$C_4 = G_3 + P_3 \cdot C_3 = G_3 P_3 \cdot G_2 P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

Objective :

Objective of 4 bit carry lookahead adder:

It computes the carries parallely thus greatly speeding up the computation.

1. understanding behaviour of carry lookahead adder from module designed by the student as part of the experiment

2. understanding the concept of reducing computation time with respect of ripple carry adder by using carry generate and propagate functions

3. the adder wil add two 4 bit numbers

Examining behaviour of carry lookahead adder for the module designed by the student as part of the experiment (refer to the circuit diagram)

Loading data in the carry lookahead adder (refer to procedure tab for further detail and experiment manual for pin numbers)

- load the two input numbers in the adder units as:

  o 1111 and 0001

Examining the carry generate and propagate function behaviour:

- check output sum 0000

- check final output carry 1

- check intermediate carry bit and sum bit of the unit adders and verify the values of carry generate and propagate function (refer to theory)

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- probing the any port can be done by verifying the color of the wire coming out of the port

Recommended learning activities for the experiment: Leaning activities are designed in two stages, a basic stage and an advanced stage. Accomplishment of each stage can be self-evaluated through the given set of quiz questions consisting of multiple type and subjective type questions. In the basic stage, it is recommended to perform the experiment firstly, on the given encapsulated working module, secondly, on the module designed by the student, having gone through the theory, objective and procuder. By performing the experiment on the working module, students can only observe the input-output behavior. Where as, performing experiments on the designed module, students can do circuit analysis, error analysis in addition with the input-output behavior. It is recommended to perform the experiments following the given guideline to check behavior and test plans along with their own circuit analysis. Then students are recommended to move on to the advanced stage. The advanced stage includes the accomplishment of the given assignments which will provide deeper understanding of the topic with innovative circuit design experience. At any time, students can mature their knowledge base by further reading the references provided for the experiment.

▢ color configuration of wire for 5 valued logic supported by the simulator:

- if value is UNKNOWN, wire color= maroon

- if value is TRUE, wire color= blue

- if value is FALSE, wire color= black

- if value is HI IMPEDENCE, wire color= green

- if value is INVALID, wire color= orange

Test plan:

1. Set one input to zero(0) and check the output.

2. Set one input to all one and another as 0001 in carry lookahead adder.

3. Check the carry lookahead adder with two arbitrary input. Check the output and show the carry propagator and generator output for every bit.

Use Display units for checking output. Try to use minimum number of components to build. The pin configuration of the canned components are shown when mouse hovered over a component.

Assignment Statements :

1. Design a 4-bit carry lookahead adder circuit using half adders and full adders and test it by giving proper input.

2. Design a 16-bit carry lookahead adder circuit using half adders and full adders and test it by giving proper input.
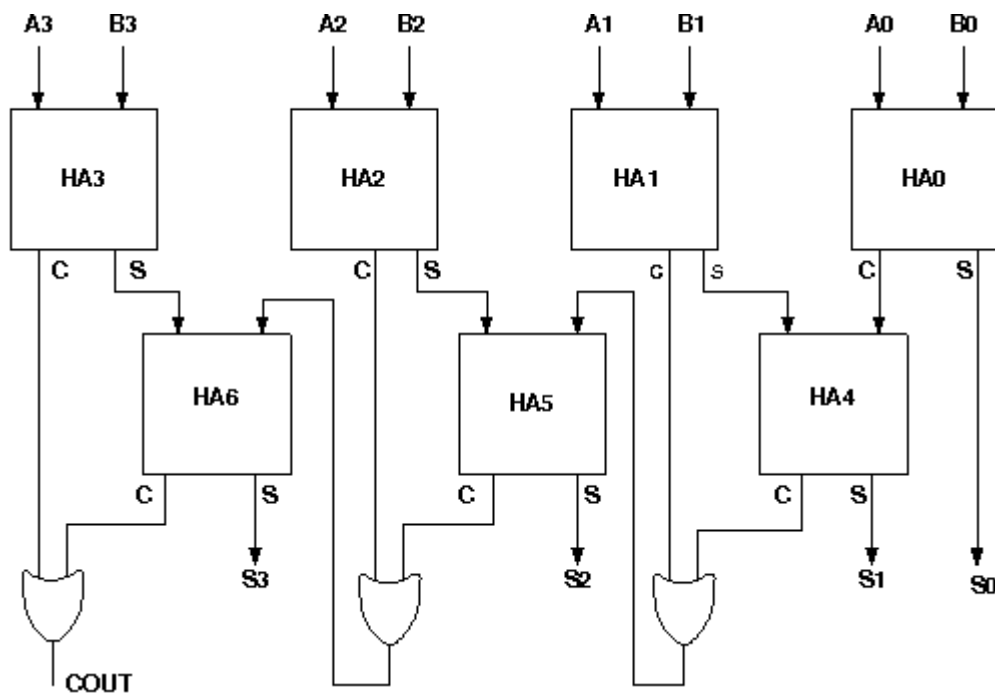
Procedure

Design of Carry Lookahead Adders :

Procedure to perform the experiment:Design of Carry Lookahead Adders

1. Start the simulator as directed.This simulator supports 5-valued logic.

2. To design the circuit we need 7 half adder, 3 OR gate, 1 V+(to give 1 as input), 3 Digital display(2 for seeing input and 1 for seeing output sum), 1 Bit display(to see the carry output), wires.

3. The pin configuration of a component is shown whenever the mouse is hovered on any canned component of the palette or press the 'show pinconfig' button. Pin numbering starts from 1 and from the bottom left corner(indicating with the circle) and increases anticlockwise.

4. For half adder input is in pin-5,8 output sum is in pin-4 and carry is pin-1

5. Click on the half adder component(in the Adder drawer in the pallet) and then click on the position of the editor window where you want to add the component(no drag and drop, simple click will serve the purpose), likewise add 6 more full adders(from the Adder drawer in the pallet), 3 OR gates(from Logic Gates drawer in the pallete), 1 V+, 3 digital display and 1 bit Displays(from Display and Input drawer of the pallet,if it is not seen scroll down in the drawer)

6. To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit diagram connect all the components, connect V+ to the upper input terminals of 2 digital displays according to you input. connect the OR gates according to the diagram shown in the screenshot connect the pin-1 of the half adder which will give the final carry output. connet the sum(pin-4) of those adders to the terminals of the third digital display which will give output sum. After

the connection is over click the selection tool in the pallete.

7. See the output, in the screenshot diagram we have given the value 0011(3) and 0111(7) so get 10 as sum and 0 as carry.you can also use many bit switches instead of V+ to give input and by double clicking those bit switches can give different values and check the result.

Circuit diagram of Carry Lookahead Adder:

Screenshot of Carry Lookahead Adder:
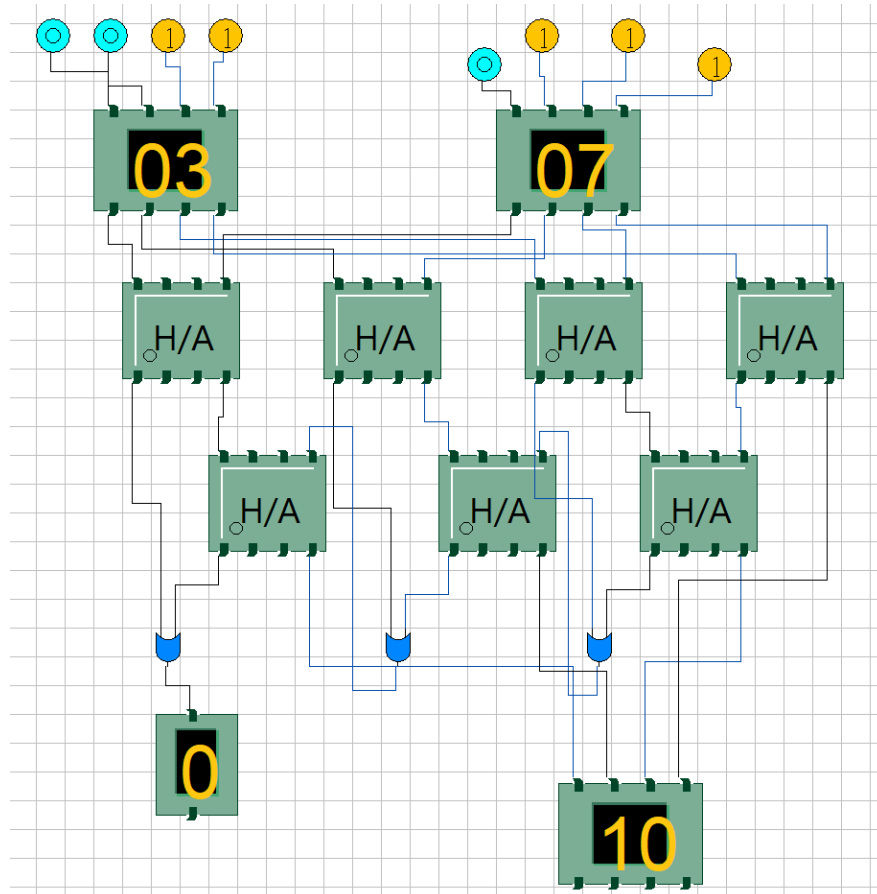
Components :

The components needed to create 4 bit carry lookahead adder is listed here -

- 7 half-adders: 4 to create the look adder circuit, and 3 to evaluate S_i and $P_i \cdot C_i$

- 3 OR gates to generate the next level carry C_{i+1}

- wires to connect

- LED display to obtain the output

Experiment :

Design of Carry Lookahead Adders :

General guideline to use the simulator for performing the experiment:

- Start the simulator as directed. For more detail please refer to the manual for using the simulator

- The simulator supports 5-valued logic

- To add the logic components to the editor or canvas (where you build the circuit) select any component and click on the position of the canvas where you want to add the component
- The pin configuration is shown when you select the component and press the 'show pinconfig' button in the left toolbar or whenever the mouse is hovered on any canned component of palette
- To connect any two components select the connection tool of palette, and then click on the source terminal and then click on the the target terminal
- To move any component select the component using the selection tool and drag the component to the desired position
- To give a toggle input to the circuit, use 'Bit Switch' which will toggle its value with a double click
- Use 'Bit Display' component to see any single bit value. 'Digital Display' will show the output in digital format
- undo/redo, delete, zoom in/zoom out, and other functionalities have been given in the top toolbar for ease of circuit building
- Use start/stop clock pulse to start or stop the clock input of the circuit. Clock period can be set from the given 'set clock' button in the left toolbar
- Use 'plot graph' button to see input-output wave forms
- Users can save their circuits with .logic extension and reuse them
- After building the circuit press the simulate button in the top toolbar to get the output
- If the circuit contains a clock pulse input, then the 'start clock' button will start the simulation of the whole circuit. Then there is no need to again press the 'simulate' button