Computer Architecture and Organization

GANPAT UNIVERSITY									
FACULTY OF ENGINEERING & TECHNOLOGY									
Programme	Bachelor of Technology					Branch/Spec.	Computer Engineering / Information Technology		
Semester	V					Version	2.0.0.0		
Effective from Academic Year		2020-21				Effective for the batch Admitted in		July 2018	
Subject code	2CEIT501	Subject Name				Computer Architecture & Organization			
Teaching scheme						Examination scheme (Marks)			
(Per week)	Lecture (DT)		Practical (Lab.)		Total		CE	SEE	Total
	L	TU	P	TW					
Credit	3	0	1	-	4	Theory	40	60	100
Hours	3	0	2	-	5	Practical	30	20	50
Pre-requisites:									
Digital Electronics									

Computer Architecture and Organization

Theory syllabus		
Unit	Content	Hrs
1	**Overview of Register Transfer and Micro Operations:** Register Transfer Language, Register Transfer, Bus & Memory Transfer, Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro Operations, Arithmetic Logic Shift Unit.	05
2	**Basic Computer Organization and Design:** Instruction Codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycle, Memory-Reference Instructions, Input-Output & Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator Unit.	05
3	**Micro Programmed Control:** Control Memory, Address Sequencing, Micro Program Example, Design of Control Unit.	03
4	**Central Processing Unit:** Introduction, General Register Organization, Stack Organization, Instruction Format, Addressing Modes, Data Transfer & Manipulation, Program Control, Reduced Instruction Set Computer (RISC).	05

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5	**Pipeline and Vector Processing:** Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction, Pipeline, RISC Pipeline, Vector Processing, Array Processor.	04
6	**Input – Output Organization:** Input-Output Interface, Asynchronous Data Transfer, Modes Of Transfer, Priority Interrupt, DMA, Input-Output Processor (IOP), CPUIOP Communication, Serial Communication.	04
7	**Memory Organization:** Memory Sub System, Memory Hierarchy, Main Memory, Auxiliary Memory, Flash Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware.	05

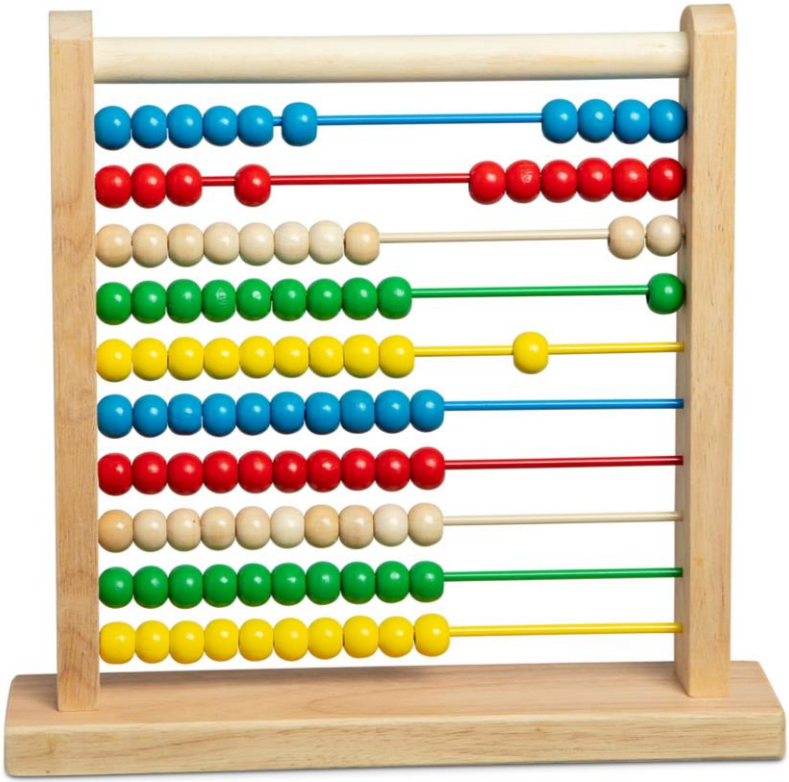
Computer Architecture and Organization

8	**Microprocessor Architecture:** 8085 Architecture, Instruction Set, Instruction Types & Formats, Instruction Execution,	14
	Instruction Cycles, Different Types of Machine Cycles & Timing Diagram, 16-Bit Microprocessors, 8086 Architecture, Registers, Memory Segmentation & Addressing, 32-Bit/64-Bit Microprocessor Families.	

Computer
Evolution and Performance

Early History of Computer

- One of the earliest and most well-known devices was an abacus.
- Then in 1822, the father of computers, Charles Babbage began developing what would be the first mechanical computer.



Science Museum – South Kensington - London – UK

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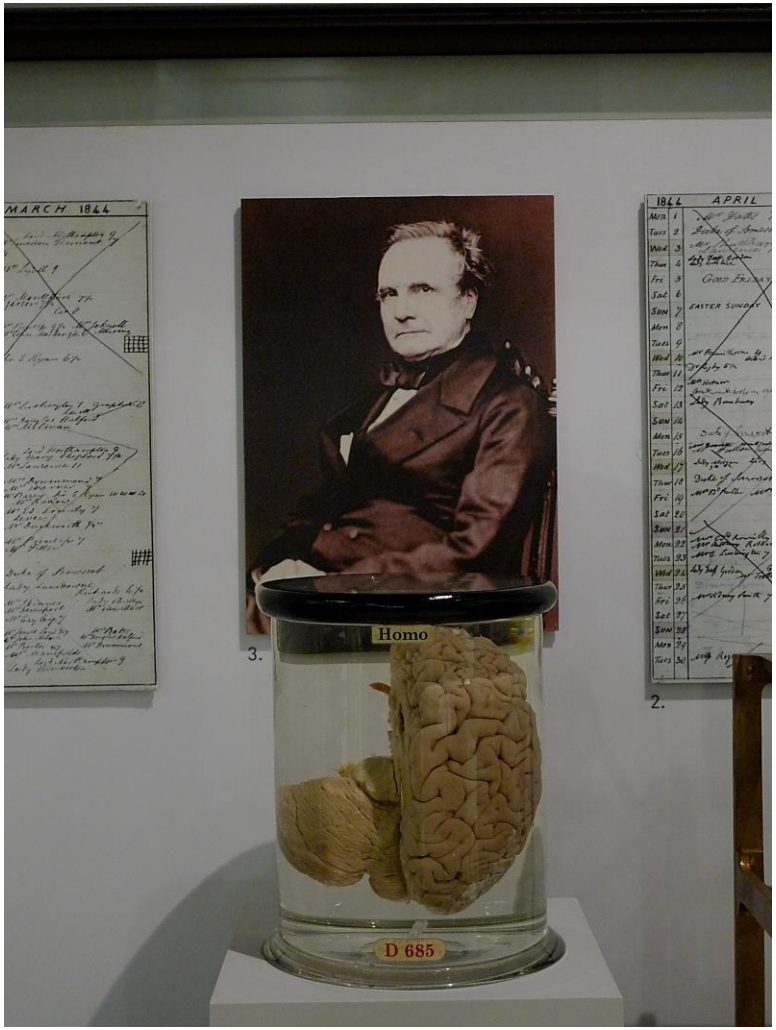
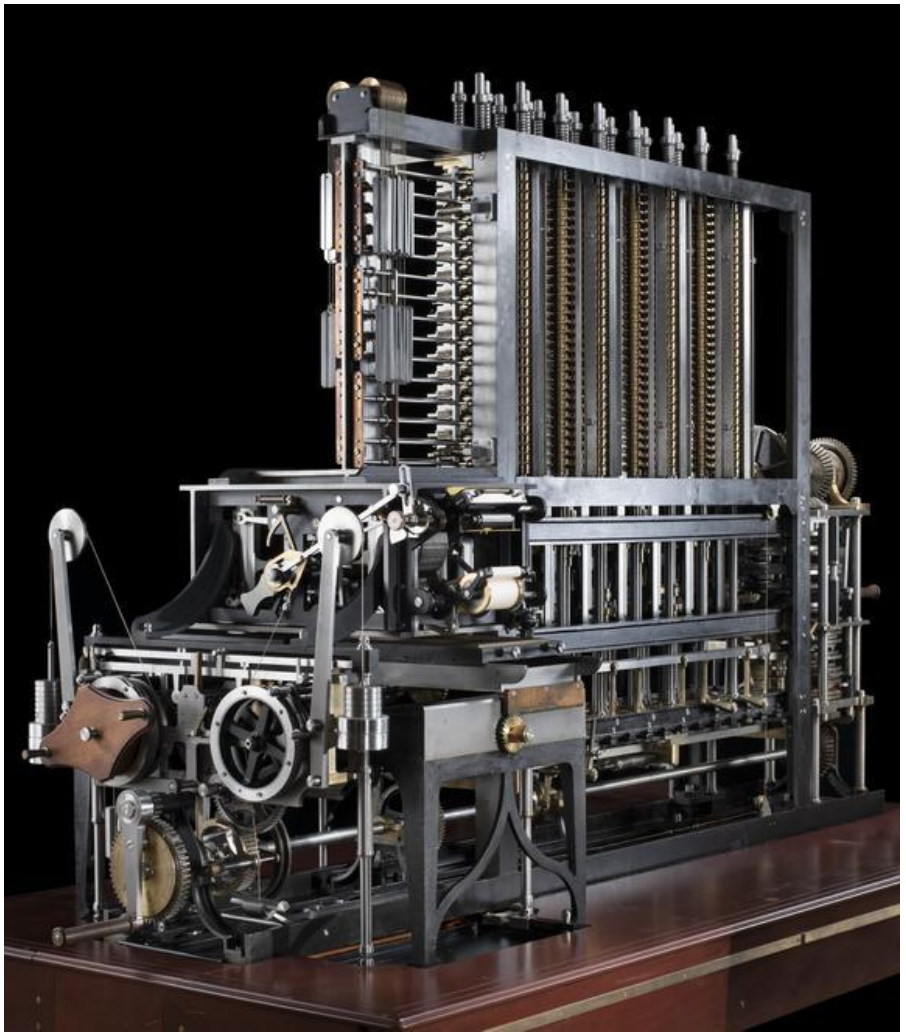




- World war I:

  28 July 1914 – 11 November 1918

- World war II:

  1 September 1939 – 2 September 1945

Turing Machine

- The Imitation Game is a 2014 American period biographical thriller film.
- Based on the 1983 biography Alan Turing: The Enigma by Andrew Hodges.
- Turing machines, first described by Alan Turing in Turing 1936–7, are simple abstract computational devices intended to help investigate the extent and limitations of what can be computed. Turing's 'automatic machines', as he termed them in 1936, were specifically devised for the computing of real numbers.

Turing Machine

- Germany's Army, Air Force and Navy transmitted many thousands of coded messages each day during World War II.

- These ranged from top-level signals, such as detailed situation reports prepared by generals at the battle fronts, and orders signed by Hitler himself, down to the important minutiae of war like weather reports and inventories of the contents of supply ships.

- Turing pitted machine against machine. The prototype model of his anti-Enigma "bombe", named simply Victory, was installed in the spring of 1940.

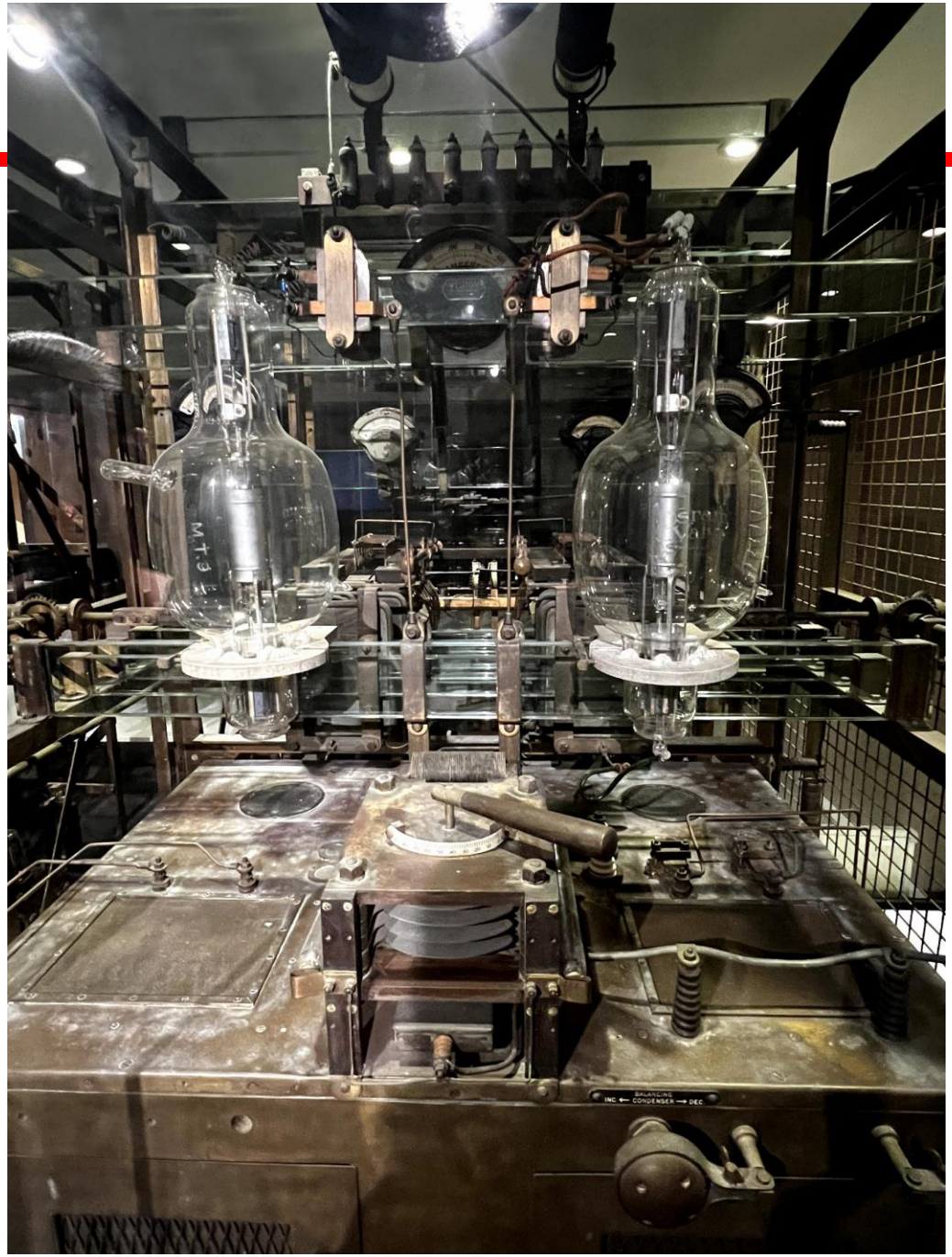
- His bombes turned Bletchley Park into a codebreaking factory. As early as 1943 Turing's machines were cracking a staggering total of 84,000 Enigma messages each month - two messages every minute.

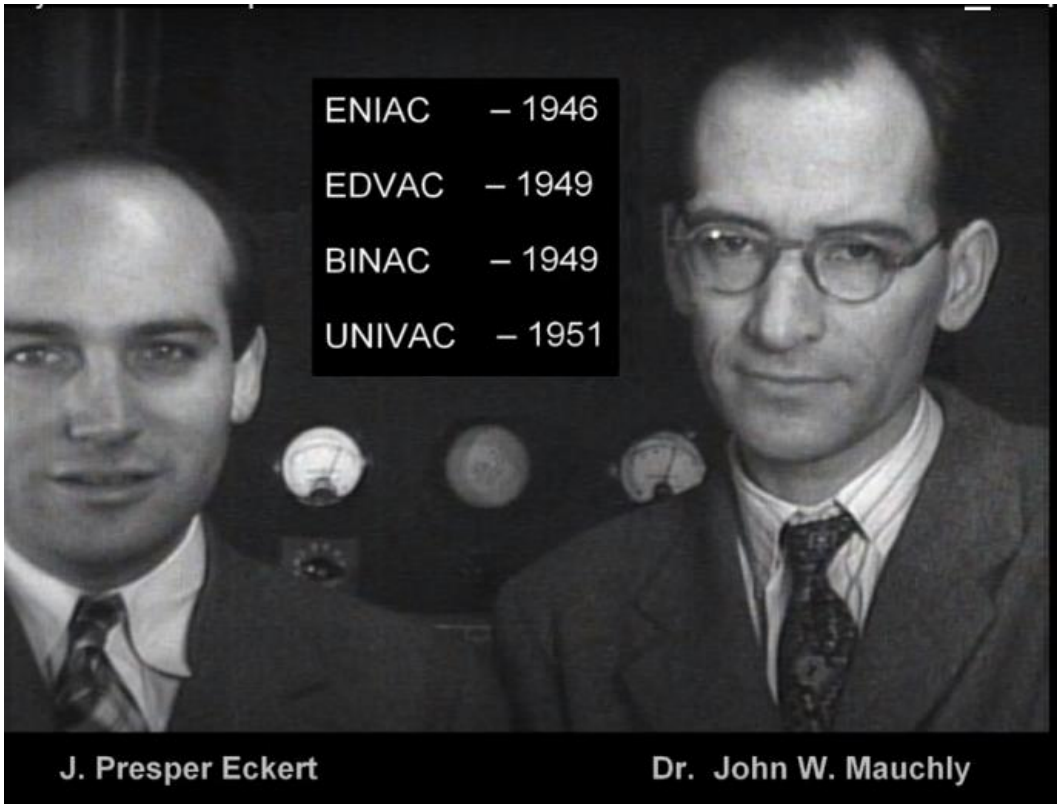
ENIAC - background

- Electronic Numerical Integrator And Computer
- Eckert and Mauchly
- University of Pennsylvania
- Trajectory tables for weapons
- Started 1943
- Finished 1946
  - Too late for war effort
- Used until 1955

ENIAC - details

- Decimal (not binary)
- 20 accumulators of 10 digits
- Programmed manually by switches
- 18,000 vacuum tubes
- 30 tons
- 15,000 square feet
- 140 kW power consumption
- 5,000 additions per second


MT3
BALANCING
INC ← CONDENSER → DEC

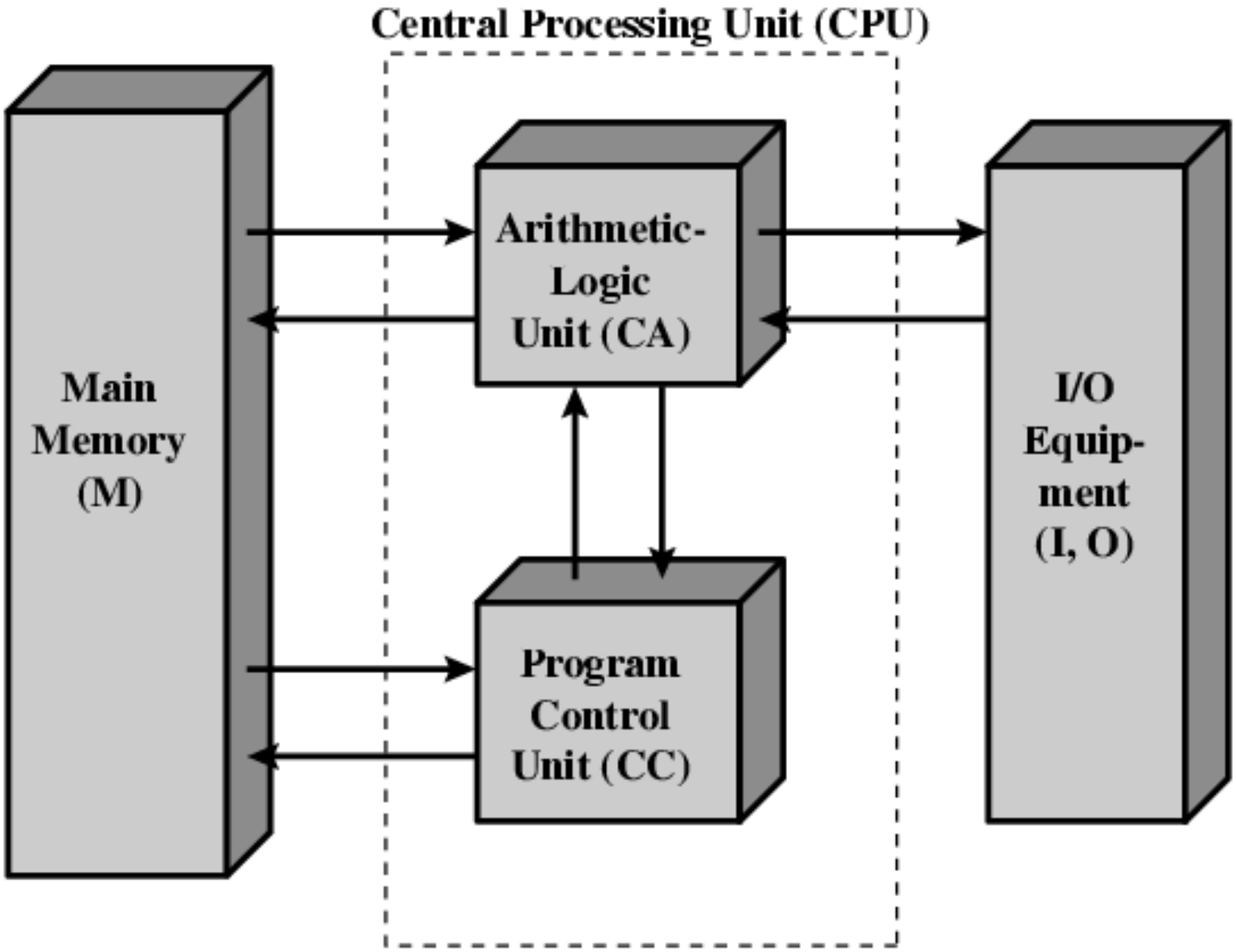


- Electronic Numerical Integrator and Computer
- Electronic Discrete Variable Automatic Computer
- Binary Automatic Computer
- Universal Automatic Computer

Von Neumann/Turing

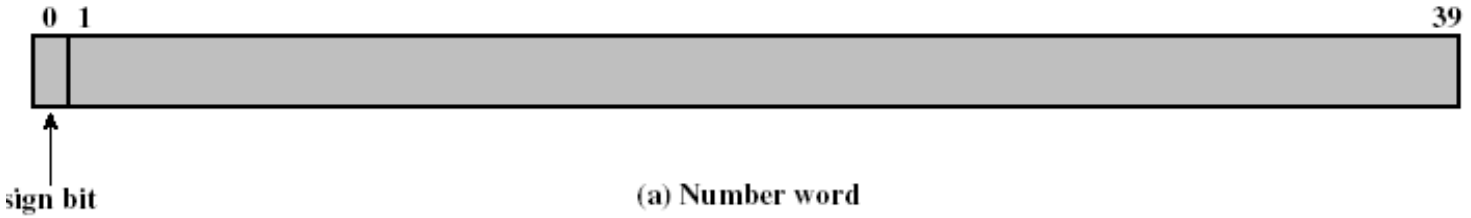
- Stored Program concept
- Main memory storing programs and data
- ALU operating on binary data
- Control unit interpreting instructions from memory and executing
- Input and output equipment operated by control unit
- Princeton Institute for Advanced Studies
  - —IAS
- Completed 1952
- Used the term “organ” to describe devices

Structure of von Neumann machine

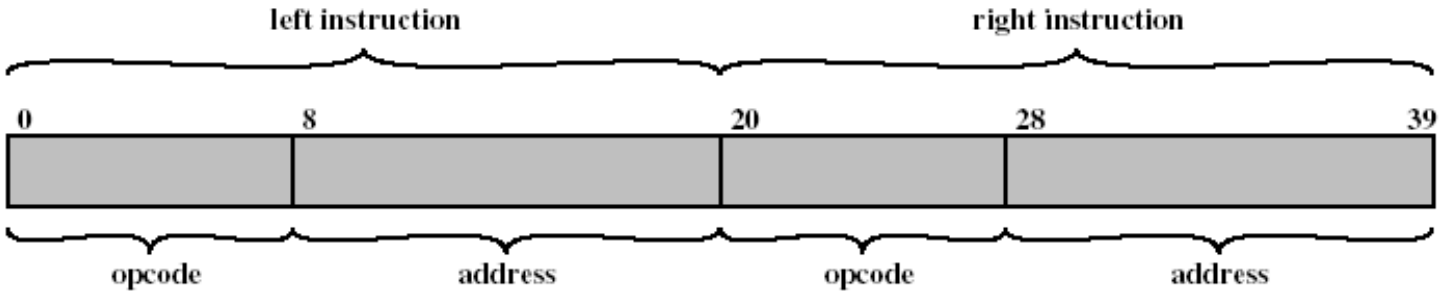


IAS - details

- 1000 x 40 bit words
  - —Binary number
  - —2 x 20 bit instructions



(a) Number word



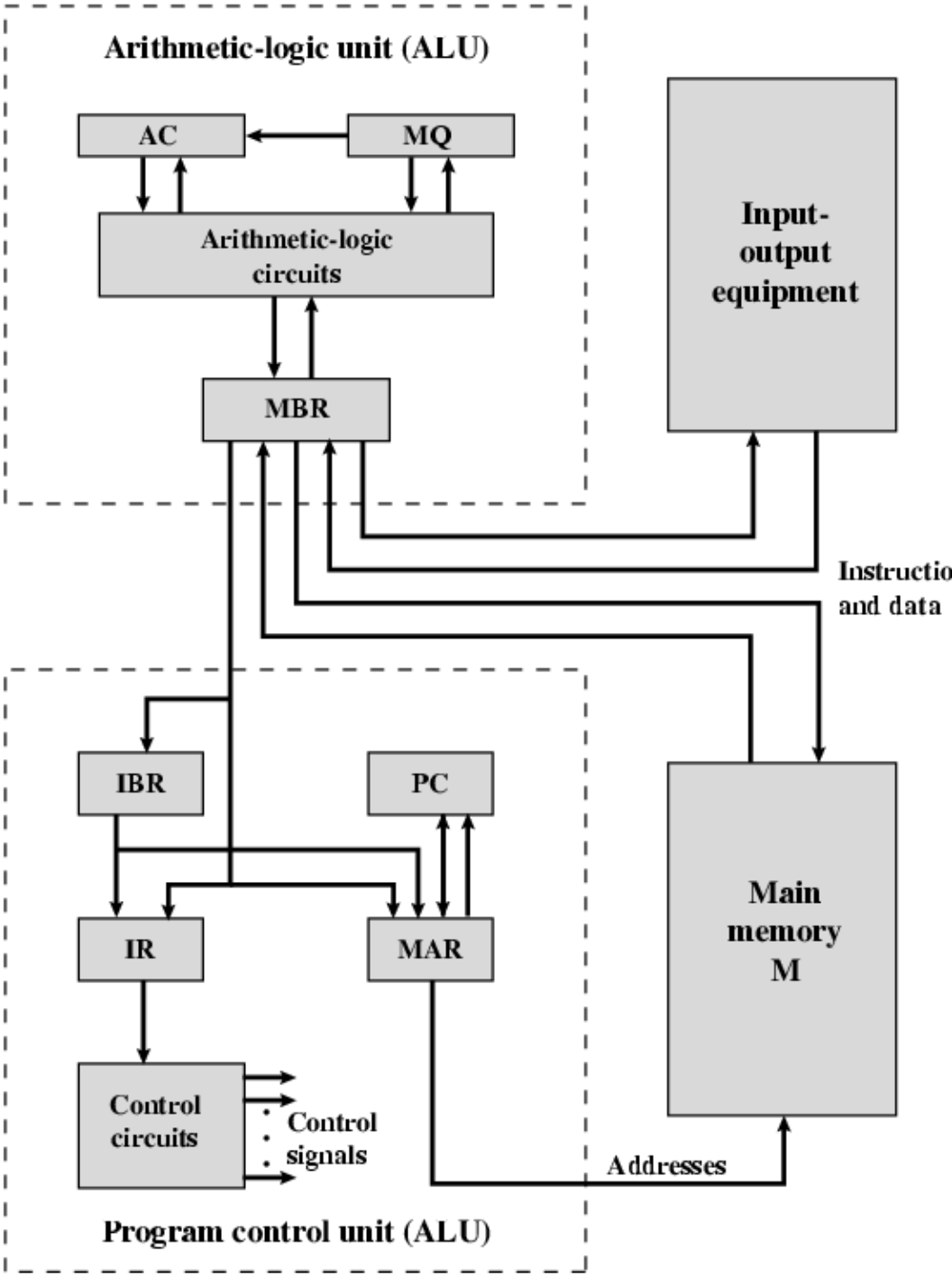
(b) Instruction word

IAS - details

- Set of registers (storage in CPU)
  - Memory Buffer Register (MBR)
  - Memory Address Register (MAR)
  - Instruction Register (IR)
  - Instruction Buffer Register (IBR)
  - Program Counter (PC)
  - Accumulator (AC)
  - Multiplier Quotient (MQ)

Structure of IAS – detail

Also see Figure 2.4 that illustrates *Fetch cycle* and *Execution cycle*, which taken together is the *Instruction cycle*.



IAS Instruction Set

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD –M(X)	Transfer –M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD –|M(X)|	Transfer –|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP+ M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP+ M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2, i.e., shift left one bit position
	00010101	RSH	Divide accumulator by 2, i.e., shift right one position
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits of AC

Commercial Computers

- 1947 - Eckert-Mauchly Computer Corporation
- UNIVAC I (Universal Automatic Computer)
- US Bureau of Census 1950 calculations
- Became part of Sperry-Rand Corporation
- Late 1950s - UNIVAC II
  - Faster
  - More memory

IBM

- Punched-card processing equipment
- 1953 - the 701
  - —IBM's first stored program computer
  - —Scientific calculations
- 1955 - the 702
  - —Business applications
- Lead to 700/7000 series

Transistors

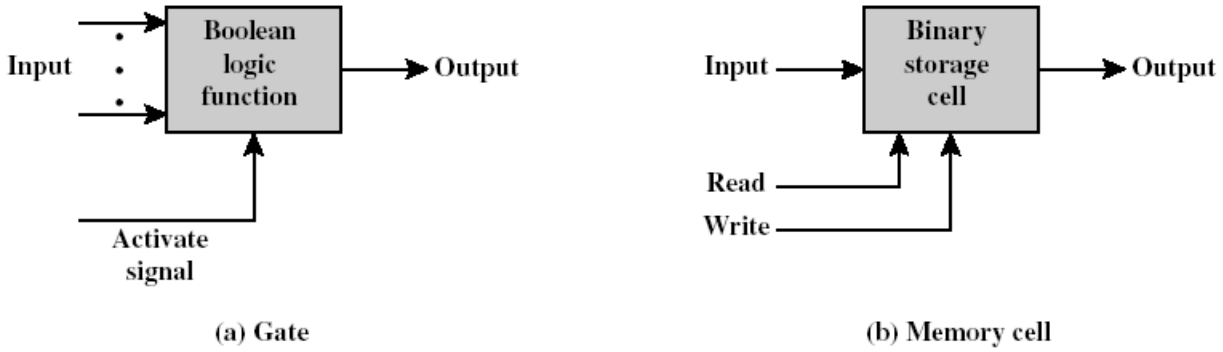
- Replaced vacuum tubes
- Smaller
- Cheaper
- Less heat dissipation
- Solid State device
- Made from Silicon (Sand)
- Invented 1947 at Bell Labs
- William Shockley et al.

Transistor Based Computers

- Second generation machines
- NCR & RCA produced small transistor machines
- IBM 7000
- DEC - 1957
  - Produced PDP-1

Microelectronics

- Literally - "small electronics"
- A computer is made up of gates, memory cells and interconnections
- These can be manufactured on a semiconductor
- e.g. silicon wafer



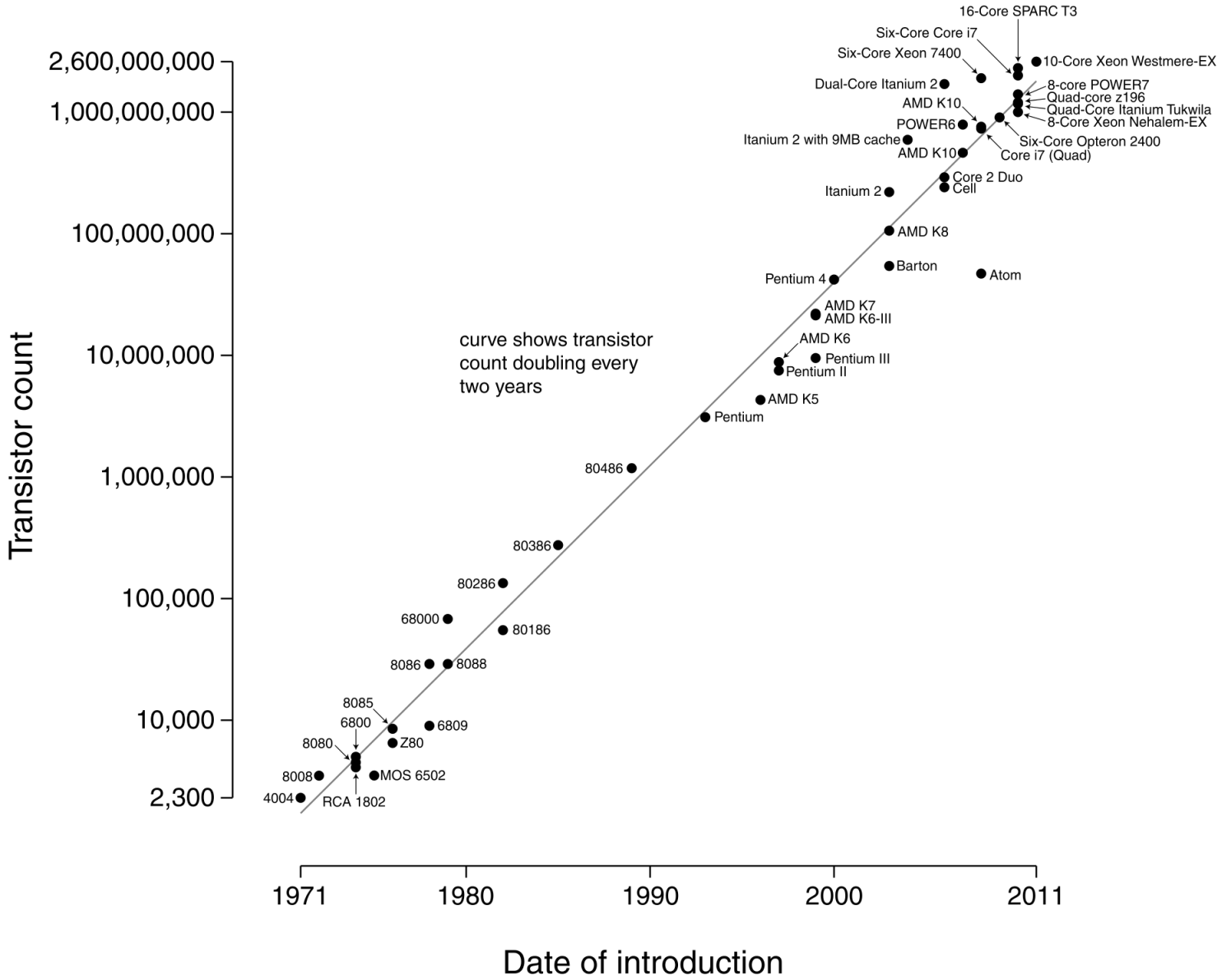
Generations of Computer

- Vacuum tube - 1946-1957
- Transistor - 1958-1964
- Small scale integration - 1965 on
  - —Up to 100 devices on a chip
- Medium scale integration - to 1971
  - —100-3,000 devices on a chip
- Large scale integration - 1971-1977
  - —3,000 - 100,000 devices on a chip
- Very large scale integration - 1978 to date
  - —100,000 - 100,000,000 devices on a chip
- Ultra large scale integration
  - —Over 100,000,000 devices on a chip

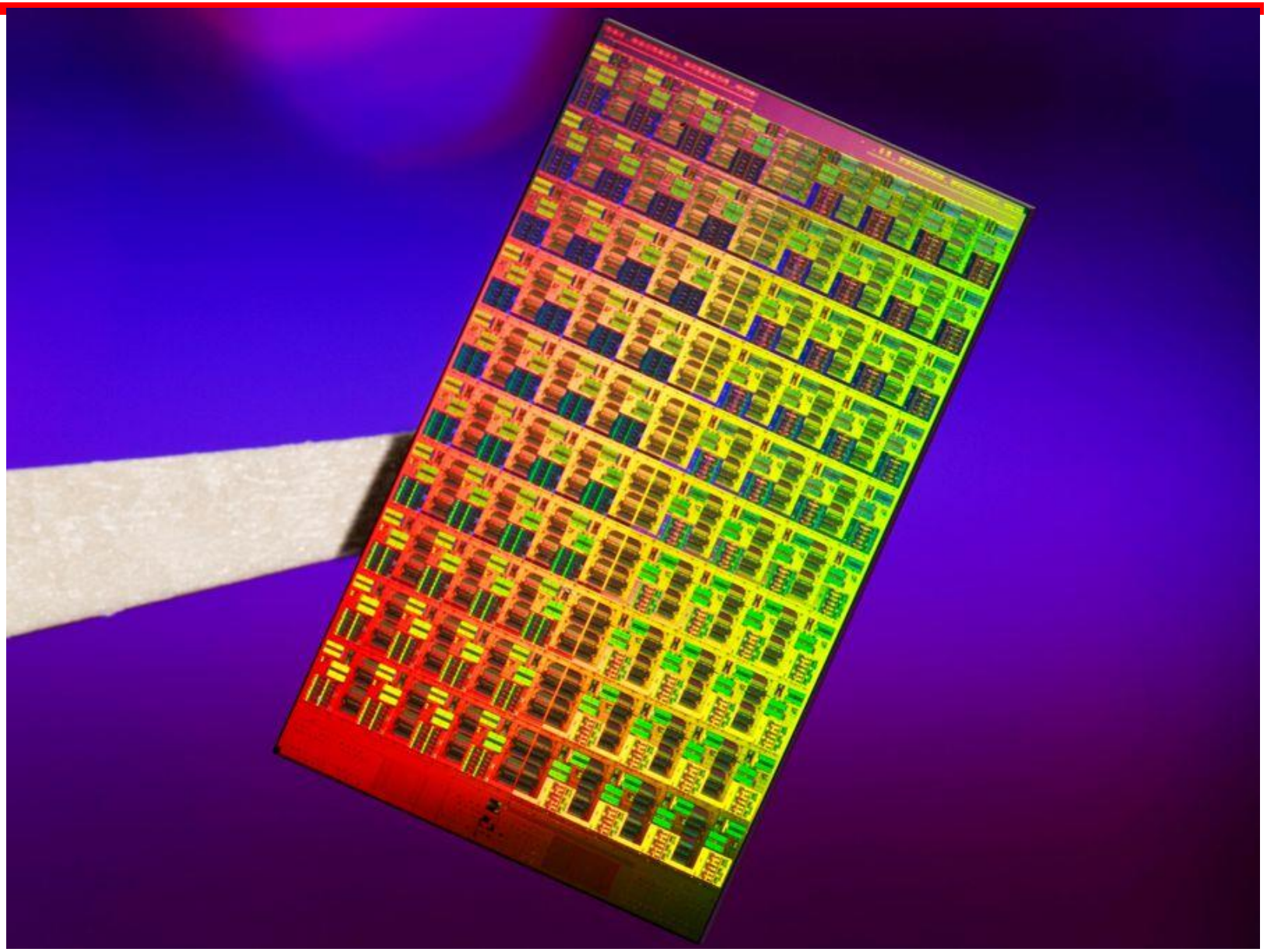
Moore's Law

- Increased density of components on chip
- Gordon Moore - cofounder of Intel
- Number of transistors on a chip will double every year
- Since 1970's development has slowed a little
  - Number of transistors doubles every 18 months
- Cost of a chip has remained almost unchanged
- Higher packing density means shorter electrical paths, giving higher performance
- Smaller size gives increased flexibility
- Reduced power and cooling requirements
- Fewer interconnections increases reliability

Growth in CPU Transistor Count



Intel Chip with 80 cores



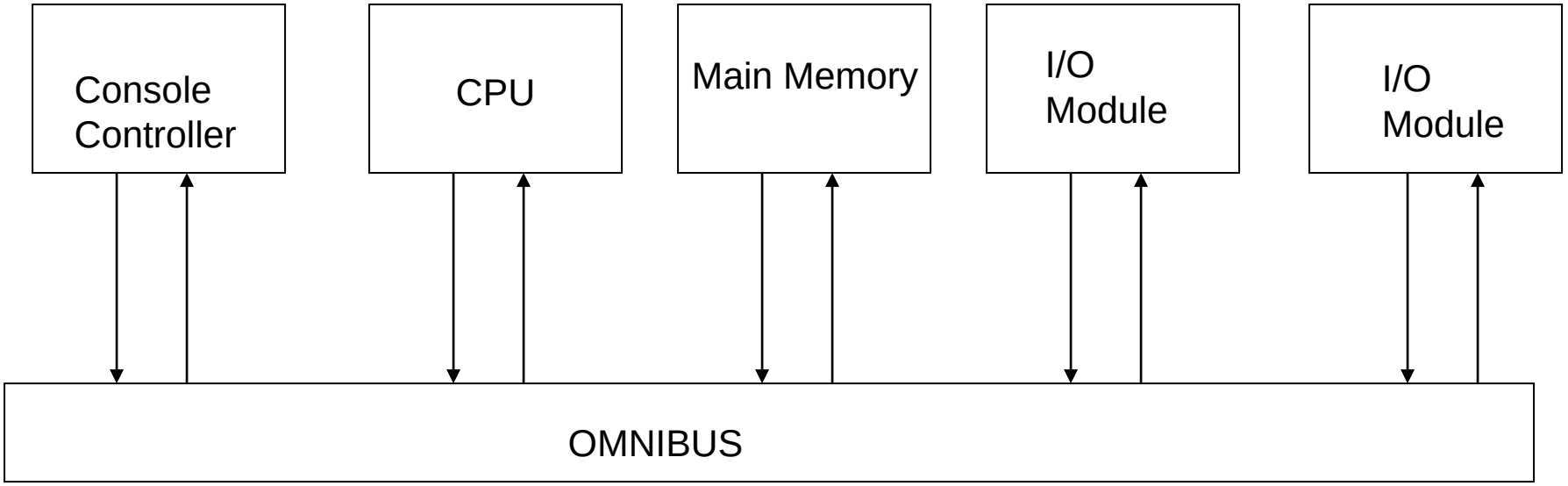
IBM 360 series

- 1964
- Replaced (& not compatible with) 7000 series
- First planned "family" of computers (See Table 2.4)
  - Similar or identical instruction sets
  - Similar or identical O/S
  - Increasing speed
  - Increasing number of I/O ports (i.e. more terminals)
  - Increased memory size
  - Increased cost
- Multiplexed switch structure (See Fig. 2.5)

DEC PDP-8

- 1964
- First minicomputer (after miniskirt!)
- Did not need air conditioned room
- Small enough to sit on a lab bench
- $16,000
  - $100k+ for IBM 360
- Embedded applications & OEM
- BUS STRUCTURE

DEC - PDP-8 Bus Structure



Semiconductor Memory

- 1970
- Fairchild
- Size of a single core
  - i.e. 1 bit of magnetic core storage
- Holds 256 bits
- Non-destructive read
- Much faster than core
- Capacity approximately doubles each year

Intel

- 1971 - 4004
  - —First microprocessor
  - —All CPU components on a single chip
  - —4 bit
- Followed in 1972 by 8008
  - —8 bit
  - —Both designed for specific applications
- 1974 - 8080
  - —Intel’s first general purpose microprocessor

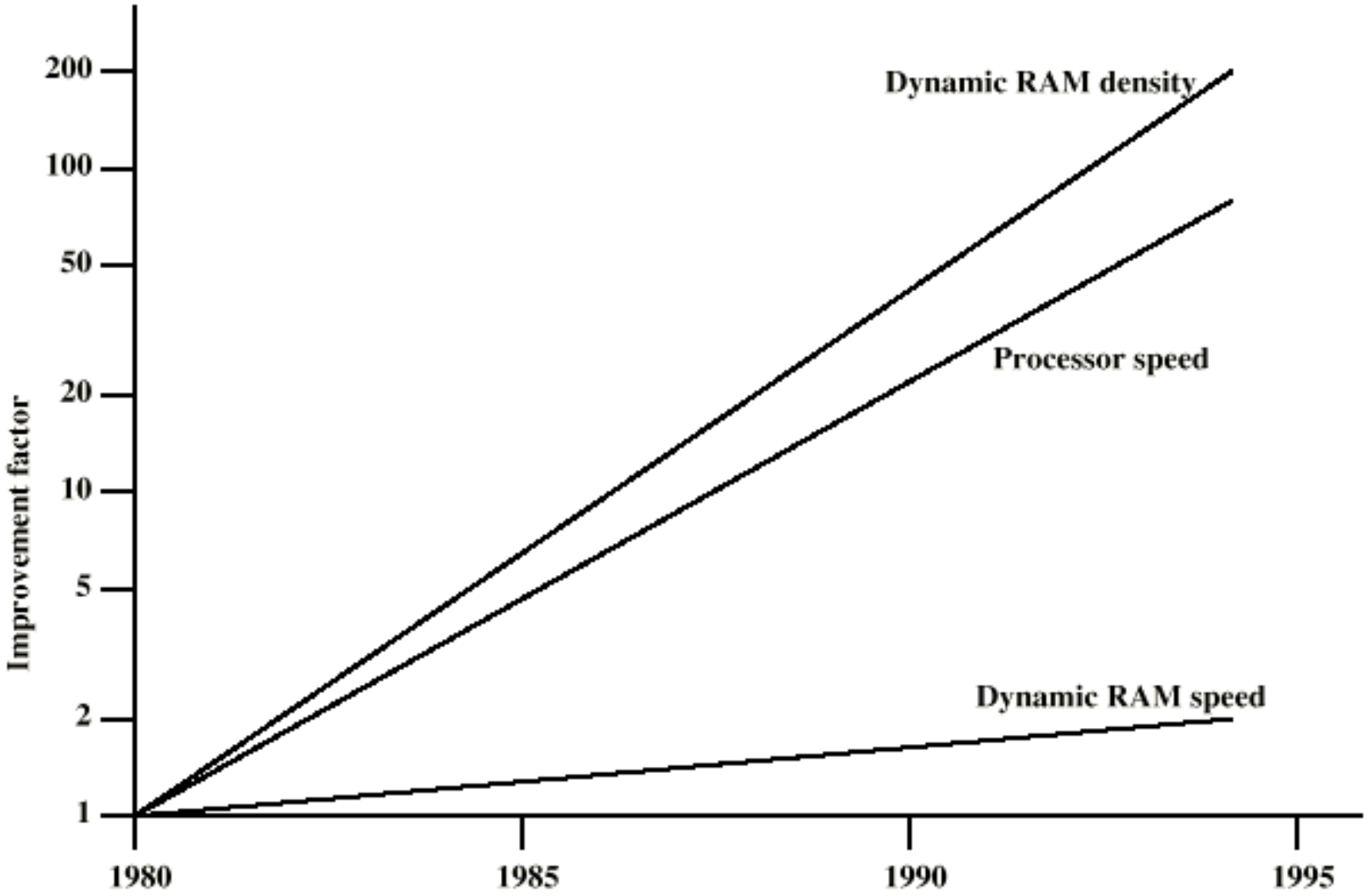
Speeding it up

- Pipelining
- On board cache
- On board L1 & L2 cache
- Branch prediction
- Data flow analysis
- Speculative execution

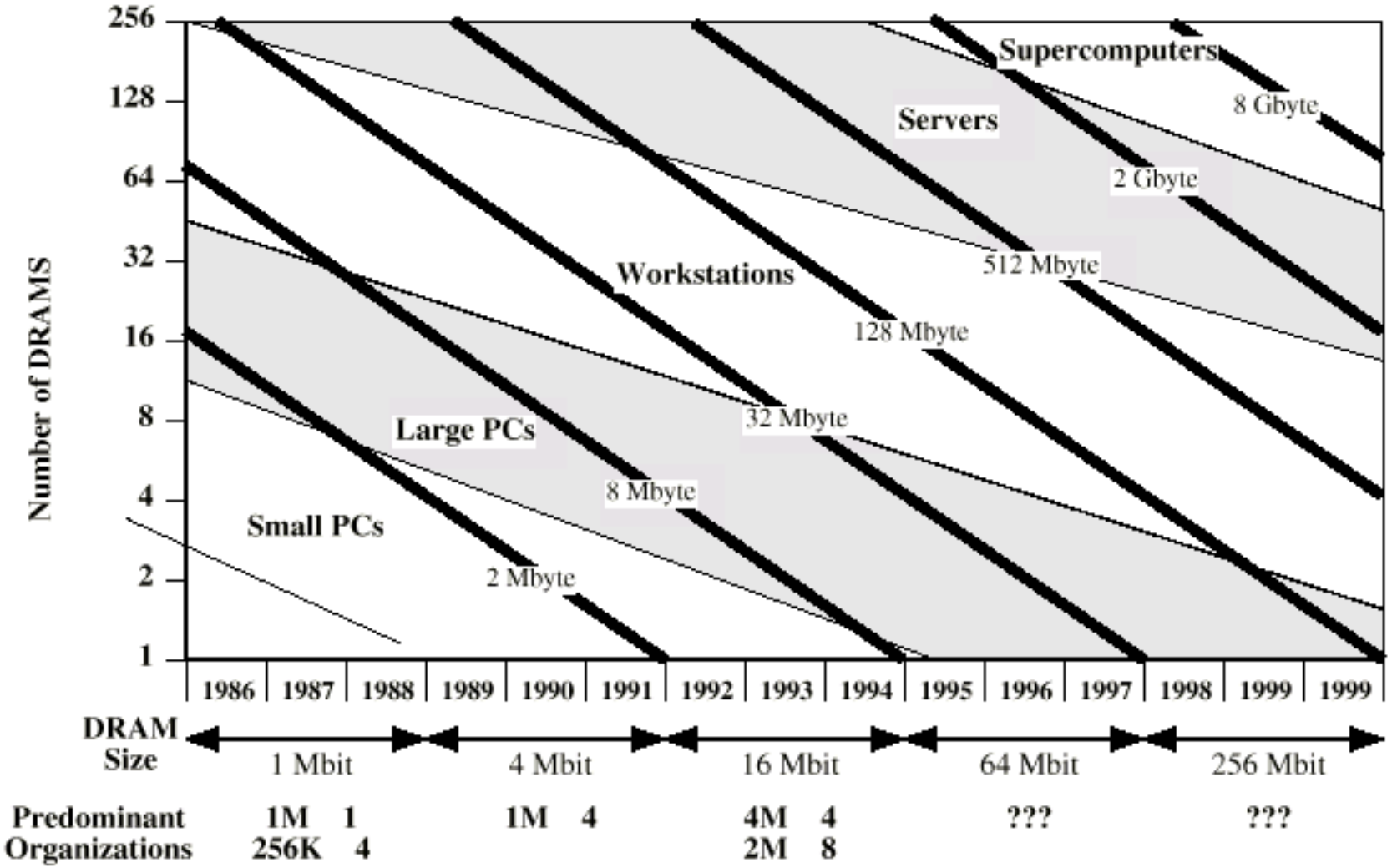
Performance Mismatch

- Processor speed increased
- Memory capacity increased
- Memory speed lags behind processor speed

DRAM and Processor Characteristics



Trends in DRAM use



Solutions

- Increase number of bits retrieved at one time
  - —Make DRAM “wider” rather than “deeper”
- Change DRAM interface
  - —Cache
- Reduce frequency of memory access
  - —More complex cache and cache on chip
- Increase interconnection bandwidth
  - —High speed buses
  - —Hierarchy of buses

Pentium Evolution (1)

- 8080
  - first general purpose microprocessor
  - 8 bit data path
  - Used in first personal computer – Altair
- 8086
  - much more powerful
  - 16 bit
  - instruction cache, prefetch few instructions
  - 8088 (8 bit external bus) used in first IBM PC
- 80286
  - 16 Mbyte memory addressable
  - up from 1Mb
- 80386
  - 32 bit
  - Support for multitasking

Pentium Evolution (2)

- 80486
  - —sophisticated powerful cache and instruction pipelining
  - —built in maths co-processor
- Pentium
  - —Superscalar
  - —Multiple instructions executed in parallel
- Pentium Pro
  - —Increased superscalar organization
  - —Aggressive register renaming
  - —branch prediction
  - —data flow analysis
  - —speculative execution

Pentium Evolution (3)

- Pentium II
  - —MMX technology
  - —graphics, video & audio processing
- Pentium III
  - —Additional floating point instructions for 3D graphics
- Pentium 4
  - —Note Arabic rather than Roman numerals
  - —Further floating point and multimedia enhancements
- Itanium
  - —64 bit

Internet Resources

- http://www.intel.com/
  - Search for the Intel Museum
- http://www.ibm.com
- http://www.dec.com
- Charles Babbage Institute
- PowerPC
- Intel Developer Home